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**Electric Field Engineering and Device Innovations for
High-Power β -Ga₂O₃ Electronics**

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy

in

Materials

by

Saurav Roy

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November 2024

Electric Field Engineering and Device Innovations for High-Power β -Ga₂O₃ Electronics

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by

Saurav Roy

Dedicated to the people who kept me going
when I wanted to give up.

“If I have seen further than others, it is by standing upon the shoulders of giants”

— Sir Isaac Newton

*“One shouldn’t work on semiconductors, that is a filthy mess; who knows whether
any semiconductors exist”*

— Wolfgang Pauli

“A mind needs books like a sword needs a whetstone”

— Tyrion Lannister

“‘I wish it need not have happened in my time,’ said Frodo.

*‘So do I,’ said Gandalf, ‘and so do all who live to see such times. But that is not for them to
decide. All we have to decide is what to do with the time that is given us.’”*

— J.R.R Tolkien

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I am deeply grateful to Jim, a mentor whose passion for science and profound knowledge of physics have been a guiding light throughout my Ph.D. journey. Jim's dedication to the field and his commitment to lifelong learning have been truly inspiring, setting a standard I aspire to. His constructive feedback and insightful suggestions have not only sharpened my research but elevated it, often in ways I hadn't initially considered. Coming from an Electrical Engineering background, I was initially unfamiliar with many aspects of Materials Science.

However, attending Jim's classes gave me a solid foundation in this field, thanks to his clear, thoughtful teaching style. His genuine curiosity and constant pursuit of new knowledge have left a lasting impression on me, and I greatly admire the example he sets as a scientist and mentor.

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- Demonstration of first **In-situ MOCVD Al₂O₃** on β -Ga₂O₃ for reduced interface traps and higher reliability.
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Patent

-
- [1] **Saurav Roy** and Sriram Krishnamoorthy, “Low Barrier Height RESURF Structure for Efficient Power Diodes” (Patent filed)

JOURNAL PUBLICATIONS (SELECT)

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- [1] **Saurav Roy**, Arkka Bhattacharyya, Carl Peterson and Sriram Krishnamoorthy. "Dielectric Reliability and Interface Trap Characterization in MOCVD grown In-situ Al_2O_3 on $\beta\text{-Ga}_2\text{O}_3$." Under review in *Applied Physics Letters* (Minor revision submitted)
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- [1] **Saurav Roy**, A. Bhattacharyya, Jacqueline Cooke, C. Peterson, Berardi Sensale Rodriguez and S. Krishnamoorthy. "Large Area Trench β -Ga₂O₃ Schottky Barrier Diode with Extreme-K Dielectric Resurf" In *6th US Workshop on Gallium Oxide (GOX 2023)*. (Oral Presentation)
- [2] **Saurav Roy**, A. Bhattacharyya, C. Peterson and S. Krishnamoorthy. "Dielectric Lifetime Enhancement of in-situ MOCVD Al₂O₃ on β -Ga₂O₃ Using Temperature Modulated Deposition" In *6th US Workshop on Gallium Oxide (GOX 2023)*. (Poster Presentation): **(Best Poster Award: GOX 2023)**
- [3] **Saurav Roy**, A. Bhattacharyya, Jacqueline Cooke, C. Peterson, Berardi Sensale Rodriguez and S. Krishnamoorthy. "First Demonstration of 15A/1.4 kV Large Area Trench β -Ga₂O₃ Schottky Barrier Diode with High-k RESURF" In *81st Device Research Conference (DRC 2023)*. (Oral Presentation)
- [4] **Saurav Roy**, B. Kostroun, Y. Liu, J. Cooke, A. Bhattacharyya, C. Peterson, B. S. Rodriguez and S. Krishnamoorthy. "Low Loss Ampere Class High Voltage β -Ga₂O₃ Vertical Schottky Barrier Diodes" In *Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD 2024)* Las Vegas, Nevada. **(Invited)**
- [5] **Saurav Roy**, A. Bhattacharyya, C. Peterson and S. Krishnamoorthy. "Enhancing the Dielectric Performance of Al₂O₃ on β -Ga₂O₃ using Temperature Modulated In-situ Dielectric Deposition" In *65th Electronic Materials Conference (EMC 2023)*. (Oral Presentation)
- [6] **Saurav Roy**, A. Bhattacharyya, C. Peterson and S. Krishnamoorthy. "High Voltage β -Ga₂O₃ Lateral Schottky barrier diode with High Permittivity Dielectric RESURF demonstrating >1 GW/cm² Power Figure of Merit" In *80th Device Research Conference (DRC 2022)*. (Oral Presentation)
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- [9] **Saurav Roy**, A. Bhattacharyya, C. Peterson and S. Krishnamoorthy, "Demonstration of Superjunction-like High-k Oxide/ β -Ga₂O₃ Lateral Schottky barrier diode with More Than 1 GW/cm² Power Figure of Merit" In *International Workshop on Gallium Oxide (IWGO 2022)*. (Oral Presentation)
- [10] **Saurav Roy**, A. Bhattacharyya, C. Peterson and S. Krishnamoorthy, " β -Ga₂O₃ Dielectric Superjunction Schottky Barrier Diode Exceeding SiC Unipolar Figure of Merit: A Novel Approach to Realizing Superjunction Devices Without p-Type Doping" In *6th IEEE International Conference on Emerging Electronics (ICEE 2022)*. (Oral Presentation)
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- [14] **Saurav Roy**, A. Bhattacharyya, P. Ranga, H. Splawn, J. Leach, and S. Krishnamoorthy, “Record High BFOM (1.47 GW/cm²) Field-Plated Vertical (001) β -Ga₂O₃ Schottky Barrier Diode with Surface Breakdown Field of 5.45 MV/cm”, In *79th Device Research Conference (DRC 2021)*. (Oral Presentation)
- [15] **Saurav Roy**, A. Bhattacharyya, P. Ranga, H. Splawn, J. Leach, and S. Krishnamoorthy, “Demonstration of High-Permittivity Oxide Field Plated Vertical β -Ga₂O₃ Schottky Barrier Diode with Very High Edge Termination Efficiency”, In *Lester Eastman Conference (LEC 2021)*. (Oral Presentation)
- [16] **Saurav Roy**, A. Bhattacharyya, and S. Krishnamoorthy, “Design and Simulation of β -Ga₂O₃ Schottky Barrier Diode with p-type III-Nitride Guard Ring for Enhanced Breakdown”, In *78th Device Research Conference (DRC 2020)*. (Oral Presentation)
- [17] **Saurav Roy**, A. Bhattacharyya, and S. Krishnamoorthy, “Improving the BV-R_{on} trade-off of β -Ga₂O₃ vertical Schottky barrier diode Using Dielectric Superjunction”, In *78th Device Research Conference (DRC 2020)*. (Poster)

Abstract

Electric Field Engineering and Device Innovations for High-Power β -Ga₂O₃ Electronics

by

Saurav Roy

This dissertation embarks on a comprehensive exploration of electric field management strategies and dielectric engineering techniques tailored to overcome intrinsic challenges in β -Ga₂O₃ power devices, particularly focusing on high-voltage applications where wide- and ultra-wide-bandgap semiconductors have a distinct edge over silicon. With the introduction of wide-bandgap materials such as SiC and GaN, and now ultra-wide-bandgap β -Ga₂O₃, there exists an opportunity to achieve unprecedented efficiencies in power electronics, thanks to these materials' higher breakdown fields and better thermal stability. However, to fully harness the potential of β -Ga₂O₃, this dissertation addresses the unique challenges that arise from its lack of viable p-type doping. By proposing novel dielectric-assisted design methodologies, this work makes significant strides in establishing β -Ga₂O₃ as a viable solution for future high-power, high-voltage applications.

In the first section, the focus is on β -Ga₂O₃ Schottky barrier diodes (SBDs) and the development of advanced field management strategies using high-permittivity (κ) dielectric materials. High-permittivity dielectrics are introduced as field plate oxides to mitigate edge field crowding and to control the electric field at the metal/semiconductor interface. This design enables the SBDs to achieve a power figure of merit (FOM) of 1.34 GW/cm², demonstrating the efficacy of high- κ dielectric-assisted RESURF (reduced surface field) designs for managing leakage currents—an essential consideration for devices operating in the kilovolt regime. By creating a trench SBD structure that integrates both high- and low-work-function anode contacts, significant reductions in leakage current and improved breakdown voltages are achieved. The low

work-function anode contact, in particular, demonstrates a breakdown voltage exceeding 3 kV while maintaining a low turn-on voltage of just 0.5 V, which positions it as a promising candidate for high-power applications, rivaling and, in certain parameters, surpassing commercial bare-die SiC SBDs.

The work further pioneers the concept of a dielectric superjunction, which emulates the charge-balancing benefits of a traditional p/n superjunction without the requirement for p-type doping and associated stringent charge balance. By leveraging high- κ dielectric materials, a lateral dielectric superjunction device is realized with a figure of merit of 1.47 GW/cm² along with a higher doped channel ($N_D = 3 \times 10^{17} \text{ cm}^{-3}$) for lowered on-resistance, showcasing the potential of this dielectric-based approach to circumvent the intrinsic limitations of β -Ga₂O₃. The dielectric superjunction structure also simplifies the design process by eliminating the need for precise charge balancing, a common and challenging constraint in traditional superjunction structures. This proof-of-concept device opens pathways for scaling up and further refining superjunction devices for vertical implementations in high-power electronics.

In the latter half, the dissertation transitions to address the pressing need for advanced β -Ga₂O₃ vertical transistor architectures, where conventional lateral designs fall short due to limited current handling capability and surface field-handling issues. A key contribution here is the development of an in-situ dielectric deposition technique using Metal-Organic Chemical Vapor Deposition (MOCVD) that enables pristine, low-defect density dielectric/semiconductor interfaces. This interface quality is critical for the reliable performance of gate dielectrics in power transistors, as impurities or defects at the interface can significantly impact device stability and operation under high electric fields. Detailed characterization of the dielectric properties and interface quality is conducted, revealing the improvements in breakdown voltage and reliability made possible through precise deposition conditions. The high-temperature MOCVD process also enhances the dielectric layer's density and crystallinity, further contributing to its breakdown robustness. By adjusting deposition conditions, the dielectric's lifetime and stability are optimized, establishing a foundation for the deployment of these dielectrics in high-power

β -Ga₂O₃ transistors.

The culmination of this work is the demonstration of a normally-off vertical β -Ga₂O₃ fin transistor, achieving a breakdown voltage over 1 kV, which represents a significant advancement toward viable power transistors in this material. This device, designed without the need for p-type doping, leverages geometric design techniques to effectively manage electric fields and provide enhancement mode operation. Further refinements to edge termination and alternative transistor structures are explored, with capacitance measurements verifying their improved switching performance. This study underscores the importance of novel transistor designs in pushing the boundaries of β -Ga₂O₃ technology, particularly for high-voltage applications where traditional device designs cannot accommodate the material's limitations.

In conclusion, this dissertation offers an innovative perspective on β -Ga₂O₃ device engineering, demonstrating that while p-type doping is advantageous in wide-bandgap devices, it is not a necessity for high-performance β -Ga₂O₃ power electronics. Instead, high- κ dielectric materials emerge as a promising alternative for electric field management, mitigating leakage currents and optimizing breakdown performance without the complexities associated with p-type doping. Through the use of high- κ dielectric materials and alternative electric field management techniques, the intrinsic challenges of β -Ga₂O₃ are addressed, showcasing the material's potential as a disruptive technology in power electronics.

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Chapter 1

Introduction

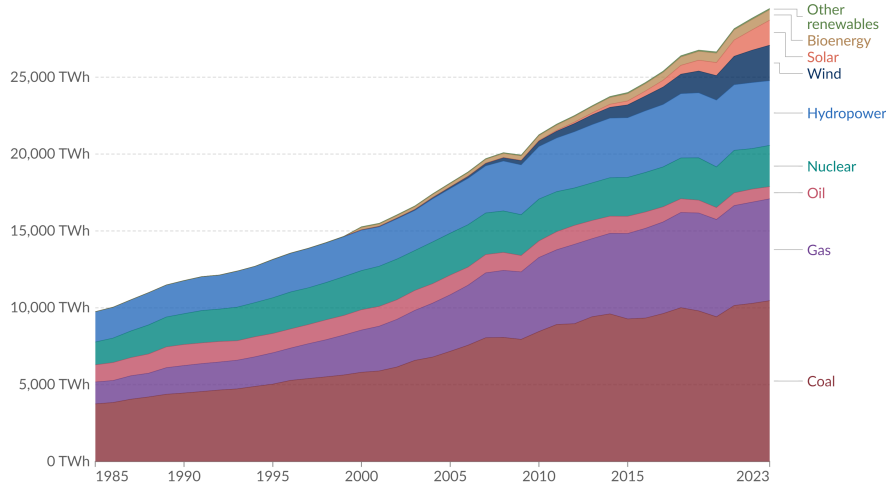
Electricity has emerged as the most indispensable form of energy, playing a central role in powering modern society. It is produced through a combination of non-renewable sources, such as fossil fuels, and renewable sources, including solar, wind, and hydroelectric power as shown in Fig. 1.1 [1]. Currently, electricity generation and consumption account for a significant 40% of the global energy demand, highlighting its critical importance in meeting the world's energy needs.

However, the growing reliance on electricity has also intensified concerns about its environmental impact, particularly its contribution to climate change. The relationship between energy consumption and climate change has become increasingly apparent, prompting urgent calls for substantial decarbonization in both energy production and usage. This shift is crucial to mitigate the adverse effects of climate change and move towards a more sustainable energy future.

In response to these challenges, there is a rising demand for renewable energy sources, energy storage systems, and electric transportation solutions, all of which are essential for reducing carbon dioxide emissions. These emerging technologies are not only reshaping the energy landscape but also creating new demands for medium to high-voltage (MV/HV) power conversion systems. These systems have become pivotal in interfacing with the utility grid, ensuring efficient and cost-effective integration of renewable energy sources.

Electricity production by source, World

Measured in terawatt-hours¹.



Data source: Ember (2024); Energy Institute - Statistical Review of World Energy (2024)

OurWorldinData.org/energy | CC BY

Note: "Other renewables" include waste, geothermal, wave, and tidal.

1. Watt-hour: A watt-hour is the energy delivered by one watt of power for one hour. Since one watt is equivalent to one joule per second, a watt-hour is equivalent to 3600 joules of energy. Metric prefixes are used for multiples of the unit, usually: - kilowatt-hours (kWh), or a thousand watt-hours. - Megawatt-hours (MWh), or a million watt-hours. - Gigawatt-hours (GWh), or a billion watt-hours. - Terawatt-hours (TWh), or a trillion watt-hours.

Figure 1.1: Cumulative global electricity production by source over the last 38 years [1].

For instance, the growing adoption of electric vehicle (EV) supercharger stations, photovoltaic (PV) systems, and wind and solar farms increasingly necessitates connection to the MV/HV grid through advanced power conversion systems. This trend underscores the importance of MV/HV power conversion as a key component in the transition to a low-carbon energy system.

1.1 Power Electronics

Power electronics, as defined by Thomas G. Wilson, is the technology focused on the efficient conversion, control, and conditioning of electric power using static devices to transform it from its input form to the desired output form. The primary objective of power electronics is to achieve power conversion between an electrical source and an electrical load in a manner that is highly efficient, reliable, and cost-effective. Whether in renewable energy systems, electric vehicles, industrial automation, or consumer electronics, power electronics plays a pivotal role

in shaping the generation, distribution, and utilization of energy. As the world increasingly moves toward sustainable and efficient energy solutions, the significance of power electronics grows, spurring innovation and expanding the horizons of technological possibilities.

Power electronics has experienced rapid technological advancements in recent years, with its applications rapidly expanding across industrial, commercial, residential, and power utility sectors. Innovations in power semiconductor technology and microprocessor control have enabled the widespread use of power electronics systems in various areas, including industrial motor drives, transportation, energy storage systems, power quality management, switch-mode power supplies, high-voltage direct current (HVDC) transmission systems, and flexible alternating current transmission systems (FACTS). Additionally, power electronics is breaking new ground in emerging fields with significant growth potential, such as lighting and medical devices, including mobile X-ray systems. This dynamic field integrates the principles of electric power, electronics, and control, driving progress across multiple industries.

Power conversion involves several methods, each tailored to specific needs based on the type of electric power being converted and the direction of power flow. Power converters are categorized according to their function and the nature of the conversion they perform. These categories include:

1. **dc-dc converters:** These converters adjust a direct current (DC) voltage from one level and polarity to another DC voltage of a different level and, in some cases, a different polarity. They are essential for applications requiring precise voltage regulation and transformation within DC systems.
2. **dc-ac converters:** Also known as inverters, these devices convert a DC voltage or current source into an alternating current (AC) voltage or current. They can produce either single-phase or three-phase AC outputs, making them crucial for integrating DC sources, such as solar panels or batteries, into AC power systems.
3. **ac-dc converters:** These devices, often referred to as rectifiers, transform a single-phase

or three-phase AC voltage into DC. They are fundamental in applications where AC power needs to be converted to DC for use in various electronic devices and systems.

4. **ac-ac cycloconverters:** Cycloconverters convert an AC voltage of one level, frequency, and number of phases to an AC voltage of a different level, frequency, and, in some cases, a different number of phases. They are used in specialized applications that require direct conversion between AC power sources of differing characteristics.

Power converters consist of various components, including both active and passive elements. Active devices such as semiconductor diodes, thyristors, and transistors, along with passive devices like resistors, capacitors, and inductors, form the discrete components of power converters. To enhance power density and reliability, multiple power semiconductor devices are often integrated into power modules. These modules are created by soldering or sintering the devices onto a power electronic substrate, offering improved performance compared to using discrete components alone.

The performance of power converters hinges on the efficiency, reliability, controllability, and cost-effectiveness of the semiconductor devices used within them. These four attributes are crucial for the economic viability of any new device structure or material. Over the years, various new materials and device designs have been explored as potential successors to silicon (Si). Some have achieved commercial success, while others have remained niche solutions with limited acceptance.

In the next section, we will compare Silicon (Si), Silicon Carbide (SiC), and Gallium Nitride (GaN) and emerging Ultra-wide bandgap (UWBG) materials as the leading platform candidates poised to dominate the next generation of power devices.

1.2 Wide and Ultra-wide Bandgap Materials for Power Semiconductor Devices

Silicon-based devices have dominated power electronics for many decades for these applications with innovations in device architecture pushing power limits higher between generations from metal-oxide field effect transistors (MOSFETs) [2] to insulated gate bipolar transistors (IGBTs) [3] and superjunction transistors [4]. As the demand for higher frequency and higher voltage switching increases, the fundamental materials limits of Si are reached. The deployment of wide-bandgap (WBG) semiconductor materials in power devices marks a significant step forward in creating lighter, smaller, and more efficient power electronics systems. Compared to traditional silicon devices, Silicon Carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) and Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) offer notable advantages in several key areas, including electrical breakdown field, thermal conductivity, electron saturation velocity, and radiation tolerance [5].

One of the key advantages of Silicon Carbide (SiC) and Gallium Nitride (GaN) over traditional silicon in power semiconductor devices is their higher critical electric field (2.4 MV/cm for SiC and 3.3 MV/cm for GaN compared to 0.2 MV/cm for Si)[6], which scales superlinearly with bandgap. This characteristic enables the use of a thinner drift layer with higher doping concentrations while still blocking the same voltage. This reduction in drift layer thickness, combined with increased doping, results in lower on-resistance compared to comparable silicon based switches, enhancing the overall efficiency of the device. Additionally, these WBG devices can sustain higher operating temperatures. For instance, SiC devices can typically maintain operating temperatures that are, on average, 25 °C higher than those of silicon, making them highly attractive for a wide range of demanding applications.

Another major reason industries are adopting wide-bandgap (WBG) technologies is the ability to reduce the size of power converters. Power converters typically draw energy from an input source, store it in passive elements like capacitors and inductors, and then deliver

it continuously and repetitively to the output load. The rate at which these energy transfers occur per second is called the switching frequency. WBG-based devices, with their smaller size, exhibit lower device capacitances, enabling higher switching frequencies. This increase in switching frequency allows for smaller energy storage components without sacrificing power transfer efficiency. As a result, the overall system becomes more compact and less complex, while performance is enhanced.

Ultra-wide bandgap (UWBG) semiconductors represent the next frontier in power semiconductor materials, characterized by bandgaps exceeding 4 eV. Transitioning to UWBG semiconductors offers significant advantages at both the device and system levels, including improvements in size, weight, and power (SWaP) efficiency. These enhancements lead to reductions in conduction and switching losses, making UWBG materials highly attractive for advanced power electronics. β -Ga₂O₃ ($E_G=4.6\text{eV}$), Diamond ($E_G=5.5\text{eV}$), and AlN ($E_G=6.2\text{eV}$) are promising UWBG material candidates. With their larger bandgaps, UWBG materials demonstrate exceptional potential in applications demanding extreme operating conditions, such as high voltage, high frequency, high temperature, and radiation-intensive environments.

Among the UWBG materials, β -Ga₂O₃ stands out for offering several unique benefits, including the availability of bulk substrates, shallow hydrogenic dopants, relatively mature device fabrication techniques, and a broad range of epitaxial growth methods. These advantages make β -Ga₂O₃ particularly attractive for commercial and large-scale applications. Table 1 provides a comparison of the material properties of various WBG and UWBG semiconductors. In the next section, we will briefly discuss the key material properties and advantages of β -Ga₂O₃.

1.3 β -Ga₂O₃ Material Properties

Among the many different polytypes of Ga₂O₃, the monoclinic β phase is the most stable one. Figure 1.2 illustrates the crystal structure of monoclinic β -Ga₂O₃ (space group C_{2v}^m) with the

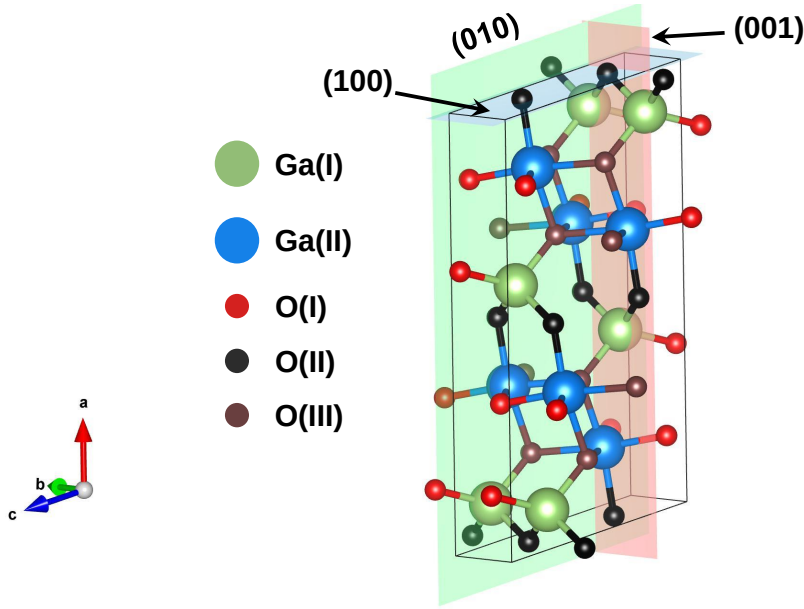


Figure 1.2: β -Ga₂O₃ monoclinic crystal structure showing three major planes drawn using VESTA [7]. In this structure, Ga(I) represents the tetrahedrally coordinated Ga site, while Ga(II) represents the octahedrally coordinated Ga site where O(I) and O(II) are twofold coordinated and O(III) is threefold coordinated Oxygen sites.

unique b-axis and a β angle of 103.7° . The conventional unit cell comprises 20 atoms, while the primitive cell contains 10 atoms. In this structure as shown in Fig. 1.2, the oxygen sites are not equivalent: two of them have threefold coordination, and one has fourfold coordination. The gallium atoms are classified into two types: tetrahedrally coordinated Ga(I) and octahedrally coordinated Ga(II). The anisotropy of the monoclinic β -Ga₂O₃ structure results in significant differences in the material's properties across its principal planes, influencing its electronic, optical, and thermal characteristics.

A significant advantage of β -Ga₂O₃ is the availability of high-quality, large-area native substrates with very low dislocation densities, which are produced using various melt-growth techniques such as Edge-Defined-Film-Fed Growth (EFG) [8], Czochralski (CZ) [9], Float Zone [10] Vertical Bridgman (VB) [11]. This contrasts sharply with materials like Diamond and AlN, as well as other wide-bandgap (WBG) materials like GaN and SiC, where the native substrate growth is more costly and limited in scale. The EFG technique, a primary method for bulk substrate growth, involves pulling a β -Ga₂O₃ slab congruently from a melt. Due to the cleavage

planes in the [010] zone, the [010] direction is commonly used for pulling, which limits the area of (010) oriented substrates but allows for the scalable production of other orientations such as (100), (001), and ($\bar{2}01$), with 6-inch substrates already demonstrated using Vertical Bridgman (VB) method [12]. Additionally, CZ techniques are being developed for β -Ga₂O₃, with 2-inch substrates in the (010) orientation already achieved [13]. These bulk substrates serve as excellent platforms for the epitaxial growth of β -Ga₂O₃, and extended defects in β -Ga₂O₃ bulk substrates have been reduced to below 10^4 cm^{-2} , a significant improvement over other WBG and UWBG semiconductors.

Doping is a critical technology for tailoring the properties of semiconductors and enabling the design of various electronic devices. For β -Ga₂O₃, several n-type dopants—such as Silicon (Si), Tin (Sn), and Germanium (Ge)—have been successfully demonstrated, showcasing its potential for high-performance electron devices [14]. Notably, β -Ga₂O₃ is unique among ultra-wide bandgap (UWBG) materials in that it supports shallow hydrogenic n-type dopants, which contribute to low on-resistance and high breakdown voltage.

However, p-type doping in β -Ga₂O₃ remains challenging due to issues such as negligible valence band dispersion, strong hole self-localization, and high acceptor ionization energies. Despite these challenges, deep acceptor dopants like Iron (Fe) [15], Magnesium (Mg) [16], and Nitrogen (N) [17] have been utilized to create semi-insulating regions, substrates, and current-blocking layers in electron devices [18]–[20]. These approaches enhance the functionality of β -Ga₂O₃-based devices and highlight the material’s versatility in various applications.

β -Ga₂O₃ also benefits from relatively mature epitaxial growth techniques compared to other UWBG materials. Established methods such as Metal-Organic Chemical Vapor Deposition (MOCVD), Molecular Beam Epitaxy (MBE), and Halide Vapor Phase Epitaxy (HVPE) have been effectively adapted for β -Ga₂O₃, enabling high-quality thin films and heterostructures to be grown with precision. These well-developed techniques facilitate the utilization of β -Ga₂O₃ into various electronic devices, contributing to its growing prominence in power electronics and other advanced applications.

The HVPE technique is particularly valued for the fabrication of thick drift layers at high growth rates, essential for vertical power devices. MOCVD has demonstrated the ability to produce highly pure, high-quality β -Ga₂O₃ materials, and is also used to explore advanced doping strategies such as delta doping and modulation doping. Additionally, MOCVD enables the formation of heterostructures with β -Ga₂O₃ alloys and in-situ dielectric deposition, further expanding its versatility. MBE offers highly controlled growth of β -Ga₂O₃, with the added benefit of in-situ characterization during deposition. Both delta and modulation doping have been successfully implemented using MBE, which allows for precise control over doping profiles. Furthermore, MBE and MOCVD have demonstrated Ga-flux-based etching of β -Ga₂O₃, enabling low-damage etching that is crucial for device fabrication [21], [22].

The device fabrication technology for β -Ga₂O₃ is relatively mature compared to other UWBG materials, and many techniques developed for GaN device fabrication can be easily adapted for use with β -Ga₂O₃. One significant advantage is the availability of anisotropic wet etching using hot phosphoric acid, which offers a less damaging alternative to more aggressive dry etching methods [23], [24]. This can be crucial for achieving damage-free or minimally damaged surfaces, enhancing device performance and reliability.

β -Ga₂O₃ stands out as a unique material among all the UWBG materials due to its numerous advantages, including mature bulk substrate growth, advanced epitaxial techniques, and established device fabrication processes. Continued research in these areas is driving the material and its associated technologies toward greater maturity, enhancing its potential for widespread use. The rapid progress in β -Ga₂O₃ development positions it as one of the most promising candidates for the next generation of power electronic materials, offering significant performance benefits for high-voltage, high-temperature, and high-frequency applications.

1.4 Power Devices

1.4.1 Ideal Power devices

An ideal power device should be capable of controlling power flow to various types of loads with zero power dissipation. These loads may be inductive (such as motors and solenoids), resistive (like heaters and lamp filaments), or capacitive (such as transducers and LCD displays). Typically, power is delivered to a load by periodically switching a power device on and off, generating pulses of current that are regulated by a control circuit. The ideal waveforms of the power delivered through a power switch are shown in Fig. 1.3.

During each switching cycle, the switch remains on for a duration up to t_{ON} , and remains off for the remainder of the period T . For an ideal power switch, the voltage drop during the on-state is zero, leading to no power dissipation. Similarly, during the off-state, the leakage current is zero, also resulting in no power loss. In this ideal picture, it is assumed that the transitions between the on-state and off-state occur instantaneously, ensuring no power loss during switching.

Power devices can be broadly categorized into two major classes: rectifiers (such as diodes) and switches (such as transistors). A rectifier allows current to flow in only one direction and blocks current flow in the opposite direction, making it useful for converting AC to DC. On the other hand, a power switch, controlled via a third terminal, regulates the flow of current. When the switch is in the on-state, current can flow freely, while no current flows when the switch is in the off-state.

Power Rectifiers

Rectifiers are essential components in power electronics, responsible for converting alternating current (AC) to direct current (DC). The most common types of rectifiers are diodes. Diodes, in turn, can be classified into two main types: pn diodes and Schottky diodes.

A pn diode is typically formed by creating a junction between two regions of a semiconductor

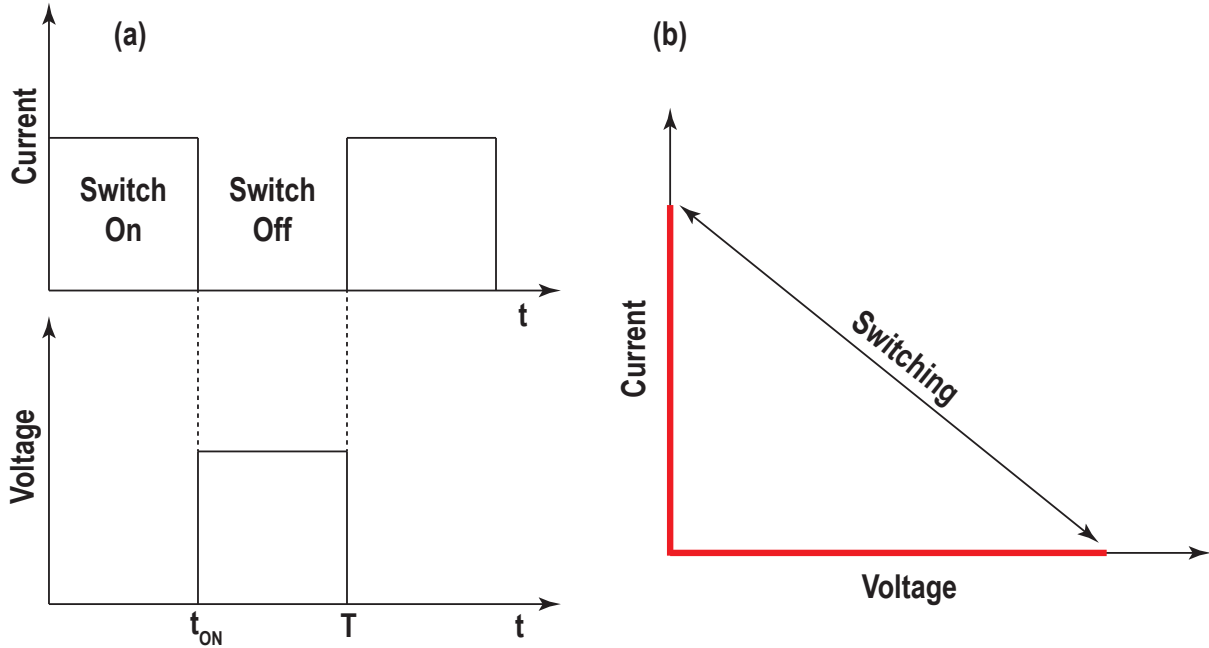


Figure 1.3: (a) Switching waveforms of an ideal power device. (b) Current-voltage characteristics of an ideal power switch.

with opposite types of charge carriers—electrons in the n-type region and holes in the p-type region. This junction can be made using the same semiconductor material (homojunction) or different materials (heterojunction). At the pn junction, an energy barrier arises due to the diffusion of charge carriers, creating a depletion region that limits the flow of current in one direction. The pn junction diode is considered a bipolar device because both types of charge carriers, electrons and holes, participate in current conduction.

In contrast, a Schottky diode is formed by the junction of a metal and a semiconductor, where an energy barrier is created due to the difference in work function between the metal and the semiconductor. Unlike pn diodes, Schottky diodes are unipolar devices, meaning that only one type of charge carrier (typically electrons) is responsible for current flow. Schottky diodes are known for their faster switching speeds and lower forward voltage drop compared to pn diodes, making them ideal for high-frequency and high-efficiency applications.

Thyristors are a class of power semiconductor devices that serve as controlled rectifiers, used primarily in high-power applications. Structurally, a thyristor consists of four alternating layers

of p-type and n-type semiconductor materials, forming three pn junctions. Unlike diodes, which conduct automatically when forward biased, thyristors require a triggering signal at their gate terminal to switch from an off-state (blocking mode) to an on-state (conducting mode). Once triggered, the thyristor continues to conduct until the current drops below a certain threshold, at which point it returns to the off-state. Hence thyristor behavior is more akin to a switch than a rectifier.

Thyristors are particularly useful in applications involving high-voltage or high-current control, such as motor drives, power conversion systems, and industrial machinery. Their ability to handle large amounts of power with minimal energy loss makes them essential in these environments. However, due to their relatively slow switching speeds compared to transistors, thyristors are typically used in low-frequency applications where high power handling is prioritized over switching speed. Variants of thyristors, such as silicon-controlled rectifiers (SCRs), gate turn-off thyristors (GTOs), and triacs, offer additional control and flexibility, enabling their use in a wide range of power electronics systems.

Power Switches

Power switches are semiconductor devices designed to regulate the flow of electrical current in power electronic systems by toggling between on and off states in response to a control signal. Two common types of power switches are Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and Insulated-Gate Bipolar Transistors (IGBTs).

Power MOSFETs are specifically engineered to handle high voltages and large currents, unlike their standard counterparts used in low-power circuits. They have three terminals: gate, drain, and source. The gate terminal controls the flow of current between the drain and source by applying a voltage that creates an electric field, modulating the device's conductivity. When the gate voltage surpasses a certain threshold, the MOSFET turns on, allowing current to flow with minimal resistance. If the gate voltage falls below this threshold, the MOSFET turns off, blocking current flow. A MOSFET essentially operates via unipolar conduction.

In contrast, IGBTs have three terminals: gate, emitter, and collector. IGBTs operate by applying a voltage to the gate, which generates an electric field that controls the current flow between the collector and emitter. The collector is composed of materials with opposite charge carriers compared to the low-doped drift region, creating an injection region. When the gate voltage exceeds a specific threshold, the IGBT turns on, enabling current to flow with a low on-state voltage drop. When the gate voltage is removed, the IGBT turns off, effectively blocking current flow. The IGBT combines high input impedance (similar to MOSFETs) with high current-handling capability (akin to BJTs), due to the injection of minority carriers from the collector. This makes IGBTs suitable for efficiently managing high voltages and large currents in power electronic systems.

1.4.2 Practical consideration for Power Semiconductor Devices

In real-world applications, power semiconductor devices face various non-idealities that significantly affect their performance. For instance, power diodes experience a small forward voltage drop during conduction, resulting in conduction losses. When operating in reverse, these diodes encounter reverse leakage current, which contributes to leakage power loss. Similarly, transistors exhibit on-state resistance during conduction, leading to on-state power losses. In the off-state, transistors also exhibit leakage currents, causing additional power dissipation, although this is generally negligible compared to other power losses. Typically, conduction losses tend to increase as the reverse blocking voltage rises, highlighting the importance of optimizing device design for improved efficiency. A diagram illustrating the current-voltage characteristics of practical diodes and transistors is shown in Fig. 1.4.

Beyond these static losses, power devices require a finite switching time when transitioning between the on-state and off-state, resulting in switching losses during both turn-on and turn-off events. These non-idealities collectively affect the efficiency and thermal performance of power electronic systems, making them key factors in device design and system optimization.

Unipolar and majority-carrier devices, particularly those based on WBG or UWBG semi-

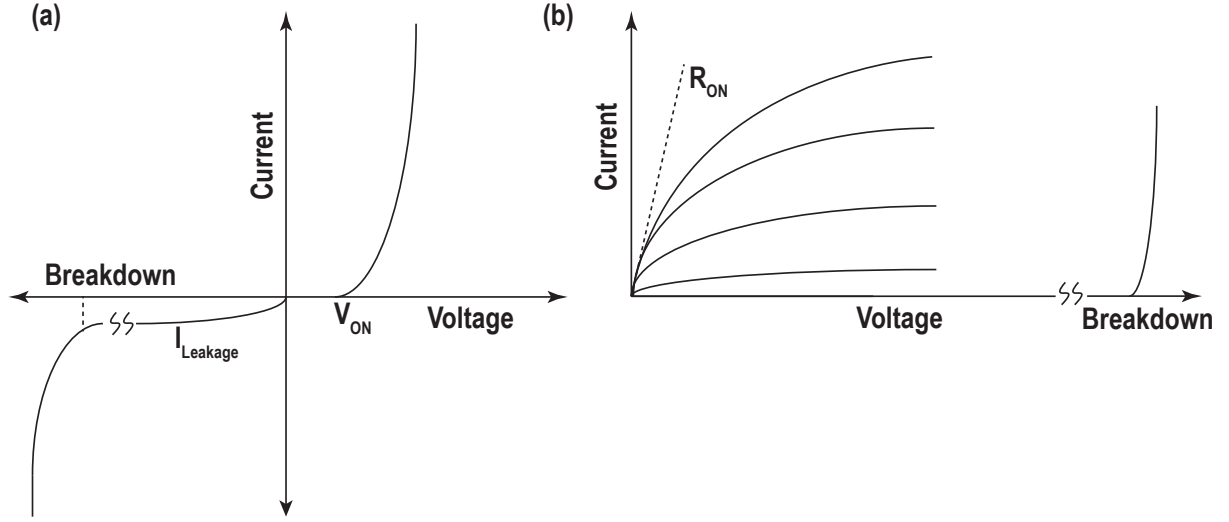


Figure 1.4: Illustrative current-voltage characteristics of real (a) diode (b) transistor.

conductor materials, enable operations at higher frequencies and power levels. This demands a deeper understanding of the different power losses involved to facilitate better designs and applications. Conduction losses tend to dominate during high-current operations, while switching losses are more prominent in high-frequency applications. Although leakage or off-state power loss is generally negligible under normal conditions, it can become significant during high-temperature operations.

By considering all these losses, the theoretical performance limits of a particular device design can be approached. To evaluate these limits and understand the advantages of material choices for power devices, several trade-offs are assessed through what are known as figures of merit. The following section will discuss these various figures of merit for power semiconductor devices.

1.4.3 Figure of Merits

Baliga's Figure of Merit (BFOM)

Baliga's Figure of Merit (BFOM) [25] alternatively known as Power Figure of Merit (PFOM) captures the inherent trade-off between breakdown voltage (V_{BR}) and conduction losses in

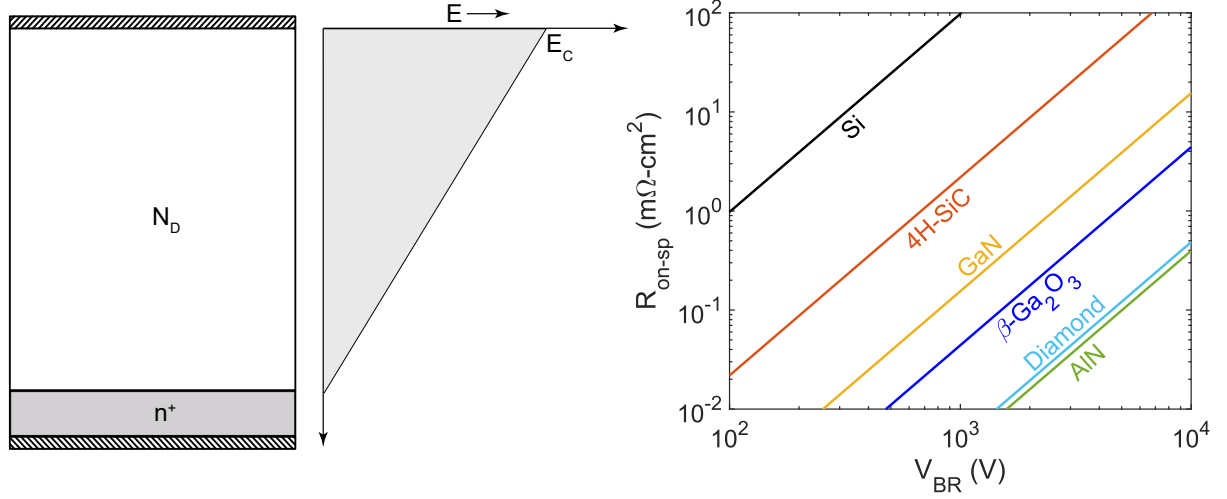


Figure 1.5: Unipolar Power Figure of Merit for different materials from Baliga's Figure of Merit assuming a triangular electric field profile and complete ionization of dopants.

vertical unipolar devices. As a material-specific metric, it is independent of device geometry, offering a projection of the material's intrinsic theoretical performance limits. This figure of merit assumes an abrupt junction and a triangular one-dimensional electric field profile, making it a valuable tool for assessing the maximum potential of a semiconductor material under idealized conditions. For an n-type semiconductor, the BFOM is generally expressed as,

$$BFOM = \frac{V_{BR}^2}{R_{on-sp}} = \frac{\epsilon_S \mu_n E_C^3}{4} \quad (1.1)$$

Where, R_{on-sp} is the specific on-resistance, ϵ_S is the permittivity of the semiconductor, μ_n is the electron mobility in the semiconductor, and E_C is the critical electric field for the semiconductor. Notably, the BFOM has a cubic dependence on the critical electric field, meaning that semiconductors with larger bandgaps inherently have higher BFOM compared to those with smaller bandgaps. The trade-off between R_{on-sp} and V_{BR} is plotted in Fig. 1.5 for various semiconductors.

The conventional BFOM assumes that all dopants are fully ionized during the device's conduction mode; however, this is not accurate for many ultra-wide bandgap (UWBG) materials, such as AlN and diamond, which exhibit significantly higher dopant ionization energies. Additionally, the model presumes a pure material free from background compensation. In

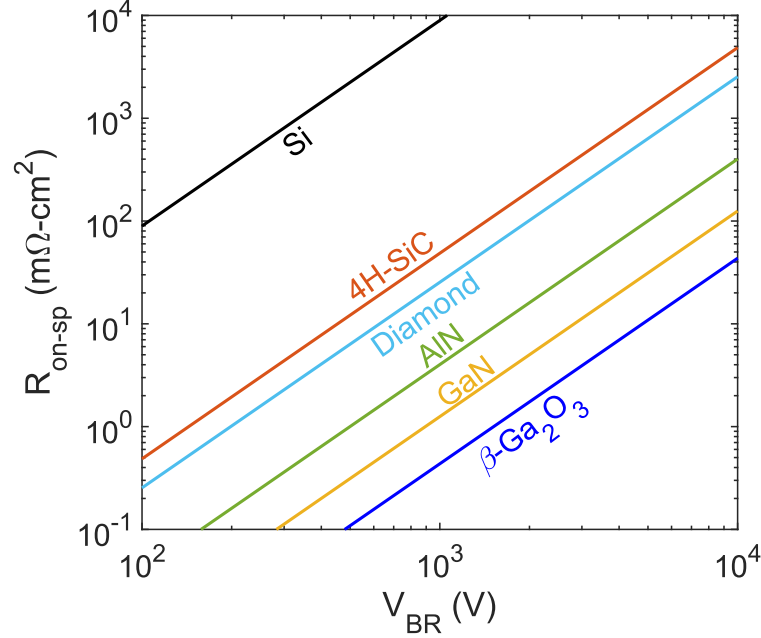


Figure 1.6: Modified Baliga's Figure of Merit for different materials considering incomplete ionization of dopants.

contrast, WBG and UWBG materials often possess background impurity levels several orders of magnitude higher than silicon. To address these limitations, Zhang *et al.* [26] proposed a modified BFOM that accounts for the effects of dopant ionization energy and background compensation within the material.

$$\text{Modified } BFOM = \frac{4V_{BR}^2}{R_{on-sp}} = \frac{n}{N_D} \mu_n \epsilon_S E_C^3 \quad (1.2)$$

Where n is the free carrier concentration and N_D is the doping concentration. Considering both incomplete ionization of dopants and background compensation, n can be expressed as,

$$n = \frac{-(N_1 + g_D N_A) + \sqrt{(N_1 + g_D N_A)^2 + 4g_D N_1 (N_D - N_A)}}{2g_D} \quad (1.3)$$

where $N_1 = N_C \exp(-\Delta E_D / k_B T)$, N_C is the effective density of states in the conduction band, ΔE_D is the donor ionization energy relative to the conduction band edge, g_D is the degeneracy factor of the donor state, and N_A is the compensating acceptor concentration. This modified BFOM suggests that the material's actual figure of merit decreases with increasing dopant

ionization energy and higher background compensating charge density.

Due to the higher background charge concentration and greater dopant ionization energies, the R_{on-sp} increases for UWBG semiconductors like AlN and diamond, thereby reducing their actual BFOM. However, β -Ga₂O₃ exhibits the best BFOM among all these materials, owing to the availability of shallow dopants ($\Delta E_D = 30$ meV) and a low background acceptor concentration ($N_A \sim 10^{14} \text{ cm}^{-3}$), as shown in Fig. 1.6.

Johnson's Figure of Merit (JFOM)

In radio-frequency (RF) devices, both the operating speed and output power are of critical importance. In 1965, Johnson introduced a figure of merit (JFOM) [27] that effectively captures the trade-off between operational frequency and output power. This figure of merit is defined as:

$$JFOM = f_T V_{BR} = \frac{E_C V_{sat}}{2\pi} \quad (1.4)$$

This equation represents the power-frequency product of a low-voltage RF transistor, where f_T denotes the device's cut-off frequency, and v_{sat} is the carrier's saturation velocity within the material. It indicates that the power-frequency product is directly proportional to both the critical electric field and the carrier saturation velocity. Given that v_{sat} is similar for most semiconductors, the JFOM is higher for wide and ultra-wide bandgap semiconductors.

Thermal Figure of Merit

The thermal conductivity of a material is also critically important in power applications, particularly in cases where the entire device consists of an active region that conducts current. A rise in temperature generally reduces carrier mobility within the semiconductor, thereby increasing the device's on-resistance. When a perfect heat sink is attached to a device with an active region encompassing the entire volume, the internal temperature can range from ambient levels to a certain maximum during current conduction. Elevated temperatures can also lead to premature device failure. Therefore, efficient heat removal is essential for optimal operation, and the

material's thermal resistance plays a crucial role in achieving this. In 1989, Shenai *et al.* [28] developed a thermal figure of merit to capture the trade-off between breakdown voltage, specific on-resistance, and the specific thermal resistance of the drift layer:

$$\text{Thermal } FOM = \frac{V_{BR}^3}{R_{th-sp} R_{on-sp}} = \frac{\kappa_{th} \epsilon_S \mu_n E_C^4}{8} \quad (1.5)$$

Where, R_{th-sp} is the specific thermal resistance of the drift region and κ_{th} is the thermal conductivity of the semiconductor.

Huang's Switching Figure of Merit

The switching performance of power devices is another critical factor to consider, and it can be represented by a specific figure of merit that facilitates comparison of different materials for switching applications. A power device must switch rapidly with minimal loss during the switching period. The switching speed of a device is typically determined by the charge stored within it during steady-state operation; this stored charge must be removed to turn the device on or off, which requires a finite amount of time. Therefore, a lower stored charge generally results in faster switching speeds and reduced switching losses. Huang [29] developed a switching figure of merit for transistors, known as Huang's Material Figure of Merit (HMFOM), which captures the trade-off between breakdown voltage, on-resistance, and the stored gate charge of a transistor, and it is dependent on specific material properties:

$$HMFOM = \frac{V_{BR}}{\sqrt{R_{on} Q_G}} = E_C \sqrt{\mu_n} \quad (1.6)$$

Where, Q_G is the gate charge in a transistor, which can also correspond to the stored charge in the drift region of a diode. A lower $R_{on} Q_G$ is desirable for faster switching and from (1.6), it is evident that a higher E_C leads to lower $R_{on} Q_G$.

A comparison of different figures of merit for different materials is provided in Table 1.1.

Table 1.1: Material parameters and Figure of Merit for different semiconductors

	Si	4H-SiC	GaN	β -Ga ₂ O ₃	Diamond	AlN
Bandgap, E_g (eV)	1.1	3.3	3.4	4.6	5.5	6.2
Critical Electric Field, E_C (MV/cm)	0.3	2.2	3	8	10	15.4
Relative permittivity, ϵ_r	11.8	9.7	9	10	5.7	8.5
Electron mobility, μ_n (cm ² /Vs)	1450	900	1200	200	2000	300
Saturation velocity, v_{sat} ($\times 10^7$ cm/s)	1	2.2	2.4	1.1	2.3	1.4
Thermal conductivity, κ_{th} (W/mK)	130	370	250	20	2300	285
BFOM	1	200	630	2216	24676	20160
JFOM	1	16	24	29	77	72
Thermal FOM	1	4200	12140	9093	1.5×10^7	2.3×10^6
HMFOM	1	6	9	10	39	23

1.4.4 Lateral vs Vertical Power Devices

Currently, two types of structures are being considered for β -Ga₂O₃-based power devices: lateral and vertical. Lateral devices, due to their planar architecture, offer ease of fabrication. In 2012, Higashiwaki *et al.* demonstrated the first β -Ga₂O₃ transistor [30], utilizing a bulk EFG-grown substrate and MBE-grown channels. This device achieved a breakdown voltage (V_{BR}) of 250 V without any field management. Since then, a variety of lateral devices, such as Schottky barrier diodes (SBDs), p/n heterojunction diodes (HJDs), metal-semiconductor field-effect transistors (MESFETs), and MOSFETs, have been developed on β -Ga₂O₃, with breakdown voltages reaching up to 10 kV [31]–[39]. Among MOSFETs and MESFETs, modulation-doped transistors (MODFETs) have been demonstrated [40]–[43], leveraging a two-dimensional electron gas (2DEG) formed at the interface of β -(Al_xGa_{1-x})₂O₃/ β -Ga₂O₃

heterostructures. MODFETs are anticipated to achieve higher electron mobilities compared to impurity-doped channels at similar charge densities by minimizing impurity scattering [44]. Theoretical predictions suggest the potential for even higher mobilities with increased charge densities (surpassing the bulk mobility limit) due to dynamic phonon screening effects. Additionally, various radio frequency (RF) transistors based on β -Ga₂O₃ have been reported [45]–[50], achieving current gain cut-off frequencies as high as 50 GHz.

However, lateral β -Ga₂O₃ devices face several limitations. First, because all three contacts (or two in the case of diodes) are located on the top surface, careful management of electric field profiles in the lateral dimension between contacts is essential for high-voltage applications. High electric fields are needed to be managed near the surface. Achieving high breakdown voltages requires substantial gate-to-drain lateral spacing; for example, a 10 kV β -Ga₂O₃ MOSFET requires a source-to-drain spacing exceeding 30 μ m. This requirement reduces the effective current density (relative to die size) achievable in these devices and leads to a decrease in current density as the breakdown voltage increases. Consequently, high-voltage lateral devices demand larger areas to reduce device on-resistance, and complex multi-finger structures are often required to achieve high current operation in lateral transistors [51]. Low current densities also limit the number of dies that can be fabricated on each wafer as voltage ratings increase, ultimately driving up the cost per ampere rating.

Additionally, the quality of the interface between the substrate and the epitaxial layer is crucial in realizing reliable lateral power devices. Impurities at the substrate/epi interface can lead to higher leakage currents and premature breakdown. Silicon, a common impurity, often accumulates at the substrate/epi interface and can be introduced onto the wafer surface from the ambient environment prior to growth. To mitigate the impact of these interface impurities, several precleaning and in-situ treatments are necessary before epitaxial growth.

Compared to lateral structures, vertical device architectures are generally preferred for discrete power electronic devices (For >1kV rated devices) due to several key advantages. First, vertical power devices typically achieve a higher current density per unit area than

lateral devices, as their footprint is independent of drift layer thickness. This allows for increased breakdown voltage by thickening the drift layer without impacting the device's area. Additionally, vertical power devices exhibit more uniform heat distribution, whereas lateral devices are prone to localized hot spots. Another advantage of vertical devices is their potential for enhanced avalanche capability, particularly when incorporating a p-type body. This has been demonstrated in a vertical p-NiO/ β -Ga₂O₃ HJD, which can withstand repetitive surge conditions [52]. Furthermore, vertical architectures enhance both reliability and long-term stability, as high electric fields are confined within the bulk of the device rather than on the surface. This configuration minimizes the reliance on surface passivation to control field dispersion. Finally, vertical designs offer a more manageable electric field profile, closely resembling a one-dimensional distribution, which helps alleviate field crowding and brings performance closer to the material's theoretical limits.

To date, most vertical devices developed with β -Ga₂O₃ have been Schottky barrier diodes (SBDs) or p-NiO/ β -Ga₂O₃ heterojunction diodes (HJDs). Vertical SBDs and HJDs have achieved impressive breakdown voltages, reaching up to 13.5 kV [53], and demonstrated power figure of merit (PFOM) values that exceed those of SiC and GaN. [31], [54]–[70]. Additionally, charge-balanced superjunction-like structures employing p-NiO have shown superior PFOM performance. In comparison, however, vertical transistor demonstrations on β -Ga₂O₃ remain limited. Sasaki *et al.* were the first to demonstrate a depletion-mode vertical trench MOSFET on β -Ga₂O₃ [71], although the device exhibited characteristics more akin to a static induction transistor (SIT) than a conventional transistor. Subsequently, Hu *et al.* demonstrated a depletion-mode vertical FinFET on β -Ga₂O₃, achieving a breakdown voltage of 185 V [72], which also exhibited SIT-like behavior. The first current aperture vertical electron transistor (CAVET), introduced by Wong *et al.* [18], [73], demonstrated transistor-like characteristics but faced issues with significant off-state leakage due to a diffused current-blocking layer that compromised its breakdown performance. In 2018, Hu *et al.* presented the first enhancement-mode single-fin vertical FinFET on β -Ga₂O₃, achieving a 1 kV breakdown voltage [74]. This work was later

advanced by Li *et al.*, who developed an enhancement-mode multi-fin vertical FinFET with a breakdown voltage of 2.6 kV [75]. Various research groups have since explored similar structures with further modifications. Continued innovation in vertical β -Ga₂O₃ devices is likely to unlock further performance improvements, paving the way for applications that demand both high voltage and high current capabilities.

1.5 Challenges in High-Voltage Device Design

1.5.1 Voltage Blocking in Power Semiconductor Devices

When a voltage is applied across a semiconductor device, an electric field is established as a result. In blocking mode, this electric field must be fully contained within the device to prevent any current flow. To achieve this, an equal and opposite electric field is generated within the semiconductor, counteracting the applied field. This opposing electric field is created through a dipole, which consists of separated positive and negative charges within the depletion region of the semiconductor (In the case of a metal/semiconductor junction, this dipole forms at the interface, with charges distributed between the metal and the semiconductor's depletion region). The ability of a semiconductor device to block voltage in this way is crucial for controlling current flow, especially at high electric fields.

As discussed in Section 1.4, a p-n junction or a Schottky junction serves as a rectifying junction that can generate the necessary electric field to block voltage. These junctions are termed “rectifying” because they allow voltage blocking in one direction only. Both types rely on a lightly doped semiconductor region to facilitate voltage drop. Another common voltage-blocking structure is the metal-oxide-semiconductor (MOS) configuration. In a MOS structure, depending on the polarity of the applied voltage, the electric field may be fully contained within the dielectric layer or divided between the dielectric and semiconductor layers.

The choice of junction type significantly impacts device performance, and different junctions are used based on specific application requirements. The next subsection will explore these

various junctions and their applications.

1.5.2 Leakage Currents in Power Semiconductor Devices

Although in ideal scenarios, a semiconductor junction should block voltage and as a result impede the flow of current, several fundamental and practical issues prevent this from happening. In practical devices in blocking mode or in off-state currents do flow, which is known as leakage current. Under high electric fields, these currents can become significant, resulting in unwanted power dissipation during the off-state of transistors and in the reverse blocking mode of diodes. MOS structures also experience leakage current, primarily through the dielectric layer.

Leakage currents can arise from both intrinsic and extrinsic mechanisms. Intrinsic sources include drift-diffusion, avalanche multiplication, and band-to-band tunneling, especially in p-n diodes. Extrinsic sources, such as thermionic field emission resulting from carrier injection, predominantly affect Schottky diodes. The intrinsic leakage processes are highly dependent on the semiconductor's bandgap and generally decrease as the bandgap (E_g) widens. For instance, drift-diffusion current in a reverse-biased junction is proportional to n_i^2 , where n_i represents the intrinsic carrier concentration. Given that $n_i \propto \exp\left(-\frac{E_g}{2k_B T}\right)$, with k_B as the Boltzmann constant and T as the temperature, drift-diffusion leakage current sharply declines with increasing bandgap. Avalanche multiplication, caused by impact ionization under high electric fields, generates electron-hole pairs and also reduces as the bandgap widens, due to the higher energy threshold (E_g) required for electron-hole pair formation. Notably, drift-diffusion currents generally increase with temperature, whereas avalanche currents tend to decrease. Band-to-band tunneling, on the other hand, decreases with increasing bandgap, as the tunneling probability follows $\exp\left(-E_g^{3/2}\right)$, thus reducing tunneling current significantly in materials with larger bandgaps.

Thermionic field emission, a combination of thermionic emission and barrier tunneling, is particularly relevant for Schottky diodes. This process, which relies on only one type of carrier, does not depend on the bandgap and can occur even in wide or ultra-wide bandgap

semiconductors. However, it exhibits a strong temperature dependence, typically increasing with temperature. In MOS structures, leakage often arises from direct tunneling through thin dielectrics, while defects in semiconductors can contribute to leakage as well. For example, Shockley-Read-Hall (SRH) generation currents result from point defects, and leakage can occur through extended line or plane defects or trap-assisted tunneling in dielectrics. Other sources of extrinsic leakage currents include photons, high-energy electron beams, cosmic radiations etc.

Understanding these leakage currents and their sources is essential for designing effective power devices. Material engineering to mitigate leakage currents is a key aspect of this research and forms a major focus of this thesis.

1.5.3 Edge Field Crowding in Power Semiconductor Devices

In an ideal, infinitely large semiconductor device without edges, the electric field distribution would be uniform. However, in practical devices, the presence of edges significantly distorts the electric field profile in these regions. Charges on a conductor naturally spread out to minimize repulsive forces, but near edges and sharp points, the limited surface area forces them to crowd together as shown in Fig. 1.7 (b). This results in higher charge density at these locations, and according to Poisson's equation, this increase in charge density produces a stronger electric field. Consequently, field crowding occurs around edges and corners.

In semiconductor devices, such field crowding leads to localized peaks in the electric field, which can exceed the material's critical electric field and potentially cause premature breakdown. Additionally, edge field crowding can increase leakage currents around the device periphery contributing to higher power losses. Therefore, managing edge-related effects is crucial to optimizing both performance and reliability in power devices.

Two distinct types of junctions typically form around the peripheries of Silicon-based semiconductor devices: cylindrical and spherical junctions as shown in Fig. 1.7 (a). Cylindrical junctions form along the edges of the device, where the peak electric field is inversely proportional to the radius of curvature, r_j (for small r_j values). This relationship means that as r_j

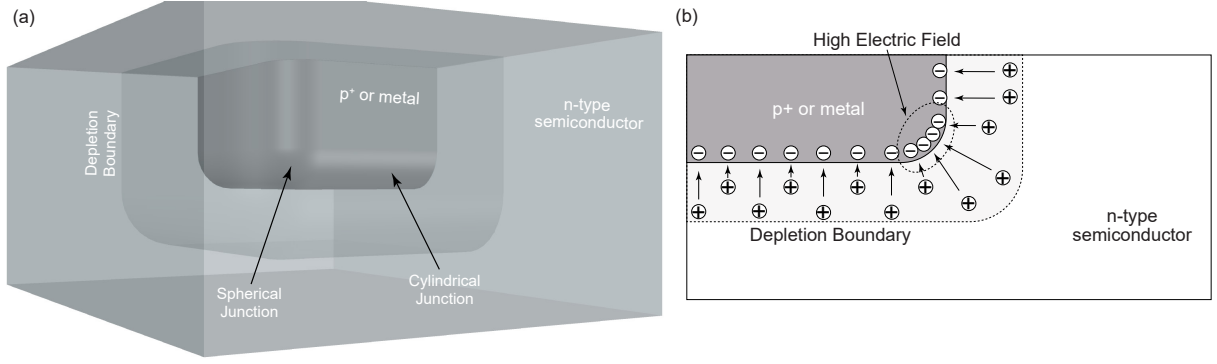


Figure 1.7: An illustrative diagram depicting (a) cylindrical and spherical junctions and (b) the phenomenon of edge electric field crowding in power semiconductor devices.

decreases, the electric field intensity increases significantly. Spherical junctions, on the other hand, develop at the device corners, where the field intensity is even higher because the electric field lines converge towards a single point in three dimensions, as opposed to a line in two dimensions for cylindrical junctions. In a spherical junction, the maximum electric field scales with r_j^{-2} , resulting in lower breakdown voltages compared to cylindrical junctions.

While spherical junctions can be effectively mitigated through layout adjustments—such as adopting circular designs or rounding off corners, eliminating cylindrical junctions presents a greater challenge in real-world power devices. Thus, precise engineering is essential to control these edge effects, which are key to achieving high breakdown voltages and dependable performance in power semiconductor applications.

This thesis will explore various strategies to minimize these edge-related challenges through materials and device engineering, aiming to enhance the overall efficiency and reliability of power devices.

1.6 Current Challenges in β -Ga₂O₃ based Power Devices

While β -Ga₂O₃ holds significant promise for high-power applications due to its unique material properties, several challenges must be addressed to unlock its full potential. One major challenge in realizing high-power β -Ga₂O₃ devices is the lack of a shallow acceptor doping mechanism.

Although many high-performing Schottky diodes have been developed on β -Ga₂O₃, p-n junctions offer superior reverse-blocking capabilities at ultra-high voltages (exceeding 10 kV). This advantage makes p-n junctions highly desirable for these applications, yet they remain difficult to achieve with β -Ga₂O₃. Additionally, p-type regions are commonly used in Si and SiC-based power devices as effective edge termination methods, a technique that is not currently feasible with β -Ga₂O₃. Although p-NiO heterojunction diodes (HJDs) have demonstrated similar characteristics to p-n diodes, such heterojunctions still need further investigation.

Another significant challenge is the low thermal conductivity of β -Ga₂O₃ ($\sim \kappa = 27$ W/mK), which can impair device performance under high-power conditions. Efficient heat dissipation is crucial for both performance and the long-term stability of power devices. To mitigate this, electro-thermal co-design approaches need to be adopted especially paying attention to thermal boundary resistances [76]. However, given the material's inherently low thermal conductivity, improvements are necessary at the packaging level, potentially through advanced active cooling solutions that enhance heat removal.

The selection of an appropriate dielectric material is also critical in β -Ga₂O₃-based devices, especially in MOSFETs, where the dielectric serves as the gate oxide or an insulating layer for current blocking. Achieving a high-quality gate dielectric/semiconductor interface is essential for threshold voltage stability in transistors. The Si/SiO₂ interface, for instance, has been instrumental to the success of Si technology due to its exceptional quality. In contrast, suitable dielectrics for β -Ga₂O₃-based devices must not only provide a pristine interface but also exhibit higher breakdown strength than the semiconductor itself. This requirement poses a substantial challenge in wide and ultra-wide bandgap materials. Although Al₂O₃ shows promise with relatively low defect density at the dielectric/semiconductor interface, it is not yet sufficient for real-world applications. This thesis will explore efforts to reduce defect density at the dielectric/semiconductor interface to improve dielectric lifetime.

In summary, despite its favorable attributes for power applications, β -Ga₂O₃ technology faces considerable obstacles, including the need for extreme electric field management in the

absence of p-type doping and the need for high-quality dielectric interfaces. Overcoming these challenges is essential for the material to achieve its true potential in high-power electronics, and this thesis will delve into strategies to address these issues, with the aim of advancing β -Ga₂O₃ toward practical, high-performance applications.

1.7 Dissertation Outline

This dissertation focuses on the electrostatic engineering of β -Ga₂O₃-based vertical and lateral devices, exploring various edge termination strategies to mitigate peak electric fields along device edges and minimize leakage currents. Additionally, it examines novel dielectric deposition techniques on β -Ga₂O₃ to reduce dielectric/semiconductor interface trap densities, enhance dielectric breakdown strength, and improve overall time-to-dielectric-breakdown of the dielectric material.

The first part of this thesis primarily investigates two-terminal β -Ga₂O₃ devices, particularly Schottky diodes, with an emphasis on edge termination techniques and field optimization strategies. The second section extends the discussion to three-terminal devices, focusing on β -Ga₂O₃-based vertical FinFETs. This includes their design considerations, field management approaches, and strategies to mitigate power losses. Additionally, innovative dielectric deposition methods are explored for gate oxides, alongside characterization of their performance and time-to-dielectric-breakdown.

In Chapter 2, various field-management strategies for vertical β -Ga₂O₃-based Schottky diodes are discussed. This chapter includes a simulation-based study examining the impact of implementing a p-type III-Nitride guard ring to enhance device performance. Additionally, a combined approach using both guard rings and high-permittivity field plates is simulated, illustrating how these methods work synergistically to improve electric field management.

In Chapter 3, the focus shifts to the implementation of high-permittivity dielectric materials as field plate oxides in β -Ga₂O₃-based vertical SBDs. This chapter investigates two high-

permittivity dielectrics with dielectric constants of 142 and 325, comparing their performance to that of a conventional SBD. In a device with a thin HVPE-grown film, the high- κ field-plated SBD demonstrates a breakdown voltage of 687 V and a Power Figure of Merit (PFOM) of 1.47 GW/cm² compared to 148V for conventional SBD. In contrast, high- κ field-plated SBDs on a thick HVPE film achieve a significantly higher breakdown voltage of ~ 2.2 kV, significantly outperforming the 816 V breakdown voltage of conventional SBDs. Additionally, an analysis of diode on-resistance, power loss calculations, and device area considerations are presented, providing insights into the optimization of these devices for power device applications.

Following the edge field reduction techniques discussed in Chapter 3, Chapter 4 addresses the mitigation of leakage currents in β -Ga₂O₃-based vertical SBDs through a trench architecture incorporating high-permittivity dielectric RESURF (REduced SURface Field) technology. Additionally, this chapter introduces a method for reducing the turn-on voltage (V_{on}) and minimizing on-state power losses by leveraging a low work-function anode contact in conjunction with the high- κ RESURF trench architecture. For example, a trench SBD with a Ru contact achieves a turn-on voltage of 0.5 V, as opposed to 1 V with a Pt contact. Large-area devices are also demonstrated, showing current capabilities of 15 A and 20 A for trench SBDs with Pt and Ru contacts, respectively. High-voltage capacitance measurements further characterize the stored charge and energy within these diodes, metrics critical for switching applications. Notably, the β -Ga₂O₃-based high- κ trench SBDs exhibit lower capacitance, stored charge, and stored energy than commercial bare-die SiC SBDs of comparable current ratings, highlighting the advantages of β -Ga₂O₃ for high-performance power applications.

The concepts in Chapters 2 and 3 feature a triangular electric field distribution within the β -Ga₂O₃ drift layer. However, the trench SBDs introduced in Chapter 4 exhibit a shift from a one-dimensional to a two-dimensional electric field profile near the Schottky metal/semiconductor interface, thanks to the MOS structures at the sidewalls. This shift reduces the electric field at the anode metal/semiconductor interface, thereby lowering leakage currents, while the electric field in the bulk drift region retains its triangular profile. Chapter 5 introduces an advanced

device architecture incorporating high-permittivity dielectrics to impact the electric field in two dimensions throughout the drift region, addressing the absence of shallow acceptors in β -Ga₂O₃. By leveraging the fringing electric field, the drift layer's field profile transitions from triangular to rectangular, emulating the behavior of superjunction devices where the device PFOM exceeds the theoretical unipolar FOM of the material enabling the use of higher doping levels in the drift layer for much lowered on-resistance. This **high- κ Dielectric Superjunction** offers several advantages over conventional p/n superjunction devices, which are elaborated upon in this chapter. Chapter 5 begins with a theoretical analysis of the high- κ dielectric superjunction device, providing design guidelines and demonstrating its advantages over stringent charge balance requirements in p/n superjunctions. In the second part, a lateral high- κ dielectric superjunction device, utilizing BaTiO₃ dielectric, is fabricated and demonstrated. This lateral configuration circumvents some of the fabrication challenges associated with a vertical architecture and serves as a proof-of-concept implementation of high-k dielectric semiconductor superjunction structures. The demonstrated device achieves a PFOM of 1.34 GW/cm² when normalized to the device footprint and surpasses the theoretical PFOM for SiC when considering only the current-conducting area.

In Chapter 6, a novel dielectric deposition technique for β -Ga₂O₃ is explored, employing Metalorganic Chemical Vapor Deposition (MOCVD). This technique allows for the in-situ growth of both the semiconductor and dielectric material (Al₂O₃) within the same reactor without breaking the vacuum. The quality of the semiconductor/dielectric interface is assessed through ultra-violet (UV)-assisted capacitance-voltage (C-V) and current-voltage (I-V) characterizations, revealing significantly fewer interface traps and a superior breakdown field compared to conventional atomic layer deposited Al₂O₃. The effect of deposition temperature on dielectric quality is also characterized, and a hybrid-temperature deposition approach is introduced. High-temperature deposition yields a dielectric with a breakdown field of 10 MV/cm. Further reliability and lifetime assessments are performed using the Time-Dependent Dielectric Breakdown (TDDB) method. Dielectrics grown at two distinct temperatures demonstrate a projected

lifetime exceeding 20 years at stress fields above 3 MV/cm.

Chapter 7 delves into the design and fabrication of a three-terminal vertical device, with a primary focus on the vertical fin topology for developing normally-off β -Ga₂O₃ vertical power transistors (FinFETs). This vertical fin architecture eliminates the need for p-type doping, enabling normally-off operation and providing excellent electrostatic control over the channel. Multi-fin designs utilizing advanced fabrication techniques are demonstrated, with the first-generation vertical FinFET achieving a breakdown field exceeding 1 kV and a specific on-resistance of $7.5 \text{ m}\Omega\text{-cm}^2$. The second-generation device builds upon this by incorporating electrostatic engineering within the trench region to further enhance the breakdown field. Novel strategies are also introduced to minimize device capacitances, addressing key challenges related to switching performance. This chapter thoroughly examines the fabrication challenges unique to this power transistor architecture, offering insights into the practical considerations for achieving high-performance, durable β -Ga₂O₃-based power devices.

In Chapter 8, a comprehensive summary of the dissertation is provided, highlighting the key contributions and findings. Additionally, the current challenges in device fabrication, material quality, and other factors impacting high-voltage and high-power β -Ga₂O₃-based devices are discussed. The chapter concludes by outlining future directions and potential advancements needed to enable successful industrial adoption of this promising technology.

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Chapter 2

Edge Termination Strategies in Power Devices

2.1 Introduction

As discussed in Chapter 1, the concentration of electric fields at the edges of power semiconductor devices creates hot spots in these regions. These edge electric fields can reach values significantly higher than those in the bulk of the device, even at relatively low voltages, which can lead to premature breakdown. Moreover, these intense electric fields can cause current leakage through thermionic field emissions along the device perimeter. Thus, effectively managing electric fields at the edges and corners is essential for achieving efficient and reliable power device performance.

β -Ga₂O₃ shows great promise as a robust material for power electronics, owing to its superior Baliga's figure-of-merit (BFOM) compared to other competing technologies like SiC and GaN. However, the absence of p-type doping in β -Ga₂O₃ presents challenges for using conventional edge termination techniques that are well-established in Si and SiC-based power devices. This chapter examines various edge termination strategies in power semiconductor devices, with a focus on the unique challenges encountered when applying these methods to

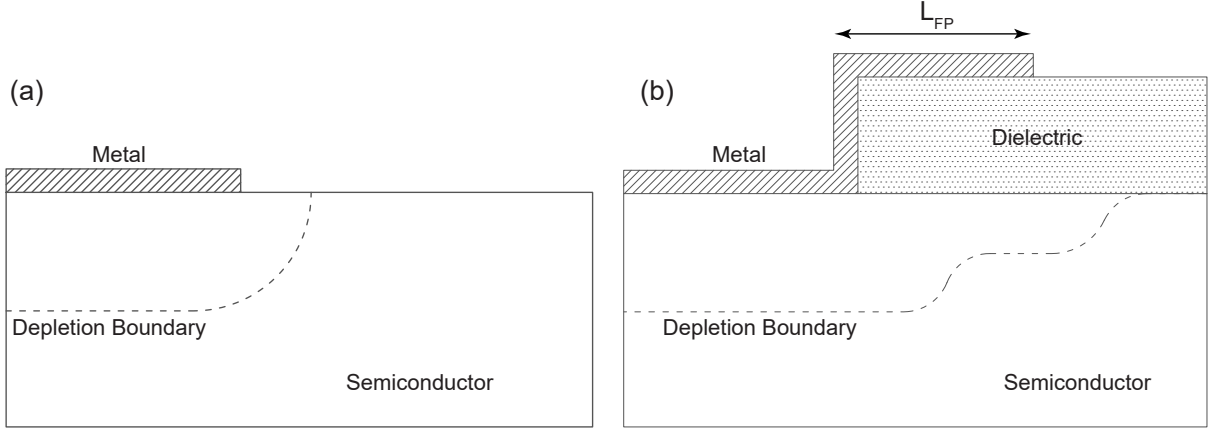


Figure 2.1: An illustration of the shape of depletion region edge in (a) non-field-plated and (b) field-plated SBDs.

β -Ga₂O₃-based devices. Additionally, it introduces techniques to overcome these challenges using TCAD simulations.

2.2 Edge Terminations

2.2.1 Field Plates

Field-plate techniques are commonly employed in power semiconductor devices to reduce electric field concentration at the device edges [1]–[4]. In a conventional Schottky barrier diode (SBD), when a reverse bias is applied, the depletion region forms a shape similar to a cylindrical junction, as illustrated in Fig. 2.1 (a). In a field-plated device, the metal contact extends beyond the contact region over a dielectric material known as field oxide. This configuration allows the depletion region to spread beyond the junction edge, distributing it over a larger area and preventing the electric field from concentrating at the edge of the metal/semiconductor junction, as shown in Fig. 2.1 (b).

The electric field profile along the metal/semiconductor interface in a conventional Schottky barrier diode (SBD) takes the shape shown in Fig. 2.2 (a). In this profile, the electric field peaks at the edge of the metal, and the device experiences breakdown when this peak field reaches the material's critical electric field. In a field-plated device, however, two edges are

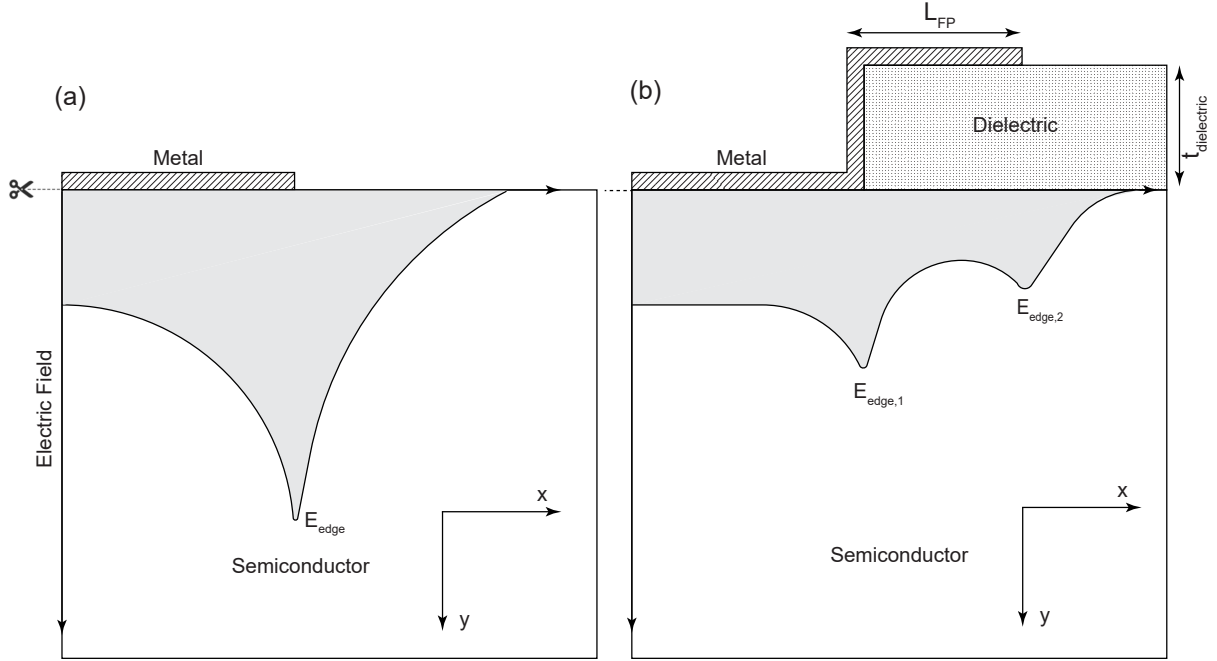


Figure 2.2: An illustration of the electric field profile along the (a) non-field-plated and (b) field-plated SBDs.

present: one at the metal/semiconductor interface (designated as $Edge, 1$) and another at the metal/dielectric interface ($Edge, 2$). Consequently, the electric field profile displays two peaks, labeled $E_{edge,1}$ and $E_{edge,2}$, as illustrated in Fig. 2.2 (b). When the same voltage is applied to both a conventional and a field-plated device, the area under the electric field profile for both devices remains the same: ie;

$$-\iint_S E^{NFP}(x,y)dx dy = -\iint_S E^{FP}(x,y)dx dy = V_{applied} \quad (2.1)$$

where $E^{NFP}(x,y)$ and $E^{FP}(x,y)$ represent the electric field in the non-field-plated and field-plated SBDs, respectively, and $V_{applied}$ is the applied reverse bias. To satisfy Equation 2.1, the field peaks $E_{edge,1}$ and $E_{edge,2}$ in a field-plated SBD must be lower than the peak electric field E_{edge} in a non-field-plated SBD. Consequently, the peak electric field at the device edges is reduced by the field-plate, allowing the device to sustain higher voltages before the edge field reaches the material's critical electric field.

The length of the field-plate extension (L_{FP}) is a critical factor in achieving optimal device design. Based on extensive design experiments, the breakdown voltage initially increases with

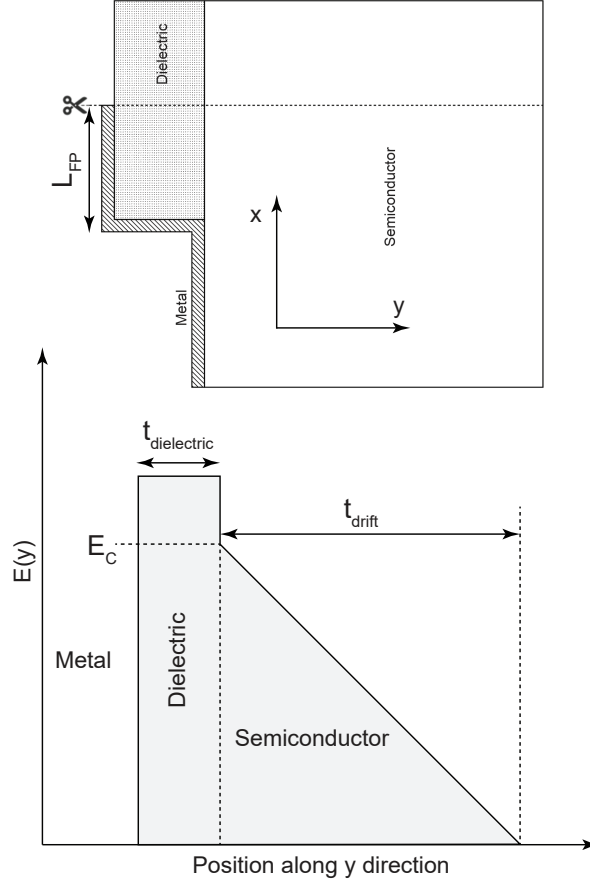


Figure 2.3: An illustration of the electric field profile at the field-plate edge along the y-axis. In this example, the dielectric's relative permittivity is assumed to be lower than that of the semiconductor (although the equations derived apply to other configurations as well). It is also assumed that breakdown occurs at the field-plate edge, which informs the dielectric thickness design.

L_{FP} , but beyond a certain point, it becomes independent of further increases. This threshold generally corresponds to the depletion region depth in the semiconductor at breakdown [5]. Consequently, an effective design strategy is to adjust the drift layer doping and thickness so that the depletion depth aligns precisely with the drift layer thickness. By extending the field-plate to match the drift layer thickness, ie;

$$L_{FP} = t_{drift} \quad (2.2)$$

where t_{drift} is the drift layer thickness, an optimal balance between breakdown voltage and R_{on-sp} can be achieved.

The thickness and dielectric constant of the field-plate dielectric are key factors in reducing

the peak electric field. Analyzing breakdown at the field-plate edge requires considering the electric field behavior in both the dielectric and semiconductor at breakdown. The difference in dielectric constants between these materials must be factored into this analysis. According to Gauss's law, the electric displacement across the dielectric/semiconductor interface remains continuous. Thus, the electric field in the dielectric and semiconductor at this interface can be expressed as:

$$\epsilon_{dielectric}E_{dielectric} = \epsilon_S E_S \quad (2.3)$$

where $\epsilon_{dielectric}$ and ϵ_S are the relative permittivities of the dielectric and semiconductor, respectively, and $E_{dielectric}$ and E_S are the electric fields at the interface within the dielectric and semiconductor. At breakdown, $E_S = E_C$, where E_C represents the critical electric field of the semiconductor.

Assuming a triangular electric field distribution at breakdown, the breakdown voltage can be approximated as the area under the electric field profile shown in Fig. 2.3, given by:

$$V_{BR} = E_{dielectric}t_{dielectric} + \frac{1}{2}E_C t_{drift} \quad (2.4)$$

Combining Equations (2.3) and (2.4), the dielectric thickness can be derived as:

$$t_{dielectric} = \left(\frac{\epsilon_{dielectric}}{\epsilon_S} \right) \left[\frac{V_{BR}}{E_C} - \frac{t_{drift}}{2} \right] \quad (2.5)$$

Using Equations (2.2) and (2.5), optimal field-plated SBDs can be designed to reach any desired breakdown voltage. Several other field-plate variations and configurations are also available, including beveled field-plates [6] and staircase field-plates [7], as shown in Figures 2.4 (a) and (b), respectively. In a beveled field-plated SBD, the breakdown voltage can be further enhanced by introducing a small bevel angle (θ) in the semiconductor; as the bevel angle decreases, the breakdown voltage correspondingly increases. The staircase field-plate configuration, on the other hand, employs multiple field-plate levels, each with progressively increasing dielectric thickness. This design results in multiple electric field peaks at the

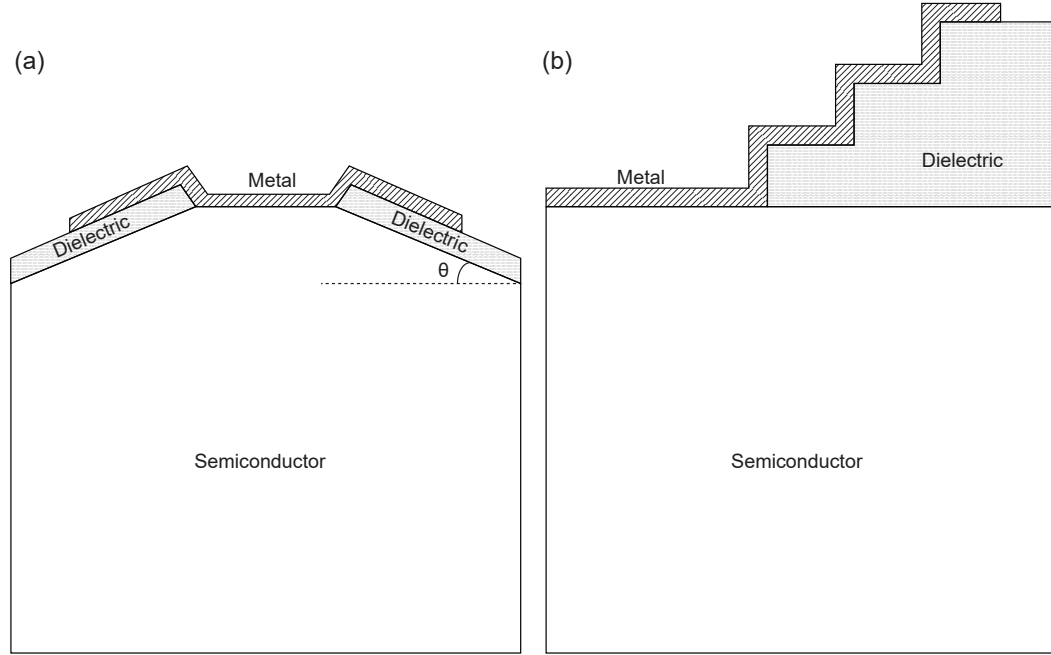


Figure 2.4: Schematic diagram of (a) Beveled Field-Plated and (b) Staircase Field-Plated SBDs

various edges, with each peak's electric field value effectively reduced. Although both of these configurations, when carefully designed, can achieve higher breakdown voltages compared to conventional field-plated SBDs, they come at the cost of added fabrication complexity.

2.2.2 Guard Rings

Guard rings represent another edge termination technique used in Schottky barrier diodes [8]–[11]. For n-type semiconductor-based SBDs, a heavily p-doped region is employed as guard rings beneath the metal edges, as illustrated in Fig. 2.5. These guard rings overlap the edges of the Schottky contact metal, effectively shielding it from high electric fields where the metal edge forms an ohmic contact with the p^+ region. The breakdown voltage of this configuration is equivalent to that of the cylindrical junction discussed in Chapter 1, provided that the diode corners are sufficiently rounded to prevent the formation of spherical junctions.

The presence of the p^+ guard ring establishes a p/n junction in parallel with the Schottky diode. Because the Schottky rectifier has a significantly lower turn-on voltage compared to p/n junctions, the p/n junction remains below the threshold necessary to inject minority carriers into

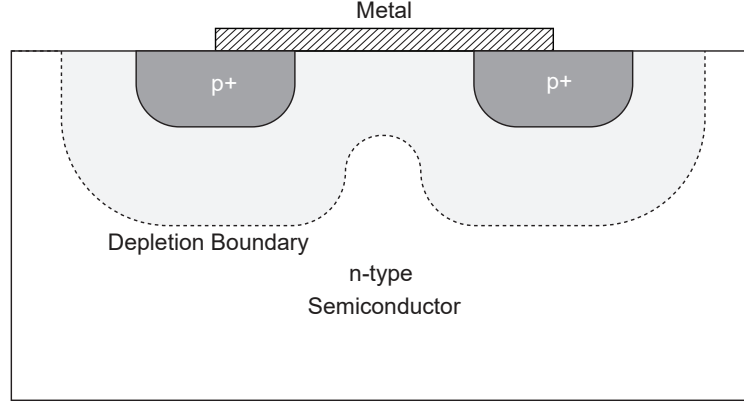


Figure 2.5: Schematic diagram of an SBD with p^+ guard rings.

the drift region under normal operating conditions. This allows the Schottky rectifier to maintain its fast switching performance, a crucial feature for high-frequency power circuits. Under surge current conditions, however, when the diode experiences very high on-state current densities, injection from the p/n junction can help reduce the on-state voltage drop and power dissipation by inducing conductivity modulation in high carrier lifetime indirect band gap semiconductors such as Si and SiC Schottky rectifiers. For GaN-based Schottky diodes, however, conductivity modulation is typically not achievable due to the short minority carrier recombination lifetimes inherent to GaN [12].

In β -Ga₂O₃-based Schottky diodes, the absence of effective p-type doping precludes the realization of p^+ homojunction guard rings. Nevertheless, resistive guard rings formed through nitrogen (N) [11] or magnesium (Mg) [13] ion implantation have been reported as alternatives.

In addition to the techniques discussed, various other edge termination methods are used in power semiconductor devices to reduce electric field crowding at the device edges, such as floating field ring termination [14], [15] and Junction Termination Extension (JTE) [16], [17]. A comprehensive analysis of all edge termination techniques lies beyond the scope of this work. However, the following section will provide a detailed analysis of heterojunction p^+ guard rings and combinations of guard rings and field-plates on β -Ga₂O₃-based SBDs, addressing the challenge of the lack of shallow acceptors in β -Ga₂O₃ through TCAD simulations.

2.3 Design of β -Ga₂O₃ Schottky Barrier Diodes using p-type

III-Nitride Guard Rings

As discussed in Section 2.3, homojunction guard rings in β -Ga₂O₃ can be realized by implanting deep acceptors, such as nitrogen (N) or magnesium (Mg), into the material edges, creating a resistive layer. While these devices demonstrate an improvement in breakdown voltage compared to designs without guard rings, the absence of a quasi-neutral region in these guard rings limits their effectiveness in screening the electric field. High-resistivity guard rings can help to spread the depletion region and reduce field crowding at metal edges. However, a guard ring with a quasi-neutral region can provide superior electric field screening at the metal edges by shifting the high-field region from the metal edge deeper into the device.

Due to the lack of shallow acceptors in β -Ga₂O₃, p-doped III-nitrides offer a promising alternative for guard ring materials, allowing for the formation of a quasi-neutral region. The concept of heterostructure guard rings has previously been proposed for Silicon Carbide substrates [18]. Additionally, Muhammed et al. [19] reported the successful growth of c-plane n-GaN epilayers on ($\bar{2}$ 0 1) β -Ga₂O₃ substrates using MOCVD, and vertical blue LEDs have been demonstrated on similar substrates [20]. Shimamura et al. [21] reported the growth of c-plane GaN on (1 0 0) oriented β -Ga₂O₃ substrates, while Cao et al. [22] achieved growth of non-polar a-plane GaN on (0 1 0) oriented β -Ga₂O₃ substrates via MOCVD. These studies confirm the feasibility of growing electronic-grade polar and non-polar GaN on β -Ga₂O₃ substrates, depending on substrate orientation.

This section presents a design for a β -Ga₂O₃ Schottky Barrier Diode (SBD) incorporating a p-doped III-Nitride guard ring, developed through electric field simulations. Three distinct guard ring configurations are evaluated: (i) p-Gallium Nitride (p-GaN) guard rings, (ii) non-polar graded p-Aluminum Gallium Nitride (p-AlGaN) guard rings, and (iii) polar graded p-AlGaN guard rings. Detailed electrostatic simulations are conducted to capture and control high electric fields within III-nitride/ β -Ga₂O₃ heterostructures. The design is optimized to determine the

Table 2.1: Material parameters used for TCAD simulation of SBD with III-Nitride guard rings

Material	Ga ₂ O ₃	GaN	AlN
Bandgap (eV)	4.85 [24]	3.3 [25]	6.2 [25]
Electron affinity (eV)	3.9 [24]	3.9 [25]	0.6 [25]
Relative permittivity	10 [24]	8.9 [26]	8.5 [26]
Electron Effective mass	0.28m ₀	0.22m ₀	0.4m ₀
Hole Effective mass	-	1m ₀	4m ₀
Critical Electric Field (MV/cm)	8 [24]	3.3 [26]	15 [26]
Sn Activation energy (eV)	0.03 [24]	-	-
Mg Activation energy (eV)	-	0.2 [26]	0.6 [26]
Spontaneous Polarization (C/m ²)	-	-0.034	-0.09

while larger spacing was used for the drift region. The spontaneous polarization model was applied to account for polarization effects in the graded polar p-AlGaN, using spontaneous polarization values of -0.034 and -0.09 C/m² for GaN and AlN, respectively [26].

The incomplete ionization model was used for p-type doping in GaN and AlGaN to accurately reflect hole concentration. In cases of high doping, the Fermi-Dirac model was included for better accuracy under operational bias. The simulation setup utilized well-calibrated mobility and thermodynamic transport models to align with experimental results [11]. Breakdown voltage estimations were based on E-field simulations, determining the breakdown point when the peak E-field reached the critical values for GaN (3.3 MV/cm) or Ga₂O₃ (8 MV/cm). Band offsets were estimated using the electron affinity rule, which correlated well with experimentally determined offsets for GaN/Ga₂O₃ [30].

To save computational time, ionization integrals for avalanche breakdown were not calculated, especially given that accurate ionization rate parameters for Ga₂O₃ are not yet established. Therefore, breakdown estimations rely on the electric field distributions generated by the simulation [31]–[33]. It's also important to note that, in real devices, field crowding can occur at the device corners. However, these fields are typically lower than the field crowding at the electrode edges, which is the primary factor in device breakdown. Thus, our device breakdown comparison for the various configurations, based on 2D simulations, remains reliable and is

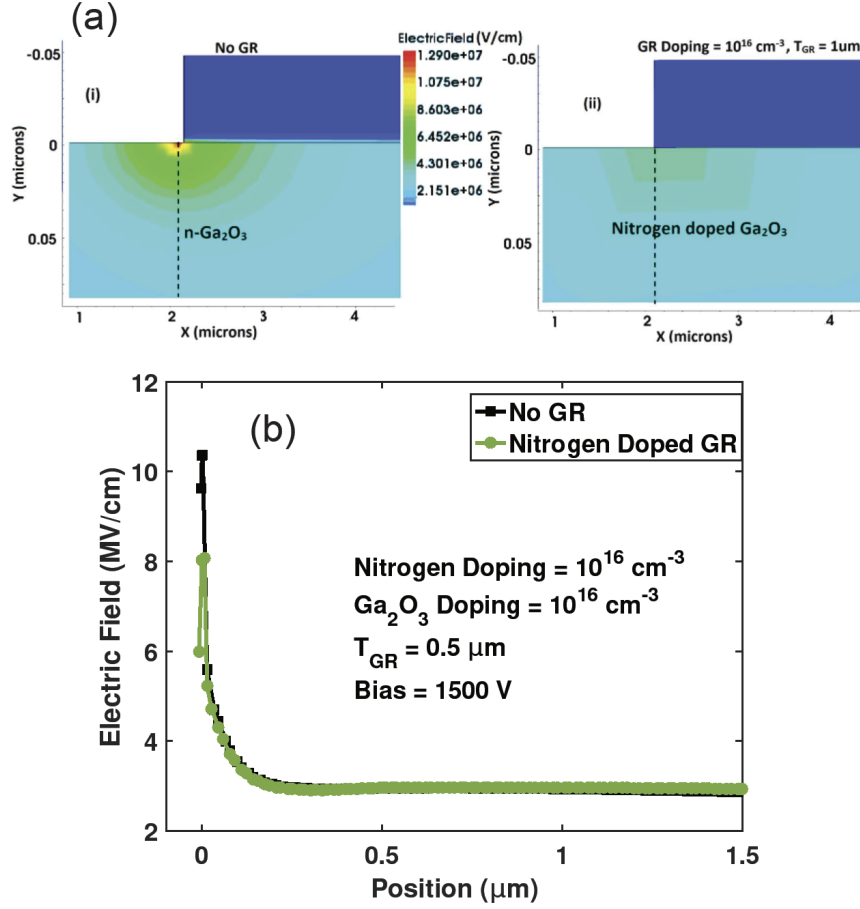


Figure 2.7: (a) Electric field distribution in SBD for (i) no GR (ii) Nitrogen doped GR at bias voltage of 1500 V (b) Electric field vs position for N-doped GR and no GR at 1500 V along the cutlines shown in the contour plots. Reprinted from Roy *et al.* [23] © 2020 IEEE.

supported by prior studies [31].

All material parameters for β -Ga₂O₃, GaN, and AlN used in the simulations are listed in Table 2.1. Parameters for intermediate Al compositions in Al_xGa_{1-x}N were calculated based on Vegard's law, using GaN and AlN data.

2.3.2 Results and Discussions

The SBD with a nitrogen-doped guard ring (GR) and the one without a GR were simulated for comparison, and their electric field profiles are shown in Fig. 2.7 (a) (i) and (ii), respectively. The circled cross-section in Fig. 2.6 is magnified and presented for each of the electric field contours. The applied bias voltage is set to 1500 V, and the ionization energy of nitrogen in

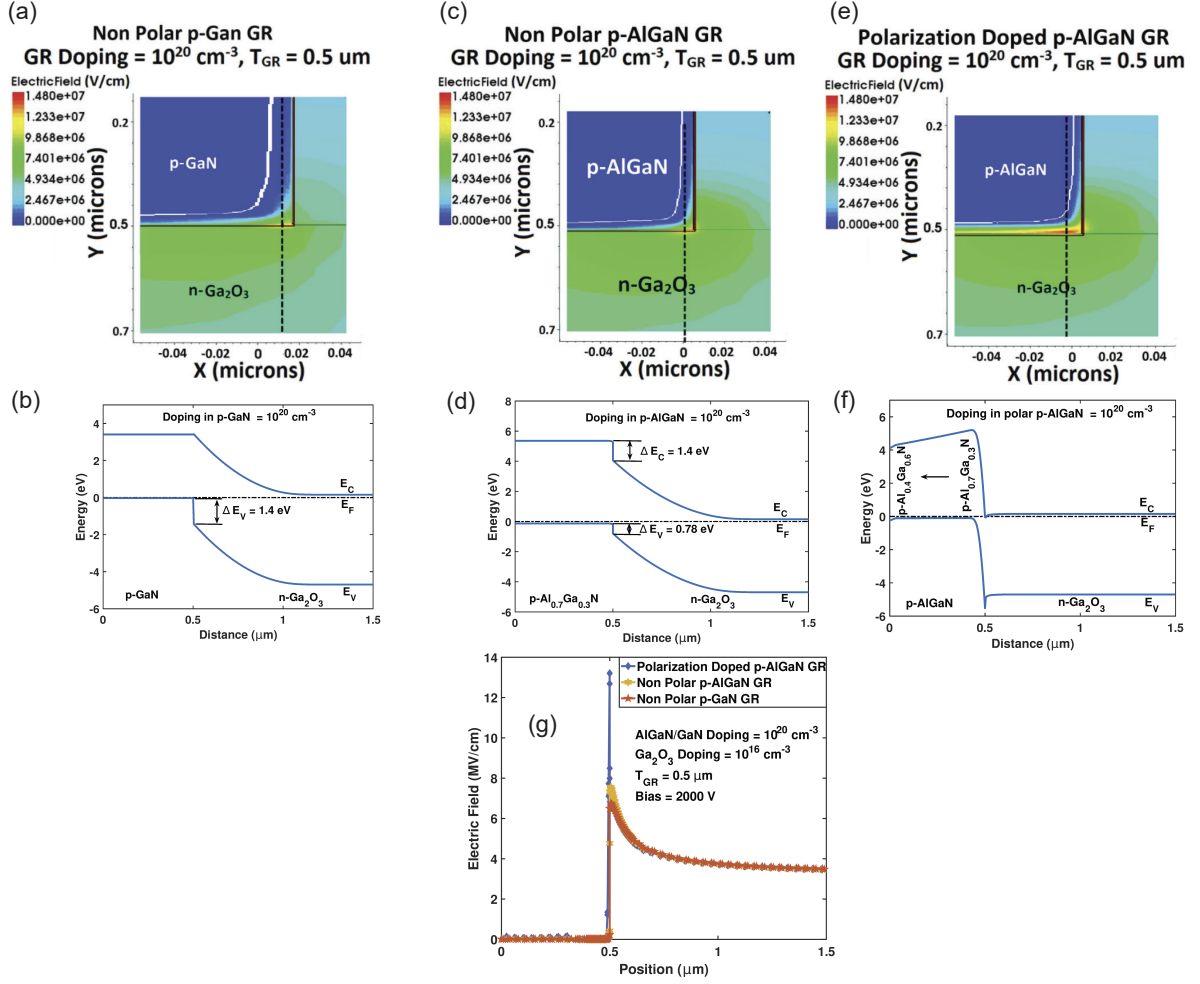


Figure 2.8: Electric field distribution and equilibrium energy band diagram for SBD with (a) (b) non-polar p-GaN GR (c) (d) non-polar p-AlGaIn GR (e) (f) polarization doped p-AlGaIn GR respectively at bias voltage of 2000 V and GR doping of 10^{20} cm^{-3} (g) Electric field vs position in SBD for the three different GR at 2000 V and at GR doping of 10^{20} cm^{-3} along the cutlines shown in the contour plots. Reprinted from Roy *et al.* [23] © 2020 IEEE.

β -Ga₂O₃ is considered to be 2 eV [34]. In both cases, the maximum electric field appears at the metal edge. However, as expected and as experimentally reported [35], the field is reduced in the guard ring structure, as shown in Fig. 2.7 (b).

We now explore the use of non-polar p-GaN as the guard ring material (Fig. 2.8(a)). The use of a magnesium-doped GaN guard ring enables electric field screening at the metal edges due to the presence of a quasi-neutral region. The activation energy for Mg in p-GaN is considered to be 0.2 eV [36]. The doping concentration is taken to be 10^{20} cm^{-3} (hole concentration = $8.2 \times 10^{18} \text{ cm}^{-3}$), with a guard ring thickness of $0.5 \text{ } \mu\text{m}$ and an anode voltage of 2000 V. The peak

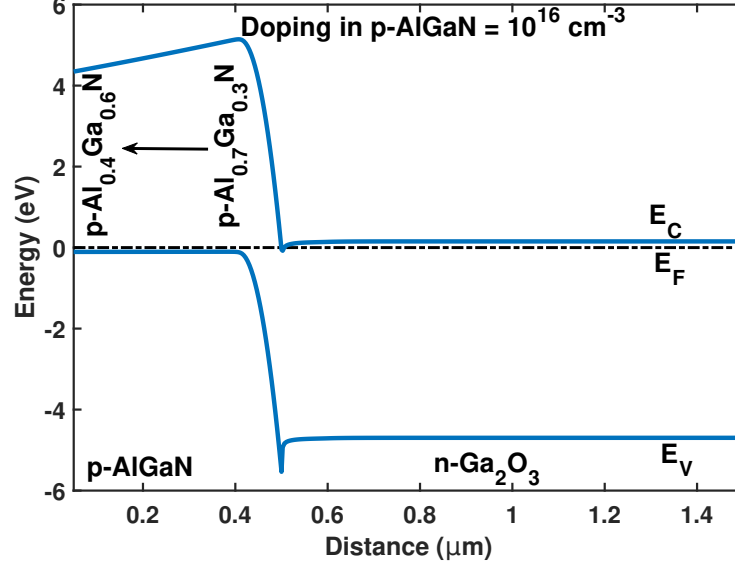


Figure 2.9: Equilibrium energy band diagram of the simulated SBD with polarization doped p-AlGaIn GR for $T_{GR} = 0.5 \mu m$ and $N_D = 10^{16} cm^{-3}$. Al composition is graded from 70 % to 40 % from the p-AlGaIn/n-Ga₂O₃ heterointerface to the SBD surface. Reprinted from Roy *et al.* [23] © 2020 IEEE.

electric field has now shifted to the p-GaN/n-Ga₂O₃ heterojunction, as shown in the electric field contour in Fig. 2.8 (a). Fig. 2.8 (b) illustrates the equilibrium energy band diagram of the p-GaN/n-Ga₂O₃ heterojunction. At an anode bias of 2000 V, the peak electric field at the p-GaN/n-Ga₂O₃ heterojunction exceeds GaN's critical field of 3.3 MV/cm. Simulations of the p-GaN guard ring configuration as a function of anode voltage are presented in Fig. 2.10. The breakdown voltage of this p-GaN guard ring configuration is 750 V.

To leverage the high critical electric field of β -Ga₂O₃, a more effective design would use a guard ring material with a higher critical field than β -Ga₂O₃. Consequently, we investigate a graded p-AlGaIn guard ring, with aluminum composition graded from 70% at the AlGaIn/Ga₂O₃ interface to 40% at the SBD surface. Fig. 2.8 (c) shows the electric field distribution for graded AlGaIn with a doping concentration of $10^{20} cm^{-3}$. However, because the ionization energy of Mg is high in AlGaIn with high Al content, realizing a high hole concentration becomes challenging. In fact, with an Mg concentration below $10^{18} cm^{-3}$, the peak electric field remains at the metal edge due to complete depletion of the GR. By growing c-axis oriented AlGaIn with a decreasing Al composition from the heterointerface to the surface, a three-dimensional

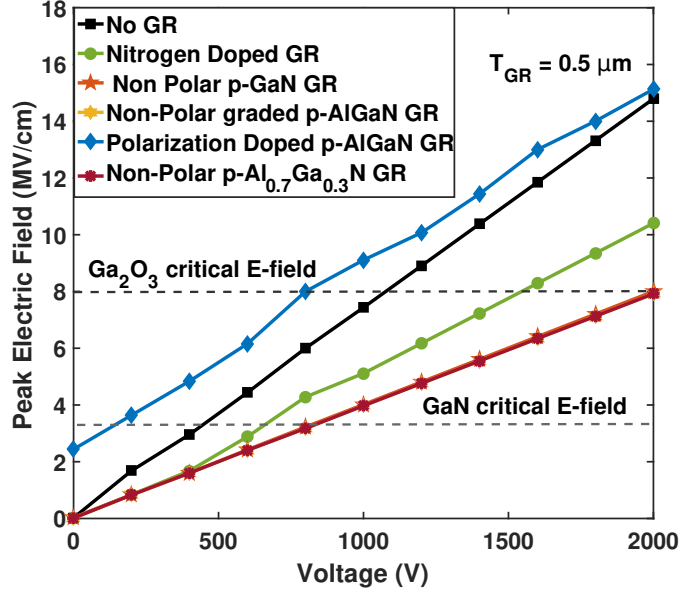


Figure 2.10: Peak electric field vs applied bias in SBD for different GR configurations with $0.5 \mu\text{m}$ of GR thickness and 10^{20} cm^{-3} of GR doping. Reprinted from Roy *et al.* [23] © 2020 IEEE.

slab of holes (3DHS) can be achieved through the polarization doping effect [37]. Fig. 2.8 (e) illustrates the electric field distribution in the polarization-doped $\text{p-Al}_x\text{Ga}_{1-x}\text{N}$ (where $x = 70\%$ at the heterojunction to 40% at the SBD surface) GR. The hole concentration in this guard ring structure significantly increases from the non-polar case (from 2×10^{17} to $6 \times 10^{18} \text{ cm}^{-3}$).

The band diagram for the polarization-doped polar graded p-AlGaIn guard ring configuration is shown in Fig. 2.8 (f). Here, the peak electric field shifts to the heterojunction, primarily due to the positive polarization sheet charge at the $\text{p-Al}_{0.7}\text{Ga}_{0.3}\text{N}/\text{n-Ga}_2\text{O}_3$ heterojunction. The energy bands rapidly drop at the polar p-AlGaIn/n-Ga₂O₃ interface, which further increases the electric field compared to the non-polar p-AlGaIn/n-Ga₂O₃ interface, as depicted in Fig. 2.8 (g). Even in the low-doped case, the energy bands steeply decline at the p-AlGaIn/n-Ga₂O₃ heterointerface, as shown in Fig. 2.9. Thus, a polarization-doped p-AlGaIn GR does not effectively reduce the peak electric field.

Fig. 2.10 presents the peak electric field versus applied bias for the SBD with six different guard ring structures. The doping concentration for the p-type guard rings is set at 10^{20} cm^{-3} , while for the nitrogen-doped case, it is 10^{16} cm^{-3} . The guard ring (GR) thickness is

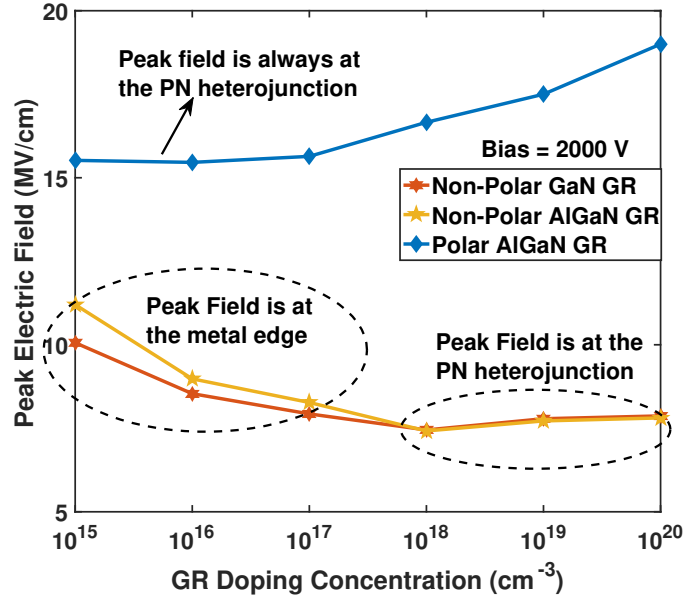


Figure 2.11: Peak electric field vs GR doping concentration with $0.5 \mu\text{m}$ of GR thickness and at an applied bias of 2000 V for different GR configurations. Reprinted from Roy *et al.* [23] © 2020 IEEE.

maintained at $0.5 \mu\text{m}$. The non-polar graded p-AlGaIn, ungraded p-AlGaIn, and p-GaN guard rings demonstrate the best performance in terms of peak electric field reduction. However, the SBD with the p-GaN guard ring exceeds its critical electric field of 3.3 MV/cm at an anode voltage of 750 V. The non-polar p-Al_xGa_{1-x}N GR, with a uniform Al composition ($x = 60\%$), has a critical electric field comparable to that of Ga₂O₃, allowing the breakdown voltage to reach up to 2000 V, as shown in Fig. 2.10. On the other hand, the electric field is significantly high for the SBD with the polarization-doped AlGaIn GR due to the strong field at the heterointerface.

Doping and thickness of the guard ring are critical parameters that would determine the amount of electric field screening and location of the peak electric field. We simulated the three guard ring configurations excluding the SBD with no GR and nitrogen-doped GR, as a function of Mg doping for a fixed thickness of $0.5 \mu\text{m}$ at a bias of 2000 V. Doping in the guard ring is found to determine the location of the peak electric field as shown in Fig. 2.11. For the polar p-AlGaIn guard ring, the peak electric field is always at the heterojunction irrespective of the doping. In the case of p-GaN and non-polar p-AlGaIn guard ring, the peak field is at the metal edge for doping concentrations lower than 10^{18} cm^{-3} . Since a high GR doping is not necessary

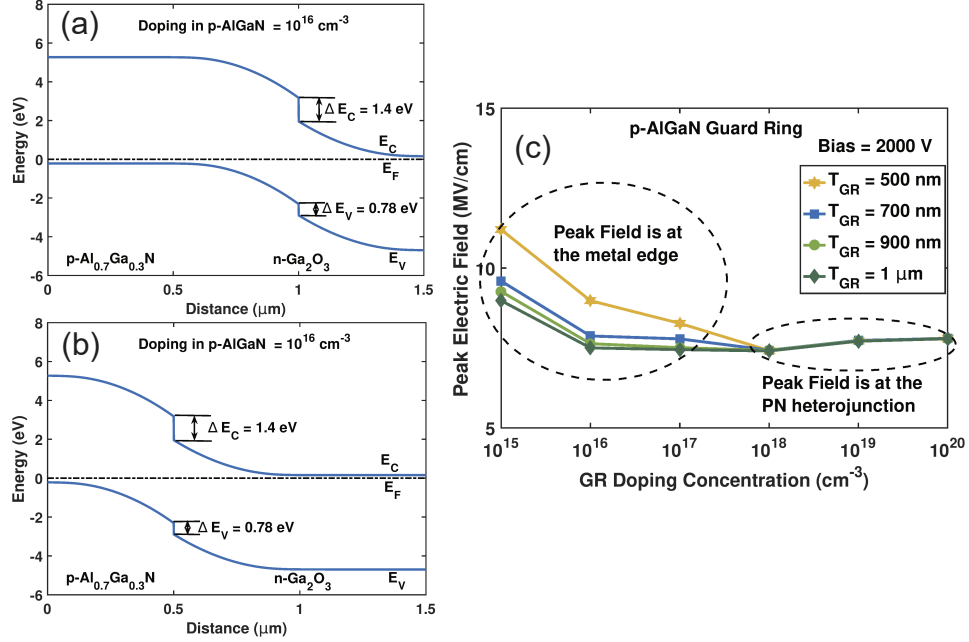


Figure 2.12: Equilibrium energy band diagram of the simulated SBD with nonpolar p-AlGa_{0.7}Ga_{0.3}N GR for (a) $T_{GR} = 0.5 \mu m$ (b) $T_{GR} = 1 \mu m$. Al composition is considered to be 70 %. (c) Peak electric field vs GR doping concentration with non-polar AlGa_{0.7}Ga_{0.3}N GR and at applied bias of 2000 V for different GR thicknesses. Reprinted from Roy *et al.* [23] © 2020 IEEE.

to minimize the peak field at the metal edge and since non polar graded and ungraded p-AlGa_{0.7}Ga_{0.3}N GR shows similar performance, compositional grading in the GR is not required, which will mitigate the challenge involving growth of graded epitaxial layer of AlGa_{0.7}Ga_{0.3}N inside the pocket of Ga₂O₃.

The doping level and thickness of the guard ring are critical parameters that dictate both the degree of electric field screening and the location of the peak electric field. We simulated the three guard ring configurations, excluding the SBD without a GR and the nitrogen-doped GR, as a function of Mg doping with a fixed thickness of $0.5 \mu m$ at a bias of 2000 V. As shown in Fig. 2.11, doping in the guard ring significantly influences the peak electric field's location. For the polar p-AlGa_{0.7}Ga_{0.3}N guard ring, the peak electric field remains at the heterojunction regardless of the doping level. In contrast, for the p-GaN and non-polar p-AlGa_{0.7}Ga_{0.3}N guard rings, the peak field is located at the metal edge for doping concentrations below $10^{18} cm^{-3}$. Since high GR doping is not required to minimize the peak field at the metal edge and both non-polar graded and ungraded p-AlGa_{0.7}Ga_{0.3}N GRs exhibit similar performance, compositional grading in the GR

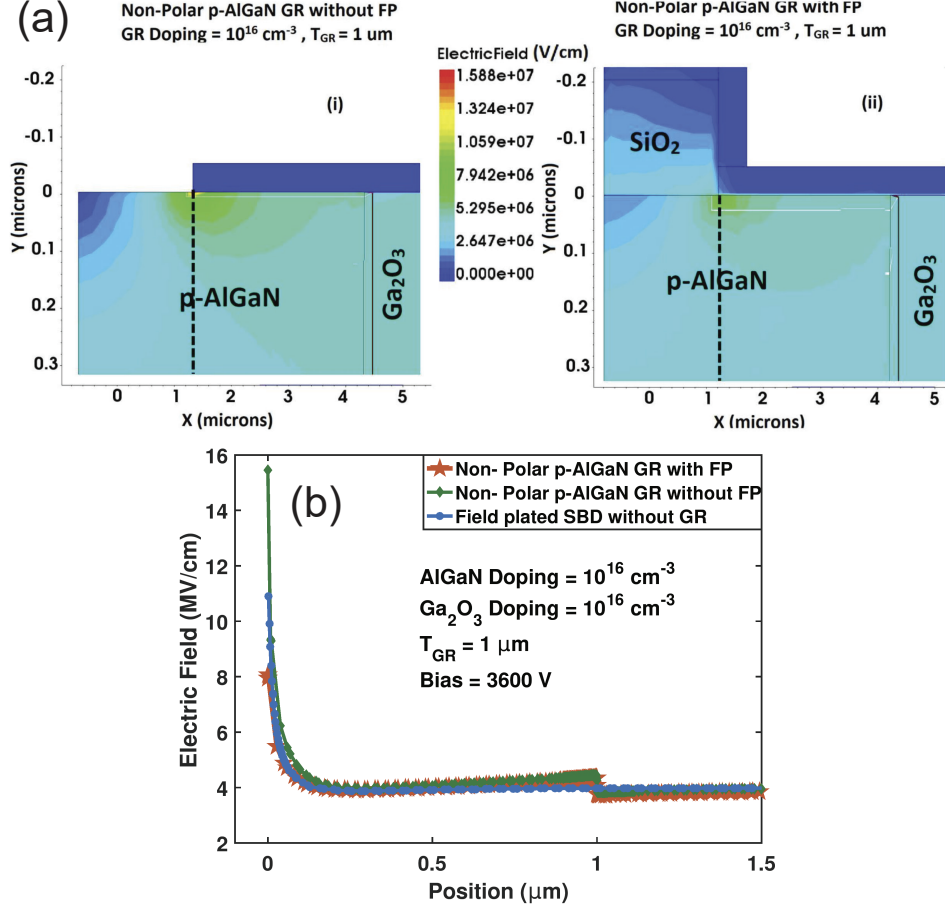


Figure 2.13: Equilibrium energy band diagram of the simulated SBD with nonpolar p-AlGaIn GR for (a) $T_{GR} = 0.5 \text{ }\mu\text{m}$ (b) $T_{GR} = 1 \text{ }\mu\text{m}$. Al composition is considered to be 70 %. (c) Peak electric field vs GR doping concentration with non-polar AlGaIn GR and at an applied bias of 2000 V for different GR thicknesses. Reprinted from Roy *et al.* [23] © 2020 IEEE.

is unnecessary. This approach also reduces the complexity associated with growing a graded AlGaIn epitaxial layer within the Ga_2O_3 pocket.

The electric field simulations clearly establish the comparably superior performance of the non-polar p-AlGaIn guard ring configuration. We now focus on this configuration in particular, studying the effect of guard ring thickness. In the case of low-doped guard rings, achieving a quasi-neutral region requires sufficient thickness to realize an undepleted region near the metal edge. The equilibrium energy band diagrams for non-polar graded p-AlGaIn GRs with low doping (10^{16} cm^{-3}) at two different thicknesses are shown in Fig. 2.12 (a) and Fig. 2.12 (b). The presence of a quasi-neutral region near the metal, as seen with the thicker, low-doped guard ring in Fig. 2.12 (b), is beneficial for electric field screening. This quasi-neutral region

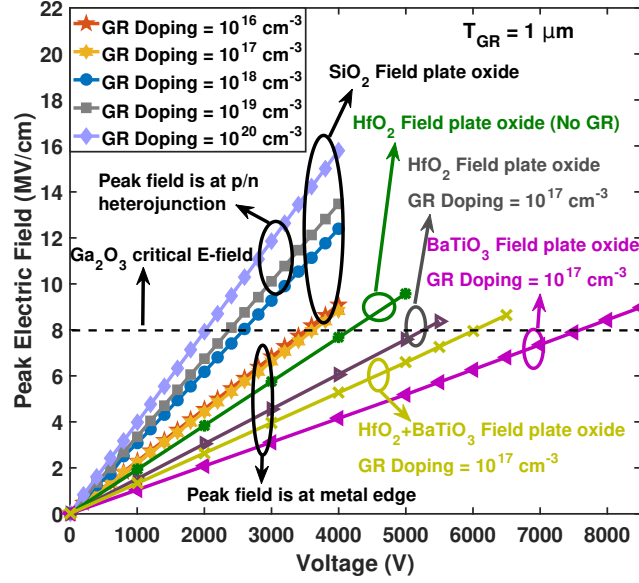


Figure 2.14: Equilibrium energy band diagram of the simulated SBD with nonpolar p-AlGaIn GR for (a) $T_{GR} = 0.5 \mu m$ (b) $T_{GR} = 1 \mu m$. Al composition is considered to be 70 %. (c) Peak electric field vs GR doping concentration with non-polar AlGaIn GR and at applied bias of 2000 V for different GR thicknesses. Reprinted from Roy *et al.* [23] © 2020 IEEE.

allows the depletion region to expand under high reverse bias. Fig. 2.12 (c) summarizes the effect of guard ring thickness as a function of Mg doping. At a bias of 2000 V, the peak electric field can be reduced from 9 MV/cm to 7.5 MV/cm with a guard ring doping of $10^{16} cm^{-3}$. The peak electric field decreases with increasing doping, up to a concentration of $10^{18} cm^{-3}$. Beyond this point, as GR thickness increases, the peak electric field continues to decrease until reaching a doping level of $10^{17} cm^{-3}$. At higher concentrations, the peak electric field shifts to the pn-heterojunction, and GR thickness has no further effect. In this regime, a field-plate is unnecessary, as the peak field region is buried.

To further improve electric field management, we select guard ring configuration B, with a thickness of $1 \mu m$ and a doping concentration of $10^{16} cm^{-3}$. In this configuration, the peak electric field occurs at the metal edge. We now explore the potential for further breakdown voltage enhancement by introducing a field plate. Fig. 2.13 (a) illustrates the electric field distribution in the SBD at a GR thickness of $1 \mu m$ and a bias voltage of 3600 V: (i) without a field-plate, and (ii) with a field-plate. A 200 nm SiO_2 layer is employed as the field-plate

oxide. For comparison, Fig. 2.13 (b) shows a field-plated SBD without a guard ring. Field plating significantly reduces the peak electric field compared to an SBD with only a guard ring. However, incorporating both a field-plate and a thick p-AlGaIn GR results in a dramatic reduction of the peak electric field at the metal edge. Once again, the peak electric field decreases with increasing doping concentration, up to 10^{17} cm^{-3} . Thus, the optimal design combines a thick, low-doped p-AlGaIn guard ring with a field-plate for enhanced electric field management.

Fig. 2.14 illustrates the effect of field plating on reducing the peak electric field in the SBD with a non-polar p-AlGaIn guard ring (GR). As shown, for doping concentrations below 10^{18} cm^{-3} , field plating significantly reduces the electric field at the metal edge, allowing the field to reach the $\beta\text{-Ga}_2\text{O}_3$ critical electric field of 8 MV/cm at a bias voltage of approximately 3600 V. At higher doping levels (above 10^{17} cm^{-3}), the field plating effect diminishes as the peak electric field shifts from the metal edge to the pn-heterojunction. In addition, using a high- κ dielectric (such as HfO_2 , with a relative permittivity of 22) as the field-plate oxide, in conjunction with the GR, further reduces the peak electric field. This setup reaches the $\beta\text{-Ga}_2\text{O}_3$ critical field at a reverse bias of 5200 V, surpassing the highest reported breakdown voltages for vertical SBDs with a $10 \mu\text{m}$ drift layer [38]. The significant permittivity difference between the semiconductor and dielectric induces polarization-bound charges within the dielectric, which balances the depletion charge at the semiconductor interface [33], [39], [40], resulting in a flattened electric field profile and reducing its peak value. For comparison, an SBD with an HfO_2 field-plate oxide but without a GR achieves a breakdown voltage of 4300 V, indicating that the GR improves the breakdown voltage by 900 V. Using extremely high- κ materials, like BaTiO_3 (with a permittivity of 300), as the field-plate oxide can further enhance breakdown voltage, reaching up to 7800 V with a GR. However, BaTiO_3 lacks a conduction band offset with $\beta\text{-Ga}_2\text{O}_3$, which may lead to charge trapping within the dielectric. To mitigate this, we analyzed a stacked dielectric configuration using HfO_2 (5 nm) + BaTiO_3 (295 nm). This stack maintains a high effective dielectric constant of 248, while the conduction band offset at the dielectric/ Ga_2O_3 interface potentially prevents bulk electron trapping by blocking current flow

through the dielectric during forward conduction. Utilizing this stacked dielectric with a thick guard ring yields a breakdown voltage of 6200 V.

Among all the devices described, the SBD with a non-polar p-AlGaN guard ring (GR) combined with a field-plate and a high- κ field-plate oxide emerges as the best choice for reducing the electric field. The thick β -Ga₂O₃ epilayers (approximately 10 μ m) on (010) β -Ga₂O₃ substrates can be grown using hydride vapor phase epitaxy (HVPE), as previously demonstrated [41], [42]. Selective area epitaxy of AlGaN GRs within Ga₂O₃ trench pockets can be performed using metal-organic chemical vapor deposition (MOCVD) [43], [44]. We recognize that AlGaN heteroepitaxy on Ga₂O₃ may compromise material quality, necessitating extensive growth and process optimizations. By implementing the design concepts explored in this work, a Ga₂O₃ SBDs with GRs in conjunction with field-plates will significantly increase the already high FOM achieved in current Ga₂O₃ power SBDs. For instance, with a breakdown voltage of 6200 V and an estimated R_{on-sp} of 3.1 m Ω -cm², assuming a mobility of 200 cm²/V.s [45], we expect to achieve an exceptionally high FOM of 10.8 GW/cm².

2.4 Summary

This chapter introduced and discussed various edge termination techniques employed in high-voltage power devices. A comprehensive design guideline for field plates was also presented, utilizing electrostatic analysis to emphasize that the field plate dimensions, dielectric thickness, and dielectric constant of the dielectric material are critical parameters for optimizing power diodes to achieve maximum breakdown voltage.

The challenges associated with achieving an efficient guard ring configuration for electric field management were addressed. A novel method to enhance the breakdown voltage of Schottky barrier diodes (SBDs) through the use of a p-doped III-nitride guard ring was proposed and substantiated by detailed device simulations. This approach effectively circumvents the challenge posed by the lack of p-type doping in β -Ga₂O₃. The simulations demonstrated that

an SBD with a thick, low-doped non-polar p-AlGaN guard ring, when combined with a field plate and high- κ dielectric, provides optimal electric field reduction. Additionally, incorporating a field plate with a high permittivity field plate oxide in low-doped guard ring configurations further mitigates the electric field at metal edges. Future research into the AlGaN/Ga₂O₃ heterointerface properties is expected to deepen our understanding and enhance the development of heterojunction-based structures for high-performance power electronic devices.

A key challenge in the proposed method lies in growing thick AlGaN layers with high Al composition on β -Ga₂O₃, as well as achieving high doping concentrations, particularly for p-type doping. However, the design guidelines provided here could be adapted for other p-type materials that can be used as guard rings, such as p-NiO, which has already been demonstrated. This methodology is also applicable to other wide bandgap materials, such as SiC or GaN, to achieve high breakdown voltages.

As discussed in this chapter, mitigating electric field crowding at the device edges is essential for the efficient and reliable realization of power devices. The next chapter presents a demonstration of field-plated SBDs that employ extreme permittivity dielectric materials as field plate dielectrics to significantly reduce electric field crowding at the device edges.

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Chapter 3

β -Ga₂O₃ Extreme Permittivity Dielectric Field-Plated Schottky Barrier Diodes

3.1 Introduction

In the previous chapter, a design guideline for Schottky Barrier Diode (SBD) design was presented, based on electrostatic analysis. It demonstrated that the field plate dimensions, dielectric thickness, and dielectric constant of the dielectric material are critical parameters for minimizing electric field crowding at the device edges.

In conventional field-plated SBDs, low- κ dielectrics such as SiO₂ or Al₂O₃ are more commonly used [1], [2]. Lateral field spreading within the semiconductor drift region is a crucial aspect of field-plated designs, and low- κ dielectrics are typically inefficient at spreading the electric field laterally beyond the field plate edge. This results in significant electric field crowding at the field-plate edge, particularly at the metal/dielectric interface. While this issue is less impactful for narrow-bandgap materials (where the dielectric breakdown field is typically orders of magnitude higher than that of the semiconductor), it becomes a significant challenge for ultra-wide bandgap materials. In these materials, dielectric breakdown fields are often comparable to those of the semiconductor. Consequently, the electric field at the field plate

edge can sometimes surpass the dielectric's breakdown field before the electric field in the semiconductor reaches the semiconductor's critical field. This can lead to premature dielectric failure and, ultimately, device breakdown.

This chapter introduces an alternative strategy that utilizes high-permittivity dielectrics as the field plate dielectric. An experimental demonstration of high-permittivity dielectric field plates on various β -Ga₂O₃ drift layers is presented, showcasing their superior field plate efficiency. Additionally, this chapter includes an analysis of area normalization and its effect on the specific on-resistance of vertical power devices, along with calculations of power losses.

3.2 high- κ vs low- κ Dielectric for Field Plates

The use of high-permittivity dielectrics as field plate dielectrics reduces the electric field at field plate edges due to the lateral distribution of electric fields [3], [4]. This effect is illustrated in Fig. 3.1. As discussed in Chapter 1, charge build-up at the metal corners results in a corresponding accumulation of negative charges at the field plate edge within the depletion region. For low- κ dielectrics, the low dielectric constant causes a significant potential drop within the dielectric, which weakens the fringing electric field and limits the lateral spread of the depletion region. Consequently, substantial charge buildup occurs near the field plate edge within the depletion region, as shown in Fig. 3.1 (a). As the charge density increases in this area, the electric field near the metal edges also rises (Fig. 3.1 (c)), according to Poisson's equation:

$$\frac{\partial E(x)}{\partial x} = \frac{\rho}{\epsilon_S} \quad (3.1)$$

where $E(x)$ is the x-component of the electric field, ρ is the charge density, and ϵ_S is the semiconductor's permittivity.

In contrast, high- κ dielectric field plates experience minimal electric field drop across the dielectric due to their higher dielectric constant. This results in a stronger fringing electric field between the metal and semiconductor, promoting the lateral spread of the depletion region, as

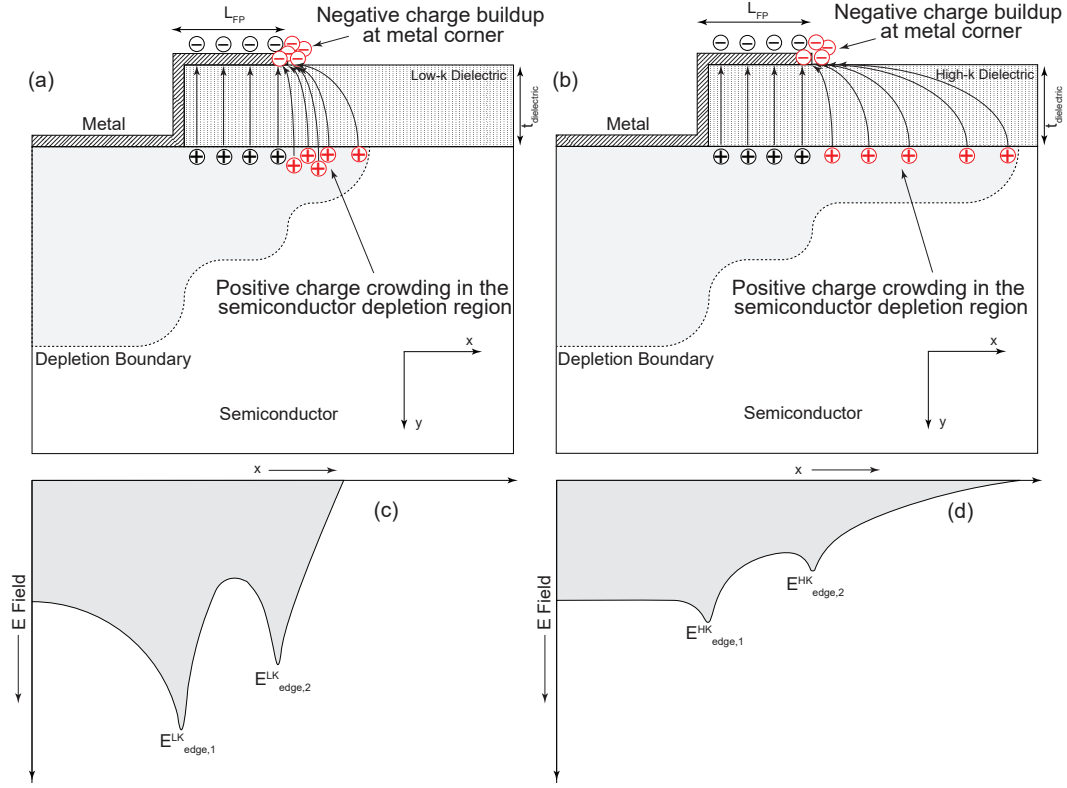


Figure 3.1: An illustration of the depletion region and electric field (along x direction) profile for (a) (c) low- κ field-plated and (b) (d) high- κ field-plated SBDs at reverse bias.

depicted in Fig. 3.1 (c). Consequently, the charge density near the field plate edge is reduced, and according to (3.1), the electric field at the edges is also lowered, as shown in Fig. 3.1 (d). Thus, using a high- κ dielectric material as the field plate oxide effectively reduces electric field crowding at the device edges, which helps to prevent premature breakdown of the device.

3.3 High permittivity Dielectric Materials

The question now becomes which material offers a sufficiently high relative permittivity to be effective in edge terminations for power electronics. HfO_2 , with a dielectric constant of ~ 25 , has been widely studied as a high- κ dielectric material for gate oxides in Si and Ge CMOS technology [5]–[7]. Other high-permittivity dielectrics include ZrO_2 ($\epsilon_r = 25$), Ta_2O_5 ($\epsilon_r = 22$), La_2O_3 ($\epsilon_r = 30$), and TiO_2 ($\epsilon_r = 80$) [8]. While these materials are effective for increasing gate capacitance in low-power electronics, their dielectric constants are not high enough to provide

sufficient lateral electric field distribution in high-power electronics.

Among these materials, TiO_2 has relatively higher dielectric constant of 80 (theoretical), making it a potential choice for high-voltage applications. However, in practical settings, the dielectric constant of TiO_2 is often closer to 50 [9], [10]. Our own experiments with TiO_2 deposited on $\beta\text{-Ga}_2\text{O}_3$ have indicated a dielectric constant in the range of 35 to 50, which may limit its effectiveness for high-power applications.

In contrast, complex oxides such as BaTiO_3 and SrTiO_3 stand out for their extremely high permittivities, with stoichiometric films exhibiting dielectric constants exceeding 1000 [11]–[13]. SrTiO_3 , in particular, has been reported to reach dielectric constants as high as 25,000 at low temperatures [14]. These exceptionally high permittivities make them highly effective for managing electric field crowding and other field control challenges in power devices. Xia et al. demonstrated a $\text{BaTiO}_3/\beta\text{-Ga}_2\text{O}_3$ heterojunction diode achieving a reverse breakdown field of 5.7 MV/cm, with a BaTiO_3 dielectric constant of 260. Additional studies have also explored the use of high- κ dielectric materials for field management in $\beta\text{-Ga}_2\text{O}_3$ and GaN-based power devices [4], [15].

Additionally, superlattices composed of medium- or low- κ dielectrics can exhibit even higher effective permittivities due to Maxwell-Wagner relaxation effects [16]. By layering BaTiO_3 and SrTiO_3 in a superlattice structure, dielectric constants of 800 to 900 have been achieved, compared to 300 to 400 in individual films [17], even at 1 MHz frequencies, which is well above the operating frequencies of modern power converters. These high permittivity values are sufficient for field management in power electronic applications. In the following section, a $\beta\text{-Ga}_2\text{O}_3$ -based Schottky Barrier Diode utilizing this type of extreme permittivity dielectric as a field-plate oxide for edge termination will be presented.

3.4 β -Ga₂O₃ Schottky Barrier Diode with high- κ Dielectric Field Plates

In this section, we demonstrate a β -Ga₂O₃ field-plated vertical Schottky Barrier Diode (SBD) utilizing a BaTiO₃/SrTiO₃ superlattice dielectric layer. Two devices were fabricated on β -Ga₂O₃ drift layers grown using Halide Vapor Phase Epitaxy (HVPE): one with a thickness of 1.7 μm with a doping concentration of $9 \times 10^{16} \text{ cm}^{-3}$ and the other with a thickness of 10 μm with a doping concentration of $8 \times 10^{15} \text{ cm}^{-3}$. Under high reverse bias, both field-plated devices operated beyond the punch-through regime, whereas the non-field-plated devices exhibited breakdown before reaching punch-through. The performance characteristics of punch-through and non-punch-through devices are discussed in the following subsection.

3.4.1 Non-Punch-through vs Punch-through Designs

The analysis provided in Chapter 1 on BFOM and field plate designs assumes a non-punch-through scenario, where the electric field profile is triangular. In a punch-through scenario, however, the depletion region depth reaches the drift layer thickness, resulting in the electric field profile shifting from a triangular to a trapezoidal shape, as illustrated in Fig. 3.2.

In the non-punch-through case, the relationship between R_{on-sp}^{NPT} and V_{BR}^{NPT} is as described in Chapter 1, where R_{on-sp}^{NPT} and V_{BR}^{NPT} are the specific on-resistance and breakdown voltage for non-punch-through device respectively.

$$R_{on-sp}^{NPT} = \frac{4(V_{BR}^{NPT})^2}{\epsilon_S \mu_n E_C} \quad (3.2)$$

As illustrated in Fig. 3.2 (b), the electric field does not reach zero at the bottom of the drift layer in a punch-through scenario. The electric field at the drift layer's bottom end can be expressed as:

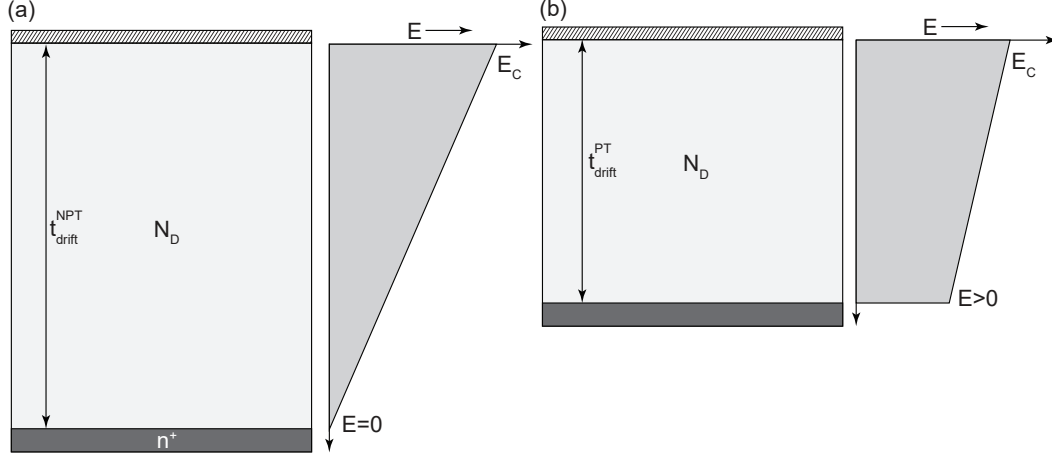


Figure 3.2: An illustration of the electric field profile for (a) non-punch-through and (b) punch-through scenarios at reverse bias.

$$E(t_{drift}^{PT}) = E_C - \frac{qN_D t_{drift}^{PT}}{\epsilon_S} \quad (3.3)$$

The device's breakdown voltage, represented by the area under the trapezoidal field profile, can be formulated as:

$$V_{BR}^{PT} = E_C t_{drift}^{PT} - \frac{qN_D (t_{drift}^{PT})^2}{2\epsilon_S} \quad (3.4)$$

For the punch-through case, using $R_{on-sp}^{PT} = \frac{t_{drift}^{PT}}{q\mu_n N_D}$ and substituting for t_{drift}^{PT} , the relationship between specific on resistance and breakdown voltage for the punch-through case can be written as,

$$V_{BR}^{PT} = qN_D \mu_n E_C R_{on-sp}^{PT} - \frac{q^3 N_D^3 \mu_n^2}{2\epsilon_S} (R_{on-sp}^{PT})^2 \quad (3.5)$$

It can be seen from (3.5) that unlike non-punch-through case, V_{BR} - R_{on-sp} relationship depends on N_D . In addition, the punch-through condition imposes a maximum limit on the breakdown voltage, determined by the real root of the quadratic equation (3.5), which can be expressed as:

$$V_{BR}^{PT} < \frac{\epsilon_S E_C^2}{2qN_D} \quad (3.6)$$

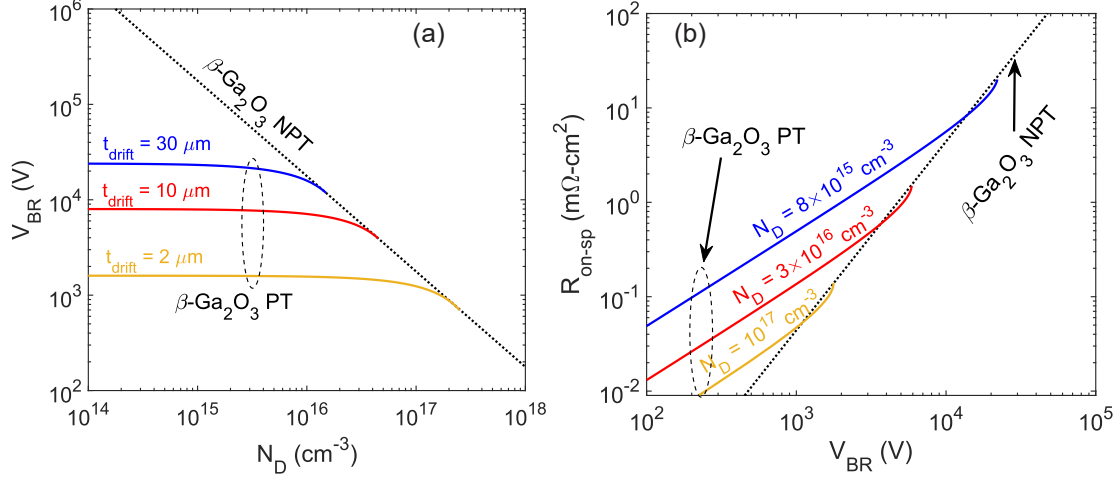


Figure 3.3: Breakdown voltage vs specific on-resistance plot for punch-through conditions for three different doping concentrations.

where, $V_{BR} = \frac{\epsilon_s E_C^2}{2qN_D}$ holds true exclusively for non-punch-through case as established by the BFOM (Eq. 1.1). The V_{BR} - R_{on-sp} relationship is plotted in Fig. 3.3 (b) for β -Ga₂O₃ assuming a doping independent E_C of 8 MV/cm.

Fig. 3.3 (a) presents the breakdown voltage versus doping concentration for various drift layer thicknesses under punch-through conditions, based on equation (3.4). Due to the truncation of the electric field at the end of the drift layer, the breakdown voltage of a punch-through diode is reduced for any given doping concentration and drift layer thickness. As illustrated in Fig. 3.3 (b), punch-through devices demonstrate a performance advantage over non-punch-through devices only within a narrow range. Consequently, punch-through devices generally exhibit inferior performance compared to non-punch-through devices, which have a one-dimensional field distribution.

In the following subsection, we present a demonstration of β -Ga₂O₃ punch-through diodes utilizing high- κ dielectric field plates. The devices operate in the punch-through regime due to the combination of thin drift layers and the chosen doping concentrations. This approach aims to leverage the high- κ dielectric material to enhance field distribution, even in a punch-through configuration.

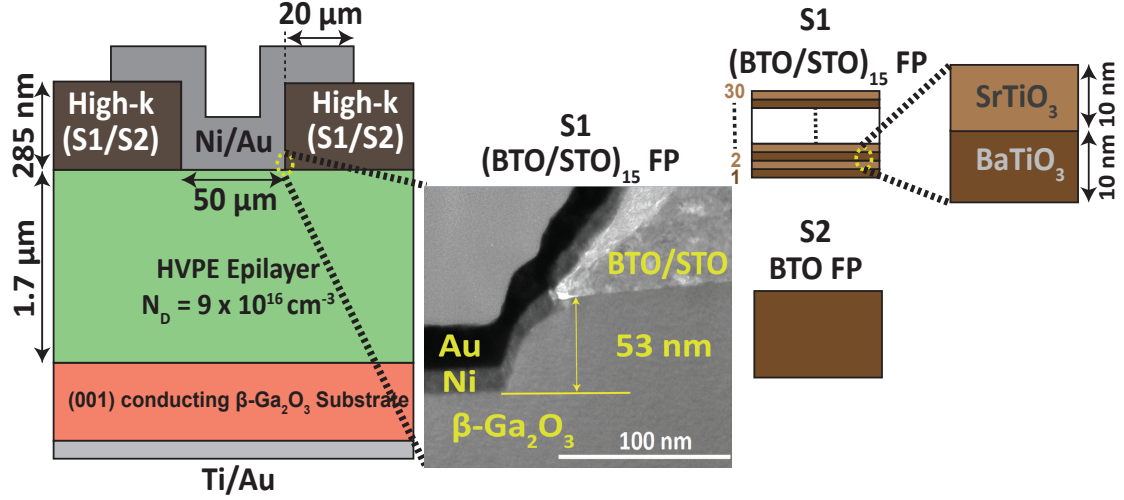


Figure 3.4: Schematic of Ga_2O_3 SBD with high- κ dielectric field plate, where S1 is the $(\text{BTO}/\text{STO})_{15}$ dielectric field oxide for $(\text{BTO}/\text{STO})_{15}$ FP SBD and S2 is the BTO dielectric field oxide for BTO FP SBD. The expanded region shows the TEM image of the anode edge of the $(\text{BTO}/\text{STO})_{15}$ FP SBD. Reprinted from Roy *et al.* [18] © 2021 IEEE.

3.4.2 Device Fabrication of $\beta\text{-Ga}_2\text{O}_3$ high- κ Field-plated SBD with Thin Drift Layer

The fabrication of the field-plated SBD, as illustrated in Fig. 3.4, began with the growth of (001) $\beta\text{-Ga}_2\text{O}_3$ epilayers. These layers were deposited using a custom-designed, subatmospheric vertical Halide Vapor Phase Epitaxy (HVPE) reactor with GaCl and O_2 precursors [19]. The GaCl was produced in situ by flowing Cl_2 over high-purity (7N) liquid Ga and was transported to the wafer surface through a quartz injector. By controlling the GaCl molar flow rates, a growth rate of approximately $5 \mu\text{m/hr}$ was achieved.

Following the growth, the as-grown samples were dipped in HF and HCl for 5 minutes to remove any residual oxides. Fifteen alternating layers of 10 nm BaTiO_3 and SrTiO_3 $[(\text{BTO}/\text{STO})_{15}]$ were then deposited via RF sputtering at room temperature in an oxygen/argon ambient (1:10 O_2/Ar ratio). The deposition was conducted at a sputtering power of 140 W and a chamber pressure of 5 mTorr, resulting in a total measured thickness of ~ 285 nm. After deposition, the sample underwent annealing at 700°C in an oxygen environment for 30 minutes to enhance the dielectric constant.

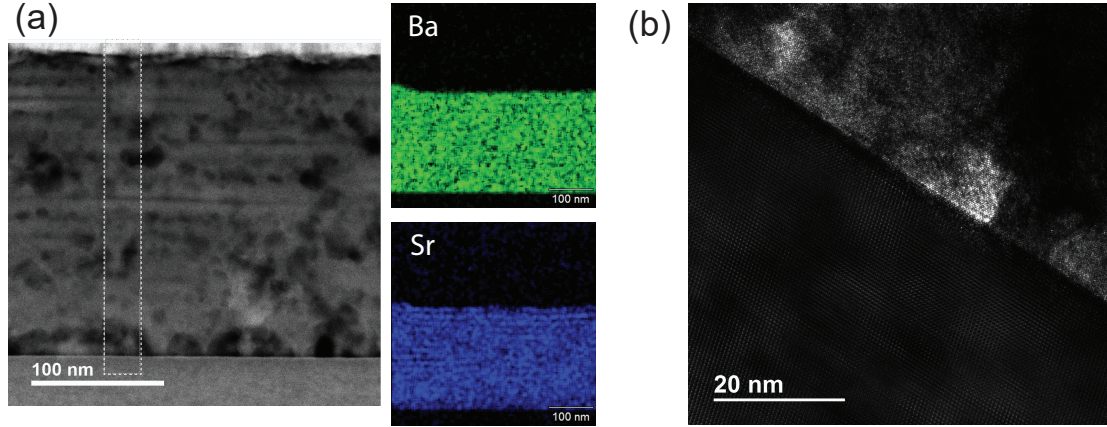


Figure 3.5: (a) EDS map of Ba and Sr in the (BTO/STO)₁₅ superlattice stack. (b) A high resolution TEM image of the β -Ga₂O₃/(BTO/STO)₁₅ stack interface.

Next, the sample was patterned through standard photolithography, and the active regions were exposed using SF₆/Ar dry etching. To ensure complete removal of the dielectric, overetching of 50 nm was performed, confirmed via transmission electron microscopy (TEM) imaging (Fig. 3.4). Energy-dispersive X-ray spectroscopy (EDS) mapping of the (BTO/STO)₁₅ layer indicated some intermixing of Sr and Ba as shown in Fig. 3.5, possibly due to the high-temperature annealing step. A high resolution TEM image of the β -Ga₂O₃/(BTO/STO)₁₅ stack is also provided in Fig. 3.5.

Subsequent to etching, Ni/Au (20/40 nm) metal stacks were deposited on the sample using electron-beam evaporation. Finally, Ti/Au (50/100 nm) ohmic contacts were sputter-deposited on the back side of the sample. For comparison, additional samples were fabricated with only BaTiO₃ (BTO) as the field plate oxide and a reference SBD without any field plate using the same process flow.

3.4.3 Dielectric Constant Extraction of high- κ Dielectrics

The dielectric constants of the (BTO/STO)₁₅ and BaTiO₃ layers were determined by depositing them on an MOCVD-grown (010) β -Ga₂O₃ substrate with a δ -doped layer, following the approach outlined by Xia et al. [20]. Capacitance measurements were taken by comparing the capacitance corresponding to the peak of the δ -doped layer, both with and without the

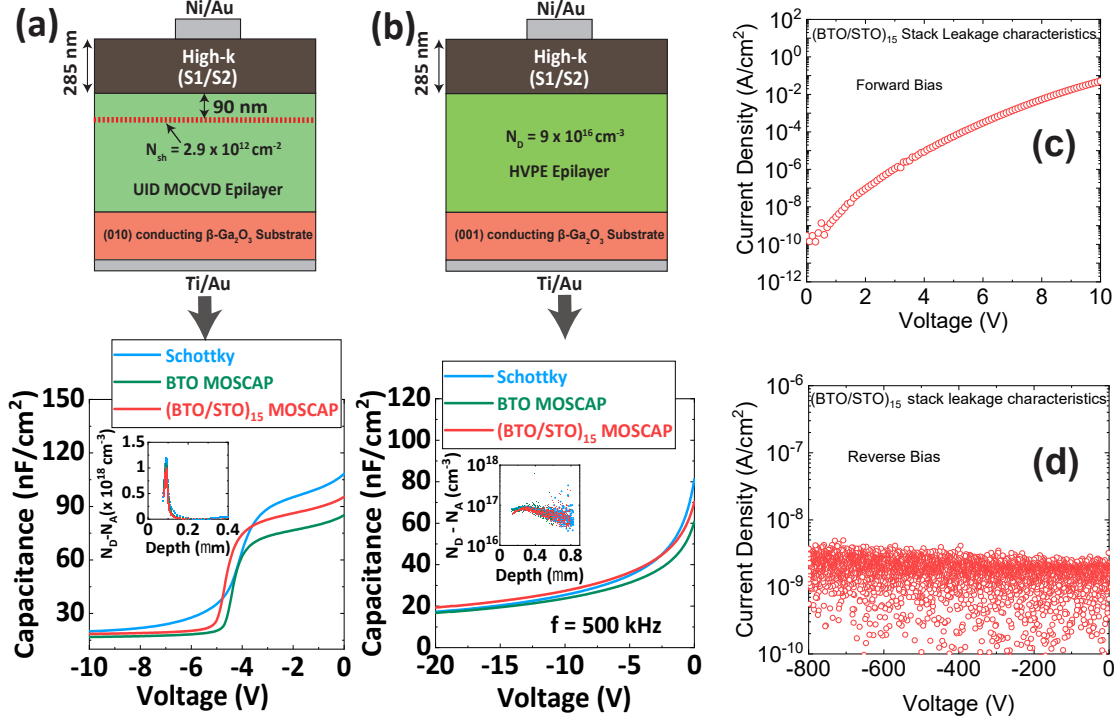


Figure 3.6: (a) CV characteristics for an MOCVD grown delta-doped sample with and without the dielectrics. (b) CV characteristics for the actual samples with and without the dielectrics. The inset of (a) and (b) shows the apparent charge density for the two samples. (c) Forward and (d) reverse leakage characteristics for the (BTO/STO)₁₅/β-Ga₂O₃ MOSCAP. Reprinted from Roy *et al.* [18] © 2021 IEEE.

dielectric layers, as illustrated in Fig. 3.6 (a). This method was chosen since β-Ga₂O₃ lacks a conduction band offset with either BaTiO₃ or SrTiO₃, making it impossible to extract C_{ox} under accumulation due to current conduction before the accumulation state is achieved, as depicted in Fig. 3.6 (c). This results in substantial conduction loss during capacitance-voltage (C-V) measurements at forward bias.

For the δ-doped films, where the precise location of the δ-doping is known from reverse-bias C-V characterization on δ-doped β-Ga₂O₃ film with Schottky contact, the dielectric capacitance can be extracted under reverse bias by considering the series combination of the dielectric capacitance and the δ-doped layer capacitance. The capacitance per unit area of the dielectric, $C_{dielectric}$, for the MOSCAP on the δ-doped film can be expressed as follows:

$$C_{dielectric} = \frac{C_{ds}C_{dM}}{C_{ds} - C_{dM}} \quad (3.7)$$

where C_{ds} is the capacitance per unit area corresponding to the peak of the δ -doping without the dielectric layer, and C_{dM} is the capacitance per unit area at the peak with the dielectric layer. Using $C_{dielectric}$, the dielectric constant ϵ_r of the materials can be calculated as:

$$\epsilon_r = \frac{C_{dielectric} \times t_{dielectric}}{\epsilon_0} \quad (3.8)$$

where $t_{dielectric}$ is the dielectric layer thickness, and ϵ_0 is the permittivity of free space. Using (3.8), the dielectric constants were determined to be ~ 325 for the (BTO/STO)₁₅ layer and ~ 142 for the BTO layer alone.

3.4.4 Current-Voltage and breakdown characteristics of β -Ga₂O₃ high- κ Field-plated SBD with Thin Drift Layer

To examine the influence of dielectric deposition and thermal annealing on the apparent charge density, capacitance-voltage (C-V) measurements were conducted on the fabricated samples, utilizing the previously extracted dielectric constants. The results, as shown in Fig. ?? (b), display the C-V profiles for the Schottky diode, the BaTiO₃ (BTO) MOSCAP, and the (BTO/STO)₁₅ MOSCAP. The inset in Fig. 3.6 (b) reveals a net doping concentration of approximately $8.9 \times 10^{16} \text{ cm}^{-3}$.

The current-voltage characteristics are presented in both logarithmic and linear scales in Fig. 3.7 (a) and Fig. 3.7 (b), respectively. The ideality factors (η) were calculated as 1.04 for the non-field-plated SBD, 1.1 for the BTO field-plated SBD, and 1.07 for the (BTO/STO)₁₅ field-plated SBD. The current was normalized by considering the area of the anode's active region for both the non-field-plated and field-plated SBDs, as the current through the dielectric was negligible across the operational voltage range (0–2 V) in the MOSCAP structures.

The specific on-resistance (R_{on-sp}) was determined from the linear fit of the I-V data, yielding values of 0.33, 0.34, and 0.35 $m\Omega\text{-cm}^2$ for the non-field-plated, BTO field-plated, and (BTO/STO)₁₅ SBDs, respectively. The lowest differential on-resistance was 0.32, 0.34, and 0.32 $m\Omega\text{-cm}^2$ for the non-field-plated, BTO field-plated, and (BTO/STO)₁₅ SBDs, respectively.

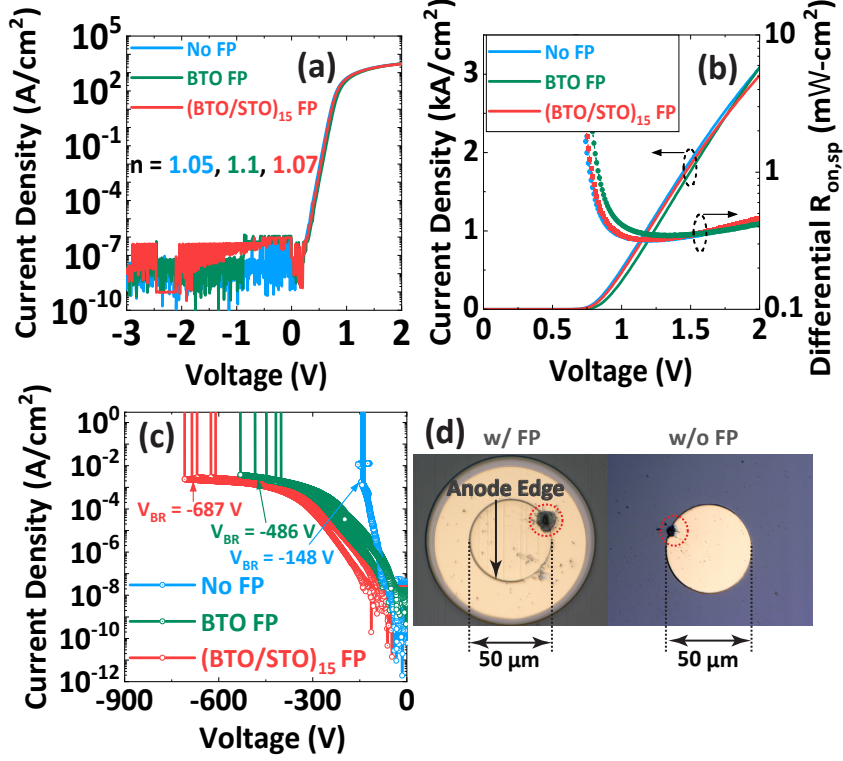


Figure 3.7: (a) Log scale, & (b) linear scale IV characteristics of non-FP SBD, BTO FP SBD, and (BTO/STO)₁₅ FP SBD. (c) Breakdown characteristics of the three different SBD structures, and (d) Microscope image of the fabricated device showing breakdown location for the representative SBDs with and without FP. Reprinted from Roy *et al.* [18] © 2021 IEEE.

These nominally similar values of ideality factors and on-resistances across the samples suggest that neither the dielectric deposition nor the subsequent dry etching process degraded the drift layer or the metal/semiconductor interface.

The reverse breakdown characteristics of the SBDs, measured using the Keysight B1505A, are shown in Fig. 3.7 (c) for devices with no field plate, a BTO field plate, and a (BTO/STO)₁₅ field plate. The extracted breakdown voltages for the three devices are 148 V, 486 V, and 687 V, respectively. Optical microscope images, displayed in Fig. 3.7 (d), show breakdown craters at the anode edges for both the FP and non-FP SBDs, indicating the locations where breakdown occurred. The significant increase in breakdown voltages for the high permittivity dielectric field plate oxide suggests enhanced edge termination and reduced field crowding at the device edges, attributable to the high permittivity of the FP dielectric.

Electric field simulations for these three SBD structures were conducted using Sentaurus TCAD software [21]. The resulting field profiles are plotted in Fig. 3.8(a), (b), and (c). Except

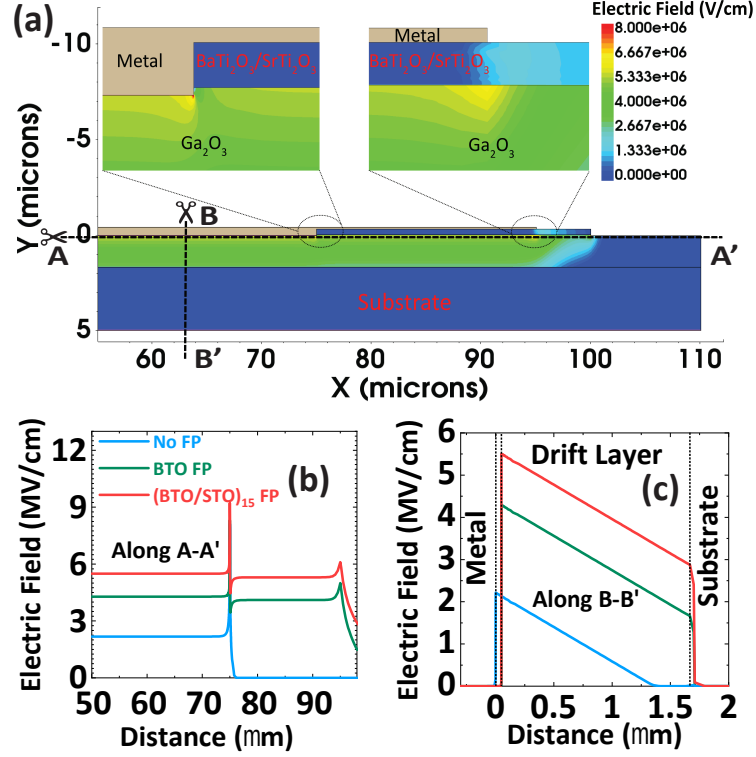


Figure 3.8: (a) Electric field contour plot of the $(\text{BTO}/\text{STO})_{15}$ FP SBD, (b) & (c) Simulated electric field profile for the three different SBDs for cutlines along the lateral and vertical directions respectively. Reprinted from Roy *et al.* [18] © 2021 IEEE.

for the non-field-plated SBD, the other two devices reach punch-through (PT) conditions at breakdown, as evidenced by the vertical electric field distribution in Fig. 3.8(c). The surface electric field E_{surf} for the non-punch-through (NPT) and punch-through (PT) conditions can be calculated as follows:

$$E_{surf}^{npt} = \sqrt{\frac{2qN_D V_{br}}{\epsilon}} \quad (3.9)$$

$$E_{surf}^{pt} = \frac{V_{br}}{t_{drift}} + \frac{qN_D t_{drift}}{2\epsilon} \quad (3.10)$$

where q is the electron charge, N_D is the donor concentration, ϵ is the dielectric permittivity, and t_{drift} is the drift layer thickness. Using these expressions, the surface electric fields are calculated as 2.2 MV/cm for the non-FP SBD, 4.2 MV/cm for the BTO FP SBD, and 5.42 MV/cm for the $(\text{BTO}/\text{STO})_{15}$ FP SBD. These calculated values closely match the simulation values shown in Fig. 3.8 (b).

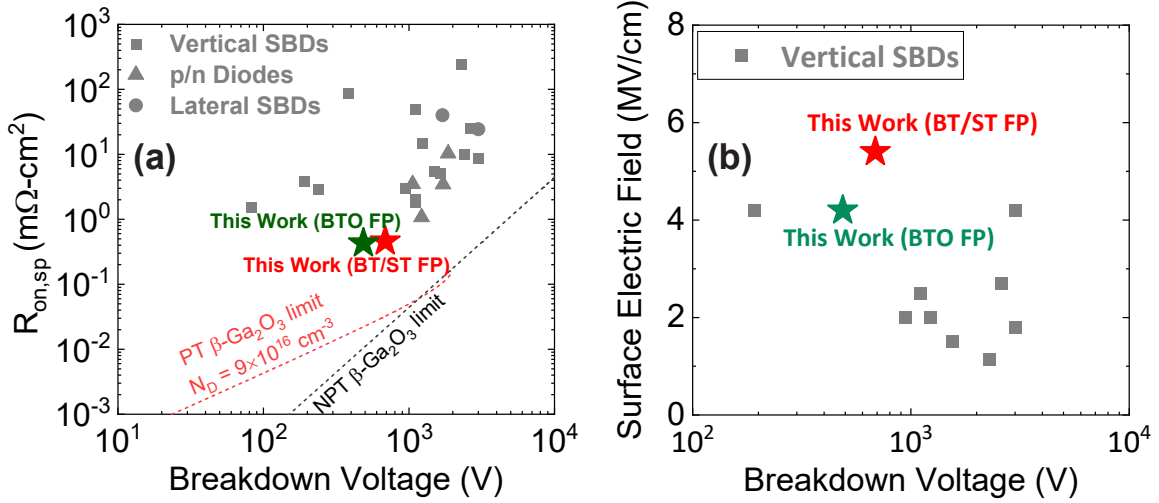


Figure 3.9: Benchmark plot for (a) R_{on-sp} vs V_{br} and (b) Surface electric field vs V_{br} comparing our device with other reported vertical and lateral diodes.

The SBD with the $(\text{BTO}/\text{STO})_{15}$ FP exhibits the highest surface electric field at catastrophic breakdown, reaching 5.45 MV/cm—one of the highest reported values for any Schottky barrier diode. Additionally, the peak electric field at the anode edges is estimated to be between 8–9 MV/cm, consistent with the observed breakdown locations in the microscope images (Fig. 3.7 (d)), which highlight weak points across the different device types. If perfect etching control is achieved, simulations of an identical structure with no 50 nm over-etching predict a peak electric field of 6.1 MV/cm at the anode edge for the $(\text{BTO}/\text{STO})_{15}$ FP under an anode bias of -687 V. This represents a 32% reduction compared to the structure with over-etched Ga_2O_3 , illustrating the impact of precise etching control on field distribution.

The edge termination efficiency, calculated as $\left[\frac{\text{Real } V_{BR}}{\text{Ideal } V_{BR}} \right] \times 100\%$, increases from 43.2% for the BTO FP to 61% for the $(\text{BTO}/\text{STO})_{15}$ FP. Here, the ideal breakdown voltage $V_{BR, Ideal}$ is determined by the equation (3.4), where E_C is taken to be the predicted critical electric field for $\beta\text{-Ga}_2\text{O}_3$, estimated at 8 MV/cm. This increase in edge termination efficiency with the $(\text{BTO}/\text{STO})_{15}$ FP highlights the effectiveness of the high- κ dielectric stack in mitigating field crowding and enhancing the breakdown voltage closer to the theoretical ideal.

The $(\text{BTO}/\text{STO})_{15}$ field-plated Schottky barrier diode (SBD) demonstrates an extremely low specific on-resistance (R_{on-sp}) of $0.32 \text{ m}\Omega\text{-cm}^2$ ($0.35 \text{ m}\Omega\text{-cm}^2$ from the linear fit) alongside a

breakdown voltage of 687 V, resulting in a record high figure of merit (FOM) of 1.47 GW/cm^2 (1.34 GW/cm^2 based on the linear fit of $R_{\text{on-sp}} = 0.35 \text{ m}\Omega\text{-cm}^2$). Fig. 3.9 (a) presents benchmark plots comparing the $R_{\text{on-sp}}$ and breakdown voltage of the $(\text{BTO}/\text{STO})_{15}$ FP SBD with existing literature, clearly indicating superior performance metrics for our device relative to others reported. The achieved surface breakdown electric field of 5.45 MV/cm ranks among the highest recorded for $\beta\text{-Ga}_2\text{O}_3$ based SBDs, as illustrated in Fig. 3.9 (b). It is important to note that the extraction of E_{surf} is dependent on the precise doping profile; for a uniform doping range of $6 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{17} \text{ cm}^{-3}$, the calculated E_{surf} falls between 4.96 and 5.57 MV/cm , with simulated values ranging from 4.97 to 5.6 MV/cm .

The demonstrated device structure can be engineered for high-voltage applications by carefully selecting the drift layer thickness and doping concentration. If the surface breakdown electric field of 5.45 MV/cm is maintained as observed in the high- k FP SBD, a drift layer thickness of $36 \mu\text{m}$ combined with a doping concentration of $8.2 \times 10^{15} \text{ cm}^{-3}$ could extend the breakdown voltage to 10 kV . In this voltage range, $\beta\text{-Ga}_2\text{O}_3$ devices exhibit significant advantages over SiC-based devices, which require drift layer thicknesses exceeding $100 \mu\text{m}$ to achieve 10 kV breakdown voltages [22], [23], thereby resulting in increased on-resistance for SiC devices.

3.4.5 $\beta\text{-Ga}_2\text{O}_3$ high- κ Field-plated SBD with Thick Drift Layer

The previous device with high- k field plates utilized a thin drift layer. While this device achieved a high parallel surface field, its absolute breakdown voltage was relatively low. To enhance the absolute breakdown voltage, another series of SBDs, as illustrated in Fig. 3.10(a), with high- k field plates using barium titanate (BTO) as the dielectric material, was fabricated on an $11 \mu\text{m}$ thick drift layer grown by halide vapor phase epitaxy (HVPE) on (001) conductive substrates from Novel Crystal Technologies, Japan (NCT Japan). Additionally, a device area-dependent analysis of $R_{\text{on-sp}}$ was conducted, along with switching calculations based on device characteristics and dimensions. The device fabrication steps followed the same process as those

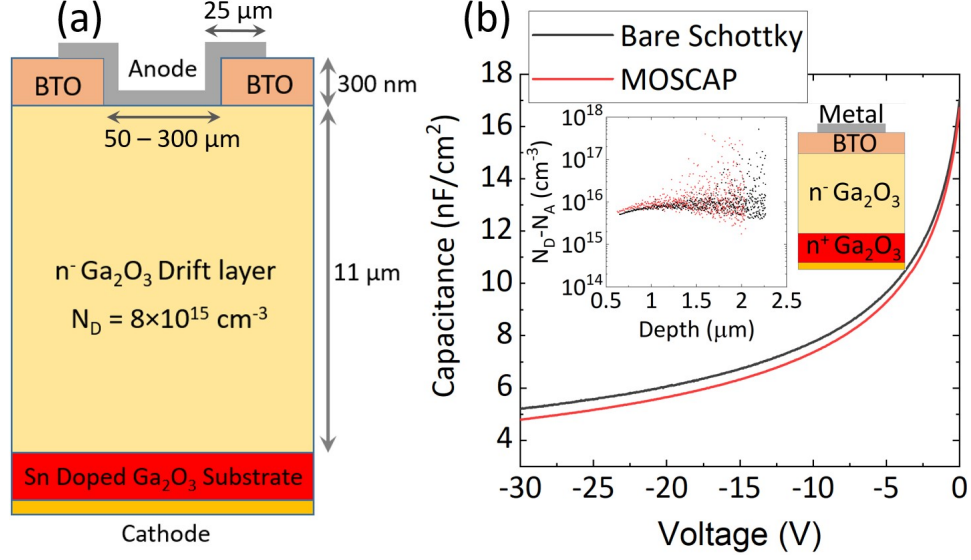


Figure 3.10: (a) Schematic diagram of the β -Ga₂O₃ high- k field-plated SBD. (b) Capacitance-voltage characteristics of the regular SBDs and MOSCAPs. The inset of Fig. 3.10(b) shows the apparent charge profile in the drift region for both the MOSCAP and the SBD. Reprinted from Roy *et al.* [24], with the permission from AIP Publishing.

used for the previous devices with thin drift layers.

Using capacitance-voltage (CV) measurements on the regular SBDs, as shown in Fig. 3.10 (b), a net doping concentration ($N_D - N_A$) of approximately $8 \times 10^{15} \text{ cm}^{-3}$ was determined. The dielectric constant of the sputtered BaTiO₃ layer was then estimated by comparing the capacitance values at zero bias, as indicated in Fig. 3.10 (b) [4], [25]. This analysis revealed a dielectric constant of 248. Since the band offset between BaTiO₃ and β -Ga₂O₃ is very small [20], we refrained from estimating the dielectric constant using accumulation capacitance. In fact, the MOSCAPs begin conducting current before achieving accumulation, as illustrated in Fig. 3.11 (d), which is similar to observations with a thin drift layer. In this instance, however, the dielectric constant was derived from reverse bias capacitance on the actual device, complemented by zero-bias depletion depth fitting based on the doping vs. depth profile shown in the inset of Fig. 3.10 (b). It is assumed that there is no potential drop within the dielectric and that the dielectric induces no additional depletion. These assumptions are reasonable given the high dielectric constant of BaTiO₃.

The current-voltage (IV) characteristics for the field-plated SBDs with varying diameters,

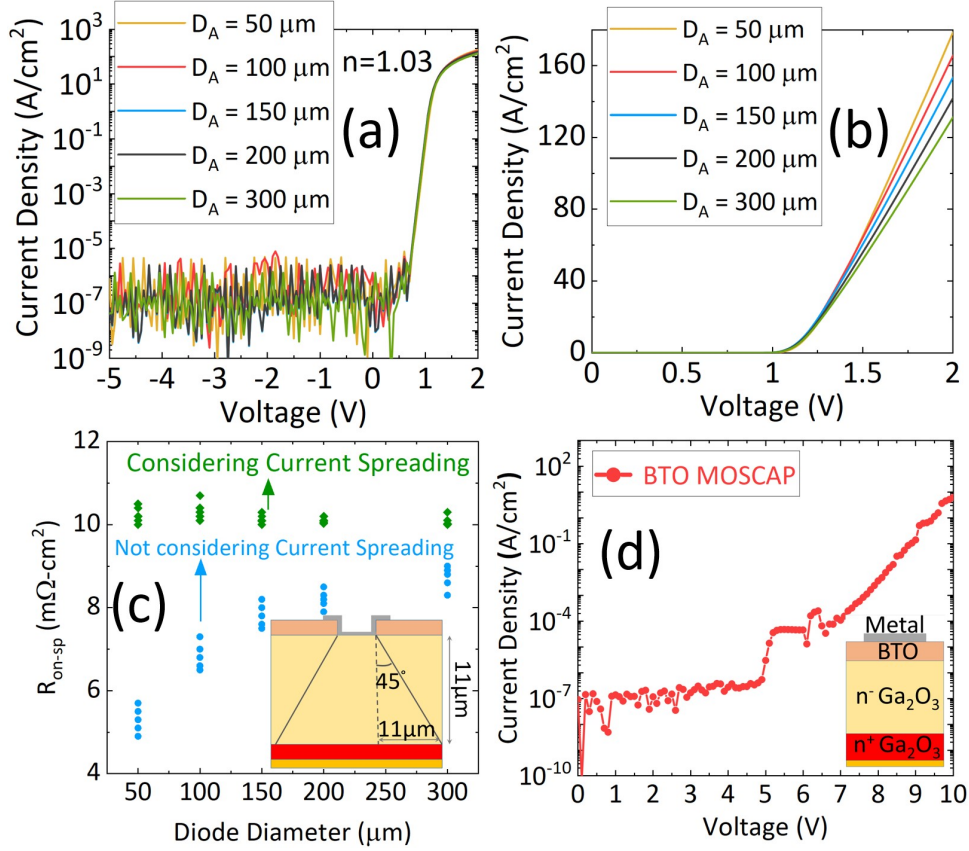


Figure 3.11: Forward current-voltage characteristics for the field-plated SBDs for different diode diameters in (a) linear and (b) log scale. (c) R_{on-sp} vs diode diameter for the field-plated SBD with and without current spreading (d) Current-voltage characteristics for the BTO MOSCAP showing negligible current density in diode operating voltage (0-2V). Reprinted from Roy *et al.* [24], with the permission from AIP Publishing.

presented in both logarithmic and linear scales, are shown in Fig. 3.11 (a) and (b). Using the thermionic emission model, a Schottky barrier height of 1.3 eV and an ideality factor (n) of 1.03 were extracted, indicating minimal damage to the Schottky interface from dry etching. The specific on-resistance (R_{on-sp}) without accounting for current spreading was determined by normalizing the forward current (I_{on}) with the anode diameter (D_A) as $\left(J_{on} = \frac{4I_{on}}{\pi D_A^2}\right)$, where J_{on} represents the current density. Subsequently, the differential specific on-resistance was calculated as $R_{on-sp} = \left(\frac{dJ_{on}}{dV}\right)^{-1}$, where V denotes the applied voltage, resulting in a range of 6.9-8.7 mΩ-cm² for the field-plated SBDs. An increase in R_{on-sp} with larger anode diameter (D_A) suggests significant current spreading in smaller diameter diodes.

Fig. 3.11 (c) illustrates the dependence of R_{on-sp} on diode diameter, with and without

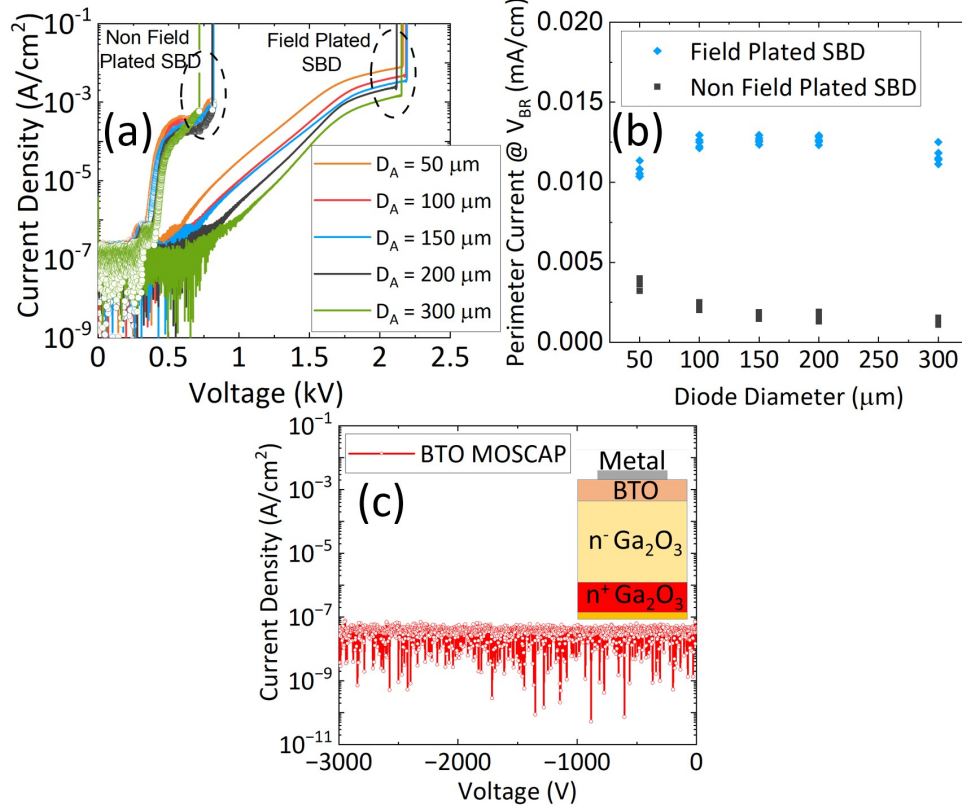


Figure 3.12: (a) Reverse IV characteristics for the field-plated and non-field-plated SBDs for different diode diameters, (b) Reverse leakage current density through diode periphery at breakdown voltage vs diode diameter, (c) Current-voltage characteristics for the BTO MOSCAP showing negligible current density in reverse bias up to 3kV. Reprinted from Roy *et al.* [24], with the permission from AIP Publishing.

current spreading (a 45° spreading angle [26] was assumed, presuming isotropic mobility within the material as depicted in the inset of Fig. 3.11 (c)). The upper bound of the specific on-resistance, taking current spreading into account, was calculated by normalizing the absolute current with the total spreading area (A_{sp}) [27], where $A_{sp} = (\pi D_{A-sp}^2) / 4$ and D_{A-sp} represents the total spreading diameter. Assuming a 45° current spreading angle, $D_{A-sp} = D_A + (2L_{Drift})$, with L_{Drift} denoting the drift layer thickness. When accounting for current spreading, R_{on-sp} becomes independent of the anode diameter. Additionally, the current through the BaTiO_3 layer is negligible at the operating voltage range (0-2V), as demonstrated in Fig. 3.11 (d), where measurements were taken on MOS capacitors.

The reverse IV characteristics for both the field-plated and non-field-plated SBDs are shown in Fig. 3.12 (a). The breakdown voltage for the non-field-plated diodes was extracted to be

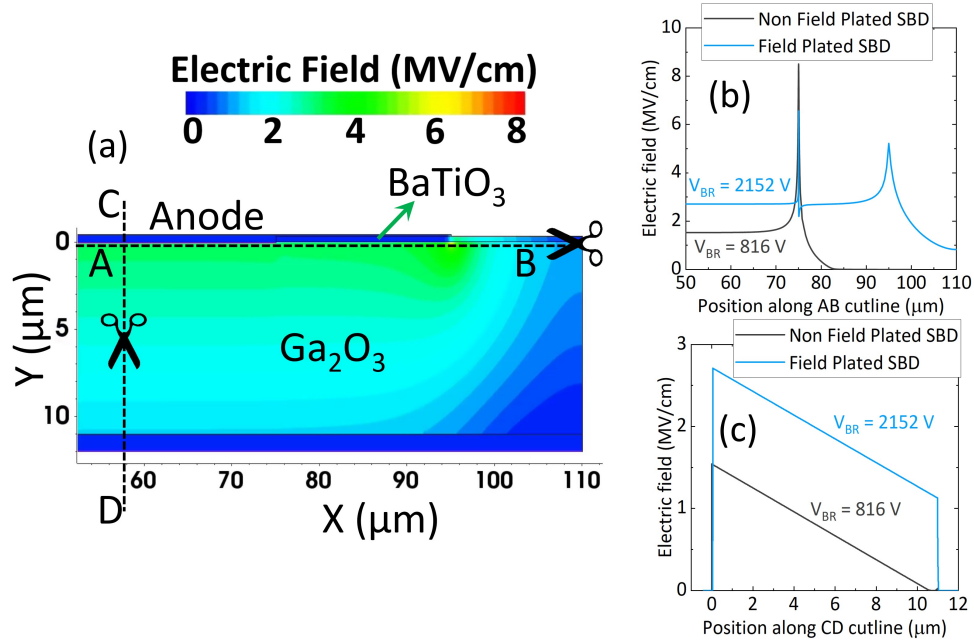


Figure 3.13: Electric field contour plot of the high- κ FP SBD. Simulated electric field profile for the field-plated and non-field-plated SBDs for cutlines along (b) AB and (c) CD. Reprinted from Roy *et al.* [24], with the permission from AIP Publishing.

approximately 771-816V, while the field-plated SBDs exhibit significantly higher breakdown voltages of around 2134-2186V, with minimal variation across diode diameters. In both cases, breakdown was catastrophic. The leakage current density at breakdown decreased with increasing diode diameter, indicating that leakage current primarily flows along the device periphery. By normalizing the currents to the device perimeter (πD_A) instead of the total area, it becomes evident that the leakage current is relatively uniform across diode diameters, as shown in Fig. 3.12 (b). This observation confirms that a significant portion of the leakage current originates from the device edges rather than the entire device area. The high periphery current at breakdown is attributed to the fact that the electric fields near the edges reach very high values (8 MV/cm) at breakdown for $\beta\text{-Ga}_2\text{O}_3$, in contrast to GaN ($\sim 3 \text{ MV/cm}$) or SiC ($\sim 2.5 \text{ MV/cm}$). Negligible current was observed through the high- κ dielectric layer up to 2 kV, as shown in Fig. 3.12 (c).

Electric field simulations for both non-field-plated and field-plated SBD structures were performed using Sentaurus TCAD software [21], with results plotted in Fig. 3.13 (a) and (b).

Both diodes reach a punch-through field profile under breakdown conditions, with the punch-through voltage estimated at approximately 729V. At breakdown voltage, the surface electric field reaches 1.5 MV/cm for the non-field-plated SBD and 2.6 MV/cm for the field-plated SBD. Peak electric fields of 8-9 MV/cm were estimated at the anode edges, suggesting that this is where breakdown occurs. The reduction in parallel plane breakdown field observed here, compared to the SBD with thin drift layer, may be due to differences in the epitaxial drift layer quality and thickness.

We have also analyzed the power losses in these field-plated and non-field-plated SBDs. The total power loss in a diode is a combination of static and switching power losses, which can be estimated using Eq. (6.6) [28]:

$$P_{Loss} = D \times P_{On} + (1 - D) \times P_{Off} + E_{sw} \times f_{sw} \quad (3.11)$$

where P_{Loss} , P_{On} , and P_{Off} represent the total, on-state, and off-state power losses, respectively, and D is the duty cycle. Here, E_{sw} and f_{sw} denote the switching energy loss and switching frequency, respectively.

First, the static power losses were estimated using $P_{On} = V_{On}J_{On}$ and $P_{Off} = V_{BR}J_{BR}$. The on-state voltage V_{On} is defined at $J_{On} = 100 \text{ A/cm}^2$, which is approximately 1.7V for the non-field-plated and 1.73V for the field-plated SBDs. The breakdown voltage V_{BR} is considered to be $\sim 816\text{V}$ for both types of SBDs for a fair comparison, with J_{BR} values of $\sim 8.9 \text{ mA/cm}^2$ for the non-field-plated SBD and $\sim 0.51 \mu\text{A/cm}^2$ for the field-plated SBD.

The on-state power loss for the field-plated and non-field-plated SBDs is approximately equal, as shown in Fig. 3.14(a) and (b), respectively. However, the off-state power loss is significantly higher for the non-field-plated SBDs, primarily due to the increased leakage current associated with these devices. Despite this, the total power loss remains similar for both the non-field-plated and field-plated SBDs, as it is predominantly influenced by the on-state power loss. Consequently, the total static power loss for both types of SBDs is nearly identical.

One major concern regarding the addition of high- k material is the potential increase in

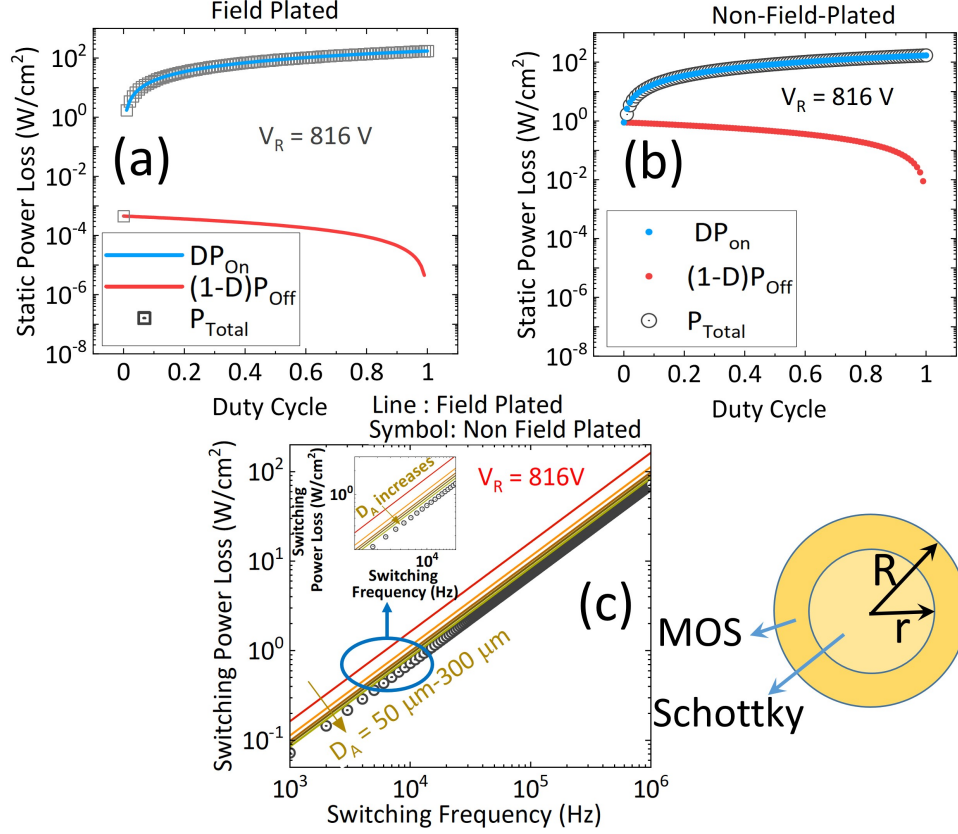


Figure 3.14: Static power loss for the (a) field-plated and (b) non-field-plated SBD as a function of duty cycle showing different components of the total loss (c) Estimated switching power loss for the field-plated and non-field-plated SBD as a function of switching frequency. Inset of (c) shows the expanded version of the marked region. V_R is the applied reverse bias. Reprinted from Roy *et al.* [24], with the permission from AIP Publishing.

switching power loss due to the elevated capacitance. To address this, we estimated the switching power losses analytically to compare the field-plated and non-field-plated SBDs evaluated by considering the total amount of charge that needs to be removed or added during the switching process, with only capacitive charge storage taken into account for the SBDs. It is important to note that the switching power loss calculations presented here are preliminary and entirely analytical; a more detailed analysis of the switching losses will be discussed in the next chapter.

Since both the non-field-plated and field-plated SBDs operate under punch-through conditions at breakdown (with $V_P = -729$ V, where V_P is the punch-through voltage), the energy loss for the non-field-plated SBD during switching (E_{sw-nFP}) can be estimated using (3.12),

$$E_{sw-nFP} = \frac{1}{2} C (V_{BR}^2 - V_P^2) = \frac{\epsilon}{2L_{Drift}} (V_{BR}^2 - V_P^2) \quad (3.12)$$

where C is the capacitance per unit area, ϵ is the dielectric constant of $\beta\text{-Ga}_2\text{O}_3$, and L_{Drift} is the thickness of the drift layer. In contrast, the field-plated SBD consists of both a Schottky region and a MOS region, as depicted in the inset of Fig. 3.14(b). Therefore, the total capacitance can be described as the combination of the Schottky depletion capacitance and the MOS depletion capacitance. The MOS depletion capacitance per unit area can be approximated as

$$\frac{\epsilon}{L_{Drift}} \times \frac{\pi(R^2 - r^2)}{\pi r^2}$$

where R is the outer circle radius and r is the inner circle radius. It is assumed that no voltage is dropped across the high- k dielectric, and lateral depletion is ignored. Thus, the total switching energy loss for the field-plated SBDs (E_{sw-FP}) can be estimated using (3.13).

$$E_{sw-FP} = \frac{1}{2} \left[\frac{\epsilon}{L_{Drift}} \left(\frac{R^2}{r^2} \right) \right] (V_{BR}^2 - V_P^2) \quad (3.13)$$

The estimated switching power losses are presented as a function of switching frequency in Fig. 3.14 (c). When the field-plated SBDs are switched at 2.1 kV, compared to 816 V for the non-field-plated SBDs, the switching power loss for the field-plated SBDs is significantly higher, approximately 26 times greater than that of the non-field-plated SBDs. However, when both types of devices are switched at the same voltage, the switching power losses are nearly identical. Additionally, it is evident that switching power loss decreases with an increase in diode diameter, as the contribution of the MOS region to the total stored charge diminishes. Thus, the inclusion of the high- κ layer does not significantly increase the power loss compared to the bare Schottky devices.

3.5 Summary

The design and efficacy of extreme permittivity dielectrics as field plate oxides is discussed in this chapter. The lateral spread of the depletion region for high- k dielectric field plates, driven by

fringing electric fields, results in reduced electric field crowding at the device edges compared to low- k dielectrics. The chapter also addresses key differences and design considerations for punch-through and non-punch-through architectures. Two demonstrations of high-permittivity dielectric field-plated Schottky barrier diodes (SBDs) are presented: one utilizing a thin drift layer and the other a thick drift layer.

The first device is fabricated on a vertical (001) oriented β -Ga₂O₃ drift layer, grown using halide vapor phase epitaxy (HVPE) on a (001) conducting substrate. This drift layer, with a thickness of 1.7 μm , features a high permittivity dielectric field plate oxide, resulting in an extremely low specific on-resistance (R_{on-sp}) of 0.32 $\text{m}\Omega\text{-cm}^2$ and a high breakdown voltage of 687 V, yielding a figure of merit (BFOM) value of 1.47 GW/cm^2 . By creating a superlattice of BaTiO₃ and SrTiO₃ followed by high-temperature annealing, a dielectric constant of 325 is achieved. The extracted surface breakdown electric field of 5.45 MV/cm is among the highest reported for β -Ga₂O₃ SBDs. The devices demonstrate marked differences in edge termination efficiencies, with higher dielectric constants leading to higher breakdown voltages. However, due to the thin drift layer, the absolute breakdown voltage remains below 1000 V.

The second device employs a thick, low-doped ($N_D = 8 \times 10^{15} \text{ cm}^{-3}$) 10 μm thick HVPE drift layer, commercially procured from a Sn-doped substrate oriented along (001). BaTiO₃ serves as the dielectric material for the field plate. This device achieves a breakdown voltage of 2.1 kV for the high- k field-plated β -Ga₂O₃ planar Schottky diodes with large diameters. The deposition of the high- k dielectric and subsequent dry etching have negligible effects on the forward characteristics of the diode. The breakdown voltage for the field-plated SBDs increases by approximately 2.7 times compared to the non-field-plated SBDs, and this voltage remains uniform across various Schottky diameters. Static and switching power losses for the SBDs are analyzed, revealing that static power loss is nearly identical for both non-field-plated and field-plated devices. The switching power loss is comparable for both types of SBDs when operated at the same reverse blocking voltage, with total switching power loss decreasing as diode diameter increases. Thus, the addition of the high- k dielectric has a negligible effect on

switching losses. Consequently, high- k field-plated devices can operate effectively at both high reverse voltages (2.1 kV) with low switching frequencies (10 kHz) and low reverse voltages (800 V) with high switching frequencies (greater than 100 kHz). This high- k dielectric usage can effectively leverage the high breakdown fields in ultra-wide bandgap materials through improved electric field management, enabling the true potential of these materials to be realized for next-generation power electronics.

These demonstrations indicate that the use of high- k dielectric field-plated structures enhances edge field termination efficiency and facilitates the investigation of intrinsic critical field limits in ultra-wide bandgap semiconductors. While these field plate techniques effectively reduce edge electric field crowding, thereby preventing premature breakdown, they do not significantly alleviate the parallel plane electric field at the bulk of the metal/semiconductor interface. The high electric field at this interface, especially under high reverse bias, can lead to various detrimental effects on the operation of the Schottky barrier diodes (SBDs). In the next chapter, we will explore methods to mitigate these high electric fields even at very high reverse bias, aiming to improve the overall performance of these devices.

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Chapter 4

β -Ga₂O₃ Extreme Permittivity Dielectric

RESURF Trench Schottky Barrier Diodes

4.1 Introduction

To recap, vertical devices offer superior performance over lateral devices in high-voltage applications, thanks to their inherent ability to handle higher currents. For these applications, thick, high-quality, low-doped drift layers are essential. These layers must withstand substantial reverse blocking voltages while ensuring high carrier mobility to minimize on-state resistance. Notably, commercially available 10 μm thick (001)- β -Ga₂O₃ epitaxial layers, grown via halide vapor phase epitaxy (HVPE) [1], exhibit a doping concentration of less than 10^{16} cm^{-3} . This characteristic makes them a highly promising option for developing vertical devices capable of operating in the multi-kilovolt range.

However, as reverse voltage increases in power diodes, the electric field at the junction interface (whether the p/n junction in p/n diodes or the metal/semiconductor junction in Schottky diodes) also intensifies. Wide and ultra-wide bandgap semiconductor-based devices, typically designed to operate at high reverse voltages, are therefore exposed to extremely high electric fields. These intense fields can lead to unwanted reverse leakage currents, which must be

minimized to reduce off-state power loss.

In p/n diodes, such reverse leakage currents are generally negligible due to the larger junction barrier. However, in Schottky barrier diodes, thermionic field emission at high reverse bias can lead to significantly higher reverse leakage currents. This issue is exacerbated by a reduction in Schottky barrier height due to image force lowering. Therefore, device engineering efforts must focus on reducing the electric field at the metal/semiconductor interface to minimize reverse leakage currents. The next section will discuss the impact of Schottky barrier height on reverse leakage mechanisms and the limitations of planar β -Ga₂O₃-based Schottky barrier diodes.

4.2 Thermionic Emission and Tunneling in Schottky Barrier Diodes at High Reverse Bias

In this section, we briefly summarize the analysis of reverse leakage currents due to thermionic and field emission, as described by Li *et al.* [2]. In ideal Schottky barrier diodes, reverse leakage current (J_{rev}) is composed of contributions from both thermionic emission (TE), where current flows over the Schottky barrier, and barrier tunneling (BT), where current flows through the barrier, as illustrated in Fig. 4.1. Therefore, the reverse leakage current, J_{rev} , is the sum of the leakage current density due to thermionic emission (J_{FE}) and the leakage current density due to barrier tunneling (J_{BT}), as shown in Equation 4.1:

$$J_{\text{rev}} = J_{\text{FE}} + J_{\text{BT}} \quad (4.1)$$

To analyze these leakage currents, it is crucial to consider the shape of the Schottky barrier. This shape is influenced by image force lowering (IFL) of the barrier height and the doping concentration in the semiconductor. Illustrations of the Schottky barrier shape are provided in Fig. 4.1(a) and (b). The conduction band minimum ($\mathcal{E}_c$) can be expressed, taking into account both IFL and doping, as follows:

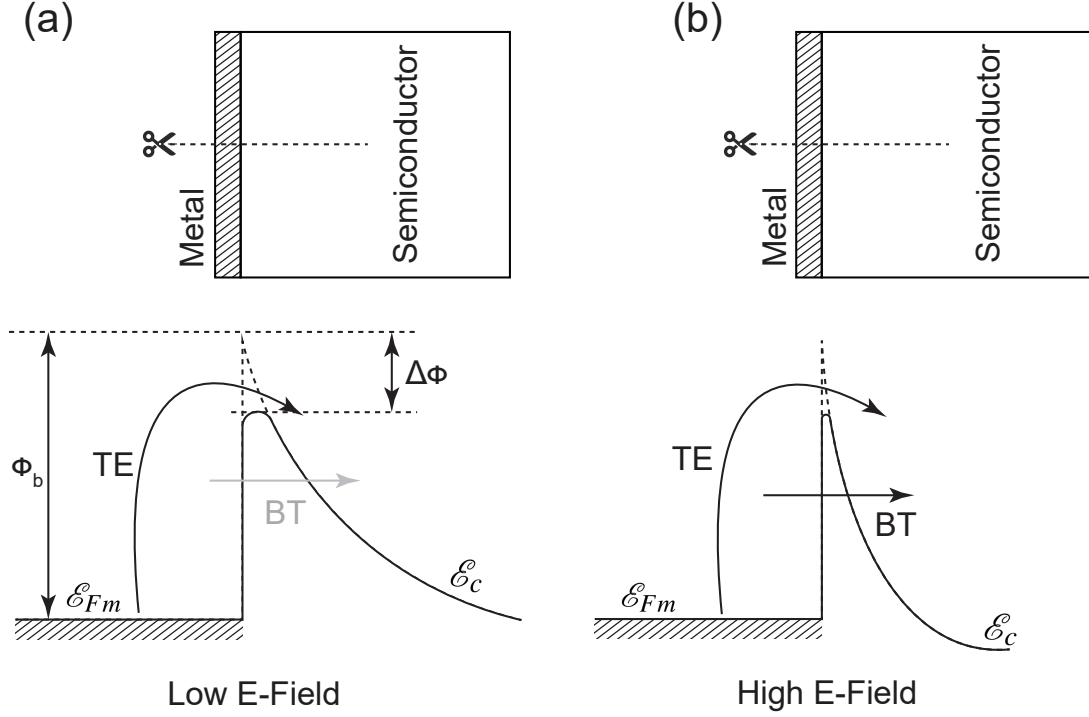


Figure 4.1: Schematic band diagram of a metal/semiconductor junction at (a) Low E-field and (b) high E-field with image force lowering and different leakage current components.

$$\mathcal{E}_c(x) = q\phi_b - qEx - \frac{q^2}{16\pi\epsilon_s x} + \frac{q^2 N_D x^2}{2\epsilon_s} \quad (4.2)$$

where ϕ_b is the Schottky barrier height, E is the surface electric field, N_D is the doping concentration in the semiconductor, ϵ_s is the permittivity of the semiconductor, and q is the electron charge. Now the J_{TE} considering IFL can be written as,

$$J_{TE} = A^* T^2 \exp\left(-\frac{q\phi_b - q\Delta\phi}{k_B T}\right) \quad (4.3)$$

where $A^* = \frac{4q\pi m^* k_B^2}{h^3}$ is the Richardson constant, m^* is the electron effective mass, k_B is the Boltzman constant, and h is the Planck's constant. $\Delta\phi = \frac{qE}{4\pi\epsilon_s}$ is the reduction in Schottky barrier height and T is the temperature.

Now the barrier tunneling current can be expressed as,

$$J_{BT} = \frac{A^* T^2}{k_B} \int_{-\infty}^{\mathcal{E}_c^{max}} \mathcal{T}(\mathcal{E}) \ln \left[1 + \exp\left(-\frac{\mathcal{E} - \mathcal{E}_{Fm}}{k_B T}\right) \right] \quad (4.4)$$

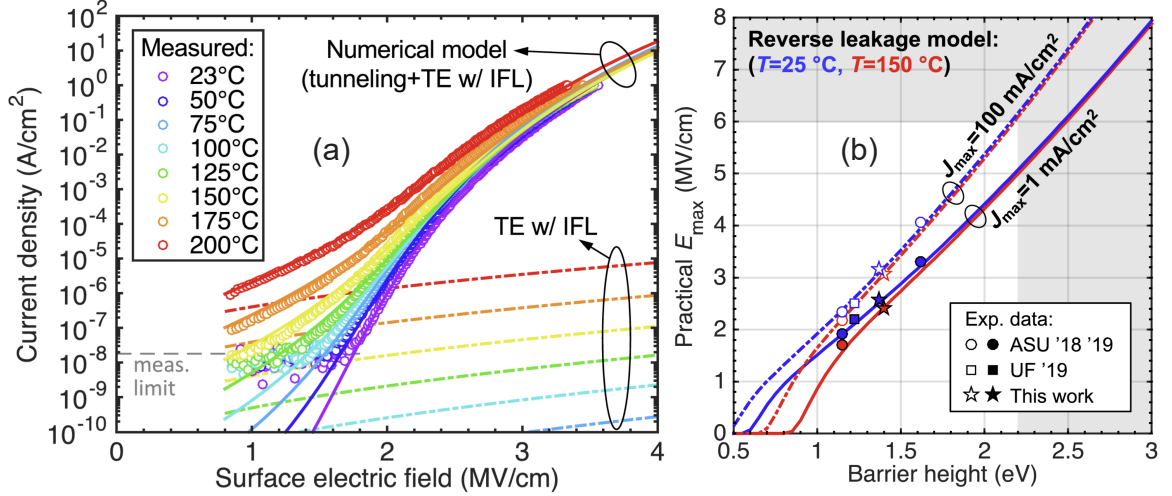


Figure 4.2: (a) Temperature-dependent reverse leakage current density as a function of the surface electric field for β -Ga₂O₃ SBDs. (b) Calculated practical maximum electric field (E_{max}) in β -Ga₂O₃ SBDs defined at fixed maximum reverse leakage current density levels ($J_{max}=1 \text{ mA/cm}^2$, 100 mA/cm^2), as a function of the barrier height. Reprinted from Li *et al.* [2], with the permission from AIP Publishing.

where $\mathcal{E}_C^{max}$ is the maxima of the conduction band at the metal/semiconductor interface, $\mathcal{E}_{Fm}$ is the Fermi level in the metal, and $\mathcal{T}(\mathcal{E})$ is the transmission probability which is written as,

$$\mathcal{T}(\mathcal{E}) = \begin{cases} \left[1 + \exp \left(-\frac{2i}{\hbar} \int_{x_1}^{x_2} p(x) dx \right) \right], & \text{if } \mathcal{E} \leq \mathcal{E}_C^{max} \\ 1, & \text{if } \mathcal{E} > \mathcal{E}_C^{max} \end{cases} \quad (4.5)$$

where $p(x) = -i\sqrt{2m^*(\mathcal{E}_C(x) - \mathcal{E})}$, x_1 and x_2 are the classical turning points and $\hbar$ is the reduced Planck's constant.

The current density versus surface electric field, as calculated by Li *et al.*, is shown in Fig. 4.2(a). It is evident that as the electric field increases, the leakage current rises sharply. Fig. 4.2(b) illustrates the practical maximum surface electric field as a function of Schottky barrier height, also based on Li *et al.*'s calculations. Here, the practical maximum electric field is defined as the field at which the reverse leakage current density reaches 1 mA/cm² (typical) or 100 mA/cm² (relaxed). From Fig. 4.2(b), it can be observed that for β -Ga₂O₃, the practical maximum applicable surface electric field is approximately 1.5–2 MV/cm for a Schottky barrier height of 1 eV. Beyond this field strength, the leakage current exceeds acceptable limits, despite the theoretical critical electric field being 8 MV/cm.

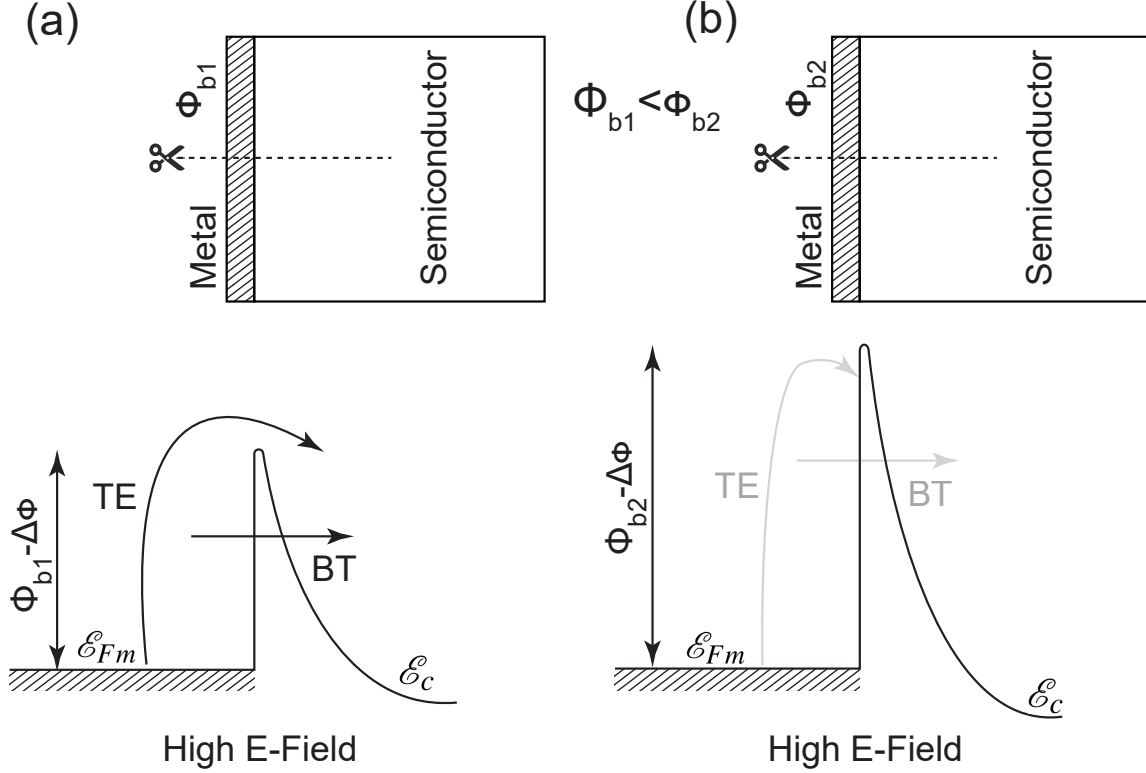


Figure 4.3: Schematic band diagram of a metal/semiconductor junction with (a) Low work-function and (b) high work-function anode contacts showing different leakage current components.

4.3 Methods of Reducing Leakage Current in Schottky Barrier Diodes

4.3.1 Increasing the Schottky Barrier in SBDs

Since both thermionic emission and barrier tunneling decrease as the energy barrier height increases, using a high work-function metal contact with an n-type semiconductor can effectively reduce reverse leakage current, as illustrated in Fig. 4.3. According to Fig. 4.2 (b) from Li *et al.*, for β -Ga₂O₃, a Schottky barrier height of 2.5 eV can support a practical maximum electric field ($E_{\max}$) of up to 6 MV/cm. This value far exceeds the theoretical critical electric field of other wide-bandgap semiconductors, such as SiC or GaN. However, conventional high work-function metals like Ni ($\phi_m = 5.1$ eV) and Pt ($\phi_m = 5.3$ eV) yield a Schottky barrier height of only 1.1–1.3 eV, which is insufficient to effectively block leakage currents.

One approach to enhance the barrier height involves using oxidized metal contacts. For instance, Hou *et al.* [3] demonstrated that oxidized metal contacts on β -Ga₂O₃, such as PdO_x, PtO_x, and AgO_x, can achieve Schottky barrier heights of 2–2.5 eV. Additionally, Saraswat *et al.* showed that PtO_x Schottky contacts with a barrier height of 2.2 eV can sustain electric fields up to 4.3 MV/cm while maintaining a leakage current below 100 A/cm².

However, a drawback of increasing the Schottky barrier height is a corresponding rise in the diode's turn-on voltage, which increases the forward voltage drop (V_F) and leads to higher on-state power losses. Since minimizing V_F is crucial for achieving high efficiency in power applications, alternative strategies to reduce leakage current while minimizing forward voltage drop must be explored. Consequently, further investigation into innovative materials and device architectures is essential for optimizing Schottky barrier diode performance across a range of high-efficiency applications.

4.3.2 High-Permittivity Interlayer Dielectric Schottky Barrier Diode

An alternative method to minimize barrier tunneling under reverse bias is to incorporate a thin high-permittivity (high- κ) interlayer dielectric between the Schottky metal and the semiconductor, with no conduction band offset between the dielectric and the semiconductor. This dielectric layer acts as a tunneling barrier during reverse bias, while allowing current to flow via thermionic emission during forward bias, thanks to the absence of a conduction band offset. The use of a high- κ dielectric is critical for maintaining a consistent tunneling width under high reverse bias. If any portion of the applied potential is dropped across the dielectric, a triangular potential barrier will form, reducing the tunneling distance in the dielectric, which could lead to ineffective suppression of tunneling currents, as depicted in Fig. 4.4(a).

High- κ dielectrics are advantageous because they sustain a lower electric field within the dielectric itself, ensuring most of the electric field is dropped across the semiconductor. This effect is described by:

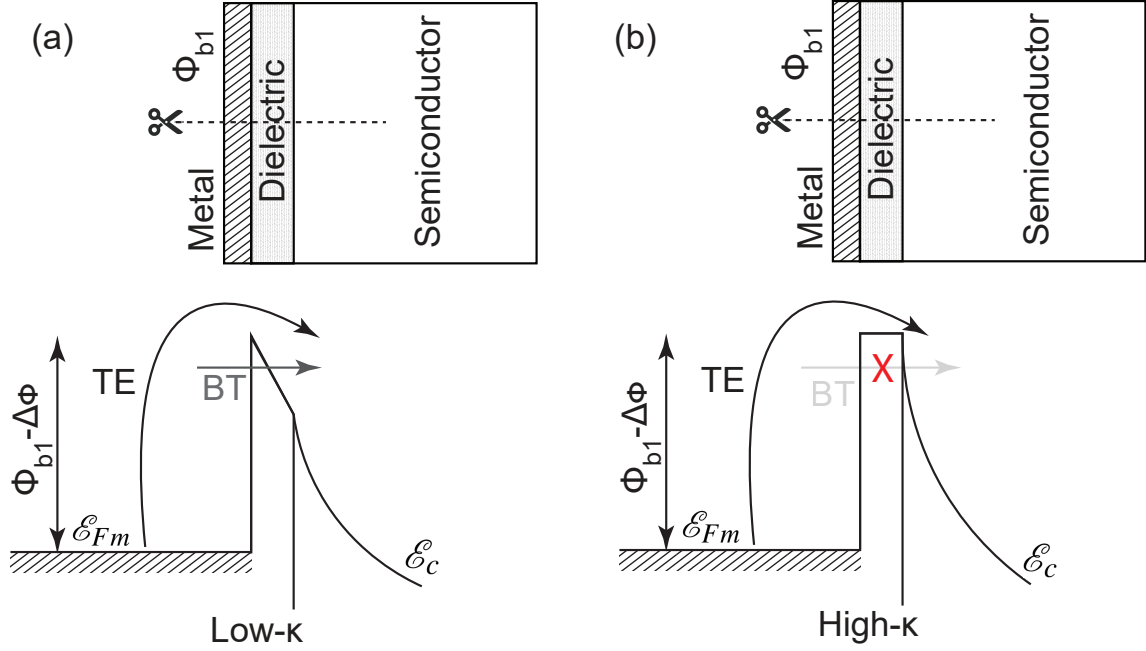


Figure 4.4: Schematic band diagram of a metal/semiconductor junction with (a) Low- κ and (b) high- κ dielectric interlayers showing different leakage current components.

$$E_d = \frac{\epsilon_s}{\epsilon_d} \times E_s \quad (4.6)$$

where E_d is the electric field within the dielectric, and E_s is the electric field at the dielectric/semiconductor interface on the semiconductor side. As a result, when a high- κ dielectric is employed, a rectangular potential barrier is maintained, effectively suppressing barrier tunneling, as illustrated in Fig. 4.4(b). The first demonstration of such a dielectric interlayer-based Schottky diode on β -Ga₂O₃ was performed by Xia *et al.* [4], who used a BaTiO₃ dielectric, achieving a breakdown field of 5.7 MV/cm. However, the relatively thick interlayer (30 nm of BaTiO₃) significantly increased the forward voltage drop, making the approach less efficient for practical applications. Later, Hendricks *et al.* [5] improved upon this design by incorporating a much thinner high- κ dielectric interlayer of only 4 nm of TiO₂, achieving a breakdown field of 2.8 MV/cm with a leakage current below 100 mA/cm². This thinner dielectric reduced the forward voltage drop, making it a more practical solution for high-efficiency devices.

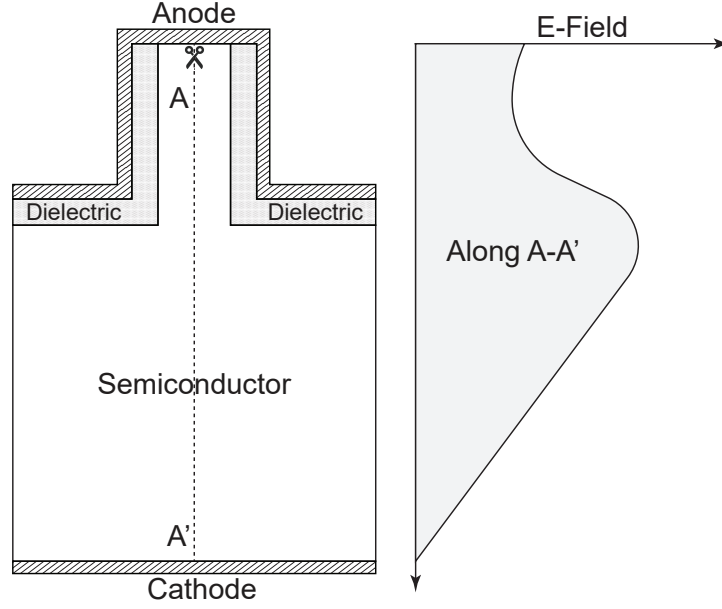


Figure 4.5: Schematic diagram of a trench Schottky barrier diode showing the electric field in the vertical direction. Due to RESURF effect, the electric field at the metal/semiconductor junction gets reduced.

4.3.3 Trench Schottky Barrier Diode

In all the previously discussed strategies, the electric field is controlled in only one dimension. When the electric field is applied solely in one direction at the metal/semiconductor junction, it must deplete sufficient charge in the semiconductor to sustain the potential. This results in the development of a very high electric field at the metal/semiconductor junction in the one-dimensional case.

In a trench Schottky Barrier Diode (SBD), fins are etched into the top region of the drift layer, with metal contacts surrounding the fins both laterally and vertically. The sidewalls of the semiconductor are isolated from the metal by a dielectric material, as illustrated in Fig. 4.5. The two-dimensional electric field in this design allows charge depletion horizontally from the sides of the drift region, significantly reducing the net electric field stress at the metal/semiconductor junction. Consequently, the leakage current is minimized due to the Reduced Surface Field (RESURF) effect at the junction.

The first demonstration of a trench SBD on β -Ga₂O₃ was reported by Sasaki *et al.* [6], utilizing HfO₂ as the dielectric material. These devices exhibited an improved breakdown field

compared to planar SBDs and demonstrated lower leakage currents at high fields. Li *et al.* [7] later developed a field-plated β -Ga₂O₃ trench SBD, achieving a breakdown voltage above 2.8 kV with extremely low reverse leakage currents. However, the use of low- κ dielectrics on the sidewalls led to potential drops within the dielectric, limiting the full impact of the RESURF effect. The following section explores how high-permittivity dielectrics can further enhance the RESURF effect.

4.4 High- κ Dielectric Trench Schottky Barrier Diode

As demonstrated in Eq. 4.6, a high-permittivity dielectric reduces the voltage drop across the dielectric, allowing most of the electric field to be applied within the semiconductor in a MOS structure. In the case of trench SBDs, using a high- κ dielectric similarly ensures that less potential is dropped within the dielectric, thereby increasing the lateral electric field in the semiconductor and enhancing the RESURF effect. Consequently, the electric field at the metal/semiconductor junction is significantly lowered, as illustrated in Fig. 4.6(b). A simplified analytical model outlining the influence of the dielectric constant on the RESURF effect in trench SBDs is presented below.

In the fin region, the two-dimensional Poisson equation can be approximated as:

$$\frac{\partial E_S(x)}{\partial x} + \frac{\partial E_S(y)}{\partial y} = \frac{qN_D}{\epsilon_S} \quad (4.7)$$

where $E_S(x)$ is the x-component of the electric field, $E_S(y)$ is the y-component, q is the electron charge, N_D is the doping concentration in the semiconductor, and ϵ_S is the dielectric constant of the semiconductor. In this approximation, the x and y components of the electric field are decoupled for simplicity, which is sufficient to demonstrate the effect of the dielectric constant on the RESURF mechanism. Using a Taylor expansion, the gradient of the electric field in the x-direction is expressed as:

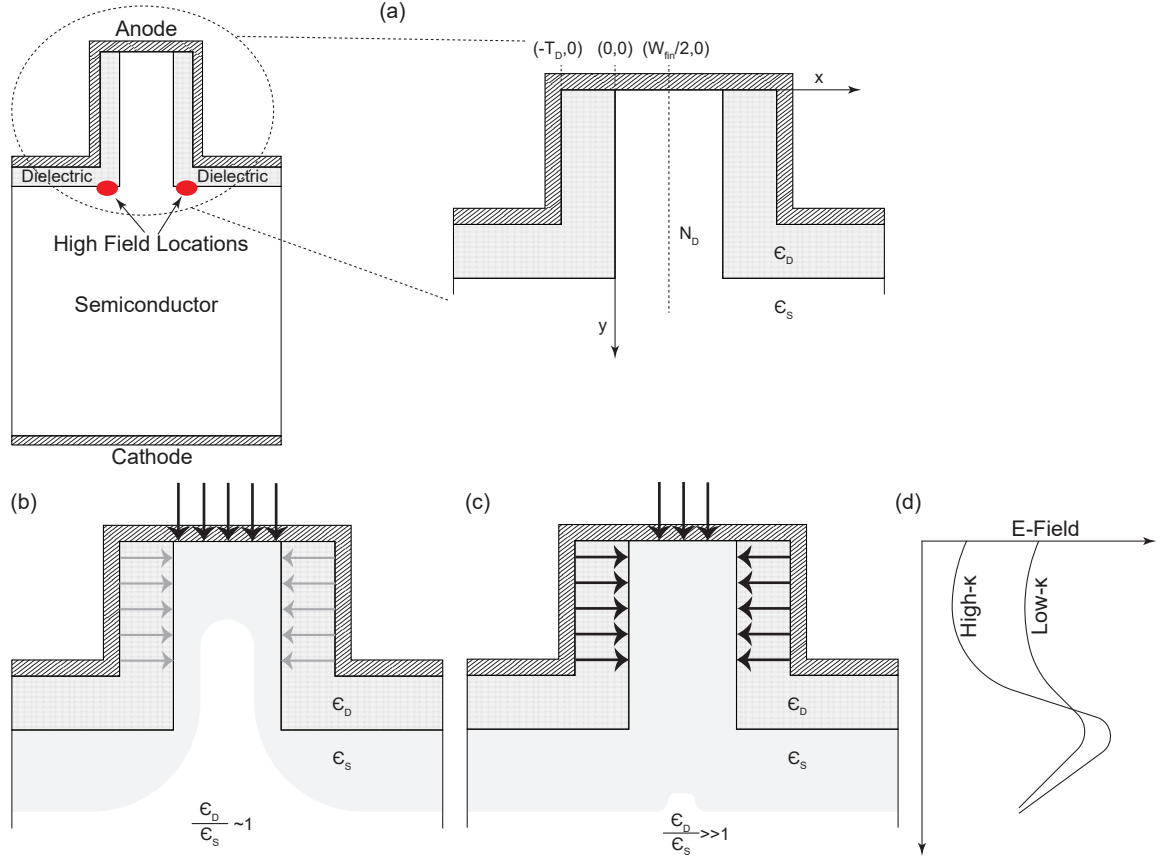


Figure 4.6: (a) Schematic diagram of trench SBD showing peak electric field location and RESURF effect under reverse bias for (b) low- κ dielectric and (c) high- κ dielectric. (d) Electric field profile for the trench SBD in vertical direction for low- κ and high- κ dielectric.

$$\frac{\partial E_S(x)}{\partial x} = \frac{E_S\left(x = \frac{W_{fin}}{2}\right) - E_S(x = 0^+)}{\frac{W_{fin}}{2}} \quad (4.8)$$

where $E_S\left(x = \frac{W_{fin}}{2}\right) = 0$ due to symmetry at the midpoint of the fin. From (4.6), the electric field at $x = 0^+$ can be written as:

$$E_S(x = 0^+) = \left(\frac{\epsilon_d}{\epsilon_S} \times E_D(x = 0^-) \right) \quad (4.9)$$

where $E_D(x = 0^-) = E_D(x)$. Substituting Eq. 4.9 into (4.8), the gradient of the electric field in the x-direction becomes:

$$\frac{\partial E_S(x)}{\partial x} = -\frac{2\epsilon_d E_D(x)}{W_{fin}} \quad (4.10)$$

Now, $E_D(x)$ can be written as:

$$E_D(x) = \frac{\psi_m - \psi_S(V_R)}{T_d} \quad (4.11)$$

where ψ_m is the potential at the metal, $\psi_S(V_R)$ is the surface potential at the semiconductor sidewall, and T_d is the dielectric thickness. Under reverse bias conditions, $\psi_m = 0$ and the surface potential $\psi_S(V_R)$ depends on the reverse bias voltage V_R . Therefore, the gradient of the electric field in the x-direction can be expressed as:

$$\frac{\partial E_S(x)}{\partial x} = \frac{2\psi_S(V_R)}{W_{fin}T_d} \left(\frac{\epsilon_d}{\epsilon_S} \right) \quad (4.12)$$

Now, using (4.7), the gradient of the electric field in the y-direction can be expressed as:

$$\frac{\partial E_S(y)}{\partial y} = \frac{qN_D}{\epsilon_S} - \frac{\partial E_S(x)}{\partial x} \quad (4.13)$$

Substituting (4.12) into (4.13), we get:

$$\frac{\partial E_S(y)}{\partial y} = \frac{qN_D}{\epsilon_S} - \frac{2\psi_S(V_R)}{W_{fin}T_d} \left(\frac{\epsilon_d}{\epsilon_S} \right) \quad (4.14)$$

From (4.14), it can be observed that the gradient of the electric field in the y-direction is reduced by a factor that depends on the ratio of the dielectric constant of the dielectric to the semiconductor permittivity, as well as the dielectric thickness and fin width. Compared to the Poisson equation in one dimension $\left(\frac{\partial E_S^{1D}(y)}{\partial y} = \frac{qN_D}{\epsilon_S} \right)$, it appears as though the doping concentration in the fin region is effectively reduced.

It is evident from (4.14) that as the dielectric constant of the dielectric increases, $\frac{\partial E_S(y)}{\partial y}$ decreases, enhancing the RESURF effect. Additionally, it can also be seen that as the fin width decreases, the RESURF effect becomes more pronounced.

Another significant advantage of employing high-permittivity dielectrics in trench structures is the ability to use a thicker dielectric layer while still maintaining the effectiveness of the RESURF effect due to the reduced potential drop across the dielectric. As shown in Fig. 4.6, the high-field regions are concentrated at the MOS interface at the bottom of the trench. The

use of a thicker high- κ dielectric helps increase the breakdown voltage significantly compared to trench SBDs utilizing low- κ dielectrics.

Dielectric leakage is another critical concern in trench SBDs employing low- κ dielectrics. Under high reverse bias, the electric field in the dielectric layer can become quite strong, leading to substantial leakage currents that may cause premature breakdown of the device. The reduced electric field within high- κ dielectrics under reverse bias mitigates this issue, allowing for improved device reliability.

These combined benefits—higher breakdown voltage and reduced dielectric leakage—make high- κ dielectrics a more attractive and practical option for trench SBDs, offering significant advantages over traditional low- κ dielectric approaches.

4.5 Power Losses in Power Diodes

A key consideration when using high-permittivity dielectrics in power applications is the associated increase in device capacitance, which can limit the switching frequency. High capacitance leads to greater energy storage and dissipation during switching events, directly impacting efficiency, especially at high frequencies. In this section, we provide an in-depth analysis of power losses in power diodes, examining both static and switching losses to assess the trade-offs introduced by high- κ materials in practical applications.

Static power losses primarily occur during the on-state of the diode, when conduction losses dominate. These losses are dependent on the forward voltage drop (V_F) and the current through the diode. However, switching losses, which occur during the transition between the on-state and off-state, are significantly influenced by the junction capacitance. As the capacitance increases, more energy is required to charge and discharge the junction during each switching cycle, leading to higher switching losses, especially at elevated frequencies.

In the context of high- κ dielectric-based diodes, if the device capacitances increase compared to the high- κ dielectric-based diodes that may also result in higher switching losses, limiting

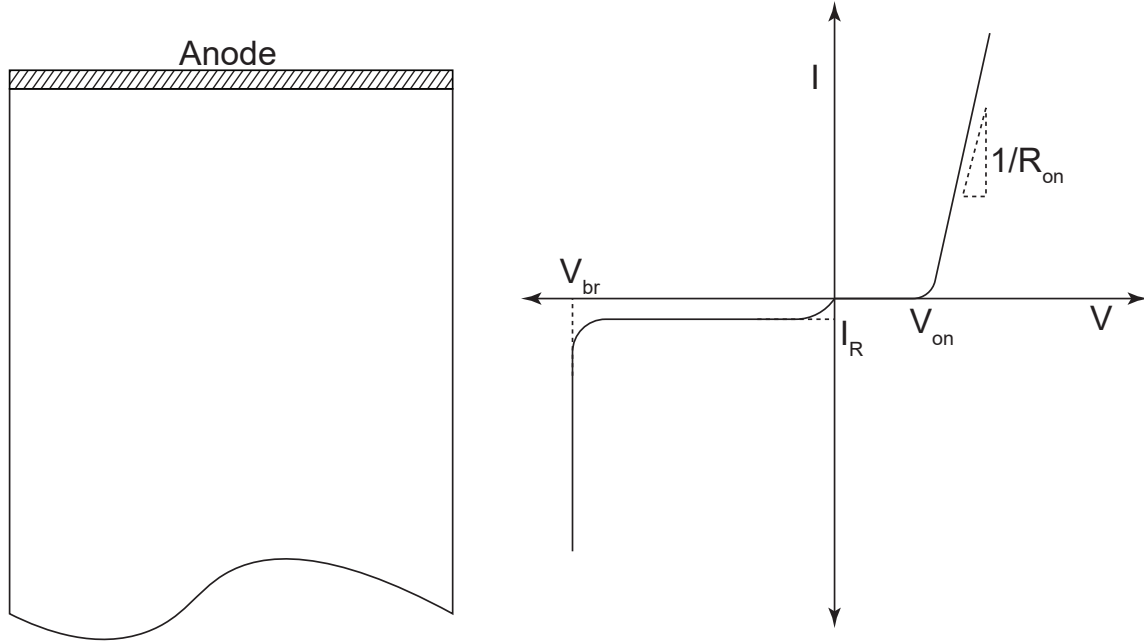


Figure 4.7: Schematic representation of current-voltage characteristics of Schottky barrier diodes under forward and reverse bias.

the device's operational frequency range. Thus, optimizing the balance between capacitance, breakdown voltage, and switching losses is crucial for ensuring high-efficiency operation in power applications. In the following subsections, we will quantify these losses and analyze the capacitances in the case of trench Schottky barrier diodes.

4.5.1 Static Power Loss

Static power loss in a power diode can be broken down into two main components: conduction loss and reverse leakage loss. Conduction loss arises from the finite forward voltage drop when the diode is in forward conduction mode. This loss depends on the diode's turn-on voltage and its on-state resistance, as illustrated in Fig. 4.7.

In contrast, reverse leakage loss results from the finite reverse leakage current that flows when the diode operates in reverse blocking mode. The overall static power loss of the diode is given by:

$$P_{loss}^{static} = I_F V_F \delta + I_R V_R (1 - \delta) \quad (4.15)$$

In this equation, $V_F = V_{on} + I_F R_{on}$ represents the forward voltage drop, where V_{on} is the turn-on voltage, I_F is the forward current, and R_{on} is the on-state resistance of the diode. Meanwhile, I_R denotes the reverse leakage current, V_R is the reverse blocking voltage, and δ represents the duty cycle. The first term on the right-hand side of (4.15) corresponds to the conduction loss, while the second term accounts for the reverse leakage loss.

It is clear from (4.15) that reducing conduction loss can be achieved by lowering V_{on} . However, a decrease in V_{on} typically results in an increase in I_R , which leads to higher reverse leakage loss. This trade-off can be effectively mitigated by using trench Schottky barrier diodes (SBDs), which help reduce the electric field at the dielectric/semiconductor interface.

4.5.2 Switching Power Loss

To analyze switching power loss in a power diode, a double-pulse test circuit is employed, where a MOSFET drives an inductive load, and the diode serves as a freewheeling diode, as depicted in Fig. 4.8. A gate driver circuit typically controls the MOSFET's gate, and for this analysis, the MOSFET is assumed to be ideal. The current direction is indicated by arrows in the figure.

In steady-state operation, when the MOSFET is off, the inductor current (I_L) flows through the diode, as shown in Fig. 4.8(a). This represents the diode's on-state, during which it dissipates the on-state power, as previously discussed and illustrated in Fig. 4.9(a).

When the MOSFET turns on, as illustrated in Fig. 4.8(b), part of the inductor current (I_L) starts flowing through the MOSFET, causing the forward current through the diode to decrease. Once the diode current reaches zero, the entire inductor current flows through the MOSFET. A reverse current then flows through the diode to charge its junction capacitance from t_3 to t_4 , as shown in Fig. 4.9(a), while the diode's reverse voltage rises to the supply voltage (V_{DD}). The switching power loss during this period can be expressed as:

$$P_{loss}^{sw} = \frac{t_4 - t_3}{2T} I_{sw} V_{DD} \quad (4.16)$$

The magnitude of reverse current through a Schottky diode depends on the diode's junction

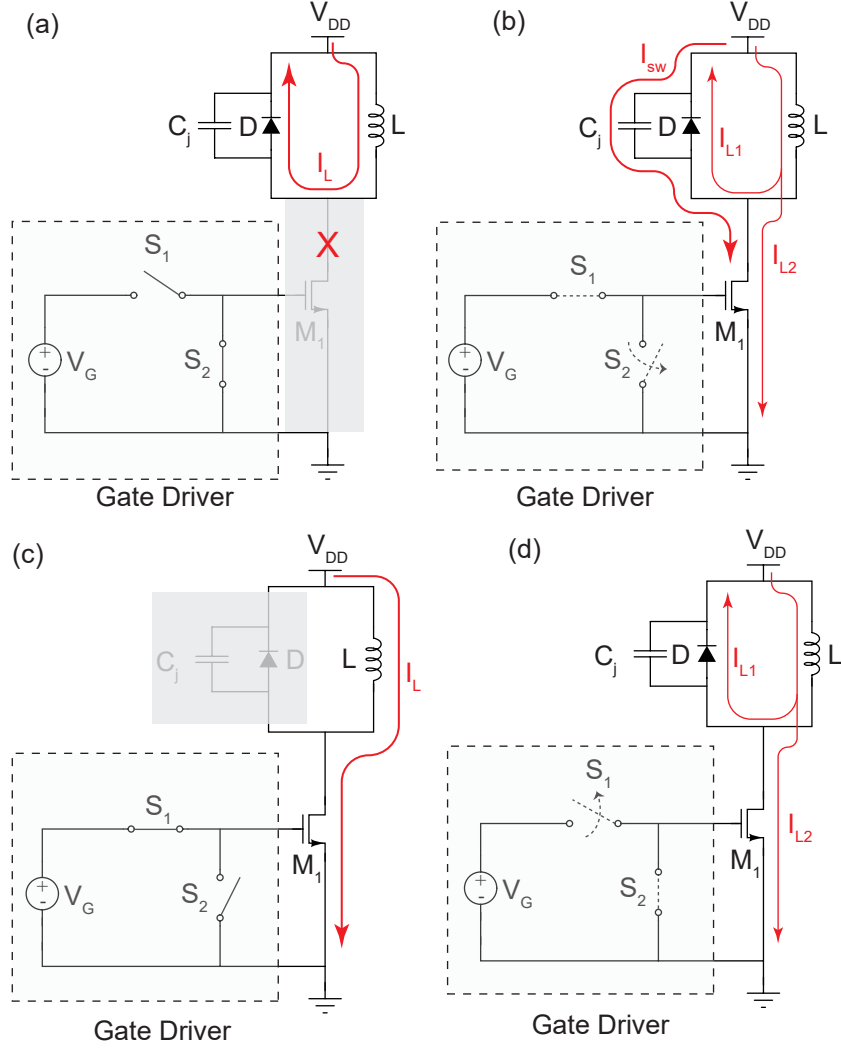


Figure 4.8: Circuit schematic of a double-pulse test circuit and current pathways during the diode's a) on-state, b) turn-off transient, c) off-state, and d) turn-on transient.

capacitance (C_j), while the switching time is governed by the $R_S C_j$ time constant, where R_S is the series resistance. This series resistance includes the undepleted drift layer resistance and other parasitic resistances present in the circuit. The switching loss can also be estimated from the energy stored in the junction capacitance and the switching frequency (f_{sw}) as:

$$P_{loss}^{sw} = \frac{1}{2} C_j V_{DD}^2 f_{sw} \quad (4.17)$$

During the turn-on transient, no power is lost in the diode, as the junction capacitance is discharged by the load current (I_L), as shown in Fig. 4.9(b). Therefore, the stored energy is

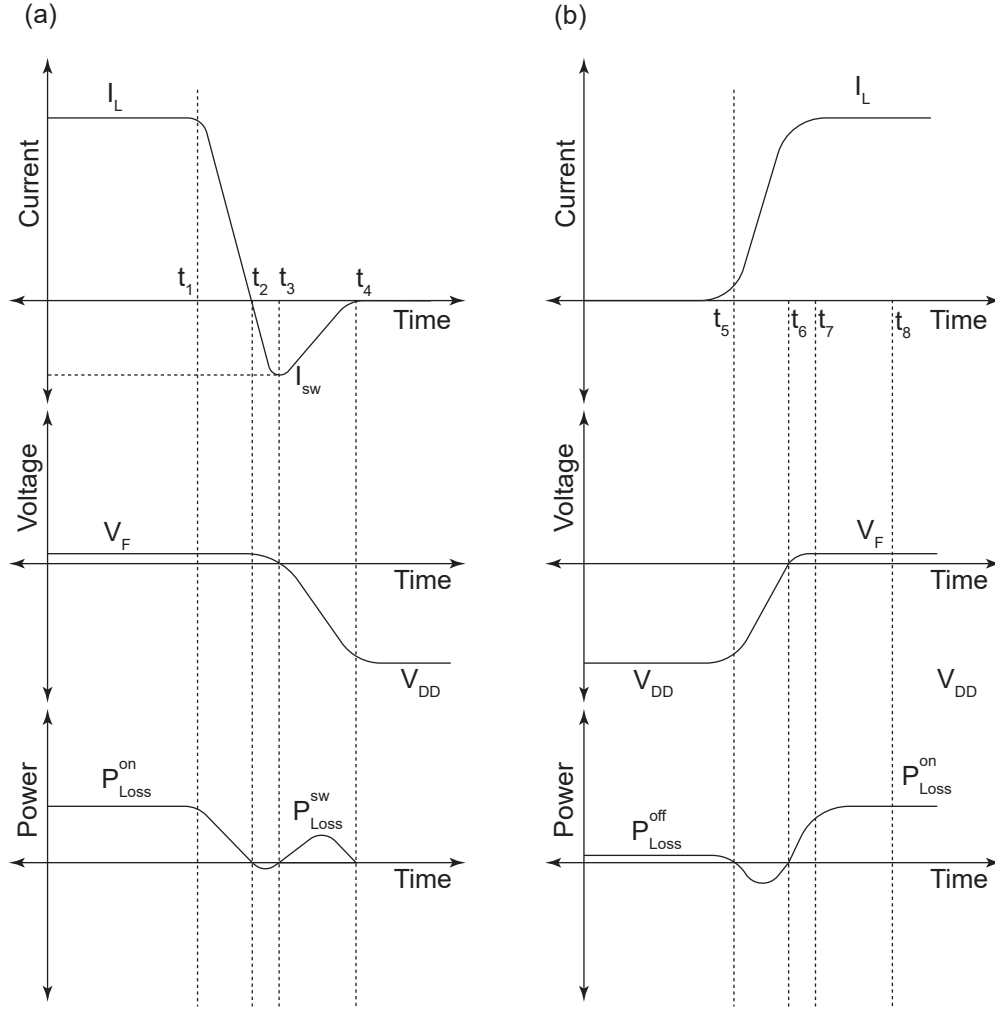


Figure 4.9: (a) Off-state and (b) on-state current, voltage, and power switching transient for a power diode

effectively delivered to the load. Consequently, the total power loss (including both static and switching losses) in a power diode can be written as:

$$P_{loss}^{total} = I_F V_F \delta + I_R V_R (1 - \delta) + \frac{1}{2} C_j V_{DD}^2 f_{sw} \quad (4.18)$$

Thus, the switching power loss in Schottky barrier diodes primarily depends on the diode's junction capacitance. Hence it is important to minimize these junction capacitances in the case of power diodes to minimize the switching losses. In the next section, a capacitance model for the trench SBD is provided.

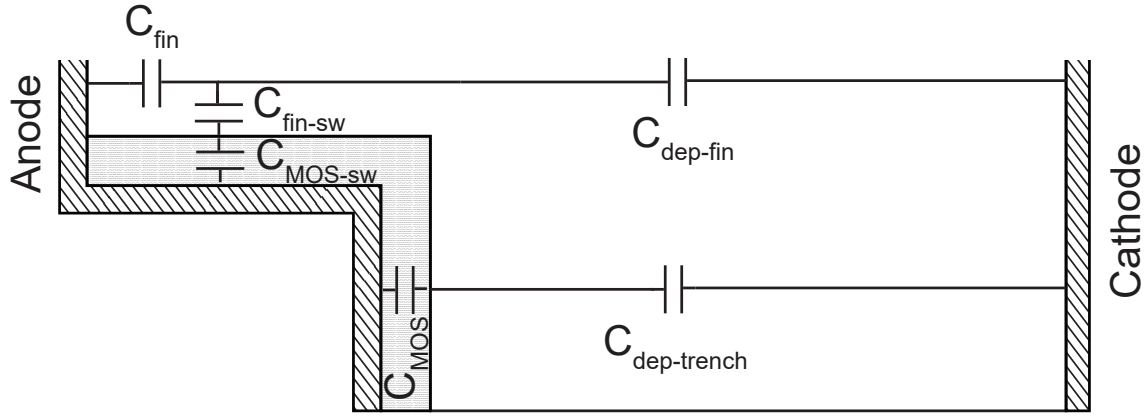


Figure 4.10: Parasitic capacitive components of a trench Schottky barrier diode.

4.6 Capacitance Model for Trench Schottky Barrier Diodes

In the case of trench Schottky barrier diodes, the junction capacitance is composed of MOS capacitance at the trench bottom and sidewall and depletion capacitance, as illustrated in Fig. 4.10.

In Fig. 4.10, $C_{dep-trench}$ and $C_{dep-fin}$ represent the drift layer depletion capacitance per unit width in the trench and fin regions of the trench SBD, respectively. C_{MOS} denotes the dielectric capacitance per unit width in the trench region, while C_{MOS-sw} corresponds to the dielectric capacitance per unit width along the fin sidewalls. Additionally, C_{fin-sw} refers to the depletion capacitance per unit width at the fin sidewalls, and C_{fin} represents the depletion capacitance per unit width in the fin region due to the metal/semiconductor contact in the trench SBD. Thus, the total capacitance of the trench SBD can be expressed as:

$$C_{Total} = (C_{MOS} + C_{dep-trench}) || [((C_{MOS-sw} + C_{fin-sw}) || C_{fin}) + C_{dep-fin}] \quad (4.19)$$

where

$$C_{MOS} = \frac{\epsilon_d W_{trench}}{T_d}$$

$$C_{MOS-sw} = \frac{\epsilon_d L_{fin}}{T_d}$$

$$C_{dep-trench} = \sqrt{\frac{\epsilon_S q N_D W_{trench}}{4(V_R - V_d)}}$$

$$C_{dep-fin} = \sqrt{\frac{\epsilon_S q N_D W_{fin}}{4(V_R - V_{fin})}}$$

$$C_{fin-sw} = \sqrt{\frac{\epsilon_S q N_D L_{fin}}{2(V_R - V_D)}}$$

$$C_{fin} = \sqrt{\frac{\epsilon_S q N_D W_{fin}}{4V_R}}$$

Here, W_{trench} , W_{fin} , and L_{fin} represent the width of the trench region, the width of the fin region, and the depth of the fins, respectively. V_d is the voltage drop across the dielectric, and V_{fin} is the voltage drop in the fin region. The depletion capacitances are calculated at low voltages, before punch-through occurs in both the drift and fin regions. In Eq. (4.19), $||$ denotes parallel capacitances.

After punch-through, the depletion capacitances can be expressed as

$$C_{dep-trench} = \frac{\epsilon_S W_{trench}}{2L_{drift}}$$

$$C_{dep-fin} = \frac{\epsilon_S W_{fin}}{2L_{drift}}$$

$$C_{fin-sw} = \frac{2\epsilon_S L_{fin}}{W_{fin}}$$

$$C_{fin} = \frac{\epsilon_S W_{fin}}{L_{fin}}$$

At high reverse bias, $C_{dep-trench}$ and $C_{dep-fin}$ will reach their lowest values. Consequently, from Eq. (4.19), it is clear that under high reverse bias, the depletion capacitances in the fin regions will dominate due to the series connection of the dielectric and depletion capacitances. As a result, using high- κ dielectrics will not significantly affect the total capacitance of the trench SBDs, and the overall capacitance will primarily be determined by the depletion capacitance of the drift region. Thus, the switching performance of trench SBDs will not degrade with the use of high- κ dielectrics.

The following section presents a demonstration of the vertical trench Schottky barrier

diode utilizing a high-permittivity dielectric, which is designed to enhance the RESURF effect. This exploration aims to illustrate the advantages of this configuration in achieving improved performance characteristics in power applications.

4.7 Vertical Trench Schottky Barrier Diode with High- κ Dielectric RESURF featuring Pt Contact

This section presents a demonstration of trench Schottky barrier diodes (SBDs) based on β -Ga₂O₃, featuring a high-permittivity dielectric RESURF with a platinum contact. For the RESURF dielectric, barium titanate (BaTiO₃, BTO) was utilized, exhibiting a dielectric constant of 248 [8]. In industrial applications, large-area power switching devices are crucial as they must handle substantial loads. These industrial power devices are designed to manage currents in the order of several amperes during the on-state while withstanding off-state voltages of several hundred volts. Such operations often occur at frequencies reaching tens to hundreds of kilohertz.

However, a significant challenge arises with increasing device area: the concomitant rise in reverse leakage currents, which leads to heightened off-state power loss. Despite intensive research efforts, all demonstrated large-area β -Ga₂O₃-based SBDs exhibit reverse leakage currents exceeding 1 mA/cm². While pn-heterojunction diodes utilizing nickel oxide (NiO) [9]–[11] have shown lower reverse leakage currents, they are burdened by excessively high turn-on voltages, resulting in increased on-state power loss. Thus, large-area devices with reduced turn-on voltage and lower off-state reverse leakage currents are critical for the successful commercialization of β -Ga₂O₃-based devices.

To address these challenges, the fabrication process involved creating both small-scale (200×200 μm^2) and larger-scale devices (1×1 mm^2 and 2×2 mm^2), which are capable of supporting ampere-level currents. The 1 mm^2 and 4 mm^2 devices demonstrated maximum forward currents of 3.5 A and 15 A, respectively, while also achieving substantial breakdown

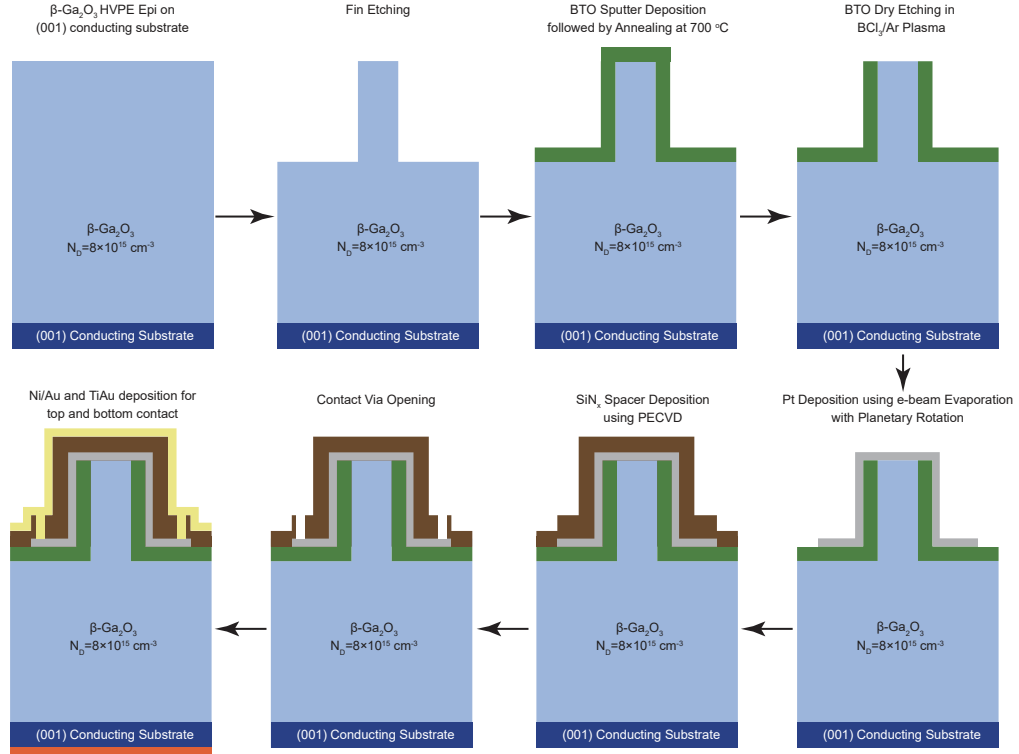


Figure 4.11: Fabrication steps of the trench Schottky barrier diode.

voltages of 1.8 kV and 1.4 kV. In contrast, the smaller devices exhibited even higher breakdown voltages, surpassing 3 kV. To comprehensively assess the performance characteristics of these devices, capacitance-voltage measurements were conducted on the larger-area devices. This analysis enabled the estimation of stored charge and switching energies, providing valuable insights into their operational behavior and confirming their potential for industrial applications.

4.7.1 Device Fabrication

The fabrication process for the trench Schottky barrier diode (SBD), as shown in Fig. 4.11, was carried out on an 11 μm thick epilayer, grown via Halide Vapor Phase Epitaxy (HVPE) on a conducting substrate provided by NCT Japan. The final structure, with all relevant dimensions, is illustrated in Fig. 4.12(a), while top-view microscope images of both small-area and large-area devices are presented in Fig. 4.12(b). The 1 μm deep fins were fabricated using BCl_3 -based Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE), with a Ni/SiO₂ hard mask, as

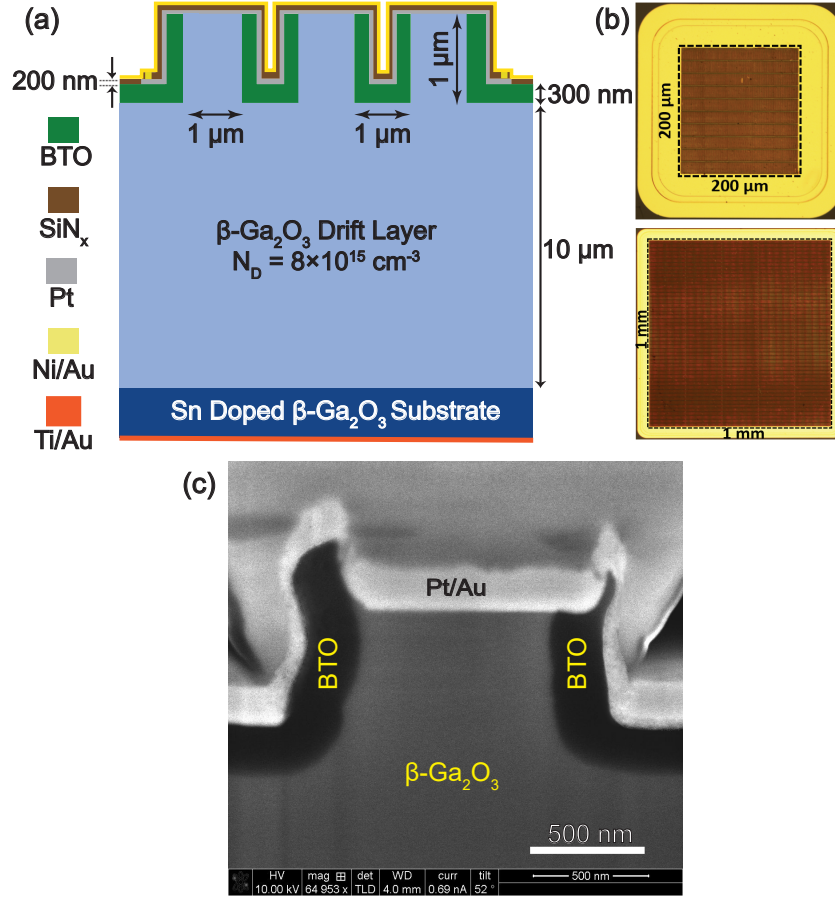


Figure 4.12: (a) Schematic diagram of the $\beta\text{-Ga}_2\text{O}_3$ high-k RESURF trench SBD. (b) The top-view microscope image of the fabricated small area ($200 \times 200 \mu\text{m}^2$) and large area ($1 \times 1 \text{ mm}^2$) SBDs. (c) Cross-sectional SEM image of the fabricated high-k RESURF trench SBD showing single fin. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

described in references [12], [13]. After the dry etching, the samples were immersed in HCl for 15 minutes to remove damage induced by the etching process [14], followed by a 5-minute dip in HF [7]. A 300 nm layer of BaTiO_3 (BTO) was sputter-deposited at room temperature and subsequently annealed at 700 $^\circ\text{C}$ in an O_2 environment to enhance its dielectric constant [15].

To enable contact deposition, the tops of the fins were exposed by selectively etching the BTO layer using SF_6/Ar -based ICP RIE with a Ni hard mask. Pt/Au (50/150 nm) was then deposited via electron beam evaporation, with planetary rotation to ensure a conformal coating. A passivation layer of SiN_x was applied using plasma-enhanced chemical vapor deposition (PECVD). Vias were etched into the SiN_x , after which Ni/Au (50/200 nm) probe pads were deposited. Lastly, Ti/Au (50/200 nm) ohmic contacts were deposited on the backside of the

sample via electron beam evaporation.

A cross-sectional scanning electron microscope (SEM) image, shown in Fig. 4.12 (c), reveals the rounding of the trench corners, with a radius of curvature of approximately 250 nm, resulting from the dry etching process. This rounding mitigates the concentration of electric fields at the trench corners.

For this structure, an aspect ratio (fin height to fin width) and area ratio (fin width to pitch size) of 1 were selected due to the limitations of optical lithography. Although a higher aspect ratio could improve RESURF performance, it would require the more complex process of electron beam lithography to produce sub-micron fins. To ensure reliable, high-yield fabrication with optical lithography, a fin width of 1 μm was used. Similarly, increasing the area ratio would reduce the on-state specific resistance (R_{on-sp}), but would necessitate a trench width narrower than the fin width. Given that the minimum achievable fin width with optical lithography is 1 μm , a narrower trench width would again demand more intricate lithography techniques.

4.7.2 Forward Current Voltage Characteristics of the high- κ RESURF Trench SBD

Fig. 4.13 (a) compares the linear current-voltage characteristics of the small-area high- κ RESURF trench SBD, a standard SBD [8], and a BTO field-plated SBD [8]. The differential specific on-resistance values are 6.8 $\text{m}\Omega\text{-cm}^2$, 7.1 $\text{m}\Omega\text{-cm}^2$, and 10.8 $\text{m}\Omega\text{-cm}^2$ for the simple, field-plated, and trench SBDs, respectively. The higher specific on-resistance of the trench SBD is likely due to damage induced on the fin sidewalls during the dry etching process, suggesting that the HF/HCl treatment did not fully recover the etch-induced damage. Such damage could potentially be mitigated by employing low-damage etching techniques, such as wet etching with hot phosphoric acid [17] or gallium etching [18].

Figs. 4.13 (b) and 4.13 (c) show the current-voltage characteristics for larger-area SBD devices. For the 1 mm^2 SBD, a peak current of 3.7 A is achieved at 5 V with a 10% duty cycle, while a current of 1.9 A is attained with a 95% duty cycle. The reduction in current at

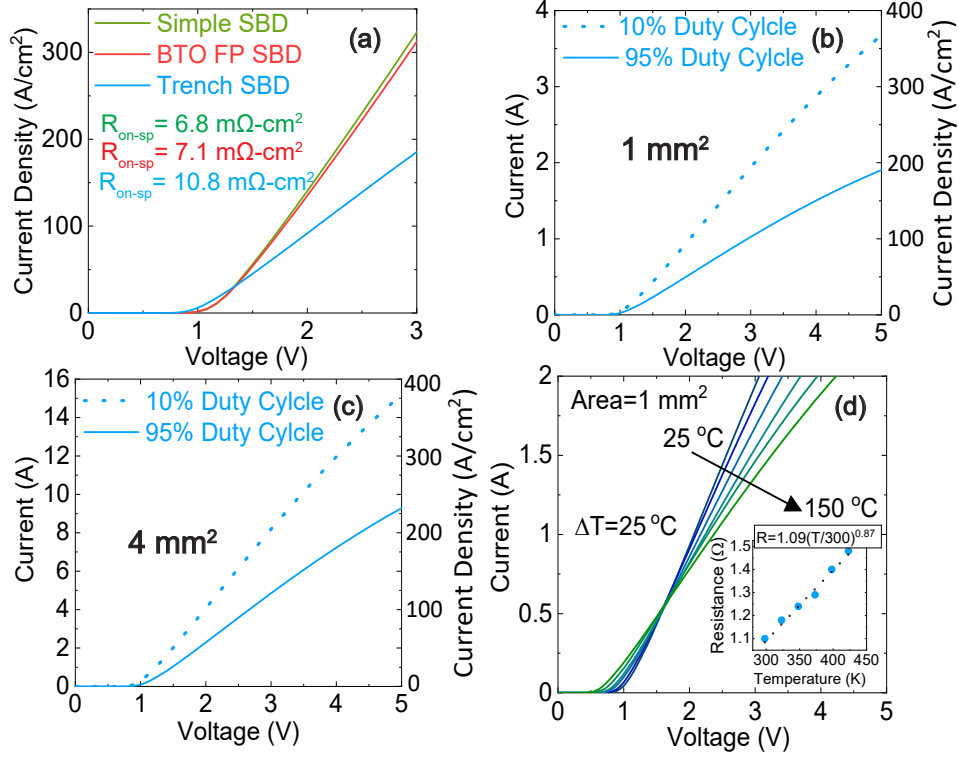


Figure 4.13: Current-voltage (I - V) plots for the β -Ga₂O₃ based (a) simple SBD, BTO field plated SBD and small area trench SBD, (b) 1 mm² large-area trench SBD (c) 4 mm² large-area trench SBD. (d) Temperature-dependent I - V characteristics for the 1 mm² trench SBD. The inset of (d) shows the temperature dependence of the differential on-resistance. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

higher duty cycles is attributed to self-heating effects within the SBD. The 95% duty cycle measurement closely approximates a DC measurement due to its prolonged operation periods. In the case of the 4 mm² SBD, it delivers a peak current of 15 A at 5 V under a 10% duty cycle and 9 A under a 95% duty cycle. To minimize the impact of self-heating on device performance, effective cooling and advanced packaging technologies should be employed [19]–[21].

Fig. 4.13 (d) presents the temperature-dependent I - V characteristics for the 1 mm² trench SBD. The turn-on voltage decreases from approximately 0.9 V at room temperature to about 0.6 V at 150 °C. The inset in Fig. 4.13 (d) shows the temperature dependence of the differential on-resistance (R_{on}). By fitting the R_{on} values using the power law expression $R_{on} = R_{on,300K}(T/300)^\alpha$, the temperature coefficient of resistance (α) for the trench SBD is found to be 0.87. This value is consistent with previously reported data (0.73 [19]) for β -Ga₂O₃-based SBDs and is significantly lower than that of SiC SBDs (2.95 [22]), indicating superior thermal

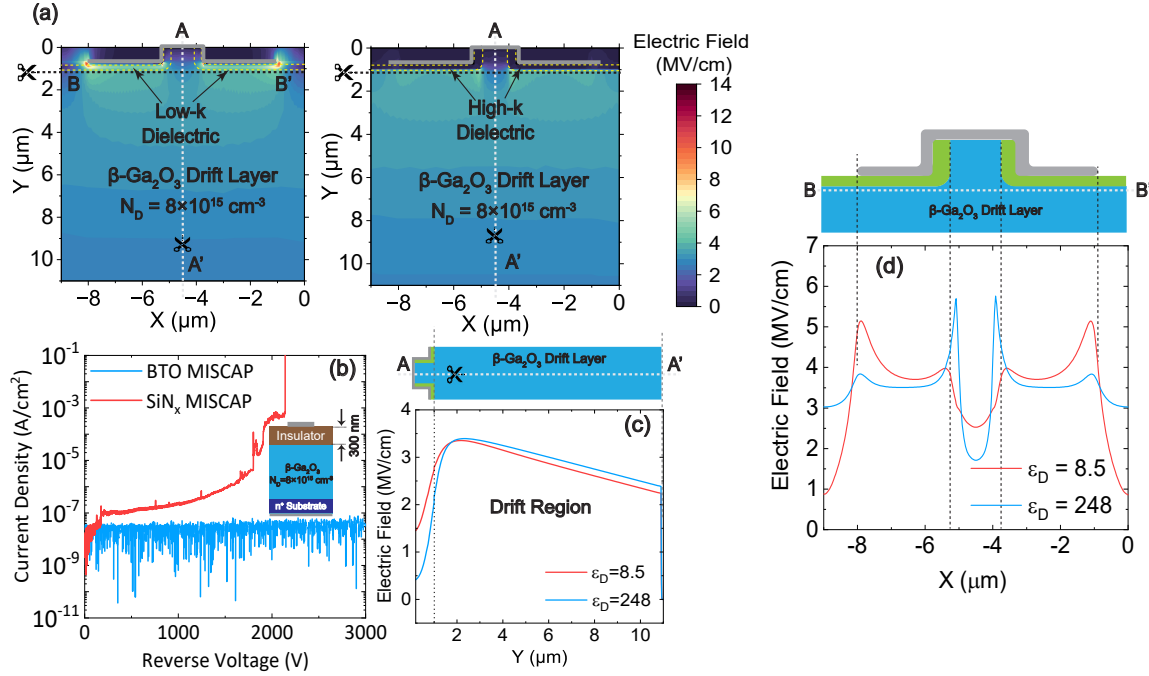


Figure 4.14: (a) Electric field contour plot of the low-k and high-k RESURF trench SBD extracted using SILVACO ATLAS simulation (Dielectric boundaries are marked with yellow dashed lines). (b) Experimentally measured I - V characteristics of the BTO (high-k) and SiN_x (low-k) MISCAPs and the electric field profile for the low-k and high-k RESURF trench SBD along (c) AA' cutline and (d) BB' cutline. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

stability for the β -Ga₂O₃-based devices.

4.7.3 Electric Field Simulations and Reverse Current Voltage Characteristics of the high- κ RESURF Trench SBD

Addressing the reverse characteristics, Fig. 4.14 (a) displays the contour plot of the electric field, simulated using SILVACO ATLAS, for the trench Schottky Barrier Diode (SBD) with low-k ($\epsilon_r = 8.5$) and high-k ($\epsilon_r = 248$) RESURF techniques. The simulation was conducted, incorporating rounded corners with a radius of curvature measuring 250 nm, as validated by the cross-sectional SEM image. It is evident that the low-k dielectric exhibits a significantly higher electric field within it compared to the high-k dielectric counterpart. This higher electric field for the low-k dielectric structure results in dielectric leakage and eventual breakdown, as evidenced by the fabricated Metal Insulator Semiconductor Capacitor (MISCAP) structure illustrated in

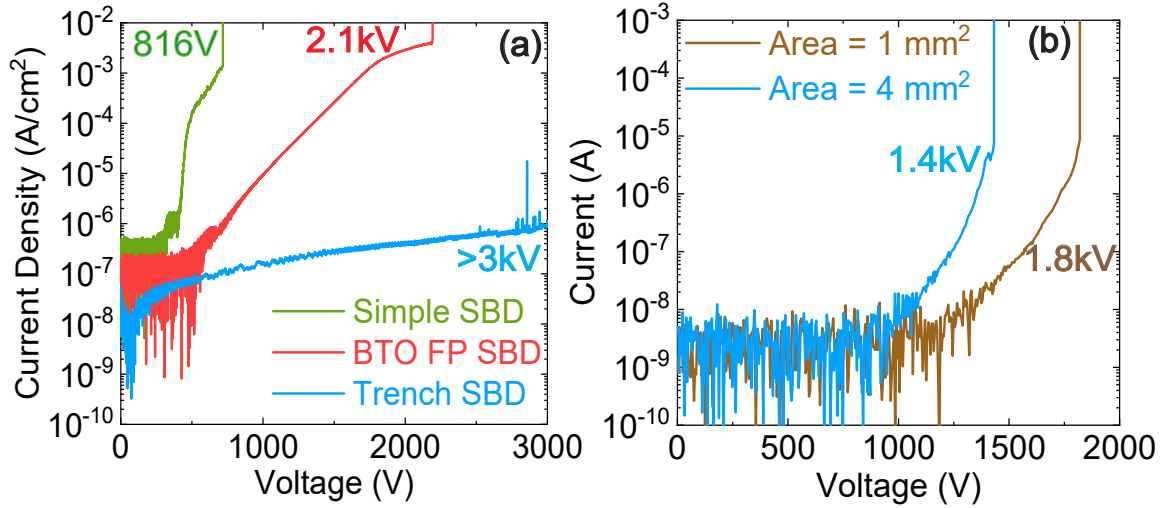


Figure 4.15: (a) Reverse I - V characteristics for the simple, BTO field plated, and small area high-k RESURF trench SBD. (b) Reverse I - V characteristics for the large area $1mm^2$ and $4mm^2$ high-k RESURF trench SBD. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

Fig. 4.14 (b) (Pt/Au and Ti/Au were used as the anode and cathode contacts, respectively). Specifically, the planar MISCAP utilizing low-k 300 nm thick SiN_x succumbs to breakdown at 2.1 kV with substantial dielectric leakage. Conversely, the BTO-based MISCAP, utilizing ~ 300 nm thick BTO, surpasses a 3 kV breakdown voltage with negligible leakage current ($< 10^{-7} A/cm^2$).

Fig. 4.14 (c) demonstrates the electric field profile along the AA' cutline for both the low-k and high-k RESURF trench SBDs. In the case of the low-k RESURF structure with a dielectric thickness of 300 nm, the electric field at the metal-semiconductor junction reaches approximately ~ 1.5 MV/cm. Conversely, for the high-k RESURF structure with the same thickness, the electric field at the metal-semiconductor interface remains below 0.5 MV/cm, indicating superior RESURF efficiency when employing a high-k dielectric. The electric field profiles along the BB' cutline for both low-k and high-k RESURF trench SBDs are depicted in Fig. 4.14 (d). Due to a greater potential drop in the low-k dielectric, the electric field in the drift layer is lower for the low-k RESURF trench SBD compared to its high-k counterpart. However, the electric field within the low-k dielectric exceeds approximately 15 MV/cm at 3 kV, which could result in dielectric breakdown in the low-k RESURF trench SBD. In applications where

higher doping is preferred, the electric field will scale in tandem with the doping concentration. Nonetheless, the trench SBD with high- κ RESURF still offers advantages over conventional planar Schottky Barrier Diodes (SBDs), whether with or without a field plate [8].

The reverse characteristics of the fabricated devices are presented in Fig. 4.15. Fig. 4.15 (a) illustrates the reverse current-voltage (I - V) plot for the simple, BTO field-plated, and high- κ RESURF trench SBDs. The breakdown voltages are determined as 816 V, 2.1 kV, and >3 kV for the simple, BTO field-plated, and high- κ RESURF trench SBDs, respectively. At breakdown, the extracted leakage current densities are 2 mA/cm^2 for the simple SBD, 4 mA/cm^2 for the BTO field-plated SBD, while for the trench SBD, the reverse leakage current at 3 kV is $1 \mu\text{A/cm}^2$, owing to the reduced electric field at the metal-semiconductor junction due to the trench structure. The reverse I - V characteristics for the larger-area devices are displayed in Fig. 4.15 (b). The 1 mm^2 device demonstrates a breakdown voltage of approximately ~ 1.8 kV, and the 4 mm^2 device exhibits a similar breakdown voltage of approximately ~ 1.4 kV. At these breakdown voltages, the extracted leakage currents are 4 and $5 \mu\text{A}$ for the 1 mm^2 and 4 mm^2 trench SBDs, respectively. This decline in breakdown voltage and simultaneous increase in leakage current with device area can be attributed to the presence of killer defects in the material [23], highlighting the need for further material development to unlock the full potential of $\beta\text{-Ga}_2\text{O}_3$. Nevertheless, it is noteworthy that the extracted leakage currents for the larger-area devices are one of the lowest among all ampere-class $\beta\text{-Ga}_2\text{O}_3$ based devices with similar dimensions.

4.7.4 High Voltage Capacitance-Voltage Characteristics of the high- κ RESURF Trench SBD

The switching losses for the large-area devices were evaluated using high-voltage capacitance-voltage (C - V) measurements conducted at 1 MHz, with the results shown in Fig. 4.16(a-c). At a bias of -1 kV , the capacitance values for the 1 mm^2 and 4 mm^2 Schottky Barrier Diodes (SBDs) were measured to be 8.4 pF and 35 pF , respectively. The capacitive stored charge (Q_C)

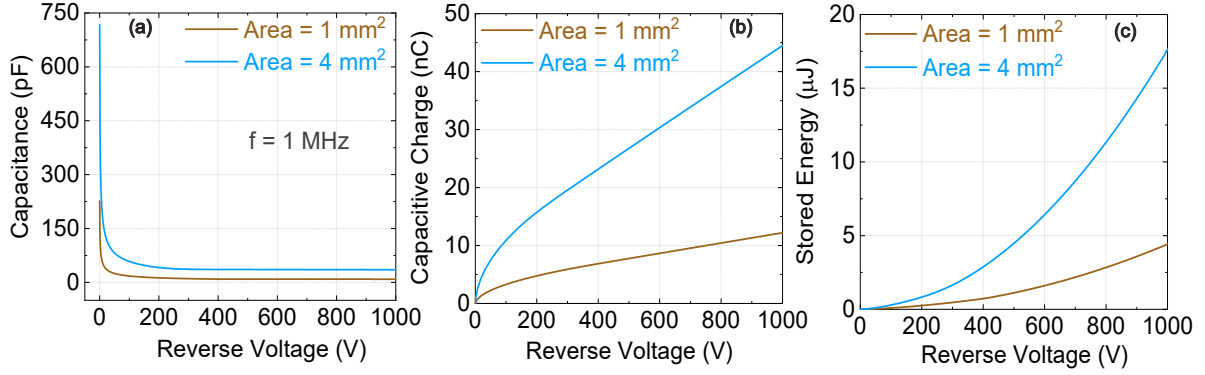


Figure 4.16: (a) Measured capacitance-voltage, (b) calculated capacitive stored charge, and (c) capacitive stored energy for the 1mm^2 and 4mm^2 high-k RESURF trench SBD with Pt anode contact. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

is determined using the integral:

$$Q_C = \int_0^{V_R} C(v_R) dv_R \quad (4.20)$$

Additionally, the stored energy (E_C) is calculated by:

$$E_C = \int_0^{V_R} C(v_R) v_R dv_R \quad (4.21)$$

where $C(v_R)$ is the capacitance as a function of the reverse voltage (V_R). The extracted stored charge amounts to 12 nC and 44 nC , while the stored energies are 4.4 μJ and 17.5 μJ for the 1 mm^2 and 4 mm^2 SBDs, respectively. Notably, the $\beta\text{-Ga}_2\text{O}_3$ trench SBDs exhibit significantly lower capacitance, stored charge, and stored energy compared to commercial SiC devices. The only drawback is the higher forward voltage drop in the $\beta\text{-Ga}_2\text{O}_3$ SBDs, primarily due to the higher on-resistance, which includes contributions from the thick doped substrates (650 μm). However, the leakage currents of the trench SBDs are notably lower than those of SiC SBDs. Further reduction in the on-resistance of the $\beta\text{-Ga}_2\text{O}_3$ trench SBDs could be achieved by employing low-damage etching techniques for fin formation and by thinning down the substrates. Additionally, accessing higher electric fields would allow for thinner drift regions, thereby further reducing the on-resistance.

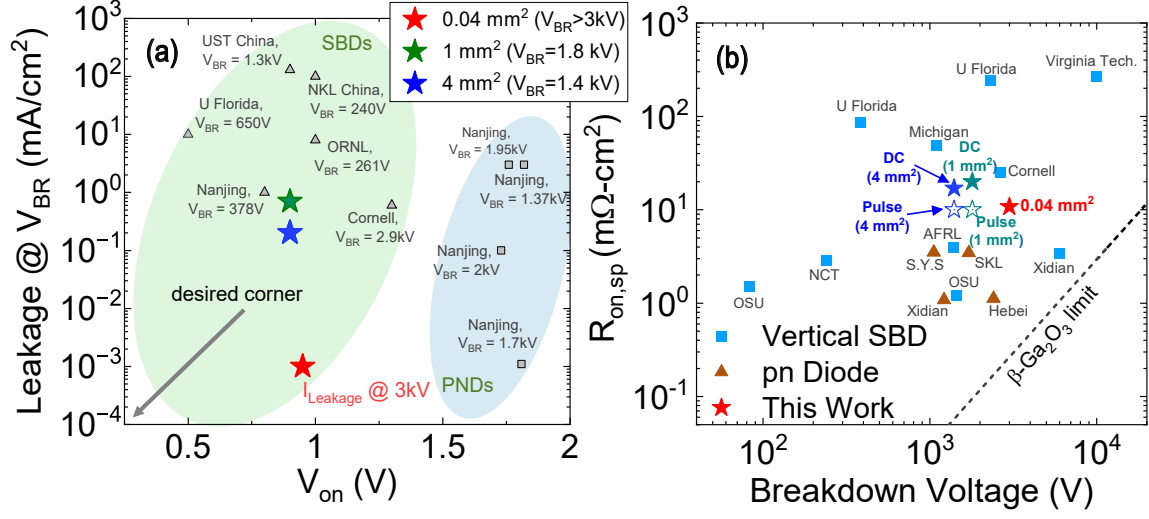


Figure 4.17: Benchmark plot showing (a) leakage at the breakdown voltage vs. the turn-on voltage and (b) R_{on-sp} vs V_{BR} for the state-of-the-art β -Ga₂O₃ based diodes. Reprinted from Roy *et al.* [16], with the permission from AIP Publishing.

4.7.5 Benchmarking and Summary

Figure 4.17 (a) and (b) present a comparative benchmark plot of leakage current at breakdown versus turn-on voltage, and R_{on-sp} versus V_{BR} for β -Ga₂O₃ diodes. Notably, the pn-heterojunction diodes exhibit lower leakage currents ($I_{Leakage}$) but higher turn-on voltages (V_{on}), while Schottky Barrier Diodes (SBDs) display lower V_{on} values but higher leakage currents. The high-k RESURF trench SBDs highlighted in this study show the most favorable $V_{on}I_{Leakage}$ product among β -Ga₂O₃ power devices, with a current exceeding 1A and a breakdown voltage above 1kV. The small-area trench SBD, with an R_{on-sp} of 10.8 m Ω -cm² and an estimated breakdown voltage of 3kV, achieves a PFOM of 0.83 GW/cm². In comparison, the large-area SBD exhibits a PFOM of 305 MW/cm² for the 1 mm² trench SBD, and 185 MW/cm² for the 4 mm² trench SBD. Further improvements in PFOM can be realized by reducing the specific on-resistance, either through low-damage etching techniques or substrate thinning.

4.8 Vertical Trench Schottky Barrier Diode with High- κ Dielectric RESURF Featuring Low Work-function Ru Contact

The performance of power rectifiers is critically dependent on both the forward voltage drop and reverse leakage currents [5], [16]. In Schottky rectifiers, the forward voltage drop is determined by the Schottky barrier height (SBH) and the on-resistance of the drift region. While a lower SBH reduces the forward voltage drop, it tends to increase reverse leakage currents due to enhanced thermionic field emission in regions with high surface electric fields. The trench architecture, by leveraging the RESURF (Reduced Surface Field) effect, mitigates these surface electric fields at the metal/semiconductor junction, enabling the use of lower work-function metals for the anode contact. As shown in the previous section, employing a high- κ RESURF dielectric further decreases the surface electric field at the Schottky interface [16]. This allows the implementation of low work-function anode metals, reducing both the turn-on voltage and forward voltage drop. Additionally, the use of high- κ dielectrics reduces electric fields within the dielectric layer at the trench bottom, minimizing dielectric leakage [16].

In this section, we demonstrate a high-performance β -Ga₂O₃ trench Schottky barrier diode that incorporates a high- κ dielectric RESURF and a low work-function ruthenium (Ru) anode contact. To minimize sputter-induced damage during the deposition of the high- κ dielectric, a thin 20 nm Al₂O₃ interfacial layer was applied using atomic layer deposition (ALD) between the high- κ dielectric and the Ga₂O₃ fins. By using a low work-function metal for the Schottky contact, we achieved a turn-on voltage of just 0.5V, a significant reduction compared to the 1V observed with platinum (Pt) contacts. The 1 mm² and 4 mm² devices demonstrated maximum forward currents of 6A and 20A, respectively, at a forward voltage of 5V. Additionally, the smaller devices exhibited breakdown voltages exceeding 3kV, while the larger 1 mm² and 4 mm² devices achieved breakdown voltages of 1.74kV and 1.42kV, respectively.

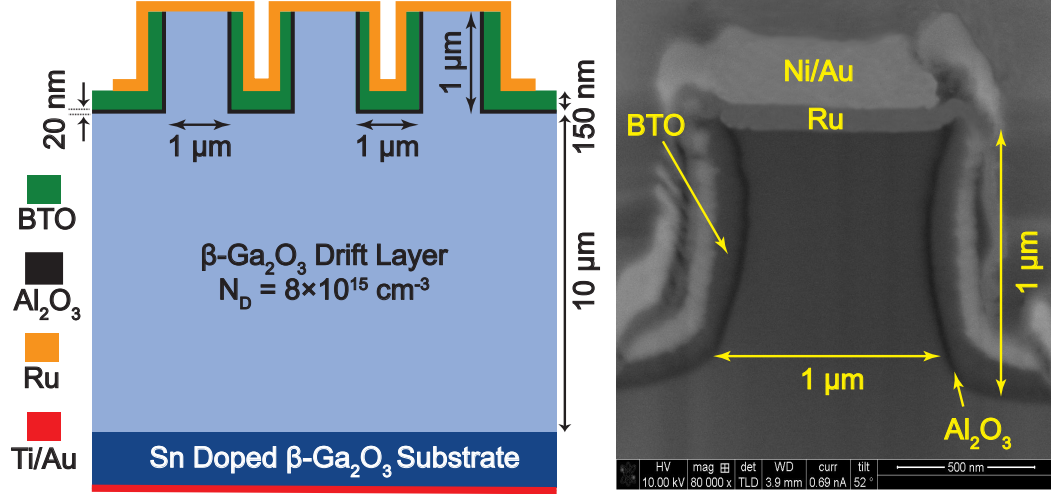


Figure 4.18: Structure of the β -Ga₂O₃ high- κ RESURF trench SBD with Ru anode contact and cross-sectional SEM image of a fabricated device. Reprinted from Roy *et al.* [24] © 2024 IEEE.

4.8.1 Device Fabrication

The fabrication process for the trench Schottky barrier diode (SBD) illustrated in Fig. 4.18 closely follows the methodology used for the high- κ RESURF trench SBD with Pt contact, as detailed in Section 4.7.1, with some minor modifications. The device fabrication commenced with an 11 μm thick β -Ga₂O₃ epilayer, which was grown on a conducting substrate (NCT Japan) using Halide Vapor Phase Epitaxy (HVPE). To create the 1 μm deep fins, BCl₃-based Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE) was employed, utilizing a sputtered Ru/PECVD-SiO₂ hard mask. After the dry etching process, the samples underwent a 15-minute immersion in HCl to remove any dry etch-induced damage [14], followed by a 5-minute dip in HF.

Subsequently, a 20 nm thick layer of Al₂O₃ was deposited using atomic layer deposition (ALD) to passivate the sidewalls. This was followed by sputter deposition of a 150 nm thick layer of BaTiO₃ (BTO) at room temperature, which was then annealed at 700 °C in an O₂ atmosphere to enhance the dielectric constant [8], [15]. The BTO atop the fin regions was etched away using SF₆/Ar-based dry etching, employing a Ni hard mask, with the etching process monitored in situ using a LASER etch monitor on a control sample. The Al₂O₃ layer on the fin regions was subsequently wet etched using AZ 300MIF (TMAH-based) developer, with an etch

rate of approximately 1.3–1.5 nm/min measured on a control sample.

Next, 800 cycles of ALD Ru (approximately 100 nm) were deposited using (ethylbenzene) (1,3-cyclohexadiene)ruthenium (EBCHDRu) and O_2 cycles at 300 °C, achieving a deposition rate of 1.2 Å/cycle. The SBDs were isolated by selectively etching the ALD Ru metal using O_2/Cl_2 -based ICP-RIE. This was followed by the deposition of Ni/Au probe pads via electron beam evaporation. Finally, Ti/Au ohmic contacts were deposited on the backside of the sample, also using electron beam evaporation, with no contact annealing performed after the deposition of the cathode ohmic contacts. The cross-sectional scanning electron microscope (SEM) image of the fabricated device is shown in Fig. 4.18.

4.8.2 Device Simulation and Current-Voltage Characteristics

Fig. 4.19 (a) presents a contour plot of the electric field for a simulated high-k RESURF trench Schottky barrier diode (SBD) with a Ru contact under reverse bias conditions, generated using SILVACO ATLAS. The work function of the Schottky metal is specified as 4.71 eV. Within the dielectric, the electric field remains negligible due to its high permittivity. The field profile along the A-A' cutline, illustrated in Fig. 4.19(a) for various fin widths, reveals that as the fin width decreases—resulting in a higher aspect ratio—the surface electric field at the metal-semiconductor junction diminishes, a phenomenon attributed to the enhanced RESURF effect.

Reverse leakage currents were simulated using thermionic and tunneling models in SILVACO, with the results presented in Fig. 4.19 (c). Notably, the reverse leakage currents also decrease as the fin width reduces, correlating with the lowered surface electric field. This approach demonstrates that by achieving a sufficiently high aspect ratio, it is possible to mitigate the surface electric field, thereby facilitating the use of low-workfunction metals as anode contacts, which in turn helps reduce the turn-on voltage.

Fig. 4.20 (a) illustrates the typical current-voltage characteristics in linear scale for the fabricated small-area ($200 \times 200 \mu m^2$) high-k RESURF trench Schottky barrier diodes (SBDs)

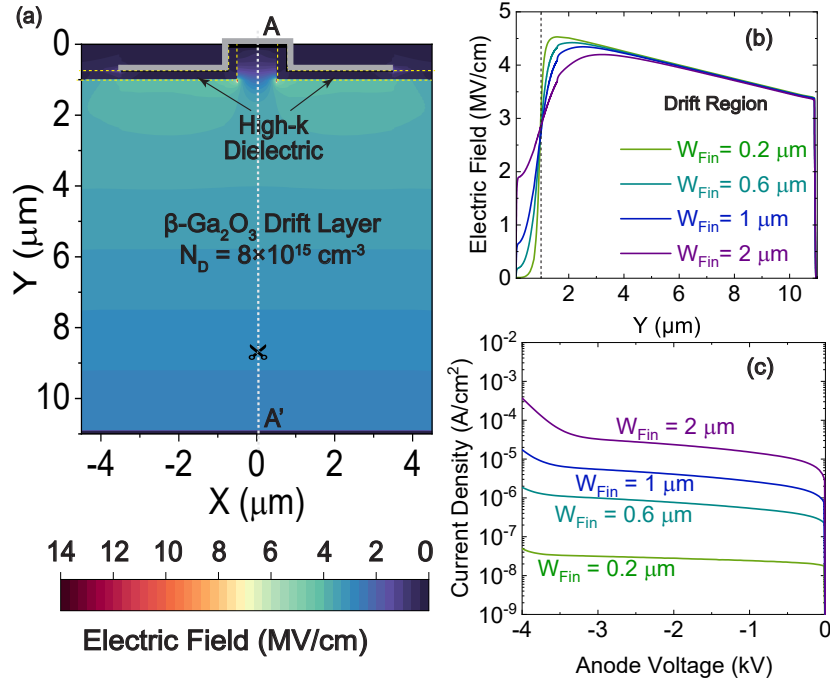


Figure 4.19: (a) Electric field contour plot of the high-k RESURF trench SBD with Ru contact under a reverse bias of 4 kV extracted using SILVACO ATLAS simulation (Dielectric boundaries are marked with yellow dashed lines). (b) Electric field profile for the high-k RESURF trench SBD along AA' cutline for different fin widths. (c) Simulated reverse leakage current densities for the high-k RESURF trench SBDs with different fin widths. Reprinted from Roy *et al.* [24] © 2024 IEEE.

with both Pt and Ru contacts. Normalization is performed by considering the entire device footprints. The built-in potential for the devices is extracted from the IV characteristics, as shown in Fig. 4.20 (a). The Schottky barrier heights are determined to be 0.74 eV for the trench SBD with Ru contact and 1.2 eV for the one with Pt contact. Notably, the trench SBD featuring the Ru contact exhibits a significantly lower turn-on voltage (X-intercept of the linear I-V curve) of 0.5 V, compared to the 1 V turn-on voltage observed in the trench SBD with Pt contact. The differential specific on-resistance (R_{on-sp}) values are calculated to be $10.8 \text{ m}\Omega\text{-cm}^2$ for the trench SBD with Pt contact and $8.9 \text{ m}\Omega\text{-cm}^2$ for the one with Ru contact, accounting for current spreading.

Fig. 4.20 (b) presents the current-voltage characteristics of the large-area SBDs. The devices achieve a maximum forward current of 6 A and approximately 20 A at 5 V with a 10% duty cycle for the 1 mm^2 and 4 mm^2 trench SBDs with Ru contact. In comparison, the trench SBDs with Pt contact reach forward currents of 3.5 A and 15 A for the 1 mm^2 and 4 mm^2

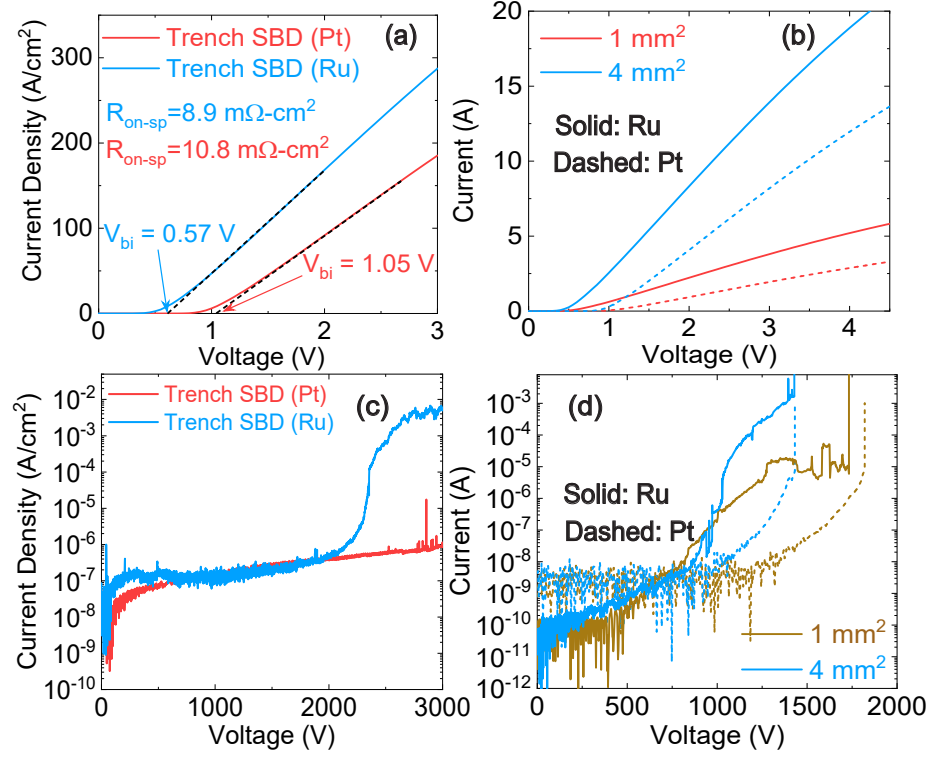


Figure 4.20: Current-voltage (I - V) plots for the β -Ga₂O₃ based (a) small area (200 × 200 μm^2) trench SBD with Pt and Ru contact, (b) Large area (1 mm² and 4 mm²) trench SBD with Pt and Ru anode contacts. (c) Reverse I - V characteristics of small area trench SBD with Pt and Ru contact. (d) Reverse I - V characteristics for the large area trench SBDs with Pt and Ru anode contact. Reprinted from Roy *et al.* [24] © 2024 IEEE.

devices, respectively. By considering a 45° current spreading angle, the extracted R_{on-sp} for the large-area SBD with Ru contact is 7.3 m Ω -cm² (4 mm²) and 6.9 m Ω -cm² (1 mm²), whereas the R_{on-sp} for the large-area SBD with Pt contact is 9.5 m Ω -cm² (4 mm²) and 9.4 m Ω -cm² (1 mm²). The variations in extracted R_{on-sp} values for the 4 mm², 1 mm², and 0.04 mm² devices may be attributed to device-to-device variation and the non-uniformity of the epitaxial layer across the wafer. Additionally, in the case of the large-area SBDs, the turn-on voltage remains at 0.5 V for the trench SBDs with Ru contact, in contrast to the 1 V turn-on voltage for the trench SBD with Pt contact.

Fig. 4.20(c) presents the reverse current-voltage (I - V) characteristics for the small-area devices. Both trench SBDs with Pt and Ru contacts exhibit breakdown voltages exceeding 3 kV. However, the extracted reverse leakage current density at 3 kV for the trench SBD with Pt contact is measured at 1 $\mu\text{A}/\text{cm}^2$, while the leakage current density for the trench SBD with

Ru contact rises significantly to 5 mA/cm^2 . This increase is attributed to the reduced Schottky barrier height (SBH) associated with the low work-function metal.

The reverse I-V characteristics for the larger-area devices are shown in Fig. 4.20(d). For the trench SBD with Pt contact, the 1 mm^2 device demonstrates a catastrophic breakdown voltage of approximately 1.8 kV, while the 4 mm^2 device exhibits a breakdown voltage of around 1.4 kV. In contrast, the trench SBD with Ru contact shows a breakdown voltage of approximately 1.74 kV for the 1 mm^2 device and approximately 1.42 kV for the 4 mm^2 device. At the respective breakdown voltages, the leakage currents for the trench SBD with Pt contact are $4 \text{ }\mu\text{A}$ and $5 \text{ }\mu\text{A}$ for the 1 mm^2 and 4 mm^2 diodes, respectively. Meanwhile, the leakage currents for the trench SBD with Ru contact increase to $100 \text{ }\mu\text{A}$ and 2 mA for the 1 mm^2 and 4 mm^2 diodes, respectively. This decline in breakdown voltage and the simultaneous increase in leakage current with device area can be attributed to the presence of killer defects in the material [23], underscoring the necessity for further material development to fully realize the potential of $\beta\text{-Ga}_2\text{O}_3$.

4.8.3 High-Voltage Capacitance-Voltage Characteristics and Benchmarking

To evaluate the switching performance, high-voltage capacitance measurements were conducted on the large-area high- κ RESURF trench SBDs with Ru contacts, as illustrated in Fig. 4.21, following the methodology described in Section 4.7.4. The capacitive stored charge and stored energies were calculated using (4.20) and (4.21), respectively. For comparison, bare die SiC SBDs were selected to eliminate any additional parasitic capacitances associated with packaging.

Table 4.1 presents the performance metrics of power diodes based on both static and switching characteristics. The extracted stored charges amount to 16 nC and 58 nC , while the stored energies are $6.2 \text{ }\mu\text{J}$ and $26 \text{ }\mu\text{J}$ for the 1 mm^2 and 4 mm^2 SBDs at 1200 V, respectively. Notably, the $\beta\text{-Ga}_2\text{O}_3$ trench SBDs demonstrate significantly lower capacitance, stored charge, and stored energy compared to commercial bare die SiC devices. This indicates the potential for $\beta\text{-Ga}_2\text{O}_3$ to offer superior performance in high-speed switching, paving the way for advancements in

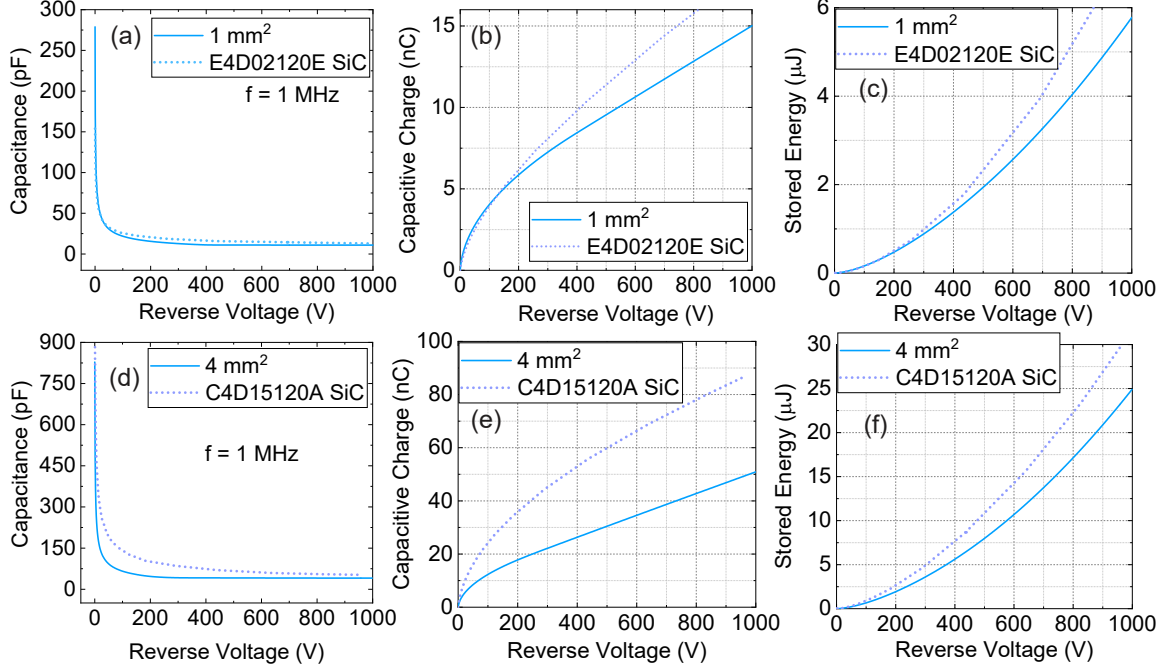


Figure 4.21: (a) Measured capacitance-voltage, (b) calculated capacitive stored charge, and (c) capacitive stored energy for the 1 mm^2 and 4 mm^2 high- k RESURF trench SBD with Ru anode contact and comparison with commercial bare die SiC JBS diodes.

power electronics technology.

In Fig. 4.22(a), a comparative benchmark plot illustrates the trade-off between leakage current at 1200 V ($I_{Leakage}$) and forward voltage drop (V_F) in $\beta\text{-Ga}_2\text{O}_3$ -based diodes. The pn-heterojunction diodes (pn-HJDs) exhibit lower leakage currents but higher turn-on voltages, leading to an increased forward voltage drop. In contrast, Schottky Barrier Diodes (SBDs) display lower V_F values but suffer from higher leakage currents. The high- k RESURF trench SBDs stand out with the most favorable $V_F I_{Leakage}$ product among $\beta\text{-Ga}_2\text{O}_3$ -based power devices, meeting the criteria of exceeding 1A in current and surpassing 1kV in breakdown voltage.

Another important metric used to characterize the trade-off between conduction and switching power loss in power devices is $Q_C V_F$, the product of the capacitive stored charge (Q_C) in the diodes and the forward voltage drop (V_F). The forward voltage is measured at the voltage where the current density reaches 250 A/cm^2 . The Ga_2O_3 SBDs and HJDs considered for comparison from the literature all experience punch-through at 1200 V. For these punch-through devices, Q_C

Table 4.1: Performance metric comparison of power diodes

Device	Ref	Area (mm ²)	V_F ^a (V)	$J_R@1200V$ (A/cm ²)	$Q_C@1200V$ (nC)
SBD	[25]	1	2.6	10^{-5}	~95
	[26]	0.78	2.8	5×10^{-4}	~9.2
	[16]	1, 4	3.5, 3	$5, 12.5 \times 10^{-8}$	14, 52
HJD	[10]	9	7	1.11×10^{-6}	~95
	[27]	9	7.35	7×10^{-5}	~95
SiC JBS ^b	—	5.1	1.75	4.9×10^{-3}	~68
SiC JBS ^c	—	4.97	1.5	5×10^{-3}	~45
This work (Ru)	—	1	2.37	2.64×10^{-4}	16
	—	4	2.22	45×10^{-4}	58

^a V_F =Forward voltage drop @ 250 A/cm²

^bWolfspeed, CPW4-1200-S010B, Gen 4 Silicon Carbide Schottky Diode

^cROHM, S6602, SiC Schottky Barrier Diode Bare Die

is calculated using $Q_C = CV_{BR}$, where $C = \epsilon_S A / t_{drift}$ represents the capacitance of the device; ϵ_S is the permittivity of the semiconductor, A is the device area, V_{BR} is the breakdown voltage, and t_{drift} is the thickness of the drift layer. High-voltage capacitance-voltage characterization of the trench SBDs with Ru contact reveals a very low $Q_C V_F$ product, as shown in Table 6.2 and Fig. 4.22 (b). However, it is important to note that the $Q_C V_F$ switching figure of merit (FOM) may not be directly comparable for devices with differing current ratings. Overall, these findings highlight the promise of β -Ga₂O₃ high- κ RESURF trench SBDs with low work-function anode contact in enhancing power electronics efficiency and performance.

4.9 Summary

In summary, this chapter emphasizes the critical role of managing reverse leakage currents in achieving high-efficiency power electronic devices. By exploring various strategies to minimize leakage currents caused by barrier tunneling at high reverse bias, the chapter outlines both the advantages and limitations of these approaches. The significance of two-dimensional field

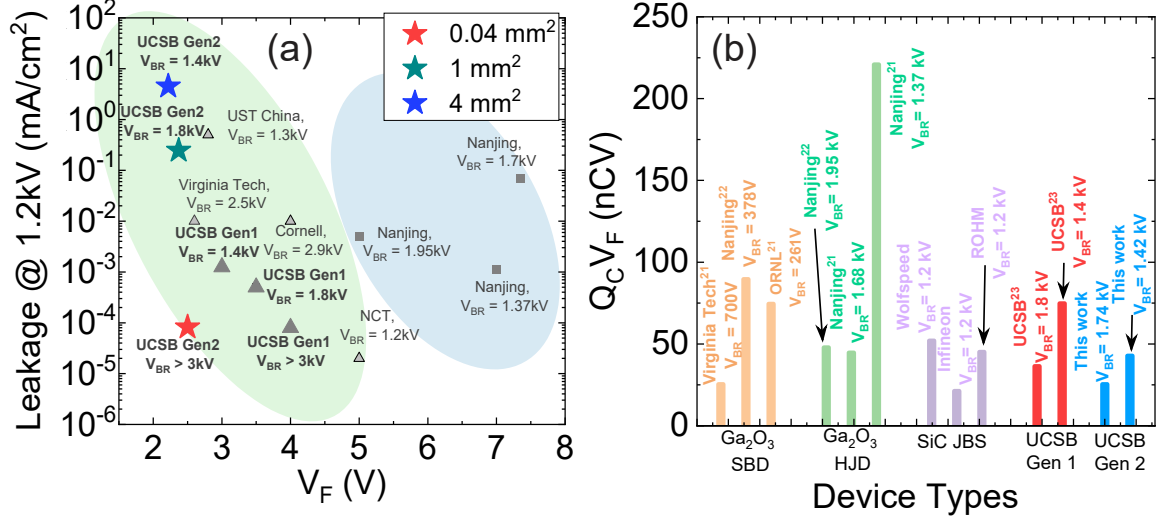


Figure 4.22: Benchmark plot showing (a) leakage at 1.2kV voltage vs. the forward voltage drop for the state-of-the-art β -Ga₂O₃ based diodes. [Reprinted from Roy *et al.* [24] © 2024 IEEE.] (b) Extracted $Q_C V_F$ product for different β -Ga₂O₃ diodes and comparison with commercial bare die SiC JBS diodes.

engineering is highlighted, particularly through trench Schottky barrier diodes, which effectively reduce electric fields at the metal/semiconductor junction, thereby mitigating thermionic field emission. An analytical examination reveals how the high dielectric constant of the RESURF dielectric enhances the RESURF effect while concurrently minimizing dielectric leakage.

Furthermore, two device architectures featuring high- κ RESURF are presented—one employing a high work-function anode contact and the other utilizing a low work-function anode contact—illustrating the potential of these designs in improving device performance.

The β -Ga₂O₃ high- κ RESURF trench SBD with Pt contact demonstrates significant advancements in both small and large-area devices. The larger devices, spanning 1 mm² and 4 mm², showcase impressive forward currents reaching 3.5 A and 15 A, respectively, accompanied by breakdown voltages of 1.8 kV and 1.4 kV. The extracted temperature coefficient of resistance ($\alpha = 0.87$) for β -Ga₂O₃ SBDs is lower than that of SiC, underlining the superior thermal stability of this technology. The small-area devices exhibit a remarkable breakdown voltage exceeding 3 kV with minimal reverse leakage current, demonstrating their robustness. Importantly, the analysis of capacitance, stored charge, and switching energies underscores the superior switching capabilities of β -Ga₂O₃-based SBDs, positioning them as a viable alternative

to commercially available SiC SBDs.

The introduction of a low work-function Schottky contact in the second β -Ga₂O₃ vertical high- κ RESURF trench SBD further enhances performance. Key features include a low turn-on voltage of 0.5 V, a high breakdown voltage exceeding 1 kV, and forward currents of up to 6 A and 20 A for larger devices, with smaller area devices maintaining a high breakdown voltage of over 3 kV. A low $Q_C V_F$ product indicates an excellent trade-off between switching and conduction power loss. Potential improvements may include further reducing turn-on voltage by employing lower work-function metals and increasing the aspect ratio of the fins. Additionally, substrate thinning could lower R_{on-sp} and forward voltage drop.

These achievements represent significant progress, yet further enhancements through material refinement, the implementation of low-damage etching techniques, substrate thinning, and improved thermal management hold the potential to unlock even greater performance. Overall, this work sets the stage for future advancements in power electronics, focusing on optimizing leakage current management through innovative diode structures.

However, all these field engineering strategies described in this chapter and previous chapters are ultimately constrained by Baliga's figure of merit (FOM) for the materials discussed in Chapter 1. This limitation arises from the formation of triangular electric fields in the drift region of power devices, which is not the most effective field profile for achieving high breakdown voltage. The next chapter will explore the engineering of the electric field throughout the entire drift region and discuss methods to surpass the theoretical unipolar figure of merit of wide and ultra-wide bandgap materials.

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Chapter 5

β -Ga₂O₃ Extreme Permittivity Dielectric Superjunction Schottky Barrier Diodes

5.1 Introduction

Unipolar (majority carrier) devices are highly attractive for power applications due to their inherently fast switching speeds. In contrast to bipolar devices, where minority carrier storage in the drift region during conduction severely slows down switching, unipolar devices avoid this limitation. In majority carrier devices, no minority carriers are stored in the drift region, and switching speed is determined only by the charging of intrinsic and parasitic device capacitances. This makes unipolar devices particularly favorable for high-speed switching applications.

However, the primary drawback of unipolar devices is their high on-resistance. The device doping concentration must be kept low to support high breakdown voltages, which limits the overall performance. Bipolar devices based on high carrier lifetime indirect bandgap semiconductors, on the other hand, benefit from conductivity modulation—under high-level injection conditions, the minority carrier concentration in the drift region can surpass the background doping level, leading to an influx of majority carriers to maintain charge neutrality. This significantly reduces the on-resistance of the drift region. Since conductivity modulation does not

occur in unipolar devices, the on-resistance is constrained by the low doping concentrations required to achieve high breakdown voltages.

As a result, Baliga's Figure of Merit (FOM) or the Unipolar Figure of Merit imposes a fundamental trade-off between breakdown voltage and specific on-resistance in unipolar devices. This FOM establishes an upper bound, dictated by the intrinsic material properties, beyond which device performance cannot be pushed without compromising either on-resistance or breakdown voltage. While extensive device engineering can help minimize non-idealities, as discussed in previous chapters, unipolar devices remain confined by this theoretical limit.

In this chapter, strategies to overcome the limitations imposed by Baliga's Figure of Merit are explored, including advanced techniques in device design and material engineering that have the potential to push performance beyond this boundary. These methods aim to address the inherent challenges of unipolar devices and pave the way for next-generation power electronics capable of breaking through the constraints of the unipolar FOM.

5.2 Surpassing the Unipolar FOM: Superjunctions

In a Schottky barrier diode (SBD), the application of a reverse bias voltage causes the electric field within the device to take on a triangular profile, as illustrated in Fig. 5.1 (a). This profile results from the charge distribution in the semiconductor, governed by Poisson's equation:

$$\frac{\partial E_S(x)}{\partial x} = \frac{qN_D}{\epsilon_S} \quad (5.1)$$

Here, E_S is the electric field in the semiconductor, N_D represents the doping concentration in the semiconductor, q is the elementary charge, and ϵ_S is the permittivity of the semiconductor material. From this relationship, it becomes clear that the slope of the electric field is proportional to the doping concentration N_D and inversely proportional to the permittivity ϵ_S , yielding a linear field profile.

Device breakdown occurs when the peak electric field at the metal/semiconductor interface

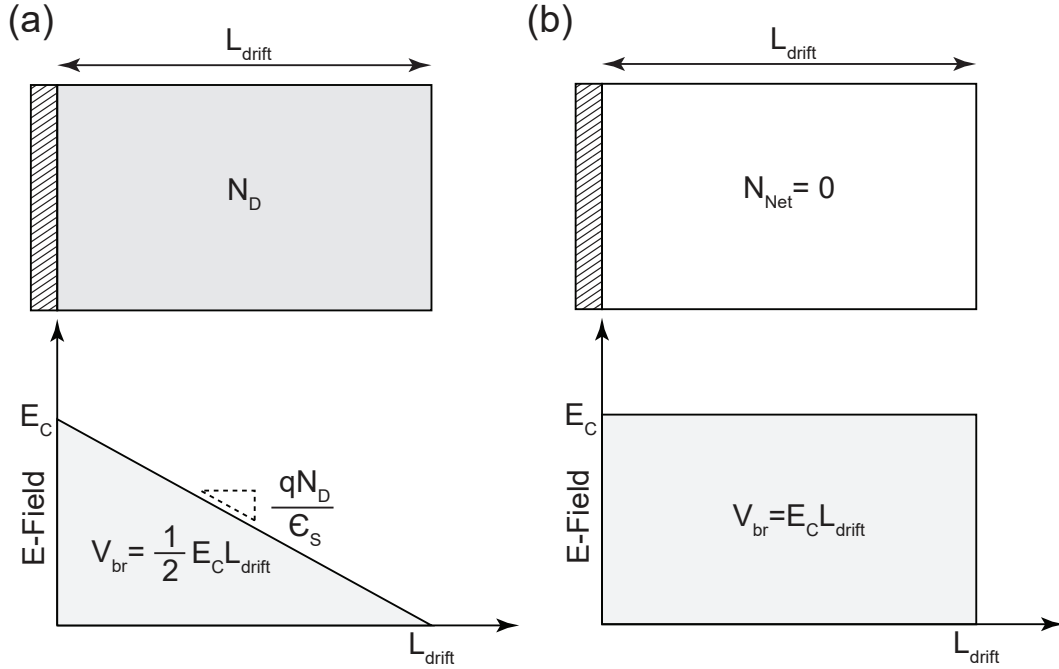


Figure 5.1: Electric field profile of Schottky barrier diode with (a) doping concentration N_D and (b) for un-doped device.

reaches the material's critical electric field, E_C . The breakdown voltage, V_{br} , which is determined by the voltage required to reach this critical field, can be calculated by integrating the electric field over the drift region. Therefore, the breakdown voltage is related to the drift region length L_{drift} and critical electric field E_C by the following equation:

$$V_{br} = \frac{1}{2} E_C L_{drift} \quad (5.2)$$

According to (5.1), increasing the doping concentration in the drift region leads to a steeper slope in the electric field profile, causing the device to reach the critical electric field, E_C , at a lower voltage. Conversely, if the semiconductor is fully undoped (i.e., no charge is present or equal concentrations of ionized acceptors and ionized donors are present), the gradient of the electric field becomes zero:

$$\frac{\partial E_S(x)}{\partial x} = 0 \quad (5.3)$$

In this case, the electric field takes on a rectangular profile, and the breakdown voltage can

be derived as:

$$V_{br} = E_C L_{drift} \quad (5.4)$$

Thus, the breakdown voltage doubles when a rectangular field profile is achieved compared to the triangular one. However, the absence of charge in the semiconductor also implies the lack of free carriers, leading to infinite on-resistance during the forward conduction mode.

If, however, the dependency of charge during forward conduction and reverse bias is decoupled—such that the device maintains finite on-resistance under forward conduction due to doping concentration while, under reverse bias, if the device can be engineered to exhibit zero net charge, it would enable the formation of a rectangular electric field profile. This design would allow for the significant advantage of a higher breakdown voltage without sacrificing the conductivity in the forward mode, thus providing the best of both worlds: reduced on-resistance and enhanced breakdown performance.

A charge-balanced periodic p- and n-doped layer, as illustrated in Fig. 5.2, can effectively emulate this scenario. In forward bias, current flows through the n-doped drift layer, ensuring standard device operation with finite on-resistance. During reverse bias, the p/n junctions within the drift region deplete, relieving electric field stress at the metal/semiconductor junction. Once the drift region is fully depleted, the n- and p-regions supply charges of opposite signs, resulting in their electric fields canceling each other out for the most part—this is known as the charge balance principle. Consequently, a rectangular electric field profile forms in the drift region, which significantly enhances the breakdown voltage without degrading forward conduction performance.

Moreover, the lateral depletion of the drift region enables the use of higher doping concentrations without raising the electric field at the metal/semiconductor junction, leading to lower on-resistance in unipolar devices. This method presents a promising strategy for advancing power device performance by integrating the advantages of reduced on-resistance and increased breakdown voltage, all while maintaining device reliability and operational efficiency.

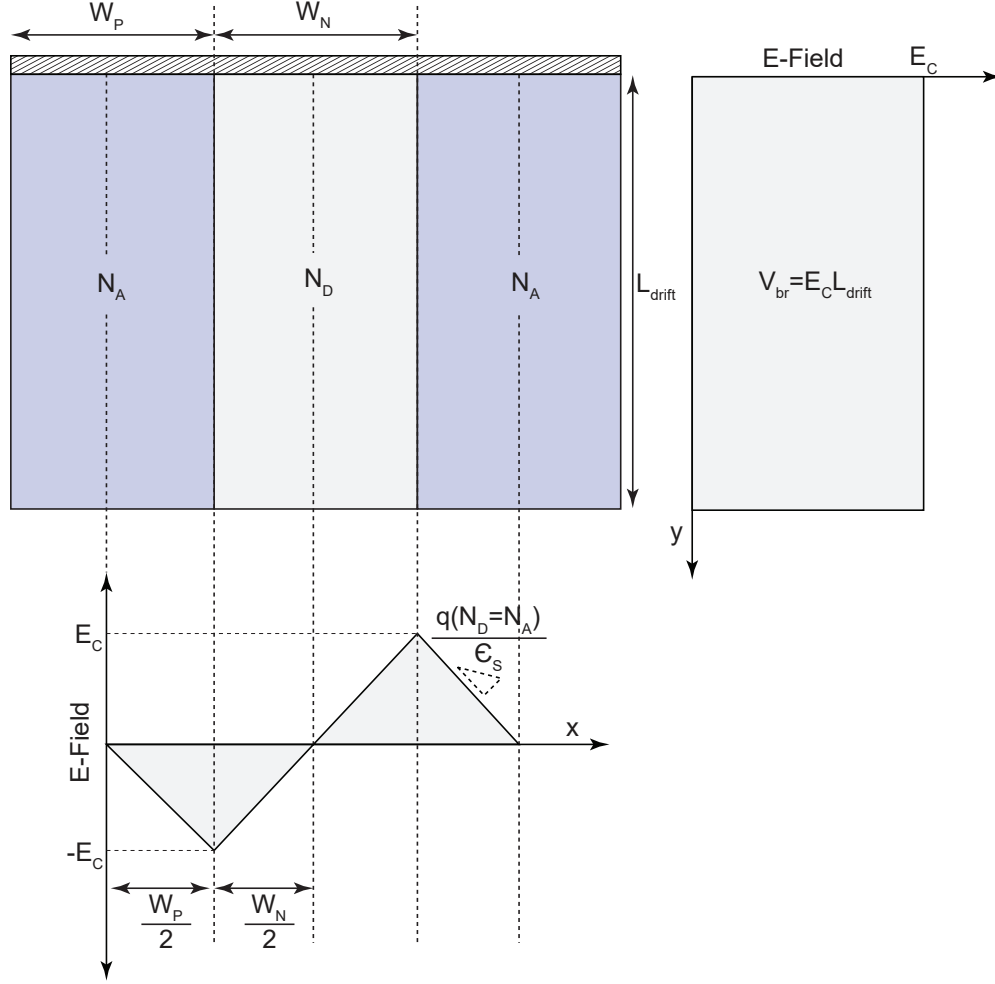


Figure 5.2: Schematic representation of a superjunction SBD showing x and y directional electric field.

5.2.1 Power Figure of Merit of Superjunction Devices

To evaluate the performance benefits of superjunction devices over conventional unipolar devices, the relationship between breakdown voltage (V_{br}) and specific on-resistance (R_{on-sp}) in superjunction devices must be compared to that in traditional unipolar devices. The R_{on-sp} - V_{br} relationship for conventional one dimensional unipolar devices, according to Baliga's Figure of Merit (FOM), is given by:

$$R_{on-sp}^{1D} = \frac{4V_{br}^2}{\epsilon_S \mu_n E_C^3} \quad (5.5)$$

Superjunction devices, however, offer performance benefits only when the charge in the

n-doped region precisely matches that in the p-doped region, i.e., $N_D W_N = N_A W_P$, where N_D is the donor concentration of the n-drift region and N_A is the acceptor concentration of the p-pillar and W_N and W_P are the width of the n- and p- pillars respectively. Under ideal conditions, breakdown occurs when the electric field at the p/n junction reaches the material's critical electric field (E_C). From Fig. 5.2, the electric field at the p/n junction can be expressed as:

$$\frac{qN_D}{\epsilon_S} \left(\frac{W_N}{2} \right) = \frac{qN_A}{\epsilon_S} \left(\frac{W_P}{2} \right) = E_C \quad (5.6)$$

Thus, the optimal charge to achieve the maximum breakdown voltage in superjunction devices is:

$$Q_{optimum} = qN_D W_N = qN_A W_P = 2\epsilon_S E_C \quad (5.7)$$

Equation (5.7) provides the design criterion to select the doping concentration and the widths of the n- and p-pillars in superjunction devices, ensuring that they operate at their highest potential breakdown voltage. Now specific on resistance for the superjunction devices can be written as,

$$R_{on-sp}^{SJ} = \frac{L_{drift}}{q\mu_n N_D} \left(1 + \frac{W_P}{W_N} \right) \quad (5.8)$$

Using the expression of $qN_D W_N$ from (5.6) in (5.8), R_{on-sp}^{SJ} can be written as,

$$R_{on-sp}^{SJ} = \frac{L_{drift}(W_N + W_P)}{2\epsilon_S \mu_n E_C} \quad (5.9)$$

where L_{drift} is the thickness of the n-drift layer. In an ideal charge-balanced structure, the electric field will take on rectangular profile as shown in Fig. 5.2, then the drift layer thickness can be expressed as,

$$L_{drift} = \frac{V_{br}}{E_C} \quad (5.10)$$

Using the expression of L_{drift} from (5.10) in (5.9), R_{on-sp}^{SJ} can be expressed as,

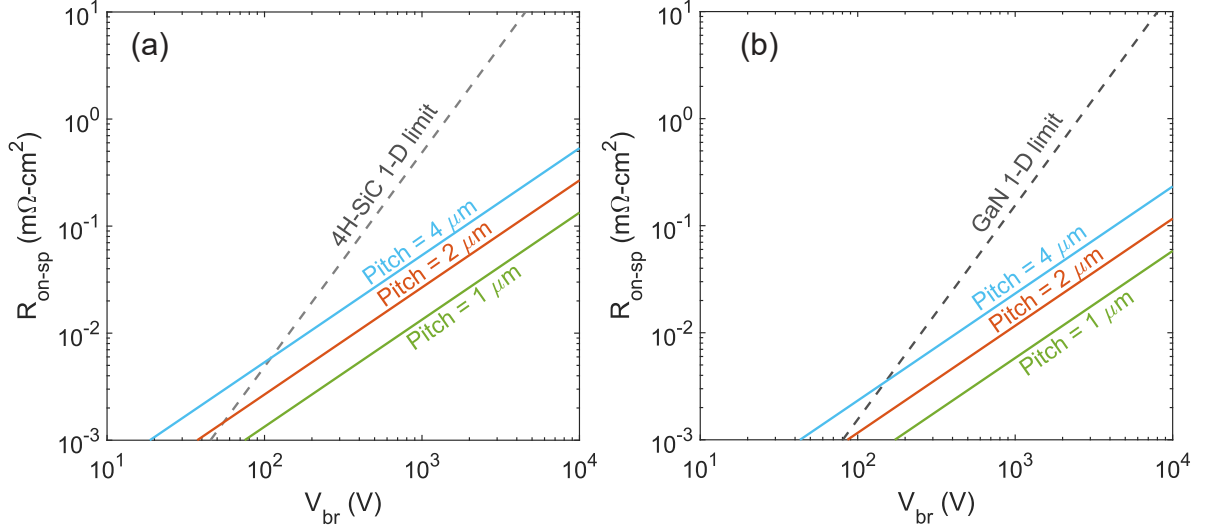


Figure 5.3: Comparison between the 1-D non-punchthrough limit and the superjunction (SJ) limit in the case of (a) 4H-SiC and (b) GaN. The SJ limit is a function of the cell-pitch ($W_N + W_P$).

$$R_{on-sp}^{SJ} = \frac{V_{br}}{2\epsilon_S \mu_n E_C^2} (W_N + W_P) \quad (5.11)$$

Hence a power figure of merit for superjunction devices can be defined as,

$$\text{PFOM}_{SJ} = \frac{V_{br}}{R_{on-sp}^{SJ}} = \frac{2\epsilon_S \mu_n E_C^2}{W_N + W_P} \quad (5.12)$$

The relationship derived in (5.11) reveals that the specific on-resistance (R_{on-sp}) of superjunction devices exhibits a linear dependence on the breakdown voltage (V_{br}), as opposed to the rapid quadratic dependence seen in conventional 1-D unipolar devices. This linear relationship offers a significant performance advantage, particularly for high-voltage applications. Furthermore, unlike the 1-D case, the V_{br} - R_{on-sp} relationship in superjunction devices is influenced by device dimensions, specifically the cell-pitch (i.e., the sum of the widths of the n- and p-pillars, $W_N + W_P$).

A comparative analysis of the V_{br} - R_{on-sp} characteristics for conventional unipolar devices and superjunction devices, for both 4H-SiC and GaN materials, is presented in Fig. 5.3. The data clearly show that the trade-off between R_{on-sp} and V_{br} improves as the cell pitch decreases. This improvement occurs because a reduction in cell pitch necessitates an increase in doping

concentration in the drift region to maintain the same optimum charge balance. The increased doping concentration reduces the resistivity of the drift region, thereby lowering the specific on-resistance (R_{on-sp}). In 2018 however, H.Kang and F.Udera modified the theory and discovered that there is a limitation on cell pitch, below which the specific on-resistance could not be further decreased

This comparison underscores the superior performance of superjunction devices, particularly for high-voltage, low-loss power electronics applications, where minimizing on-resistance without compromising breakdown voltage is critical. The ability to decouple the forward and reverse performance characteristics through optimized cell-pitch design is a key advantage of superjunction technology.

5.2.2 Brief History of Superjunction Devices

The concept of superjunction devices was first introduced in a patent by D.J. Coe [1]. In this design, the inclusion of a p-type region promotes the depletion of the entire drift region, enabling higher breakdown voltages compared to conventional unipolar devices. Over time, the development of superjunction technology branched into two main approaches. The first approach expanded on Coe's original idea by incorporating buried or floating opposite-doped regions within the drift layer [2], [3]. The second approach utilized alternating layers of p- and n-doped regions or multi-RESURF (Reduced Surface Field) superjunction regions as the drift layer [4]–[9]. One of the earliest vertical devices using a superjunction concept was proposed in 1980 [10], leading to the introduction of commercial products such as CoolMOS [5], [8] and MDMESH [11] in the late 1990s.

Although these early works successfully implemented superjunction structures, the term "superjunction" gained widespread recognition when T. Fujihira formally introduced it in 1997 [12]. Fujihira's paper provided a comprehensive review of various superjunction architectures and derived the first generalized equation for their operation. Subsequent research offered variations of this equation, consistently demonstrating a linear or near-linear relationship

between specific on-resistance (R_{on-sp}) and breakdown voltage (V_{br}) [2], [9]. This represented a significant breakthrough, surpassing the quadratic relationship characteristic of conventional unipolar devices, and overcoming the "silicon limit" for power device performance.

The first SiC superjunction (SJ) structure was demonstrated by Kosugi et al. in 2014 using a multi-epitaxial (ME) growth method [13], [14]. This milestone showcased the experimental benefits of SiC SJ structures in enhancing both breakdown voltage (V_{br}) and specific on-resistance (R_{on-sp}). However, these initial SJ structures did not yet represent fully functional devices. In 2017 and 2018, Masuda et al. demonstrated 4H-SiC superjunction V-groove trench MOSFETs with remarkable performance, achieving $0.97 \text{ m}\Omega - \text{cm}^2/820\text{V}$ and $0.63 \text{ m}\Omega - \text{cm}^2/1170\text{V}$, respectively [15], [16].

The implementation of superjunction devices in GaN has proven to be much more challenging compared to Si and SiC, primarily due to the difficulty in achieving effective p-type doping in GaN. Moreover, ion implantation, a common method used for doping in Si and SiC devices, causes significant damage in wide-bandgap semiconductors like GaN. Consequently, researchers have explored alternative concepts such as AlGaIn/GaN "natural superjunction" designs, which leverage polarization effects in GaN and AlGaIn layers. The first such natural superjunction diode was reported by Ishida et al. [17], employing a multi-junction structure. Nakajima et al. [18] later demonstrated a transistor based on the polarization junction concept. In 2013, Li et al. [19] explored the design space for GaN p/n superjunction devices through TCAD simulations, targeting voltage ranges from 5 to 20 kV. In 2023, Qin et al. introduced a charge-balanced lateral Schottky rectifier using p-NiO, achieving a breakdown voltage of 10 kV. Subsequently, Xiao et al. demonstrated the first vertical GaN super heterojunction using p-NiO [20], which was further improved by Ma et al. in 2024 through a self-aligned process, surpassing the GaN 1-D theoretical limit [21].

5.2.3 Challenges Associated with Superjunction Devices

Despite the superior performance of superjunction devices compared to conventional 1-D structures, several practical challenges hinder their widespread adoption in high-voltage power applications. One of the most critical challenges is achieving precise charge balancing between the p- and n-doped layers, which is necessary for surpassing the performance of traditional 1-D devices. Studies have shown that even a 20% charge imbalance can result in a more than 30% reduction in breakdown voltage [22]. Achieving this charge balance is particularly difficult in wide and ultra-wide bandgap semiconductors, due to their material properties and complexities in doping control.

Another significant issue is the lack of avalanche ruggedness in ideal superjunction devices. In theory, superjunction structures require approximately equal doping levels in both the n- and p-regions, but this configuration can lead to critical reliability issues under real-world operating conditions. During avalanche events—often triggered by switching of unclamped load currents—the voltage can rise rapidly, causing the electric field to reach its maximum strength. At this point, electron-hole pair generation occurs, with electrons moving toward the drain and holes toward the source. The presence of these mobile charges alters the net doping profile of the drift region and distorts the electric field. In cases where the electric field is flat, the additional charge from the avalanche process can lower the breakdown voltage, leading to a negative differential breakdown characteristic. This can cause the avalanche current to form a localized filament, which could destroy the device at very low current levels. As a result, superjunction devices may fail catastrophically during avalanche events, posing a serious limitation to their reliability in high-voltage power applications.

Finally, achieving charge balancing using p/n-homojunctions in β -Ga₂O₃ is nearly impossible due to the absence of shallow acceptors. Although p/n homojunctions with deep acceptors theoretically could be field-ionized under high reverse bias, the extremely slow response time of holes in the deep acceptor levels of β -Ga₂O₃ introduces excessive delays, rendering such devices impractical for high-speed switching applications. To address this challenge, several

approaches have explored the use of p-NiO/n- β -Ga₂O₃ super heterojunction diodes, which have shown promising results.

For example, Qin *et al.* demonstrated a charge-balanced lateral p-NiO/n- β -Ga₂O₃ Schottky rectifier with an impressive breakdown voltage of 10 kV [23]. This group later reported a vertical p-NiO/n- β -Ga₂O₃ super heterojunction Schottky rectifier, showcasing dynamic robustness [24]. Despite these advancements, charge balancing remains a significant challenge in superjunction devices based on these materials. One major issue is the difficulty in achieving consistent and repeatable doping concentrations when depositing p-NiO, typically done through sputtering. Furthermore, the low reported hole mobility in p-NiO ($0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) exacerbates the problem, as it introduces delays in hole removal, further limiting the device's performance in high-speed applications.

Thus, while heterojunction approaches provide some relief, the charge balancing issue continues to hinder the full realization of β -Ga₂O₃ superjunction devices for practical use in power electronics. In the next section, an alternative strategy to achieve superjunction-like effects in power devices is discussed. This method eliminates the need for precise charge balancing, which has been a critical obstacle in the realization of superjunction structures, particularly in materials like β -Ga₂O₃. By leveraging device dimensions and electrostatic engineering, these designs aim to retain the benefits of high breakdown voltage and low on-resistance without the complexities associated with doping uniformity and charge compensation. This opens up new pathways for advancing high-performance power devices that are better suited for ultra-wide bandgap materials and their associated challenges.

5.3 Mimicking Superjunction Effects in β -Ga₂O₃ Power Devices: High- κ Dielectric Superjunction

Dielectric polarization charge, induced by an applied electric field, provides an alternative method for charge balancing in superjunction-like devices. When a dielectric is exposed to

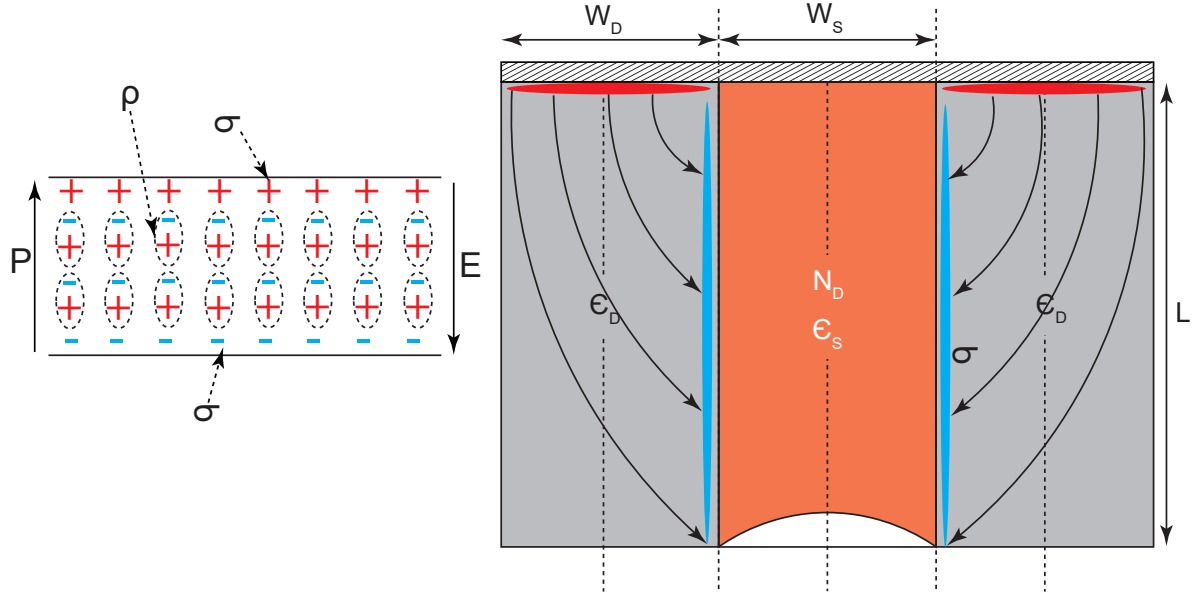


Figure 5.4: (Left) A capacitor with applied potential showing polarization charges and (Right) Schematic representation of dielectric superjunction device showing the depletion of the drift layer due to the induced polarization charges.

an external electric field, the internal dipoles in the material respond to the electric field and polarizes the medium. The polarization P is defined as the dipole moment per unit volume. As a macroscopic quantity, polarization results from averaging the dipole moments over a large enough volume that contains many dipoles. In an isotropic medium, the induced polarization due to an electric field E can be described by the equation:

$$P = \epsilon_0 \chi E \quad (5.13)$$

Here, ϵ_0 is the permittivity of free space, and $\chi = (\epsilon_d - 1)$ is the dielectric susceptibility, where ϵ_d represents the relative permittivity of the dielectric. This polarization generates an effective charge that can be interpreted as a macroscopic bound or polarization charge.

There are two contributions to this bound charge: bulk charge and surface charge. The volume charge density ρ due to the polarization is expressed as:

$$\rho = -\nabla \cdot P \quad (5.14)$$

Meanwhile, the surface charge density σ is given by:

$$\sigma = P = \epsilon_0(\epsilon_d - 1)E \quad (5.15)$$

In isotropic dielectrics with uniform polarization, the average polarization charge within the bulk is effectively zero. This occurs because, on a macroscopic scale, a sufficiently large volume contains equal amounts of positive and negative charges, which cancel each other out, resulting in no net charge. However, at boundaries perpendicular to the direction of polarization, there exists a net surface charge—either positive or negative—due to the uncompensated charges at the dielectric surface, as shown in Fig. 5.4 (a). This surface polarization charge plays a key role in enabling charge balancing, mimicking the effects of a superjunction without the need for precise doping control, which is a major challenge in semiconductor-based approaches. A schematic of the dielectric superjunction structure is presented in Fig. 5.4 (b) where the drift layer is sandwiched between two high-permittivity dielectric [25], [26] layers.

Fig. 5.4 (b) also illustrates how the fringing electric field induces surface polarization charge at the dielectric/semiconductor interface. This, in turn, depletes the channel from the sides in a manner similar to conventional superjunction devices. Importantly, the amount of surface polarization charge generated is highly dependent on the dielectric constant of the material, as described in (5.15). In lower- κ dielectrics, the potential drop increases, which diminishes the strength of the fringing electric field within the dielectric. Consequently, the surface charge at the dielectric/semiconductor interface is reduced, particularly in deeper regions of the structure far from the anode contact, leading to increased charge imbalance.

5.4 Design and Performance Analysis of Dielectric Superjunction Structures

While dielectric superjunctions can offer superior performance compared to conventional 1-D structures, achieving these improvements requires careful design optimization, as the performance is highly sensitive to the dimensions of the structure. In this section, we develop a

simplified analytical model for dielectric superjunction structures by solving Poisson's equation in both the drift layer and the dielectric. The model is validated through comparisons with numerical TCAD simulations.

The motivation behind this work is to provide a clear, intuitive understanding of dielectric superjunction behavior and offer design guidelines that enable optimal configurations. The device's performance is discussed in terms of a modified doping concentration modulated by the dielectric constant of the high-permittivity material and the structural dimensions. Furthermore, we extend our analysis to estimate the switching energy losses in dielectric superjunction Schottky Barrier Diodes (SBDs) and compare them to conventional SBDs. Finally, we provide design guidelines that balance switching losses with conduction loss, optimizing the Power Figure of Merit (PFOM).

5.4.1 Analytical modeling: Static Characteristics

The 2-D Poisson equation of a dielectric superjunction structure with doped n-type semiconductor drift region as shown in Fig. 5.5, can be written as,

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = -\frac{\rho}{\epsilon} \quad (5.16)$$

where,

$$\rho = \begin{cases} qN_D, & x > 0 \\ 0, & x < 0 \end{cases}$$

where, $\psi(x,y)$ is the electrostatic potential, q represents the electron charge, N_D is the ionized donor concentration inside the drift region.

The boundary conditions at top and bottom contacts are considered as,

$$\psi_S(x,0) = 0 \quad (5.17)$$

$$\psi_S(x,L) = V_R \quad (5.18)$$

where V_R is the applied reverse bias voltage. For the dielectric side, the Poisson's equation

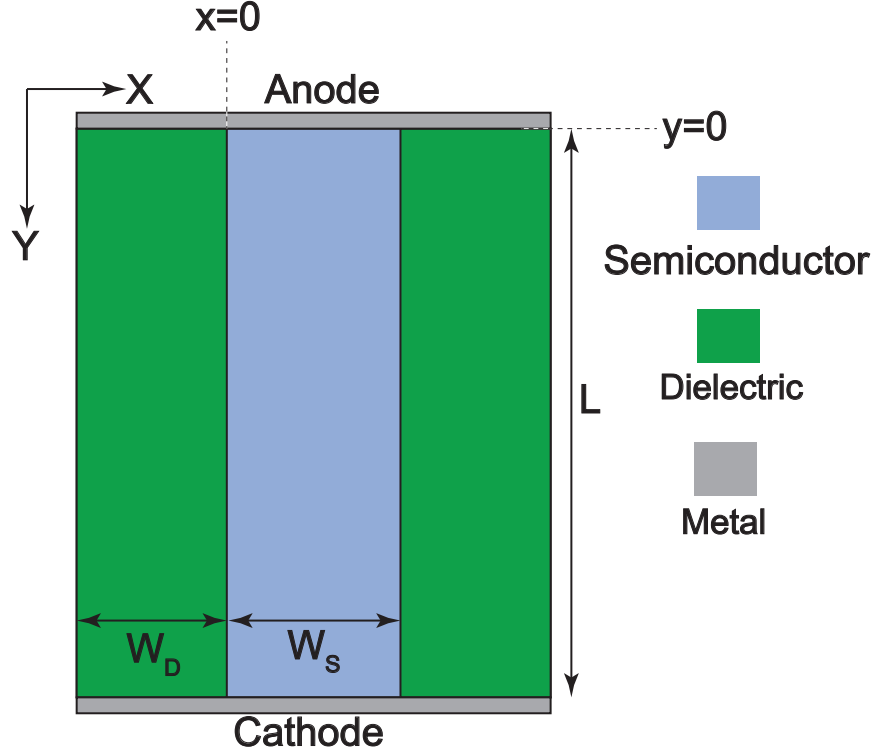


Figure 5.5: Schematic diagram of an ideal vertical dielectric superjunction SBD with co-ordinates used for the analytical modeling.

becomes Laplace's equation due to the absence of charge in the dielectric, which can be solved using the following boundary conditions.

$$\frac{d\psi_D(y=L)}{dy} = 0 \quad (5.19)$$

$$\frac{d\psi_D(x=-W_D/2)}{dx} = 0 \quad (5.20)$$

The first boundary condition (5.19) is derived from the requirement that the electric field at the cathode terminal must be zero. The second boundary condition (5.20) is a consequence of the symmetry of the device around the midpoint of the dielectric. Similarly, the potential boundary conditions for $y=0$ and $y=L$ can be written as,

$$\psi_D(x,0) = 0 \quad (5.21)$$

and,

$$\psi_D(x, L) = V_R \quad (5.22)$$

Solution for the x-directional electric field (E_D) at $x = 0^-$ can be derived using the above mentioned boundary conditions as,

$$\frac{d\psi_D(x=0^-)}{dx} = E_D(x=0^-) = \frac{V_R W_D}{L^2} \quad (5.23)$$

Now in the semiconductor side, Neumann boundary condition of continuity of electric displacement can be applied at the dielectric/semiconductor interface as,

$$\epsilon_S \frac{\partial \psi_S(x=0^+)}{\partial x} \Big|_y = \epsilon_D \frac{\partial \psi_D(x=0^-)}{\partial x} \Big|_y \quad (5.24)$$

or

$$\epsilon_S E_S(x=0^+) \Big|_y = \epsilon_D E_D(x=0^-) \Big|_y \quad (5.25)$$

ϵ_S and ϵ_D are the dielectric constant of the semiconductor and the dielectric and E_S is the electric field in the semiconductor. Now, employing a Taylor series expansion and approximating it to first order, we can express the gradient of the electric field on the semiconductor side as follows,

$$\frac{\partial E_S(x)}{\partial x} \approx \frac{E_S(x=W_S/2) - E_S(x=0^+)}{W_S/2} \quad (5.26)$$

where, $E_S(x=W_S/2) = 0$ due to the symmetry of the device along the semiconductor half-width. Now, using the values of $E_S(x=W_S/2)$ and $E_S(x=0^+)$ from (5.23), (5.25), and (5.26), the gradient of electric field in the x-direction for the semiconductor side from (5.26) can be written as,

$$\frac{\partial E_S(x)}{\partial x} = \frac{2V_R W_D \epsilon_D}{L^2 W_S \epsilon_S} \quad (5.27)$$

Now the 2-D Poisson equation (6.6) for the semiconductor side can be alternatively written as,

$$\frac{\partial E_S(y)}{\partial y} = \frac{qN_D}{\epsilon_s} - \frac{\partial E_S(x)}{\partial x} = \frac{qN_D^{eff}}{\epsilon_s} \quad (5.28)$$

where, N_D^{eff} is the effective doping concentration in the dielectric superjunction SBD. Fig. 5.6(b) presents a comparison between the distribution of the electric field magnitude obtained from the analytical model for β -Ga₂O₃ and the 2D numerical simulation of a dielectric SJ Schottky diode using Sentaurus TCAD [27]. The figure shows that as the dielectric constant of the dielectric material increases, the electric field profile changes from a triangular shape to a rectangular shape for $L/W_S = 10$ and $W_D/W_S = 1$. Although we have considered hypothetical dielectric materials in this study, there are several potential high-k material options available, particularly perovskites that offer high dielectric constants [28]. Some discrepancy between the model and the simulation can be observed, especially near the electrodes. This discrepancy arises due to the absence of lateral depletion effects close to the metal electrodes in the model. This issue could be addressed by introducing a correction factor into the electric field expression [29], [30]. However, for the sake of preserving the model's simplicity and intuitiveness, we have chosen not to incorporate such correction factors. Now integrating (5.28) along y-direction and applying the boundary condition (5.18), we can express V_R as,

$$V_R = \frac{qN_D}{2\epsilon_s} \frac{L^2}{1 + \frac{W_D\epsilon_D}{W_S\epsilon_s}} = \frac{qN_D^{eff}}{2\epsilon_s} L^2 \quad (5.29)$$

Thus, the effective doping concentration (N_D^{eff}) can be expressed as,

$$N_D^{eff} = \frac{N_D}{1 + \frac{W_D\epsilon_D}{W_S\epsilon_s}} \quad (5.30)$$

Therefore, when comparing the dielectric superjunction Schottky Barrier Diode (SBD) to the conventional SBD, the effective doping concentration in the dielectric superjunction SBD is reduced by a factor of $1 + \frac{W_D\epsilon_D}{W_S\epsilon_s}$. Consequently, the breakdown voltage for the dielectric SJ SBD can be derived in a manner similar to the conventional case, with the only difference being the substitution of N_D with N_D^{eff} . Furthermore, in the scenario where $W_D\epsilon_D \gg W_S\epsilon_s$, the dielectric SJ SBD approaches the limits of a conventional p/n superjunction structures.

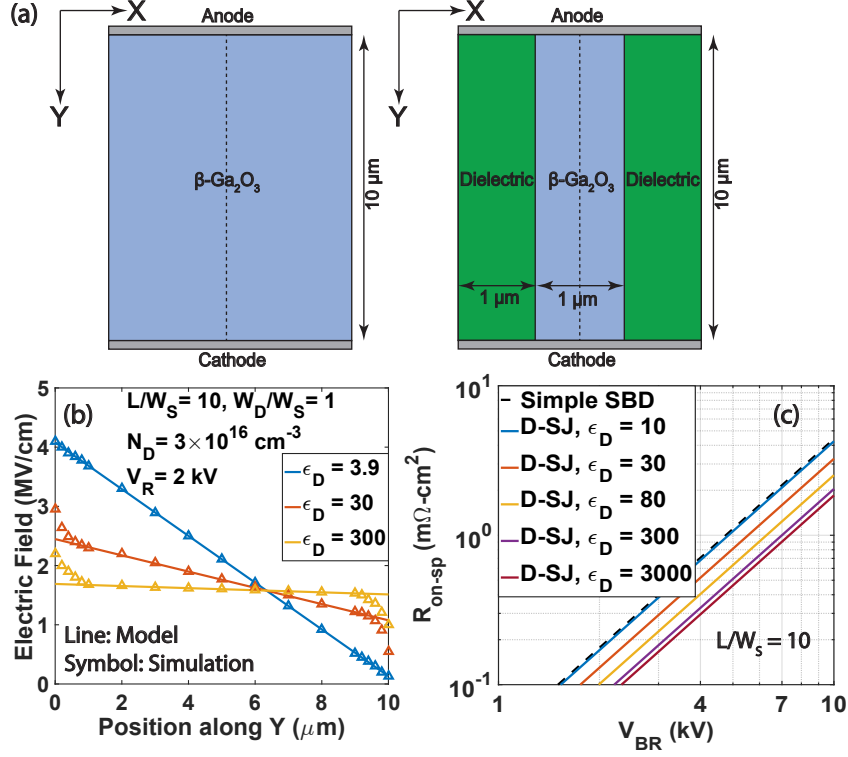


Figure 5.6: (a) Schematic diagram of conventional SBD and dielectric SJ SBD structure showing cutlines for the electric field profiles. (b) Electric field profile inside the dielectric SJ SBD along the cutlines shown for aspect ratio greater than 1. (c) R_{on-sp} vs V_{BR} for the dielectric SJ SBD for different ϵ_D

The breakdown voltage (V_{BR}) for the dielectric SJ SBD can be expressed as,

$$V_{BR} = E_C L - \frac{q N_D^{eff} L^2}{2 \epsilon_S} \quad (5.31)$$

$$= E_C L - \frac{q N_D L^2}{2 \epsilon_S \left(1 + \frac{W_D \epsilon_D}{W_S \epsilon_S} \right)} \quad (5.32)$$

Now the specific on-resistance (R_{on-sp}) for the dielectric SJ SBD considering the entire footprint of the device can be expressed as,

$$R_{on-sp} = \frac{L}{q \mu_n N_D} \left(1 + \frac{W_D}{W_S} \right) \quad (5.33)$$

The optimum doping concentration ($N_{D,opt}$) to achieve the maximum breakdown voltage can be derived by differentiating (5.31) and equating it to zero as,

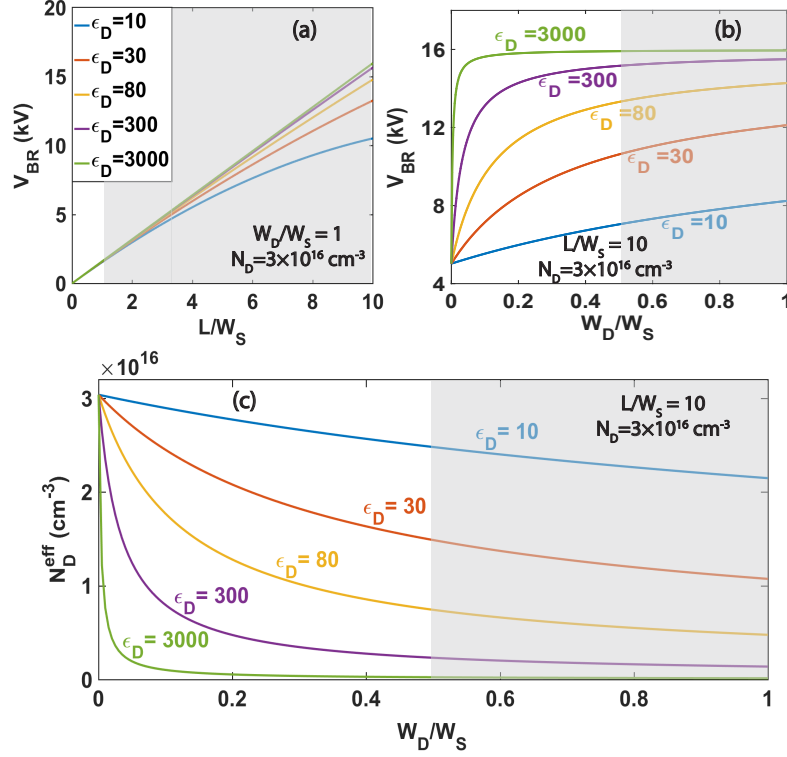


Figure 5.7: (a) Variation of breakdown voltage as a function of aspect ratio (L/W_S) of the device for different ϵ_D . (b) Variation of breakdown voltage as a function of dielectric to semiconductor width ratio (W_D/W_S) for different aspect ratios. (Preferred dimensional ranges for L/W_S and W_D/W_S are shown by the grey shaded region) (c) Effect of the width ratio (W_D/W_S) on the effective doping concentration (N_D^{eff}) for different ϵ_D .

$$N_{D,opt} = \sqrt{\frac{2}{3} \frac{\epsilon_S E_C \left(1 + \frac{W_D}{W_S}\right)}{q^2 \mu R_{on-sp}}} \quad (5.34)$$

5.4.2 Design Guidelines for Static Operations

In Fig. 5.6(c), we illustrate the impact of the dielectric constant of the dielectric column on the trade-off between V_{BR} (breakdown voltage) and R_{on-sp} for $\beta\text{-Ga}_2\text{O}_3$, considering an aspect ratio (L/W_S) of 10 and a width ratio (W_D/W_S) of 1 (The rationale behind selecting these dimensional ratios will be elucidated in the subsequent paragraphs). Notably, as the dielectric constant increases, the V_{BR} - R_{on-sp} trade-off surpasses the unipolar figure of merit for $\beta\text{-Ga}_2\text{O}_3$. However, it's important to highlight that achieving these benefits requires precise and deliberate design considerations compared to conventional unipolar devices.

To gain insights into the impact of device dimensions, we have plotted breakdown voltage against aspect ratio and width ratio in Fig. 5.7 (a) and (b), respectively. Fig. 5.7(a) clearly indicates that achieving an enhancement in breakdown voltage compared to the conventional case is feasible only when the aspect ratio exceeds one ($L/W_S > 1$). Consequently, the length of the device drift layer (L) must surpass the width of the semiconductor column (W_S) to achieve performance beyond the unipolar figure of merit. Moving on to Fig. 5.7(b), we observe that, for a specific aspect ratio, the breakdown voltage increases with an increase in the width ratio (W_D/W_S). However, it's important to note that, as per Equation (5.33), as the width ratio increases, the R_{on-sp} also increases due to a reduction in the current conducting area relative to the total device area. Therefore, it is not advantageous to have a width ratio exceeding 1. Furthermore, Fig. 5.7(b) reveals that the breakdown voltage saturates beyond a width ratio of 0.5 for most of the high-permittivity dielectric. Hence, to minimize R_{on-sp} while achieving an optimal breakdown voltage, it is advisable to maintain the width ratio within the range of 0.5 to 1.

In Fig. 5.7(c), we can observe how the width ratio affects the effective doping concentration (N_D^{eff}) to achieve the optimal trade-off between V_{BR} and R_{on-sp} for a specific aspect ratio and dielectric constant. A minimum N_D^{eff} leads to a constant field profile and hence a minimal N_D^{eff} is desired. Notably, an increase in the dielectric constant of the column leads to a reduction in the effective doping concentration, primarily due to the higher lateral depletion effect. Furthermore, it becomes apparent that for a device with a specific dielectric material, the effective doping concentration ceases to be sensitive to the width ratio (W_D/W_S) when the dielectric constant reaches a sufficiently high value, affording more flexibility in selecting the appropriate widths for the dielectric and semiconductor columns to attain the desired Figure of Merit (FOM).

Using all the design constraints mentioned above, i.e.,

- Constraint 1: $L/W_S > 1$
- Constraint 2: $0.5 \leq W_D/W_S \leq 1$

the design of a 10kV β -Ga₂O₃ SBD is outlined as follows:

Step 1: Begin by specifying the breakdown voltage ($V_{BR}=10$ kV), specific on-resistance ($R_{on-sp} = 2 \text{ m}\Omega - \text{cm}^2$) and the critical breakdown field ($E_C=8$ MV/cm).

Step 2: Select an appropriate dielectric material with a known dielectric constant (Assume $\epsilon_D=300$).

Step 3: If the chosen dielectric material has a lower breakdown field than β -Ga₂O₃, then set $L > V_{BR}/E_{BR-D}$, where E_{BR-D} represents the breakdown field of the dielectric. In this scenario, assume $E_{BR-D} > E_C$, resulting in $L > V_{BR}/E_C = 12.5 \mu\text{m}$.

Step 4: Calculate N_D using equation (5.34) by assuming a width ratio based on constraint 2. Assuming $W_D/W_S = 0.5$, find $N_D = 3 \times 10^{16} \text{ cm}^{-3}$.

Step 4: Determine an appropriate L/W_S using (5.31). In this case $L/W_S = 6.5$. Since $L = 13 \mu\text{m}$, calculate $W_S = 2 \mu\text{m}$.

Step 5: Calculate W_D based on constraint 2. Assuming $W_D/W_S = 0.5$, find $W_D = 1 \mu\text{m}$.

By following the above design approach, considering an ideal case, a power figure of merit (V_{BR}^2/R_{on-sp}) of approximately $50 \text{ GW}/\text{cm}^2$ can be achieved. These dimensions and doping levels are practical and realizable. In contrast, the conventional unipolar figure of merit for β -Ga₂O₃ stands at about $34 \text{ GW}/\text{cm}^2$. This proposed approach can be extended to other wide bandgap materials such as GaN, SiC, and ultra-wide bandgap materials like AlN and Diamond, providing an alternative to pn superjunction structures. This approach allows to avoid the complexities of achieving charge balance in p and n regions in these material systems. This approach can also be a solution in achieving high performance in UWBG semiconductors where only one type of doping is available.

For instance, applying the design rule mentioned above, a 1.2kV dielectric superjunction device for GaN ($E_C = 3 \text{ MV}/\text{cm}$, $\mu_n = 1000 \text{ cm}^2/\text{Vs}$) can be designed using a dielectric material with a dielectric constant of 300. The design parameters would include a drift layer thickness (L) of $33 \mu\text{m}$, semiconductor column width (W_S) of $3.3 \mu\text{m}$, dielectric column width (W_S) of $1.65 \mu\text{m}$, and drift layer doping concentration (N_D) of $4.66 \times 10^{15} \text{ cm}^{-3}$. This designed GaN

high-k superjunction diode would yield a power figure of merit of approximately 17.2 GW/cm^2 , a significant improvement compared to the 5.97 GW/cm^2 unipolar figure of merit for GaN.

5.4.3 Switching Performance

A significant concern when using high-k superjunction SBDs is the potential increase in capacitance due to the high dielectric constant of the dielectric column. This elevated capacitance can lead to higher switching losses, making it crucial to optimize these losses for real device applications. Switching losses can be estimated by considering the total charge that needs to be either removed or added during switching events. For SBDs, we focus solely on capacitive charge storage, as there is no minority carrier storage in these unipolar devices.

Because high-k superjunction SBDs always operate at the punch-through voltage near breakdown, caused by lateral depletion, we can derive the switching losses by considering the parallel combination of the dielectric capacitance and the semiconductor depletion capacitance. Consequently, the total capacitance for the device can be expressed as follows:

$$C_{Total} = C_{Dielectric} + C_{Semiconductor} = \frac{\epsilon_S W_S + \epsilon_D W_D}{L(W_S + W_D)} \quad (5.35)$$

where, $C_{Dielectric}$ and $C_{Semiconductor}$ are the dielectric and semiconductor capacitance respectively. The switching energy for the dielectric superjunction SBD can be written as,

$$\mathcal{E}_{sw-DSJ} = \int_{V_{PT-DSJ}}^{V_{BR}} Q_{Total} v_R dv_R \quad (5.36)$$

Where, Q_{Total} is the total charge in the device and can be written as $C_{Total} \times V_R$. V_{PT-DSJ} is the punch-through voltage for the dielectric superjunction SBD and can be written as,

$$V_{PT-DSJ} = \frac{qN_D}{\epsilon_S} \frac{L^2}{1 + \frac{W_D \epsilon_D}{W_S \epsilon_S}} \quad (5.37)$$

Now, Using (5.35) and (5.37) in (5.36), $\mathcal{E}_{sw-DSJ}$ can be written as,

$$\mathcal{E}_{sw-DSJ} = \frac{\epsilon_S W_S + \epsilon_D W_D}{2L(W_S + W_D)} (V_{BR}^2 - V_{PT-DSJ}^2) \quad (5.38)$$

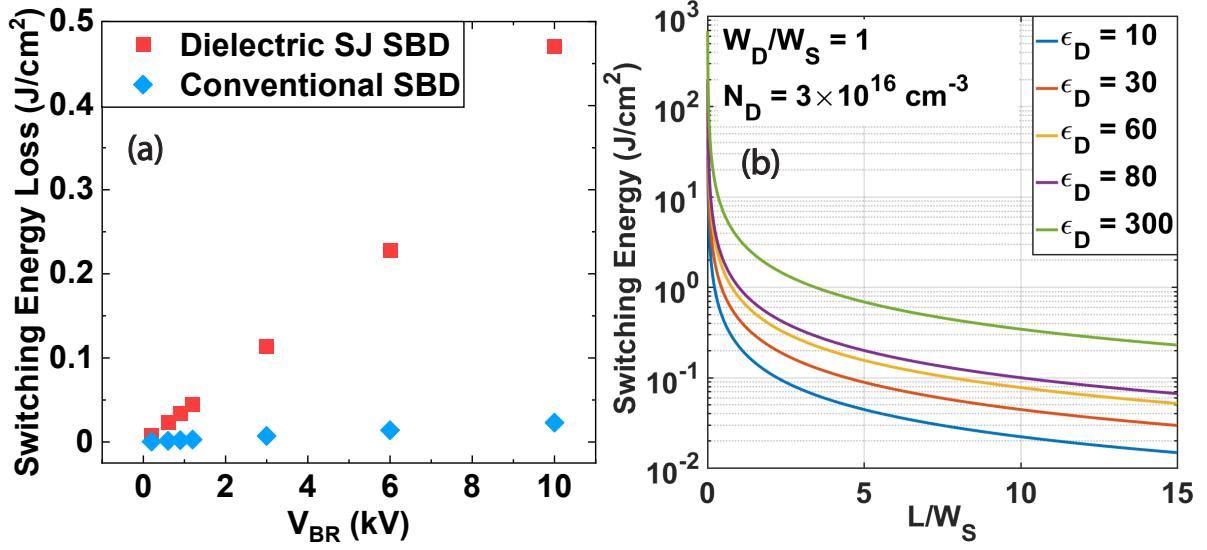


Figure 5.8: (a) Switching energy vs breakdown voltage for dielectric SJ SBDs with $\epsilon_D = 300$, $L/W_S = 10$, and $W_D/W_S = 1$. (b) Variation of switching energy with aspect ratio for different ϵ_D

For conventional SBDs, the switching energy loss after punch-through can be expressed as,

$$\mathcal{E}_{sw-conv} = \frac{\epsilon_S}{L} (V_{BR}^2 - V_{PT-conv}^2) \quad (5.39)$$

And the punch-through voltage ($V_{PT-conv}$) for the conventional SBDs can be written as,

$$V_{PT-conv} = \frac{qN_DL^2}{2\epsilon_S} \quad (5.40)$$

The switching energy for one cycle of full charge and discharge for optimally designed dielectric superjunction SBDs, with breakdown voltage (V_{BR}) ranging from 200V to 10kV and utilizing a dielectric constant of 300 for the dielectric column, is illustrated in Fig. 5.8 (a). It is evident that these dielectric superjunction SBDs exhibit significantly higher switching energy (over 20 times) when compared to conventional SBDs. Therefore, it becomes imperative to redesign the dielectric SJ SBDs to minimize these switching energy losses and trade it off with increased conduction loss, towards a minimized total loss.

In Fig. 5.8 (b), the switching energy is depicted as a function of drift layer length (L) for different dielectric constants (ϵ_D). The results indicate that the switching energy decreases with an increase in drift layer length and a decrease in the dielectric constant of the dielectric column (ϵ_D). This trend is due to the total capacitance of the drift layer and the dielectric

column decreasing with the increase in L and decrease in ϵ_D . However, it's important to note that analytical solutions for a minimum $\mathcal{E}_{sw-DSJ}$ cannot be obtained, as (5.40) is a monotonic function. Consequently, specific values of ϵ_D must be manually selected based on allowable $\mathcal{E}_{sw-DSJ}$ and practical constraints.

To redesign the β -Ga₂O₃ dielectric SJ SBD for a specific power figure of merit and an allowable switching energy, the following design rules can be employed:

Step 1: Begin by specifying the breakdown voltage ($V_{BR}=10kV$), the desired power figure of merit ($50 \text{ GW}/cm^2$), and the acceptable switching energy ($\mathcal{E}_{sw-DSJ} \leq 0.05 \text{ J}/cm^2$).

Step 2: Select a dielectric material with a sufficiently low dielectric constant (ϵ_D) while considering practical dimensions to achieve the desired power figure of merit. From Fig. 4(b), it can be observed that $\epsilon_D=80$ and $L \geq 30 \mu m$ can provide an $\mathcal{E}_{sw-DSJ} \leq 0.05 \text{ J}/cm^2$

Step 3: Calculate the value of R_{on-sp} based on $PFOM = \frac{V_{BR}^2}{R_{on-sp}}$. In this case, $R_{on-sp} = 2 \text{ m}\Omega\text{-cm}^2$.

Step 4: Determine the value of W_S using (5.37). In this case, $W_S = 2 \mu m$ to yield a $\mathcal{E}_{sw-DSJ} = 0.05 \text{ J}/cm^2$.

Step 5: Choose W_D based on constraint 2. Assuming $W_D/W_S = 0.5$, $W_D = 1 \mu m$.

Step 6: Obtain N_D using (5.33) to get desired R_{on-sp} . In this case, $N_D = 9.3 \times 10^{16} \text{ cm}^{-3}$.

Fig. 5.9 presents a plot depicting the relationship between R_{on-sp} and V_{BR} for β -Ga₂O₃ at various switching energies. It becomes evident that as the power figure of merit (PFOM) increases, the switching energy loss for the dielectric SJ SBDs also increases. By adhering to the design guidelines outlined earlier, it becomes feasible to optimally configure dielectric SJ SBDs to achieve a specific power figure of merit within an acceptable range of switching energies. Importantly, these dielectric SJ SBDs will exhibit lower on-state static power losses compared to conventional SBDs with a similar breakdown voltage. This reduction in specific on-resistance is a key advantage of the dielectric superjunction SBD design, contributing to its overall efficiency.

In summary, it is feasible to design practical dielectric superjunction Schottky Barrier Diodes

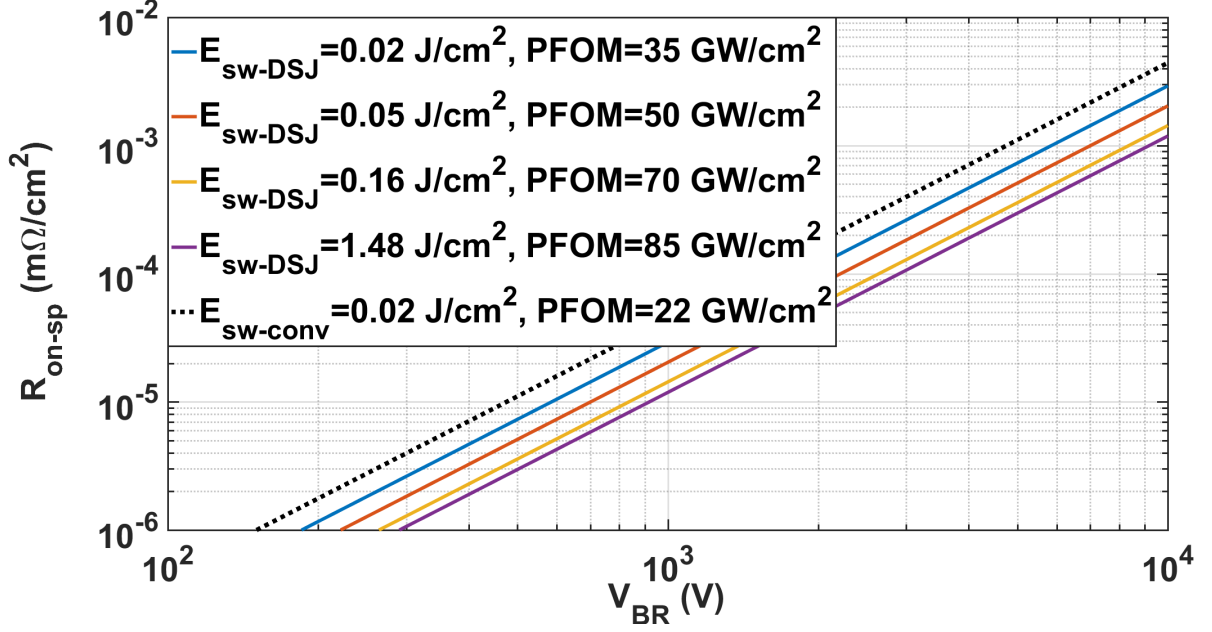


Figure 5.9: R_{on-sp} vs V_{BR} plot for different switching energy losses showing the dependence of E_{sw} on PFOM (SBDs) using β -Ga₂O₃ that deliver exceptionally high power figures of merit (PFOM). Critical design parameters, such as the aspect ratio and the semiconductor-to-dielectric width ratio, have proven to be pivotal in determining device performance. A high aspect ratio is particularly important; if the aspect ratio falls below one, the advantages of dielectric superjunction SBDs diminish compared to conventional SBDs. While dielectric superjunction SBDs offer superior PFOM over their conventional counterparts, they tend to exhibit higher switching energy losses due to increased capacitive charge storage. However, with careful design optimization, these losses can be minimized, maximizing the overall PFOM.

This design approach can also be extended beyond β -Ga₂O₃ to other wide and ultra-wide bandgap materials, providing a promising alternative to traditional pn superjunction devices, which often pose fabrication challenges. In the next section, a demonstration of a β -Ga₂O₃-based high- κ dielectric superjunction Schottky rectifier using BaTiO₃ in a lateral geometry is presented.

5.5 β -Ga₂O₃ Lateral High-Permittivity Dielectric Superjunction Schottky Barrier Diode

The realization of a vertical dielectric superjunction structure presents several fabrication challenges. Achieving a high aspect ratio requires either deep etching of β -Ga₂O₃ or high-resolution lithography for shallower structures. Furthermore, the process of void-free gap-filling in the etched trenches with high- κ dielectric is critical, as any voids can significantly reduce the breakdown voltage and compromise the device's reliability. To demonstrate dielectric superjunction action while avoiding these fabrication complexities, a lateral geometry has been employed, as illustrated in Fig. 5.10(a).

In this lateral structure, trenches are used to surround the drift layer on three sides with high- κ dielectric, facilitating enhanced depletion of charge from the drift region and resulting in a higher breakdown voltage compared to conventional planar SBDs. A cross-sectional view along the C-D cutline of Fig. 5.10(a) closely resembles that of a vertical structure, as depicted in Fig. 5.10(c). The evolution of the space charge region within the β -Ga₂O₃ drift layer for the lateral dielectric superjunction SBD is shown in Fig. 5.10(d). This design enables the incorporation of a higher charge density without compromising the breakdown voltage, which also leads to a lower on-resistance.

The device demonstrated an impressive breakdown voltage of 1487 V, coupled with a low specific on-resistance (R_{on-sp}) of 1.65 m Ω -cm² for a dielectric superjunction SBD with an anode-to-cathode distance of 5 μ m, resulting in a power figure of merit (PFOM) of 1.34 GW/cm².

5.5.1 Device Fabrication

The fabrication steps of the lateral dielectric SJ SBDs are illustrated in Fig. 5.11 Lateral trench SJ SBDs as shown in Fig. 5.10(a) were fabricated on a $\sim$ 500 nm thick β -Ga₂O₃ epitaxial layer on Fe doped (010) oriented substrate. After the standard solvent cleaning (Acetone/Methanol/DI

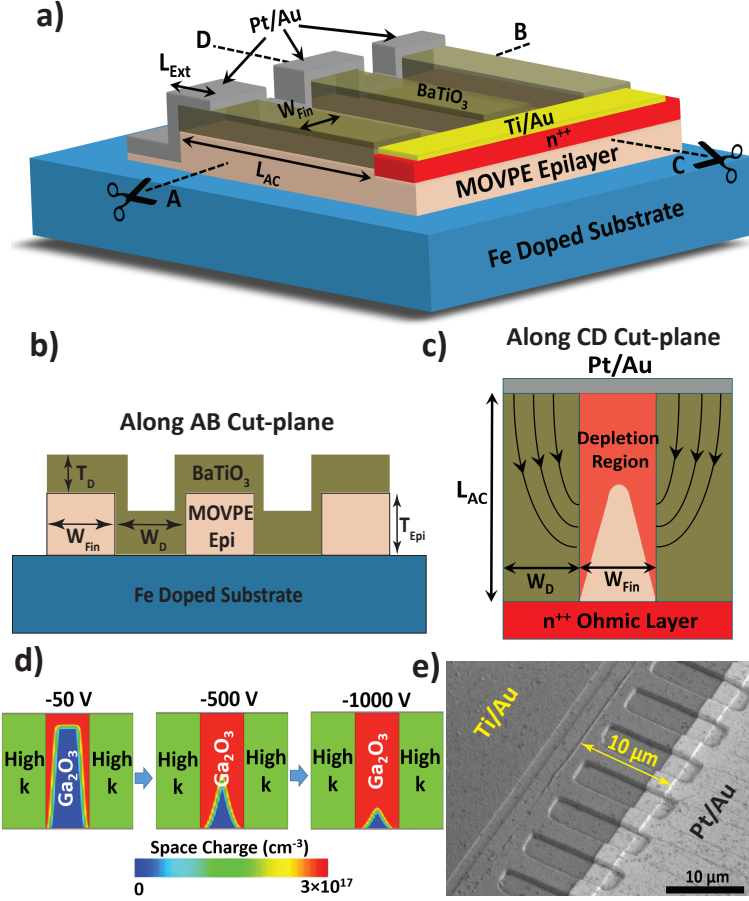


Figure 5.10: (a) 3D schematic of the Ga₂O₃ lateral trench SBD with high-k dielectric superjunction. (b) Cut-plane along AB of Fig. 1(a) showing different layers. (c) Cut-plane along CD of Fig. 1(a) showing the depletion of the drift layer due to fringing electric field. (d) Representative simulation of dielectric SJ structure showing the evolution of the depletion region with applied reverse bias in the drift layer. (e) Top view scanning electron microscope (SEM) image of the lateral trench SBD with high-k superjunction. Reprinted from Roy *et al.* [31] © 2022 IEEE.

water), the substrate was treated with HF followed by DI water. The growth of epilayer was performed in an Agnition MOVPE reactor using Triethyl-Gallium (TEGa), O₂ and Silane (SiH₄) as precursors and Argon as carrier gas [32]–[34]. Hall measurements were performed on the samples and room temperature channel charge and mobility was extracted to be $1.5 \times 10^{13} \text{ cm}^{-2}$ ($\sim 3 \times 10^{17} \text{ cm}^{-3}$) and $135 \text{ cm}^2 \text{V}^{-1} \text{sec}^{-1}$ respectively.

After the growth of the epilayer, 500 nm deep rectangular trenches of different lengths and widths were patterned using photolithography followed by BCl₃ based Inductively coupled plasma (ICP) reactive ion etching (RIE) with an etch rate of $\sim 12 \text{ nm/min}$. After the trench definition, ohmic contact recess etching was performed using BCl₃ based ICP RIE and n⁺ ohmic

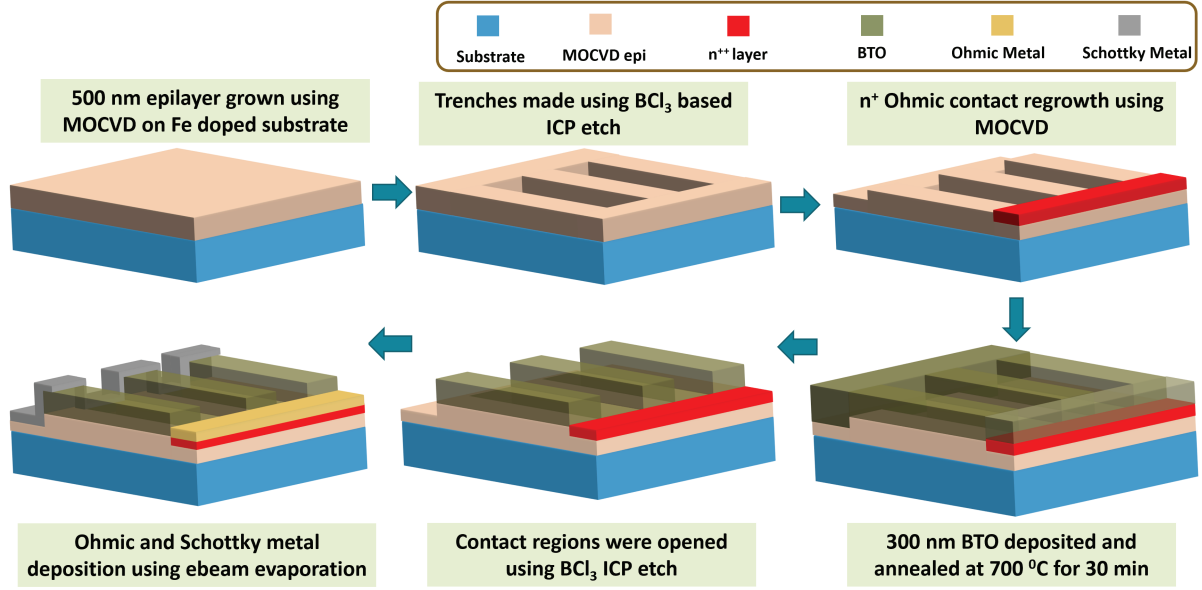


Figure 5.11: Fabrication process steps of lateral high- κ dielectric superjunction Schottky barrier diodes.

contact with doping concentration of approximately $1.4 \times 10^{20} \text{ cm}^{-3}$ was then regrown using MOVPE [35], [36] using a SiO_2 regrowth mask. 300 nm thick BaTiO_3 was then deposited on the sample using RF sputtering at room temperature in oxygen ambient with O_2/Ar ratio of 1:10 and at a sputter power of 140 W and chamber pressure of 5mTorr [37]. After the dielectric deposition, the samples were annealed at 700°C in oxygen ambient for 30 minutes to enhance the dielectric constant. Following the dielectric deposition and annealing, the ohmic and schottky contact regions were opened up using BCl_3/Ar based ICP RIE. Finally ohmic (Ti/Au) was deposited on the regrown n^+ contact regions using electron beam evaporation (annealed at 470°C for 1 min) followed by schottky (Pt/Au) metal deposition on the sidewall of the trenches. Using capacitance voltage characteristics, the dielectric constant of the BaTiO_3 layer was extracted to be ~ 220 using MOSCAP structures. A top view SEM image of the fabricated device is shown in Fig. 5.10(e).

5.5.2 Forward and Reverse Current-Voltage Characteristics

The typical current voltage plots in log and linear scale for the high-k SJ SBDs are shown in Fig. 5.12(a) and 5.12(b) respectively. The normalization is done by considering the entire device

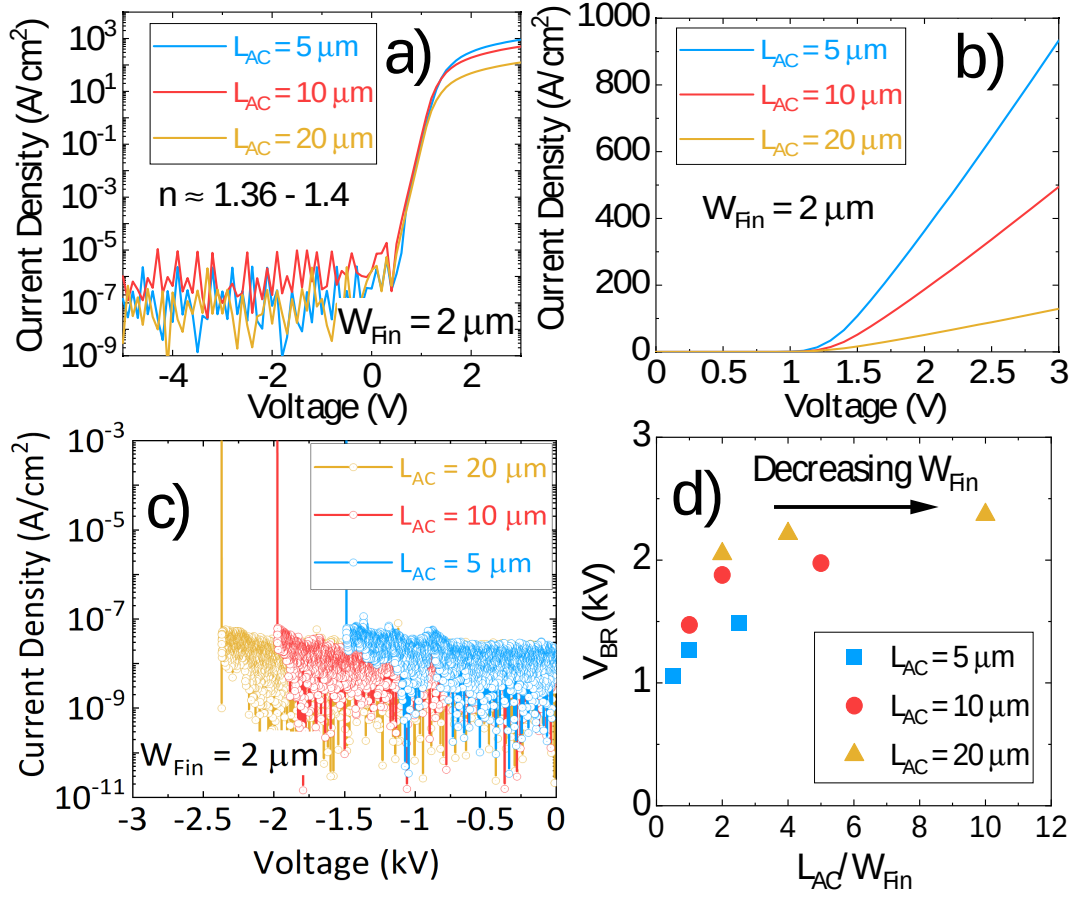


Figure 5.12: (a) Log scale, & (b) linear scale IV characteristics of the high-k SJ SBD with $L_{AC}/W_{Fin} = 5 \mu\text{m}/2 \mu\text{m}$, $10 \mu\text{m}/2 \mu\text{m}$, and $20 \mu\text{m}/2 \mu\text{m}$ (c) Breakdown characteristics of the SJ SBDs with the three different L_{AC}/W_{Fin} , and (d) Variation of V_{BR} with aspect ratio (L_{AC}/W_{Fin}) for the high-k SJ SBDs. Reprinted from Roy *et al.* [31] © 2022 IEEE.

width ($N_{Fin}(W_{Fin} + W_D)$), where W_{Fin} and W_D are the $\beta\text{-Ga}_2\text{O}_3$ fin width and high-k dielectric width respectively as shown in Fig. 1 and N_{Fin} is the number of fins. The moderately high ideality factor (n) of ~ 1.3 - 1.4 is probably due to the sidewall etching damage, which can be improved using sidewall treatment [38]. Schottky barrier height of ~ 1.4 eV is extracted from both IV and CV characteristics for all the SJ SBDs. The R_{on-sp} for the high-k SJ structures are extracted to be 1.65, 4.72, and 17.8 $\text{m}\Omega\text{-cm}^2$ for L_{AC}/W_{Fin} of $5 \mu\text{m}/2 \mu\text{m}$, $10 \mu\text{m}/2 \mu\text{m}$, and $20 \mu\text{m}/2 \mu\text{m}$ respectively.

The reverse IV characteristics for the high-k SJ SBDs for three different L_{AC} are shown in Fig. 5.12(c). The devices were measured while submerged in FC-40 Fluorinert dielectric liquid using B1505A parameter analyzer. Catastrophic breakdown voltages of 1487 V, 1972

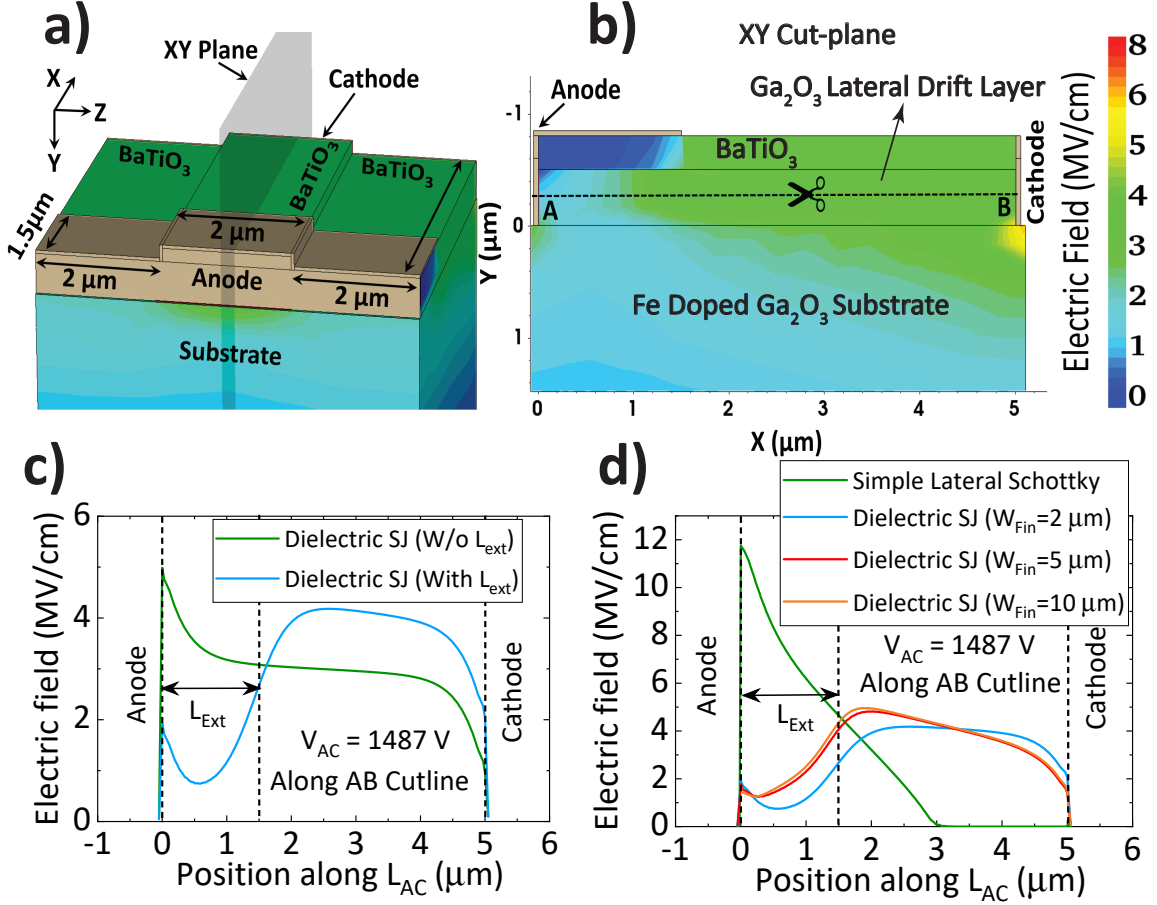


Figure 5.13: (a) 3D TCAD electric field simulation for the high-k lateral SJ SBD at and applied voltage of -1487V, (b) simulated electric field contour plot along the XY cut-plane of Fig. 3(a). Simulated electric field profile for the high-k SBDs (c) with and without L_{Ext} and (d) with different W_{Fin} for cut-lines along the lateral direction (A-B). Reprinted from Roy *et al.* [31] © 2022 IEEE.

V, and 2359 V were observed for the SJ SBDs with $L_{AC}/W_{Fin} = 5\mu\text{m}/2\mu\text{m}$, $10\mu\text{m}/2\mu\text{m}$, and $20\mu\text{m}/2\mu\text{m}$ respectively. The low leakage current at high reverse bias is due to the RESURF effect by the anode extension length (L_{ext}) which reduces the electric field at the schottky metal/semiconductor interface. It can be seen in Fig. 5.12(d) that as the aspect ratio (L_{AC}/W_{Fin}) increases for SBDs with same L_{AC} , the breakdown voltage also increases. Thus, proper device dimensions need to be maintained to achieve optimum performance for the SJ SBDs [39].

5.5.3 Electric Field Simulation and Benchmarking

The three-dimensional electric field simulations at an applied reverse bias (V_R) of -1487V for the high-k dielectric SJ SBD structures are also performed using Sentaurus TCAD software and

results for the $L_{AC} = 5 \mu\text{m}$ and $W_{Fin} = 2 \mu\text{m}$ are plotted in Fig. 5.13(a),(b). In Fig. 5.13(c), electric fields are plotted for the dielectric SJ SBD with and without the anode extension length (L_{ext}). It can be seen that the electric field at the Schottky contact exceeds 4 MV/cm at the breakdown voltage without L_{ext} , which would result in a significant amount of reverse leakage current. Due to the anode extension, the electric field at the schottky metal/semiconductor interface reduces to less than 2 MV/cm, which results in significantly less leakage currents as shown in Fig. 5.12(c). In Fig. 5.13(d), electric fields are plotted along the length of the diode for three different aspect ratios and for a planar lateral SBD. It can be seen that the high-k SJ SBDs have rectangular field profile and the planar regular SBD has triangular field profile. This is due to the fact that, in the SJ SBDs, the fringing electric field through the high-k dielectric depletes the lateral drift layer from the sides whereas for planar regular SBD, the depletion happens only due to the parallel anode surface electric field. Due to the anode extensions, the electric field at the anode interface is also significantly lower than the bulk, which reduces the leakage current in reverse bias [40]. It can also be seen that, for SBD with aspect ratio greater than 1, the electric field profile along L_{AC} is more uniform compared to the SBDs with aspect ratio less than 1. Hence, SBD with higher L_{AC}/W_{Fin} can block larger voltage compared to the SBDs with smaller L_{AC}/W_{Fin} . The average electric field for the SBD with $L_{AC}/W_{Fin} = 5/2 \mu\text{m}$ is about ~ 4 MV/cm at $V_R = -1487\text{V}$ and electric field at point A of Fig 5.13(c) is ~ 2 MV/cm.

A benchmark plot of R_{on-sp} vs V_{br} for state of the art $\beta\text{-Ga}_2\text{O}_3$ based vertical and lateral SBDs from literature are shown in fig. 5.14. The high-k SJ SBD with $L_{AC}/W_{Fin} = 5\mu\text{m}/2\mu\text{m}$ with an R_{on-sp} of $1.65 \text{ m}\Omega\text{-cm}^2$ and breakdown voltage of -1487V has a power figure of merit (V_{BR}/R_{on-sp}) of 1.34 GW/cm^2 which is the highest among all lateral $\beta\text{-Ga}_2\text{O}_3$ SBDs. The PFOM of 10 and 20 μm devices are 824 MW/cm^2 and 312 MW/cm^2 respectively. We hypothesize that the reduction in PFOM for larger L_{AC} could be due to non-ideal effects such as etched fin sidewall related damage and fixed charge at the high-k/ Ga_2O_3 interfaces. The use of dielectric superjunction structures also enables the implementation of heavily doped epilayer to achieve low R_{on-sp} while simultaneously supporting high blocking voltage. It should be

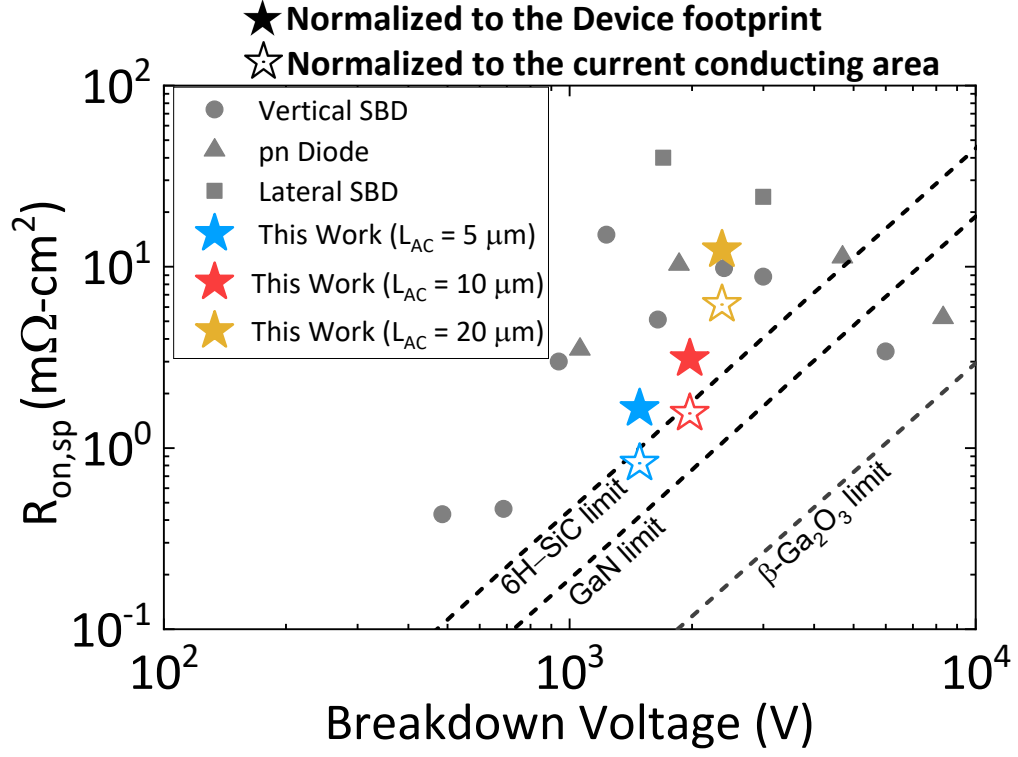


Figure 5.14: Benchmark plot for R_{on-sp} vs V_{br} comparing our devices with other reported state-of-the-art vertical and lateral diodes.

noted that the R_{on-sp} was calculated by normalizing to the entire device footprint. If only the current conducting regions are considered in normalization, the resulting PFOM would be ~ 2.7 GW/cm², which crosses the SiC unipolar figure of merit.

The demonstrated device is the first report of a high-k lateral trench SJ Schottky barrier diode implemented in β -Ga₂O₃. Due to the difficulty in implementing conventional pn-superjunction structures, the proposed device architecture can be extended to other WBG and UWBG materials to push the device performance towards their material limit or potentially beyond their unipolar FOM. The lack of requirement of charge balancing as needed in superjunction devices makes the design and fabrication of high-k SJ device less taxing. In the ideal case, such structures should provide performance benefit beyond a material's unipolar figure of merit. Non-idealities such as sidewall etching damage can be minimized by performing wet treatments [38] after dry etching, which will improve the performance of such devices.

5.6 Summary

This chapter provides comprehensive design guidelines aimed at surpassing the unipolar power figure of merit (PFOM) of wide and ultra-wide bandgap materials through the innovative use of dielectric superjunction Schottky Barrier Diodes (SBDs). The integration of a dielectric superjunction addresses a fundamental challenge inherent to gallium oxide technology—the limitation imposed by the absence of viable p-type doping. This challenge has historically constrained the performance and application range of β -Ga₂O₃ devices. By implementing a dielectric superjunction, we can effectively manipulate the electric field profile within the drift region of the diode. This manipulation leads to the formation of a rectangular electric field distribution, significantly enhancing the breakdown voltage (V_{BR}).

Through meticulous optimization of the device structure, it is feasible to extend the already impressive V_{BR} - R_{on-sp} trade-off of β -Ga₂O₃ beyond its conventional unipolar limits. This optimization is critical for applications demanding high voltage and low resistance, thus making β -Ga₂O₃ a compelling candidate for future power electronics.

While initial observations indicate that the switching energy losses in these devices are somewhat elevated compared to traditional SBDs, it is essential to recognize that with rigorous design optimization, these energy losses can be effectively minimized. This optimization ensures that the desired PFOM is not only achievable but also sustainable in practical applications. The significant advantages presented by this innovative device architecture—such as improved voltage handling and efficiency—clearly outweigh the relatively minor drawbacks associated with increased switching energy losses. Furthermore, it is important to highlight that ongoing research into the high- k dielectric/ β -Ga₂O₃ interface is crucial for fully realizing the potential of superjunction structures.

In addition to these theoretical advancements, we have successfully demonstrated a novel β -Ga₂O₃ lateral trench Schottky barrier diode featuring a high- k dielectric superjunction structure, serving as a proof of concept for the proposed design strategies. This device has achieved a remarkably low specific on-resistance of 1.65 m Ω -cm² through the strategic growth

of an epilayer characterized by a higher sheet charge density. The superjunction effect plays a pivotal role in reducing the electric field within the lateral drift region by effectively distributing the depletion region across the entire length of the diode. As a result of this design innovation, the diode exhibits an impressive breakdown voltage of -1487 V, which makes this architecture particularly attractive for low to medium-voltage applications, where minimizing conduction losses is critical for overall efficiency.

Moreover, this device has achieved a record figure of merit of 1.34 GW/cm^2 among all $\beta\text{-Ga}_2\text{O}_3$ -based lateral SBDs, highlighting the significant progress and potential of this first-generation demonstration of superjunction devices. This achievement underscores the capability of the proposed design to set new benchmarks in power electronics, reinforcing the notion that dielectric superjunction SBDs represent a transformative step forward in the pursuit of high-performance, energy-efficient power devices.

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Chapter 6

In-situ Dielectric on β -Ga₂O₃ using Metal-Organic Chemical Vapor Deposition

6.1 Introduction

The emergence of β -Ga₂O₃ as a leading material for power electronics, due to its exceptionally high breakdown field (8 MV/cm) and superior Baliga's figure of merit (BFOM), has prompted significant research into identifying suitable insulator materials for gate dielectrics in device applications. For transistors, an ideal gate dielectric must exhibit low leakage current, minimal interface trap densities to ensure a stable threshold voltage (V_T), and a breakdown field higher than that of the underlying semiconductor. Several dielectric materials, including SiO₂ [1]–[4], Al₂O₃ [5], [6], SiN [7], and HfO₂ [7], [8], have been extensively studied as gate oxides and passivation layers for Ga₂O₃ devices. Additionally, high-permittivity materials like Barium Titanate (BaTiO₃) have been explored for use in β -Ga₂O₃ transistors and heterojunction Schottky barrier diodes [9]–[11]. Furthermore, complex oxides such as the ternary rare-earth alloy (Y_{0.6}Sc_{0.4})₂O₃ have been investigated as gate dielectrics for β -Ga₂O₃ MOS structures by Masten *et al.* [12].

Among these options, Al₂O₃ has emerged as the most extensively researched and widely

adopted dielectric for β -Ga₂O₃ devices due to its compatibility with the semiconductor. Chabak *et al.* demonstrated lateral MOSFETs utilizing Al₂O₃ as the gate dielectric, achieving remarkable field strength [13]–[15]. Similarly, Li *et al.* developed vertical FinFET structures based on β -Ga₂O₃, achieving exceptional figures of merit (FOM) with Al₂O₃ as the gate dielectric [16]–[18]. Jian *et al.* also examined the impact of post-deposition annealing on interface trap density in ALD-grown Al₂O₃ on (001) β -Ga₂O₃ [19].

Most studies have employed ex-situ deposition techniques, such as atomic layer deposition (ALD), where the Ga₂O₃ substrate or epilayer is transferred to a different reactor for dielectric deposition. However, during this transfer, complete removal of interface contamination is challenging. In contrast, in-situ deposition of Al₂O₃ within the same reactor preserves the pristine surface of Ga₂O₃, preventing exposure to ambient contamination. Moreover, in-situ deposition via metal-organic chemical vapor deposition (MOCVD) at higher growth temperatures (500–1000°C) enhances dielectric and interface quality compared to lower-temperature ALD (100–300°C). MOCVD also offers significantly higher deposition rates and allows for high-temperature in-situ annealing, which can further reduce interface state densities and improve bulk dielectric quality. The in-situ growth of Al₂O₃ on both Ga-face and N-face GaN using MOCVD has been extensively studied [20]–[24]. In this chapter, the in-situ growth of Al₂O₃ using MOCVD, as well as the electrical characterization of metal/in-situ Al₂O₃/ β -Ga₂O₃ vertical MOS capacitors (MOSCAPs) is presented.

6.2 600 °C Insitu-Dielectric Growth and Characterization

6.2.1 Dielectric Growth and Structural Characterization

The growth of the in-situ Al₂O₃ layer, following the epitaxial deposition of a 500 nm β -Ga₂O₃ layer on Sn-doped (010) β -Ga₂O₃ substrates (NCT Japan), and the subsequent fabrication of metal-oxide-semiconductor capacitors (MOSCAPs), as shown in Figure 6.1(a), began with substrate preparation. The substrates were cleaned using acetone, methanol, and deionized

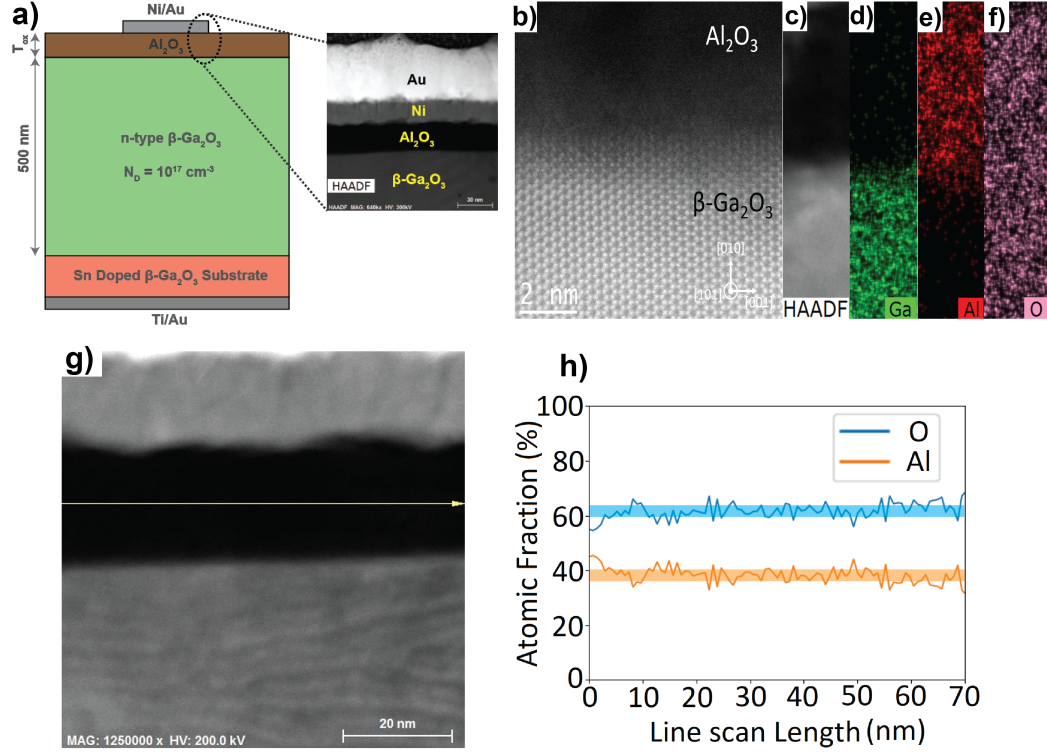


Figure 6.1: (a) Schematic diagram of the fabricated MOSCAP structures and the cross-sectional TEM image of the expanded region showing different layers. (b) High-resolution HAADF-STEM image of the Al₂O₃/β-Ga₂O₃ in the [101] direction. (c) low magnification HAADF-STEM image of the same region with its corresponding EDS maps of (d) Ga, (e) Al, and (f) O. (g) HAADF-STEM image of the Al₂O₃/β-Ga₂O₃ interface within the direction of the EDS line scan indicated by the yellow arrow. (h) Atomic fraction extracted from the EDS line scan. Horizontal orange and blue full lines are plotted at 38% and 62% respectively and their widths are equal to 4% which corresponds absolute value of the $\pm 2\%$ errors of the XEDS quantitative analysis. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

water, followed by a 15-minute dip in HF solution. The epitaxial growth was performed using an Agnitron metal-organic vapor-phase epitaxy (MOVPE) reactor equipped with a far-injection showerhead design. Triethylgallium (TEGa) and O₂ served as precursors, while argon was used as the carrier gas, and diluted silane acted as the dopant source. Growth was conducted at 600 °C under a chamber pressure of 60 Torr, consistent with previously reported low-temperature growth processes for β-Ga₂O₃ [26], [27].

The gas flow rates for TEGa and O₂ were set at 65 and 800 sccm, respectively, with an argon flow rate of 1100 sccm. A silane flow rate of 0.06 nmol/min was maintained to achieve a silicon doping concentration of approximately 10¹⁷ cm⁻³. After the β-Ga₂O₃ growth, a 30-second purge was employed to remove unreacted precursors from the reactor. During this step, the

reactor pressure was lowered from 60 Torr to 15 Torr while maintaining the temperature at 600 °C, and the O₂ flow rate was reduced from 800 to 500 sccm.

The in-situ growth of the Al₂O₃ dielectric layer followed, with growth times varied to achieve thicknesses of 14, 24, and 55 nm on three different substrates. The Al₂O₃ was grown at a rate of 1.2 nm/min using trimethylaluminum (TMAI) as the precursor, with a flow rate of 5.33 μ mol/min and an O₂ flow rate of 500 sccm. The dielectric thickness was measured by etching the Al₂O₃ layer using buffered oxide etch (BOE) after photolithography patterning, with the etch depth confirmed by atomic force microscopy, as detailed in the supporting information.

Following Al₂O₃ deposition, ohmic Ti (50 nm)/Au (100 nm) contacts were sputtered on the backside of the MOSCAPs. Circular Ni (10 nm)/Au (50 nm) gate contacts were patterned on the Al₂O₃ surface using standard photolithography and deposited via E-beam evaporation.

The MOSCAPs were fabricated to assess the interface quality between the in-situ Al₂O₃ and β -Ga₂O₃. To evaluate the abruptness of the Al₂O₃/ β -Ga₂O₃ interface and verify the stoichiometry of the Al₂O₃ layer, a combination of scanning transmission electron microscopy (STEM) using a high-angle annular dark field detector (HAADF-STEM) and energy-dispersive X-ray spectroscopy (EDS) was employed. Cross-sectional samples of the interface were prepared using a focused ion beam (FEI Helios 660).

The HAADF-STEM imaging was carried out on a FEI Titan G2 60-300 STEM with an acceleration voltage of 300 kV, a condenser lens aperture of 70 μ m, and a probe current of approximately 100 pA. Figure 6.1(b) presents a HAADF-STEM image of the Al₂O₃/ β -Ga₂O₃ interface along the [101] crystallographic direction. The β -Ga₂O₃ substrate appears brighter than the Al₂O₃ film due to the higher atomic number of Ga compared to Al. The interface is observed to be abrupt, with a transition region of about 2 nm, where the contrast from Ga atoms diminishes, and the high-resolution imaging degrades.

The sharpness of the Al₂O₃/ β -Ga₂O₃ interface was further corroborated by EDS mapping (using a Bruker system) performed on the same region. Figure 6.1(c) shows a HAADF-STEM image of the interface alongside the corresponding EDS elemental maps for (d) Ga, (e) Al, and

(f) O. A smooth transition between the two materials is visible, with minimal diffusion of Al atoms into the top of the β -Ga₂O₃ epilayer.

Additionally, the composition of the Al₂O₃ film was determined using the Cliff-Lorimer ratio technique from the EDS mapping analysis, as outlined in the supporting information [28]. The results show that the film has a uniform composition of $38 \pm 2\%$ Al and $62 \pm 2\%$ O, maintaining homogeneity throughout the Al₂O₃ layer, as evidenced by the EDS linescan in Figure 6.1(h).

6.2.2 Characterization of Trap Densities

To characterize the trap densities, the fabricated MOSCAPs with different thicknesses were subjected to a series of CV measurements using Keithley 4200, shown in Figure 6.2. The alternating current (AC) bias and frequency used were 30 mV and 1 MHz respectively and the MOSCAPs were swept at a rate of 200 mV/sec. The dielectric constant was extracted to be 8.2-8.5 from the accumulation capacitance on all three samples. The methodology used to extract the trap densities is same as the technique developed by Liu *et al.* [21] and presented briefly here. The MOSCAPs were first taken from depletion (D) to accumulation (A) and kept at accumulation for 10 minutes to fill all the empty electron traps. After 10 minutes, they were again swept back to depletion (1st sweep). Another CV curve is measured by sweeping the MOSCAP from depletion to accumulation and immediately back from accumulation to depletion (2nd sweep). The total charge (Q_I) within the MOSCAPs is calculated from the equation (6.6),

$$V_{FB} = -\frac{qQ_I T_{ox}}{\epsilon \epsilon_0} + V_{FB}^{Ideal} \quad (6.1)$$

where, V_{FB} is the flat band voltage, T_{ox} is the oxide thickness, V_{FB}^{Ideal} is the ideal flat band voltage, q is the electron charge, ϵ is the relative permittivity of the Al₂O₃ layer, and ϵ_0 is the absolute permittivity. Assuming all the charges are located at or near the oxide/semiconductor interface, Q_I can be determined from the linear fit of the V_{FB} vs oxide thickness plot. The

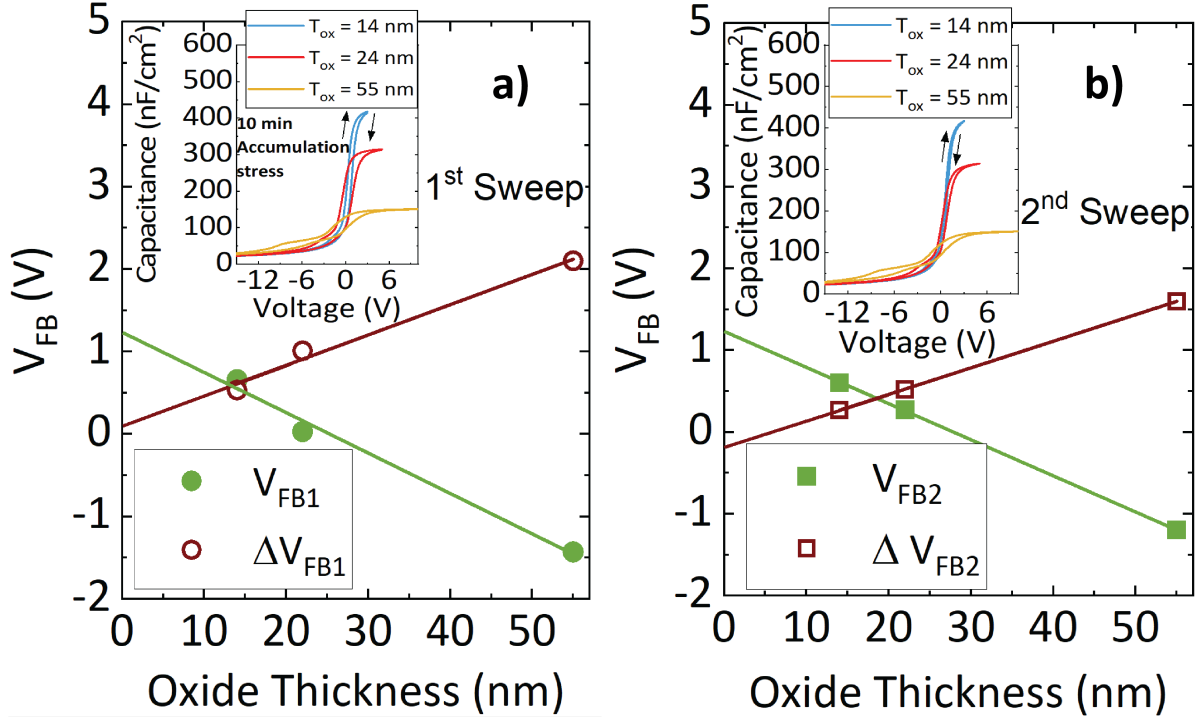


Figure 6.2: Flat band voltage vs oxide thickness for (c) first & (d) second capacitance-voltage sweeps for MOSCAPs with three different dielectric thicknesses. The inset of (a) and (b) shows the corresponding first and second sweep of the CV hysteresis. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

change in V_{FB} for D to A and A to D sweeps of the hysteresis plot can be attributed to the total amount of initially empty trapped charge within the MOSCAPs as described by the equation (6.2),

$$\Delta V_{FB} = -\frac{q\Delta Q_T T_{ox}}{\epsilon\epsilon_0} \quad (6.2)$$

where, ΔV_{FB} is the flat band voltage difference between the D to A and A to D sweeps and ΔQ_T is the trapped electron density. Inset of Figure 6.2 (a) and (b) shows the 1st and 2nd sweeps of the CV hysteresis plots respectively for the MOSCAPs with three different Al_2O_3 thicknesses. The CV measurements were repeatable after the 2nd sweep, overlapping with the 2nd sweep measurements. Different forward bias voltages were applied for MOSCAPs with different Al_2O_3 thicknesses to maintain approximately same electric field through the oxide (~ 2 MV/cm). The electric field of ~ 2 MV/cm was chosen so that the applied electric field remains below the breakdown field of the Al_2O_3 , and also be sufficient enough to cause accumulation.

At this field, the leakage current through the oxide is also found to be negligible and hence it is reasonable to assume that additional traps are not created at such fields. Figure 6.2 (a) and (b) shows the corresponding V_{FB} and ΔV_{FB} for the 1st and second sweeps. Flat band voltages were extracted from the deflection point of the capacitance-voltage plot [29]. V_{FB1} and V_{FB2} are the flat band voltages calculated from the D to A sweeps of the 1st and 2nd sweep, respectively. Fixed charges (Q_{I1} & Q_{I2}) are determined from the slope of the flat band voltage vs oxide thickness plot. Q_{I1} is the fixed charge of the MOSCAP without any bias history. So, Q_{I2} is the total fixed near interface charge in the same MOSCAP, but also contains trapped electrons due to the measurement sweeps and 10 minutes of accumulation stress. Now, ΔV_{FB1} and ΔV_{FB2} are the flat band voltage differences, between each pair of D to A and A to D sweeps of the 1st and 2nd sweep respectively. During the 10 minutes of accumulation stress of the first hysteresis measurement electrons fill the empty slow near interface states and due to the high emission time of the slow traps these electrons remain trapped afterwards. However, electron will fill the fast near interface states also during the 10 min accumulation time. So, ΔV_{FB1} can be attributed to the initially empty fast and slow near interface states (ΔQ_{T1}). Only the fast traps will respond during the second hysteresis and subsequent measurements since the slow traps were filled during the first sweep. So ΔV_{FB2} can be attributed to only the fast near interface states (ΔQ_{T2}). Density of the initially empty slow near interface traps can be evaluated from the difference between ΔQ_{T1} and ΔQ_{T2} ($|\Delta Q_{T1} - \Delta Q_{T2}|$). However, during the first D to A and A to D sweeps, there could be electron emission from some of the slow near interface states due to the applied reverse bias. So, the difference in flat band voltage for the D to A sweeps of 1st and 2nd sweep can be attributed to the more stably filled slow near interface states (ΔQ_{TS}). All the fixed and trapped charges described here are summarized in Table 1. The positive fixed charge observed in this work is similar to the previous report of ALD $\text{Al}_2\text{O}_3/(-201) \text{Ga}_2\text{O}_3$ interface [5].

Very little is known about the origin of the fixed charges and trap states in case of wide band-gap semiconductor/oxide interfaces. The positive fixed charge density at the semiconductor/oxide interface could arise from ionized donor-like traps located in the oxide/semiconductor

Table 6.1: Fixed charge and trap densities at the 600 °C Al₂O₃/β-Ga₂O₃ interface

Q_{I1} (cm^{-2})	Q_{I2} (cm^{-2})	ΔQ_{T1} (cm^{-2})	ΔQ_{T2} (cm^{-2})	$ \Delta Q_{T1} - \Delta Q_{T2} $ (cm^{-2})	ΔQ_{TS} (cm^{-2})
2.3×10^{12}	2×10^{12}	-1.7×10^{12}	-1.2×10^{12}	5×10^{11}	3×10^{11}

interface above the conduction band of the semiconductor. According to the first principle calculations for the Al₂O₃/GaN interface, reported by Choi *et al.* [30], the origin of the positive fixed charges can be attributed to the native defects such as Al vacancies, Al interstitials, and Oxygen interstitials if such defects are present near the interfaces and the fast near interface traps could be attributed to the Al dangling bonds. GaN and β-Ga₂O₃ have similar electron affinity (~4 eV) and, the location of the trap states above the conduction band minima of Ga₂O₃ at the Ga₂O₃/Al₂O₃ interface could have a similar origin related to native defects in Al₂O₃. However, further detailed experimentation is necessary for an accurate understanding of the origin of fixed charges.

The conduction band offset at the Al₂O₃/β-Ga₂O₃ heterostructure can be evaluated using equation (6.7) as V_{FB} can be written as [5],

$$qV_{FB} = -qE_{ox}T_{ox} + (\phi_b - \Delta E_C - \phi_s) \quad (6.3)$$

where, E_{ox} is the electric field in the oxide at flat band condition due to the fixed charge at the Al₂O₃/β-Ga₂O₃ interface, ϕ_b is Ni/Al₂O₃ conduction band barrier height, ϕ_s the difference between the conduction band and fermi level in β-Ga₂O₃, and ΔE_C is the conduction band offset between β-Ga₂O₃ and Al₂O₃. ϕ_b was considered to be 3 eV as evaluated by Zhang *et al.* using internal photoemission spectroscopy [31]. From Figure 6.2 (c) and (d), $(\phi_b - \Delta E_C - \phi_s)$ is extracted to be 1.23 eV. Using equation 6.7, the value of ΔE_C is calculated to be 1.7 eV which matches well with the previous reports on the ALD Al₂O₃/β-Ga₂O₃ heterostructure.

Now, to find the density of all the initially filled slow near interface states and the trap distribution as a function of energy dependence near the β-Ga₂O₃ band edge, we use UV-assisted CV technique developed by Swenson *et al.* [32] and later modified by Liu *et al.* [33]

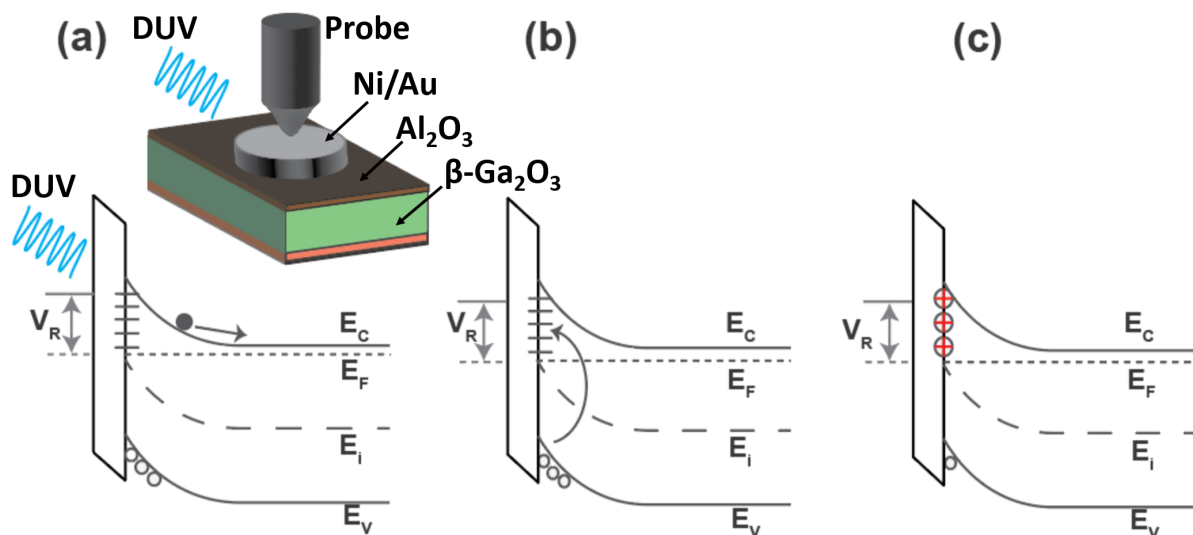


Figure 6.3: Representative energy band diagram for the UV-assisted CV measurements showing (a) generation of electron-hole pairs when excited by UV rays, (b) generated holes recombining with the trapped electrons at the interface, and (c) trap states became positively charged after the electron-hole recombination process. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

This technique was also used by Jian *et al.* [19] for ALD Al₂O₃/(001) β-Ga₂O₃ MOSCAPs and briefly summarized here. The MOSCAPs were first taken from D to A and kept at accumulation for 10 minutes to fill all the interface states. After 10 minutes, the MOSCAPs were again swept back to depletion without any optical excitation. This dark curve is considered as the ideal CV curve, assuming all the states are filled with electrons. Next the MOSCAPs were held at depletion and were exposed to UV light using a Deep ultra-violet (DUV) light emitting diode (LED) with 254 nm wavelength for 5 minutes. After 5 minutes the UV light is turned off and the MOSCAPs were held at depletion for 15 minutes followed by another sweep from D to A. The dark curve is then shifted horizontally to match the post-DUV CV curve and obtained as the reference CV curve. The total density of all the interface states is calculated from the difference between the post-DUV and the reference CV curve (ΔV) and their energy dependence is calculated from the amount of band bending (dielectric/semiconductor surface potential) that occurs during the bias sweep.

Fig. 6.3 (a) to (c) shows energy band diagrams of the MOSCAPs under applied bias and UV illumination. During the UV exposure, electron-hole pairs are generated and the photo-

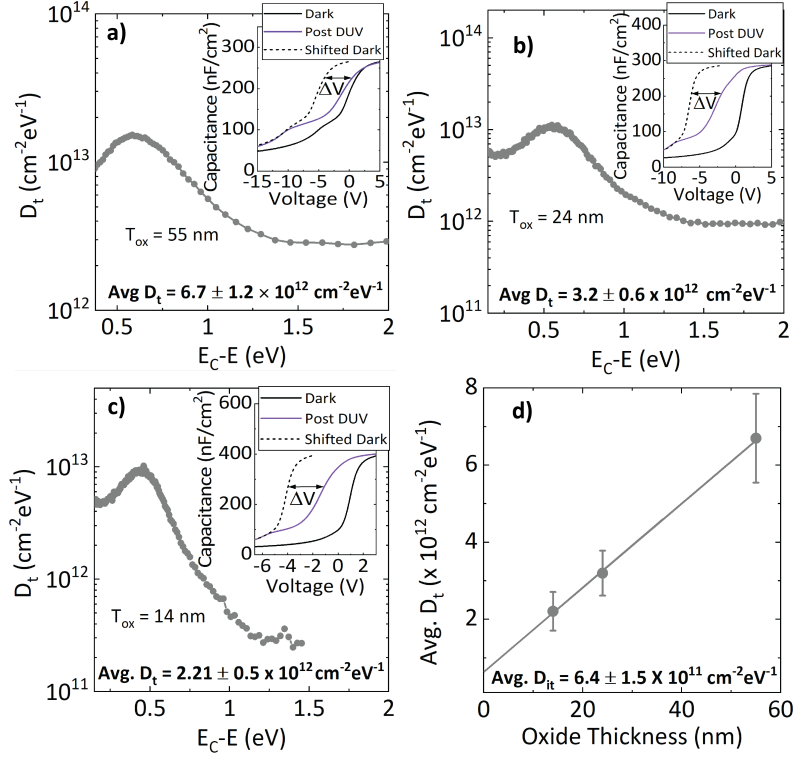


Figure 6.4: Trap density vs energy distribution plots for MOSCAPs with (a) 55 nm, (b) 24 nm, and (c) 14 nm Al_2O_3 thickness. The inset of (a), (b), and (c) shows the UV-assisted CV characteristics of the three MOSCAPs. (d) Average trap density vs oxide thickness plot and the corresponding linear fit. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

generated holes either recombine with the electrons trapped in the interface or gets self-trapped, which results in the ledge observed in the post-DUV curve. Due to the recombination of photo-generated holes with the trapped electrons at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface, the trapped states become positively charged, which changes the width of the depletion region. Some of the extra holes also get trapped in the dielectric bulk hole traps inside the Al_2O_3 layer. Inset of Figure 6.4 (a) to (c) shows CV plots for the MOSCAPs with three different oxide thicknesses. The black curve (Dark) is the A to D sweep after the 10 minutes of accumulation stress. The purple curve is the D to A sweep after DUV exposure and the dashed black curve is the reference curve obtained after shifting the dark curve to match deep depletion part of the post-DUV plot [32]. ΔV in the CV plot of Figure 6.4 (a) to (c) includes the effects of both interface traps at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface and bulk hole traps inside the Al_2O_3 layer. Density of all the initially filled interface and bulk dielectric traps is calculated using the equation (6.4) [32],

$$D_t = \frac{C_{ox}}{qA} \frac{d\Delta V}{d\psi_S} \quad (6.4)$$

where, ψ_S is the surface potential at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface, given by $\psi_S = \frac{q\epsilon\epsilon_0 N_D A^2}{2C_{dep}^2}$. N_D is the doping density, A is the area of the contacts, C_{dep} is the depletion capacitance and C_{ox} is the oxide capacitance.

Figure 6.4 (a) to (c) shows the D_t vs the trap energy distribution for the MOSCAPs with three different oxide thicknesses. Due to the existence of a positive valence band offset, the extra holes (which did not recombine with the interface traps) get accumulated at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface (some holes also get self-trapped). The rise in the D_t near the conduction band edge can be attributed to the accumulated holes, either at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface or possibly also due to the self-trapped holes in the depletion region [34]. The average D_t for each of the MOSCAPs are obtained after eliminating the contribution from holes by neglecting the rise in D_t .

We can also see from Figure 6.4 (a) to (c) that the average D_t reduces as the thickness of the Al_2O_3 layer decreases. There would not be any dielectric thickness dependence if all the traps were located at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface. Instead, due to the presence of bulk hole traps inside the Al_2O_3 layer, some of the holes get captured inside the Al_2O_3 layer. So, the density of the interface states (D_{it}) without the contribution from the bulk hole traps in the Al_2O_3 is calculated from the equation (6.5) [33]

$$D_t = D_{it} + T_{ox} \frac{dn_{ht}}{2d\psi_S} \quad (6.5)$$

where, n_{ht} is the amount of bulk hole traps inside the Al_2O_3 . So, average D_{it} is obtained to be $6.4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ by extrapolating the linear fit of average D_t vs oxide thickness for $T_{ox} = 0$ as shown in Figure 6.4(d). The amount of bulk hole traps (n_{ht}) is estimated from the equation 6.5 to be $2.1 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$. The fact that we see a linear relationship of D_t vs oxide thickness clearly indicates that not all the holes are self-trapped in the $\beta\text{-Ga}_2\text{O}_3$ and in-fact can move and get inside the Al_2O_3 layer and get trapped. The mobility of holes could

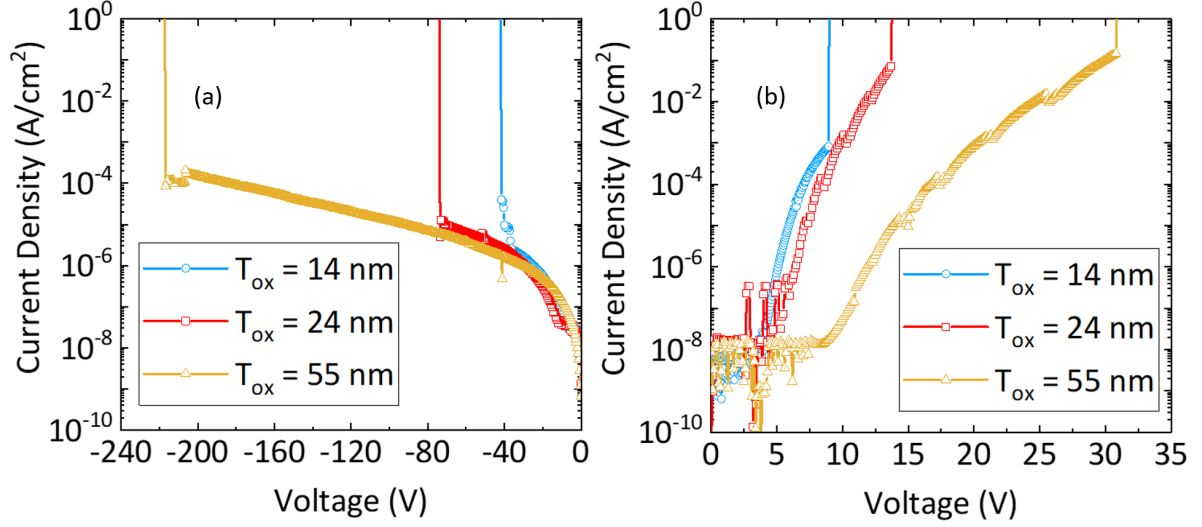


Figure 6.5: (a) Reverse and (b) forward current-voltage characteristics for MOSCAPs with three different dielectric thicknesses. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

be significant enough to cause bulk hole trapping in the dielectric as also extracted by Akyol [35] for β -Ga₂O₃ Schottky barrier diode based photodetector. The value of D_{it} obtained for the in-situ Al₂O₃ MOSCAPs are significantly lower than the previous reports of ALD Al₂O₃/ (001) β -Ga₂O₃ interface and may have resulted from the O vacancies and Al dangling bonds at the interface. However, the average D_{it} obtained for ALD Al₂O₃/(010) β -Ga₂O₃ as reported by Kamimura *et al.* was found to be lower than the present work ($5.9 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ - $9.3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [36]. We should mention here that the high-low CV method used for extracting the trap densities by Kamimura *et al.* underestimates the total D_{it} as it cannot keep track of deep level traps.

6.2.3 Current-Voltage Characterization

To determine leakage currents and breakdown voltages of the MOSCAPs, reverse and forward current voltage (IV) characteristics is measured and shown in Figure 6.5 (a) and (b) respectively. The measurement is performed at a sweep rate of 200 mV/sec. Breakdown voltages with positive bias on the gate metal (accumulation) for MOSCAPs with 14, 24 and 55 nm Al₂O₃ thicknesses are 9, 14, and 32 V, respectively. The breakdown field for all the MOSCAPs were determined

using Sentaurus device simulator [37] and the field profile is shown in Figure 6.6 (a). For the accumulation case with positive potential on the gate, the entire voltage is dropped across the Al_2O_3 layer and so the breakdown can be attributed to the breakdown of the dielectric. The average breakdown field at the center of the gate metal region and peak field at the edges of the metal for the Al_2O_3 dielectric are estimated to be ~ 5.8 MV/cm and 15 MV/cm respectively from electric field simulations as shown in Figure 6.6 (a). Electric fields were shown only in the Al_2O_3 region during forward bias as the entire bias voltage is dropped across the oxide layer. Breakdown voltage of the in-situ MOCVD-grown oxide is lower compared to previous reports based on ALD deposition, and the breakdown voltage could be improved using in-situ O_2 annealing as demonstrated in MOCVD-grown Al_2O_3 on III-Nitrides [38]. The barrier to tunneling for the MOSCAPs were also estimated using trap assisted tunneling model and extracted to be 1.1 eV and presented in the supporting information. The reduced barrier to tunneling compared to the actual band-offset extracted using CV method suggests that the leakage current is mostly dominated by the positive fixed charge state at the interface which exists in between the conduction band minima of the Al_2O_3 and $\beta\text{-Ga}_2\text{O}_3$ possibly due to the presence of Aluminum or Oxygen interstitials. However, other traps states such as border traps which may originate from Oxygen vacancies cannot be ruled out and requires further investigation. If the leakage is dominated by the border traps due to oxygen vacancies, then annealing in oxygen may passivate these traps and can lead to reduced leakage currents. The reverse breakdown voltage from the IV characteristics in Figure 6.5 (a) for MOSCAPs with 14, 24 and 55 nm Al_2O_3 thicknesses are approximately 40, 80, and 200 V, respectively. From the electric field distribution in Figure 6.6 (b), a peak field of ~ 15 MV/cm is observed at the metal edges but the center of the gate metal, the electric field is less than the observed field in case of forward bias (~ 3.5 MV/cm as compared to 5.8 MV/cm). This is due to the fact that, at reverse bias, the total applied voltage is dropped across both Al_2O_3 and Ga_2O_3 region and a significant amount of electric field is present in the Ga_2O_3 (~ 2.6 MV/cm) as also shown by the dashed curves in Figure 6.6 (b). At reverse bias, all the three MOSCAPs ($T_{\text{ox}} = 14, 24$ and 55

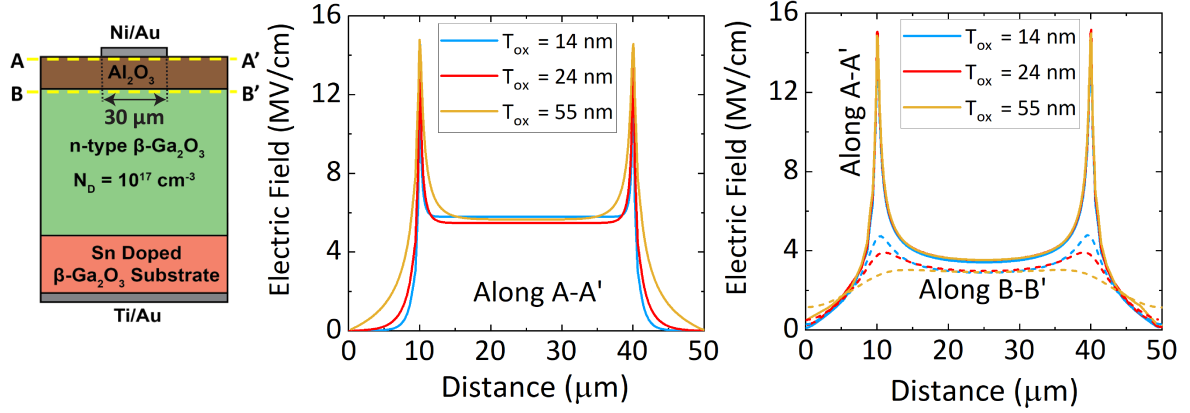


Figure 6.6: Simulated electric field profiles for the MOSCAPs with three different Al_2O_3 thicknesses at (a) forward breakdown voltage along A-A' (9, 14, and 32 V for $T_{\text{ox}} = 14, 24,$ and 55 nm respectively) and (b) reverse breakdown voltage along A-A' (solid line) and B-B' (dashed line) (-40, -80, and -200 V for $T_{\text{ox}} = 14, 24,$ and 55 nm respectively). Electric field is plotted only at the Al_2O_3 region at forward bias because entire bias voltage is dropped across the oxide layer during accumulation. Reprinted from Roy *et al.* [25], with permission from John Wiley and Sons.

nm) have a peak electric field of around ~ 15 MV/cm, indicating that the breakdown is probably happening at the metal edges. These high edge electric fields can be reduced by creating a field plate structure using the same in-situ Al_2O_3 material showing the versatility of this technique.

The in-situ Al_2O_3 grown using MOCVD, in this work, is found to have reduced fixed charges and interface traps (D_{it}) compared to the more commonly used ALD technique. A lower fixed charge concentration of $+2 \times 10^{12} \text{ cm}^{-2}$ is found when compared to ALD Al_2O_3 on (-201) $\beta\text{-Ga}_2\text{O}_3$ ($+3.6 \times 10^{12} \text{ cm}^{-2}$) reported by Hung *et al.* [5]. A lower interface trap density (D_{it}) of $6.4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ is also extracted using UV-assisted CV method. It is to be noted that no high temperature post deposition annealing (PDA) or post metallization annealing (PMA) is performed on these MOSCAPs, which is expected to further improve the interface quality [38]. Further experiments to understand the effect of growth parameters such as growth temperature, chamber pressure and precursor ratios and also higher temperature PDA will be necessary to improve the dielectric constant, fixed charge, interface traps and critical breakdown fields of the Al_2O_3 layers in these fully MOCVD-grown $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ MOSCAPs. Also, detailed work is necessary to investigate the origin of the interface traps which may have resulted from native defects and impurities at the interface and can be performed using structural and spectroscopic

techniques.

6.3 High-temperature Growth of Insitu-Dielectric and Characterization

In this section, the MOCVD growth of in-situ dielectric at high temperature and capacitance-voltage (C-V) characterization of Al_2O_3 on (010) oriented $\beta\text{-Ga}_2\text{O}_3$ metal-oxide-semiconductor capacitors (MOSCAPs) is presented. Two different dielectrics are grown, one at 800 °C (Fig. 6.7 (a)) and another with 800 °C interfacial layer and the bulk grown at 600 °C (Hybrid) (Fig. 6.7 (b)). Additionally, we present findings on the quality, reliability, and lifetime analysis of in-situ MOCVD-grown Al_2O_3 dielectrics grown at various temperatures. This includes evaluations of interface-state density, leakage current, breakdown strength, and time-dependent dielectric breakdown.

6.3.1 Dielectric Growth and Structural Characterization

The growth of a 500 nm $\beta\text{-Ga}_2\text{O}_3$ epilayer on Sn-doped bulk (010) $\beta\text{-Ga}_2\text{O}_3$ substrates (NCT Japan) was conducted using an Agnitron MOVPE reactor with a far injection showerhead design [27]. Prior to loading the sample into the growth chamber, the substrates were cleaned with acetone, methanol, and deionized (DI) water, followed by a 15-minute dip in hydrofluoric acid (HF). Triethylgallium (TEGa) and O_2 were used as precursors, argon (Ar) as the carrier gas, and diluted silane as the dopant. The growth process was performed at a low temperature of 600 °C and a chamber pressure of 60 Torr. The gas flow rates for TEGa and O_2 were set at 65 sccm and 800 sccm, respectively, with an Ar flow rate of 1100 sccm. A silane flow rate of 0.06 nmol/min was used to achieve a silicon doping concentration of 10^{17} cm^{-3} . Under these conditions, a $\beta\text{-Ga}_2\text{O}_3$ growth rate of 6.3 nm/min was achieved.

After the $\beta\text{-Ga}_2\text{O}_3$ growth, a 90-second purge step was implemented to remove all unreacted precursors from the reactor. During this step, the reactor pressure was reduced from 60 to 15

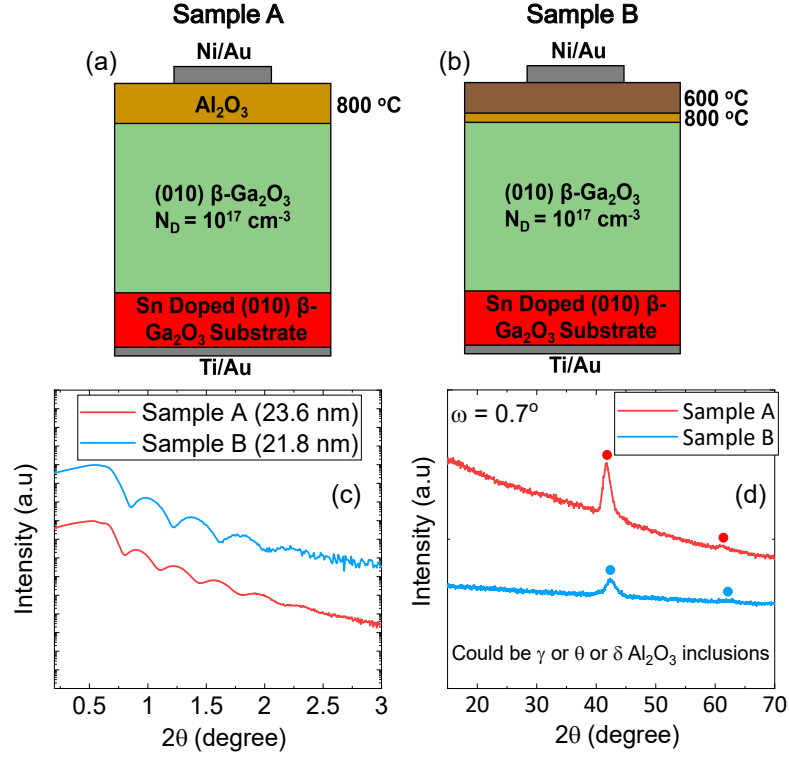


Figure 6.7: Schematic diagram of the fabricated MOSCAP structures with (a) Sample A (800 °C) and (b) Sample B (800/600 °C). (c) X-ray reflectivity plot and (d) GIXRD spectra for Sample A and Sample B.

Torr while the substrate temperature was increased from 600 °C to 800 °C. Additionally, the O₂ flow rate was decreased from 800 to 500 sccm. Following this purge step, an in-situ Al₂O₃ layer was grown at a rate of 1.2 nm/min using the trimethylaluminum (TMAI) precursor at a flow rate of 5.33 $\mu\text{mol/min}$ and O₂ at a flow rate of 500 sccm. The growth rate of the Al₂O₃ layer was determined to be 4.7 nm/min. This is referred to as sample A.

To grow the hybrid dielectric (800 °C thin interfacial layer/600 °C bulk), a 5 nm thin interfacial layer was first grown at 800 °C. After this, the growth temperature was ramped down from 800 °C to 600 °C over the course of 5 minutes. Following this temperature ramp, the bulk of the dielectric was grown at 600 °C, using the same gas flow rates and chamber conditions as for the 800 °C dielectric. The growth rate of the dielectric at 600 °C was determined to be 1.2 nm/min. This is referred to as sample B. The thicknesses of the dielectric layers were measured using X-ray reflectivity (XRR) as shown in Fig. 6.7 (c), resulting in values of 23.6 nm for the 800°C dielectric and 21.8 nm for the hybrid dielectric.

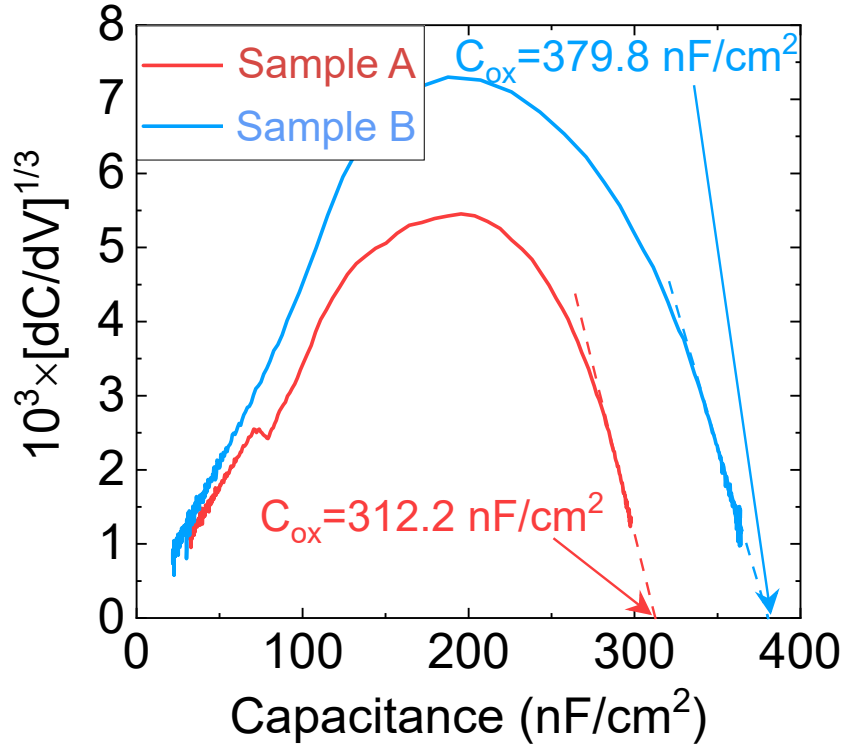


Figure 6.8: $|dC/dV|^{1/3}$ vs capacitance plot for Sample A and Sample B, which is used to extract the oxide capacitance from the x-intercept of the linear fit in the accumulation region.

Grazing incident X-ray measurements (GIXRD) were conducted on the dielectrics grown using metal-organic chemical vapor deposition (MOCVD) to analyze the crystallinity of the MOCVD grown Al_2O_3 layers. The measurements were performed at a fixed incident angle of 0.7° , as depicted in Fig. 6.7 (d). The resulting GIXRD spectra were then compared against the International Centre for Diffraction Data (ICDD) Powder Diffraction File (PDF) database to determine the phase of Al_2O_3 . Dielectrics in sample A and B exhibited some degree of crystallinity, possibly in the θ or γ phase. However, the presence of the δ phase cannot be entirely ruled out as the major diffraction peaks of the δ phase closely resemble those of the γ or θ phase. Further microstructure analysis using transmission electron microscopy will be reported elsewhere.

After the growth of the Al_2O_3 layer, Ti (50 nm)/Au (100 nm) ohmic contacts were sputter-deposited on the backside of the MOSCAPs. Finally, circular Ni (10 nm)/Au (50 nm) gate contacts were patterned using standard photolithography and deposited on the Al_2O_3 surface

via E-beam evaporation.

6.3.2 Extraction of Trap-Densities and dielectric constant

The dielectric constant of the dielectrics are extracted based on the method described by Islam *et al.* [39]. C_{ox} is calculated from the x-intercept of the linear fit at the accumulation region of the $\left|\frac{dC}{dV}\right|^{1/3}$ vs Capacitance plot as shown in Fig. 6.8. The applied method considers a distribution of electrons in the accumulation layer and electron wave function penetration into the dielectric and is more accurate than the dielectric constant extraction from accumulation capacitance. The extracted dielectric constant for the sample A and sample B are 8.32 and 9.35 respectively.

The detailed C-V measurement techniques and the extraction of trap densities are described elsewhere [21], [25]. Using a direct-current (DC) bias range of (-10 V, 5 V) and a sweep rate of 200 mV/s, a MOSCAP was initially swept from depletion to accumulation (D to A) and held in accumulation for 10 minutes before being swept back to depletion (A to D). It was then swept from D to A and immediately back from A to D for a second time. The alternating-current (AC) measurement bias and frequency were set at 30 mV and 1 MHz, respectively. Fig. 6.9(a) and 6.9(b) present the first and second pairs of D to A and A to D sweeps measured on MOSCAPs with sample A and sample B, respectively.

In this study, only interface traps and border traps are considered, which can be identified by the hysteresis they induce in the C-V curve. However, distinguishing between interface states and border traps using only C-V measurements is not straightforward, so we treat them collectively as near-interface states. We also differentiate trap states based on their electron emission characteristics. Fast trap states, which have relatively short emission responses, always induce hysteresis. In contrast, slow trap states, with longer emission responses, behave like fixed charges [21] once filled and no longer induce hysteresis. This behavior is due to the scarcity of holes available to recombine with the trapped electrons, as the minority carrier generation rate in β -Ga₂O₃ at room temperature is very low. Slow trap states may also exhibit long emission time constants. Fixed charges, which cause a permanent shift in the flat band voltage without

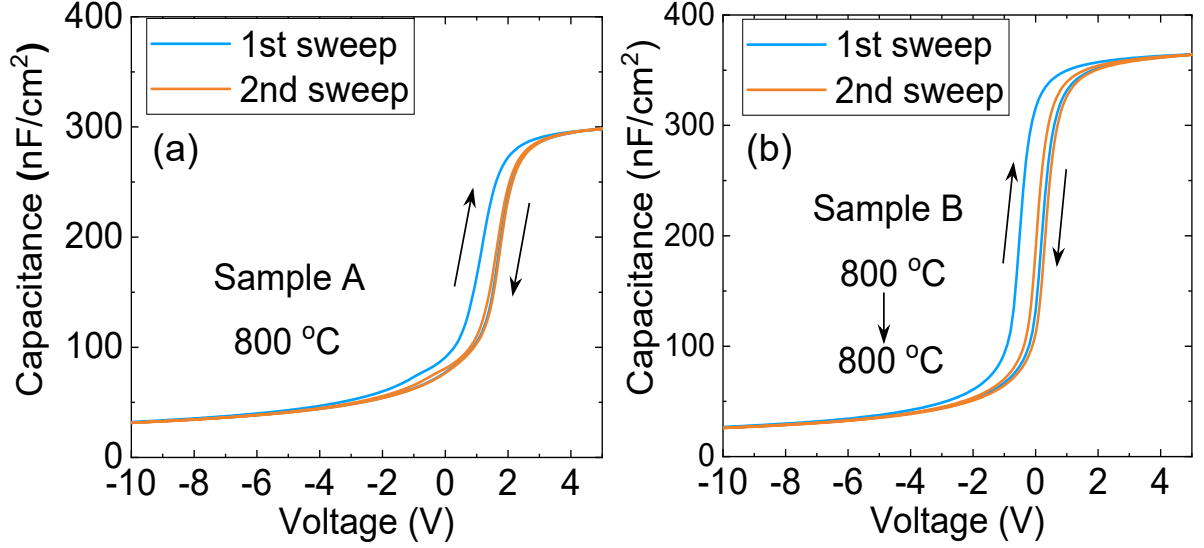


Figure 6.9: First and second sweep of capacitance vs voltage characteristics for (a) Sample A and (b) Sample B. In each case, during the first D-A sweep, MOSCAPs were subjected to a 10 minutes of accumulation stress.

inducing hysteresis, are typically identified through a dielectric thickness-dependent flat band voltage analysis. However, this aspect is not considered in our current work. The hysteresis (ΔV_{FB}) is quantified as the difference in flat band voltage between each pair of depletion-to-accumulation (D to A, V_{FB}^{D-A}) and accumulation-to-depletion (A to D, V_{FB}^{A-D}) sweeps as shown in Fig. 6.9(a) and (b). After the first D to A sweep, the MOSCAPs are held in accumulation for 10 minutes, allowing electrons to fill all the empty near-interface states and remain trapped. During any D to A sweep, electrons can also fill the fast near-interface states, but these electrons are not released at the same rate during the subsequent A to D sweep. Consequently, the first hysteresis (ΔV_{FB1}) is influenced by both fast and initially empty slow near-interface states, while the second hysteresis (ΔV_{FB2}) is influenced only by the fast near-interface states [23]. Without the presence of any additional charge components, both ΔV_{FB1} and ΔV_{FB2} should be positive due to electron trapping, with ΔV_{FB1} being larger than ΔV_{FB2} . The trapped electron density (ΔQ_T) associated with ΔV_{FB} can be estimated from,

$$\Delta Q_T = -\frac{C_{ox}\Delta V_{FB}}{q} \quad (6.6)$$

Using (6.6), we can determine the amount of fast and initially empty slow near-interface

Table 6.2: Near-interface trap densities of the MOSCAPs

Dielectric Type	ϵ_{ox}	^a Q_{T1} (cm^{-2})	^b ΔQ_{T2} (cm^{-2})	^c $\Delta Q_{T1} - \Delta Q_{T2}$ (cm^{-2})	^d Avg. D_t ($cm^{-2}eV^{-1}$)
600 °C [25]	8.3	-1.7×10^{12}	-1.2×10^{12}	-5×10^{11}	3.2×10^{12}
Sample A (800 °C)	8.32	-8.3×10^{11}	-1.5×10^{11}	-6.8×10^{11}	6.1×10^{11}
Sample B (800/600 °C)	9.35	-1.64×10^{12}	-2.74×10^{11}	-1.36×10^{12}	1.02×10^{12}

^a ΔQ_{T1} = Amount of fast and initially empty slow near-interface states

^b ΔQ_{T2} = Amount of fast near-interface states

^c $\Delta Q_{T1} - \Delta Q_{T2}$ = Amount of initially empty slow near-interface states

^dAvg. D_t extracted from deep UV CV measurements.

states (ΔQ_{T1}) as well as the fast interface states (ΔQ_{T2}). Also, the difference, $\Delta Q_{T1} - \Delta Q_{T2}$, represents the densities of the fast and initially empty slow near-interface states. From these measurements, trap densities and dielectric constants are extracted and summarized in Table 6.2. For comparison, the trap densities of the 600 °C dielectrics from our previous work [25] are also included in Table 6.2.

The MOSCAP with the sample A exhibits fewer fast and initially empty slow near interface states ($\Delta Q_{T1} = -8.3 \times 10^{11} cm^{-2}$) and also the lower amount of fast interface states ($\Delta Q_{T2} = -1.5 \times 10^{11} cm^{-2}$) compared to the 600 °C dielectric as can be seen from Table 6.2. This improvement is likely due to the enhanced interface crystallization at 800 °C, which reduces the number of Al dangling bonds at the dielectric/semiconductor interface. However, dielectric growth at higher temperatures can also lead to bulk nanocrystalline inclusions, raising long-term reliability concerns. To mitigate these issues, a hybrid dielectric structure with a 5nm interfacial layer grown at 800 °C (5nm) and bulk dielectric grown at 600 °C (sample B) is more favorable. ΔQ_{T1} and ΔQ_{T2} of the sample B is also found to be lower than 600 °C dielectric as shown in Table 6.2. Higher values of ΔQ_{T1} and ΔQ_{T2} for the sample B compared to the sample A is

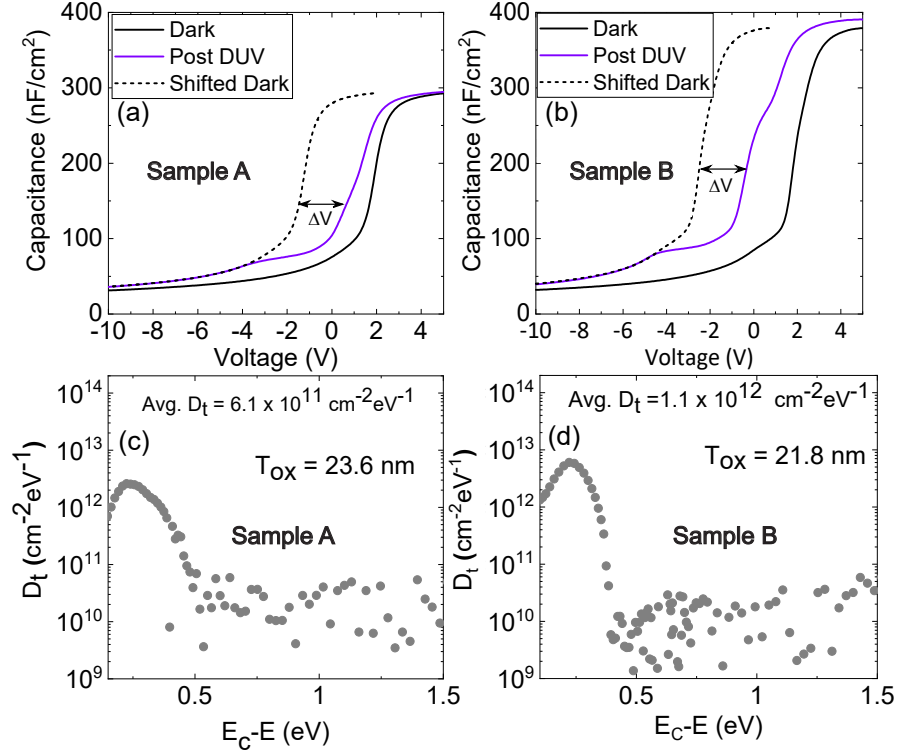


Figure 6.10: UV-assisted CV characteristics and Trap density vs energy distribution plots respectively of the MOSCAPs on (a) (c) Sample A and (b) (d) Sample B.

likely due to the near interface states at the 800/600 °C dielectric interface.

The density of all (slow and initially filled) interface trap states are extracted using UV-assisted CV method as described in section 6.2.2 and shown in Fig. Fig. 6.10(a-b). Fig. 6.10(c) to (d) depicts the relationship between trap density (D_t) and the trap energy distribution for the MOSCAPs with sample A and sample B. The presence of a positive valence band offset at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ results in the accumulation of additional holes at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface, which do not recombine with the interface traps. Notably, the increase in D_t near the conduction band edge can be attributed to these accumulated holes. To obtain the average D_t for the MOSCAPs, we exclude the contribution from holes by disregarding the rise in D_t . The average D_t values for the different MOSCAPs are listed in Table 6.2. The MOSCAP with sample A exhibits the lowest average D_t density ($6.1 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$) among the three MOSCAPs. Additionally, the MOSCAP with sample B also shows a lower average D_t ($1.02 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$) compared to the MOSCAP grown at 600°C dielectric (3.2×10^{12}

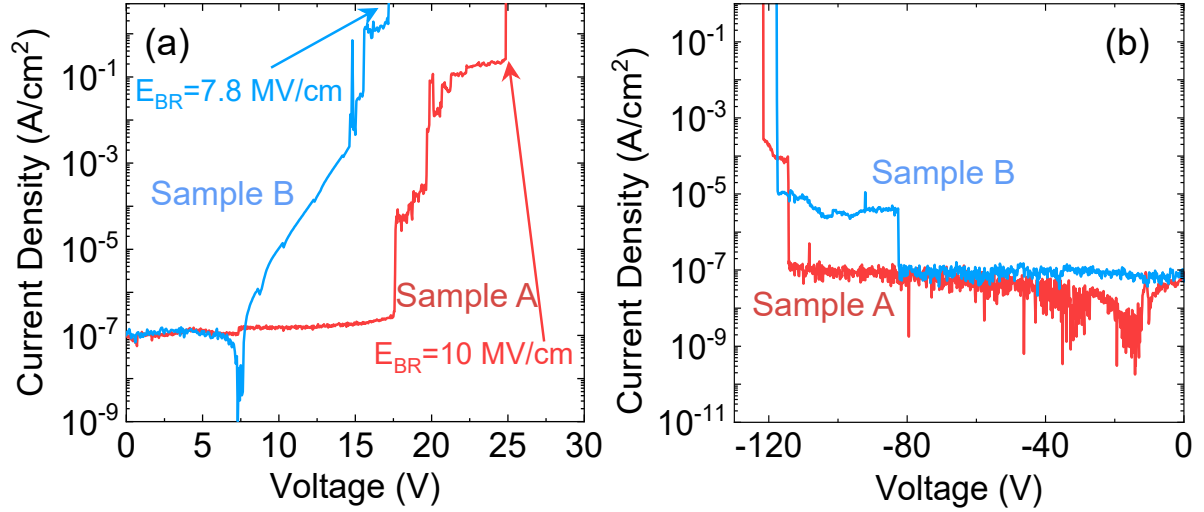


Figure 6.11: (a) Forward and (b) reverse current-voltage characteristics for MOSCAPs on Sample A and Sample B.

$\text{cm}^{-2}\text{eV}^{-1}$). Notably, the D_t values for both sample A and sample B are lower than the ΔQ_{T1} and ΔQ_{T2} values, which likely indicates a different origin for the fast and initially empty slow interface states.

6.3.3 Current-Voltage Characterization

To determine the breakdown voltages of the MOSCAPs under forward and reverse bias, current-voltage (IV) measurements were performed, as shown in Fig. 6.11. Sample A exhibits a breakdown voltage of 25V, corresponding to an impressive breakdown field of approximately 10 MV/cm under forward bias, as illustrated in Fig. 6.11(a). For sample B, the breakdown voltage is around 17V, translating to a breakdown field of about 7.8 MV/cm.

The reverse breakdown voltage, derived from the IV characteristics in Fig. 6.11(b), is approximately 120V for MOSCAPs with both sample A and sample B. In the accumulation case, with a positive potential applied to the dielectric, the entire voltage drop occurs across the Al_2O_3 layer, thus the breakdown can be attributed to the dielectric. However, under reverse bias, the total applied voltage is distributed across both the Al_2O_3 and Ga_2O_3 regions. Consequently, a significant electric field is present in the Ga_2O_3 , indicating that the reverse breakdown cannot be

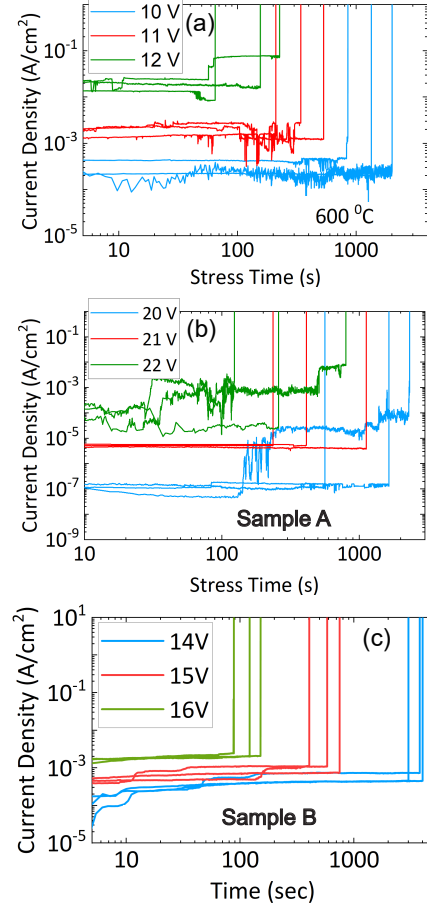


Figure 6.12: Constant-voltage-stress current density vs time plot performed at three different voltages on the MOSCAPs on (a) 600 °C [25] (b) Sample A, and (c) Sample B.

solely attributed to the dielectric breakdown. Hence, the forward breakdown is a good indication of the dielectric material quality.

6.3.4 Dielectric Reliability and Lifetime Characterization

To characterize the reliability of the in-situ dielectrics, time-dependent dielectric breakdown tests [40], [41] were performed under constant voltage stress. The currents in the 600°C, 800°C (sample A), and hybrid dielectric (sample B) MOSCAPs under constant stressing voltages at room temperature are displayed in Fig. 6.12(a)-(c). For each dielectric sample, the MOSCAPs were stressed at three different voltages close to the breakdown voltage of the devices, with 10 devices for each sample stressed at the same voltage to obtain sufficiently good statistics.

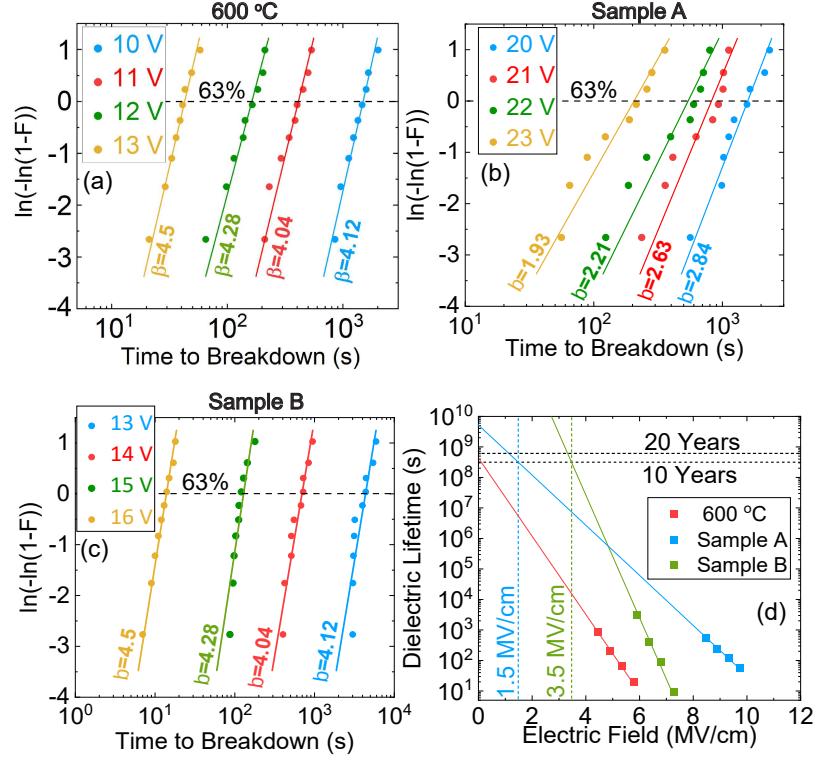


Figure 6.13: Weibull distributions of measured lifetimes at room temperature with different voltage stress for (a) 600 °C [25] (b) Sample A, and (c) Sample B. (d) Dielectric lifetime vs oxide electric field for the three different dielectrics

The 600°C and sample B exhibit hard breakdown during stress, indicated by a sudden rise in current marking the breakdown. However, sample A exhibits some pre-breakdown current increases in many devices, indicating soft breakdown, which likely results from leakage through grain boundaries of polycrystalline regions. The time-to-breakdown for dielectrics can be well approximated using a Weibull function given by (6.7).

$$F(t_{stress}) = 1 - \exp \left[- \left(\frac{t_{stress}}{\eta} \right)^\beta \right] \quad (6.7)$$

where $F(t_{stress})$ is the cumulative probability of breakdowns, t_{stress} is the stress time, η is the scale parameter (often referred to as the characteristic lifetime or the time at which 63.2% of the sample population fails), and β is the shape parameter. The Weibull plots for the time to breakdown for the three different dielectrics are shown in Fig. 6.13 (a)-(c). For all three cases, the breakdown is found to be intrinsic, as indicated by $\beta > 1$ for all dielectrics. However, the

600°C and hybrid dielectrics exhibit much tighter distributions ($\beta > 4$) compared to the 800°C dielectric, suggesting higher oxide uniformity.

We define the lifetime of the in-situ Al_2O_3 films as the time to breakdown when the cumulative probability of breakdowns reaches 63%, satisfying $\ln[-\ln(1 - F(t_{\text{stress}}))] = 0$ [42]. Assuming $E_{BR} \approx V_{BR}/t_{ox}$, the extracted $t_{63\%}$ as a function of E_{BR} for the three different dielectrics is plotted in Fig. 6.13 (d). Lifetime predictions under typical operating conditions are made based on the commonly used E-model [43], which states that the breakdown time (t_{BR}) in the log scale is inversely proportional to the oxide electric fields ($\ln(t_{BR}) \propto -\gamma E_{BR}$). The slope parameter γ is often referred to as the electric field acceleration factor, describing the rate at which t_{BR} changes with E_{BR} .

For sample A, the estimated time to breakdown (t_{BR}) is 10 years if the oxide electric field (E_{ox}) remains below 1.5 MV/cm ($E_{ox} \leq 1.5$ MV/cm). Although the lifetime of the 600 °C dielectric is shorter than that of the 800 °C dielectric (sample A) at the same stressing electric field, the acceleration factor (γ) for the 600 °C dielectric is higher, as evident in Fig. 7(d). This higher acceleration factor is expected due to the higher β value of the 600 °C dielectric. On the other hand, sample B exhibits a t_{BR} of 10 years, with a stressing electric field of 3.5 MV/cm. The longer t_{BR} for the hybrid dielectrics results from reduced polycrystalline features within the bulk of the dielectric compared to the sample A, as well as a pristine dielectric/semiconductor interface compared to the 600 °C dielectric.

The in-situ Al_2O_3 grown using MOCVD at a temperature of 800 °C (sample A) exhibits fewer near-interface trap states compared to Al_2O_3 grown at 600 °C. Additionally, the breakdown field for sample A (10 MV/cm) is higher than that of the 600 °C dielectric (5.6 MV/cm). However, the time-to-breakdown of the 600 °C dielectric is more uniform compared to sample A. Sample B combines the best features of both materials, with reduced interface traps and higher breakdown strength compared to the 600 °C dielectric. Furthermore, the uniformity of the time-to-breakdown is also higher for the sample B compared to both the 600 °C and 800 °C dielectrics. Consequently, sample B is a more suitable choice as gate dielectrics in

β -Ga₂O₃-based high-voltage transistor applications.

6.4 Summary

In summary, this chapter investigates the potential of in-situ Al₂O₃ growth using Metal-Organic Chemical Vapor Deposition (MOCVD) as a superior alternative to Atomic Layer Deposition (ALD). The quality of the interface has been thoroughly characterized through capacitance-voltage (C-V) measurements. Our analysis identified and quantified the presence of near-interface fixed charges in the metal-oxide-semiconductor capacitors (MOSCAPs), revealing a stable positive fixed charge density of $+2 \times 10^{12} \text{ cm}^{-2}$. Additionally, we determined the sheet density of trap states with both fast and slow emission times by examining the linear relationship between C-V hysteresis and Al₂O₃ thickness.

The density of near-interface traps, along with their energy dependence, was further quantified using the ultraviolet (UV)-assisted C-V technique, yielding a value as low as $+6.4 \times 10^{11} \text{ cm}^{-2}$. We also calculated the conduction band offset, deriving a value of 1.7 eV from the linear correlation between flat band voltage and oxide thickness. Moreover, the average breakdown field for the MOCVD-grown Al₂O₃ material was found to be approximately 5.8 MV/cm.

Additionally, this chapter explores in-situ Al₂O₃ growth at elevated temperature, and further employs a hybrid dielectric growth method that combines an 800 °C interfacial layer with bulk dielectric deposition at 600 °C. To evaluate interface quality, we conducted a comparative study of different dielectric materials using capacitance-voltage measurements. The density of near-interface states was characterized using both conventional and UV-assisted C-V techniques across the three dielectric materials.

The results indicate that the 800 °C dielectric demonstrates superior performance in terms of near-interface trap states and breakdown field strength compared to the other two dielectric materials. However, the hybrid dielectric (Sample B) exhibited significantly improved uniformity, leading to enhanced dielectric lifetime and better interface quality than the 600 °C

dielectric. Consequently, the hybrid dielectric represents a more suitable compromise among the three options examined. This in-situ dielectric deposition approach on β -Ga₂O₃ holds great promise for the development of future high-performance MOSFETs, providing improved interface and bulk quality, as well as greater uniformity compared to conventional dielectric deposition techniques.

This approach of in-situ dielectric deposition on β -Ga₂O₃ can pave the way as gate dielectrics for future β -Ga₂O₃ based high performance MOSFETs due to its promise of improved interface and bulk quality compared to other conventional dielectric deposition techniques.

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Chapter 7

β -Ga₂O₃ Vertical Power Transistors

7.1 Introduction

The lack of p-type doping in β -Ga₂O₃ presents a significant obstacle to transistor development. In traditional Si and SiC-based power transistors, a conducting channel is typically formed by inverting a semiconductor with carriers of the opposite type through an electric field, the principle behind Field Effect Transistors (FETs). However, due to the unavailability of p-type doping in β -Ga₂O₃, new architectures based on unipolar operation must be devised to realize power transistors in this material system.

Before exploring the technical specifics of Ga₂O₃ vertical fin transistors, it is essential to review the core requirements of vertical power transistors, which help clarify whether p-type doping is indeed necessary. At the heart of any power transistor lies a junction capable of blocking voltage. This function can be served by a p-n junction, a Schottky junction, or a MOS structure, each with distinct advantages, as discussed in Chapter 1. In the absence of p-type doping, only the latter two structures—Schottky and MOS—are viable, with MOS structures typically offering superior performance in terms of reducing reverse leakage current, making them a strong candidate.

Another critical requirement is the confinement of carriers within a channel to enable

effective gate control. This can be achieved through three different mechanisms: (i) geometric confinement through patterning techniques such as etching, (ii) potential barriers, which are formed at abrupt heterojunction interfaces or inversion channels, and (iii) conductivity contrast, often seen in lateral transistors fabricated on semi-insulating substrates. Crucially, none of these methods necessitates p-type doping. For example, AlGaN/GaN HEMTs utilize potential barriers, while most lateral transistors in β -Ga₂O₃ rely on conductivity contrast. The first method, which uses etched fin channels, is a defining feature of vertical fin transistors.

In terms of gate control, the structure itself plays a vital role in transistor performance. The primary device configurations—junction gates, Schottky gates, and MOS structures—each lend their characteristics to different transistor types: junction-gate FETs (JFETs) [1], metal-semiconductor FETs (MESFETs) [2], and MOSFETs [3]. Even without p-type doping, Schottky and MOS structures remain highly effective, with MOS gates being particularly advantageous for achieving normally-off operations due to their lower gate leakage current.

Lastly, establishing efficient ohmic contacts for the source and drain is crucial in most vertical power transistors. For devices other than insulated-gate bipolar transistors (IGBTs) [4], only n-type ohmic contacts are typically required, simplifying fabrication. While p-body contacts also play a role in certain designs, they are not pertinent to this discussion.

Thus, the absence of p-type doping does not preclude the realization of vertical transistors. In fact, by leveraging MOS structures, vertical transistors, such as the vertical fin MOS-gate transistors, can be successfully implemented, providing a path forward for power electronics in β -Ga₂O₃.

7.2 History of β -Ga₂O₃ Vertical Transistors

Despite remarkable advancements in β -Ga₂O₃ electronics, the development of vertical transistors has faced persistent challenges. Sasaki *et al.* [5] pioneered the field with a depletion-mode vertical trench MOSFET, though its behavior resembled that of a static induction transistor

(SIT) rather than a conventional MOSFET. Subsequently, Hu *et al.* [6] introduced a depletion-mode vertical FinFET, achieving a breakdown voltage of 185 V, albeit with similar SIT-like characteristics. Wong *et al.* [7]–[9] later demonstrated the first current aperture vertical electron transistor (CAVET), which exhibited transistor-like behavior but was hindered by significant off-state leakage due to a diffused current-blocking layer.

The field saw a transformative milestone in 2018 when Hu *et al.* [10] presented the first enhancement-mode single-fin vertical FinFET, achieving a breakdown voltage exceeding 1 kV. This marked a shift toward true transistor-like operation with robust high-voltage performance. Li *et al.* [3] subsequently advanced the technology with an enhancement-mode multi-fin vertical FinFET, achieving an impressive breakdown voltage of 2.6 kV, underscoring the potential of β -Ga₂O₃ for high-power applications.

Since then, various research groups have proposed and demonstrated innovative vertical transistor designs [11]–[19]. These developments continue to push the boundaries of β -Ga₂O₃ technology, promising breakthroughs for applications requiring both high voltage and high current capabilities.

7.3 Charge Control to Achieve Normally off Operation in Unipolar Power FinFETs

For power transistors, normally-off (or enhancement-mode) operation is highly favored to ensure fail-safe performance. In the event of gate control failure, such as a malfunction in the gate driver, the transistor must block the high supply voltage to prevent catastrophic damage. If the transistor lacks normally-off operation, the failure to block the supply voltage would lead to the destruction of the entire circuit and potentially cause severe damage to the connected load, often large-scale utilities. Hence, ensuring normally-off behavior is critical for the reliable and safe operation of power systems.

To ensure this behavior, a vertical FinFET structure is employed in this work, as illustrated

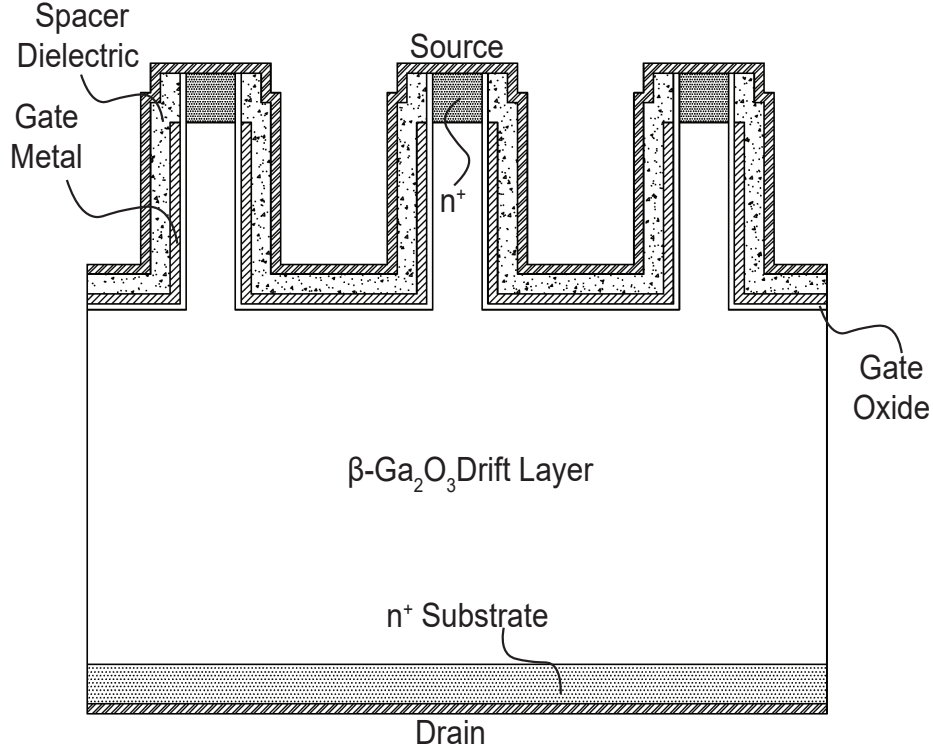


Figure 7.1: Schematic diagram of a unipolar vertical FinFET structure

in Fig. 7.1, where the gate controls the channel through the sidewalls of the fins. A high-quality gate insulator is essential to minimize gate leakage and avoid threshold voltage instability due to interface traps. In this structure, the work function difference between the gate metal and $\beta\text{-Ga}_2\text{O}_3$ depletes the channel region at zero gate bias. This causes the energy band of $\beta\text{-Ga}_2\text{O}_3$ to bend upward, creating a dipole charge across the insulator, resulting in a built-in potential. If the channel width (W_{fin}) is sufficiently small, the channel becomes fully depleted, ensuring that no current flows at zero bias.

As the gate-source voltage (V_{GS}) increases, the depletion region shrinks, and the channel begins to open. When the potential across the structure reaches zero, the energy bands become flat, and the flat-band voltage (V_{FB}) is defined by the following equation:

$$qV_{FB} = \phi_m - \phi_{Ga_2O_3} = -qV_{bi} \quad (7.1)$$

where ϕ_m and $\phi_{Ga_2O_3}$ represent the work functions of the gate metal and $\beta\text{-Ga}_2\text{O}_3$, respectively and V_{bi} is the built-in potential. Beyond the flat-band voltage, increasing V_{GS} further

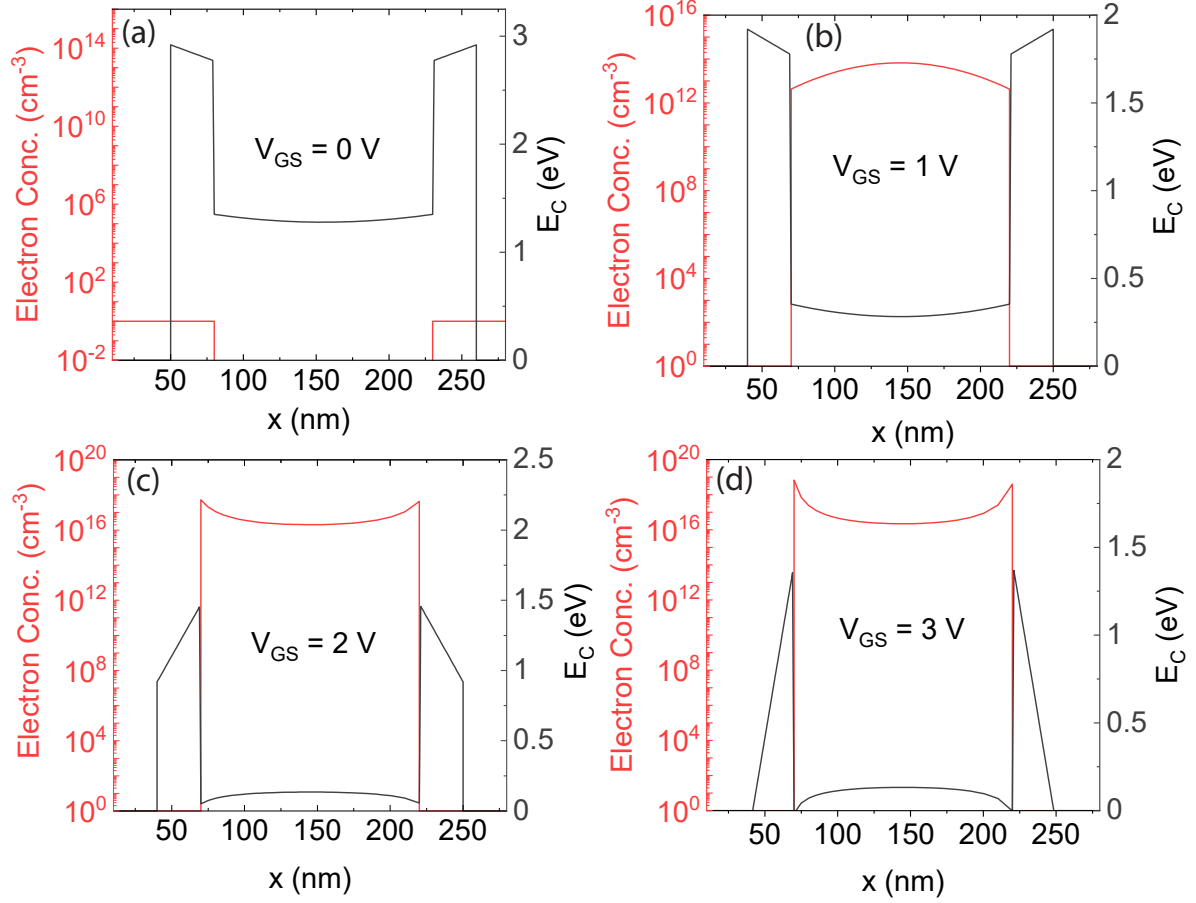


Figure 7.2: Band diagrams and electron concentration in the channel for power FinFET under (a) $V_{GS} = 0$ V, (b) $V_{GS} = 1$ V, (c) $V_{GS} = 2$ V, and (d) $V_{GS} = 3$ V.

causes electrons to accumulate at the dielectric interface.

Power FinFETs operate in three distinct regimes during the on-state:

1. Subthreshold regime: $V_{GS} < V_{th}$
2. Depletion regime: $V_{th} < V_{GS} < V_{FB}$
3. Accumulation regime: $V_{GS} > V_{FB}$

The electrostatics of the power FinFET, similar to that of a MOS structure, is governed by the following relationship:

$$V_{GS} = V_{FB} + \phi_S + V_{ox} \quad (7.2)$$

where ϕ_S is the surface potential and V_{ox} is the potential drop across the gate dielectric. The value of V_{ox} can be calculated as:

$$V_{ox} = \frac{Q_{Ga_2O_3}}{C_{ox}} = \frac{qN_D x_d}{C_{ox}} \quad (7.3)$$

Here, $Q_{Ga_2O_3} = qN_D x_d$ represents the charge in the fin region, where N_D is the doping concentration in the channel region, x_d is the depletion depth, which is a function of the surface potential, and C_{ox} is the oxide capacitance. The next subsection provides a detailed explanation of the transistor's operation within each regime.

7.3.1 Depletion Regime

In the depletion regime, as the gate-source voltage (V_{GS}) increases, the depletion region contracts, and the channel begins to open. The depletion width (x_d) can be determined from the surface potential (ϕ_S) using the following equation:

$$x_d = \sqrt{\frac{2\epsilon_{Ga_2O_3} \phi_S}{qN_D}} \quad (7.4)$$

where $\epsilon_{Ga_2O_3}$ is the permittivity of β -Ga₂O₃. From (7.3), the oxide voltage (V_{ox}) can be expressed as:

$$V_{ox} = \frac{\sqrt{2\epsilon_{Ga_2O_3} qN_D \phi_S}}{C_{ox}} \quad (7.5)$$

Using the value of V_{ox} from equations (7.2) and (7.5), the depletion width x_d can be derived from equation (7.4) as:

$$x_d = \frac{\epsilon_{Ga_2O_3}}{C_{ox}} \left(\sqrt{1 + \frac{2C_{ox}^2 (V_{FB} - V_{GS})}{q\epsilon_{Ga_2O_3} N_D}} - 1 \right) \quad (7.6)$$

We can define a body factor (γ), similar to a MOSFET, as:

$$\gamma = \frac{2q\epsilon_{Ga_2O_3} N_D}{C_{ox}} \quad (7.7)$$

Now, the depletion width x_d can be expressed in terms of γ :

$$x_d = \frac{\epsilon_{Ga_2O_3}}{C_{ox}} \left(\sqrt{1 + \frac{4(V_{FB} - V_{GS})}{\gamma^2}} - 1 \right) \quad (7.8)$$

For a typical power FinFET, the body factor γ is usually very small, meaning $\frac{1}{\gamma^2} \gg 1$. Therefore, x_d can be approximated as:

$$x_d = \frac{\epsilon_{Ga_2O_3}}{C_{ox}} \left(\frac{2\sqrt{V_{FB} - V_{GS}}}{\gamma} \right) = \sqrt{\frac{2\epsilon_{Ga_2O_3}(V_{FB} - V_{GS})}{qN_D}} \quad (7.9)$$

Equation (7.9) establishes the relationship between the depletion width (x_d) and the gate voltage (V_{GS}), which can be used to estimate the one-sided depletion width. For enhancement-mode operation, the channel width must satisfy $W_{fin} < 2x_d$.

The gate bias required to fully pinch off the channel (V_P) in a power FinFET with channel width W_{fin} is given by:

$$V_P = \frac{qN_D W_{fin}^2}{8\epsilon_{Ga_2O_3}} \quad (7.10)$$

The depletion width in the fin region is usually uniform at zero drain bias and some positive gate bias. As the gate bias decreases, the depletion region extends until the channel is completely depleted. When a positive drain bias is applied, the depletion region grows larger near the drain side due to the increased potential difference between the gate and drain, similar to a MOSFET. The channel begins to pinch off at the drain side once the drain voltage reaches $V_{DS,sat}$, after which the drain current remains constant, even as the drain voltage continues to increase. This is known as the saturation region.

Assuming the gradual channel approximation, the current-voltage relationship for the power FinFET can be expressed as:

$$I_D = \frac{q\mu_n N_D N_{fin} Z W_{fin}}{L_G} \left(V_{DS} - \frac{4}{3} \sqrt{\frac{2\epsilon_{Ga_2O_3}}{qN_D W_{fin}^2}} \left((V_{DS} + V_{bi} - V_{GS})^{\frac{3}{2}} - (V_{bi} - V_{GS})^{\frac{3}{2}} \right) \right) \quad (7.11)$$

where L_G is the length of the fin-channel, N_{fin} is the number of fins, and Z represents the width of the device. Using the expression for V_P from (7.10), equation (7.11) can be rewritten as:

$$I_D = \frac{q\mu_n N_D N_{fin} Z W_{fin}}{L_G} \left(V_{DS} - \frac{2}{3\sqrt{V_P}} \left((V_{DS} + V_{bi} - V_{GS})^{\frac{3}{2}} - (V_{bi} - V_{GS})^{\frac{3}{2}} \right) \right) \quad (7.12)$$

When $V_{DS} \ll (V_{bi} - V_{GS})$, applying Taylor's expansion simplifies (7.12) to:

$$I_D = \frac{q\mu_n N_D N_{fin} Z W_{fin}}{L_G} \left(1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_P}} \right) V_{DS} \quad (7.13)$$

Equation (7.13) describes the drain current in the linear regime of the power FinFET. The on-resistance (R_{on}) of the device can be derived by taking $\left(\frac{dV_{DS}}{dI_D} \right)$, resulting in:

$$R_{on} = \frac{L_G}{q\mu_n N_D Z W_{fin}} \left(1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_P}} \right)^{-1} \quad (7.14)$$

At saturation, the drain voltage is given by:

$$V_{DS,sat} = V_{GS} - V_{th} \quad (7.15)$$

where $V_{th} = V_{bi} - V_P$. Substituting this into (7.13), the saturation drain current becomes:

$$I_{D,sat} = \frac{q\mu_n N_D N_{fin} Z W_{fin}}{L_G} \left(\frac{1}{3} V_P + V_{GS} - V_{bi} + \frac{2(V_{bi} - V_{GS})^{\frac{3}{2}}}{3V_P^{\frac{1}{2}}} \right) \quad (7.16)$$

7.3.2 Accumulation Regime

When V_{GS} exceeds V_{FB} , accumulation occurs as an electron layer forms near the oxide interface. The resulting current has two primary components: the accumulation electron current and the channel current, which can be modeled using equations (7.13) and (7.14). The accumulation electron density, which directly impacts the current flow, is expressed as:

$$n_{acc} = C_{ox}(V_{GS} - V_{FB}) \quad (7.17)$$

This behavior closely mirrors the MOSFET's operation above the threshold voltage. As such, the IV characteristics typically used for MOSFETs can be applied to estimate the accumulation current. In the linear regime, the total current, considering both the accumulation and channel components, is given by:

$$I_{D,acc} = \frac{\mu_n C_{ox} N_{fin} Z W_{fin}}{L_G} \left((V_{GS} - V_{bi}) V_{DS} - \frac{V_{DS}^2}{2} \right) + \frac{q \mu_n N_D N_{fin} Z W_{fin}}{L_G} \left(V_{DS} + \frac{2V_{DS}^{\frac{3}{2}}}{3V_P^{\frac{1}{2}}} \right) \quad (7.18)$$

As the drain voltage increases, the accumulation current saturates when $V_{DS} > V_{GS} - V_{bi}$, and the saturated accumulation current is expressed as:

$$I_{D,acc-sat} = \frac{\mu_n C_{ox} N_{fin} Z W_{fin}}{L_G} (V_{GS} - V_{bi})^2 + \frac{q \mu_n N_D N_{fin} Z W_{fin}}{3L_G} V_P \quad (7.19)$$

This analysis provides a comprehensive understanding of how the accumulation and channel currents contribute to the overall current flow in power FinFETs, particularly in the accumulation regime. The derived relationships allow for an approximate prediction of device performance under varying gate and drain voltages.

Channel Length Modulation

Once V_{DS} exceeds $V_{DS,sat}$, the drain side of the channel becomes fully depleted. Any further increase in V_{DS} no longer contributes to a potential rise across the channel. Instead, it extends the pinch-off region toward the source, effectively reducing the channel length. This phenomenon, known as channel length modulation, results in a finite output conductance, which can be expressed as:

$$g_D = \frac{I_{DS}}{\pi(V_{DS} - V_{DS,sat})} \left(\frac{W_{fin}}{L_G} \right) \quad (7.20)$$

7.3.3 Subthreshold Regime

In the subthreshold regime, the channel remains fully depleted due to the work-function difference between the gate metal and the semiconductor. This regime is critical for power transistors, as the leakage current at $V_{GS} = 0$ directly impacts power loss. Carrier transport in this region is primarily governed by electron density in the depletion region, where the electron density within the channel is determined by the shape of the conduction energy band. The volumetric electron density at height y (in the vertical direction) in the channel follows an exponential relationship with the surface potential $\phi_S(y)$, as given by:

$$n(y) \propto \exp\left(\frac{q\phi_S(y)}{k_B T}\right) \quad (7.21)$$

where k_B is the Boltzmann constant and T is the temperature. The surface potential at the source side, $\phi_{S,\text{source}}$, is derived from the oxide and body capacitor model:

$$\phi_{S,\text{source}} \propto (V_{FB} - V_{GS}) \quad (7.22)$$

Similarly, the surface potential at the drain side, $\phi_{S,\text{drain}}$, is expressed as:

$$\phi_{S,\text{drain}} \propto (V_{DS} + V_{FB} - V_{GS}) \quad (7.23)$$

The difference in electron density between the drain and source sides of the channel drives electron diffusion, resulting in subthreshold current. This current can be described by:

$$I_D \propto \frac{dn(y)}{dy} = \frac{n_{\text{source}} - n_{\text{drain}}}{L_G} \propto \exp\left(-\frac{q(V_{bi} - V_{GS})}{k_B T}\right) \left(1 - \exp\left(-\frac{qV_{DS}}{k_B T}\right)\right) \quad (7.24)$$

As a result, power FinFETs with narrower fin widths exhibit a smaller subthreshold slope.

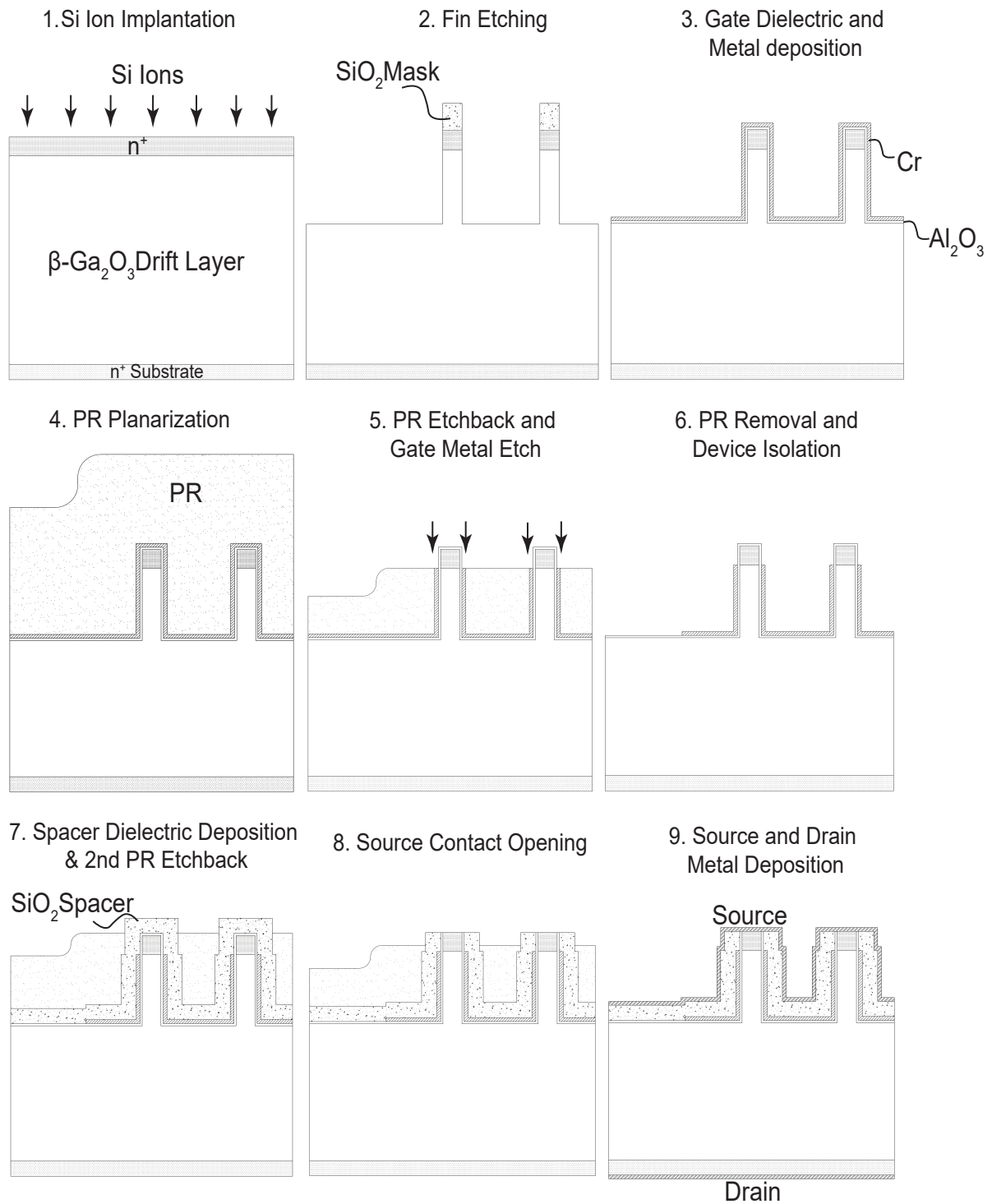


Figure 7.3: Fabrication process flow of vertical $\beta\text{-Ga}_2\text{O}_3$ power FinFET.

7.4 Fabrication of β -Ga₂O₃ Vertical Power FinFETs

The fabrication of power FinFETs presents several key challenges: fin etching, gate metal formation, and source-gate isolation. Achieving vertical or near-vertical sidewalls during the etching process is crucial to ensure that the effective channel width at the base of the fin matches the design specifications, while minimizing sidewall etch damage is essential for maintaining device performance. The gate metal must adequately cover the channel region without extending over the highly doped cap layer. Additionally, given the sub-micron scale of the channel width, precise control is required to prevent the source contact from making any contact with the gate metal.

The overall process flow for fabricating the β -Ga₂O₃ power FinFET is illustrated in Fig. 7.3. Each step is explained in detail in the following subsections.

7.4.1 Si Ion Implantation

The fabrication process began with silicon (Si) implantation at Kroko Inc. on the β -Ga₂O₃ HVPE wafer's top surface, featuring a doping concentration of $N_D = 10^{16} \text{ cm}^{-3}$ on a (001) Sn-doped conductive substrate sourced from NCT Japan. A 25 nm SiO₂ layer served as the implantation mask. To achieve a box profile with a Si concentration $\sim 5 \times 10^{19} \text{ cm}^{-3}$, SRIM simulations were conducted using five distinct Si doses and energies, as shown in Fig. 7.4(a).

Following implantation, activation annealing of the implanted layer was carried out at 925 °C in an N₂ environment under two different pressure conditions. One annealing process was conducted in a rapid thermal annealing (RTA) chamber at atmospheric pressure (760 Torr), while the other was performed in a MOCVD chamber at a reduced pressure of 100 Torr. Secondary Ion Mass Spectroscopy (SIMS) results showed that Si diffused up to 800 nm into the drift layer under atmospheric pressure annealing, diluting the n^+ concentration to approximately $1.5 \times 10^{19} \text{ cm}^{-3}$, as illustrated in Fig. 7.4(b). In contrast, the 100 Torr annealed sample retained a more defined box profile, with Si diffusion limited to 300 nm and the n^+ region concentration

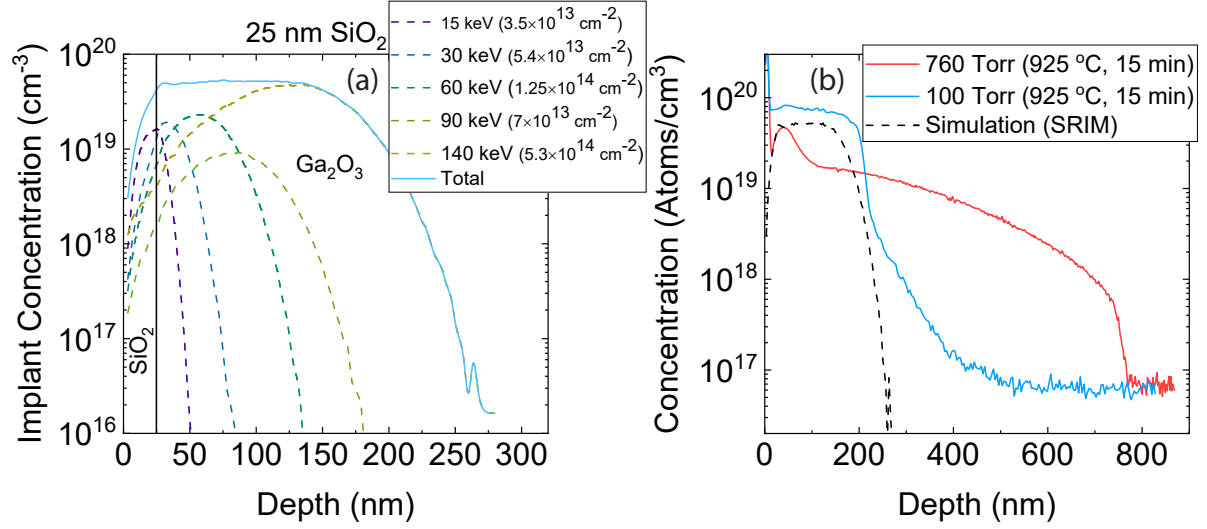


Figure 7.4: (a) SRIM simulation of the Si-implanted profile on β -Ga₂O₃ at five different Si doses and implant energies. (b) SIMS profile of the implant activation annealed samples under two different pressure conditions.

maintained at approximately $7 \times 10^{19} \text{ cm}^{-3}$. Consequently, the low-pressure annealed sample was selected for all vertical FinFET devices.

7.4.2 Fin Etching

Hard Mask Formation

After Si implantation and the SiO₂ mask removal, the creation of fins through dry etching is performed. Given the sub-micron channel length, Electron-Beam Lithography (EBL) is employed for precision patterning. To achieve a sufficient aspect ratio (L_G/W_{fin}), a deep etch of approximately one micron is necessary. An aspect ratio greater than 2 is critical for ensuring transistor-like behavior and avoiding triode-like characteristics. For such deep etching, the use of a hard mask is essential to achieve the required etch selectivity between the mask and β -Ga₂O₃, as EBL photoresists are typically thin and exhibit poor etch resistance.

The hard mask can be fabricated through either lift-off of metals using the EBL resist or by directly etching a hard mask with the EBL resist. However, the lift-off process introduces significant challenges, particularly for densely packed submicron fins, and often results in low yield. To address this, a multilayered hard-mask approach is developed, utilizing the latter

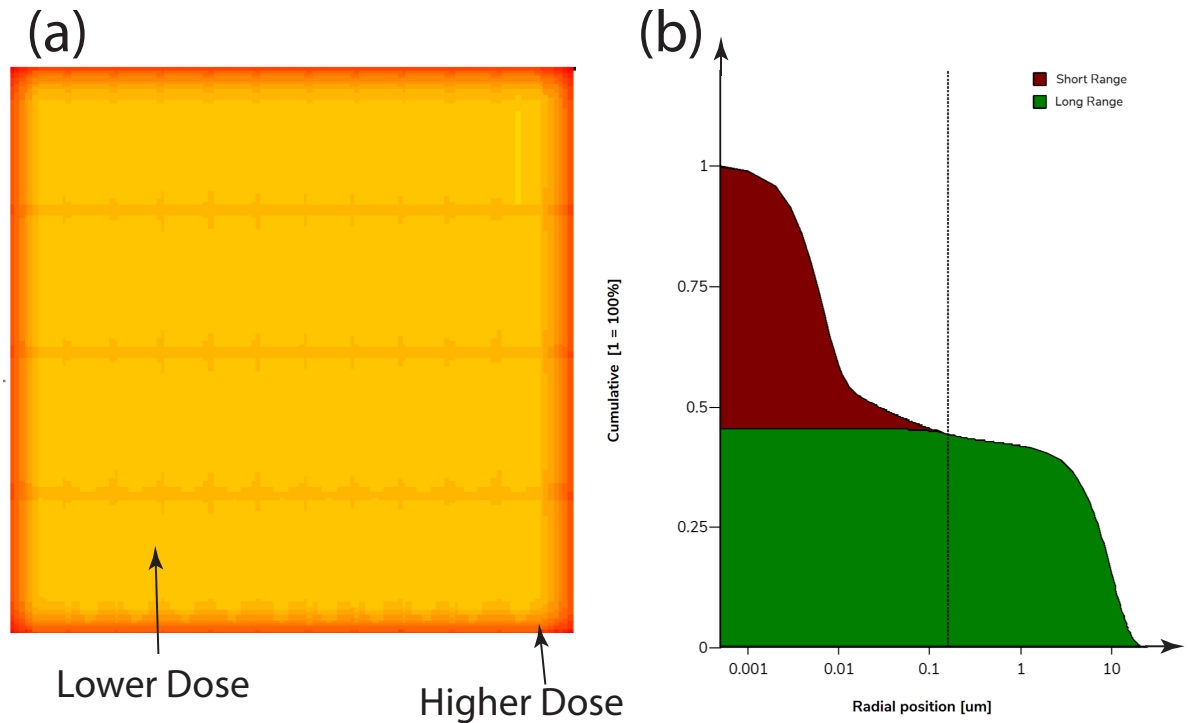


Figure 7.5: (a) Dose distribution using proximity effect correction (PEC) across the device (b) Gaussian distribution profile of doses along radial direction for the specific mask material.

technique to effectively create the submicron fins with higher precision and better process reliability.

In this approach, a multilayer hard mask comprising $\text{SiO}_2/\text{Ru}/\text{SiO}_2$ is employed. The process begins with the deposition of a 700 nm thick SiO_2 layer on top of $\beta\text{-Ga}_2\text{O}_3$ using plasma-enhanced chemical vapor deposition (PECVD). Next, a 20 nm layer of ruthenium (Ru) is deposited via DC sputtering, with a thin interfacial layer of titanium (Ti) to enhance adhesion between Ru and SiO_2 . Finally, a 5 nm SiO_2 layer is added using atomic layer deposition (ALD), completing the hard-mask structure. This multilayered approach provides robust etch resistance, essential for accurately patterning the submicron fins with improved precision and process reliability.

Proximity Effect Correction (PEC)

When electrons in the electron-beam lithography (EBL) system interact with the e-beam resist, they undergo various scattering events, including backscattering from the substrate and the

resist surface. This phenomenon, known as the proximity effect, limits the ultimate resolution of e-beam writing. The proximity effect becomes more pronounced when dealing with dense patterns like transistor fins, as the scattered electrons can expose unintended areas, leading to distortions in the pattern. To mitigate this, proximity effect correction (PEC) is applied using the Beamer software, as illustrated in Fig. 7.5 (a). The backscattering proximity effect is modeled as a Gaussian distribution, shown in Fig. 7.5 (b), to accurately predict and correct the exposure dosage across the pattern.

Electron Beam Lithography

After depositing the SiO₂(700 nm)/Ru(20 nm)/SiO₂(5 nm) hard mask, a layer of negative-tone ma-N 2403 resist is spin-coated onto the sample, followed by a soft bake at 100 °C for 1 minute. The sample is then exposed using the JEOL JBX 6300FS electron beam lithography system, operating at an acceleration voltage of 100 kV to create 200 nm wide fins. To ensure precise pattern transfer, Proximity Effect Correction (PEC) is applied during the exposure process. The base exposure dose used for the lithography was 500 $\mu\text{C}/\text{cm}^2$, optimized for the given resist and pattern density.

Hard Mask Etching

The patterned sample is subsequently transferred to a Panasonic ICP etching system for the precise etching of the hard mask layers. First, the 5 nm SiO₂ layer is etched using a CHF₃/CF₄ plasma. Following this, the 20 nm Ru layer is etched using an O₂/Cl₂ plasma, with the 5 nm SiO₂ serving as a protective mask during this step. A laser etch monitor is employed during the Ru etch to track the etch rate and ensure precise termination of the etching process. Finally, the 700 nm SiO₂ layer is etched using the Ru layer as a hard mask in a CHF₃/CF₄ plasma as shown in Fig. 7.6.

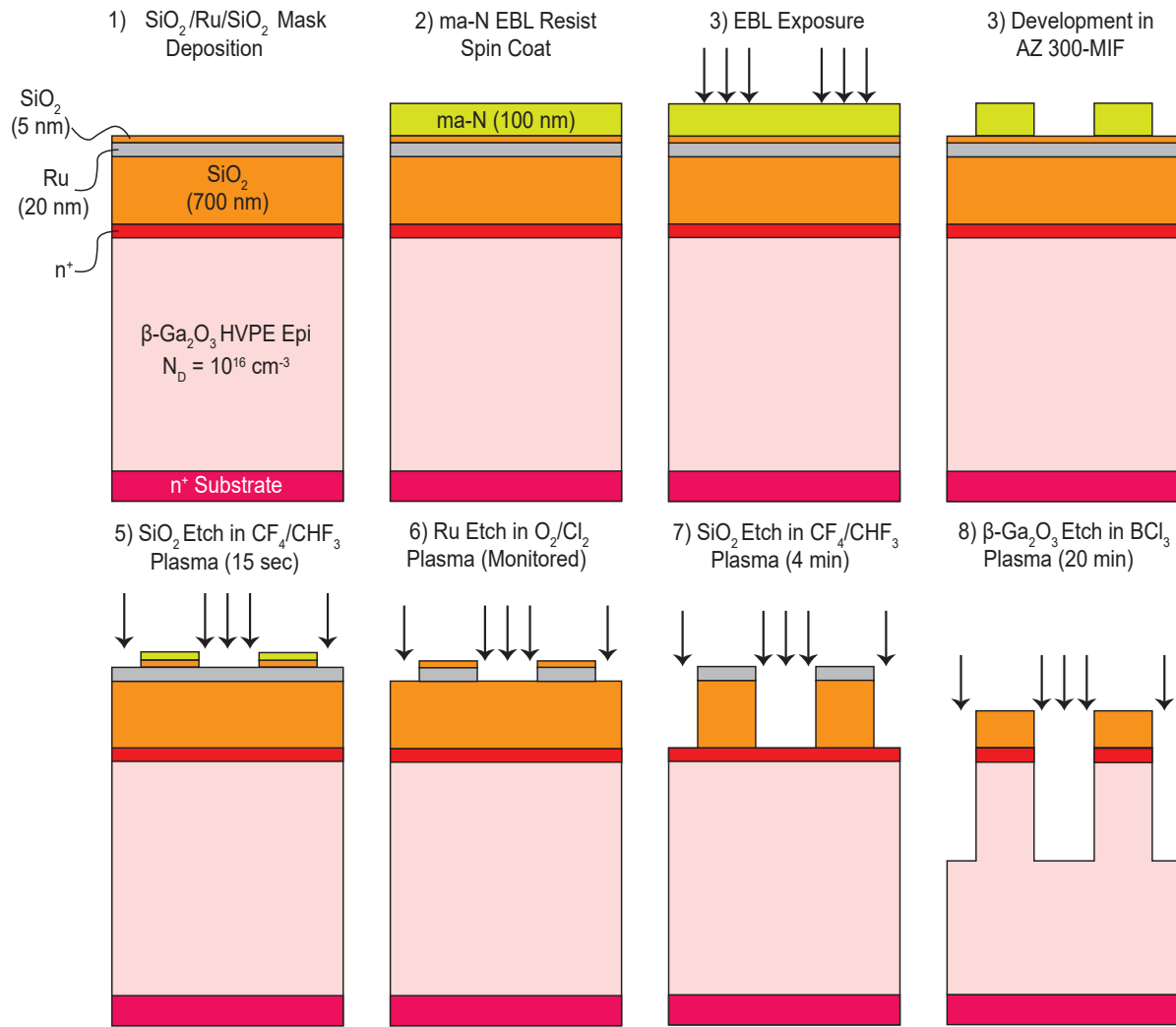


Figure 7.6: Hard mask deposition and etching of $\beta\text{-Ga}_2\text{O}_3$ for fin formation.

$\beta\text{-Ga}_2\text{O}_3$ Etching

The patterned $\beta\text{-Ga}_2\text{O}_3$ sample is etched using the previously deposited and patterned hard mask in a BCl_3 plasma, with an etch duration of 20 minutes and an etch rate of approximately 50 nm/min. After completing the fin etching, the samples are immersed in HF for 20 minutes to remove the hard mask and mitigate any dry etch-induced damage. This is followed by a 15-minute dip in HCl to further cleanse the surface. The complete etching process including the hard mask etching is illustrated in Fig. 7.6 The specific etching parameters for each step are detailed in Table 7.1.

Table 7.1: Etching Parameters for Different Layers

Layer	Etch Gas	Flow Rate (sccm)	ICP Power (W)	Bias Power (W)	Pressure (mT)	Etch Duration (sec)
SiO ₂ (5 nm)	CHF ₃ /CF ₄	10/30	900	50	3.75	15
Ru (20 nm)	O ₂ /Cl ₂	49.5/5.5	500	50	18.7	Monitored
SiO ₂ (5 nm)	CHF ₃ /CF ₄	10/30	900	50	3.75	300
β -Ga ₂ O ₃ (1 μ m)	BCl ₃	30	300	50	3	1200

7.4.3 Gate Oxide and Gate Metal Deposition

Following fin formation, a 35 nm layer of Al₂O₃ is deposited as the gate oxide using an Oxford FlexAL atomic layer deposition (ALD) system. The ALD process utilizes H₂O and Trimethylaluminum (TMA) as precursors, with the reaction occurring at 300°C without a plasma precleaning step. Due to the self-limiting nature of ALD, the gate dielectric exhibits excellent conformality, achieving uniform thickness both on the fin sidewalls and on flat surfaces.

The gate metal is deposited immediately after the gate dielectric. To ensure adequate sidewall coverage on the fins, sputtering is preferred over e-beam evaporation. The threshold voltage of the FinFET is influenced by the work function of the gate metal, as expressed in Equation (7.1). The selected metal must have a high work function to achieve the desired threshold voltage and must also be compatible with dry-etching processes. Suitable options include Molybdenum (Mo), Chromium (Cr), Ruthenium (Ru), and Tungsten (W). Although metals with higher work functions, like Nickel (Ni) and Platinum (Pt), could further increase the threshold voltage, they are not dry-etchable due to poor selectivity with most photoresists. For the first-generation device, Chromium (Cr) was selected as the gate metal, offering a work function of 4.5 eV while meeting the process requirements.

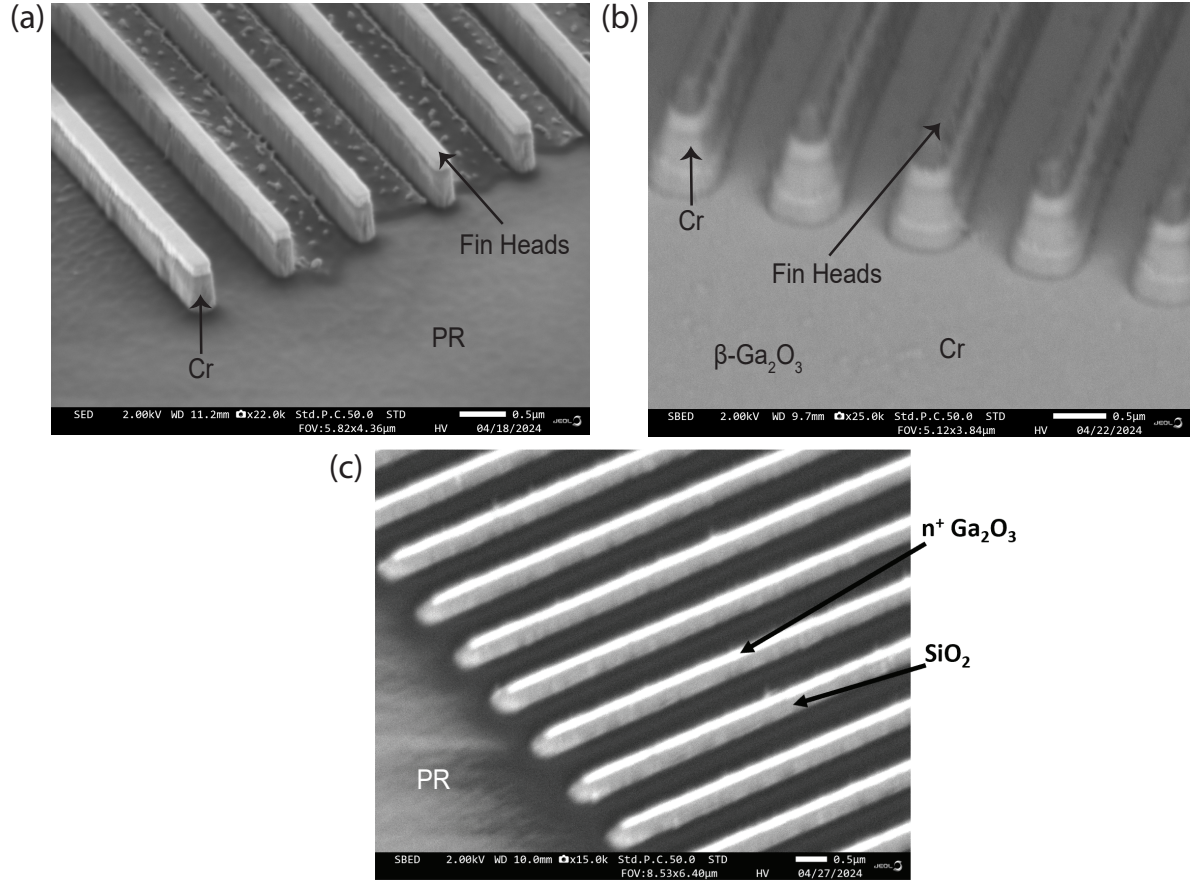


Figure 7.7: SEM images of fins (a) after planarization etchback and Cr etch, (b) after planarization etchback and Cr etch with PR removed, and (d) after spacer dielectric etch to open source contacts.

7.4.4 Gate Formation

At this stage, the gate metal (Cr) covers the entire fin structure, including both the sidewalls and the n^+ source regions. The gate metal over the n^+ source region must be etched away to prevent shorting between the source and gate electrodes. Given the 200 nm width of the fins, conventional aligned lithography is impractical for this purpose; instead, a self-aligned process is employed. A 2.2 μm thick layer of photoresist is spun onto the wafer, followed by a timed dry etch in an O_2 plasma to expose the fin top and sidewalls of the n^+ source region of the fins. This approach allows for precise control of the gate-fin overlap L_g , determined by the remaining thickness of the photoresist. After the photoresist is selectively etched to reveal the tops of the fins, the Cr is etched from the fin heads and the n^+ sidewalls using a Cl_2/O_2 plasma as shown in the SEM images of Fig. 7.7 (a) and (b).

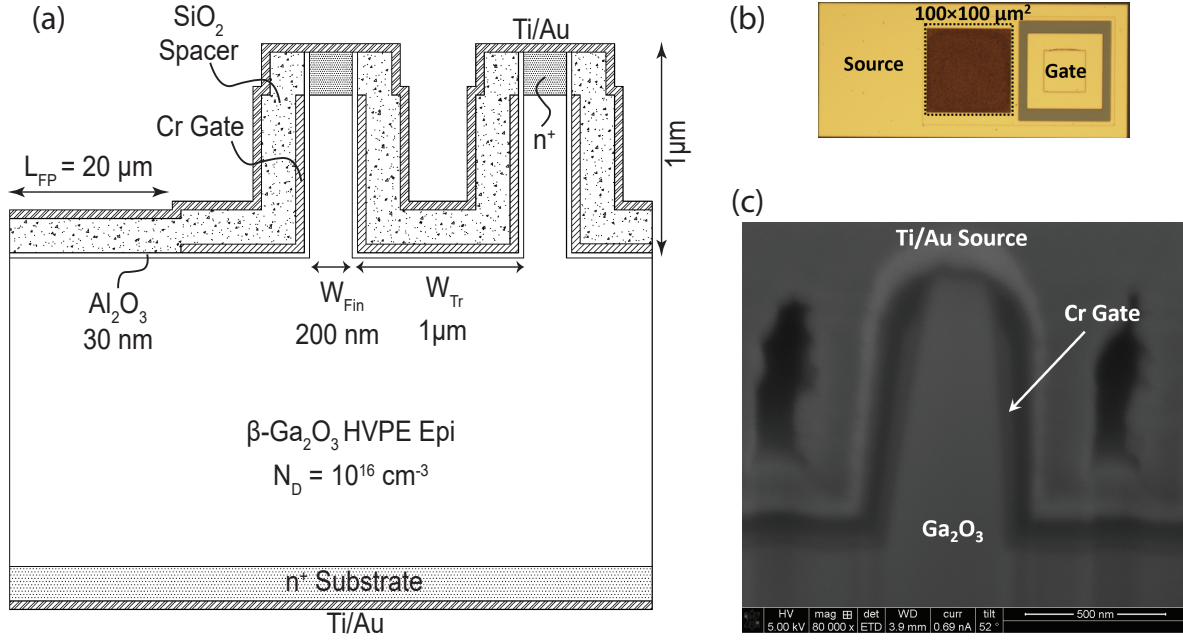


Figure 7.8: (a) Final Fabricated Structure of the β -Ga₂O₃ Vertical Power FinFET (b) Top view microscope image and (c) cross-sectional SEM image of the fabricated β -Ga₂O₃ vertical FinFET.

7.4.5 Dielectric Spacer

With the fin width less than $0.3 \mu\text{m}$, precise placement of the source metal solely on top of the fin using aligned lithography is impractical. Instead, a “self-aligned” process is employed to form the source contact without requiring fine alignment, necessitating isolation between the gate and source metal. Following gate formation, a 150 nm layer of SiO₂ is deposited on the wafer using plasma-enhanced chemical vapor deposition (PECVD), creating a dielectric spacer that isolates the gate from the source. The gate is now fully encapsulated in SiO₂.

7.4.6 Source and Drain Formation

Following the deposition of the spacer dielectric, a similar etch process is performed to expose the fin tops, as previously done for the gate. A $2.2 \mu\text{m}$ thick layer of photoresist is spun onto the wafer, followed by a timed dry etch in an O₂ plasma to selectively reveal only the tops of the fins. Once the photoresist has been etched back to expose the fin heads, the SiO₂ spacer and Al₂O₃ gate dielectric are etched sequentially from the fin tops using a CF₄/CHF₃ plasma and a

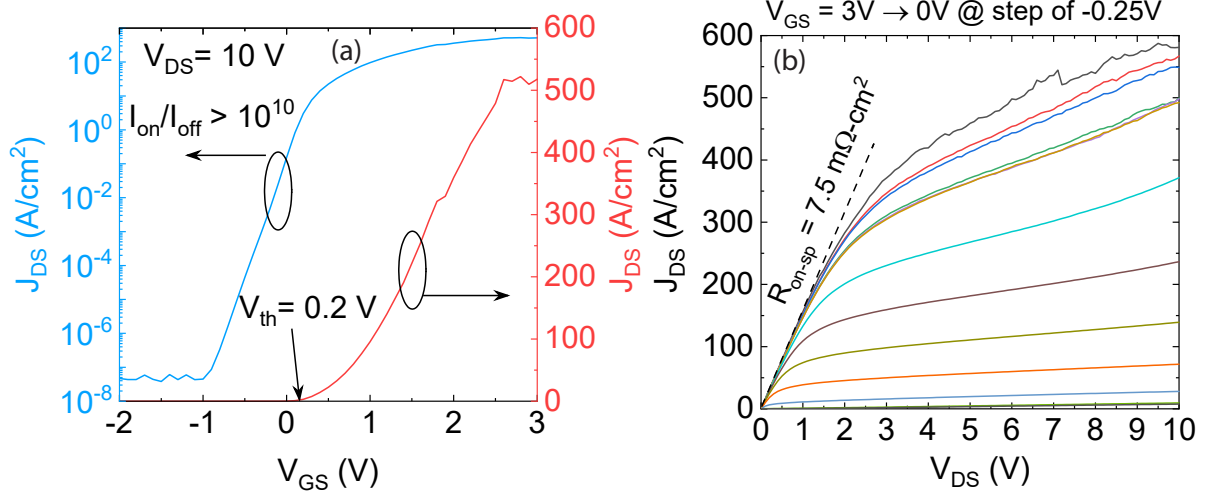


Figure 7.9: (a) Transfer and (b) output characteristics of the fabricated β -Ga₂O₃ vertical FinFET.

BCl₃ plasma, respectively, exposing the n⁺ region at the fin tops as shown in the SEM image of Fig. 7.7 (c).

To establish the source contact, 50/200 nm of Ti/Au is then deposited on the exposed fin tops through a lift-off process using e-beam evaporation with planetary rotation to ensure uniform sidewall coverage. Following this, another 50/200 nm of Ti/Au is blanket-deposited on the backside of the wafer to form the drain contact. No annealing of either the source or drain contact is performed.

The final structure with top view microscope image and a cross-sectional SEM image is shown in Fig. 7.8.

7.5 Current-Voltage Characteristics

The on-wafer transfer and output behavior characterization was performed using a Keithley 4200A-SCS Parameter Analyzer. The tested transistor was designed with fins of 100 μ m in length, a fin width of 200 nm, and a gate length (L_G) of 800 nm. Current density and on-resistance values were calculated based on the total area of the transistor, covering both the fin and trench regions.

The transfer characteristics of the fabricated FinFET are shown in Fig. 7.9 at $V_{DS} = 5$ V.

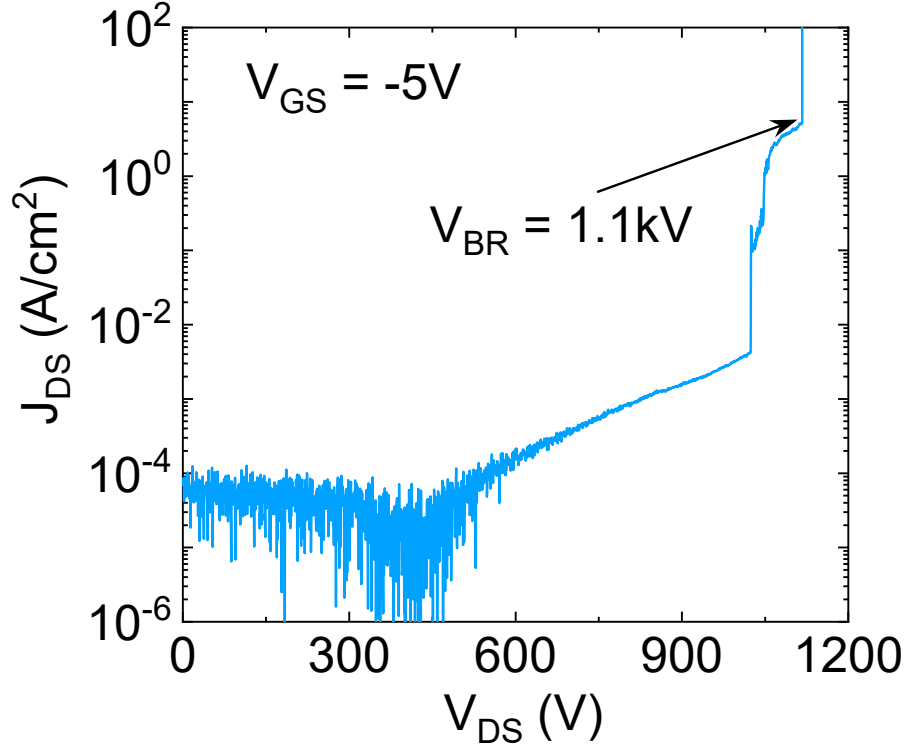


Figure 7.10: Off-state breakdown characteristics of the the fabricated β -Ga₂O₃ vertical FinFET ($100 \times 100 \mu\text{m}^2$).

These measurements indicate an I_{on}/I_{off} ratio exceeding 10^{10} and a gate leakage current below 10^{-6} A/cm^2 at $V_{GS} = 5 \text{ V}$. Gate leakage could be further reduced by improving the quality of the gate dielectric and minimizing the overlap between the gate and the n^+ region. The threshold voltage (V_{th}), determined by linearly extrapolating the J_D - V_{GS} plot in linear scale, is 0.2 V. A positive shift in V_{th} could be achieved by reducing the channel doping density, further narrowing the channel width, or using gate metals with a higher work function.

The output characteristics depicted in Fig. 7.9 reveal a specific on-resistance (R_{on-sp}) of $7.5 \text{ m}\Omega\text{-cm}^2$ based on the total device area, excluding the pad regions. When normalized to the active fin area alone, an impressive R_{on-sp} of $1.2 \text{ m}\Omega\text{-cm}^2$ is achieved, highlighting the efficiency of the design. The J_D versus V_{DS} curve in the linear regime exhibits a perfectly linear response, confirming the formation of excellent source/drain contacts without the necessity for high-temperature contact annealing, which is often a critical step in achieving optimal performance.

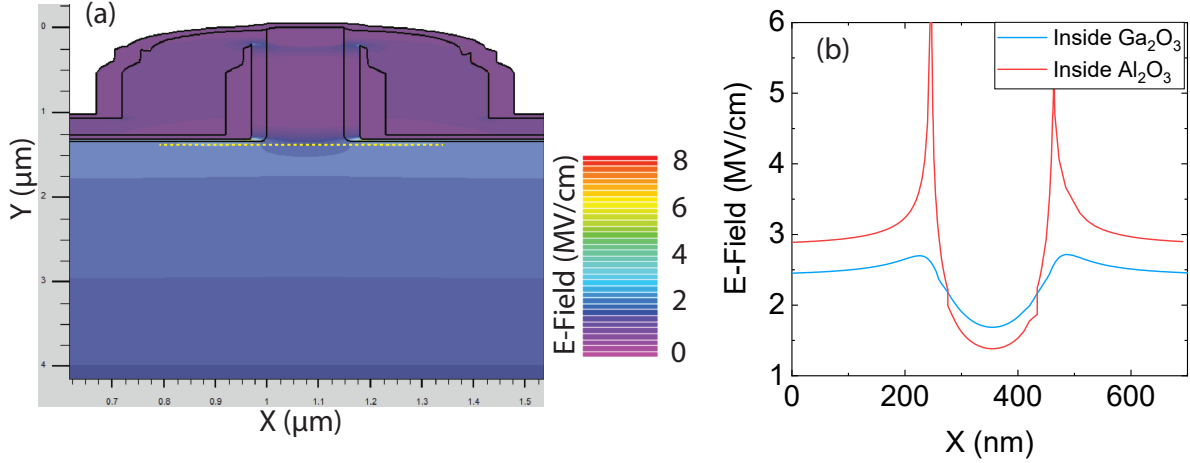


Figure 7.11: (a) Electric field contour plot of the β -Ga₂O₃ vertical power FinFET (b) Electric field profile along the cutline shown in Fig. 7.11 in β -Ga₂O₃ and in Al₂O₃. The simulation is performed at $V_{GS} = -5$ V and $V_{DS} = 1.2$ kV.

In Fig. 7.10, the off-state breakdown characteristics of the fabricated β -Ga₂O₃ FinFET are presented, measured at a gate-source voltage (V_{GS}) of -5 V using the Keysight B1505A Power Device Parameter Analyzer. The device achieves a breakdown voltage of 1.1 kV, accompanied by an impressively low leakage current of less than 10^{-4} A/cm², which aligns with the noise floor of the measurement tool. Furthermore, the TCAD simulation depicted in Fig. 7.11 reveals a peak electric field of 2.5 MV/cm within the β -Ga₂O₃ material. Notably, the peak electric field exceeds 6 MV/cm in the Al₂O₃ dielectric layer, indicating the potential onset of dielectric breakdown, a critical consideration for ensuring device reliability and long-term performance.

In conclusion, these results highlight the effectiveness of the fabricated β -Ga₂O₃ FinFET structure in achieving high I_{on}/I_{off} ratios, low gate leakage, stable threshold voltage, and minimal on-resistance. However, the observed breakdown voltage is constrained by the thin gate dielectric employed in this first-generation device. In the following section, we will discuss and demonstrate more advanced designs aimed at mitigating this limitation.

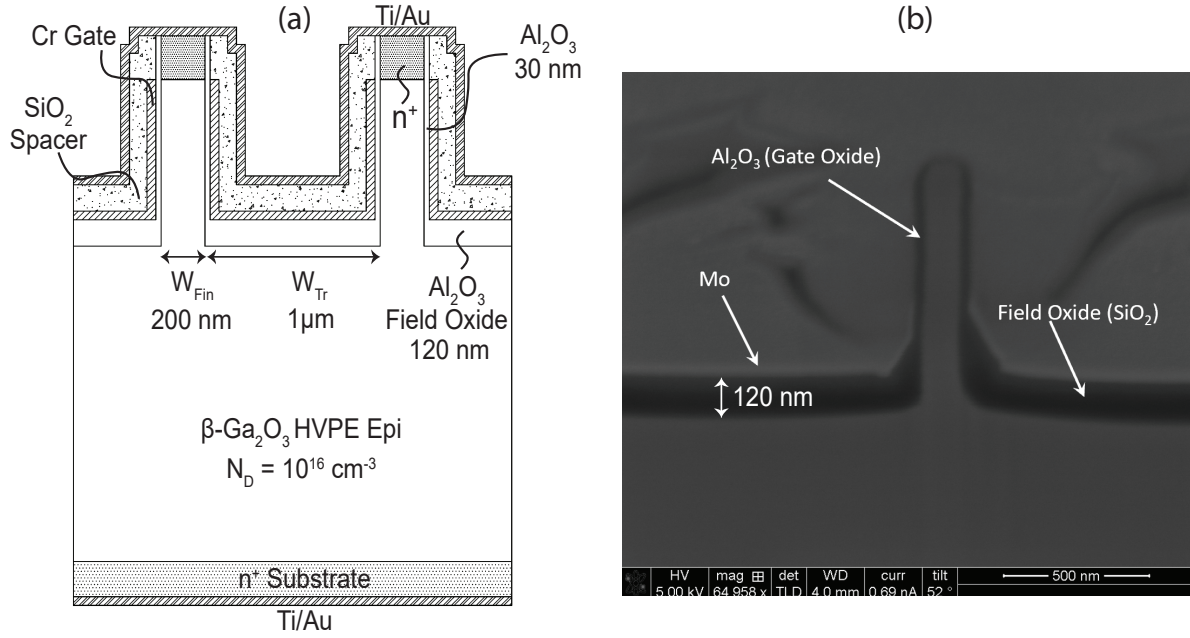


Figure 7.12: Schematic diagram of a vertical FinFET with Field Oxide layer.

7.6 Electric Field Engineering by Field Oxide Layer

As illustrated in Fig. 7.11 (a) and (b), the electric field exhibits significant peaks at the fin bases, which represent critical bottlenecks for the performance of power FinFETs. High electric field strengths at these locations can lead to premature breakdown of the device. To address this challenge, a 120 nm Al_2O_3 field oxide layer is strategically incorporated onto the trench regions, as depicted in the structural diagram shown in Fig. 7.12 (a). The introduction of this insulating layer is anticipated to alter the electric field distribution within the device. In this modified structure, the peak electric field at the transistor edge is expected to remain comparable to the value presented in Fig. 7.11. However, a notable reduction in the electric field peak near the fin base is anticipated, which indicates that the thicker Al_2O_3 insulating layer effectively mitigates the electric stress concentrated at this critical region, thereby enhancing device breakdown voltage.

The fabrication process for the Al_2O_3 field oxide layer is very carefully performed prior to the gate formation step. This step employs a technique analogous to that used for the source/gate spacer oxide, as illustrated in Fig. 7.3. Initially, the Al_2O_3 layer is deposited onto the drift layer

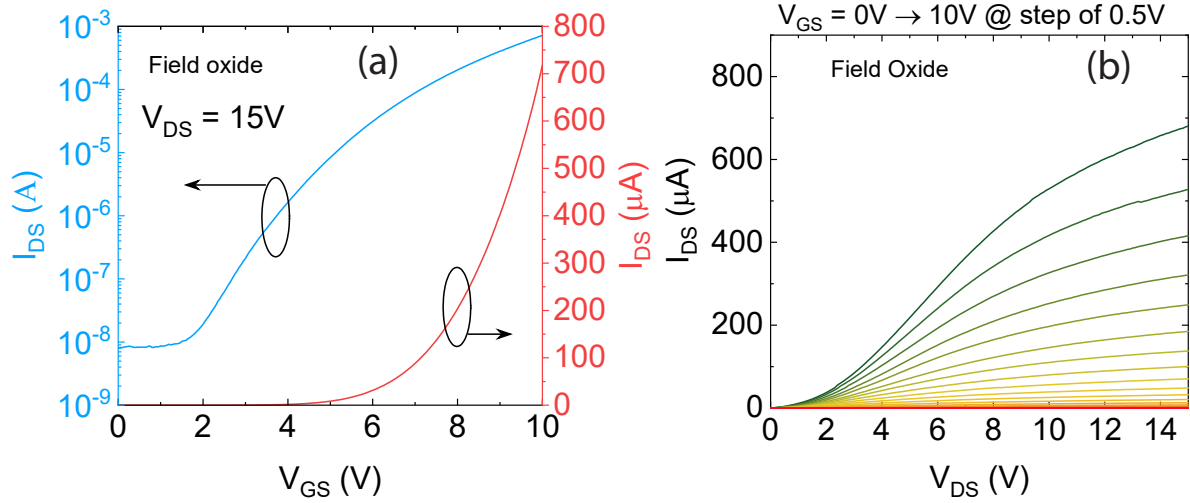


Figure 7.13: (a) Transfer and (b) output characteristics of the fabricated β -Ga₂O₃ vertical FinFET with field oxide.

using Atomic Layer Deposition (ALD), which guarantees uniform coverage over the trench regions. Following the deposition, photoresist planarization is performed and subsequently dry etched to selectively expose the sidewalls of the fins. After the etching of the photoresist, the sample undergoes a dip in Buffered Oxide Etch (BOE), effectively removing the oxide from the sidewalls of the fins. This step is essential to ensure that the fin sidewalls remain free from unwanted oxide residues, which could otherwise adversely affect the electrical performance of the devices.

The fins, following the etching process of the Al₂O₃ layer, are depicted in Fig. 7.12 (b). These images showcase the refined structures, which are now prepared for the subsequent processing steps similar to those illustrated in Fig. 7.3. However, it is noteworthy that the etching of the fins did not proceed as intended for the second-generation devices. As a result, the electrical performance of these devices exhibited degradation, highlighting the importance of meticulous fabrication techniques in achieving high-performance outcomes.

7.6.1 Current-Voltage Characteristics

The transfer characteristics of the fabricated $1 \times 1 \text{ mm}^2$ FinFET with a field oxide layer, illustrated in Fig. 7.13 (a), were measured under a drain-source voltage (V_{DS}) of 15 V. These devices

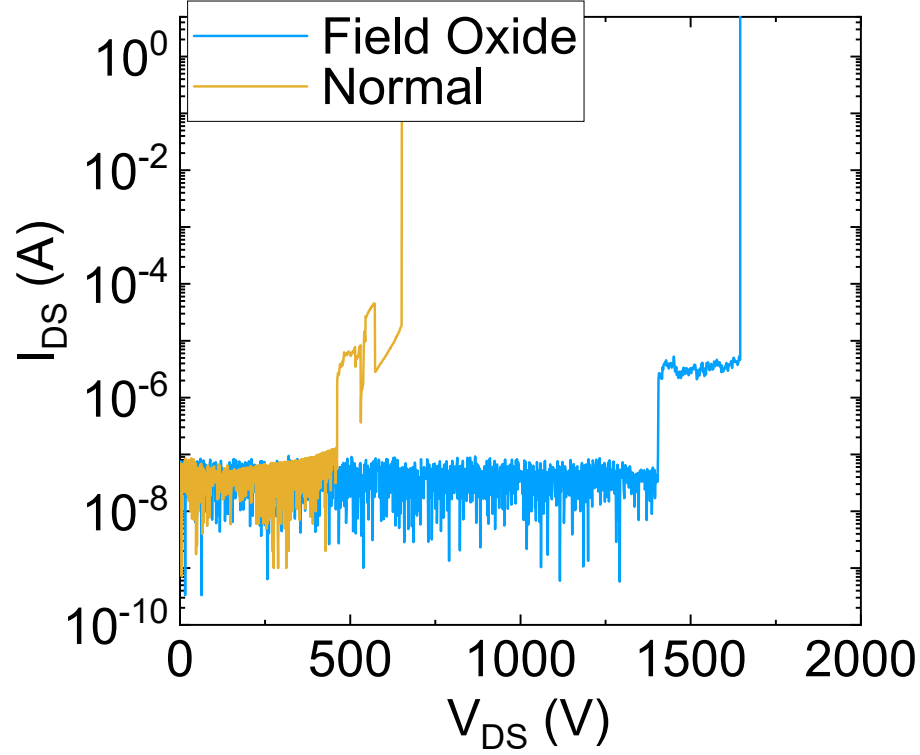


Figure 7.14: Off-state breakdown characteristics of the fabricated second generation β -Ga₂O₃ vertical FinFET with and without field oxide.

demonstrate a low on-current, below 1 mA, which can be attributed to fabrication challenges encountered during the fin etching process. Notably, the isotropic component of dry etching introduced structural irregularities, resulting in an hourglass-shaped profile of the fins and, in some cases, their complete breakage. Nevertheless, the devices exhibit a relatively high threshold voltage of approximately 4 V, which is likely a consequence of the reduced fin width achieved during etching.

The output characteristics, shown in Fig. 7.13 (b), further highlight the limitations of the current fabrication process. A substantial amount of contact resistance is evident, as indicated by the pronounced non-linear behavior near $V_{DS} = 0$ V. This observation underscores the importance of optimizing contact interfaces to enhance device performance. Furthermore, improving the dry etching process to produce uniformly vertical fins is crucial for realizing the full potential of these FinFET structures in practical applications.

The off-state breakdown characteristics for power FinFETs incorporating a field oxide

layer are depicted in Fig. 7.14. Notably, the breakdown voltage has improved to 1.7 kV, a significant enhancement compared to the 700 V observed in the devices without the field oxide. It is essential to highlight that these power FinFETs are of a larger area, measuring $1 \times 1 \text{ mm}^2$, in contrast to the earlier generation devices that measured only $100 \times 100 \text{ }\mu\text{m}^2$. This size difference plays a critical role in the observed performance metrics. In fact, the breakdown voltage of the vertical FinFETs without the field oxide has degraded from 1.1 kV in the first-generation devices to 700 V in the second-generation devices, which can be attributed to the killer defects in the HVPE epitaxial layer. Nevertheless, the substantial improvement in breakdown voltage—exceeding twofold—for the second-generation devices with the field oxide, when compared to their counterparts without it, demonstrates the effectiveness of the proposed method. This advancement indicates that the integration of the field oxide layer significantly contributes to the reliability and robustness of the power FinFET structure in high-voltage applications.

7.7 Switching Performance of Power FinFETs

A power switch requires both time and energy to transition between states. During the transition period t_f , there is an overlap between V_{DS} and I_D . The energy dissipated during this on/off transition is referred to as switching loss, which is directly proportional to the switching time and the switching frequency, f_{sw} .

The switching performance of a power transistor is primarily influenced by its intrinsic capacitances, which determine the amount of charge required to change the switch state. For a field-effect transistor (FET), the three critical capacitances are:

- Gate-to-source capacitance (C_{GS}),
- Gate-to-drain capacitance (C_{GD}), and
- Drain-to-source capacitance (C_{DS}).

Circuit designers often work with terminal-specific capacitances, which aggregate these intrinsic values for practical use:

- **Input capacitance** (C_{iss}):

$$C_{iss} = C_{GS} + C_{GD}$$

- **Reverse transfer capacitance** (C_{rss}):

$$C_{rss} = C_{GD}$$

- **Output capacitance** (C_{oss}):

$$C_{oss} = C_{GD} + C_{DS}$$

Among these, C_{GD} is particularly significant due to its highly nonlinear nature. As V_{DS} increases, C_{GD} decreases because the depletion region widens, reducing the number of available charge carriers. To simplify design and analysis, power electronics engineers frequently use **gate charge** (Q_G) to characterize switching performance. Q_G represents the total charge that must be supplied to the gate terminal to fully turn on the power switch. Before defining Q_G in detail, it is essential to understand the concept of hard switching in power devices.

7.7.1 Hard Switching

Gate charge is measured by applying a constant gate current to transition a switch from its off state to the on state [20]. As illustrated in Fig. 7.15 (a), the inductor current I_D flows through the freewheeling diode D , while the drain voltage of the power switch is V_{DS} . The $v_{GS}(t)$ waveform during turn-on is depicted in Fig. 7.15 (b).

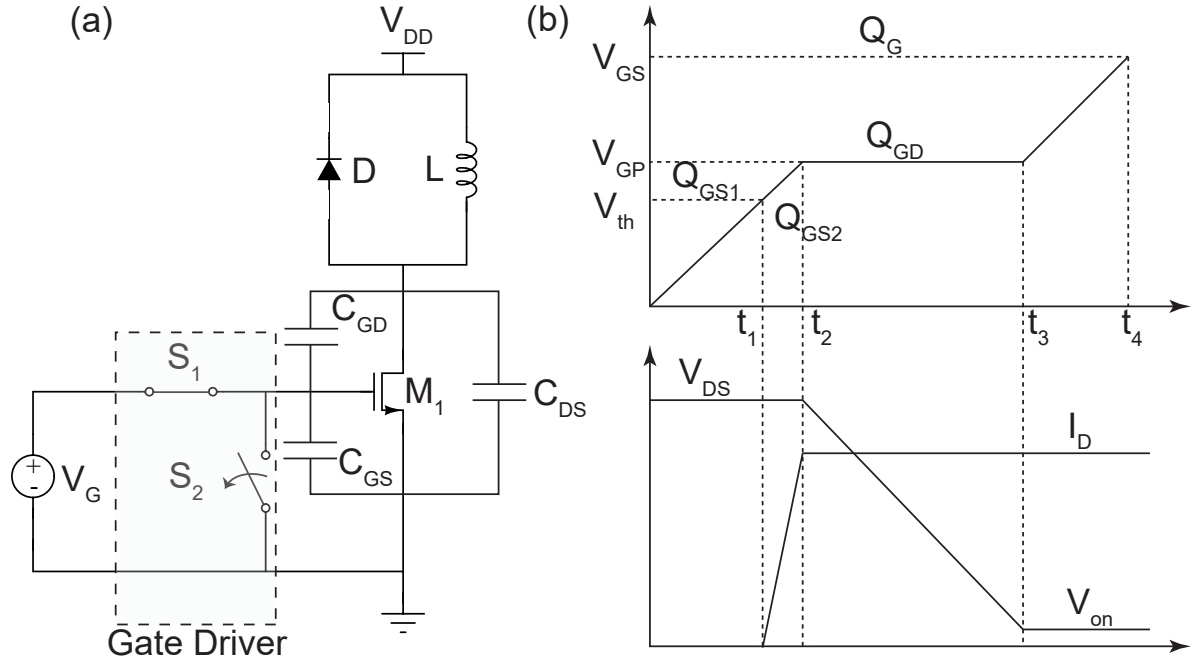


Figure 7.15: (a) Double pulsed test circuit to measure the switching performance of power transistor with a freewheeling diode where the transistor drives an inductive load. (a) Schematic diagram of transistor switching waveforms during hard switching.

Before t_1 , the capacitance experienced by the gate drive circuit is the parallel combination of C_{GS} and $C_{GD}(v_{DS})$. During this period, the drain voltage remains constant because the switch is still in the off state. The gate-source voltage, v_{GS} , increases linearly at a constant rate:

$$\frac{dV_{GS}(t)}{dt} = \frac{I_G}{C_{GS} + C_{GD}(v_{DS})} \quad (7.25)$$

where, I_G is the gate drive current. V_{GS} will reach the threshold voltage V_{th} at time t_1 :

$$t_1 = \frac{V_{th}(C_{GS} + C_{GD}(v_{DS}))}{I_G} \quad (7.26)$$

After t_1 , the drain current begins to increase according to:

$$I_D = k(v_{GS}(t) - V_{th})^2 \quad (7.27)$$

A quadratic I - V relationship is employed for simplicity, where k is a coefficient dependent on the gate oxide capacitance (C_{ox}), channel mobility (μ), and the device geometry. The drain current increases up to I_D by time t_2 . Prior to t_2 , the freewheeling diode remains active,

maintaining the drain voltage at V_{DS} . The value of t_2 can be derived using the preceding equations:

$$t_2 = \frac{(C_{GS} + C_{GD}(v_{DS}))}{I_G} \left(\sqrt{\frac{I_D}{k}} + V_{th} \right) \quad (7.28)$$

The gate voltage at t_2 is V_{GP} :

$$V_{GP} = V_{th} + \sqrt{\frac{I_D}{k}} \quad (7.29)$$

After t_2 , the drain voltage V_{DS} begins to decrease, while the drain current remains constant at I_D . Consequently, the gate voltage stabilizes at V_{GP} , known as the gate plateau voltage or Miller plateau voltage. During this phase, C_{GD} is discharged by the gate drive current I_G , and no part of I_G flows into C_{GS} , as V_{GS} remains constant. The rate of change of $v_{DS}(t)$ is given by:

$$\frac{dv_{DS}(t)}{dt} = -\frac{I_G}{C_{GD}(v_{DS})} \quad (7.30)$$

It is to be noted that C_{GD} is a function of $v_{DS}(t)$. At time t_3 , $v_{DS}(t)$ decreases to V_{on} :

$$t_3 - t_2 = \frac{\int_{V_{on}}^{V_{DS}} C_{GD}(v_{DS}(t)) dv_{DS}(t)}{I_G} = \frac{Q_{GD}}{I_G} \quad (7.31)$$

Beyond t_3 , $v_{DS}(t)$ stabilizes and becomes constant at V_{on} . At this stage, the gate drive current begins to charge a larger capacitance (C_{GS}). Eventually, the gate voltage reaches its supply value, V_{GS} , at time t_4 .

$$t_4 - t_3 = \frac{V_{GS} - V_{GP}}{I_G} (C_{GS} + C_{GD}(v_{on})) \quad (7.32)$$

The total gate charge, Q_G , represents the amount of charge required for the power switch to reach its gate supply voltage, V_{GS} . Fig. 7.15 (b) illustrates the distribution of gate charge across various time intervals. The majority of the switching power loss occurs during the interval $t_3 - t_2$, a phase dominated by the discharge of Q_{GD} . To mitigate these losses, it is crucial to minimize Q_{GD} , which can be achieved by reducing the gate-to-drain capacitance, C_{GD} .

In addition to power loss during the transition period, switching losses also include gate

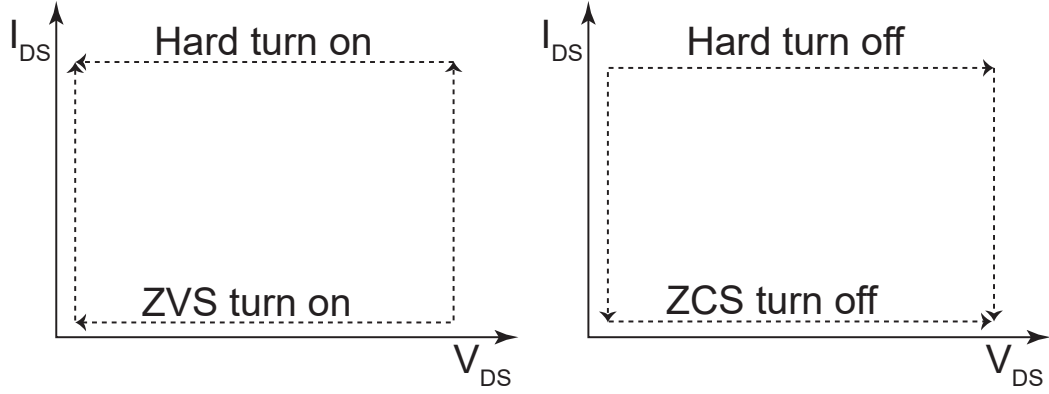


Figure 7.16: Switching trajectories of ZVS turn-on (left) and ZCS turn-off (right) transitions.

charge losses. Gate charge loss refers to the energy required by the gate drive circuit to charge and discharge the gate capacitances. This type of loss becomes significant at higher switching frequencies and lower power output levels.

In Si MOSFETs, another critical contributor to power loss is *reverse recovery loss*. This occurs when the body diode, typically connected anti-parallel to the switch, transitions from the on state to the off state. However, unlike Si power MOSFETs, β -Ga₂O₃ power FinFETs do not suffer from reverse recovery losses, as they lack minority carriers that would otherwise be stored in a junction.

To summarize:

$$Q_{GD} = \int_{V_{DS}}^{V_{on}} C_{GD}(v_{DS}) dv_{DS} \quad (7.33)$$

$$Q_{GS1} = V_{th} (C_{GS} + C_{GD}(v_{DS})) \quad (7.34)$$

$$Q_{GS2} = (C_{GS} + C_{GD}(v_{DS})) \sqrt{\frac{I_{on}}{k}} \quad (7.35)$$

7.7.2 Soft Switching

Soft switching techniques are designed to ensure that a power switch does not simultaneously experience high voltage and high current during commutation [21], [22], thereby reducing

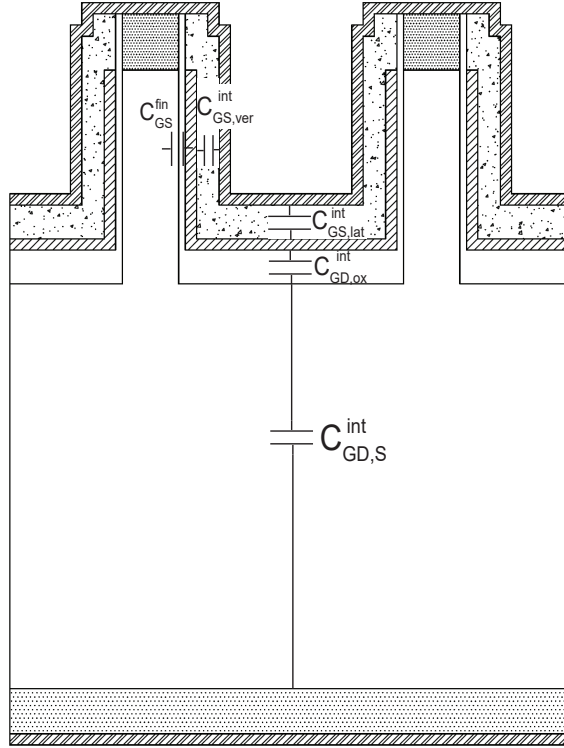


Figure 7.17: Parasitic capacitances of a vertical power FinFET with field oxide.

switching losses. Two commonly used methods are zero-voltage switching (ZVS) and zero-current switching (ZCS) [23]. The switching trajectories for hard switching, ZVS turn-on, and ZCS turn-off are illustrated in Fig. 7.16.

In soft switching, a passive network is integrated into the power circuit to alter the transition trajectories of the transistor's voltage and current. For ZVS, the drain voltage decreases to zero before the current increases to the load current. Conversely, for ZCS, the current reduces to zero before the switch turns off. Unlike hard switching, soft switching prevents simultaneous high voltage and current during commutation, significantly reducing switching losses.

However, soft switching introduces power losses associated with the output capacitance, C_{oss} . The energy stored in the output capacitance, proportional to Q_{oss} , is dissipated within the transistor [24].

$$Q_{oss} = \int_0^{V_{DS}} (C_{GD}(v_{DS}) + C_{DS}) dv_{DS} \quad (7.36)$$

7.8 Capacitances of Power FinFET

The parasitic capacitances of the power FinFET are depicted in Fig. 7.17. The dominant capacitances include:

1. The gate-to-source capacitance of the fin region (C_{GS}^{fin}), comprising the gate oxide capacitance and the fin depletion capacitance.
2. The gate-to-source vertical sidewall oxide capacitance ($C_{GS,ver}^{int}$), formed between the gate metal and the source metal in the interfin region.
3. The gate-to-source lateral oxide capacitance ($C_{GS,lat}^{int}$), also located between the gate metal and the source metal in the interfin region.
4. The gate-to-drain oxide capacitance ($C_{GD,ox}^{int}$), which arises between the gate metal and the semiconductor in the interfin region.
5. The gate-to-drain semiconductor depletion capacitance ($C_{GD,S}^{int}$) in the interfin region.

Consequently, the dominant gate-to-source and gate-to-drain capacitances can be expressed as:

$$C_{GS} = C_{GS}^{fin} \parallel \left(C_{GS,lat}^{int} + C_{GS,ver}^{int} \right) \quad (7.37)$$

$$C_{GD} = C_{GD,ox}^{int} \parallel C_{GD,S}^{int} \quad (7.38)$$

In vertical power FinFETs, the interfin region occupies a significantly larger area compared to the fin region (200 nm fin width versus 1 μm interfin gap). As a result, the gate-to-drain capacitance is predominantly influenced by the interfin region. Given that most of the switching power loss occurs during the Miller plateau—where the gate current is primarily used to charge or discharge the gate-to-drain capacitance—minimizing this capacitance is crucial for enhancing switching speed and reducing switching power loss.

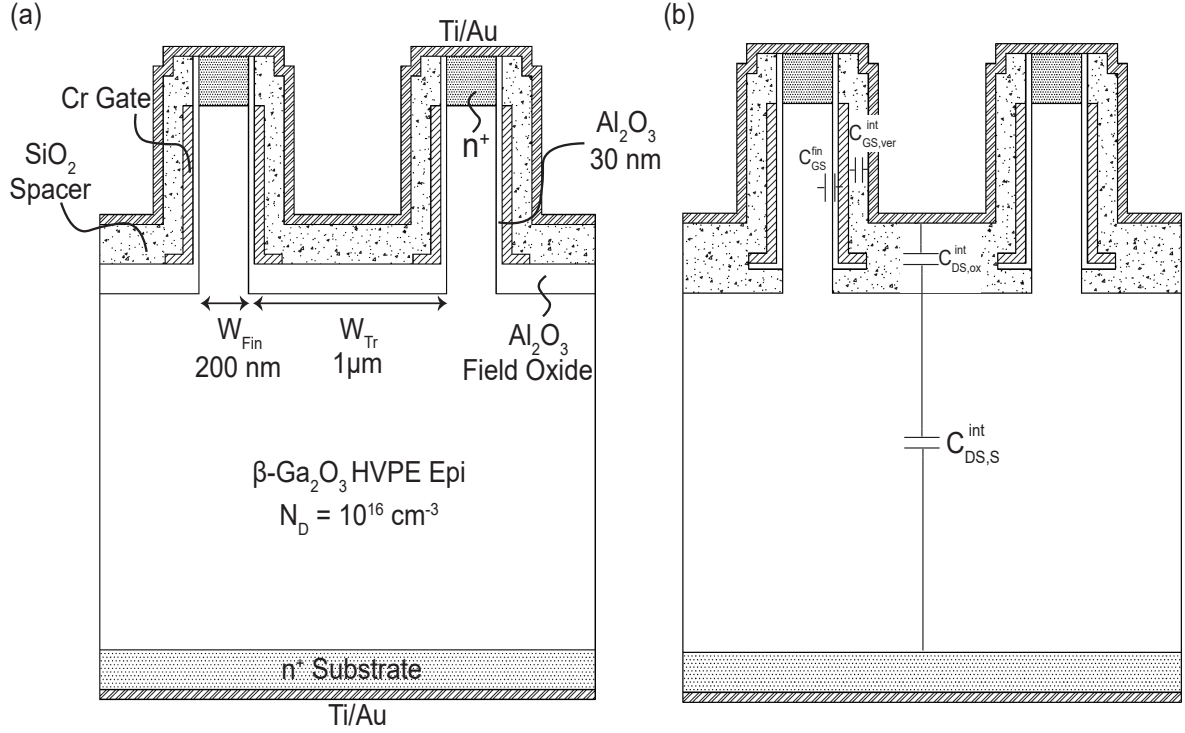


Figure 7.18: (a) Schematic diagram and (b) parasitic capacitances of a split gate vertical power FinFET.

7.9 $\beta\text{-Ga}_2\text{O}_3$ Split Gate Vertical Power FinFET

As discussed in the previous section, the majority of the switching loss arises from the gate-to-drain charge during the Miller plateau. In the vertical FinFET structure shown in Fig. 7.17, it can be observed that the gate metal in the interfin region does not contribute to the transistor's operation. However, this interfin gate metal significantly contributes to the gate-to-drain capacitance ($C_{\text{GD,lat}}^{\text{int}}$) and also accounts for a substantial portion of the gate-to-source lateral spacer oxide capacitance ($C_{\text{GS,lat}}^{\text{int}}$). Removing this gate metal from the interfin region would allow the stored charge in the semiconductor depletion region to be added or removed through both the source and gate currents during switching [25]. This modification could dramatically enhance the switching speed by reducing the parasitic capacitances.

To reduce the gate-to-drain capacitances, a split-gate transistor is designed and fabricated, as illustrated in Fig. 7.18 (a), with the corresponding capacitive components shown in Fig. 7.18 (b). In this structure, the gate metal in the interfin region is removed and retained only along

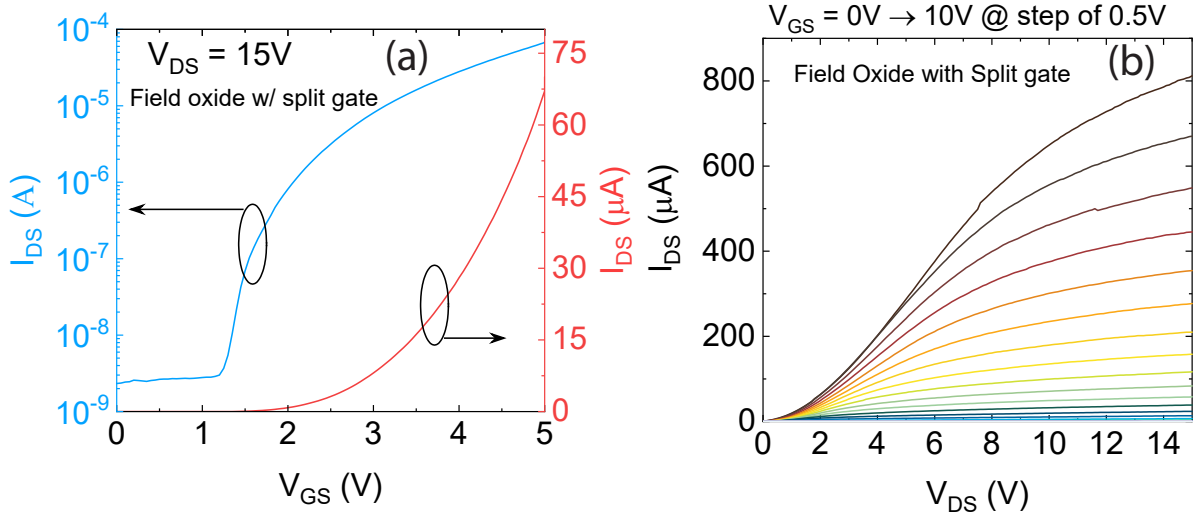


Figure 7.19: (a) Transfer and (b) output characteristics of the fabricated β -Ga₂O₃ split-gate vertical FinFET with field oxide.

the sidewalls. As a result, the entire lateral gate-to-source capacitance ($C_{GS,lat}^{int}$) is replaced by lateral drain-to-source capacitance ($C_{DS,lat}^{int}$). In this configuration, the charge stored in the drift region is managed through both the gate and source currents, thereby reducing the current drive load on the gate driver circuit.

The fabrication process for the split-gate vertical FinFET follows a similar procedure to that of the vertical FinFET with a field oxide layer, with one key modification. After the deposition of the field oxide layer, a blanket etching of the gate metal (Mo) is performed to remove the metal from the interfin region, leaving the gate metal only on the gate pads. During this step, the gate metal is also etched from the top of the fins. Following this, the process continues as outlined in steps 4 to 9 of the flow described in Fig. 7.3.

7.9.1 Current Voltage Characteristics

The transfer and output characteristics of the fabricated $1 \times 1 \text{ mm}^2$ split-gate FinFET are shown in Fig. 7.19 (a) and (b), respectively. These devices were fabricated alongside the non-split-gate FinFETs discussed in Section 7.6.1, and as a result, they exhibit similar fabrication challenges, particularly those associated with the dry etching process. Consequently, the transfer and output

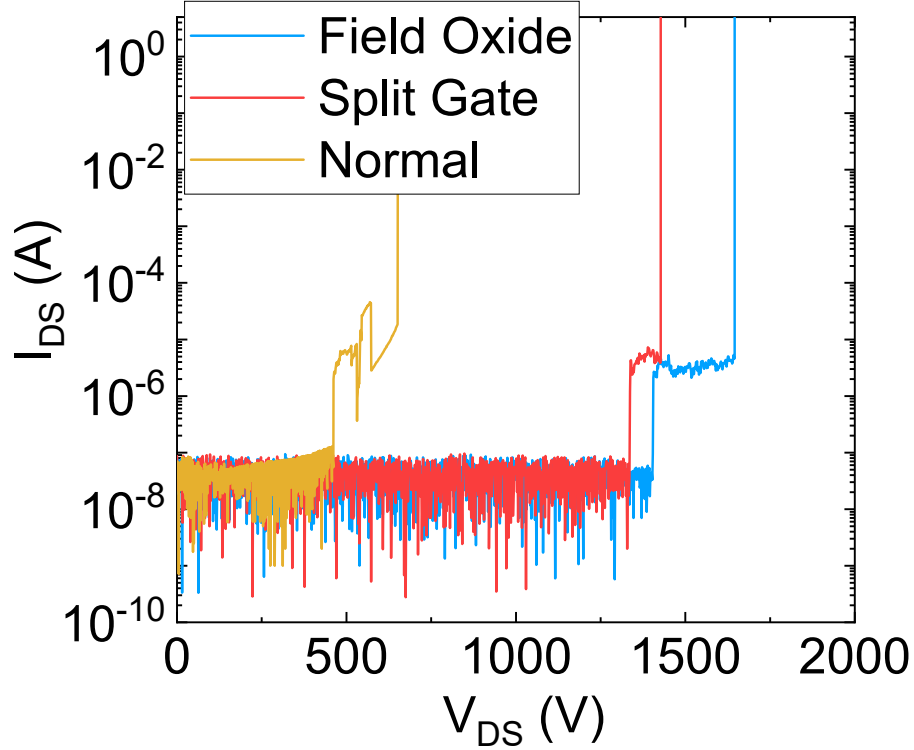


Figure 7.20: Off-state breakdown characteristics of the fabricated second generation β -Ga₂O₃ vertical FinFET without field oxide, with field oxide, and split-gate vertical FinFET with field oxide.

characteristics of the split-gate devices closely resemble those of the non-split-gate devices with a field oxide layer.

The reverse characteristics of the split-gate power FinFETs incorporating a field oxide layer are illustrated in Fig. 7.20. A breakdown voltage of approximately 1.5 kV is observed, which is comparable to the performance of the non-split-gate counterparts with a field oxide layer. Similar to the non-split-gate devices with field-oxide layer, these devices are large-area devices, due to which the breakdown voltage is reduced compared to the smaller-area first-generation devices.

7.9.2 Capacitance Voltage Characteristics

The Keysight B1505A employs HVSMU and MFCMU units to facilitate direct capacitance measurement of power transistors. As depicted in Fig. 7.21 (a), (b), and (c), the capacitance measurement unit features high and low outputs along with an AC guard, which serves as the

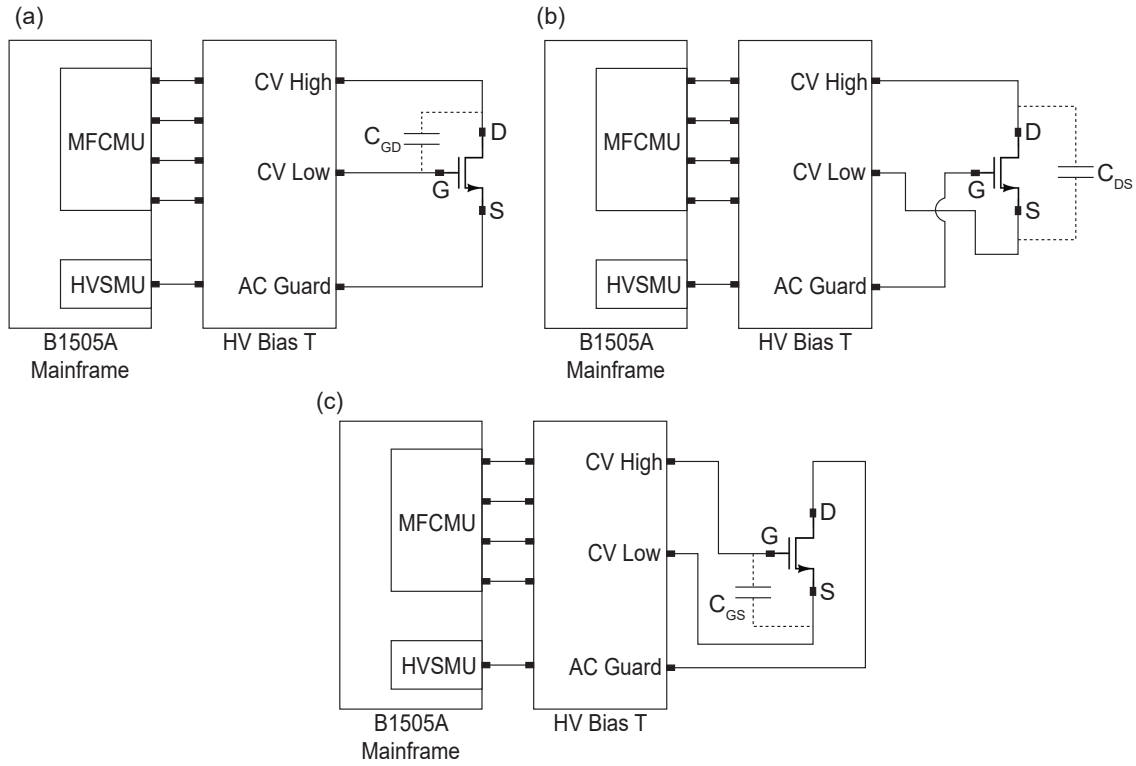


Figure 7.21: (a) C_{GD} , (b) C_{DS} , and (c) C_{GS} measurement setup for a vertical power FinFET using Keysight B1505A parameter analyzer with MFCMU, HVSMU and high voltage bias-T.

ground reference for the unit. To ensure accurate measurements, the AC guard must be connected to the unused terminal when measuring transistor capacitances. Without this connection, floating currents could flow through the other two capacitors, leading to erroneous results.

In Fig. 7.21 (a), the source terminal, being unused, is connected to the AC guard for C_{GD} measurement. Similarly, in Fig. 7.21 (b), the gate terminal is connected to the AC guard for C_{DS} measurement. In both cases, the high bias (HVSMU) is applied to the drain terminal.

Measuring C_{GS} poses additional challenges. For this measurement, the drain terminal must be connected to the AC guard, as shown in Fig. 7.21 (c), while simultaneously applying the high bias to the drain. At AC frequencies above 1 MHz, an additional RC bias network is required to divert the AC current to the AC guard terminal instead of the HVSMU. However, for measurements conducted at lower frequencies, such as 1 kHz, the HVSMU can function effectively as the AC ground.

The capacitance versus drain voltage characteristics for the fabricated vertical FinFET

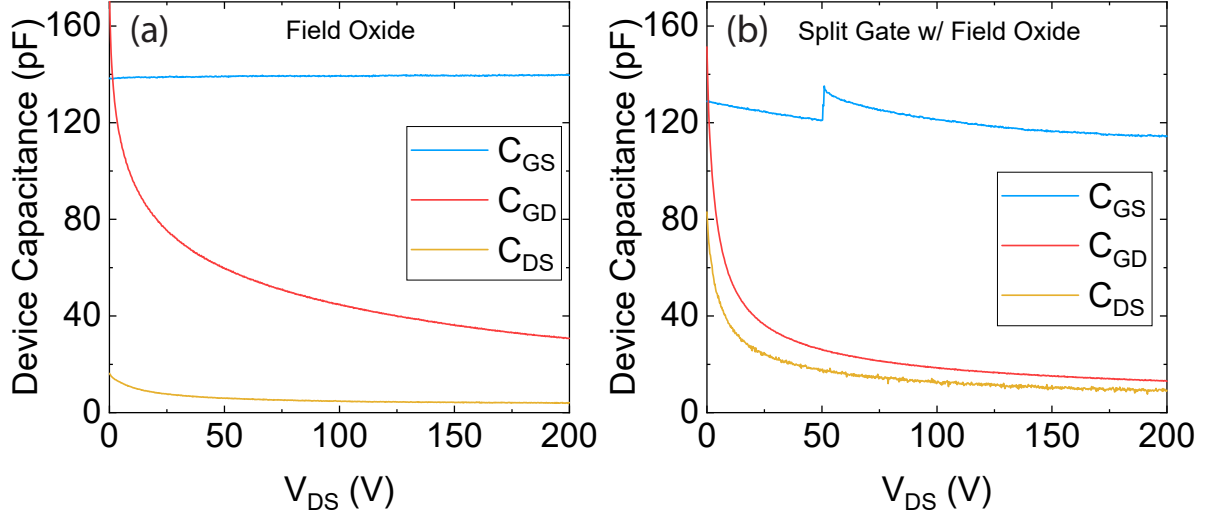


Figure 7.22: Measured three terminal capacitance-voltage plots for the fabricated vertical FinFET with field oxide and (a) without split-gate and (b) with split-gate design.

without split-gate and with split-gate structures are shown in Fig. 7.22 (a) and (b), respectively.

Drain-to-Source Capacitance (C_{DS})

For the vertical FinFET without a split-gate, C_{DS} is minimal, as illustrated in Fig. 7.22 (a). This is because the fin regions are fully depleted in the off state, and the source metal in the inter-fin region is screened by the gate metal.

In contrast, for the split-gate device, the gate metal is removed from the inter-fin region, allowing the entire inter-fin region to contribute to C_{DS} . Consequently, the drain-to-source capacitance increases, as shown in Fig. 7.22 (b). The C_{DS} in the inter-fin region comprises two components:

1. A source metal-insulator-semiconductor (MIS) capacitance.
2. A semiconductor depletion capacitance, both connected in series.

Gate-to-Source Capacitance (C_{GS})

In a vertical FinFET without a split-gate, C_{GS} consists of three components:

1. The intrinsic capacitance of the fin region ($C_{GS,fin}$).
2. The vertical gate-source parasitic capacitance ($C_{GS,ver}^{int}$) in the inter-fin region.
3. The lateral gate-source parasitic capacitance ($C_{GS,lat}^{int}$) in the inter-fin region, as depicted in Fig. 7.17.

As observed in Fig. 7.22 (a), C_{GS} remains mostly constant in vertical FinFETs, since it predominantly arises from the MIS capacitances and the depletion capacitance in the narrow fins.

In the split-gate vertical FinFET, however, the vertical parasitic gate-to-source capacitance in the inter-fin region is eliminated due to the absence of gate metal. Consequently, C_{GS} is significantly reduced compared to the non-split-gate device, as observed in Fig. 7.22 (b). This reduction in C_{GS} is a critical advantage of the split-gate design.

Gate-to-Drain Capacitance (C_{GD})

For the vertical FinFET without a split-gate, C_{GD} is composed of:

1. A gate metal-insulator-semiconductor (MIS) capacitance ($C_{GD,ver}^{int}$).
2. A semiconductor depletion capacitance ($C_{GD,S}^{int}$) connected in series.

As shown in Fig. 7.22 (a), C_{GD} is a highly non-linear capacitance that decreases with increasing drain voltage due to the expansion of the semiconductor depletion width.

In the split-gate device, the removal of the gate metal from the inter-fin region eliminates the inter-fin component of C_{GD} , resulting in a significantly lower C_{GD} compared to the non-split-gate transistor.

Impact on Switching Performance

The reduction in both C_{GS} and C_{GD} for the split-gate device results in:

1. A decrease in the overall input capacitance ($C_{iss} = C_{GS} + C_{GD}$).
2. A reduction in the reverse transfer capacitance ($C_{rss} = C_{GD}$).

This reduction shortens the rise and fall times of the power transistor, as the stored charge in the semiconductor depletion region is added or removed by both the gate current (I_G) and the drain-source current (I_{DS}). Consequently, the total switching power loss is significantly reduced, enhancing overall performance.

While the increase in the output capacitance (C_{DS}) leads to a higher capacitive power loss due to the stored charge in C_{DS} , this loss remains substantially lower compared to the power loss from voltage-current crossover during the Miller plateau in low switching speed devices. Thus, the net effect still favors the split-gate device for improved efficiency.

7.10 Summary

In this chapter, we explored the development of multifin β -Ga₂O₃ normally-off vertical power transistors. The first-generation device achieved a significant milestone, demonstrating kilo-volt-class breakdown voltage alongside a record-low specific on-resistance of $7.5 \text{ m}\Omega \cdot \text{cm}^2$, the lowest reported for any kilo-volt-class β -Ga₂O₃ transistor. However, its breakdown voltage was constrained by the dielectric strength of the thin gate oxide, which also functioned as the voltage-blocking layer. To address this limitation, we introduced and demonstrated a second-generation vertical FinFET featuring a thick field oxide layer in the inter-fin region. This modification significantly improved the breakdown voltage compared to conventional vertical power FinFET designs.

Additionally, the switching characteristics of the power FinFETs were analyzed, culminating in the development of a split-gate architecture. This innovative design effectively reduces the gate-to-drain capacitance, enhancing the overall switching speed and lowering switching power losses without compromising breakdown voltage.

Despite these advancements, the second-generation devices with field oxide and split-gate architectures encountered fabrication challenges, particularly during the fin etching process. These issues led to reduced current conduction and increased resistance, limiting the devices' performance. Consequently, the figure of merit (FOM) of these devices remains below the theoretical limit for β -Ga₂O₃. To fully unlock the potential of β -Ga₂O₃ power transistors, further improvements in device design, fabrication processes, and advances in doping and material science are imperative.

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Chapter 8

Conclusion and Future Directions

8.1 Denouement

In the initial section of this dissertation, we undertake a comprehensive exploration into the design, fabrication, and in-depth analysis of three advanced Schottky barrier diode (SBD) architectures that utilize high- κ dielectric materials to push the boundaries of performance in power electronics. This study focuses on three distinct SBD configurations, each of which employs high- κ dielectric materials to achieve specific device performance enhancements: (1) SBDs integrated with high- κ dielectric field plates, (2) trench SBDs based on β -Ga₂O₃ equipped with high- κ dielectric reduced surface field (RESURF) structures, and (3) superjunction SBDs, also based on β -Ga₂O₃, which incorporate high- κ dielectrics to achieve high field management and power handling. Each of these configurations represents an innovative approach to controlling electric field distribution within the device, ultimately improving device efficiency and performance under high-voltage operating conditions. These designs not only highlight advancements in material applications but also pave the way for next-generation SBDs with enhanced power-handling capabilities.

To thoroughly understand and quantify the advantages of these architectures, this work presents a blend of analytical modeling and simulation studies, offering insights into the

electrostatic behavior and operational benefits of each device design. The simulations delve into critical parameters such as breakdown voltage, leakage current, and electric field distribution, providing a structured analysis framework that reveals the impact of high- κ dielectric properties and structural modifications on device performance. By establishing a clear connection between material choices, structural innovations, and device characteristics, these findings present a robust framework that underpins the design principles of SBDs intended for high-voltage applications. The groundwork laid here will serve as a foundation for future research in this area, with potential implications for enhancing the power efficiency and reliability of SBDs and other power electronic devices.

A key element in this research is the application of high-permittivity (high- κ) dielectrics, particularly in edge termination structures, RESURF mechanisms, and superjunction devices. High- κ dielectrics are integral to effective electric field management, especially at the edges and corners of devices, where electric field crowding often leads to premature breakdown. Edge termination, in this context, is a vital design feature that mitigates electric field concentrations, enhancing the durability and reliability of the device under stress. The use of high- κ dielectrics in edge termination outperforms traditional low- κ dielectrics by reducing peak electric fields and spreading depletion charges over a larger surface area. Both analytical and experimental evidence in this study demonstrate that high- κ dielectric field plates, when applied in β -Ga₂O₃ SBDs, achieve significantly improved parallel-plane electric fields, thereby increasing the power figure of merit and enhancing overall device performance. This approach showcases how material innovations can be harnessed to overcome critical limitations in electric field management for high-voltage SBDs.

One of the major design challenges addressed in this dissertation is the mitigation of reverse leakage current in SBDs, which is especially sensitive to high surface electric fields. In wide bandgap (WBG) and ultra-wide bandgap (UWBG) semiconductor materials, realizing electric fields close to the material's theoretical breakdown field is crucial to fully leverage the unique material properties and unlock the maximum potential of these devices. However, this

requirement poses a specific challenge for SBDs: numerical studies, such as those conducted by Li et al. [1], indicate that the practical limit for surface electric fields is approximately 2 MV/cm for a Schottky barrier height of 1 eV. Exceeding this threshold leads to a drastic increase in reverse leakage current, which diminishes device efficiency and reliability. This discrepancy necessitates novel electrostatic engineering solutions that go beyond conventional design approaches, addressing the limitations imposed by high electric fields and the associated leakage currents.

To address the challenges associated with reverse leakage currents and voltage performance in Schottky barrier diodes (SBDs), this dissertation introduces high- κ dielectric RESURF structures meticulously designed to optimize electric field modulation near the metal/ semiconductor interface of the diode. By incorporating high- κ dielectrics in these RESURF-enhanced architectures, along with a low work-function anode metal contact, this dissertation contributes to the development of SBDs that aim to effectively reduce reverse leakage currents while simultaneously lowering turn-on voltage and increasing breakdown voltage. These enhancements contribute to the creation of devices that minimize power loss in power rectifiers, thereby establishing a pathway toward high-voltage, low-loss, and energy-efficient power devices tailored for modern power electronics applications. This work not only emphasizes the significance of material selection and interface engineering but also highlights the potential for high- κ dielectrics to revolutionize the performance of SBDs in demanding operational environments.

Another notable achievement of this research is the successful realization of high- κ dielectric superjunction structures within β -Ga₂O₃. The inherent lack of p-type doping in β -Ga₂O₃ poses significant challenges for the development of conventional superjunction structures, which rely on balanced p-n doping to function effectively. However, by leveraging dielectric polarization charge and engineering device dimensions, we propose and demonstrate superjunction-like devices utilizing high- κ dielectrics. These innovative structures offer distinct advantages over traditional p-n superjunction devices, primarily due to the elimination of the charge balancing requirement—a significant hurdle in the advancement of wide and ultra-wide bandgap

semiconductors. With continued improvements in material quality and the application of advanced edge termination techniques, these high- κ dielectric superjunction structures possess the potential to exceed the already impressive unipolar power figure of merit associated with β -Ga₂O₃. This achievement underscores the transformative possibilities that high- κ dielectrics present for the future of high-performance power devices, paving the way for enhanced efficiency and reliability in power electronics applications.

In the second part of this dissertation, we explore selected topics related to β -Ga₂O₃-based vertical power transistors, beginning with an innovative approach to dielectric deposition. The Prologue to this part introduces the development of the first in-situ dielectric deposition technique specifically tailored for β -Ga₂O₃ applications, aimed at establishing reliable gate dielectrics for transistors. This novel technique involves growing the dielectric material in the same chamber as the semiconductor without breaking the vacuum, ensuring an exceptionally pristine dielectric/semiconductor interface.

The high-temperature conditions employed during the metal-organic chemical vapor deposition (MOCVD) process not only contribute to the formation of denser dielectrics but also significantly enhance the breakdown voltage of the dielectric layer. This elevated temperature environment further improves the crystallinity of the dielectrics, resulting in a low interface state density dielectric/semiconductor interface that is vital for optimal device operation. The incorporation of both medium and high-temperature dielectrics as distinct layers within the transistor structure demonstrates a marked improvement in the reliability and lifetime of the dielectric material. Remarkably, this enhancement is achieved without degrading the breakdown voltage, underscoring the effectiveness of the in-situ deposition technique in optimizing dielectric performance.

By focusing on the interface quality and the characteristics of the gate dielectrics, we aim to contribute to the broader field of power electronics, where the performance and longevity of transistors are paramount. The innovative in-situ dielectric deposition technique not only addresses existing challenges in the fabrication of β -Ga₂O₃ transistors but also sets the stage for

future developments in high-performance, reliable power devices. Through these investigations, the dissertation not only highlights the potential of β -Ga₂O₃ in next-generation power electronics but also emphasizes the importance of interface engineering in achieving high-performing semiconductor devices.

This thesis culminates in the demonstration of vertical transistors based on β -Ga₂O₃. Given the current limitations in achieving native p-type doping in β -Ga₂O₃, the vertical fin transistor structure emerges as the most viable option for high-performance applications. While alternative architectures, such as CAVETs and UMOSFETs, have been explored in the literature, they are often hindered by excessive leakage current through the deep acceptor-doped current-blocking regions. This leakage current presents a critical barrier to achieving the high-voltage operation required for efficient power devices.

In our research, we successfully demonstrated normally-off β -Ga₂O₃ fin transistors with a commendable breakdown voltage exceeding 1 kV, highlighting the immense potential of the vertical fin architecture in addressing the limitations of conventional designs. This milestone showcases the efficacy of the vertical fin structure in achieving robust high-voltage performance. Furthermore, we present advanced and optimized designs aimed at further enhancing breakdown voltage while minimizing switching losses, demonstrating the transformative impact of strategic design innovations on overall device performance. Additionally, we explore the implementation of cutting-edge edge termination techniques, which promise to significantly elevate the operational capabilities of vertical transistors.

Despite these advances, the intricate fabrication processes required for these devices pose substantial challenges, often risking material integrity. Overcoming these hurdles is critical for realizing the full potential of vertical β -Ga₂O₃ fin transistors. Future efforts must focus on mitigating fabrication-induced damage, such as by employing post-dry-etch wet etching techniques [2] or completely avoiding dry etching by using heated wet etching [3]. Improving material quality will also be essential to ensure the successful integration of these advanced devices into practical applications. By addressing these challenges, vertical β -Ga₂O₃ fin transistors can lead

the next wave of high-voltage, energy-efficient power electronics, cementing β -Ga₂O₃ as a cornerstone material in the evolution of modern power semiconductor technologies.

8.2 Benchmarking of β -Ga₂O₃-based Power Devices

The primary accomplishments of this work include the development of β -Ga₂O₃-based high- κ field-plated Schottky barrier diodes (SBDs), high- κ RESURF trench SBDs, high- κ dielectric superjunction SBDs, and β -Ga₂O₃-based vertical FinFETs. The high- κ field-plated SBD marked a significant milestone as the first β -Ga₂O₃ diode to surpass a power figure of merit (FOM) of 1 GW/cm². Subsequently, the high- κ dielectric superjunction SBD achieved a record-breaking unipolar FOM that exceeded the theoretical limits of 4H-SiC. Additionally, the trench SBD demonstrated the lowest reverse leakage current reported for any β -Ga₂O₃-based SBD, while maintaining a breakdown voltage exceeding 1 kV. Furthermore, the β -Ga₂O₃ vertical FinFET exhibited normally-off operation and achieved the lowest specific on-resistance among all kilovolt-class β -Ga₂O₃ vertical transistors.

Benchmark comparisons of β -Ga₂O₃ diodes and power transistors are presented in Fig. 8.1 (a) and (b). For diodes, state-of-the-art SiC and GaN devices are included as references. While β -Ga₂O₃-based devices demonstrate competitive performance relative to SiC and GaN, there remains a considerable gap between their current performance and the theoretical limits of the material. Continued advancements in β -Ga₂O₃ device design and fabrication are essential to fully realize the material's immense potential.

8.3 Paths Yet to Explore: Journey Ahead

8.3.1 Breakdown Mechanisms in β -Ga₂O₃

Currently, there is no conclusive study or consensus regarding the mechanisms behind device breakdown in β -Ga₂O₃. Some research indicates that breakdown occurs intrinsically due to

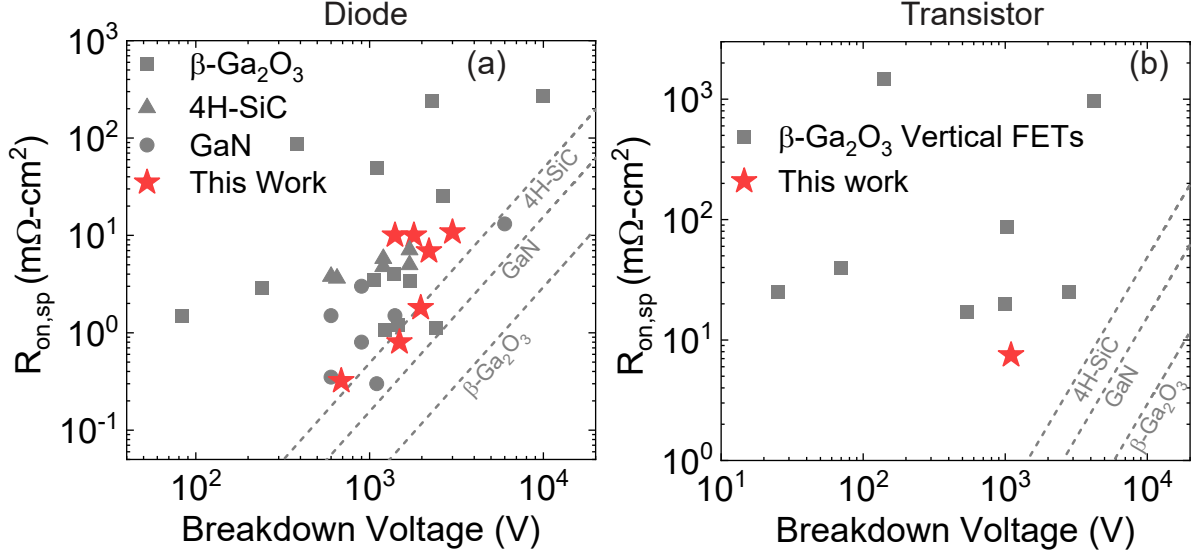


Figure 8.1: (a) Benchmark plots of β -Ga₂O₃ based diodes, SiC JBS diodes, and GaN vertical diodes. (b) Benchmark plots of β -Ga₂O₃ vertical power transistors.

excessive heating of the material caused by high power densities [4], while other studies suggest that breakdown is primarily related to defect-mediated processes [5], [6]. It is plausible that these two mechanisms are interconnected, each contributing to the overall breakdown behavior of the device.

Moreover, a systematic study investigating the correlations between breakdown voltage and dislocation density in the epitaxial drift layer is notably lacking. Establishing a clear understanding of what level of dislocation density is acceptable for power electronics applications would be highly beneficial. Such insights could guide the optimization of material quality and device design, ultimately leading to improved performance in power semiconductor technologies. Additionally, the precise breakdown mechanisms remain elusive, complicating efforts to address device failures effectively.

Understanding the mechanisms underlying breakdown phenomena is crucial for the development of high-performance power devices. By elucidating these mechanisms and the role of dislocation density, researchers can better predict device behavior and enhance the reliability and efficiency of β -Ga₂O₃-based power electronics. This knowledge will not only advance the field but also facilitate the realization of next-generation power devices capable of operating at

high voltages and power densities.

8.3.2 Impact Ionization Co-efficients in β -Ga₂O₃

It has been over a decade since the realization of the first β -Ga₂O₃ device, yet there remains a significant gap in our understanding of the impact ionization coefficients within this material [7]. It should be noted that there is no experimental evidence of avalanche or impact ionization in β -Ga₂O₃. While some studies have attempted to extract these coefficients using unclamped Inductor Switching (UIS) tests in β -Ga₂O₃ heterojunction diodes and using Electron Beam Induced Current (EBIC) characterization[8], the results are often inconclusive due to the involvement of multiple materials, complicating the analysis. Most devices presented in this work, as well as those documented in the literature, rely on a theoretical critical electric field of β -Ga₂O₃ as a standard for comparing breakdown strength. However, it is crucial to recognize that the critical electric field of a semiconductor is not a constant; it varies significantly with factors such as doping concentration, defect density, and temperature [9].

This lack of knowledge regarding the impact ionization coefficients in β -Ga₂O₃ poses a substantial challenge, as it hinders the ability to optimize device designs. Consequently, many demonstrated devices tend to underperform, failing to reach their full potential. Understanding the impact-ionization coefficients and their dependencies on various factors is essential for the accurate design and implementation of high-performance power devices.

By establishing a clearer understanding of these coefficients, researchers can develop more effective models for predicting device behavior under various operating conditions. This knowledge will ultimately facilitate the optimization of β -Ga₂O₃ device designs, leading to enhanced performance and reliability in power electronics applications.

8.3.3 Development of Thick β -Ga₂O₃ Epitaxial Layers

The development of low point- and extended-defect density thick epitaxial layers is crucial for realizing high-voltage vertical devices. To achieve a 10 kV vertical device, a drift layer thickness

of over $25\ \mu\text{m}$ is necessary, given the highest breakdown field reported to date. Some studies, particularly from NCT Japan, have demonstrated devices with $40\ \mu\text{m}$ thick drift layers [10]. However, these thicker epitaxial layers often exhibit an increased density of killer defects, which compromises the breakdown fields and ultimately limits device performance [11]. Therefore, advancing material research aimed at growing thick, high-quality drift layers on conducting substrates is of paramount importance.

8.3.4 Vertical High- κ Dielectric Superjunctions Devices

In this work, we successfully demonstrate a lateral dielectric superjunction device as a proof-of-concept for high- κ dielectric superjunctions. While this achievement marks a significant step forward, the demonstration of a vertical dielectric superjunction device remains pending. Vertical devices are generally preferred over their lateral counterparts due to their superior current scaling capabilities and enhanced reliability, which is attributed to their non-surface transport characteristics.

Throughout this thesis, we discuss numerous challenges associated with the implementation of high- κ dielectric superjunctions, primarily stemming from existing technological limitations. These challenges underscore the need for innovative fabrication processes that can facilitate the realization of vertical structures [12], [13]. By overcoming these obstacles, we anticipate that vertical dielectric superjunction devices can be developed, leading to substantial improvements in overall device performance.

Ultimately, the pursuit of vertical high- κ dielectric superjunction devices holds great promise for advancing power semiconductor technology. As we continue to refine fabrication techniques and address the associated challenges, we move closer to unlocking the full potential of these advanced structures, paving the way for enhanced efficiency in future power electronics applications.

8.3.5 Cooling Strategies and Packaging of β -Ga₂O₃ Devices

Despite the numerous advantages of β -Ga₂O₃-based devices, the material's low thermal conductivity remains a significant challenge for their deployment in real-world applications. For β -Ga₂O₃ to operate efficiently compared to other materials—whether narrow or wide bandgap—it must function at much higher power densities [14], [15]. However, this increase in power density results in greater heat generation, necessitating effective thermal management to prevent thermal failure.

The inherent low thermal conductivity of β -Ga₂O₃ [16] exacerbates the issue of heat dissipation, making it imperative to employ extrinsic cooling methods for high-power density devices. Some preliminary work has been conducted on double-side cooling strategies, which involve managing thermal output from both the junction and the bottom side of β -Ga₂O₃ vertical devices [4], showing promising potential for improved thermal management.

Moreover, any commercial power device must be packaged appropriately to ensure reliability and performance. Therefore, research into the packaging of β -Ga₂O₃-based devices that can handle high power densities is critically important. Such efforts will help prevent device performance from being limited by packaging constraints, enabling β -Ga₂O₃ to reach its full potential in practical applications. The body of work on thermal management does indicate that the low bulk thermal conductivity is not a show stopper and heat dissipation can be managed. Through innovative cooling and packaging solutions with electro-thermal co-design approaches, the viability of β -Ga₂O₃ for next-generation power electronics can be enhanced.

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