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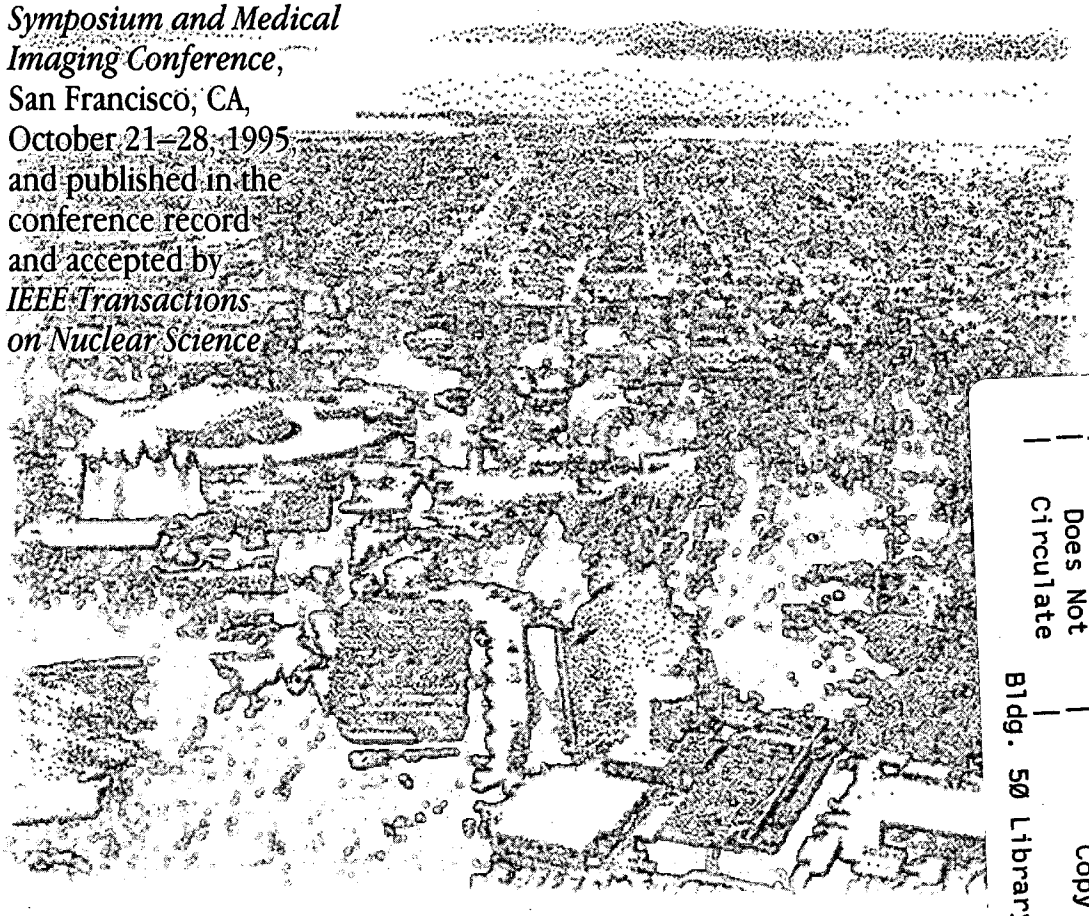

## DISCLAIMER

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# A Sixteen Channel Peak Sensing ADC for Singles Spectra in the FERA Format

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## ABSTRACT

To read out multi-element small X-ray detectors for X-ray fluorescence applications with synchrotron radiation one needs the capability to record multiple singles spectra for each detector element at high rates. We have developed a sixteen channel 11 bit peak sensing ADC in a CAMAC module. We use the FERA readout bus to place the data into a commercially available histogramming module developed to generate multiple histograms from FERA ADCs. The sixteen channels digitize shaped pulses from the detectors without external gating. The digitizing time is 8 μsec, the peak acquisition time is ≥ 2 μsec. The module contains a LIFO to permit block transfers in order to minimize dead times associated with the readout. There is a common CAMAC controlled analog threshold for noise suppression and a 16 bit mask to enable or disable individual ADCs. Differential non linearity is less than +8% / -4%. A γ-ray spectrum collected using this ADC is presented.

## I. INTRODUCTION

At LBL a 64 element linear silicon detector is used to record spectra in a dispersive spectrometer for X-ray fluorescence work with synchrotron radiation. In this application one wants to accumulate amplitude histograms (spectra) for each of the elements at rates as high as possible. Each detector element signal is processed in a standard spectroscopy chain: a charge sensitive preamplifier followed by a shaping amplifier and an ADC. 16 preamplifiers and shapers have been placed in an analog integrated circuit (IC). This leaves the task of building peak sensing ADCs to digitize the signals. Commercially available multi-channel ADCs are not designed to digitize asynchronous signals from their inputs, they require a gating signal which triggers all channels at the same time. Since the signals from our detector are random we have to provide one ADC per input with the proper "self trigger".

## II. ELECTRONICS

We have chosen a 16 bit sampling ADC IC (Burr Brown ADS 7805) using only the most significant 11 bits. We combined it with a peak detector and placed this circuit on 16 small daughter boards with a size of 53x39mm$^2$. These boards are then plugged into a CAMAC mother board which holds the logic for control, setup, and readout. Because of the high rate requirements we have chosen the FERA readout [1]. Commercial histograming memories for this standard are available in CAMAC which are designed to accumulate histograms from FERA bus data. These histograms can be read through CAMAC. We provide also a LIFO on the motherboard for intermediate storage. This allows the transfer of the data to the histogramming memory in 16 word blocks minimizing the dead time associated with reading out of the data. Within the processing time of one ADC (10 μsec) 100 digitized data words can be read neglecting the overhead associated with block transfer. Therefore, with this arrangement six of these modules (each producing 16 words or 96 total in 10 μsec) can be connected to one histogramming memory of the proper size (>96 times 2k = 192k words) without slowing down the data collection since the reading takes 96 times 100 nsec or 9.6 μsec.

## III. DESIGN

The schematic of a daughter board is given in fig 1. The input signal is amplified by a factor of 2.5 and limited to a range of 0 to 5V in the first stage. This is followed by a peak detector similar to the one proposed in ref.[2]. In this method the signal is fed through a RC integrator to the ADC and a RC differentiator to a zero cross comparator. The output of the RC integrator is amplified by a factor of 4 and level shifted so that the signal falls within the input range of the ADS 7508 i.e. -10V to +10V. The zero cross discriminator output changes state at the peak of the integrated pulse going to the ADC. The signal there triggers a BUSY flipflop which starts the ADC IC. At the end of the ADC-busy signal the ADC data are transferred into an output register and a DATA-READY signal is set. At this time the ADC can start another conversion cycle, therefore the BUSY flipflop is cleared. The logic on the motherboard then has to read the output register before the next signal has been digitized.

The block diagram of the CAMAC board design is shown in fig.2. The 16 ADC daughterboards are connected to the field programmable gate array (FPGA) that controls the digitizing, the control, and the readout by a bus that carries the data and separate lines for the control signals. The connection to the CAMAC and FERA busses is achieved with the appropriate line driver ICs. There is also a DAC which controls the trigger threshold for the ADCs. The schematic of the control FPGA is shown in fig.3. which shows the different state machines that accomplish the different functions. Details of the logic will be published in a separate paper.

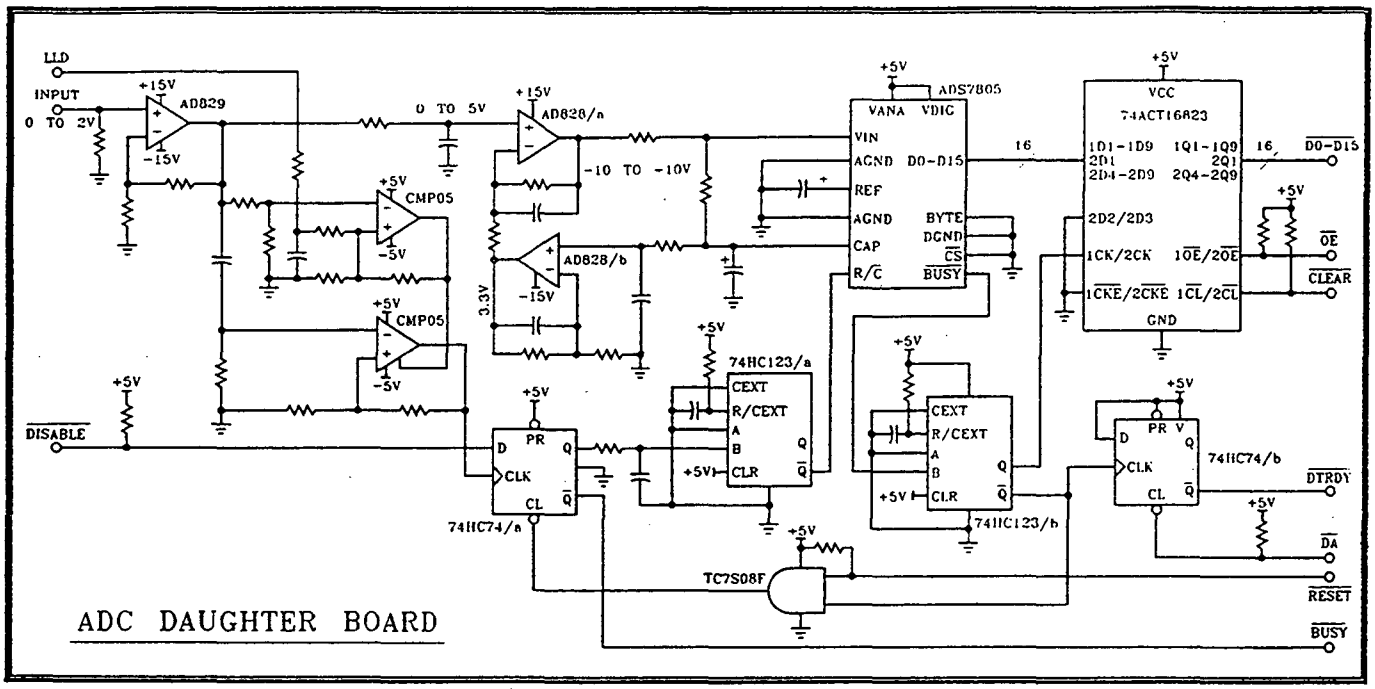


Fig. 1. ADC Daughter Board Schematic

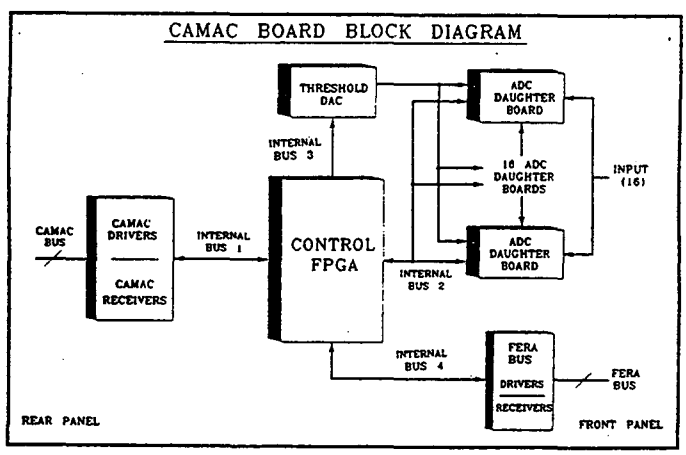


Fig. 2. Block Diagram of the CAMAC module design

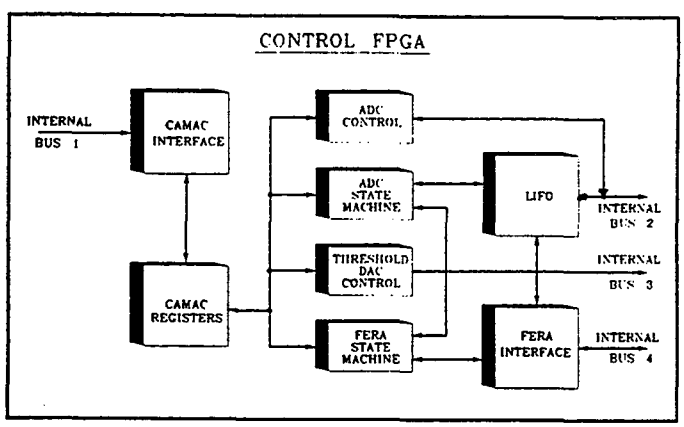


Fig. 3 Block diagram of the control FPGA design

## IV. RESULTS

Tests with early daughter board prototypes have shown the following results: Peak acquisition time is 1.5 μsec, digitizing time is 8 μsec.

At a peaking time of the input signal of 2 μsec the boards trigger at <0.3% of full scale in the prototype version. Differential non linearity is +8% / -4%. We show a test of the differential nonlinearity using a ramp pulser. 0% corresponds to 1.6 million counts per channel in fig. 4.

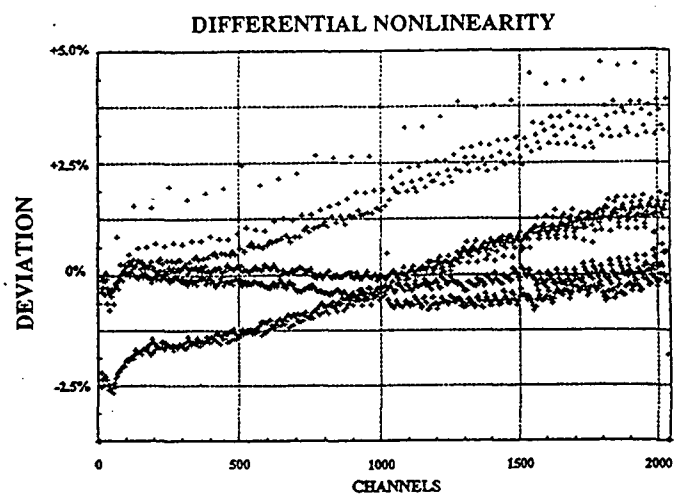


Fig. 4.Plot of the differential nonlinearity of a prototype ADC daughter board obtained with a ramp pulser. 0% corresponds to 1.6 million counts per channel. The integral nonlinearity of the pulser contributed to the slope of the curve..

In fig. 5 we show a spectrum of a Co60 source taken with a 75% Germanium detector. The resolution at the 1333 keV line is about 2.7 keV FWHM.

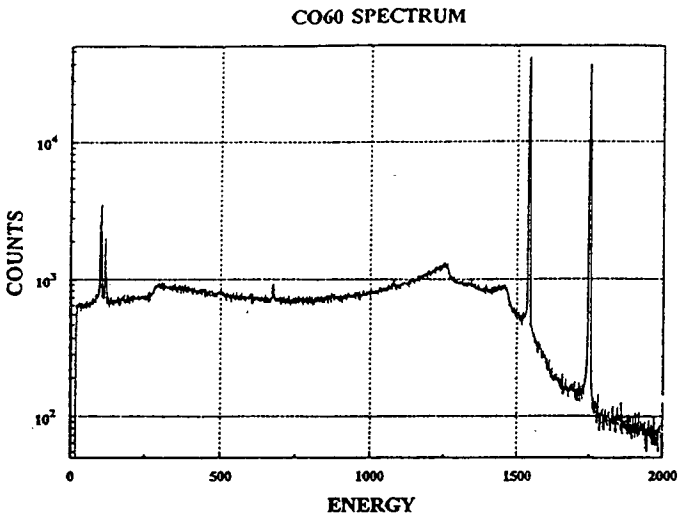


Fig. 5 Germanium detector spectrum of Co60

The experimenters have requested recently that the ADC be able to digitize pulses with shorter peaking times. This requires the use of a separate sample and hold I.C. We have designed a version of this "improved" circuit. Preliminary tests of a breadboard version of this variant show that it can digitize pulses with 250 nsec peaking time. In that design we have also included a base line restorer [3].

## V. CONCLUSION

In summary, we have built a module which allows the accumulation of multiple singles spectra at high speed. This is a function which is needed, but is not yet commercially available, for new multi-element detectors used in X-ray applications at the new high intensity synchrotron radiation facilities. This is achieved using commercial hardware and software wherever possible. Results from an initial $\gamma$-ray spectrum show resolutions comparable to commercial spectroscopy ADCs.

## VI.ACKNOWLEDGMENTS

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Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

## VII. REFERENCES

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[3] L. B. Robinson, Rev. Sci. Instr. 32 (1961) 1057

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