UNIVERSITY OF CALIFORNIA SAN DIEGO

Ultra-Low Power, Narrow-Band Receivers Employing Regenerative Amplifiers

A Dissertation submitted in partial satisfaction of the requirements
for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Committee in charge:

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2022

The Dissertation of Bao Huu Lam is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

To my family.

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The material presented in this dissertation is based on the following published articles and/or works that have been submitted or being prepared for submission for publication.

Chapter 2, in part, is based on the material as it appears in B. H. Lam, P. Gudem and P. P. Mercier, "Analysis and Measurement of Noise Suppression in a Nonlinear Regenerative Amplifier," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, doi: 10.1109/TCSI.2022.3184924. The dissertation author was the primary researcher and author of this paper.

Chapter 3, in part, has recently been submitted to be considered for a future publication, and is coauthored with Hongyu Lu, Ahmed Gharib Gadelkarim, Nader Fathy, Prasad Gudem, and Patrick Mercier. The dissertation author was the primary researcher and author of this material.

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PUBLICATIONS

B. H. Lam, M. Dunna, S.-K. Kuo, D. Bharadia, and P. P. Mercier, "An Ultra-Low Power BLE/WiFi-Compatible Downlink for Smart Wearable Devices", In preparation.

B. H. Lam, H. Lu, A. G. Gadelkarim, N. Fathy, P. Gudem, and P. P. Mercier, "A 0.11mW 2.4GHz Receiver Employing a Q-Boosted Impedance Transformer and Regenerative Amplifier Achieving -101dBm Sensitivity and -28dB SIR", Submitted.

B. H. Lam, P. Gudem and P. P. Mercier, "Analysis and Measurement of Noise Suppression in a Nonlinear Regenerative Amplifier," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, doi: 10.1109/TCSI.2022.3184924.

A. Abdulslam, **B. H. Lam** and P. P. Mercier, "A Battery-Connected Symmetric Modified Multilevel Ladder Converter Achieving 0.45W/mm2 Power Density and 90% Peak Efficiency," *2019 IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1-4, doi: 10.1109/CICC.2019.8780196.

ABSTRACT OF THE DISSERTATION

Ultra-Low Power, Narrow-Band Receivers Employing Regenerative Amplifiers

by

Bao Huu Lam

Doctor of Philosophy in Electrical Engineering

(Electronic Circuits and Systems)

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Professor Patrick Mercier, Chair

This dissertation investigates the operation of the regenerative amplifier (RA) in the linear and nonlinear regimes, especially regarding the noise performance, and several integrated applications in which it can be extremely helpful to enhance system performance. Chapter 2 analyzes an interesting phenomenon associated with an RA operating in the

nonlinear regime, that exhibits a suppression of the in-band noise, resulting in an improvement on the output carrier-to-noise (CNR) ratio. A promising application of the phenomenon in electromagnetic tomography is also discussed. Chapter 3 delves into an application of a dual RA architecture to demodulate an OOK signal non-coherently, which is a state-of-the-art 2.4-GHz receiver that has an excellent sensitivity of -101 dBm and an ultra-low power of 112 μW with an impressive signal-to-interference ratio (SIR) of -28 dB at a 3-MHz offset. Chapter 4 presents yet another state-of-the-art, ultra-low power receiver employing dual RAs that is compatible with Bluetooth Low Energy (BLE) and WiFi, that achieves an excellent sensitivity of -80 dBm for 16QAM, while the active power consumption is only 30 μW and the energy efficiency is the highest compared to prior works in the literature. The receiver can be deployed on smart wearable devices to communicate directly with a smartphone or a WiFi access point to significantly improve battery life while still retaining a high data throughput.

CHAPTER 1

Introduction

I – Challenges of Ultra-Low Power Receivers Based on Envelope Detector

Ultra-low power receivers remain a hot research trend to extend battery life for wireless sensor networks, smart wearables, implantable medical devices, Internet-of-Things (IoT) devices, etc. [1 – 6]. These receivers typically operate over a short range and with a low data rate (< 1 Mbps) while requiring a high power efficiency for long lifetime. A key component widely employed in these ultra-low power receivers is the envelope detector (ED) which performs the down-conversion of the signal from RF frequencies into DC or near DC frequencies. In essence, the ED can simply be a device that exhibits a second-order nonlinear relationship between its input and output, e.g. a diode operating in the large-signal regime that squares the RF voltage into a DC current. Interestingly, as shown in Chapter 3, the ED does not need to employ active components that constantly consume power. In fact, it can be designed using only passive components [5, 6] that have no current flowing through them and therefore consume absolutely zero power! In addition, even if the ED is implemented using active components, the design can be fairly simple and the cost of additional power consumption is only a negligible portion of the overall power of the entire receiver [7]. The main benefit that the ED offers is that it squares the RF signal, hence acting as a mixer to mix the signal down to DC. Therefore, the ED essentially does the job of a local oscillator (LO) and a mixer in a zero-IF receiver. As a result, the need to generate an LO on the receiver side can be precluded, leading to an extremely high reduction in power consumption.

Although the ED sounds like an ideal device that can permanently and completely replace a power-hungry LO and thereby a phase-locked loop (PLL) in the receiver, it also comes with several downsides that can potentially make it look less attractive in the consideration of a high-performance, robust architecture, as shown in detail in Chapters 3 and 4 [8]:

- Firstly, it can only down-convert signal non-coherently, i.e. the phase information will no longer be preserved.
- Secondly, the ED's noise performance can be inferior. This stems from the fact that due to the nonlinear squaring operation, various types of noise are mixed down into DC or near-DC frequencies; in addition, the squaring of the desired signal results in significantly lower signal power, which can easily be overwhelmed by the noise present at the ED output, thereby worsening the SNR.
- Thirdly, the ED does not distinguish between the desired signal and any interference accompanying the signal. Both of these will get mixed down to DC, potentially further degrading the SNR.

Since inherently, the ED does not support coherent demodulation of the signal, one way to facilitate that is the clever use of an additional tone that accompanies the signal during transmission. Fig. 1.1 shows such a scheme where an external continuous-wave (CW) tone is sent along with a desired signal. The frequency spacing between the external CW tone and the desired signal will set the intermediate frequency (IF) after down-conversion. With the squaring operation, the ED will multiply the external tone with the desired signal, leading to the down-conversion of the desired signal onto the IF spectrum. As shown later in the dissertation, due to the squaring of the ED, a significant amount of RF front-end gain is required to combat the various noises stemming from the ED's operation.

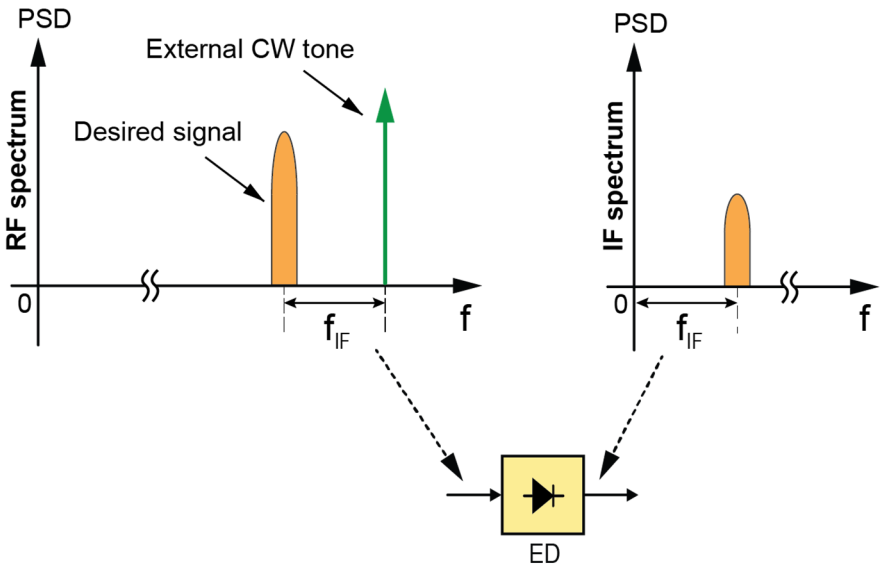


Figure 1.1: A clever way of sending an external CW tone along with the desired signal to enable coherent demodulation via the ED.

Based on the aforementioned disadvantages of the ED, in order to achieve good noise performance and interference resiliency, it is important that the block prior to the ED must be able to deliver:

- A high gain to combat all the various noises associated with the ED. As shown in later chapters;
- A narrow bandwidth to reduce the mixing of noise into DC and to help suppress interferences outside of the frequency band of interest;
- A relatively low noise figure while consuming a very low amount of power, although the requirement on noise is less stringent than that on the gain, as will be seen shortly.

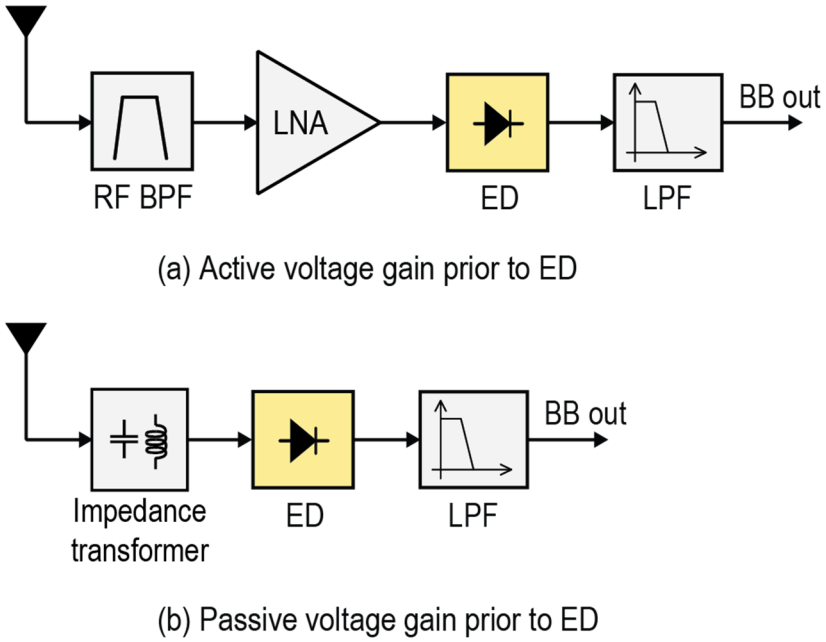


Figure 1.2: Some existing solutions to provide voltage gain prior to the ED: (a) active voltage gain; and (b) passive voltage gain.

Some existing solutions to meet these requirements are shown in Fig. 1.2 which include one of the following:

1. Placing an active stage prior to the ED, e.g. a conventional low-noise amplifier (LNA), to provide a certain amount of gain. However, this solution suffers from the cost of additional power consumption due to the active stage constantly dissipating current.
2. Placing an all-passive input impedance transformation network to transform the low source resistance of 50 Ω into a much higher value [9]. This solution is generally preferred over the first one, especially in receivers where the power consumption budget is on the order of only a few nW [9], since the impedance transformer does not consume any power. Also, the conservation of power dictates that when a source resistance is transformed from a low value to a much higher one, the source voltage is

boosted accordingly from the input to the output, leading to a certain amount of voltage gain on the signal before passing through the ED. This voltage gain is equal in dB to the resistance ratio of the input and the output of the transformation network. In addition, the transformation of a lower resistance into a much higher one with a high ratio also boosts the quality factor (Q-factor) of the network, resulting in a narrow bandwidth, which also helps with noise reduction and interference resiliency, as mentioned above [9].

Although implementing an all-passive impedance transformation network in front of the ED seems to be a promising solution, as mentioned in Chapter 3, at GHz frequencies, due to the low quality factor of passive components employed in the impedance transformer, the overall achievable gain is limited to only the range of 10 ~ 30 dB [10] whereas as shown later, the required gain before the ED typically needs to be in excess of 50 ~ 60 dB or even higher to completely nullify the noise contribution associated with the ED.

II – The Regenerative Amplifier as Potential Promising Solution and Its Nonlinear Characteristics

Interestingly, there exists a certain type of amplifier called "regenerative amplifier" (RA) that can meet these requirements. The main idea is to take a portion of the output, "re-generate" it, and send it back to the input where it adds up constructively, thereby leading to a significant increase on gain. In essence, this is equivalent to having a positive feedback path in the circuit topology. Due to the positive feedback nature, it is possible to tune the gain of an RA to an extremely high value, e.g. 60 dB, to completely nullify the contribution of the ED noises. Although an RA's noise performance might not be as good as that of a conventional LNA, as shown later, for an ED-based receiver, a conventional LNA with even a perfect noise figure

(NF), i.e. 0 dB with a gain in the range of 10 ~ 20 dB is inferior to an RA with an awful NF of 30 dB but with a gain of 50 dB. Care must be taken since having too much gain will potentially make the RA unstable, turning it into an oscillator rather than an amplifier, as shown later. Fig. 1.3 summarizes the characteristics of an RA where the gain can be tuned to be extremely high with a corresponding narrow bandwidth and a high Q-factor, and the input-output relationship becomes nonlinear at high input power. Normally, an RA will be deployed in the linear operating condition, especially near the sensitivity level where the input signal power is low. However, as proven later, when the input signal power is high enough to push the operation into the nonlinear condition, an RA with a high gain, narrow bandwidth, and a compressive third-order nonlinearity can exhibit a very interesting phenomenon where the in-band noise floor is suppressed, i.e. "noise-suppression" phenomenon, effectively leading to an improvement on the output CNR.

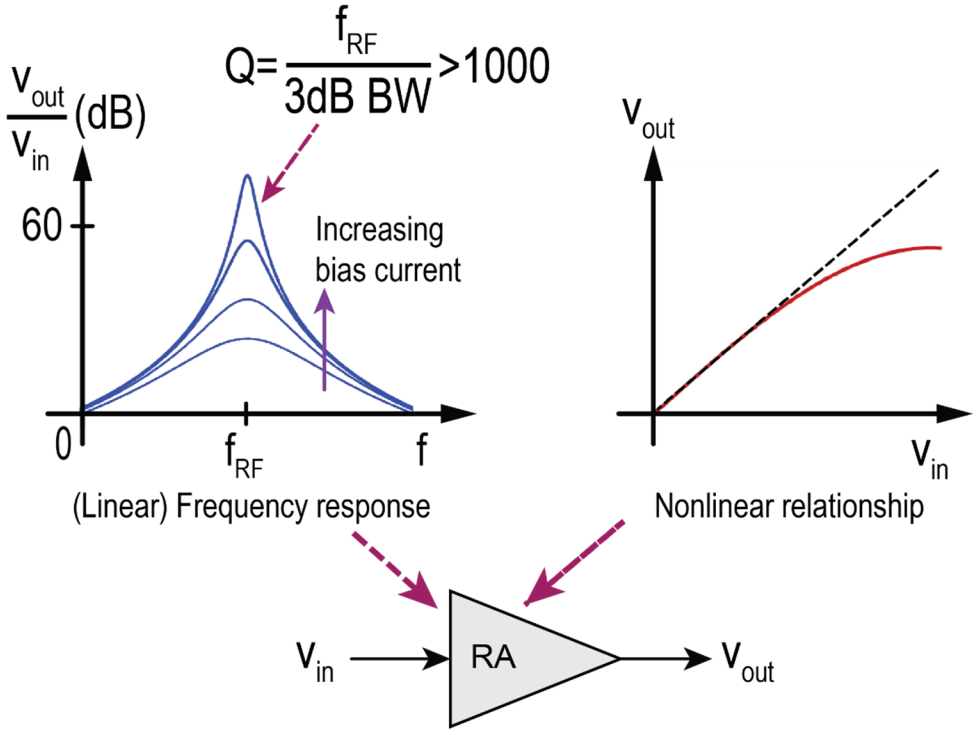


Figure 1.3: Frequency response with tunable high gain and high Q-factor and nonlinear input-output relationship of an RA.

III – Overview of the Dissertation

This dissertation will therefore examine this type of amplifier in detail, including a summary of its operation in the linear and nonlinear regimes, and then will take an in-depth look at the noise-suppression phenomenon associated with the nonlinearity of the amplifier. Lastly, the dissertation will delve into a number of different integrated applications in which an RA can be used to realize an ultra-low power and narrow-band receiver with state-of-the-art performance.

Chapter 2 analyzes the nonlinear noise-suppression phenomenon that is inherent in an RA with a high gain, narrow bandwidth, low noise, and a compressive third-order nonlinearity. Depending on the level of the input CW signal that pushes the RA into the nonlinear operation condition, the output spectrum can exhibit a suppression of the in-band noise floor, which effectively leads to an improvement on the output CNR. A promising potential application of such an interesting phenomenon can be found in electromagnetic tomography (EMT), where the scan rate of a CW signal can be maintained or improved significantly in order to obtain a high-quality image of a scanned object.

Chapter 3 presents a 2.4-GHz, OOK, ED-based receiver that employs dual differential RAs in a 65nm CMOS process. Different from conventional designs, a passive impedance transformation network is first used to transform the source resistance of 50 Ω to a very high value. And then the first RA is used to boost the quality factor of the inductor used in the passive impedance transformer to match with the transformed impedance. Hence, the high voltage gain generated by the passive impedance transformer is preserved thanks to the first RA. The second RA is then used to boost the overall gain even much further while also narrowing down the bandwidth significantly, before passing the signal through the ED. The ED is a passive topology

that is truly differential, i.e. it is not just pseudo-differential as in other state-of-the-art designs, that can add an amount of 6 dB more to the overall gain from the RF front-end to the output of the ED. The receiver operates at a data rate of 5 kbps and consumes only an ultra-low amount of power of 112 μW. The narrow bandwidth of the dual RAs also enables an impressive interference resiliency of -28 dB at a 3-MHz offset. The performance of the receiver is favorably comparable with the state of the art.

Chapter 4 discusses yet another 2.4-GHz receiver also based on dual differential RAs and an active ED with the ability to demodulate signal coherently, e.g. 16QAM in OFDM. While the dual differential RAs are largely adopted from the design in Chapter 2, the ED is an active topology that allows for flexible post-fabrication tuning to optimize the conversion gain, noise, and bandwidth performance. In addition, although the design is still based on an ED, thanks to the clever use of an external LO tone sent along with the data from the transmitter, the receiver is now capable of demodulating coherently, i.e. not only OOK, but any high-order modulations such as 16QAM, 64QAM, etc. The receiver is also implemented in 65nm CMOS and is compatible with Bluetooth Low Energy (BLE) and WiFi standards that precludes the need for a power-hungry PLL for local oscillator generation. Therefore, if employed on smart wearable devices, the ability to operate over an extended period of time with a high data throughput is greatly enhanced. The receiver is able to achieve an excellent sensitivity of -80 dBm at a very low power consumption of only 30 μW while exhibiting the highest energy efficiency among the previous BLE/WiFi-compatible state-of-the-art works.

Finally, Chapter 5 summarizes the findings of the dissertation and presents an outlook of the future work on the use of regenerative amplifiers for ultra-low power, narrow-band integrated receiver solutions.

CHAPTER 2

Noise Suppression in a Nonlinear Regenerative Amplifier

I – Overview of Behavior of RA in Nonlinear Operation Condition

The RA was invented by Armstrong in 1912 and became very successful for a short period of time until it was replaced by the super-regenerative amplifier (SRA) and later by a conventional amplifier in a super-heterodyne receiver [11]. Some modern designs still employ the concept of regeneration to improve system performance such as the works presented in [2, 3, 12 – 17]. Mainly, these designs operate the RA in a linear fashion where the input signal power is still low. As a result, the output CNR is only almost equal to the input CNR, assuming a low NF. If the input signal power is increased significantly, the RA will gradually transition into the nonlinear operation, which is typically undesirable and leads to a degradation of the NF, as shown in [18 – 21]. Under certain circumstances, the nonlinear operation can lead to an interesting phenomenon in which both the gains on the signal and on the noise begin to drop, due to signal compression; however, the gain on the noise drops faster than that on the signal, leading to a suppression of the in-band noise floor and an improvement on the output CNR.

The suppression of noise power in a nonlinear microwave amplifier has been studied in the literature. For example, in [22] the authors analyzed the behavior of a microwave amplifier in a nonlinear mode, and showed that the power spectral density (PSD) of the output noise can be reduced under large-signal operating conditions. Although the paper provided both analysis and measurement data, the assumption that the input consists of a low-frequency noise centered around DC, along with a sinusoidal signal located at a high frequency outside of the noise bandwidth, is not practical in many RF scenarios. In [23], the authors showed that for a typical

RF scenario where the desired signal is located at the center frequency of a receiver, and the noise bandwidth is also centered around the same frequency, the gain on the thermal noise drops faster than that on the signal in nonlinear operation, leading to an improvement in the signal-to-noise ratio (SNR). However, similar to [22], the analysis on the reduction of the noise is solely based on the statistical characteristics of the noise, which is involved and does not offer a lot of intuitive insight into RF behavior of microwave amplifiers. The discussion on the applications of the phenomenon is only focused on phase noise reduction, while in reality, it can be extended to a number of other applications. Lastly, the paper does not offer simulation or experimental data to support their analytical results.

This chapter attempts to fill in those gaps by providing a simple yet intuitive analytical model of the suppression of in-band noise resultant from the nonlinear operation of an RA. In the analysis, the signal and noise are represented by familiar single tones in the frequency domain for simplicity. By using tones, behaviors such as compression of signal, compression of noise, the occurrence of the "image noise" at high input power, etc. can easily be visualized and understood. Analysis, simulations, and measurement results clearly demonstrate noise suppression and improvement of CNR. Also, the paper discusses a number of important advantages and disadvantages of this concept, and discusses potential applications in which the RA can be useful.

It is worth noting that this nonlinear noise-suppression phenomenon is distinguished from conventional noise-cancellation techniques employed in some other linear amplifiers [24 – 28]. In such approaches, the amplifier still operates in the linear regime; as a result, there is no improvement on the CNR at the output. At best, it can only be the same as the CNR at the input (assuming the amplifier is noiseless).

II – Analysis of Noise Suppression in a Nonlinear Regime

A. Starting Point: A Linear Circuit Model

A general model of an RA in the linear region that is widely adopted in the literature is shown in Fig. 2.1. The input is assumed to be a current source, which includes both the input signal current and the input noise current. The RA model includes an RLC tank and an active device that generates a negative resistance. The output is taken as a voltage. For an input model that includes a voltage source along with a source resistance or impedance (i.e. a Thevenin-equivalent circuit), a Norton-equivalent circuit can readily be used to transform such an input into the model used in Fig. 2.1. In a practical RF scenario, it is generally desirable to place a low-noise amplifier (LNA) in front to isolate the regenerative circuit from the antenna, to facilitate input impedance matching, and to set the total NF of the system [2, 3, 12 – 17]. In that case, the output stage of the isolation LNA can also be transformed into the Norton-equivalent circuit shown in Fig. 2.1. The output resistance or impedance of the isolation LNA can simply be lumped into the RLC model of the RA.

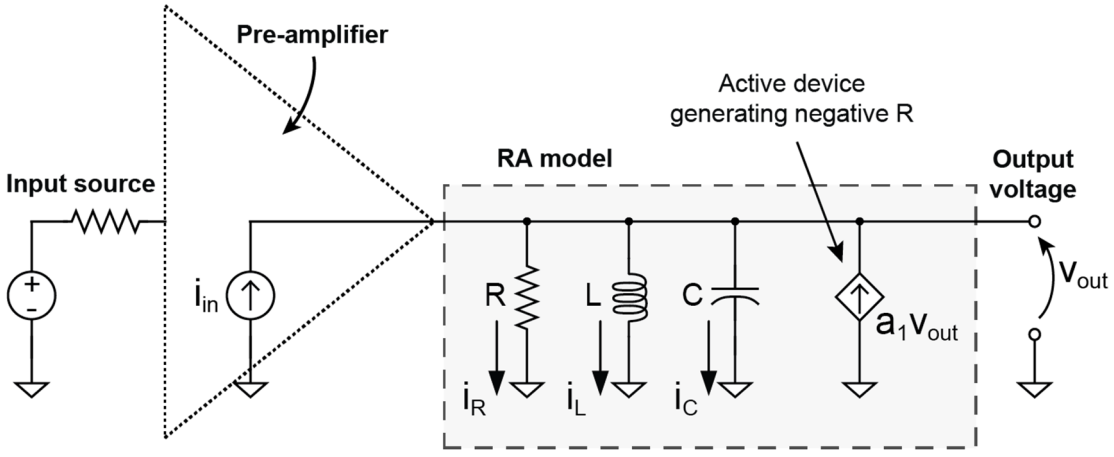


Figure 2.1: General model of the regenerative amplifier in the linear region.

The RLC tank with an equivalent lossy parallel resistor, R, sets the center frequency of the RA. The feedback current, $a_1 v_{out}$, produced by an active device, feeds an amount of output current back to the input, thereby effectively representing a negative resistance to cancel part of R, boosting the Q-factor of the LC tank and narrowing down the bandwidth. a_1 is typically the same as the transconductance of the active device.

By providing a proper amount of positive feedback, the RA can theoretically have an infinite gain along with an infinitesimally small bandwidth. The transimpedance gain at the center frequency of the RA is given by:

$$Gain = \frac{v_{out}}{i_{in}} = \frac{1}{\frac{1}{j2\pi fL} + j2\pi fC + \frac{1}{R} - a_1} = \frac{1}{\frac{1}{R} - a_1} \tag{2.1}$$

In other words, a_1 subtracts a portion of the resistance R such that the gain can be boosted significantly, as long as $\frac{1}{R} - a_1$ remains positive to maintain stability and not oscillate. In the linear regime, this gain is the same for the signal and for the noise, leading to an unchanged SNR at the output of the RA, provided that the RA is noiseless. In practice, noise introduce by the RA will of course then reduce the SNR at the output.

The frequency response of this baseline RA is shown in Fig. 2.2. The steep filtering performance of an RA can potentially help reject out-of-band noise and interference. The frequency response can easily be verified experimentally by observing the output power spectral density (PSD) on a spectrum analyzer; the noise floor at the output of the RA will simply take on the shape of the frequency response.

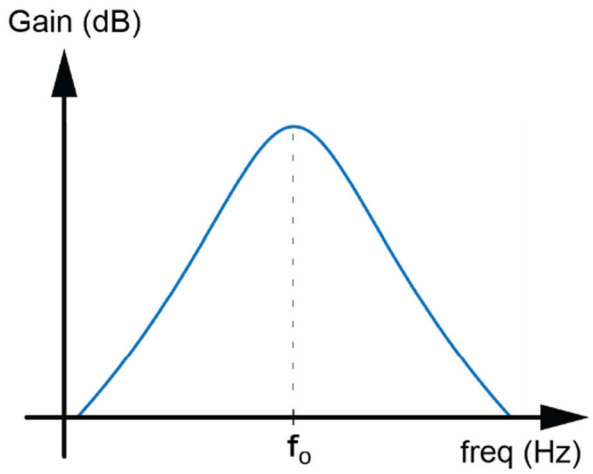


Figure 2.2: Frequency response of the RA.

B. Non-linear Modeling

As the input power to the RA increases to the point of nonlinearity, the relationships described by the circuit in Fig. 2.1 no longer hold. For example, due to the interaction of the signal and the noise, which have different amplitudes and bandwidths, the gains on the signal and on the noise are no longer the same; the noise floor at the output no longer remains constant, but is now dependent on the input signal power. In a compressively nonlinear RA, which is the typical case, it will be shown later that the noise floor in the output spectrum drops down as the input signal power increases, effectively leading to an increase in CNR if the input signal is a CW tone. A different analytical method is therefore required to predict and characterize the behavior of the regenerative amplifier under large-signal nonlinear operating conditions.

Fig. 2.3 will be used to construct the model used in this work. All proceeding analysis will consider a CW tone as the input signal. The roles of each block in Fig. 2.3 are described as follows:

- The pre-amp with high gain and a low NF is to amplify the signal to a high power to trigger nonlinearity while not degrading the original CNR significantly.

- The narrow RF bandpass filter (BPF) is to narrow down the noise BW, effectively reducing the total noise power that passes through the nonlinear block. The BPF has the same center frequency as the desired input tone.
- The nonlinear block with a certain nonlinear input-output relationship is to facilitate in-band noise suppression. The nonlinearity of this block is limited to the first-order and third- order coefficients a_1 and a_3, respectively, for simplicity, though more coefficients can be considered.

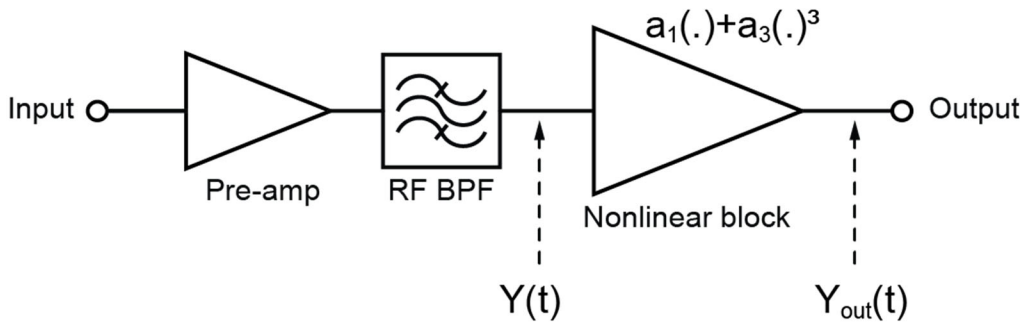


Figure 2.3: Theoretical model of the RA explicitly containing a high-gain, low-noise pre-amplifier, a narrow RF band-pass filter, and a nonlinear block.

Without loss of generality, all the blocks after the pre-amp in Fig. 2.3 are assumed to be noiseless; in some cases, thanks to the high gain of the pre-amp, the noise contributions of the subsequent stages can indeed be neglected. It is important to note that the model in Fig. 2.3 has been simplified. Practically, due to the feedback nature of the RA, even if the nonlinear device is limited to only the third-order harmonic, the mixing of the input signal and part of it that is fed from the output back to the input produces an infinite number of higher-order harmonics, leading to a much more complicated scenario.

In reality, these blocks do not necessarily exist independently, but they can co-exist. For example, due to positive feedback, the gain is extremely high, which is represented by the pre-amp, and the bandwidth is extremely small, which is represented by the RF BPF, and the

nonlinear block is always inherent to an active circuit. However, this model still serves a good starting point for the sake of analysis.

From here onwards, the analysis will be focused on the behavior of the nonlinear block. Assuming the input signal to the nonlinear block is given by:

$$S(t) = A_s(t)\cos\big(\omega_s t + \phi_s(t)\big), \tag{2.2}$$

where ω_s is the center frequency of the signal, which is the same as that of the RA.

As mentioned earlier, instead of considering wideband additive white Gaussian noise (AWGN), which will require complicated statistical analysis that will not yield much intuitive insight, a simplified model, where the input noise to the nonlinear block is represented by a single tone whose power is equal to the total integrated noise across the RA's bandwidth [29], is employed:

$$N(t) = A_n(t)\cos\big(\omega_n t + \phi_n(t)\big) \tag{2.3}$$

Here, ω_n is the center frequency of the input noise spectrum, which is equal to the center frequency of the input signal spectrum; however, for the sake of visibility and ease of analysis, ω_n is assumed to be slightly different from ω_s.

The total input to the nonlinear block is then the sum of the signal and noise:

$$\begin{aligned} Y_{in}(t) &= S(t) + N(t) \\ &= A_s(t)\cos\big(\omega_s t + \phi_s(t)\big) + A_n(t)\cos\big(\omega_n t + \phi_n(t)\big) \end{aligned} \tag{2.4}$$

The relationship between the input and output of the nonlinear block is given by:

$$y = a_1 x + a_3 x^3 \tag{2.5}$$

Although typically, a nonlinear relationship also contains the second-order nonlinearity coefficient a_2, the inclusion of that coefficient does not change the output terms since it will only generate second-order harmonic components which will either land at 0 Hz (DC) or at double the

frequency range of interest. This statement will not be accurate in a strong feedback system where the second-order harmonic is fed back and mixed with the fundamental signal, effectively affecting the amount of third-order harmonic component showing up at the output.

Assuming the nonlinear block has a compressive nature, which is the general case [30]:

$$a_1 a_3 < 0 \tag{2.6}$$

The output of the RA is given by:

$$Y_{out}(t) = a_1 Y_{in}(t) + a_3 Y_{in}^3(t) \tag{2.7}$$

$$\begin{aligned} Y_{out}(t) \quad &= a_1(A_s(t)(\cos\left(\omega_s t + \phi_s(t)\right) + \\ &+A_n(t)\left(\cos\left(\omega_n t + \phi_n(t)\right)\right) \\ &+a_3(A_s(t)\left(\cos\ \omega_s t + \phi_s(t)\right) + \\ &+A_n(t)\left(\cos\left(\omega_n t + \phi_n(t)\right)\right)^3 \end{aligned} \tag{2.8}$$

In order to simplify the above expression of $Y_{out}(t)$, the following assumptions are made:

- The input noise power is of a small amplitude, which is much smaller than that of the desired input signal,
- Only the output terms that are located around the center frequency of the RA are considered.

As a result, higher-ordered polynomial terms such as $A_n^2\ (t)$, $A_n^3\ (t)$, etc. will be negligible, and terms that will fall out of the region around the center frequency will be ignored. The output can then be simplified into:

$$\begin{aligned} Y_{out}(t) \approx &\left[1 + \frac{3}{4}\frac{a_3}{a_1}A_s^2(t)\right] a_1 A_s(t)\cos\left(\omega_s t + \phi_s(t)\right) + \\ &+\left[1 + \frac{3}{2}\frac{a_3}{a_1}A_s^2(t)\right] a_1 A_n(t)\cos\left(\omega_n t + \phi_n(t)\right) + \\ &+\left[\frac{3}{4}\frac{a_3}{a_1}A_s^2(t)\right] a_1 A_n(t)\cos\left((2\omega_s - \omega_n)t + 2\phi_s(t) - \phi_n(t)\right) \end{aligned} \tag{2.9}$$

In other words, there are only three dominant terms that show up at the output of the nonlinear block:

- the amplified signal tone $\left[1+\frac{3}{4}\frac{a_3}{a_1}A_s^2(t)\right]a_1A_s(t)\cos\left(\omega_s t+\phi_s(t)\right)$ located at the same frequency ω_s of the input signal;
- the amplified noise tone $\left[1+\frac{3}{2}\frac{a_3}{a_1}A_s^2(t)\right]a_1A_n(t)\cos\left(\omega_n t+\phi_n(t)\right)$ located at the same frequency ω_n of the input noise;
- and an "image noise" tone $\left[\frac{3}{4}\frac{a_3}{a_1}A_s^2(t)\right]a_1A_n(t)\cos\left((2\omega_s-\omega_n)t+2\phi_s(t)-\phi_n(t)\right)$, which lands on the frequency of $2\omega_s-\omega_n$ and is a third-order intermodulation component of the input signal tone and the input noise tone.

These dominant output tones are visualized in Fig. 2.4, along with the input tones of the nonlinear block.

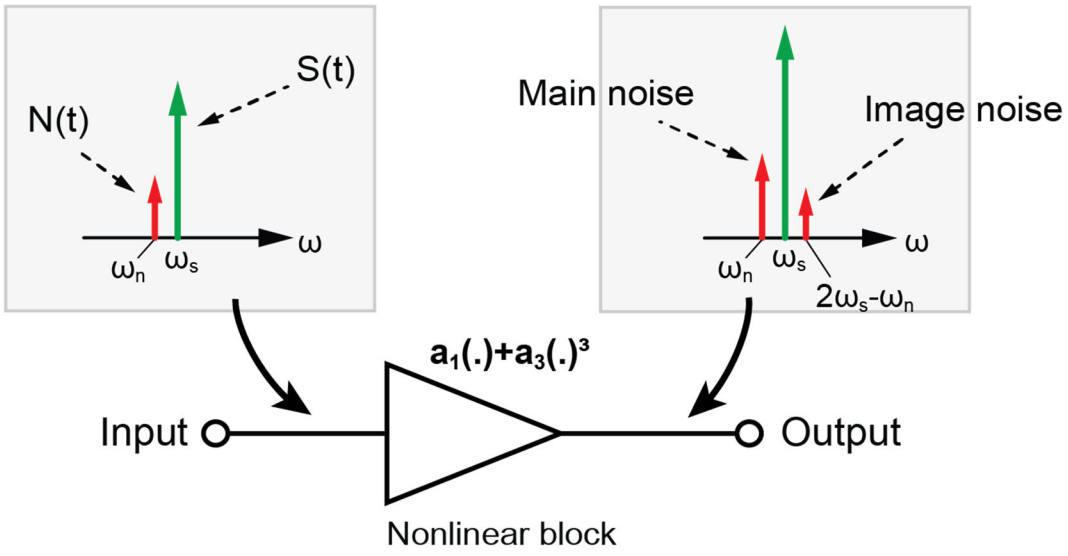


Figure 2.4: Input tones and dominant resultant output tones of the nonlinear block in the frequency domain, respectively.

Assuming the total gain of the pre-amp and the RF BPF at the center frequency is G, the overall effective gain on the signal of the entire RA can be given by:

$$G_{signal} \approx G \times a_1 \left[1 + \frac{3}{4}\frac{a_3}{a_1} A_s^2(t)\right] \tag{2.10}$$

Since the image noise is uncorrelated with the main output noise, the overall effective gain on the noise of the entire RA can be given by:

$$G_{noise} \approx \sqrt{F} \times G \times a_1 \sqrt{\left[1 + \frac{3}{2}\frac{a_3}{a_1} A_s^2(t)\right]^2 + \left[\frac{3}{4}\frac{a_3}{a_1} A_s^2(t)\right]^2} \tag{2.11}$$

Here F is the noise factor of the pre-amp, i.e. the NF in the linear scale.

It is instructive to also look at the ratio of the input CNR to the output CNR of the entire RA. From (2.10) and (2.11), this ratio can then be given by:

$$\frac{CNR_{in}}{CNR_{out}} \approx F \times \frac{\left[1 + \frac{3}{2}\frac{a_3}{a_1} A_s^2(t)\right]^2 + \left[\frac{3}{4}\frac{a_3}{a_1} A_s^2(t)\right]^2}{\left[1 + \frac{3}{4}\frac{a_3}{a_1} A_s^2(t)\right]^2} \tag{2.12}$$

Although the above analysis has been done using a single tone to represent the band-limited input white Gaussian noise, it is worth noting that the same results can also be obtained for a two-tone equivalent of the input noise symmetrical to the input signal tone, provided that the total power of the two noise tones are the same as that of the single noise tone.

The next sub-section will describe an RA simulation model to verify the above analysis. It will also discuss the behavior of Equations (2.10), (2.11), and (2.12) when the CW input power P_{in} increases from the linear regime into the nonlinear regime. Lastly, it will show how the $\frac{CNR_{in}}{CNR_{out}}$ decreases when P_{in} increases, leading to an augmentation of the output CNR.

C. Analytical and Simulation Results

In order to verify the analytical results in the previous sub-section, an RA circuit has been implemented in Advanced Design System (ADS) as shown in Fig. 2.5. To facilitate transient simulation on the circuit without sacrificing the generality of the simulation, a center frequency of 200 kHz has been chosen. The pre-amplifier is simply an ideal LNA block with a gain of 100 dB and a NF of 0.8 dB. The LC tank has a Q-factor of about 16 to obtain a 3dB-bandwidth of approximate 12.5 kHz around the center frequency. The nonlinear block has coefficients a_1 and a_3 of 0.1 and -10, respectively. As mentioned shortly, this choice of $\frac{a_1}{a_3}$ ensures the compressive nature of the nonlinear block (2.6), which is essential for noise suppression to happen. It is worth noting that this simulation model assumes a white Gaussian noise at the input of the RA.

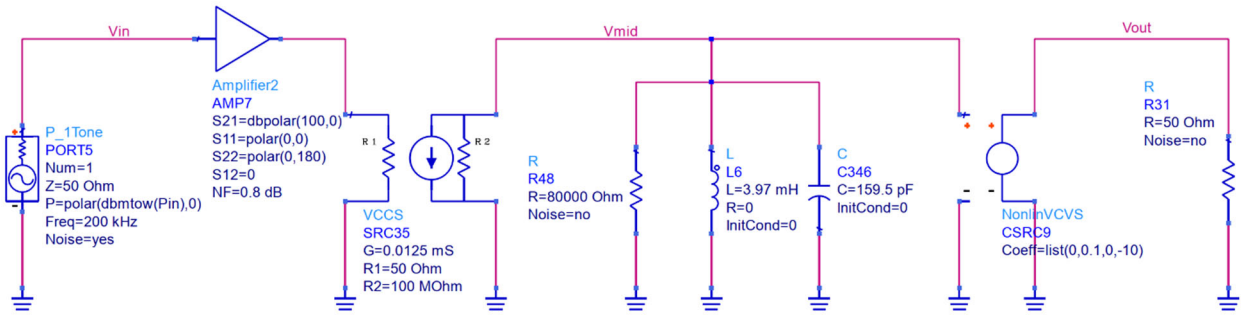


Figure 2.5: RA circuit to simulate the noise-suppression phenomenon.

When the input signal is assumed to be a purely sinusoidal (CW) signal, the amplitude $A_s(t) = A_s$ is now a constant and is directly related to the input signal power P_{in}. In this case, Fig. 2.6 shows a plot of the effective gains on the signal and on the noise, obtained from (2.10) and (2.11), and the ratio of the input CNR to the output CNR from (2.12), as a function of the input signal power. In Fig. 2.6, the analytical results and the transient simulation results are compared with each other. It is clear that the simulation results are in excellent agreement with

the theoretical analysis, which verifies the use of a single tone for the input noise to analyze the RA's nonlinear behavior, rather than using a traditional representation of a band-limited white noise as done in [22] and [23]. In Fig. 2.6, it can be seen that as the input power P_{in} is still small, the RA operates in the linear region and the gains of the signal and the noise are constant; and the ratio of $\frac{CNR_{in}}{CNR_{out}}$ remains constant and is equal to the pre-amplifier's NF. This is when A_s is still small in (2.10) and (2.11).

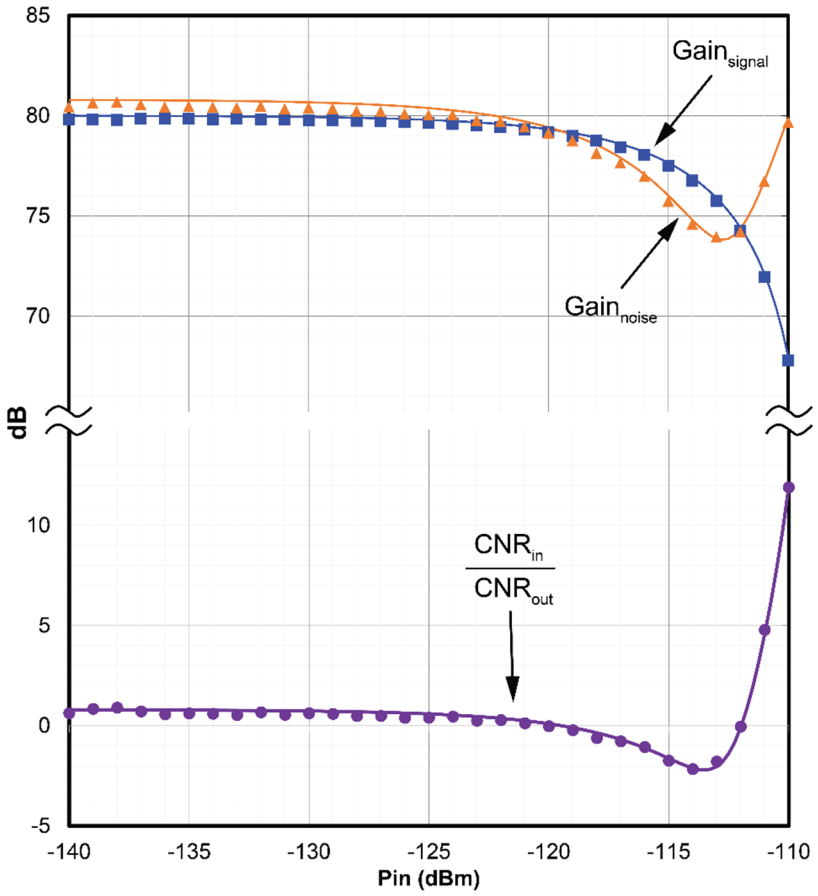


Figure 2.6: Analytical results (lines) and transient simulation results (symbols) of the overall effective gains on signal and noise, and the ratio $\frac{CNR_{in}}{CNR_{out}}$, respectively, as functions of the CW input power to the RA.

However, as P_{in} increases, the RA transitions into the nonlinear regime and the gains on the signal and on the noise start to drop, i.e., A_s becomes more significant, resulting in the

decreases of G_{signal} and G_{noise} in (2.10) and (2.11) due to the negative sign of $\frac{a_3}{a_1}$. In addition, due to the different factors associated with $\frac{a_3}{a_1}A_s^2$ in (2.10) and (2.11), the gain on the noise drops faster than that on the signal, leading to an improvement on the CNR of up to 3 dB. This is the phenomenon of noise suppression. When the input CW power increases even further, the "image noise" tone starts to become significant, thereby pushing the total output noise power back up. This is when the term $\frac{3}{4} \times \frac{a_3}{a_1}A_s^2$ becomes significant in (2.11) and (2.12). As a result, there exists a certain limit beyond which the noise suppression and the CNR improvement will disappear. Practically, this limit can be tuned based on the gain of the pre-amp and the bandwidth of the RF BPF. In addition, the onset of noise suppression can also be tuned accordingly, depending on the pre-amp's gain and the RF BPF.

This scenario can also be explained alternatively: in the case when the input to the nonlinear device consists of two CW tones: one with a lower power (noise) and the other a higher power (signal). At the output, due to the compressively nonlinear nature of the RA, both tones will be compressed, but the weaker tone will be compressed more heavily than the stronger one. This situation is similar to the "desensitization" of an RF receiver where a weak desired signal is accompanied by a strong nearby interference [31]. In the case of the RA, the input signal acts as a strong "interference" and the input noise acts as a weak "desired signal". To facilitate this condition, the RF BPF placed in front of the nonlinear block narrows down the noise bandwidth, thereby effectively reducing the power of the input noise tone to the nonlinear block, making it easier for noise suppression to happen.

Fig. 2.7 depicts the simulated output spectrum of the RA circuit in three scenarios when wideband AWGN noise is present at the input: (a) when there is no input signal; (b) when there is a weak CW input of -140 dBm; and (c) when there is a sufficiently strong CW input of -113

dBm, respectively. Also shown in Fig. 2.7 (d) is the amount of noise floor suppression in dB near the center frequency as a function of the input power. Initially, when there is no input signal, the output noise floor is fixed at a certain level; the output PSD is simply the noise level that takes on the shape of the linear frequency response of the RA, which is centered at 200 kHz with a 3dB-bandwidth of 12.5 kHz. This level remains constant even when there is a weak CW input such that the RA remains in the linear regime. However, as the CW input power increases to the point of nonlinearity, the RA starts to enter into the nonlinear regime. As can be seen, the noise floor at the output of the RA is suppressed. It should be noted that the gain is not adjusted between these tests. Here, the higher the input power, the more the noise floor is pushed down, effectively leading to an increase in CNR. However, as mentioned earlier, in this particular RA model, there is a limit of P_{in} beyond which the noise floor starts to go back up, nullifying the improvement on the CNR.

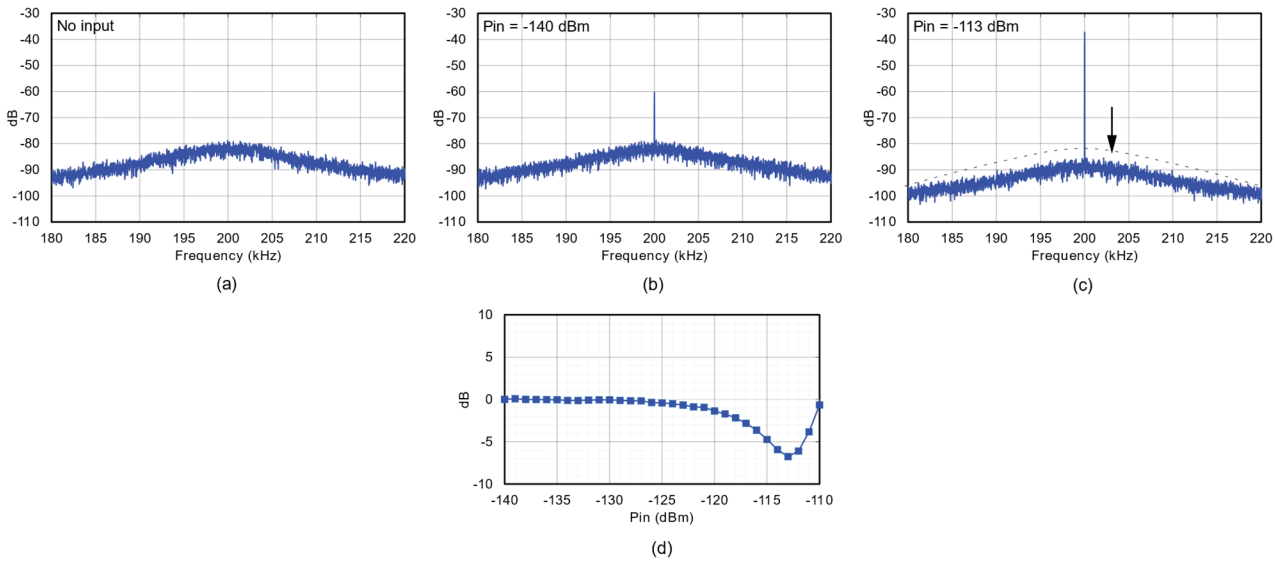


Figure 2.7: Simulated output PSD of the RA when: (a) there is no input, (b) there is a weak CW input with power of -140 dBm, and (c) there is a sufficiently strong CW input with power of -113 dBm. (d) Amount of noise floor suppression as a function of the input power.

III – Experimental Measurement of Noise Suppression

An experimental discrete RA has been implemented to verify the concept of noise suppression in the nonlinear operating regime. Fig. 2.8 shows the schematic of the RA, which can be broken down into three parts:

- First, a two-stage pre-amplifier is designed using two cascaded common-emitter amplifiers. The first stage is an inductively degenerated amplifier which provides input impedance matching to achieve a high gain and a low NF of around 0.8 dB. Along with the second stage, the overall pre-amplifier provides a sufficiently high transconductance gain to push the RA into the nonlinear regime at relatively small input signal power. The high gain also ensures that the overall NF of the entire RA will be dominated by this pre-amp. This acts as the pre-amp block in the theoretical model of the RA in Fig. 2.3. Both the bipolar-junction transistors (BJT) transistors in the two stages are BFP842ESD [32] with an extremely high transition frequency of 57 GHz for ultra-low-noise RF applications. The gain of the pre-amplifier can be tuned by changing the base bias voltages. The center frequencies of the two stages can also be tuned by discrete variable capacitors.
- A differential cross-coupled pair (i.e. the RA core) provides a negative resistance to boost the Q-factor of the resonant tank of the second stage of the pre-amplifier [30], thereby narrowing down the RA bandwidth around the center frequency as well as providing the primary nonlinear relationship through the two discrete BJTs. As a result, the cross-coupled pair acts both as a narrow-band BPF and as a nonlinear block in the theoretical model of Fig. 2.3. The two BJT transistors used here are the matched BFU520Y [33]. The amount of negative resistance generated by this cross-

coupled pair, which dictates the overall narrow bandwidth, can be tuned by changing the bias voltage on the drain or the base. A pair of varactor diodes (SMV1251 [34]) connected to the cross-coupled pair are used to tune the center frequency of the overall RA circuit. Fig. 2.9 shows the conversion of the RA core schematic into a similar model as used in Fig. 2.3. A similar conversion of the nonlinear differential cross-coupled pair can also be found in [35].

- The output buffer provides a connection to the output port with good reverse isolation to avoid affecting the sensitive operating condition of the RA core. The buffer also consists of a capacitive attenuator at the input to ensure that its nonlinearity does not significantly affect the CNR at its input. The buffer is also implemented in a common-emitter configuration using the BFP842ESD.

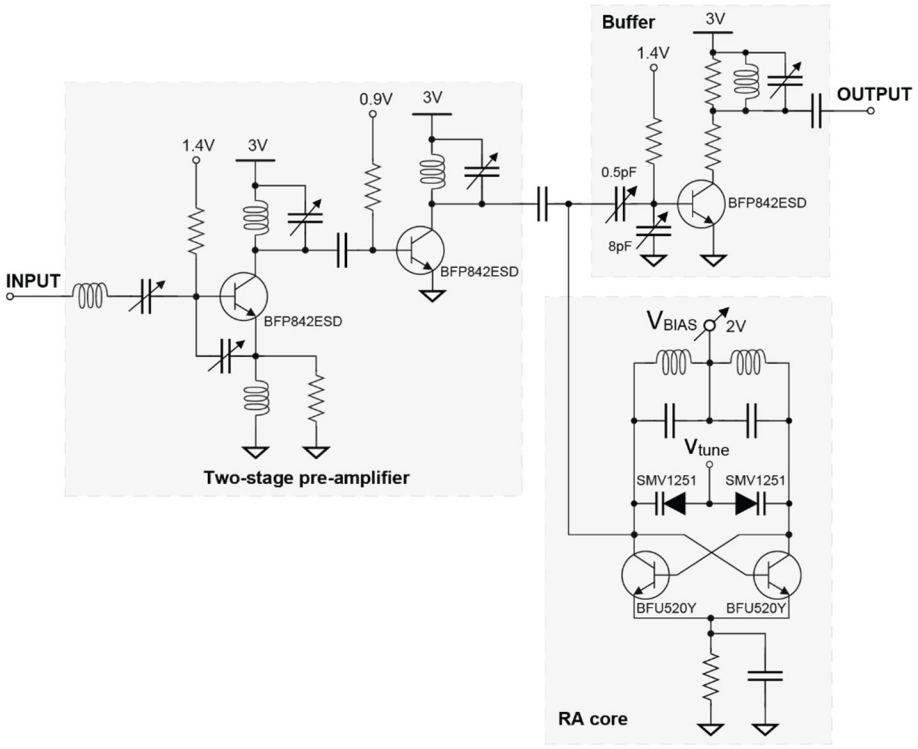


Figure 2.8: Schematic of the experimental discrete RA operating at 87 MHz.

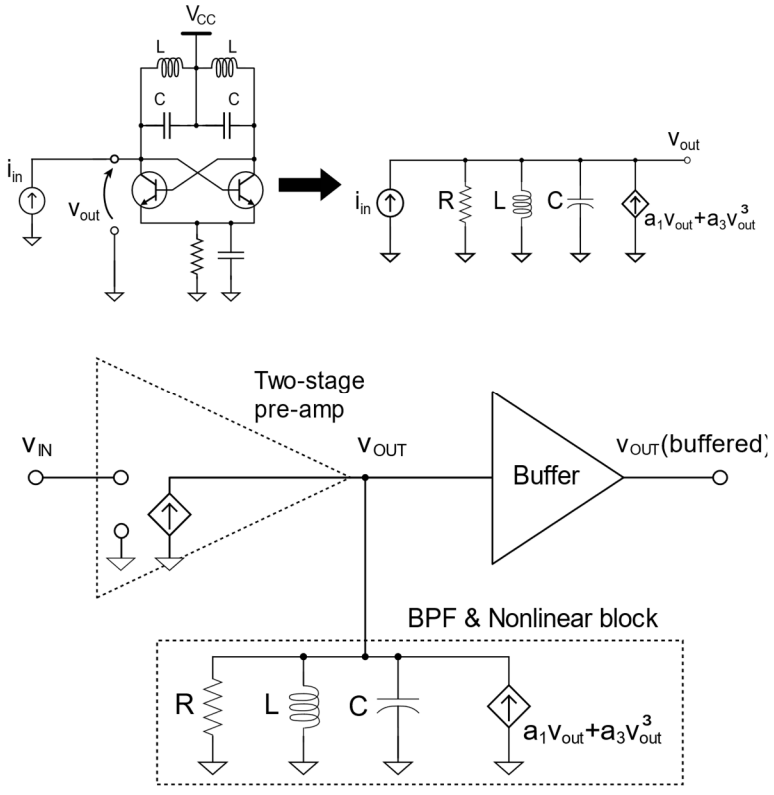


Figure 2.9: Converting the schematic of the experimental discrete RA into the equivalent original analytical model.

The center frequency of the three stages of the RA is tuned to approximately 87 MHz. The bias voltage of the cross-coupled pair is tuned to obtain a 3dB-bandwidth of around 12.5 kHz, which indicates an effective Q-factor of around 7000. With these conditions, the overall gain of the RA is around 80 dB at the center frequency, which facilitates noise suppression at relatively low input powers. Fig. 2.10 shows the simulated total gain and NF of the RA as a function of the tuning bias voltage of the cross-coupled pair. It is clear that the RA can be tuned to achieve a high gain and a narrow bandwidth while the NF is essentially unchanged.

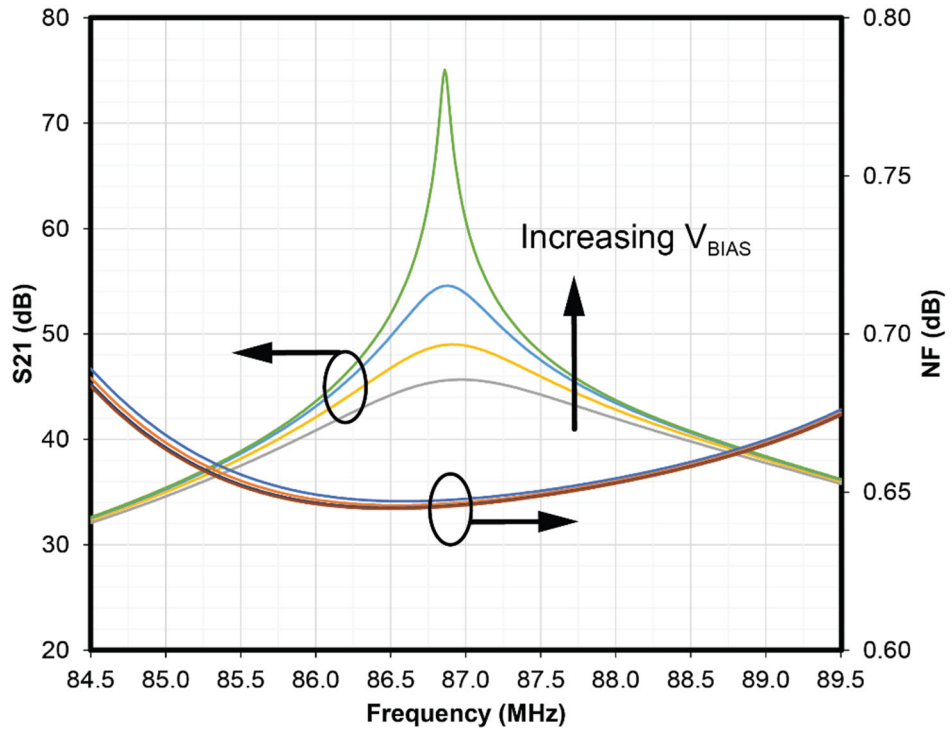


Figure 2.10: Simulated total gain and NF of the experimental 87MHz RA as a function of the bias voltage on the cross-coupled pair.

Fig. 2.11 shows a photograph of the experimental discrete RA. The RA's input is connected to an RF signal generator while its output is observed on a spectrum analyzer. It is worth noting that proper filtering on the bias voltages and the power supplies connecting to the RA is critical to prevent the 60 Hz noise from mixing up to around the RA's center frequency

due to its extremely high gain and nonlinearity, potentially corrupting the CNR. The CW input power from the signal generator is swept from -144 dBm to -50 dBm. In order to properly compute the in-band noise power to obtain the CNR from the spectrum analyzer, the bandwidth within which the noise power is integrated is chosen in the vicinity of the center frequency, e.g. 100 Hz around 87 MHz. Within this small bandwidth, the noise floor is essentially flat and the integrated noise power is simply the product of the PSD of the noise near the center frequency and this chosen bandwidth. When computing the ratio of the input CNR to the output CNR, due to the common chosen bandwidth for noise power integration that shows up both on the numerator and on the denominator, one can simply ignore this bandwidth and only consider the PSD of the noise near the center frequency. In addition, due to the random nature of noise, averaging multiple measurements is performed to obtain the mean values of noise power and CNR. The video bandwidth (VBW) of the spectrum analyzer is also set to be small enough to easily compute the noise power [36].

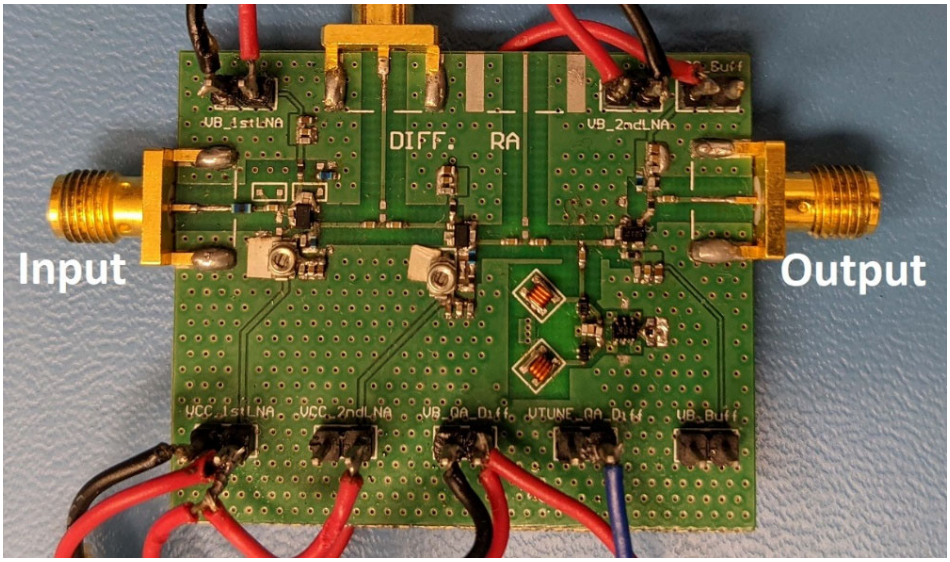
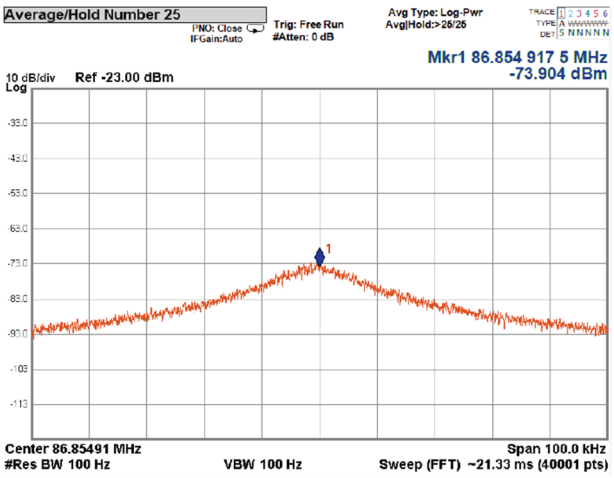
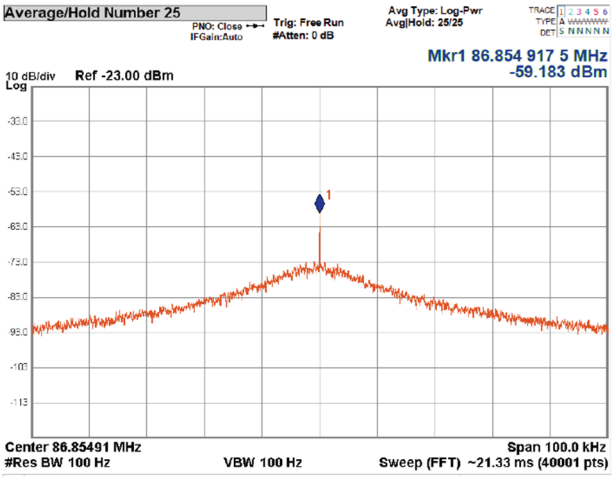


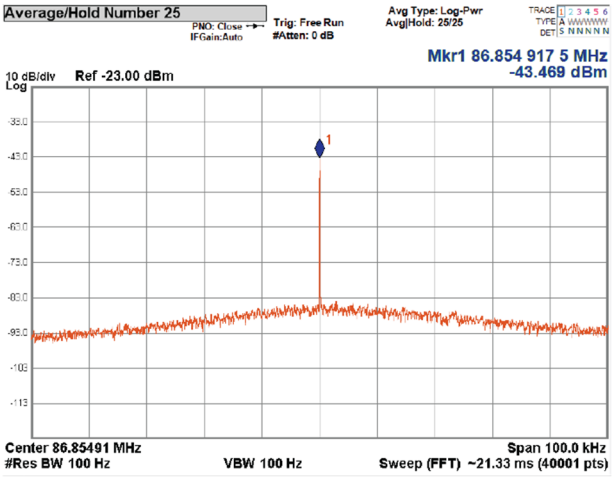
Figure 2.11: Photograph of the discrete RA operating at 87 MHz.



(a)



(b)



(c)

Figure 2.12: Measured output spectra of the RA (a) when there is no input signal; (b) when there is a weak input CW signal of -140 dBm; and (c) where there is a sufficiently strong input CW signal of -115 dBm, respectively.

Fig. 2.12 shows the output spectra of the RA in three different cases: (a) when there is no input signal; (b) when there is a weak input CW signal of -140 dBm; and (c) when there is a sufficiently strong input CW signal of -115 dBm, respectively. It is clear that the output noise floor near the center frequency, in the presence of a sufficiently strong input CW signal, can be suppressed by 10 dB or more, demonstrating the noise suppression phenomenon. Fig. 2.13 shows the measured gains on the signal and the noise, and the ratio of the input CNR to the output CNR, respectively, when a CW input is used. Initially, the gain on the signal and the gain on the noise differ by an amount approximately equal to the measured NF; in other words, the ratio $\frac{CNR_{in}}{CNR_{out}}$ in the linear regime is around 0.8 dB. However, as the input CW power increases, the gain on the noise drops faster than that on the signal, effectively leading to a CNR amplification of up to 3 dB as expected. At even excessively higher input powers, the gain on the noise starts to catch up with that on the signal, thereby degrading the improvement on the CNR. Hence, the existence of CNR improvement only exists within a certain range of input power. This behavior has been predicted in the analysis and simulation.

Overall, the measurement agrees quite well with simulation results, with a small exception where the CNR improvement extends further than simulated. This can be attributed to the feedback nature of the amplifier. It is inevitable that nonlinear devices must be placed in a positive feedback loop in order to create such an extremely narrow bandwidth around a high RF frequency. As a result, as mentioned earlier in the paper, higher-order terms generated by the non-linear devices start to kick in at high input powers, effectively nullifying the assumption that the nonlinear relationship is only limited to the third order. As a result, it is difficult to predict the behavior of the RA beyond this point. Another contributor of the discrepancy is that the pre-amplifier also introduces a certain amount of distortion and compression on the signal before it

hits the nonlinear block. In addition, the buffer is subjected to high input power and therefore also distorts the result to some extent due to its nonlinearity. Lastly, discrete component models also typically contain a certain amount of inaccuracy.

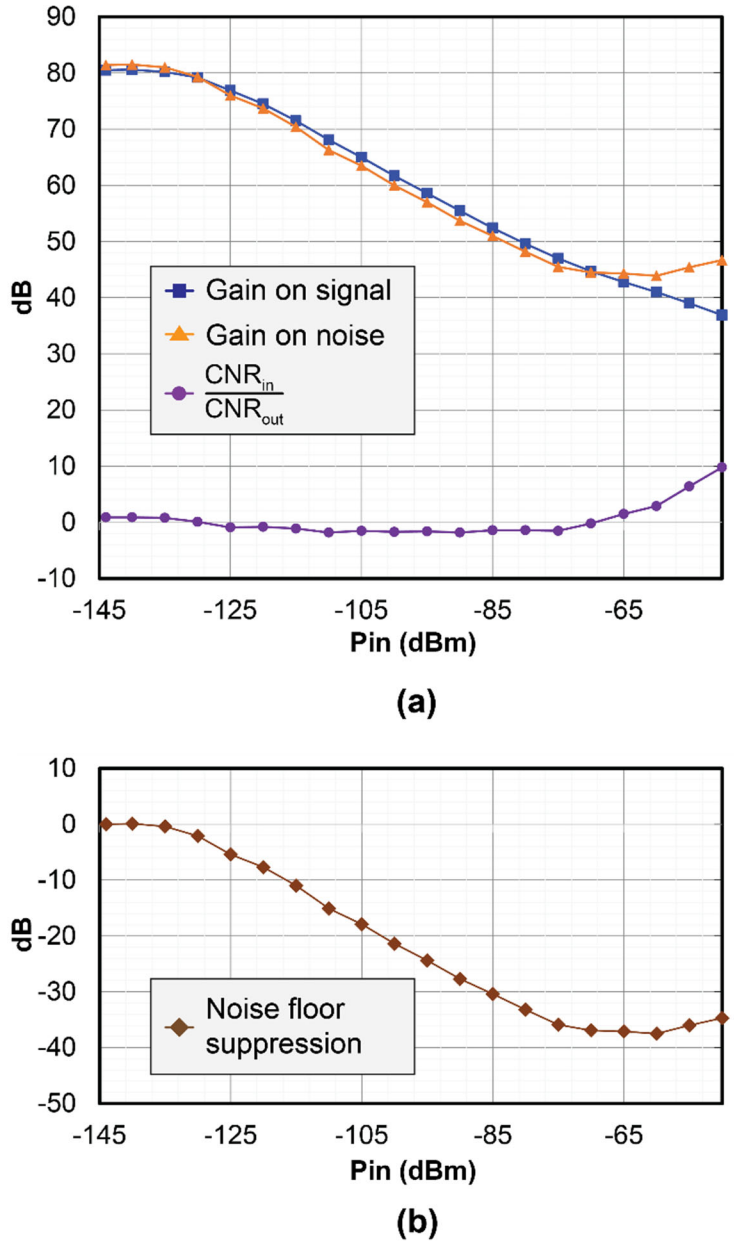


Figure 2.13: (a) Measured effective gains on signal and noise, the ratio of $\frac{CNR_{in}}{CNR_{out}}$; and (b) Measured amount of noise-floor suppression, respectively, as a function of the input CW signal power, at the center frequency of 87 MHz.

The presented design was not meant to be a competitive, state-of-the-art solution, but was instead built simply to experimentally demonstrate the noise suppression phenomenon. With that said, Table 2.1 summarizes the key performance metrics of the RA in comparison with some other LNA's and microwave amplifiers in the literature to show that while other LNA's and amplifiers have been constructed with super-regenerative and/or noise cancellation circuitry, these are distinct from the noise suppression phenomenon shown in this chapter.

Table 2.1: Comparison with other LNA's and microwave amplifiers.

	[37]	[4]	[26]	[28]	**This work**
Noise-reduction technique	None	None	On-antenna linear noise cancellation	Linear noise cancellation	**Nonlinear noise suppression**
Amplifier type	Super-regenerative amplifier	Super-regenerative amplifier	Common gate & Common source with g_m boosting	Inverter-based with dual resistive feedback	**Regenerative amplifier**
Frequency	400 MHz	900 MHz	80 GHz	Up to 2.6 GHz	**87 MHz**
Signal type	OOK	OOK	Arbitrary	Arbitrary	**CW**
NF	>1.2 dB	6.2 dB (simulated)	4.6 dB (minimum)	1.56 dB (minimum)	**0.8 dB (linear regime)**
Power consumption	>2 mW	0.273 mW	46 mW	6 mW	**43 mW**
$\frac{CNR_{out}}{CNR_{in}}$	No demonstrated improvement	No demonstrated improvement	No demonstrated improvement	No demonstrated improvement	**Up to 3 dB of improvement**

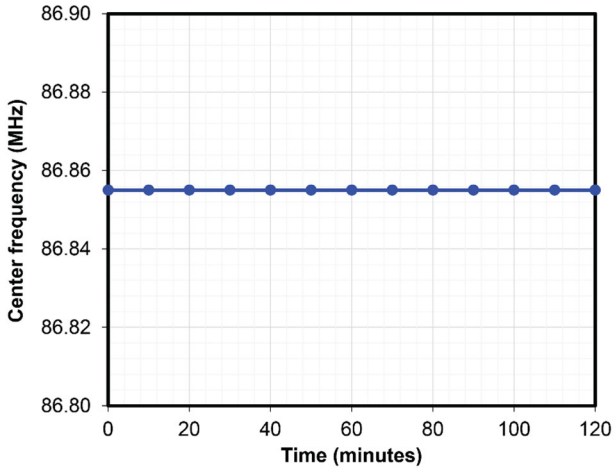


Figure 2.14: Measured instantaneous center frequency of the experimental RA for a two-hour period during which it also remains stable and does not go into an oscillatory mode.

IV – Advantages, Disadvantages, and Potential Applications of Noise Suppression in Nonlinear Regenerative Amplifier

Inherently, the RA possesses a number of advantages in the linear operation such as:

- High gain and relatively low noise, which helps nullifying the noise contribution of the subsequent stages in a receiver.
- Narrow bandwidth which acts as a high-Q, sharp filter and helps reject out-of-band noise and interference, relaxing the linearity requirements of the subsequent stages. In addition, if used in a super-heterodyne receiver, the need for an external off-chip bulky image-reject filter can potentially be eliminated [30].
- Relatively low power consumption.

However, it is worth mentioning that due to the positive feedback that leads to a narrow bandwidth of the RA, potential instability issues can arise in practice, especially when the bandwidth is unduly narrow, which leads to the challenge of keeping the center frequency stable and preventing the RA from becoming oscillatory. Nonetheless, as long as the amount of positive feedback is not significant, the RA can still be stable enough to operate as an amplifier and not go into an oscillatory mode, as demonstrated in prior work [2, 3, 12 – 17]. To verify the stability of the experimental 87MHz RA in this work, Fig. 2.14 shows a time-series measurement of the instantaneous center frequency of the RA for a period of two hours. It can be seen that the instantaneous center frequency is essentially unchanged. During this measurement, the RA has remained stable and has not gone into an oscillatory mode.

In some cases, when the bandwidth of the RA is required to be significantly narrow, depending on a specific application, a frequency and/or amplitude calibration procedure can be performed prior to the operation of the RA to sporadically monitor and adjust the center

frequency as well as to ensure the amplifier does not become an oscillator. Similar approaches have been employed in the literature [1, 4, 37, 38]. Although these approaches have been used mostly on a super-regenerative amplifier, they can be applied to a regenerative amplifier.

According to the above analysis, the RA can also potentially be useful in the nonlinear regime thanks to its ability to suppress the in-band noise floor, effectively leading to an enhancement of the CNR. As discussed previously, a potential application of this mode of operation is for the detection of CW signals located within an uncertain analysis bandwidth. However, when the input signal is no longer purely a CW tone but is a signal with phase and amplitude modulation, one caveat is that along with the suppression of the in-band noise, the nonlinearity also generates in-band distortion that is difficult to remove from the output signal. This in-band distortion effectively reduces the overall signal-to-noise-and-distortion ratio (SNDR), thereby nullifying the benefit of noise suppression.

As shown in (2.9), the distortion in the fundamental output term is associated with the component $\frac{3}{4} \times \frac{a_3}{a_1} A_s^2(t)$ in the signal amplitude where $A_s(t)$ is no longer a constant but is time varying. The spectrum of the output signal in this scenario is depicted in Fig. 2.15. Thus, application of noise suppression requires a system where the signal is very narrowband relative to the analysis bandwidth.

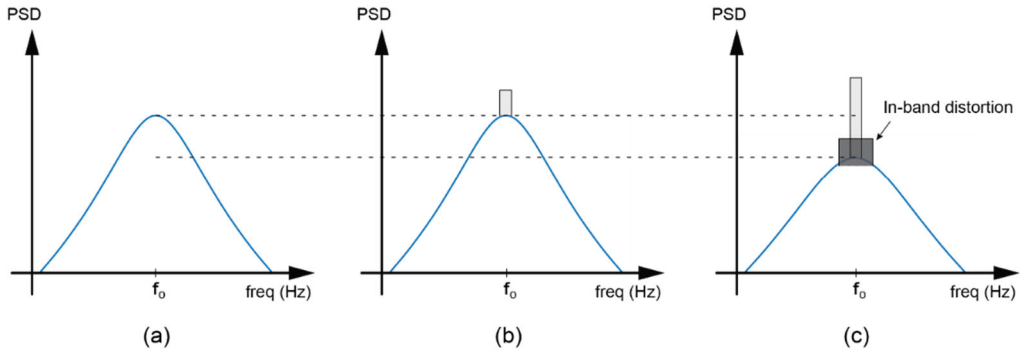


Figure 2.15: The output PSD of the RA when: (a) there is no input, (b) there is a weak modulated input signal, and (c) when there is a sufficiently strong modulated input signal.

As an excellent CW tone detector, a promising application of the RA is in electromagnetic tomography (EMT), where the excitation is normally a CW tone at microwave frequencies and the detector is an array of antennas. Due to the dielectric properties of the object being scanned, e.g., a human brain, altering the electromagnetic signal penetrating through it, an image of the internal structure of the object can be reconstructed from the received scattering signals obtained by the antennas [39 – 43]. In this modality when the object is a human brain, for example, the scan rate is of critical importance to obtain an image rapidly. The scan rate and the quality of the reconstructed image are directly correlated to the SNR. To achieve a high SNR, it is often desirable to reduce the resolution bandwidth (RBW) of the detector in order to push the noise floor down [36]. However, the RBW is also directly related to the time required to scan a signal, as given by [36]:

$$T = k\frac{f_{span}}{RBW^2}, \tag{2.13}$$

where T is the scan time, k is a proportionality factor, and f_{span} is the span of the frequency range that contains the signal of interest. Hence, with a normal EMT detector, the scan rate might be undesirably slow. However, when the RA is used as an amplifier that receives the CW signal from the receiving antennas of the EMT device, it offers the benefit of noise suppression.

As discussed earlier, the onset of the noise suppression can also be tuned such that a weak CW signal can still trigger noise suppression. Thus, an improvement on the SNR can be achieved. The end result is that the EMT device can now still take advantage of a higher RBW while not sacrificing the image quality to properly scan a CW signal for further processing, effectively leading to a faster scan rate. For example, with all other factors being held constant, a 3-dB improvement on the SNR resulting from noise suppression translates directly to a 6-dB improvement on the scan rate. Future work will investigate using an RA in such an application.

V – Conclusion

In conclusion, the suppression of the noise floor in the nonlinear regime of a high-gain, narrow-band RA has been analyzed simply by utilizing a polynomial nonlinear relationship of the third order, where the narrow-band, Gaussian noise is represented by a single tone in the frequency domain. The analysis has been verified by transient simulation of a simplified RA circuit model. In addition, the suppression of the noise floor by an in-band CW input has been shown experimentally by observing the output spectrum of a nonlinear RA on a spectrum analyzer. Even when accounting for the signal compression, an improvement in CNR is demonstrated. Lastly, potential applications of the RA with noise suppression have also been suggested; most notably, a CW-tone detector in electromagnetic tomography.

Acknowledgements

Chapter 2, in part, is based on the material as it appears in B. H. Lam, P. Gudem and P. P. Mercier, "Analysis and Measurement of Noise Suppression in a Nonlinear Regenerative Amplifier," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022, doi: 10.1109/TCSI.2022.3184924. The dissertation author was the primary researcher and author of this paper.

CHAPTER 3

An Ultra-Low Power, Low Data-Rate, 2.4GHz, OOK Receiver Based on Dual Regenerative Amplifiers

I – Ultra-Low Power, ED-Based Receivers and Existing Challenges

Conventionally, a super-heterodyne receiver is used to receive and demodulate signal coherently with both amplitude and phase information. Fig. 3.1 shows the simplified block diagram of such a receiver. It consists of the first LO (local oscillator) to linearly down-convert the RF signal into an intermediate-frequency (IF) domain. Another LO is used to coherently demodulate the signal in order to extract the in-phase (I) and the quadrature (Q) components separately. The phase component of the modulated signal is preserved throughout the entire demodulation process. In addition, the super-heterodyne receiver typically has excellent overall performance, including noise and sensitivity, albeit with a higher power consumption and more design complexity.

Nowadays, for applications in emerging areas such as wireless sensor networks, smart wearables, implantable medical devices, etc., radio receivers typically do not need to communicate over a long distance or with a high data rate. In fact, receivers deployed in these areas are generally ultra-low power and low data rate, which means the focus is placed more on power efficiency to extend battery lifetime rather than high data throughput. Fig. 3.2 shows the block diagram of a typical direct-conversion envelope-detection receiver, which is ubiquitous in ultra-low power solutions. As can be seen, in contrast to the super-heterodyne receiver, an envelope-detection receiver does not typically contain an LO since the down-conversion directly to DC is done via the envelope detector (ED). In addition, the design of the ED-based receiver is

much simpler with a much lower power consumption, although the noise performance is typically inferior and the modulation is usually limited to only amplitude modulation such as on-off keying (OOK). Table 3.1 compares the pros and cons of this type of receiver with its super-heterodyne counterpart. The bottom line here is that for ultra-low power, low-data-rate receivers, envelope detection is typically the way to go.

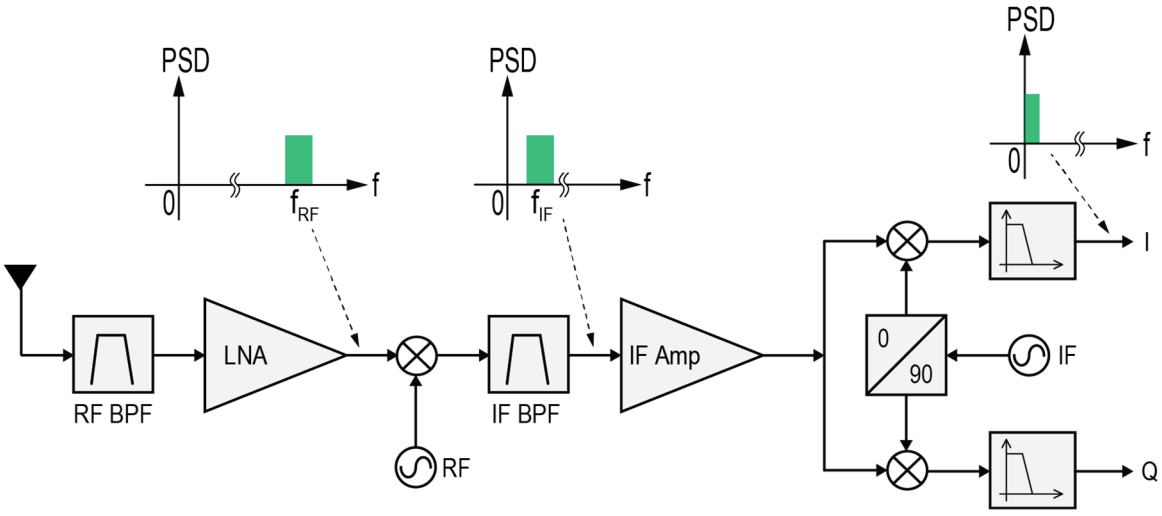


Figure 3.1: Block diagram of a conventional super-heterodyne receiver.

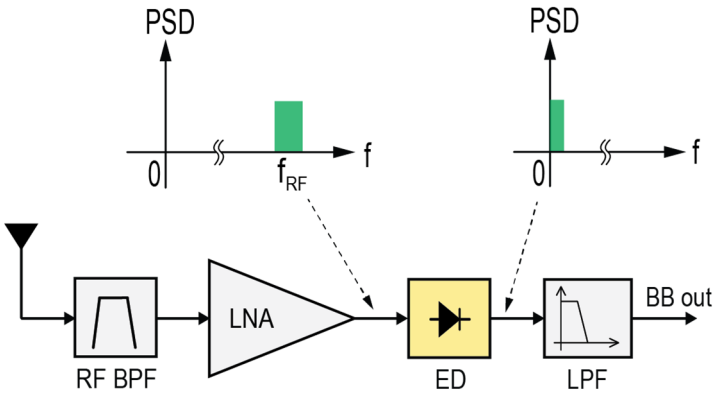


Figure 3.2: Block diagram of a typical direct-conversion envelope-detection receiver.

Table 3.1: Comparison between the super-hetero receiver and the envelope-detection receiver.

COMPARISON	Super-het RX	Envelope RX
Coherent detection	✓	✗
Good noise performance	✓	✗
Low power	✗	✓
Simplicity	✗	✓

Fig. 3.3 depicts the down-conversion of an RF signal into DC by an ED. The ED typically exhibits the following squaring operation:

$$y = k_{ED}x^2 \tag{3.1}$$

Assuming the input to the ED is given by:

$$x = A(t)\,cos\big(\omega_{RF}t + \phi(t)\big) \tag{3.2}$$

The output of the ED is then:

$$y = k_{ED}\big(A(t)\cos\big(\omega_{RF}t + \phi(t)\big)\big)^2 \tag{3.3}$$

$$y = \frac{1}{2}k_{ED}A^2(t) + \frac{1}{2}k_{ED}A^2(t)\cos\big(2\omega_{RF}t + 2\phi(t)\big) \tag{3.4}$$

With a low-pass filter (LPF) that follows the ED, only the DC-centered term at the output will be retained, leading to a final output of:

$$y = \frac{1}{2}k_{ED}A^2(t) \tag{3.5}$$

As a result, the phase component of the input is no longer present. Therefore, the ED receiver is only mainly suited to amplitude-modulated signals such as OOK.

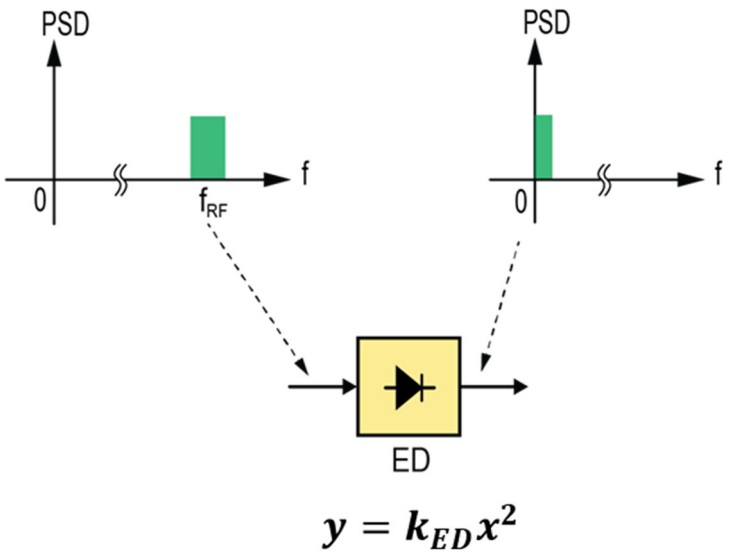


Figure 3.3: Down-conversion of an RF signal into DC via the squaring operation of an ED.

As mentioned above, the ED-based receiver typically suffers from having poor noise performance. Fig. 3.4 shows the mixing of the RF noise into DC which contains two types of noise: linear mixing of the RF noise with the RF signal and nonlinear mixing of the RF noise with itself [8]. The linear mixing is based on the assumption that the RF signal bandwidth is much smaller than the RF noise bandwidth, hence the RF desired signal appears as a CW tone to the noise; therefore, the noise will be linearly translated from the RF domain into the baseband (BB) domain. The nonlinear mixing of noise with itself produces a triangular shape whose width is the same as the RF noise bandwidth. In addition to these two types of noise that are down-converted from the RF domain, the ED also has its own flicker noise and thermal noise at the output, as shown in Fig. 3.5. The flicker noise can be particularly detrimental since the desired signal is now centered at DC. Additionally, the squaring operation of the ED significantly reduces the powers of the desired RF signal and the RF noise; therefore, they can easily be overwhelmed by the magnitude of the ED's output noise at the baseband (BB) spectrum.

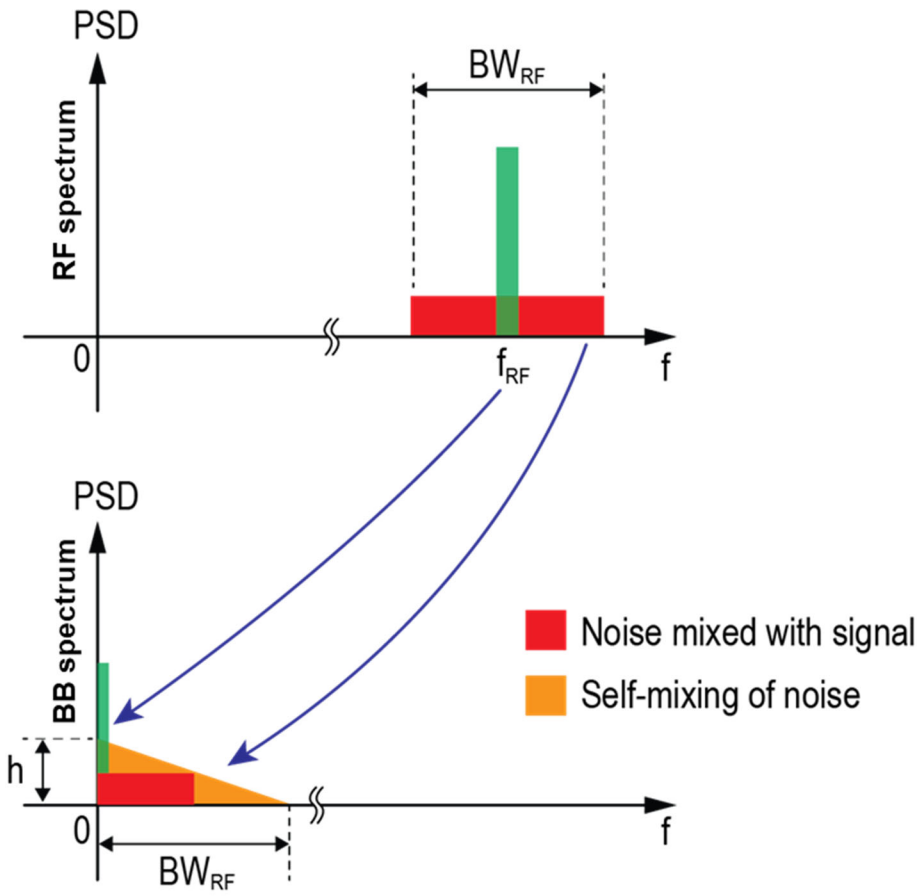


Figure 3.4: Down-conversion of RF noise onto DC leading to various types of noises.

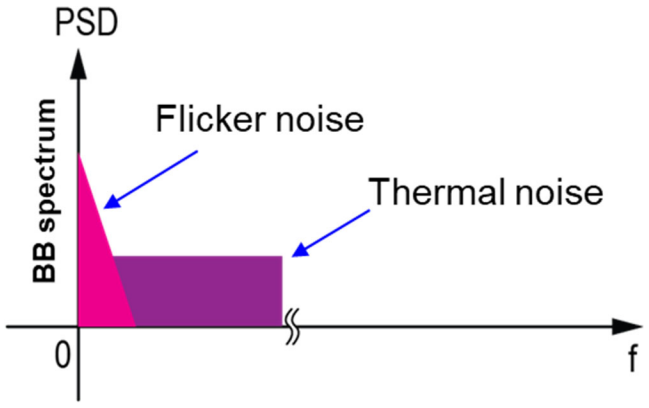


Figure 3.5: Flicker noise and thermal noise spectral density inherent to the ED at its output.

Apart from having poor noise performance, the ED also suffers from another potential interference issue. Fig. 3.6 shows how any interference that exists in the RF domain is down-

converted directly to DC due to the squaring operation, potentially corrupting the signal-to-noise-and-distortion ratio (SNDR).

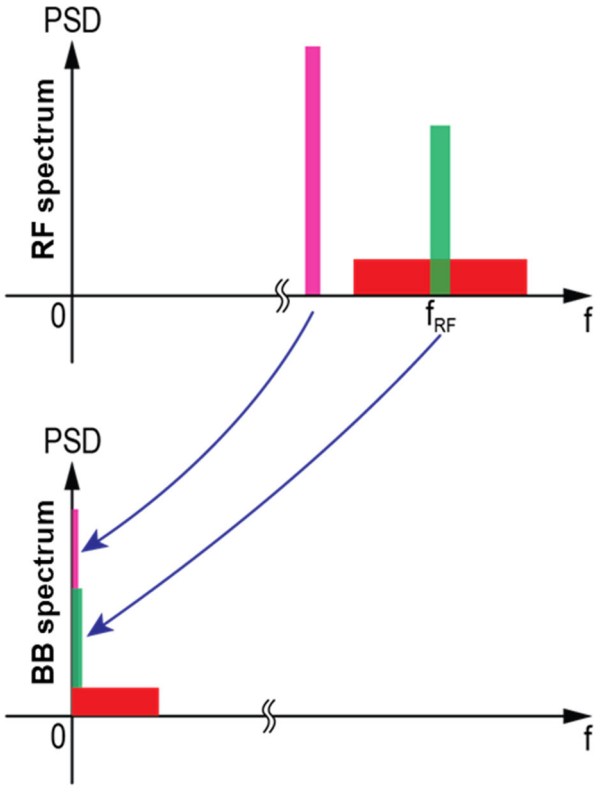


Figure 3.6: Down-conversion of an interference to DC, along with the down-conversion of the desired signal, potentially corrupting the desired signal.

The above discussion implies that it is desirable to have a high RF gain prior to the ED in order to minimize the effect of the ED's output noise. Additionally, a narrow RF bandwidth can also filter out interferences before passing the signal through the ED, effectively helping improve interference resiliency and alleviate the degradation of the SNDR.

In agreement with the above discussion, recent works in ultra-low-power OOK receivers (RXs) have also shown that adding gain in the RF front-end improves the sensitivity of ED-based receivers by an amount proportional in dB to the added RF gain [5, 8]. Fig. 3.7 shows a

numerical simulation of the sensitivity of a typical ED-based receiver as a function of the RF front-end gain for four different values of the noise figure, respectively. As can be seen, a conventional LNA with a perfect NF but a lower gain, e.g. 15 dB, will not be adequate for a direct-conversion receiver based on envelope detection; whereas a regenerative amplifier (RA) with a much higher gain, e.g. 50 dB, even with a much worse NF, e.g. 25 dB, can still beat the conventional LNA in terms of sensitivity performance.

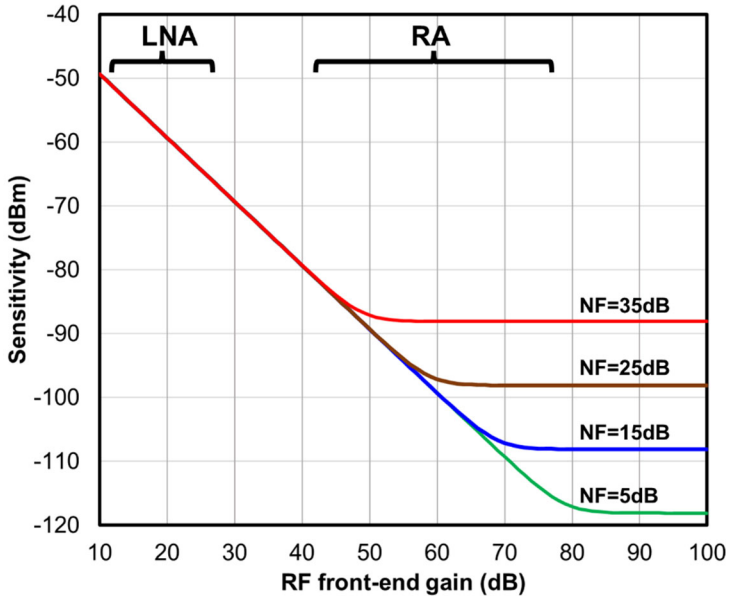


Figure 3.7: Sensitivity of a typical direct-conversion ED receiver as a function of the RF front-end gain for four different values of noise figure, respectively.

Adding passive gain in the RF front-end is also a feasible option to achieve high performance. However, due to finite passive Q-factors, further increasing passive gain at GHz frequencies is impractical, while adding active RF gain can require significant power. In addition, worsening Q-factors at GHz frequencies limits the ability to perform sharp filtering at RF to attenuate potential interferers, as previously mentioned [5].

To tackle these issues, a receiver architecture employing dual differential RAs is proposed to Q-boost inductors to offer sharp filtering and high gain. Here, the first RA is used to

boost the Q-factor of the input impedance matching and transformation network to provide additional "semi-passive" voltage gain and relatively sharp filtering, while the second cascode-driven RA provides a large amount of active gain and very sharp filtering prior to envelope detection. The ED is passive and is implemented using an all-NMOS truly differential architecture based on dynamic-threshold MOSFET (DTMOS) transistors to increase the conversion gain further to help nullify the noise contribution of itself and the baseband circuitry.

II – Circuit Implementation Details

A. Input Impedance Transformation Network and Dual Differential Regenerative Amplifiers

Fig. 3.8 shows the overall block diagram of the receiver, along with the operation of the input impedance matching and transformation network and that of the dual differential RAs. A low-loss, commercial balun converts the 50-Ω single-ended source resistance into differential. A differential tapped-capacitor circuit then transforms the 50-Ω source impedance into 66 kΩ at 2.4 GHz, providing a corresponding voltage gain of approximately 31 dB.

To maintain this large (and power-free!) voltage gain as well as realize antenna impedance matching, the 66-kΩ output resistance of the tapped-capacitor transformer must see an equal resistance coming from the equivalent parallel resistance of the resonant inductor, which is employed to keep the overall impedance of the network real. Since this effective parallel resistance is limited by the finite Q of the inductor (estimated to be 70 which is equivalent to a parallel resistance of 10.6 kΩ for a 10-nH inductor) and not likely to reach 66 kΩ at 2.4 GHz, even with a large off-chip implementation, the complementary differential cross-coupled pair in the first RA provides a negative resistance that cancels out part of the conductance of the inductor, thereby boosting its Q-factor to around 440 and presenting an

overall resistance equal to about 66 kΩ. As a result, the 31-dB voltage gain of the input matching network is maintained and the bandwidth is narrowed down to around 11 MHz, all while impedance matching is accomplished. The first RA also dictates the noise performance of the receiver and provides a moderate degree of noise and interference suppression prior to the cascode-driven second RA.

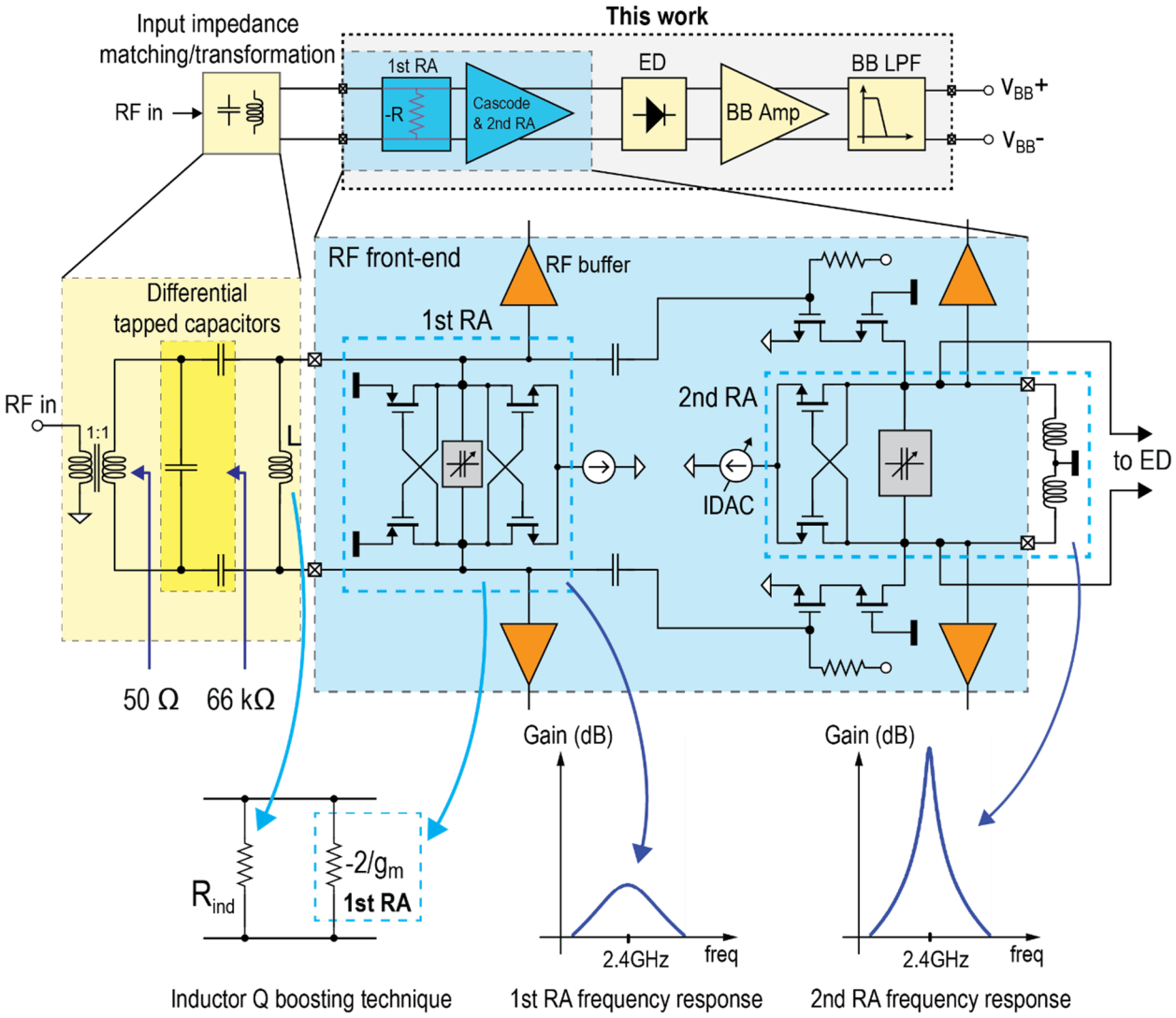


Figure 3.8: Block diagram of the proposed 2.4GHz OOK receiver and the operation of the dual differential RA's along with the input impedance transformation network.

The second RA is also based on a differential cross-coupled pair and is used to boost the Q-factor of the off-chip inductors on its output. The second RA can provide an additional gain such that the total overall gain of the dual differential RA's front-end can be upwards of 65 dB with an overall ultra-narrow 3-dB bandwidth of only around 240 kHz at a 2.4-GHz center frequency, i.e. the total inductor's Q is boosted from an estimate of 70 to 10000. The second RA therefore provides ultra-sharp filtering to suppress interference and especially noise even further, which has been proven to be desirable in a direct-conversion envelope-detection RX [8]. The IDAC bias current can be tuned to achieve a desired total high gain and narrow bandwidth.

Since tuning of one RA can potentially affect the other, a cascode stage is placed between the two RA's to provide additional transimpedance gain as well as sufficient isolation to enable independent tunings of input matching, noise performance, and desired total gain and bandwidth.

B. Differential Passive Envelope Detector

Fig. 3.9 (a) shows the schematic of the differential passive ED which consumes no power and is flicker-noise free [5]. The ED is based on the Dickson topology where an identical branch of diodes and capacitors is oriented in the opposite direction to achieve differential signaling, helping double the conversion gain. Different from the design in [5], however, this ED architecture truly benefits from the differential signaling scheme, i.e. it is not just pseudo-differential, by taking advantage of the already-available differential dual RA's output, effectively more than quadrupling the gain compared to a conventional all single-ended architecture. In addition, all transistors employed have the body connected to the gate, similar to a dynamic-threshold MOSFET's (DTMOS) configuration to increase the conversion gain even further. Normally, the main downside of using DTMOS transistors would be an increase on the input loading. However, for this passive structure, the parasitic diode between the body and

source still remains zero-biased, leading to essentially no difference on the input loading. The next paragraph will show that for the chosen ED design, the overall input loading is essentially negligible compared to the 2nd RA's output inductors.

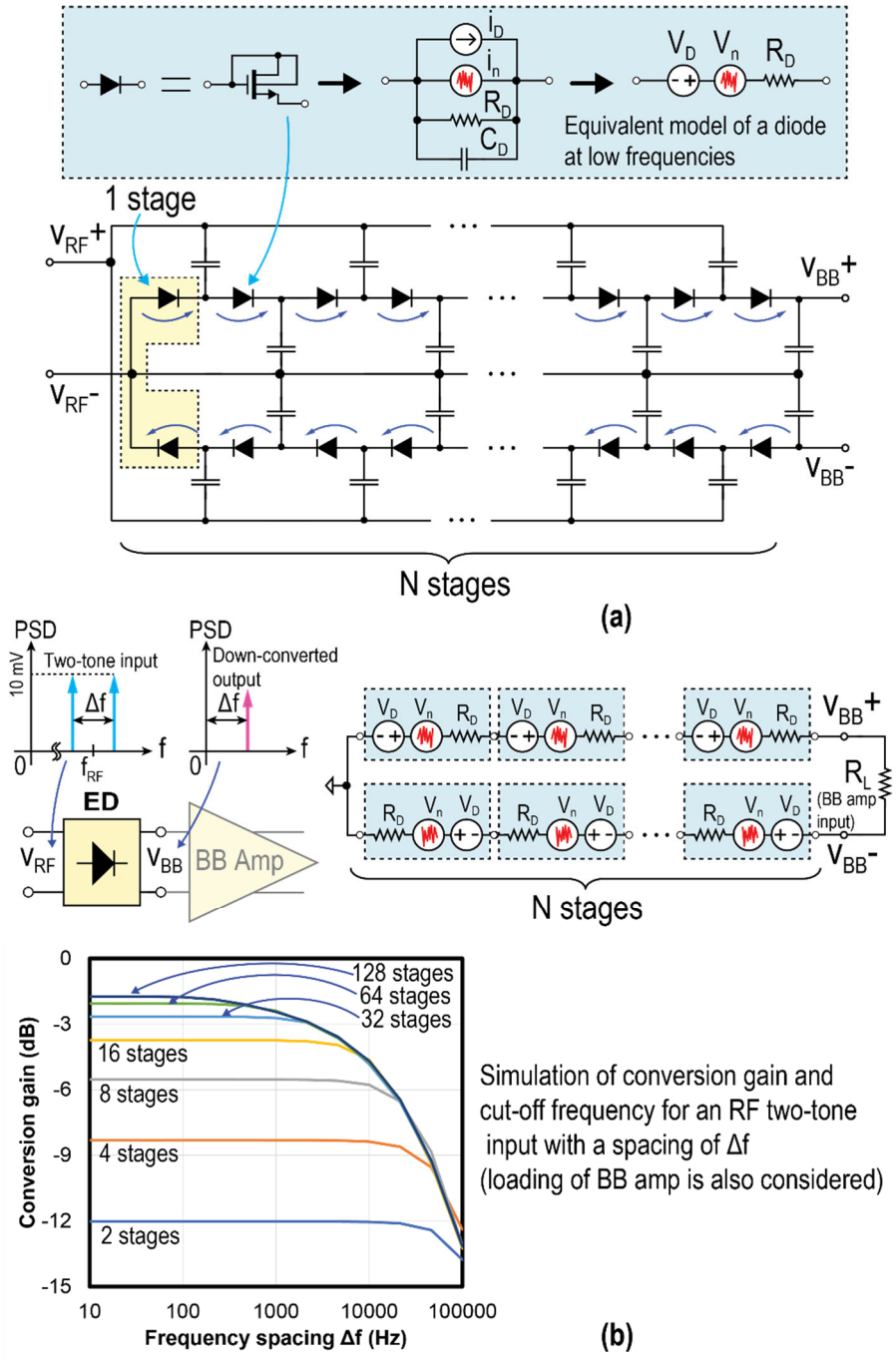


Figure 3.9: (a) Schematic of the differential passive envelope detector (ED); and (b) Simulation of the conversion gain with the frequency spacing of an RF two-tone input as a function of the number of ED stages.

Fig. 3.9 (b) shows the simulation of the conversion gain of the ED when the input is a two-tone signal each fixed at 10 mV, centered at around 2.4 GHz separated by a spacing of Δf, as a function of the number of stages in the ED. By looking at the ED's equivalent model at baseband [6] where the Norton model of each diode is converted into a Thevenin circuit, it can be seen that for every doubling of the number of ED stages, the conversion gain increases by approximately 6 dB. Therefore, it can be desirable to maximize the number of ED stages especially for ultra-low data rate RXs. The output noise also only increases at half the rate of the conversion gain [6] due to the un-correlation between the noises of the diodes. However, increasing the number of stages will inevitably lead to a lower cut-off frequency (see Fig. 3.9), increase the loading on the dual RA's output, complicate RF layout and potentially leading to more RF loss. Lastly, due to the limited input resistance of the baseband (BB) amplifier, the output BB voltage will eventually be saturated, as given by:

$$V_{BB} = \frac{2NV_D R_L}{2NR_D + R_L}, \tag{3.6}$$

which is capped at $\frac{V_D R_L}{R_D}$ as N approaches infinity. In this design, the ED has 32 stages for an adequate conversion gain and sufficient cut-off frequency for a target data rate of 5 kbps. In addition, the 32-stage ED has a simulated input resistance and capacitance of 230 kΩ and 27 fF, respectively; the resistance is negligible in comparison with the output inductors of the 2nd RA (assuming 11-nH total inductance with a Q of 70) while the capacitance can be absorbed into the 2nd RA's output. As a result, the loading on the 2nd RA is considered to be insignificant.

Fig. 3.10 shows the schematics of the BB amplifier and LPF, respectively. Each stage of the BB amplifier and LPF is implemented using a fully differential g_m cell with dedicated stabilized common-mode feedback (CMFB). PMOS transistors are used as the amplifying devices with large sizes, especially in the first g_m cell, to minimize flicker noise.

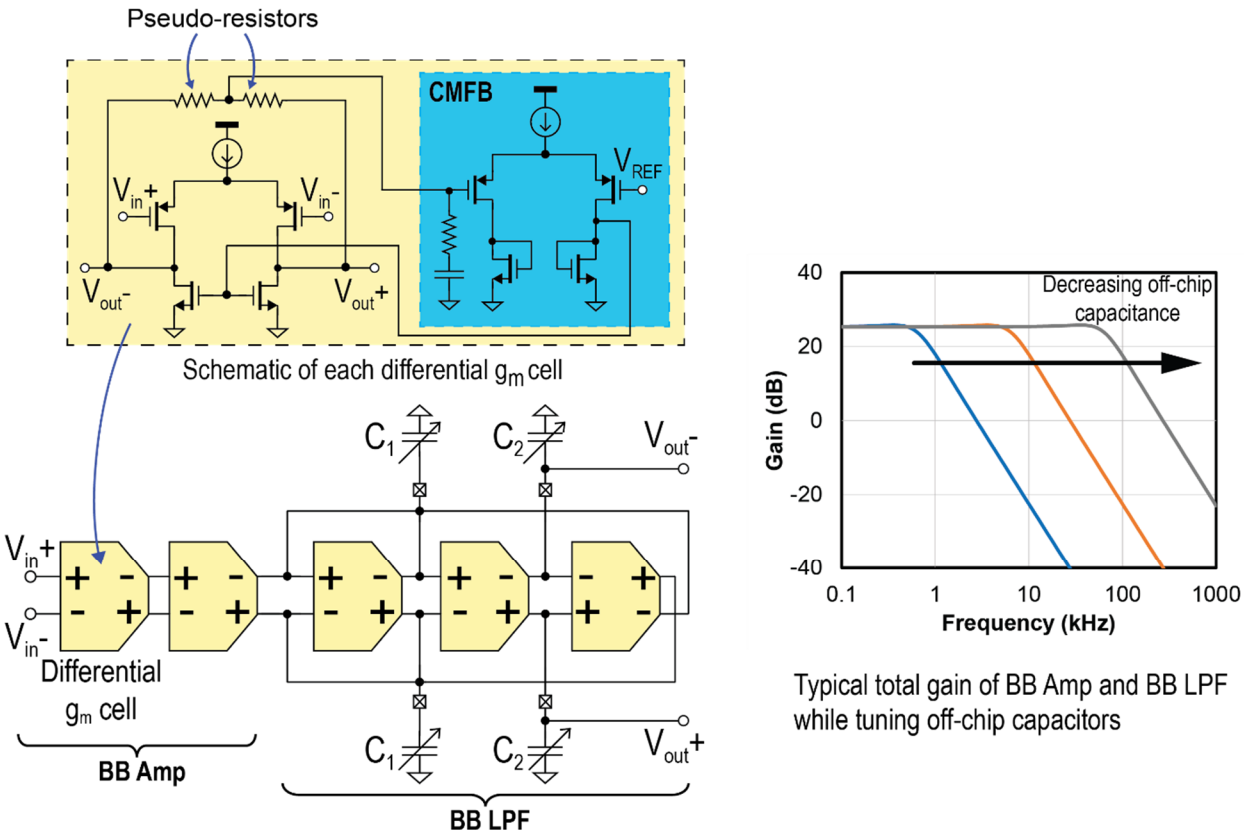


Figure 3.10: Schematic of the differential baseband amplifier and the differential baseband low-pass filter.

The BB amplifier consists of two g_m cells while the second-order LPF is based on a g_m-C topology, which employs off-chip capacitors with a cut-off frequency that can be tuned to as low as only a few hundred Hz to provide additional filtering for the baseband signal. Together, the BB amplifier and the LPF can achieve a tunable gain anywhere from -30 dB to 26 dB. The cut-off frequency and the Q-factor of the frequency response can be given by, respectively:

$$\omega_0 = \sqrt{\frac{g_m^2}{C_1 C_2}} \tag{3.7}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{3.8}$$

III – Measurement Results and Conclusion

The receiver is implemented in a 65-nm CMOS process. Fig. 3.11 shows the die photo of the chip and the top and bottom sides of the PCB, respectively. Discrete inductors, namely the Coilcraft 0908SQ and 0402DC series, are used for the input impedance matching and transformation network as well as the output inductors of the second RA.

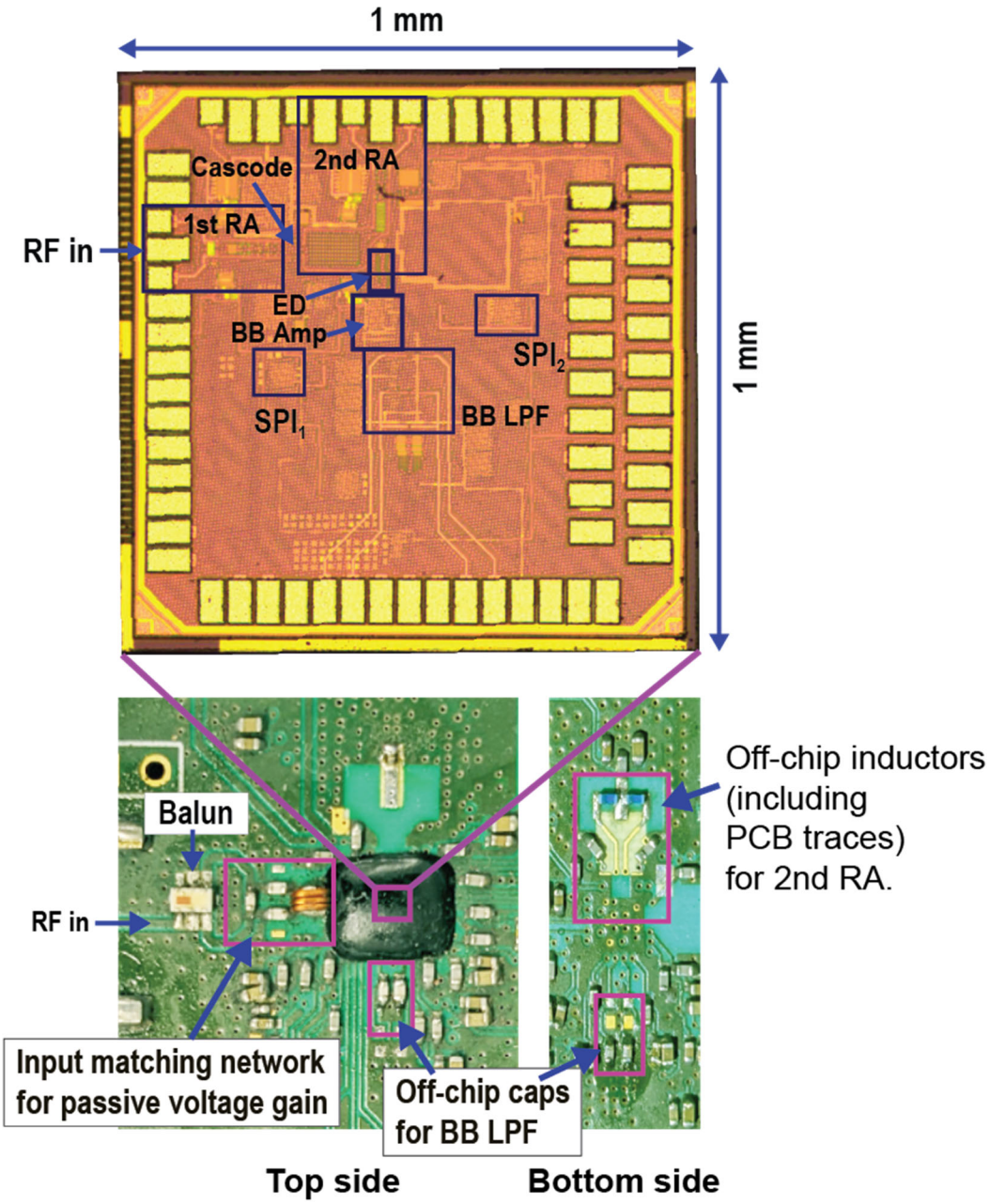


Figure 3.11: Die micrograph along with the top and bottom sides of the PCB.

Due to the extremely high gain of the dual RA's, coupling from the second RA back to the first RA might occur due to the bulky off-chip inductors. As a result, careful PCB layout precautions must be practiced to ensure that the coupling is negligible. To that end, the off-chip inductor and input network of the first RA is placed on the top of the PCB while those of the second RA are placed on the bottom.

Fig. 3.12 shows the measurement results of S11, and S21 of the first RA (a) and the output power spectral density (PSD) of the second RA (b), respectively. S11 is below -10dB for a frequency range of around 4 MHz, while S21, which is observed through the on-chip single-ended lossy RF buffer, shows a narrow bandwidth of around 11 MHz, demonstrating the Q-boosting technique of the first RA. The output spectrum of the second RA for a noise-only input, which is also observed through another identical RF buffer, shows an ultra-narrow bandwidth of only around 240 kHz, demonstrating the Q-boosting technique of the second RA.

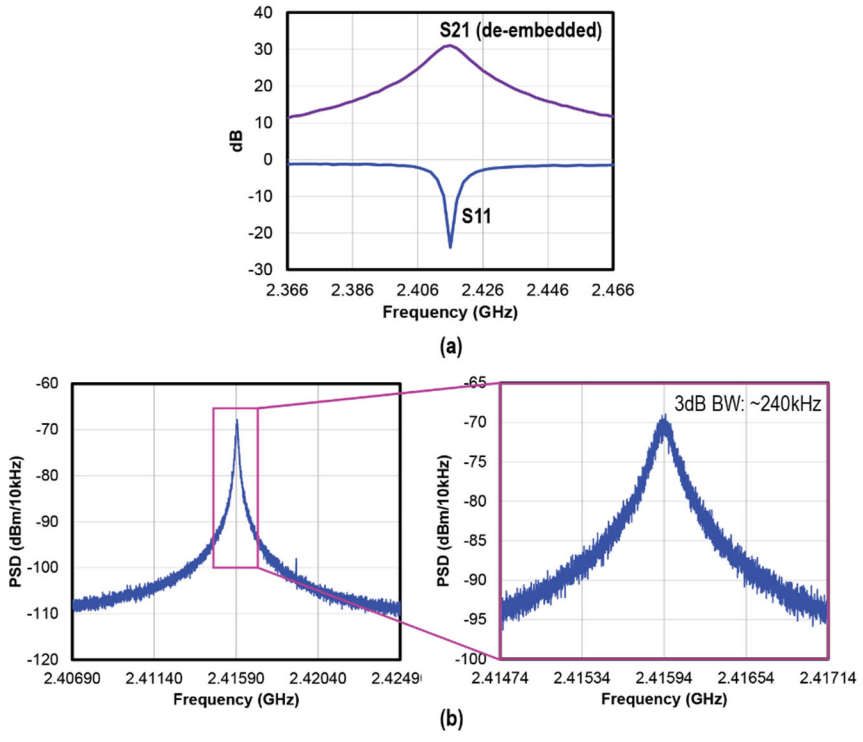


Figure 3.12: (a) Measured S11 and S21 (through the on-chip RF buffer) of the 1st RA; and (b) Measured output spectrum of the 2nd RA.

Fig. 3.13 shows the measured BER and SIR of the receiver, respectively. The BER measurement is done for a 5-kbps OOK signal and demonstrates a sensitivity of -101 dBm. For interference-resiliency measurement, a power combiner is used at the RF input to combine the 5-kbps OOK signal with a continuous-wave (CW) interference at a certain offset from the signal frequency. The measurement in Fig. 3.13 (b) shows an SIR of -28 dB at an offset of 3 MHz.

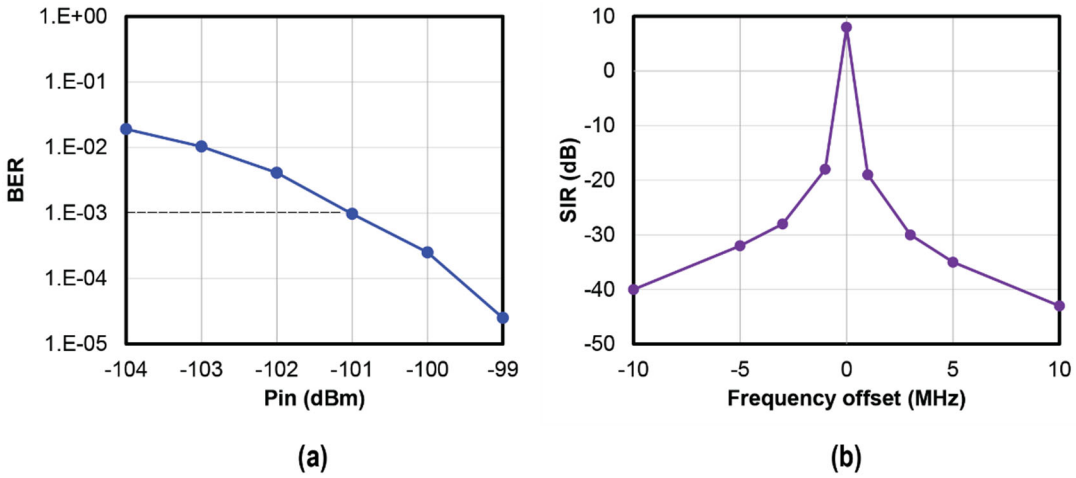


Figure 3.13: (a) Measured BER; and (b) Measured SIR.

To address the potential issue of frequency fluctuation due to the extremely narrow bandwidth, Fig. 3.14 shows a time-series measurement of the instantaneous center frequency of the 2nd RA, demonstrating stable operation within 10 kHz of the original calibrated frequency over approximately an hour in a normal lab room without temperature regulation, all with no discernable change in the 240-kHz bandwidth.

Fig. 3.15 shows the power breakdown of the receiver. The dual differential RA's consume more than the majority of the total power. With a VDD of 0.5 V, the total power consumption is only around 112 μW, demonstrating the ultra-low power, high-sensitivity receiver at GHz frequencies.

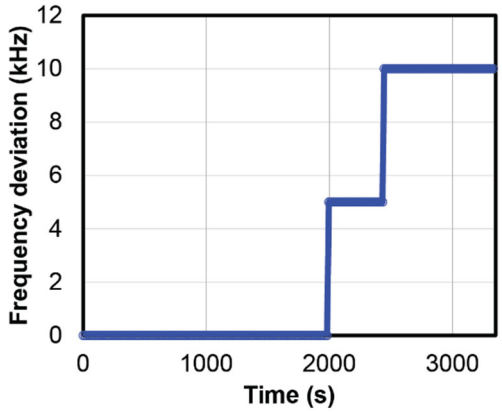


Figure 3.14: Measured instantaneous center frequency of the 2nd RA over approximately an hour.

Block	Pdc (μW)
1st RA	5.91
Cascode	27.15
2nd RA	77.34
ED	0
BB Amp & LPF	1.68
Total	**112.1**

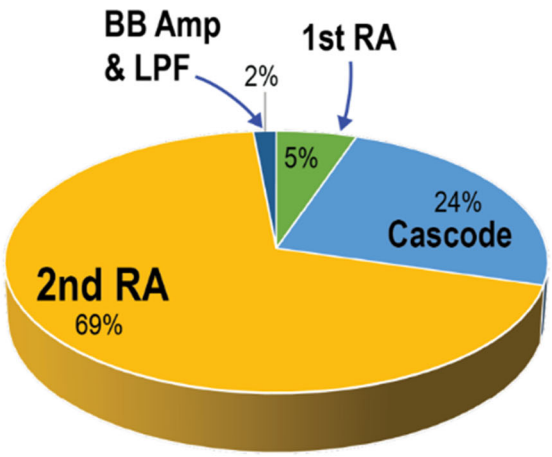


Figure 3.15: Breakdown of the total power consumption of the receiver.

Table 3.2 summarizes the performance of the receiver in comparison with state-of-the-art ultra-low power receivers at and beyond the operation frequency of 2.4 GHz. By employing dual-differential RAs along with a differential passive ED architecture, this receiver is able to achieve a GHz operation frequency with a sensitivity of -101 dBm for a 5-kbps OOK signal, and an SIR of -28 dB at a 3-MHz offset while consuming only 112 μW. It is worth noting that the receiver can be employed in areas where ultra-low power consumption and high sensitivity are

more important than high data throughput; a figure of merit (FOM) similar to the one presented in [9] for the receiver can therefore be defined as:

$$FOM_1 = P_{sen} + 10\log P_{DC} \tag{3.9}$$

If the data rate must be included, then another FOM can also be used:

$$FOM_2 = P_{sen} - 10\log(DataRate) + 10\log P_{DC} \tag{3.10}$$

Table 3.2: Performance comparison with other state-of-the-art ultra-low power receivers.

	[44] JSSC 2016	[45] RFIC 2017	[46] VLSI 2017	[47] CICC 2018	[48] ESSCIRC 2018	[49] MTT-S 2021	**This work**
Technology	65 nm	65 nm	65 nm	65 nm	40 nm	65 nm	**65 nm**
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	5.8 GHz	4.9 GHz	**2.4 GHz**
Vdd (V)	0.5	0.1/0.5/0.8	0.6	0.75	0.5/0.95	1.2-1.5	**0.5**
Modulation	OOK	OOK	BFSK	GFSK	OOK/FSK	OOK	**OOK**
Architecture	Dual uncertain IF	Antenna + Rectifier co-design	Sliding IF + Cascaded N-path Hybrid PPF	Mixer-first IF downconversion	Mixer-first direct downconversion	Envelope-detection, direct downconversion	**Dual differential regenerative amplifier & Differential passive envelope detector**
Date rate (kbps)	10	2.5	25/50	83	62.5	0.016	**5**
Sensitivity (dBm)	-97	-61.5	-102/-101	-80	-92.5/-90	-74.5	**-101**
Power consumption	99 µW	0.365 µW	466 µW	230 µW (always on Pdc)	470/490 µW	0.366 µW	**112 µW**
SIR (dB)	-22 dB @3 MHz	-22 dB @3 MHz	-44/-45 dB @3 MHz	N/A	-24 dB @20 MHz	-7.6 dB @3 MHz	**-28 dB @3 MHz**
FOM_1 (dB)	-137	-125.9	-134.3	-116.4	-125.6	-138.9	**-140.5**
FOM_2 (dB)	-177	-159.9	-181.3	-165.6	-173.6	-150.9	**-177.5**

In Table 3.2, both FOMs are presented which shows that the performance of the receiver compares favorably with the state of the art. Fig. 3.16 depicts a comprehensive comparison which takes into consideration both the FOMs and the SIR. It can be seen that the performance of the receiver is among the best of the previously published works at or beyond GHz of operation frequencies. In addition, thanks to its fairly simple but novel architecture, as opposed to the complex super-heterodyne design in [46], this work can be an excellent candidate for ultra-low power, low data-rate, short-range radio receivers in many different applications such as wireless sensor networks, implantable medical devices, smart IoT devices, etc.

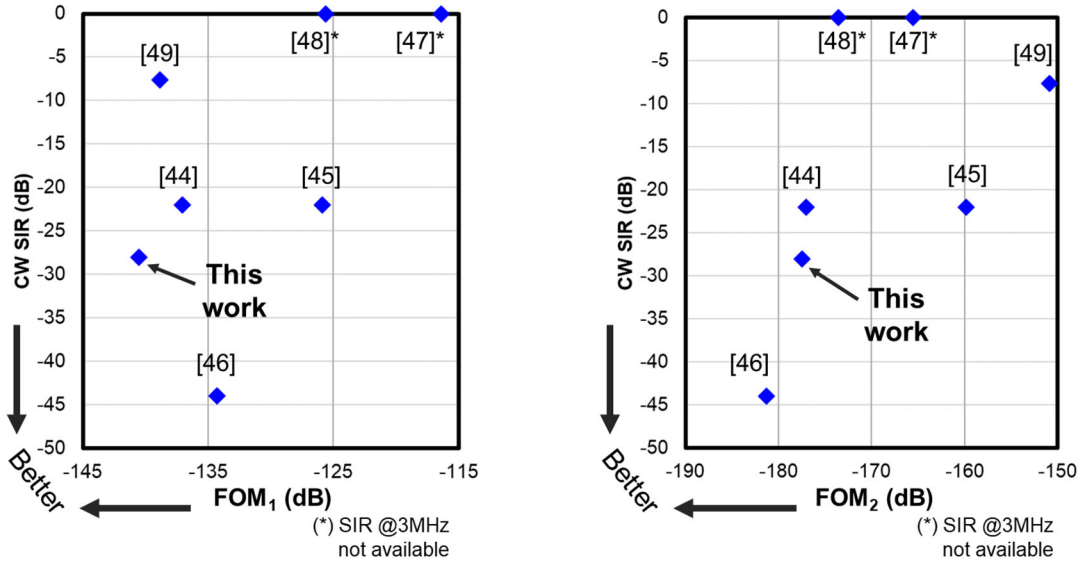


Figure 3.16: Comprehensive comparison including the SIR for both definitions of the figure of merit.

Acknowledgements

Chapter 3, in part, has recently been submitted to be considered for a future publication, and is coauthored with Hongyu Lu, Ahmed Gharib Gadelkarim, Nader Fathy, Prasad Gudem, and Patrick Mercier. The dissertation author was the primary researcher and author of this material.

CHAPTER 4

An Ultra-Low Power BLE/WiFi-Compatible Receiver Based on Dual Regenerative Amplifiers

I – Existing BLE/WiFi-Compatible Downlinks and Their Challenges

Smart wearable devices are becoming more and more ubiquitous in everyday life. Recently, there is a research trend to implement smart wearable devices that can communicate directly with a WiFi access point (AP) or a smartphone via either Bluetooth Low Energy (BLE) and/or WiFi standards. However, due to high power consumption and poor sensitivity, these devices normally do not have a long battery life and can occasionally go out of range. As shown in Fig. 4.1, these smart devices generally have one of the following two architectures [50 – 52]:

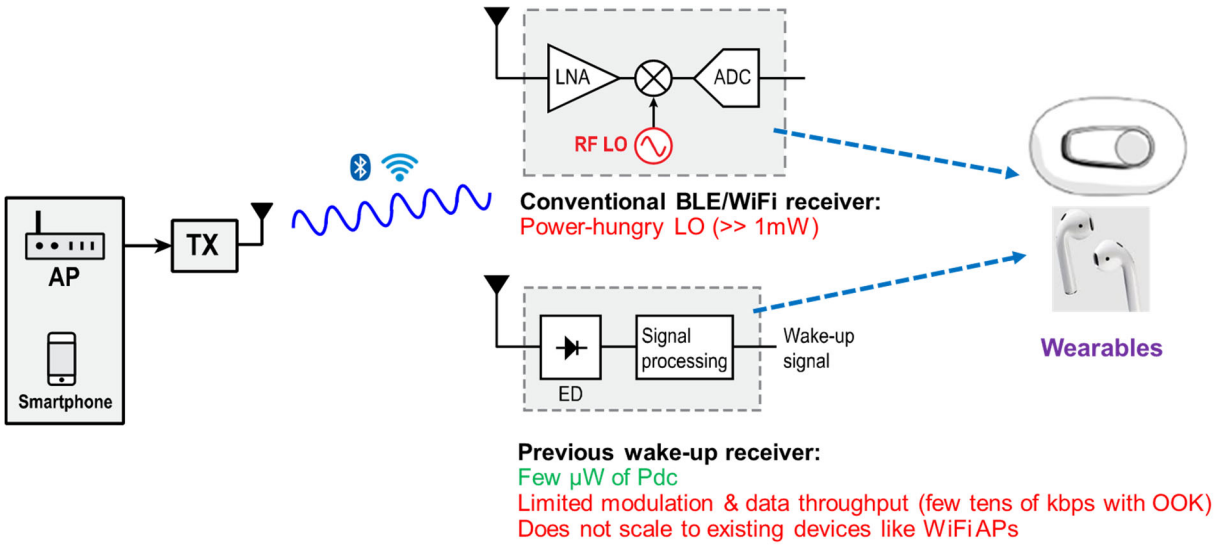


Figure 4.1: Existing downlink architectures that are compatible with BLE/WiFi suffer from two major challenges: high power consumption or limited modulation and data throughput.

(a) Using a conventional BLE and/or WiFi receiver. For these receivers, due to the need to generate a local oscillator (LO) internally in the device, the power consumption tends to be excessive and is easily much higher than 1 mW.

(b) Using a wake-up receiver. For these receivers, the main limitation is non-coherent, low-order modulations such as only OOK. In addition, the data throughput is generally very low, only a few tens of kpbs.

In this chapter, a novel architecture of a receiver used in a smart wearable device is proposed, based on a dual regenerative amplifier (DRA) technology that allows for an ultra-low power consumption and high performance. As shown in Fig. 4.2, an external LO or "pilot" tone is transmitted alongside the desired BLE/WiFi signal; the architecture will reduce energy per bit, i.e. increase energy efficiency, significantly while still being able to obtain high data throughput via high-order modulations, e.g. 16QAM in OFDM. Most importantly, the receiving device is able to connect directly to an AP or a smartphone thanks to its compatibility with existing standards such as BLE and/or WiFi.

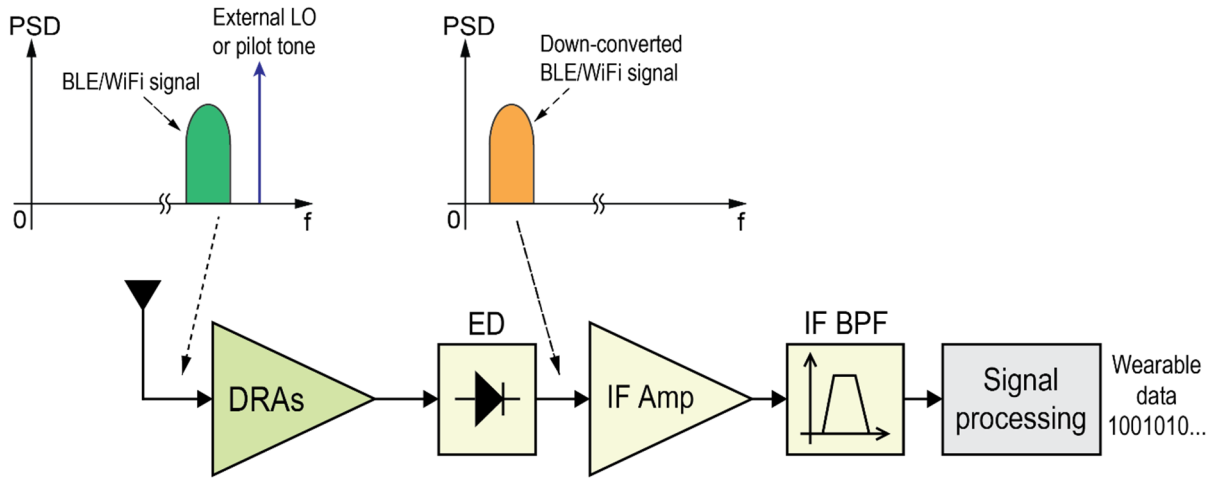


Figure 4.2: Overall proposed architecture of the ultra-low power, BLE/WiFi-compatible receiver for wearable devices.

II – Overall Architecture and Challenges of the Receiver Implementation

In [52], the authors have implemented a reverse-engineered WiFi IEEE 802.11ax standard that allows the transmission of only three subcarriers along with two pilot tones within a resource unit (RU). Fig. 4.3 depicts the spectrum of such a signal. The three subcarriers that contain data are -13, -12, and -11 respectively. The pilot tones are simply continuous-wave (CW) tones and are named -7 and +7. The pilot tone -7 will act as a local oscillator for the down-conversion of the three subcarriers. After this signal passes through an envelope detector (ED) with a squaring operation, the mixing of pilot tone -7 with the three subcarriers will result in a new desired three subcarriers at the intermediate-frequency (IF) spectrum. Since the mixing of the CW pilot tone -7 and the three subcarriers is linear, the demodulation can be done coherently for any type of signal modulation. The modulation of the three subcarriers can then be QPSK, 16QAM, 64QAM, etc. The individual subcarriers are combined in the orthogonal frequency division multiplexing (OFDM) manner, allowing the demodulation of the received signal in the digital domain using the inverse FFT computation.

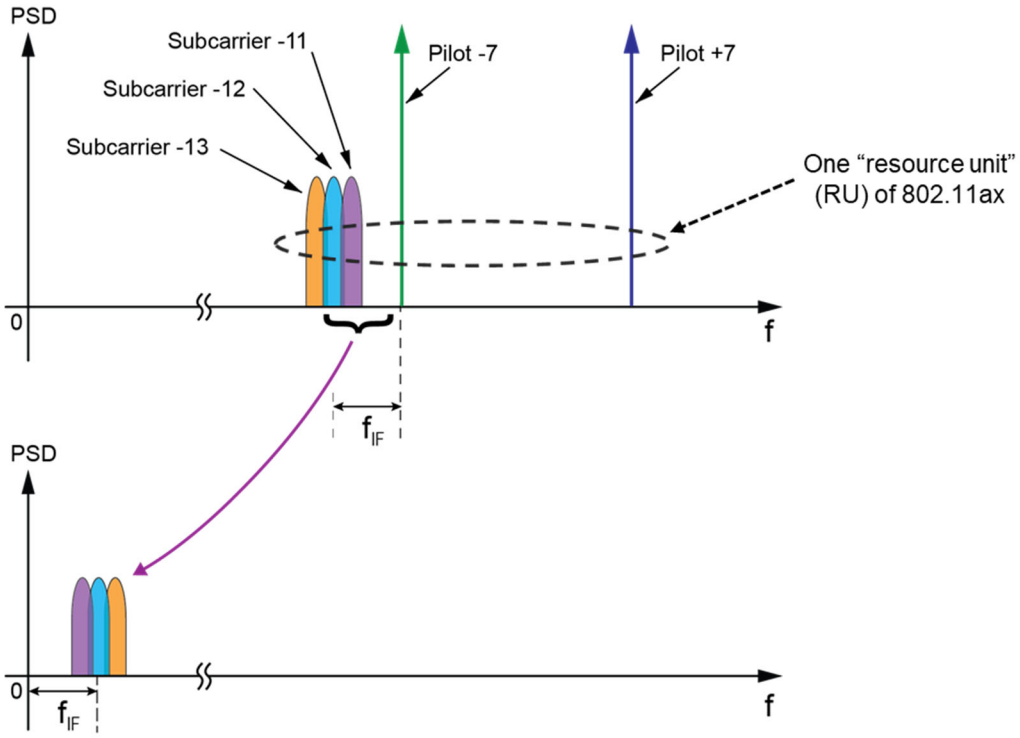


Figure 4.3: The reverse-engineered transmitted IEEE 802.11ax WiFi standard to generate two pilot tones along with three data-carrying subcarriers and the down-conversion of the signal accordingly.

The question that arises is then why there is a necessity to use a regenerative amplifier (RA) rather than a conventional LNA. The answer lies again in the fact that this receiver is an ED-based receiver with the ED being notorious for poor noise performance, as shown in the previous chapter. Fig. 4.4 shows how the RF noise gets mixed down to the IF spectrum and potentially worsens the receiver performance. The RF noise is mixed with either of the pilot tones located on the two sides. The center frequency of each portion of the noise in the frequency domain is separated from the pilot tones by the same distance between the three subcarriers and pilot tone -7. As a result, all these portions of the noise are down-converted and land exactly on top of the desired three subcarriers in the IF spectrum. This problem is similar to the age-old problem of image frequency in a super-heterodyne receiver.

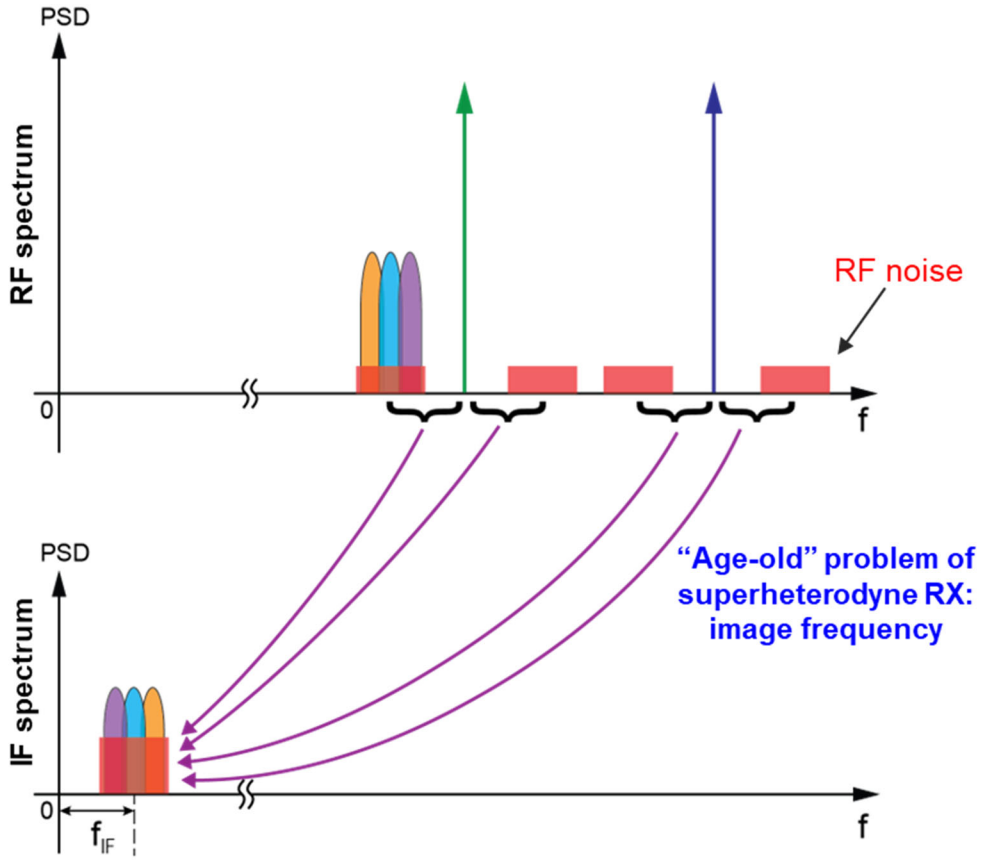


Figure 4.4: Linear mixing of the noise with either of the pilot tones.

In case the three subcarriers have significant power compared to the two pilot tones, the mixing of the three subcarriers with the noise in the region around pilot tone -7 can also be significant enough to affect the resultant SNR in the IF domain. Additionally, if the bandwidth of the RF front-end, in this case the dual RAs, is not sharp enough to capture only the desired RU and filter out any other signal outside of the RU bandwidth, then another image noise on the left side of the three subcarriers will also be down-converted to the same IF frequency, further degrading the SNR. These two additional noises are depicted in Fig. 4.5, along with the other noises mentioned in Fig. 4.4.

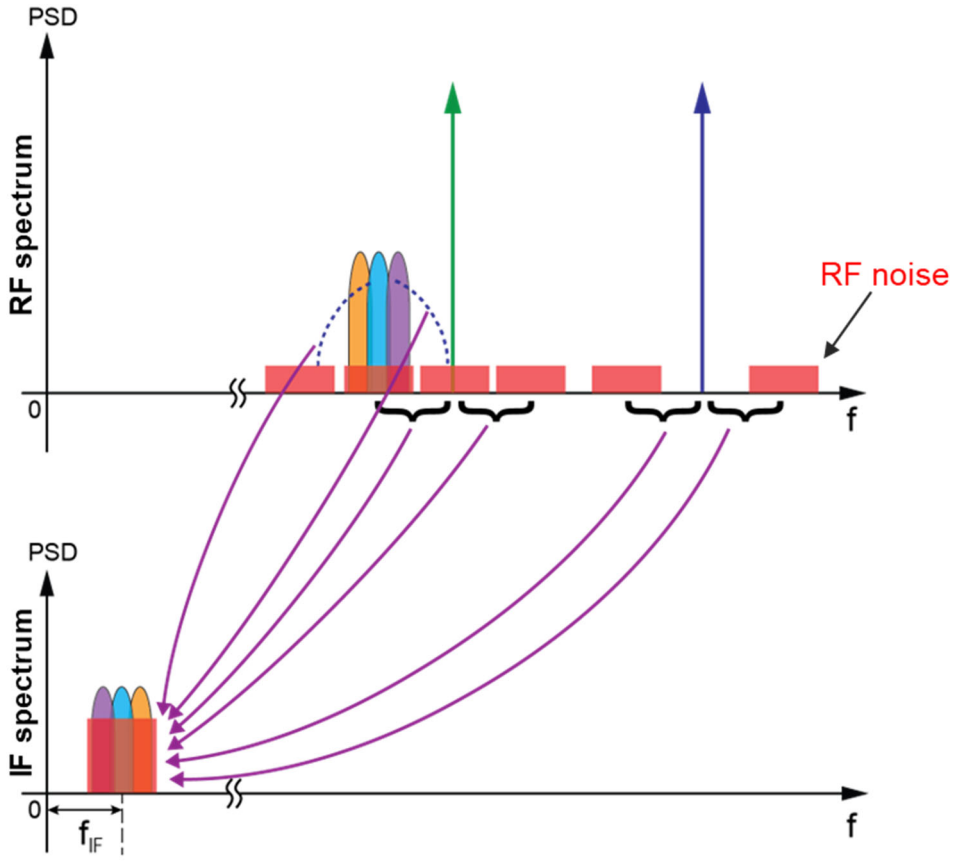


Figure 4.5: Additional image noise portions due to the mixing of the three subcarriers and the noise.

Fig. 4.6 shows the nonlinear self-mixing of the RF noise that produces a triangular shape of the resultant noise in the IF spectrum, as mentioned in the previous chapter. Fig. 4.7 shows the inherent flicker noise and thermal noise at the output of the ED. Since the IF spectrum is away from DC, the effect of the flicker noise is minimal. In addition, if the RF front-end bandwidth is narrow enough, the self-mixing of noise is also negligible [8].

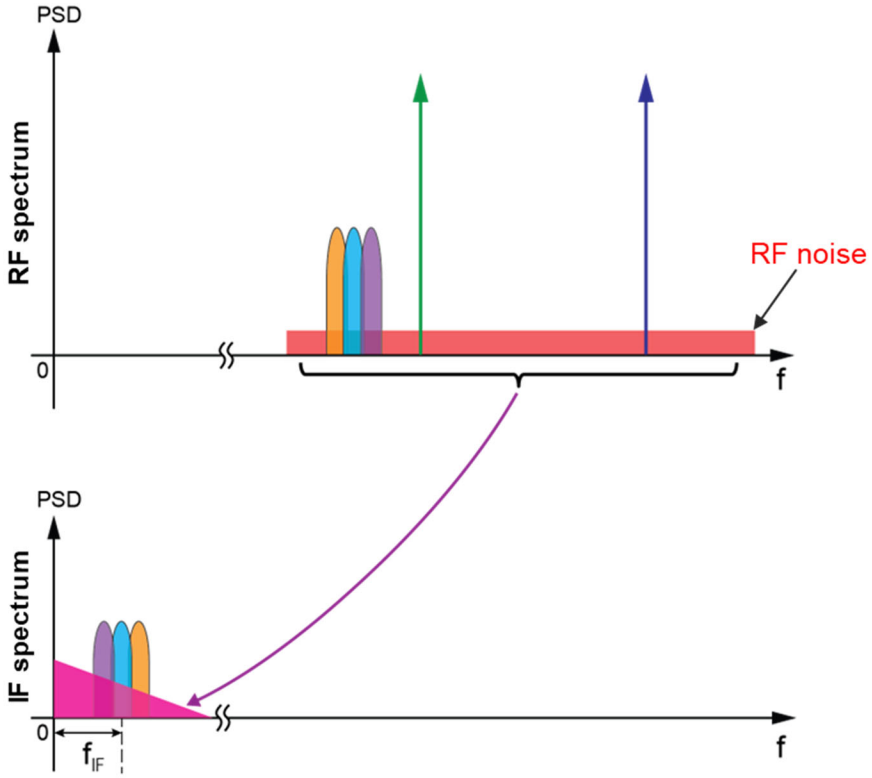


Figure 4.6: Nonlinear mixing of noise with itself, producing a triangular shape at the IF spectrum (not to scale).

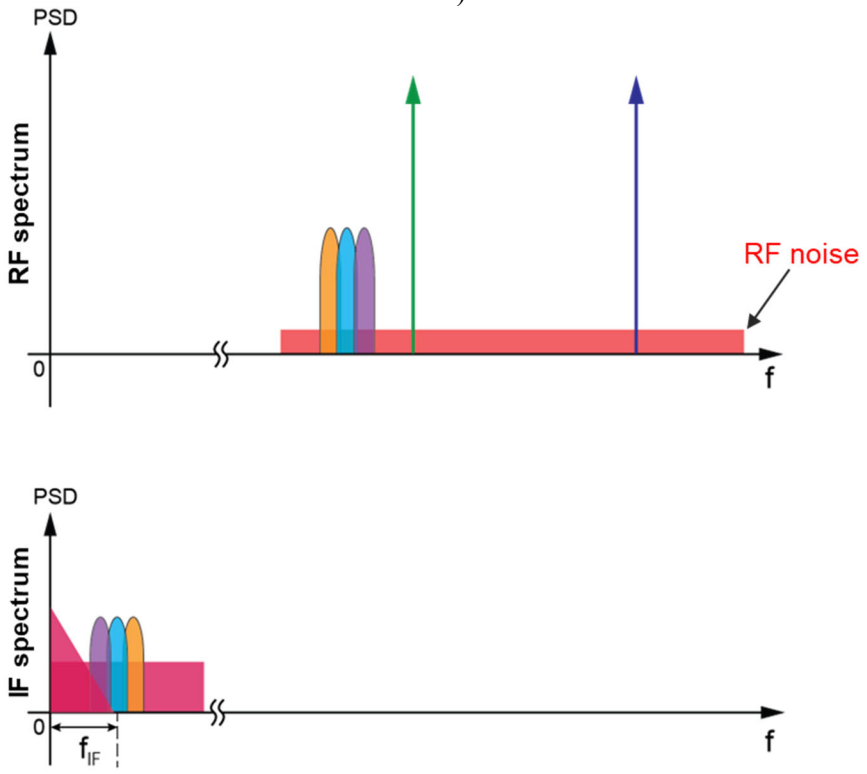


Figure 4.7: Flicker noise and thermal noise at the output of the ED.

The bottom line here is that due to the squaring operation of the ED which is desired for ultra-low power down-conversion, the unwanted side effect is that a number of new types of noise is generated, and both the RF signal and RF noise powers are reduced significantly when mixing down onto the IF spectrum and can easily be overwhelmed by the IF noise inherent at the ED output. As a result, it is critical to ensure a high RF front-end gain in order to help alleviate the effect of the IF noise that shows up at the ED output.

Following the above discussion, as opposed to a conventional LNA, not only does the DRAs have a relatively low noise figure and low power consumption, the DRAs can also help enormously in the following ways:

- It has a much higher gain, which helps boost the power level of the three subcarriers and the pilot tone -7, thereby leading to a much higher down-converted IF signal and helping fight against the ED's output noise.
- It has a much narrower bandwidth, which helps reduce the aforementioned unwanted noise that can be mixed down to the desired IF spectrum due to the squaring operation of the ED.

The following section will analyze the sensitivity performance as a function of the RF front-end gain.

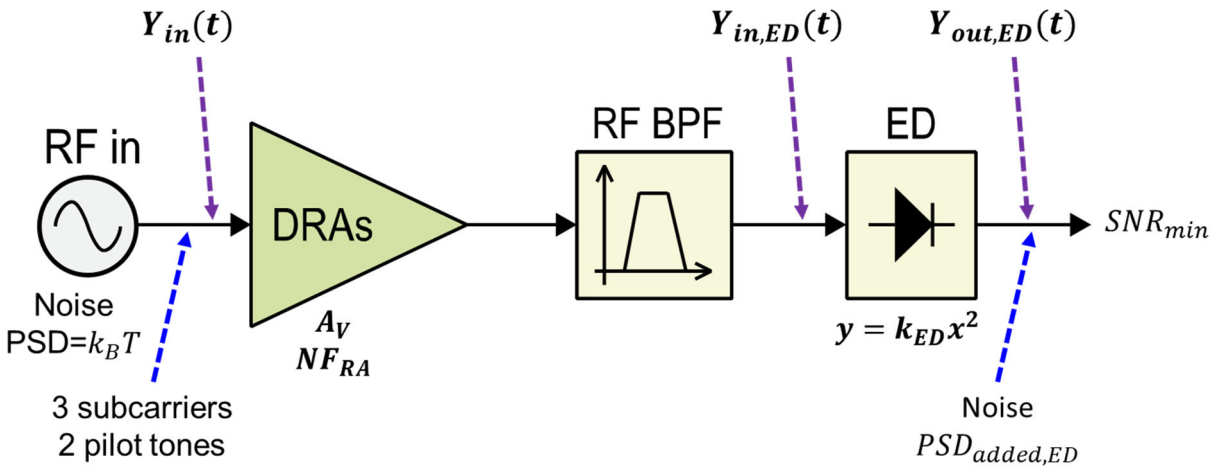


Figure 4.8: A simple model to analyze the sensitivity performance of the receiver.

III – Analysis of the Sensitivity Performance of the Receiver and Numerical Simulation

Fig. 4.8 depicts a simple model of the receiver used to analyze the sensitivity performance, consisting of the dual regenerative amplifiers DRAs, the RF bandpass filter (BPF) to represent the DRAs' narrow bandwidth, followed by the ED. Assuming the input to the receiver consists of three subcarriers and two pilot tones along with additive white Gaussian noise (AWGN), given by:

$$Y_{in}(t) = S_{in}(t) + N_{in}(t), \tag{4.1}$$

where $S_{in}(t)$ is the reverse-engineered 802.11ax signal:

$$\begin{aligned} S_{in}(t) = {} & S_{-13}(t)\cos\left(\omega_{-13}t + \phi_{-13}(t)\right) + S_{-12}(t)\cos\left(\omega_{-12}t + \phi_{-12}(t)\right) \\ & + S_{-11}(t)\cos\left(\omega_{-11}t + \phi_{-11}(t)\right) + S_0\cos(\omega_{-7}t) + S_0\cos(\omega_{+7}t), \end{aligned} \tag{4.2}$$

where $S_{-13}(t)\cos\left(\omega_{-13}t + \phi_{-13}(t)\right)$, $S_{-12}(t)\cos\left(\omega_{-12}t + \phi_{-12}(t)\right)$, and $S_{-11}(t)\cos\left(\omega_{-11}t + \phi_{-11}(t)\right)$ represent the subcarriers -13, -12, and -11, respectively; and $S_0\cos(\omega_{-7}t)$ and $S_0\cos(\omega_{+7}t)$ represent the pilot tones -7 and +7, respectively;

and $N_{in}(t)$ is the AWGN noise.

Assuming the DRAs gain is A_V, the signal at the input of the ED is given by:

$$\begin{aligned} S_{in,ED}(t) &= A_V S_{in}(t) \\ &= A_V S_{-13}(t)\cos\left(\omega_{-13}t + \phi_{-13}(t)\right) \\ &+ A_V S_{-12}(t)\cos\left(\omega_{-12}t + \phi_{-12}(t)\right) \\ &+ A_V S_{-11}(t)\cos\left(\omega_{-11}t + \phi_{-11}(t)\right) + A_V S_0 \cos(\omega_{-7}t) \\ &+ A_V S_0 \cos(\omega_{+7}t) \end{aligned} \tag{4.3}$$

The noise power at the input of the ED is given by:

$$\sigma_{in,ED}^2 = k_B \times T \times BW_{RA} \times A_V^2 \times NF_{RA}, \tag{4.4}$$

where:

- k_B is the Boltzmann constant,
- BW_{RA} is the bandwidth of the DRAs,
- NF_{RA} is the noise figure of the DRAs in the linear scale.

The output of the ED is:

$$Y_{out,ED}(t) = k_{ED}\left[S_{in,ED}(t) + N_{in,ED}(t)\right]^2 + N_{added,ED}(t) \tag{4.5}$$

where: $N_{added,ED}(t)$ is the inherent output noise of the ED itself combined with the input-referred noise of the subsequent IF stages, including the flicker noise and thermal noise. Since the IF frequency is located far away from DC, the flicker noise can be neglected, leading to an approximation of the power of the added inherent thermal noise at the output of the ED as:

$$\sigma_{added,ED}^2 \approx PSD_{added,ED} \times BW_{IF} \tag{4.6}$$

where:

- $PSD_{added,ED}$ is the combination of the ED's thermal noise density and the input-referred noise density of the subsequent IF stages;
- BW_{IF} is the bandwidth of the total desired signal, consisting of the three subcarriers. This bandwidth is simply equal to three times the symbol rate of each subcarrier.

The output of the ED can then be extended further into:

$$Y_{out,ED}(t) = k_{ED}S_{in,ED}^2(t) + k_{ED}N_{in,ED}^2(t) + 2k_{ED}S_{in,ED}(t)N_{in,ED}(t) + N_{added,ED}(t) \quad (4.7)$$

Since the input noise power of the ED is negligible compared to the input signal power, based on the assumption that the DRAs bandwidth is small compared to the center frequency, the self-mixing of noise component $k_{ED}N_{in,ED}^2(t)$ can be neglected, leading to an approximation of the output of the ED as:

$$Y_{out,ED}(t) = k_{ED}S_{in,ED}^2(t) + 2k_{ED}S_{in,ED}(t)N_{in,ED}(t) + N_{added,ED}(t) \quad (4.8)$$

Rewriting $Y_{out,ED}(t)$ as a function of A_V, $S_{in}(t)$, and $N_{in}(t)$ of the receiver gives:

$$Y_{out,ED}(t) = k_{ED}A_V^2S_{in}^2(t) + 2k_{ED}A_V^2\sqrt{NF_{RA}}S_{in}(t)N_{in}(t) + N_{added,ED}(t) \quad (4.9)$$

It can be seen that $Y_{out,ED}(t)$ consists of three components:

- The desired signal: $k_{ED}A_V^2S_{in}^2(t)$;
- The noise resulting from the mixing of the RF noise with the RF signal: $2k_{ED}A_V^2\sqrt{NF_{RA}}S_{in}(t)N_{in}(t)$;
- The added noise of the ED: $N_{added,ED}(t)$.

Rewriting $Y_{out,ED}(t)$ one more time leads to:

$$Y_{out,ED}(t) = k_{ED}A_V^2\left\{S_{in}^2(t) + 2\sqrt{NF_{RA}}S_{in}(t)N_{in}(t) + \frac{N_{added,ED}(t)}{k_{ED}A_V^2}\right\} \quad (4.10)$$

By looking at (4.10), it is clear that as k_{ED} and A_V approach infinity, the contribution of the ED's output noise becomes negligible, after which point, the system performance is only limited by the RF front-end noise. The rate at which the ED's output noise becomes more and more negligible as a function of A_V is twice as fast as that as a function of k_{ED}. Hence, it is more important to ensure a high gain in the RF front end.

The overall SNR at the output of the ED can then be given by:

$$SNR_{out,ED}$$

$$= \frac{\{power\ of\ [S_{in}^2(t)]^2\}}{4 \times NF_{RA} \times \{power\ of\ [S_{in}(t)N_{in}(t)]^2\} + \frac{1}{k_{ED}^2 A_V^4}\left\{power\ of\ \left[N_{added,ED}(t)\right]^2\right\}} \tag{4.11}$$

At this point, it is necessary to examine (4.11) more rigorously due to the fact that the signal component resulting from the squaring operation of the ED $S_{in}^2(t)$ does contain the desired three subcarriers centered at the IF frequency, but it also contains other unwanted components as well, e.g. the components that land on approximately twice the RF center frequency. The same thing can also be said about the squaring of the noise, since ultimately there will be an IF bandpass filter (BPF) at the subsequent stages to only process the frequency range between the IF bandwidth of the three subcarriers. As a result, the following will discuss how the true SNR at the output of the ED can be extracted from (4.11).

The desired components of $S_{in}^2(t)$ are the three subcarriers that result from mixing of the three subcarriers at RF with only the pilot tone -7:

$$\begin{aligned} S_{desired}(t) = \big[&S_{-13}(t)\cos\big(\omega_{-13}t + \phi_{-13}(t)\big) + S_{-12}(t)\cos\big(\omega_{-12}t + \phi_{-12}(t)\big) \\ &+ S_{-11}(t)\cos\big(\omega_{-11}t + \phi_{-11}(t)\big) + S_0\cos(\omega_{-7}t)\big]^2 \end{aligned} \tag{4.12}$$

Ignoring the components of $S_{desired}(t)$ at twice the RF center frequency leads to:

$$\begin{aligned} S_{desired}(t) = {} & S_0 S_{-13}(t)\cos\big((\omega_{-13} - \omega_{-7})t + \phi_{-13}(t)\big) \\ & + S_0 S_{-12}(t)\cos\big((\omega_{-12} - \omega_{-7})t + \phi_{-12}(t)\big) \\ & + S_0 S_{-13}(t)\cos\big((\omega_{-11} - \omega_{-7})t + \phi_{-11}(t)\big) \end{aligned} \tag{4.13}$$

Assuming the total input signal power of the receiver, including the three subcarriers and the two pilot tones, is P_{in}, then since each of the three subcarriers and pilot tones has the same power, the amplitude of pilot tones -7 and +7 can be given by:

$$\frac{\left(\frac{S_0}{\sqrt{2}}\right)^2}{50} = \frac{1}{5} \times P_{in} => S_0 = \sqrt{20P_{in}} \tag{4.14}$$

By looking at (4.13), it can be seen that when each of the three subcarriers mixes with a pilot tone, their instantaneous amplitude is multiplied by $S_0 = \sqrt{20P_{in}}$; in other words, their power is multiplied by $20P_{in}$ (unitless). The total desired signal power of $S_{desired}(t)$ in (4.13) is then given by:

$$P_{desired} = 3 \times 20P_{in} \times \frac{1}{5} P_{in} = 12P_{in}^2 \ (unit\ of\ power) \tag{4.15}$$

In order to extract the noise power of interest out of the component $S_{in}(t)N_{in}(t)$ in (4.11) within the desired IF bandwidth, it is assumed that the mixing of the noise with either pilot tone is more significant than that with each subcarrier, due to each subcarrier having a certain bandwidth (78.125 kHz) as opposed to being a CW. Hence, only the mixing of noise with either pilot tone, as shown in Fig. 4.4, is considered. In addition, assuming that the DRAs bandwidth is sharp enough to help partially filter out the other unwanted pilot tone +7 and its associated image noise portions, reducing each of their powers by 3 dB (i.e. reducing their amplitudes by $\frac{1}{\sqrt{2}}$) then the total power of the IF noise landing at the same location as the desired three IF subcarriers can be approximated as $2 + 2\frac{1}{\sqrt{2}} \times \frac{1}{\sqrt{2}} = 3$ times the power of the mixing of one image portion of the noise (whose bandwidth equal to that of the total three subcarriers BW_{IF}) and pilot tone -7, due to their un-correlation. As mentioned previously, when mixing with pilot tone -7, the power of one portion of the noise is multiplied by $20P_{in}$, hence the total noise power of interest in $S_{in}(t)N_{in}(t)$, resulting from the RF signal mixing with the RF noise, can be simplified into:

$$P_{noise,RF@ED} = 3 \times 20P_{in} \times k_B \times T \times BW_{IF} \tag{4.16}$$

Plugging both the desired signal power and the noise power of interest back into (4.11) results in:

$$SNR_{out,ED} = \frac{P_{desired}}{4 \times NF_{RA} \times P_{noise,RF@ED} + \frac{1}{k_{ED}^2 A_V^4} power\ of\ \left[N_{added,ED}(t)\right]^2} \tag{4.17}$$

$$SNR_{out,ED} = \frac{12P_{in}^2}{4 \times NF_{RA} \times 3 \times 20P_{in} \times k_B \times T \times BW_{IF} + \frac{1}{k_{ED}^2 A_V^4} \times PSD_{added,ED} \times BW_{IF}} \tag{4.18}$$

When P_{in} reaches the sensitivity level of P_{sen}, $SNR_{out,ED}$ must be equal to the minimum required SNR for the corresponding modulation scheme, e.g. 16QAM:

$$SNR_{out,ED} = SNR_{min} \tag{4.19}$$

Hence:

$$\frac{12P_{sen}^2}{4 \times NF_{RA} \times 3 \times 20P_{sen} \times k_B \times T \times BW_{IF} + \frac{1}{k_{ED}^2 A_V^4} \times PSD_{added,ED} \times BW_{IF}} = SNR_{min} \tag{4.20}$$

Re-arranging (4.20) leads to:

$$P_{sen}^2 - (20 \times NF_{RA} \times k_B \times T \times BW_{IF} \times SNR_{min})P_{sen} - \left(\frac{1}{12k_{ED}^2 A_V^4} \times PSD_{added,ED} \times BW_{IF} \times SNR_{min}\right) = 0 \tag{4.21}$$

(4.21) is a quadratic equation with a solution given by:

$$P_{sen} = 10NF_{RA}k_B TBW_{IF}SNR_{min} + \sqrt{(10NF_{RA}k_B TBW_{IF}SNR_{min})^2 + \left(\frac{1}{12k_{ED}^2 A_V^4} PSD_{added,ED} BW_{IF} \times SNR_{min}\right)} \tag{4.22}$$

Table 4.1 shows the parameters of the receiver in order to compute the sensitivity based on (4.22).

Table 4.1: Summary of the parameters of the numerical simulation of the receiver for sensitivity analysis.

Parameter	Value
NF_{RA}	0 to 30 dB
k_B	1.38e-23 J/K
T	290 K
BW_{IF}	234.375 kHz
SNR_{min}	16 dB (for 16QAM)
k_{ED}	64 (1/V)
A_V	10 to 100 dB
$PSD_{added,ED}$	520 $\frac{nV}{\sqrt{Hz}}$ (peak amp.)

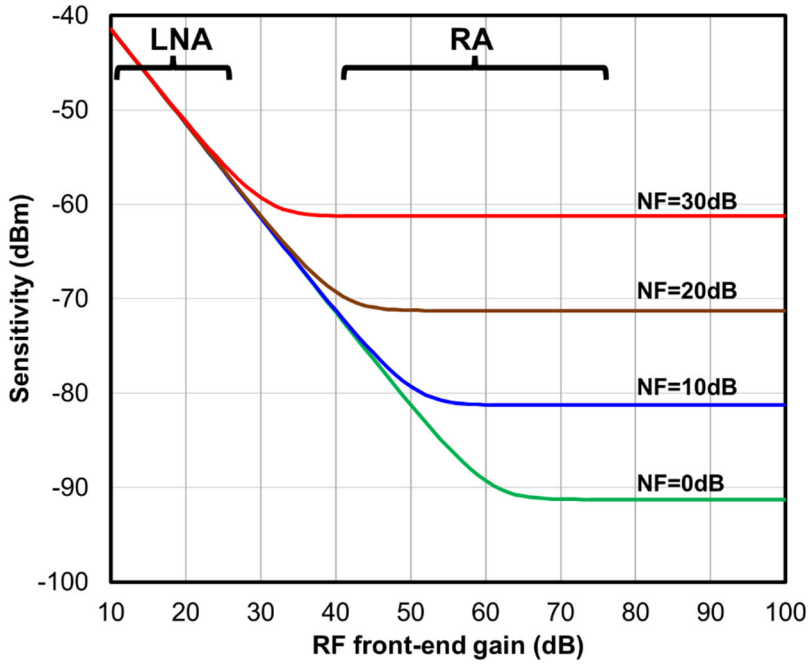


Figure 4.9: Analytical results of the sensitivity as a function of the DRAs RF front-end gain for different values of NF.

Fig. 4.9 shows the sensitivity as a function of the DRAs gain (RF front-end gain) for different values of NF, which confirms the similar results obtained in the previous chapter. Again, it can be seen that when the RF gain is still low, each dB increase in gain directly translates into a dB improvement in sensitivity. Also, a conventional LNA with a relatively low gain within the range of 10 ~ 20 dB, even with a perfect NF of 0 dB, cannot outperform an RA with a high gain (e.g. 50 dB) and a terrible NF (e.g. 20 dB).

Fig. 4.10 shows a numerical simulation model of the receiver's sensitivity performance in MATLAB. The three subcarriers have a symbol rate of 78.125 kS/s and are 16QAM modulated. The RF operation frequency is around 2.44 GHz. All the other important parameters of the receiver are also shown in the figure.

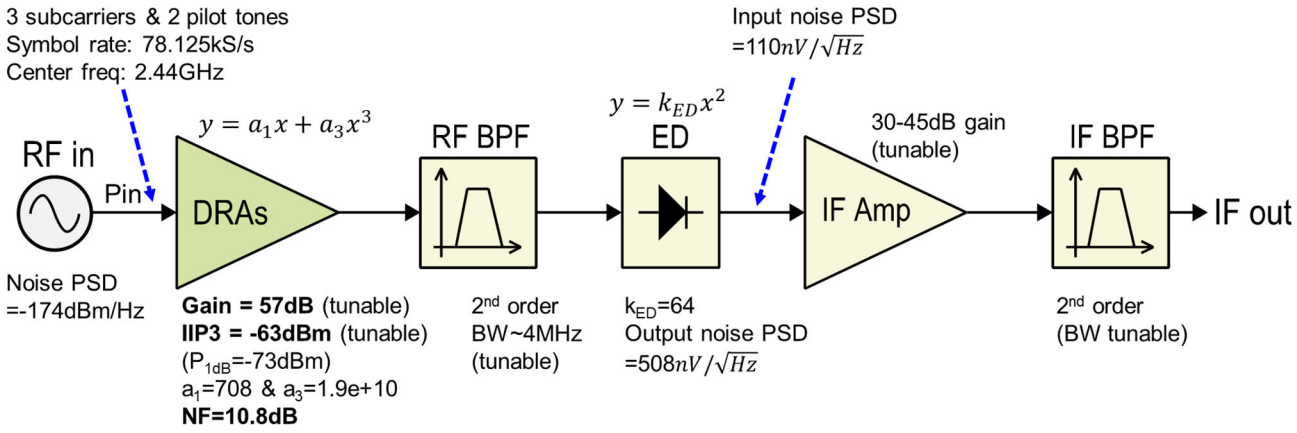


Figure 4.10: Numerical simulation model of the receiver's sensitivity performance.

Fig. 4.11 shows two representative spectral densities of the signal in the RF and IF domains, respectively. In the RF domain, the three subcarriers can clearly be seen along with the two pilot tones, located to the right of the subcarriers. In the IF domain, the desired three subcarriers are now located at approximately 390 kHz. The demodulation to compute bit error

rate (BER) is based on the inverse Fourier transform operation and will then be performed on these new three subcarriers at the IF frequency of around 390 kHz.

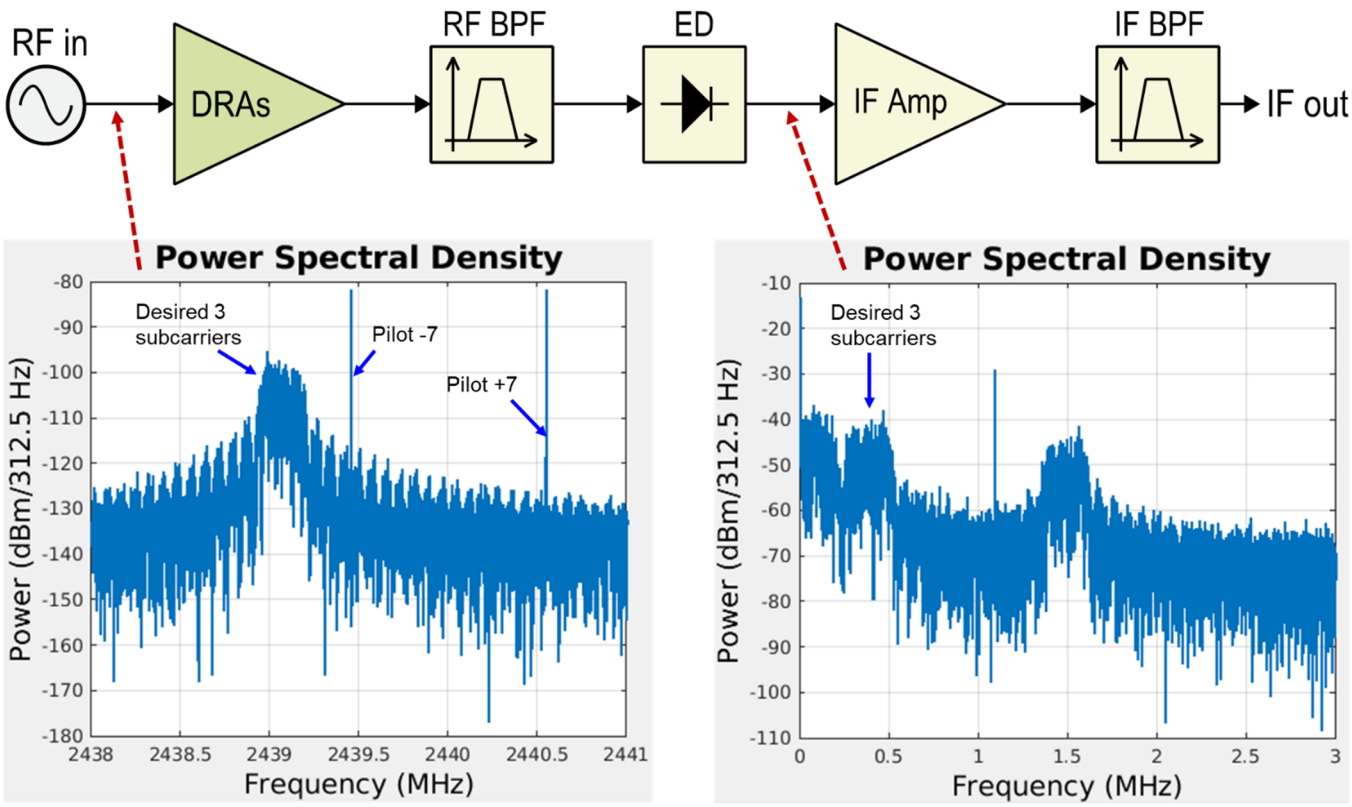


Figure 4.11: Representative spectral densities of the RF domain and the IF domain of the receiver, respectively.

Fig. 4.12 shows the constellations of the three subcarriers for different input powers, respectively. All the constellation diagrams have been normalized based on their mean power. It can be inferred from these diagrams that:

- At a low input power of P_{in} = -85 dBm, the received constellation diagrams of the three subcarriers are noisy, indicating a low SNR value and a high bit error rate (BER).

- At a medium input power of P_{in} = -78 dBm, the constellations are now much clearer, indicating a good SNR value that will lead to a very low BER. This input power is then close to the sensitivity level.
- However, at an even higher power level of P_{in} = -65 dBm, the constellations of the three subcarriers begin to be distorted, indicating that nonlinearity now starts to kick in. The nonlinearity stems from the limited P1dB or the IIP3 of the DRAs. As a result, there exists a certain dynamic range of the input signal for the best performance, which is bounded by the noise floor and the P1dB compression point of the receiver. Note that the previous analysis has not considered the effect of nonlinearity on the receiver performance, since it has mainly focused on the input signal level around the sensitivity.

Fig. 4.13 shows the simulated BER result of the receiver as a function of the input power. The simulation is done using a bit sequence of around 30000 bits which are split between the three subcarriers. An inverse Fourier transform computation is done in MATLAB to demodulate the bit sequence. By looking at the BER level of 10^{-3}, it can be seen that a sensitivity of around -80 dBm is achieved.

The next section will discuss the circuit implementation of the receiver in detail.

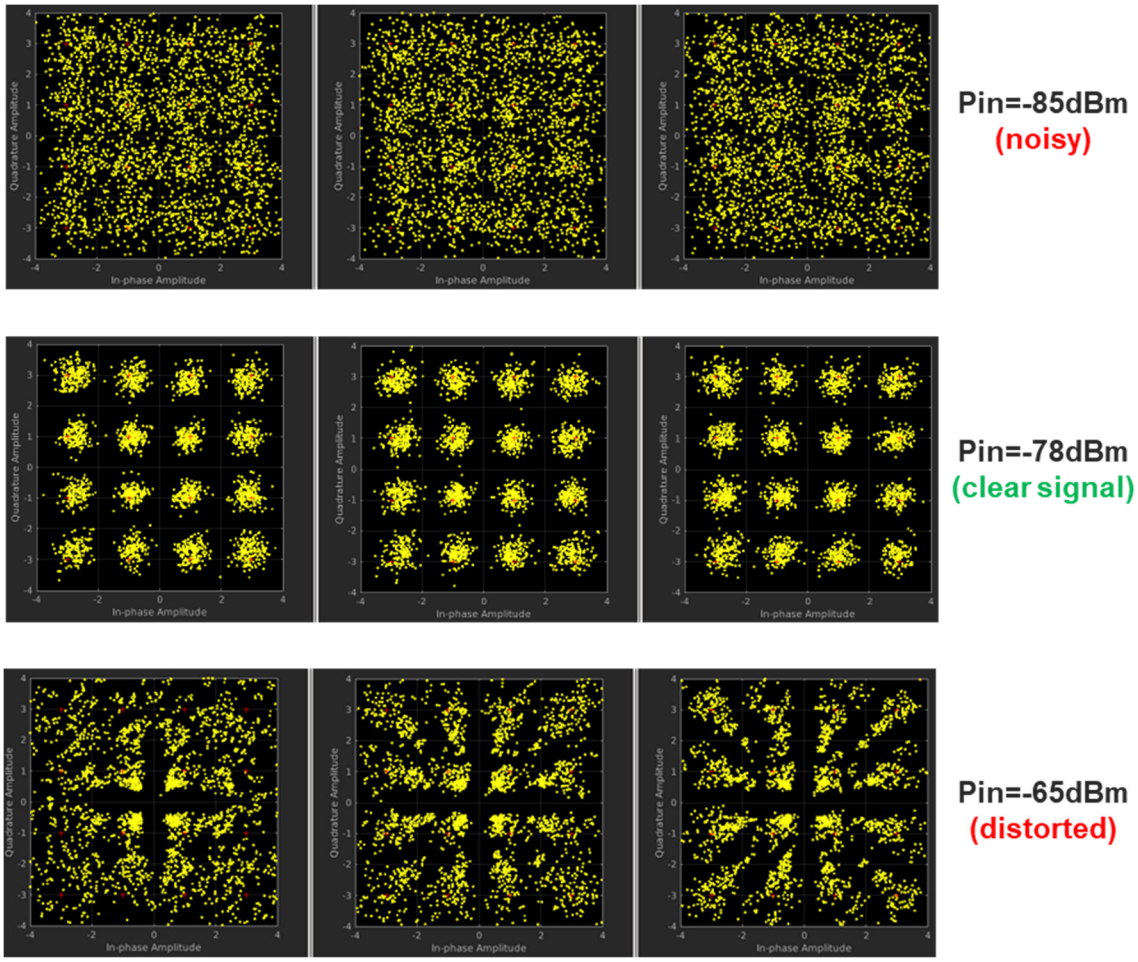


Figure 4.12: The simulated received constellation diagrams of the three subcarriers, respectively, for three different values of P_{in}.

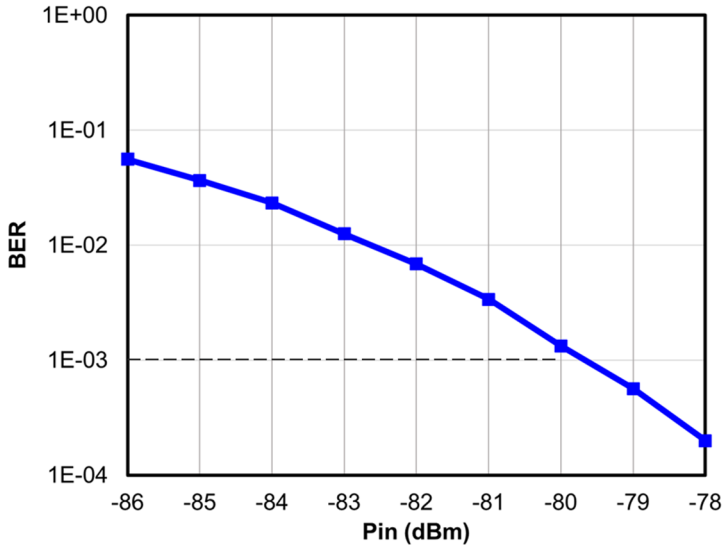


Figure 4.13: Simulated BER as a function of P_{in}, showing a sensitivity of around -80 dBm at $BER = 10^{-3}$.

IV – Circuit Implementation Details

Fig. 4.14 shows a block diagram of the overall receiver. The dual regenerative amplifiers (DRAs) concept is largely adopted from the design in the previous chapter with significant improvement, which will be discussed later in this section. Due to the requirement of a potentially high IF bandwidth and a high conversion gain, an active ED is chosen. An active ED also allows for post-fabrication tuning to optimize the performance during measurement. There are several additional blocks such as the all-digital phase-locked loop (ADPLL) and amplitude-locked loop (ALL). The ADPLL is used to calibrate the operation frequency intermittently for robustness, due to the narrow RF bandwidth of the receiver at around 2.4 GHz that can potentially lead to frequency variation over time. The ALL is to aid the ADPLL in performing frequency calibration, as discussed later in the chapter.

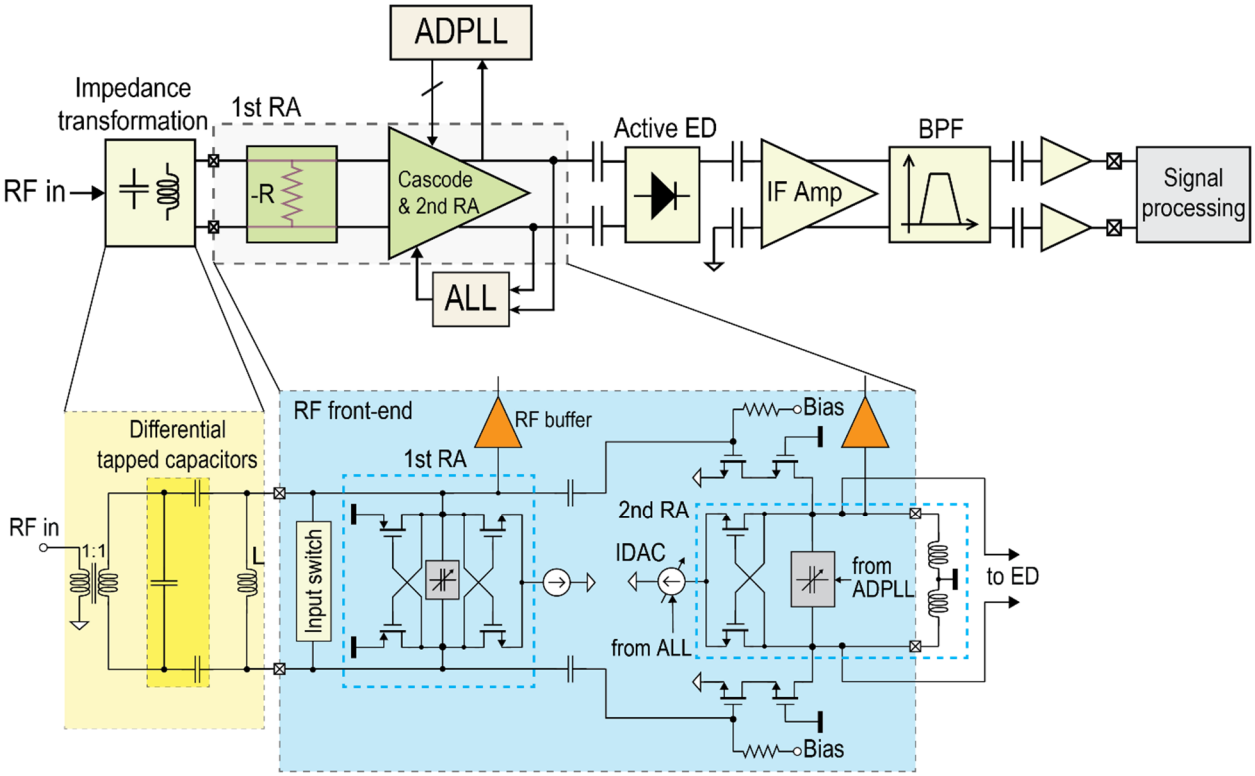


Figure 4.14: Block diagram of the proposed two-tone receiver for IEEE 802.11ax Wi-Fi standard.

Fig. 4.15 shows an example of the timing diagram of the operation of the receiver. Initially, the RF input can be turned off prior to frequency calibration. Then the bias current of the 2nd RA is now increased by the ALL to push it into the oscillation mode and frequency calibration now begins by the ADPLL. During the calibration, the ALL maintains the oscillation amplitude of the 2nd RA at a constant low value while the ADPLL performs its role of locking the oscillation frequency to an intended target frequency, depending on the particular application, e.g. 2446 MHz. Once frequency calibration is done, the bias current of the 2nd RA can be decreased to turn it back into an amplifier. The RF input is now turned back on and the normal operation resumes. An off-chip FPGA will control and oversee the whole operation of the individual blocks of the chip.

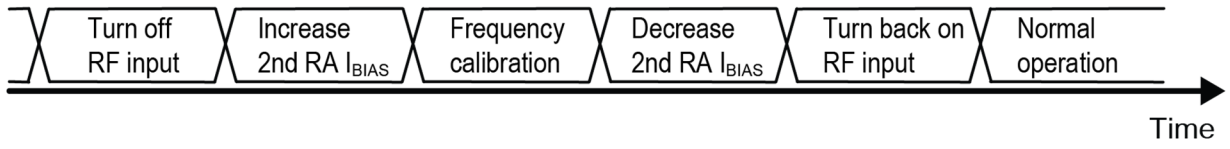


Figure 4.15: Example of a timing diagram of the operation of the receiver.

Due to the high target Q-factor of the receiver, the layout of the RF sensitive blocks, most notably the DRAs, proves critical to minimize resistive loss, prevent unwanted coupling, power loss to the substrate, etc. Since the lossy substrate can significantly degrade the overall Q-factor, leading to high power consumption if not taken into consideration, in the implementation of the DRAs, all the signal lines consist of two top metals which are connected by arrays of vias to minimize the series resistance. Fig. 4.16 shows the simplified layer stackup of a typical 65nm CMOS process. The bottom metal layers have the smallest thickness whereas the top ones are significantly larger and are located much further away from the lossy substrate.

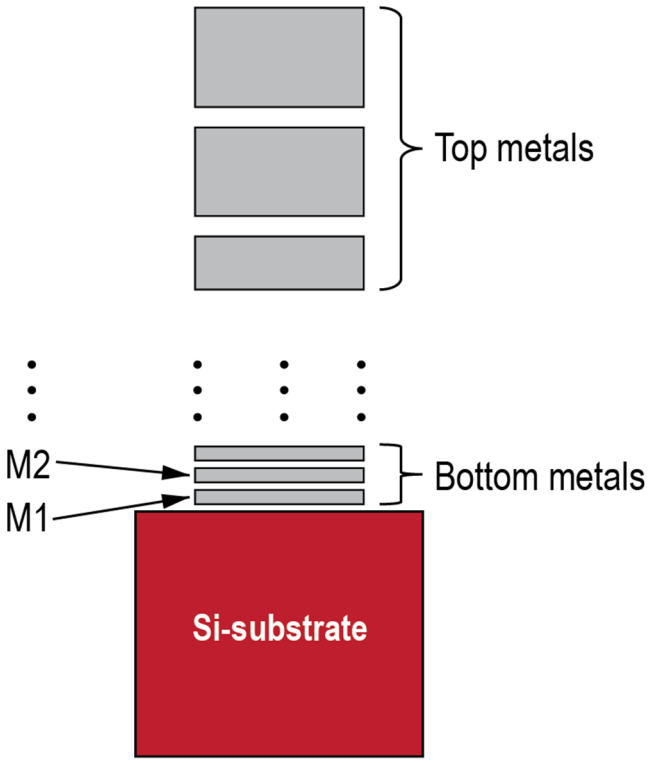


Figure 4.16: Simplified layer stackup of a typical 65nm CMOS process (not to scale).

In addition to using the two top-level metal layers to implement all RF signal lines, a ground shield beneath signal lines is also included to effectively prevent the electric field on the signal lines from entering the lossy substrate below, which would result in further power loss. Due to the density requirement, the ground shield is made up of two bottom metal layers metal M1 and metal M2, as shown in Fig. 4.17, with alternating slots. The slots are perpendicular to the signal line in order to minimize the unwanted Eddy current, effectively creating a slow-wave transmission line structure [53], helping maintain a high Q-factor. The two metal layers M1 and M2 are connected by arrays of vias further away on the two sides of the signal line and are grounded. The inclusion of the ground shield beneath the signal line leads to almost 10 times improvement on the quality factor while suffering from only a slight increase on the shunt

parasitic capacitance to ground. A similar structure is also used to implement other large-sized passive components, such as the RF input and output pads.

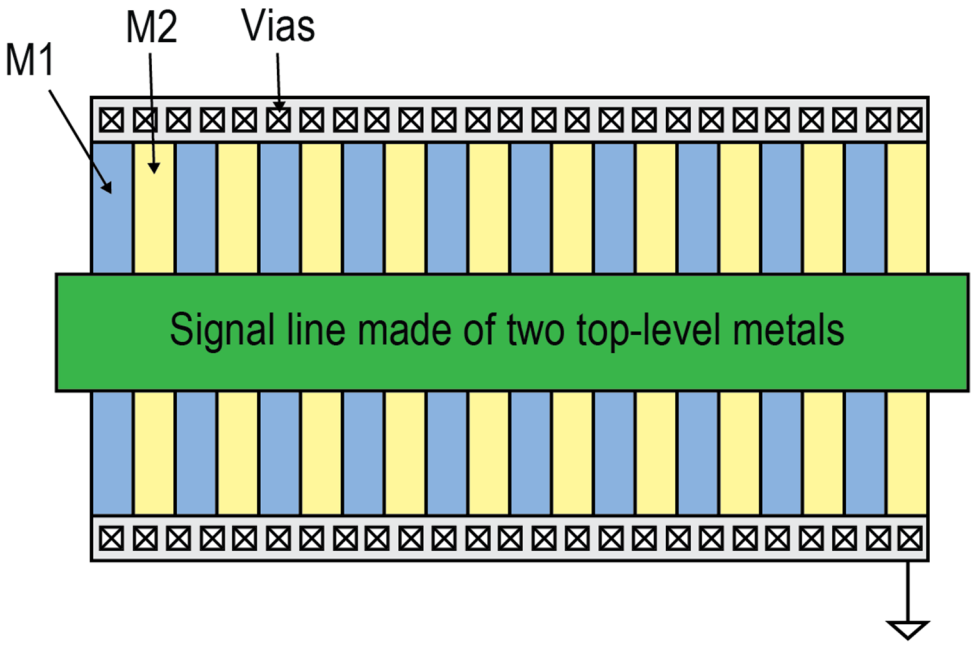


Figure 4.17: Implementation of RF signal line with ground shield beneath.

Fig. 4.18 shows the simulated S-parameters and NF of the DRAs around the center frequency of 2.44 GHz. The simulation setup is also shown at the top of the figure. It can be seen that the DRAs can achieve a narrow bandwidth and an S31 gain of more than 50 dB, which can easily be tuned by changing the bias current of the 1st RA, the bias voltage of the cascode, and the bias current of the 2nd RA, respectively. In these simulations, the DRAs are assumed to be connected to off-chip inductors with a Q-factor of 80.

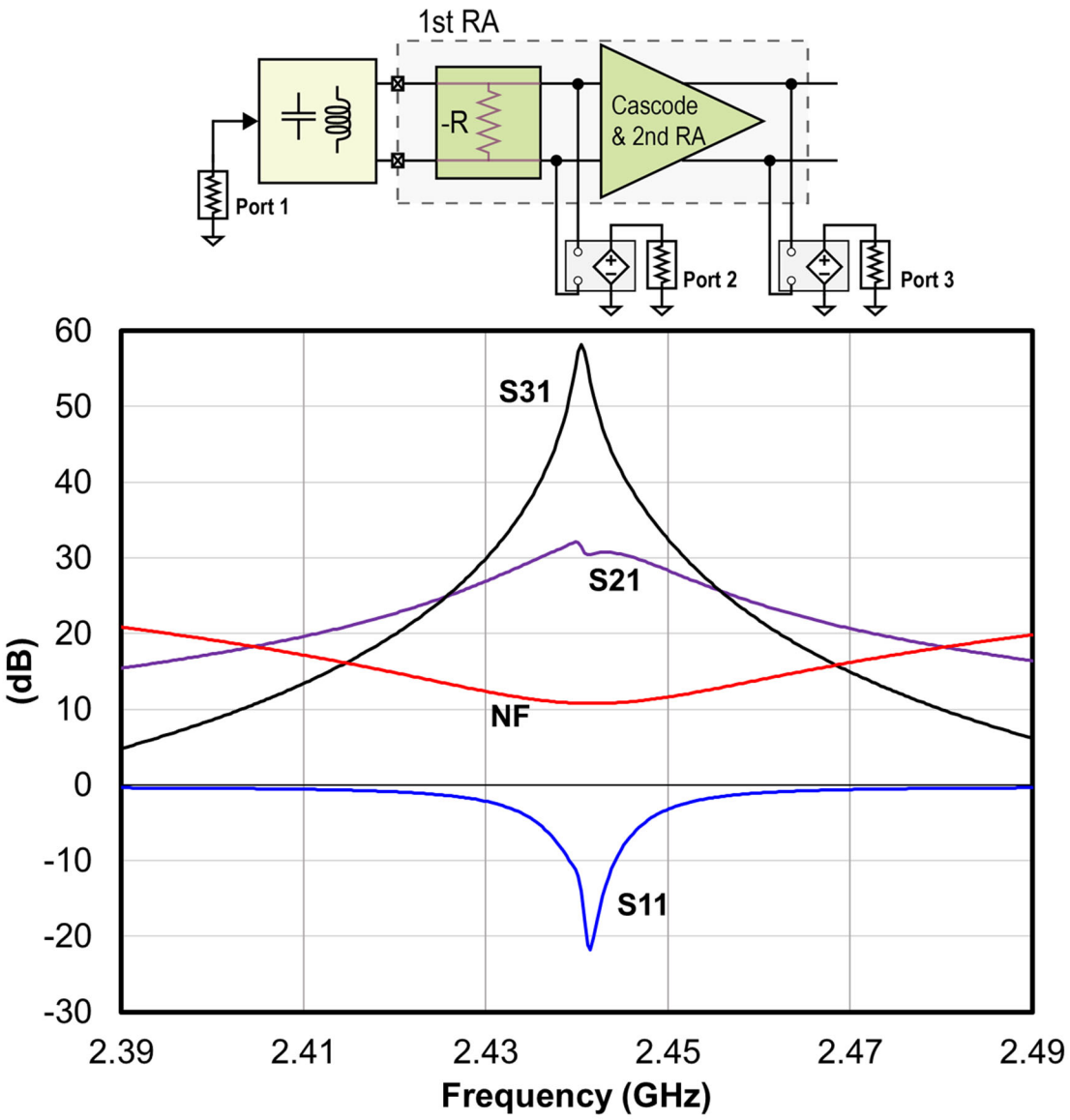


Figure 4.18: Simulation of S-parameters and NF of the DRAs at around the operation frequency of 2.44 GHz.

Table 4.2 shows the breakdown of the power consumption of the DRAs. The 2nd RA and the cascode consume the most power of the DRAs. This can simply be explained by considering that the cascode needs to have good noise performance in order not to degrade the overall NF, while the 2nd RA needs to generate a high g_m to cancel out almost all the parallel resistance of its output inductors to achieve a much higher Q-factor than the 1st RA. Table 4.3 summarizes the

simulated performance of the DRAs at the center frequency of around 2.44 GHz. It can be seen that the DRAs consume an ultra-low power while providing an extremely high gain with relatively low noise and good linearity performance.

Table 4.2: Breakdown of the power consumption of the DRAs.

Stage	I_{DC} (μA)
1st RA	7.2
Cascode	24.2
2nd RA	19.4
Other (I_{ref}, etc.)	1.2
Total	**52**

Table 4.3: Summary of the parameters of the DRAs.

	DRAs
Frequency	2.44 GHz
VDD (V)	0.5
Gain (dB)	>55
NF (dB)	10.8
P_{DC} (μW)	26
IIP3 (dBm)	>-63

Fig. 4.19 shows the schematic of the input switch of the DRAs to turn on/off the RF input for frequency and bandwidth calibration. Fig. 4.20 shows the simulated parameters of the DRAs again, including the S-parameters and NF when the RF input is turned off. It is clear that the

input switch is capable of achieving an isolation of approximately 50 dB between the RF input and the internal circuitry of the RF front-end in the OFF state, which can be critical for frequency calibration.

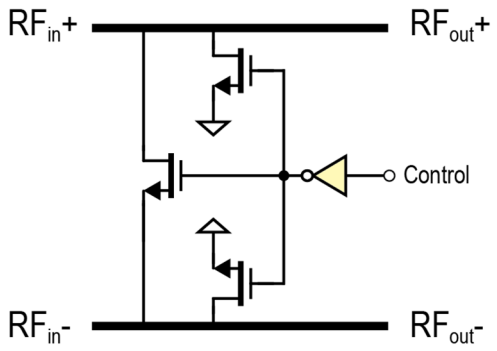


Figure 4.19: Schematic of the input switch of the DRAs.

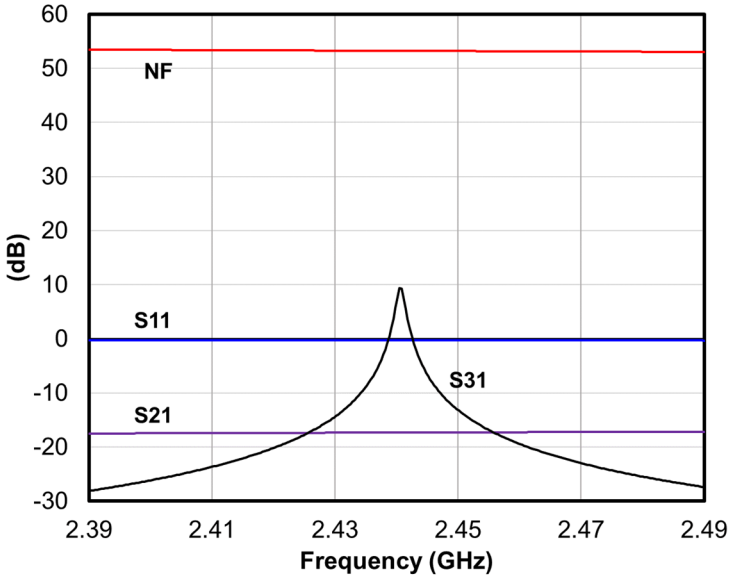


Figure 4.20: Simulation of S-parameters and NF of the DRAs at around the operation frequency of 2.44 GHz, when the input switch turns off the RF input.

Fig. 4.21 depicts the schematic of the RF buffer to observe the outputs of the 1st RA and 2nd RA, respectively. The buffer is simply a cascode configuration to obtain good isolation between the output and the input. The bias resistor on the gate of the common-source NMOS transistor is implemented using a pseudo-resistor to avoid loading the corresponding RA. The

drain resistor is chosen to be just 50 Ω to match with the output load. The AC-coupling capacitor C is to resonate out the RLC network of the die pad, the bond wire, and the PCB pad at the center frequency of interest of around 2.44 GHz. Two RF buffers are used for the two RAs, respectively. The two buffers also have slightly different sizing strategies to account for compression resulting from high signal power and noise performance. Fig. 4.22 shows the simulated gain and S22 of the buffer of the 1st RA. It can be seen that this buffer introduces a low loss of only approximately -8.5 dB while providing wideband matching around the center frequency of 2.44 GHz.

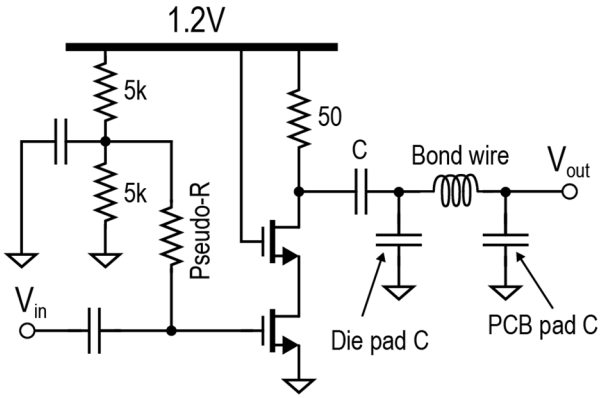


Figure 4.21: Schematic of the RF buffer to observe the outputs of the 1st RA and the 2nd RA, respectively.

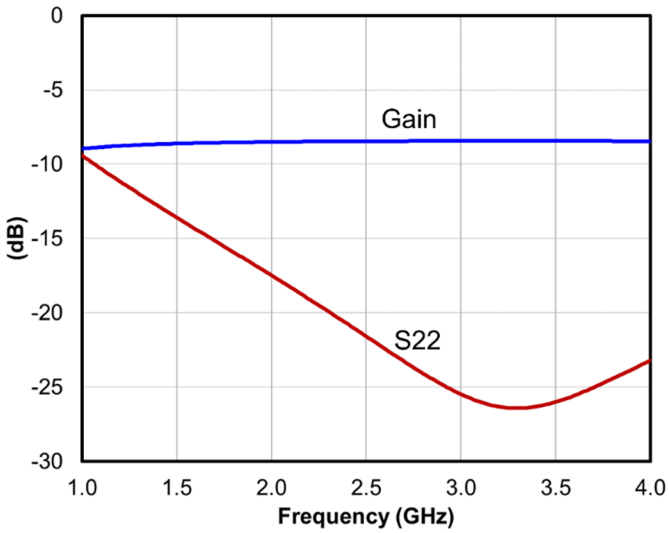


Figure 4.22: Simulated gain and S22 of the RF buffer of the 1st RA.

Fig. 4.23 shows the schematic of the active envelope detector (ED) used in the design. The two NMOS transistors are self-biased with pseudo-resistors to obtain high input impedance to avoid significantly loading the 2nd RA. The two NMOS transistors also see an active load made by a PMOS current mirror for high output impedance. Due to the squaring nature of the ED's operation, the ED can only output a single-ended signal and so the differential signaling scheme is no longer preserved. Lastly, the transistors operate in the sub-threshold region and are biased as dynamic-threshold MOS (DTMOS) in order to increase the conversion gain even further; a similar topology has been used in [7, 9].

Fig. 4.24 shows the simulated conversion gain of the active ED as a function of the frequency spacing of an RF two-tone input for different values of the reference current I_{REF}. The two tones are centered at around 2.44 GHz and are fixed at 10mV each; the frequency spacing is swept from 10 kHz to 10 MHz. The simulation is performed while considering the loading effect of the IF amplifier. The conversion gain with respect to the amplitude of 10 mV of one tone is given by:

$$G(dB) = 20 \times \log\left[\frac{V_{IF,out}(V)}{0.01(V)}\right] \tag{4.23}$$

It can be seen that the more current the ED consumes, the lower the conversion gain while the bandwidth is wider. This can be explained by the fact that the two DTMOS transistors slowly transition out of the sub-threshold region as I_{REF} increases, leading to a lower second-order nonlinearity. The simulated conversion gain shows an effective k-factor k_{ED} of approximately $64\left(\frac{1}{V}\right)$ for a reference current of 2 μA within the passband of the ED and a 3-dB cut-off frequency of larger than 10 MHz, which is sufficient for the target center frequency of ~400 kHz of the three subcarriers.

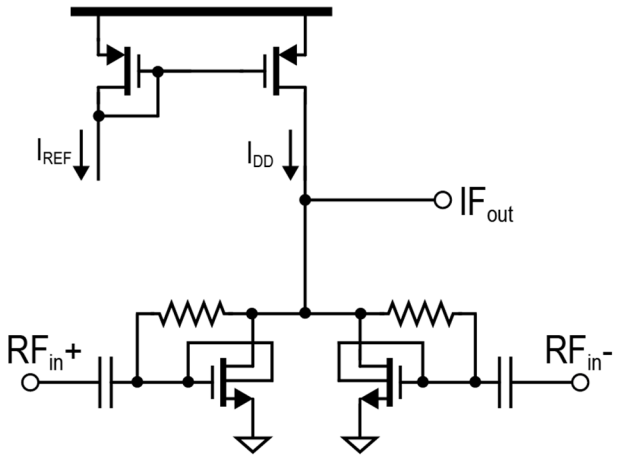


Figure 4.23: Schematic of the active envelope detector (ED).

Fig. 4.25 shows the simulation of the output noise of the active ED. It can be seen that the flicker noise is negligible around the IF center frequency of 400 kHz. In addition, the noise PSD near 400 kHz is around 508 $nV/\sqrt{Hz}$. In this simulation, the loading of the following block, which is the IF amplifier, is also considered.

Fig. 4.26 shows the simulated input shunt resistance and simulated input shunt capacitance of the ED, around the RF operation frequency of 2.44 GHz for different values of the reference current I_{REF}. Assuming an overall inductor of 11 nH with a Q-factor of 80, the resistive part of the input impedance is completely insignificant and will not load the 2nd RA substantially while standing alongside the inductor, while the capacitive part can simply be absorbed into the output network of the 2nd RA.

The bottom line of the simulation of the ED is that by employing an active ED, the reference current can be tuned to optimize the conversion gain, the 3-dB cutoff frequency, the output noise, as well as the input impedance of the ED. The higher the current consumption of the ED, the lower the conversion gain, the wider the ED bandwidth, and the lower the output noise PSD.

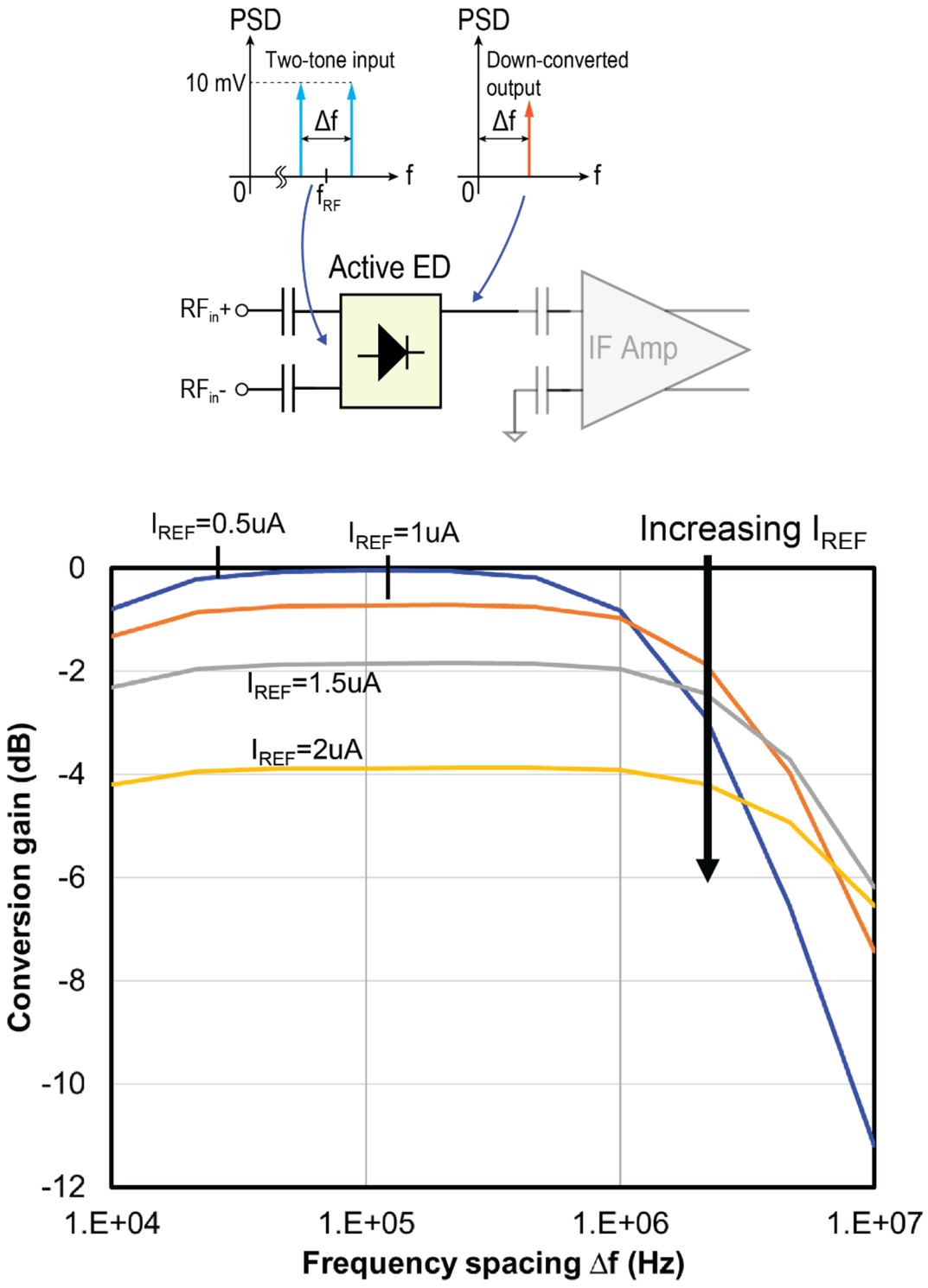


Figure 4.24: Simulation of the conversion gain of the active ED as a function of the frequency spacing of a two-tone input at around 2.44 GHz for different values of the reference current I_{REF}.

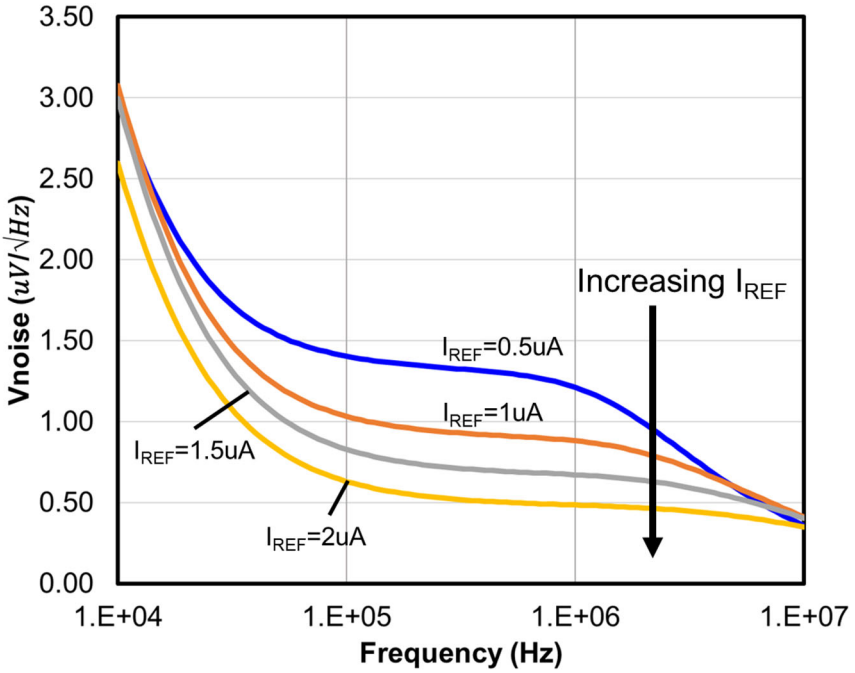


Figure 4.25: Simulation of the noise PSD at the output of the ED as a function of frequency for different values of the reference current I_{REF}.

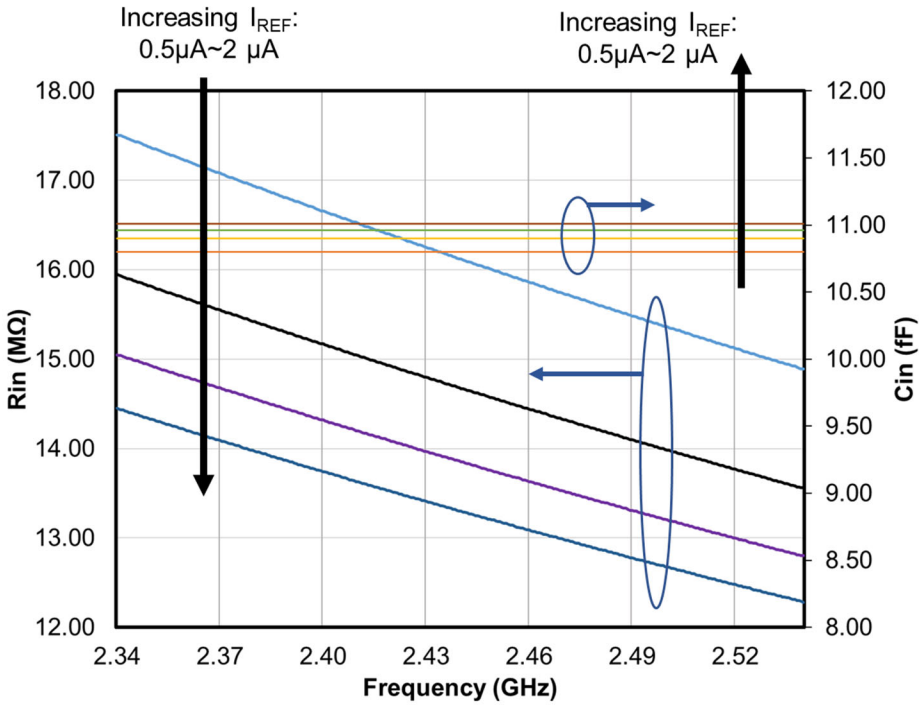


Figure 4.26: Simulation of the input shunt resistance and shunt capacitance of the ED as a function of frequency for different values of the reference current I_{REF}.

Fig. 4.27 shows the simplified schematic of the IF amplifier and the bandpass filter (BPF). Both the IF amplifier and the BPF are implemented using differential g_m cells, with common-mode feedback (CMFB) for bias stabilization. The amplifying differential pair in each g_m cell is made up of two PMOS transistors with relatively large size for low flicker noise. Each capacitor of the BPF is implemented using 5-bit switched capacitor arrays. The center frequency and the Q-factor of the BPF can be given by:

$$\omega_0 = \sqrt{\frac{g_m^2}{C_1 C_2}} \tag{4.24}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{4.25}$$

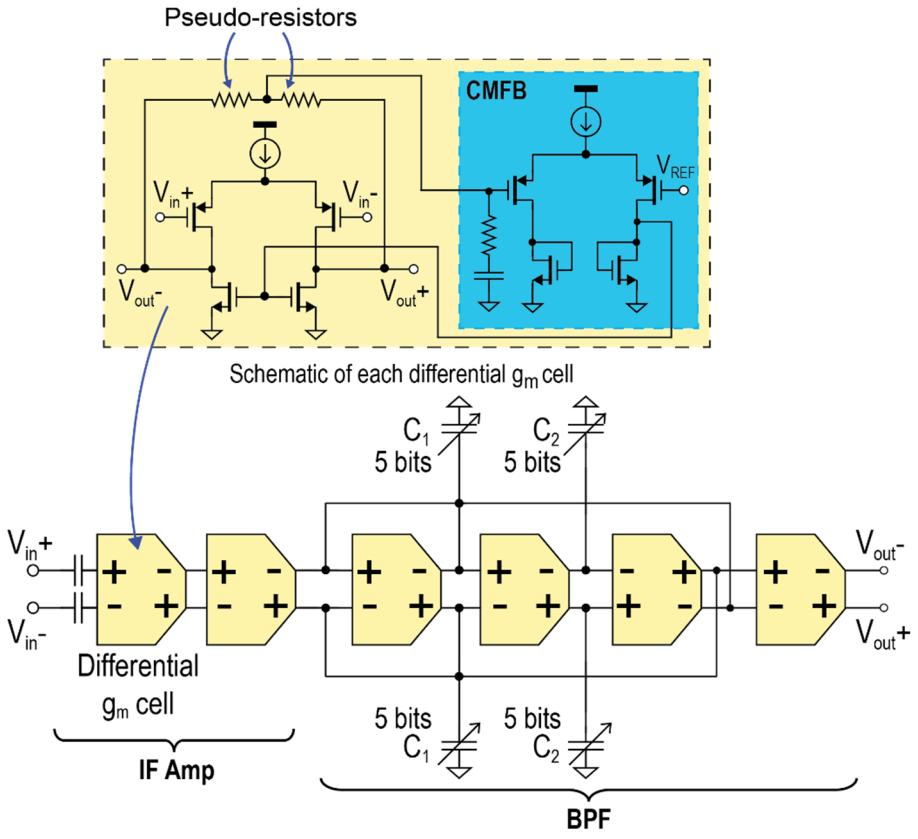


Figure 4.27: Schematic of the IF amplifier and the BPF.

Fig. 4.28 shows the simulated input-referred noise spectral density of the IF amplifier. The noise density at around ~400 kHz is approximately 110 $nV/\sqrt{Hz}$. In addition, thanks to the high gain of the IF amplifier, its input-referred noise essentially dictates the input-referred noise of the IF circuitry.

Fig. 4.29 shows an example of the simulated frequency response of the IF amplifier and the BPF for several different values of capacitor tuning. It can be seen that the frequency response can be tuned to cover a wide range of frequencies, including the target center frequency of ~400 kHz with a total nominal gain of around 39 dB.

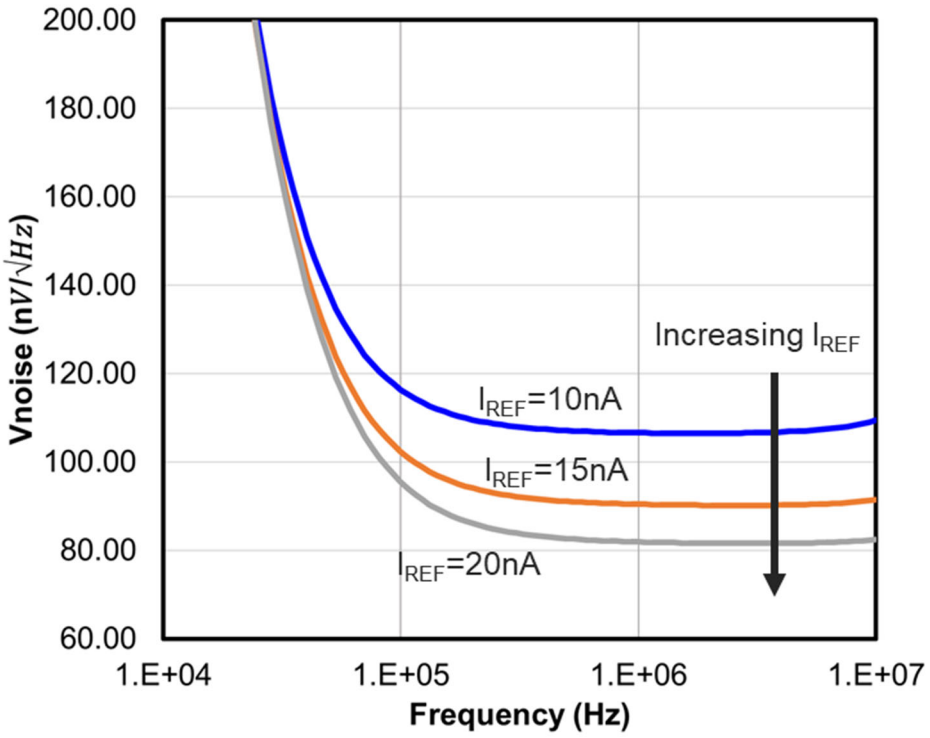


Figure 4.28: Simulation of the input-referred noise spectral density of the IF amplifier.

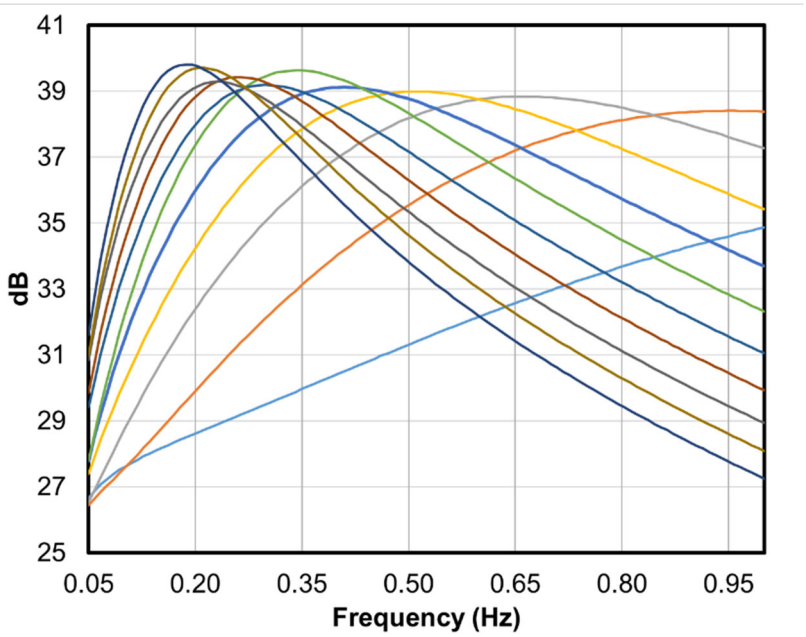


Figure 4.29: Simulated frequency response of the IF amplifier and the BPF for different values of capacitor tuning.

Due to the high capacitance of the output die pads, analog buffers are used to take the IF output of the BPF to the outside world. Fig. 4.30 is the schematic of each of the analog buffers in the receiver, which is a source follower operating at a VDD of 1.2 V which is shared with the RF buffers. The bias resistor on the gate of the source follower is made of a pseudo-resistor for high input impedance. Each analog buffer is able to handle a heavy off-chip load of 1 pF and 1 MΩ, which is typical of an input probe of an oscilloscope.

Fig. 4.31 shows the frequency response of the analog buffer connected with an output pad and a load of 1 pF and 1 MΩ. It can be seen that the buffer is essentially able to preserve the signal amplitude with only less than -1 dB of loss across a wide range of bandwidth, with a 3-dB cutoff frequency of higher than 5 MHz.

Fig. 4.32 shows a block diagram of the amplitude-locked loop (ALL). The ALL is connected to the output of the 2nd RA to sense its oscillation amplitude. The main purpose of the

ALL is to detect the operation state of the 2nd RA, whether it is in oscillatory mode or amplification mode. In addition, the ALL also maintains a constant and small oscillation amplitude to assist the ADPLL in frequency calibration.

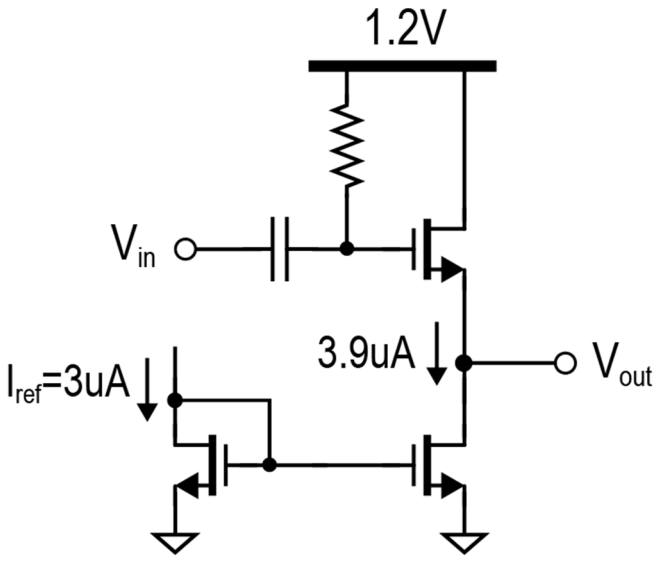


Figure 4.30: Schematic of the analog buffer for IF signal.

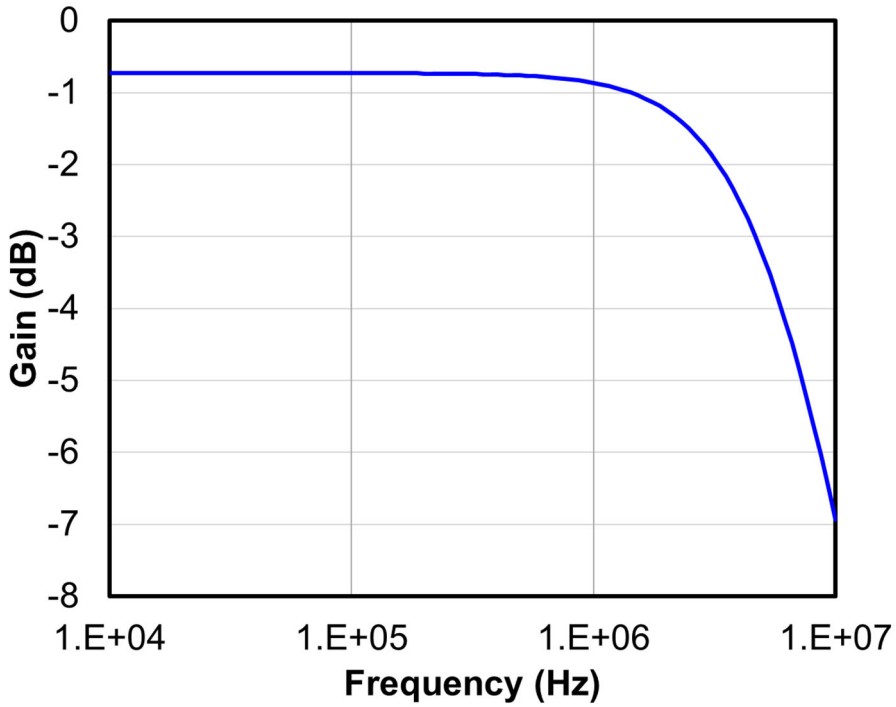


Figure 4.31: Simulation of the frequency response of the analog buffer.

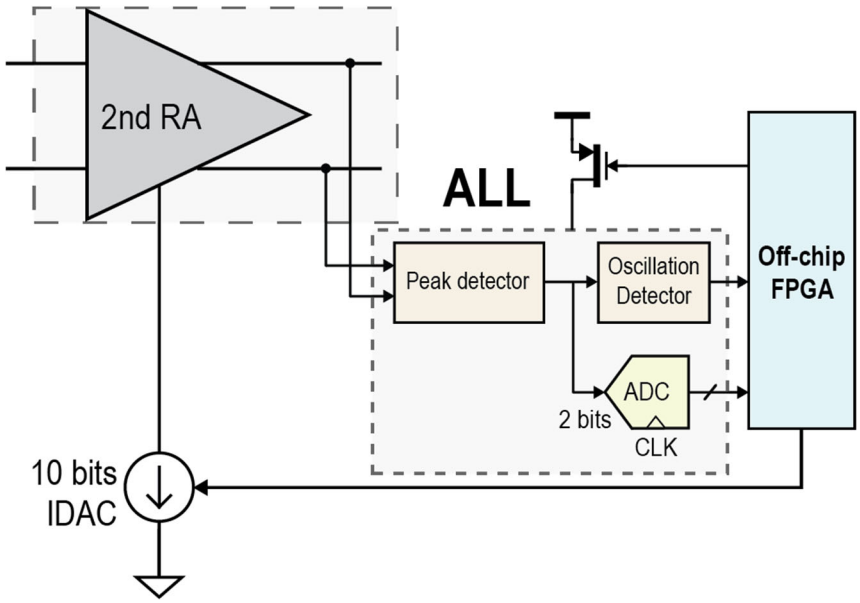


Figure 4.32: Schematic of the ALL.

Fig. 4.33 shows the schematic of the peak detector of the ALL connected with the 2nd RA, consisting of a main source follower and a dummy one. The main source follower converts the oscillation of the 2nd RA into a DC voltage, whereas the dummy one maintains a DC reference on its output with respect to the main source follower. Since it is critical to detect a small amplitude of oscillation of the 2nd RA, when there is no oscillation, the DC voltage on the output of the main source follower must be identical to that on the dummy source follower. In order to ensure that it is the case, the gates of the main source follower are not directly connected to the 2nd RA but via AC-coupling capacitors and biased via pseudo-resistors, to avoid taking on the inevitable offset stemming from the output of the 2nd RA.

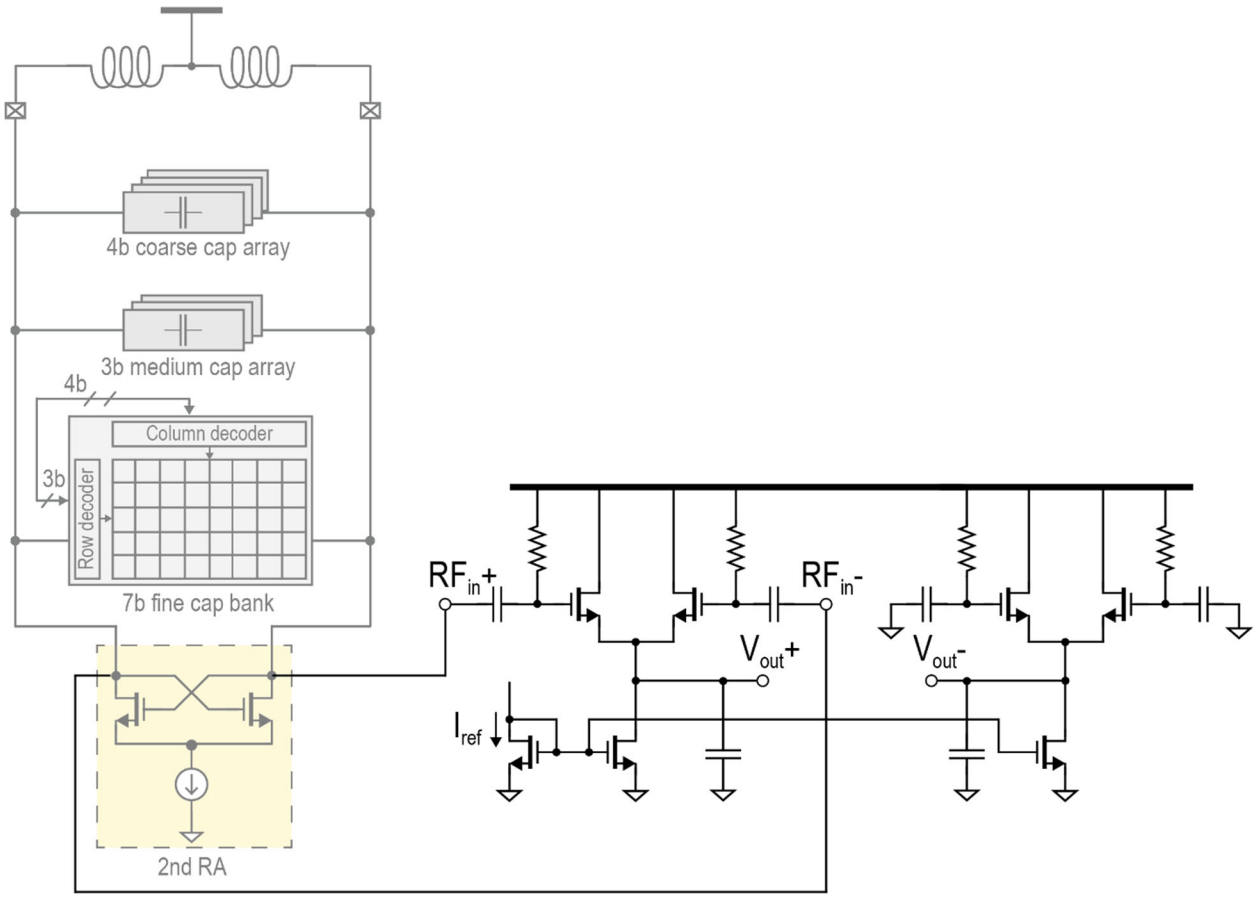


Figure 4.33: Schematic of the peak detector of the ALL.

Fig. 4.34 shows the schematic of the oscillation detector of the ALL. The detector consists of a differential g_m cell followed by a comparator clocked at the universal clock of 1 MHz. Due to the offset voltage which comes from multiple sources such as the inherent mismatch of the preceding peak detector, the differential g_m cell, the following clocked comparator, etc., the body of one amplifying PMOS transistor of the differential g_m cell is tunable whereas that of the other PMOS is fixed at $V_{CM} = 250\,mV$, as shown in the figure. By allowing V_{tune} to be controlled flexibly from off-chip, the offset that exists at the oscillation

detector input can be tuned to be virtually any small value, making it possible to detect a small oscillation amplitude if needed.

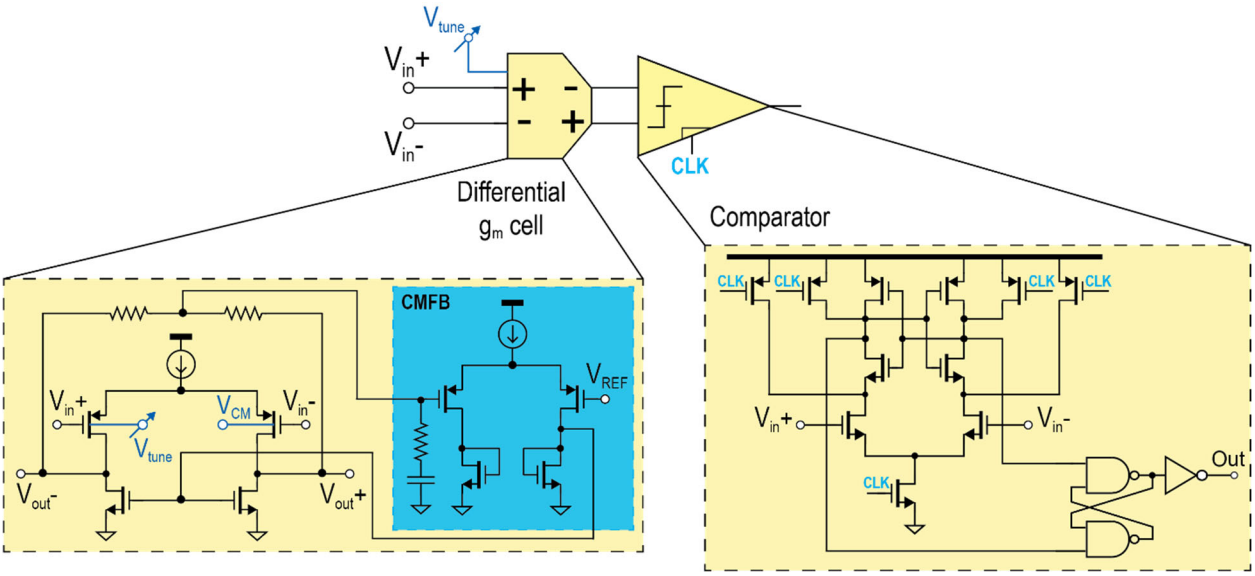


Figure 4.34: Schematic of the oscillation detector.

Fig. 4.35 shows the schematic of the analog-to-digital converter (ADC) of the ALL. The ADC consists of 2 bits and is similar to a flash configuration where the three clocked comparators are connected to a chain of four identical resistors in series. A thermometer-to-binary converter is used to convert the three comparator outputs into a 2-bit binary output. The comparators share the same universal clock of 1 MHz from the overall chip. The comparator topology is adopted from the one used in the oscillation detector, as discussed earlier.

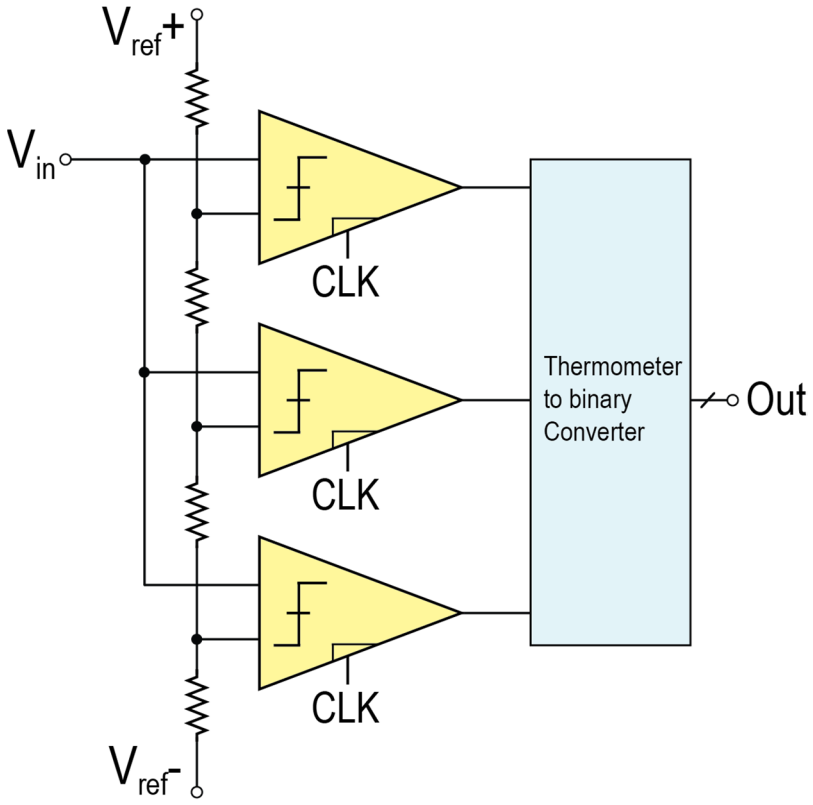


Figure 4.35: Schematic of the ADC of the ALL.

In [4], it is mentioned that for frequency calibration, the amplitude of the oscillation should be kept low such that the offset between the calibrated frequency and the normal operation frequency remains small. To that end, Fig. 4.36 shows a simple exemplary algorithm of the off-chip FPGA to lock the oscillation amplitude of the 2nd RA through the ALL to only a small value of around 100 mV. The algorithm detects the oscillation of the 2nd RA and enables the operation of the 2-bit numerical comparator. Based on how the two reference voltages of the ADC are chosen with respect to the target desired oscillation amplitude, the comparison threshold of the 2-bit comparator can be set accordingly. Note that due to the non-unity conversion gain of the peak detector, calibration needs to be done prior to receiver operation in order to determine the relationship between the peak detector's output voltage amplitude and the corresponding oscillation amplitude of the 2nd RA, ultimately to properly select the references for

the ADC. Then, as long as the peak detector's output amplitude is still higher than the target value, i.e. the corresponding oscillation amplitude is still higher than the desired value, the 2-bit comparator will keep clocking the down counter and enable the amplitude retainer to pass the output of the down counter through, continuously reducing the bias current on the 2nd RA.

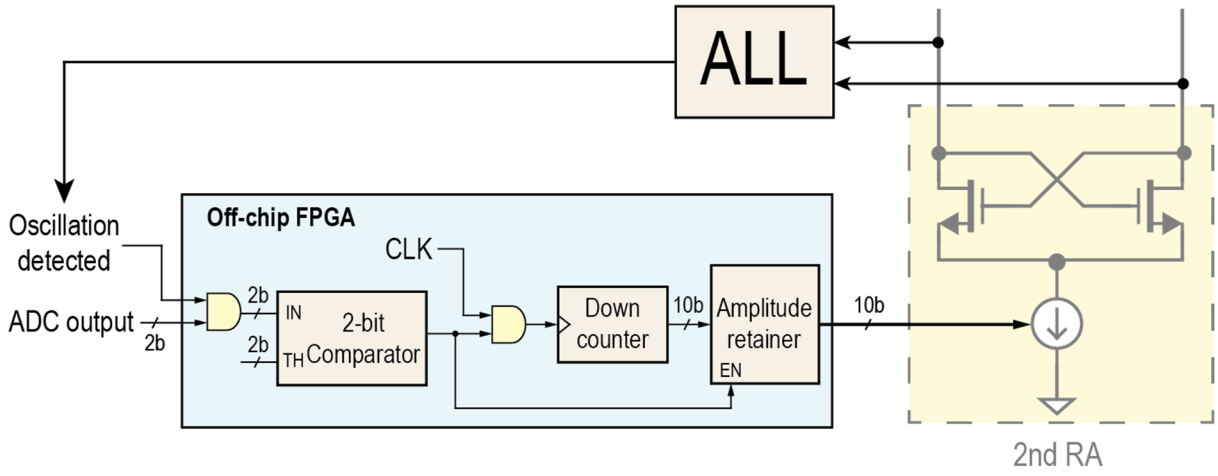


Figure 4.36: A simple exemplary algorithm of the ALL to lock the oscillation amplitude.

In Fig. 4.37, the timing diagram of the simulation of the exemplary ALL operation is depicted. At around 2 μs, the algorithm starts and the bias current on the 2nd RA decreases with time, leading to a continuation of the decrease of its oscillation amplitude. The continuously decreasing oscillation amplitude of the 2nd RA leads to the continuously decreasing output voltage amplitude of the peak detector. At around 4 μs, once this voltage amplitude is lower than a desired threshold, which is approximately 250 mV, the 2-bit comparator will output a LOW, blocking the clock from entering the down counter, and freezing the amplitude retainer. The amplitude retainer can be implemented using an array of ten D latches with a common enable (EN) pin. Once the EN pin is negated, the bias current will be frozen and the oscillation amplitude of the 2nd RA is locked to the corresponding desired target value, e.g. 100 mV.

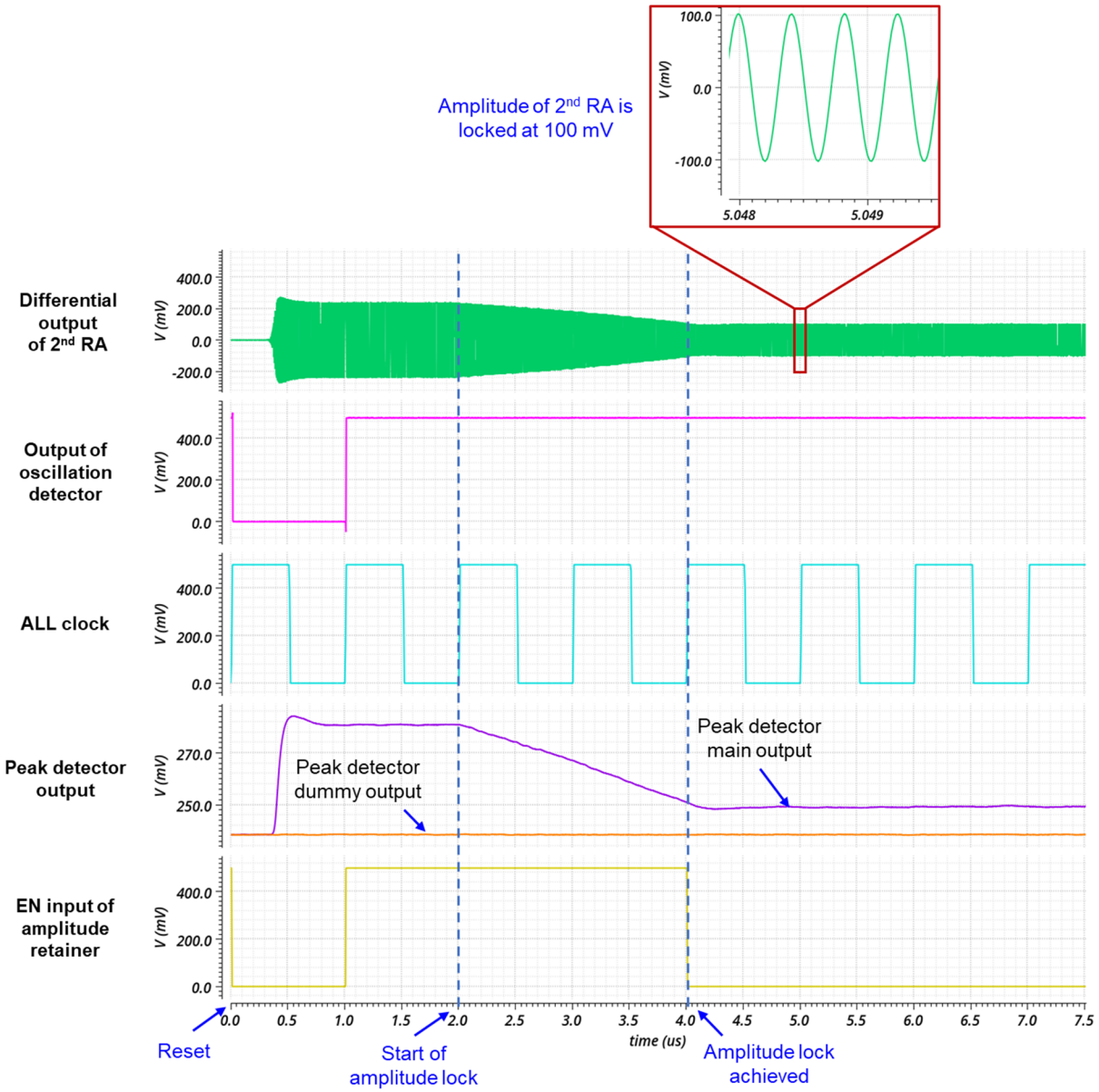


Figure 4.37: Timing diagram of the exemplary simulation of the ALL operation.

Fig. 4.38 shows a block diagram of the all-digital phase-locked loop (ADPLL). The ADPLL consists of a buffer to amplify the analog small sinusoidal signal from the 2nd RA into a rail-to-rail digital signal. The divide-by-N block divides the 2.4 GHz digital pulses into approximately 1 MHz for phase comparison with the reference universal clock of 1 MHz. The time-to-digital converter (TDC) digitizes the phase error and passes it through the thermometer-

to-binary encoder, where the output is converted into a binary value. The digital loop filter (DLF) filters this binary value and sends it into a “frequency retainer”, which is an array of 10 D latches, that controls the center frequency of the 2nd RA via a system of switched capacitors.

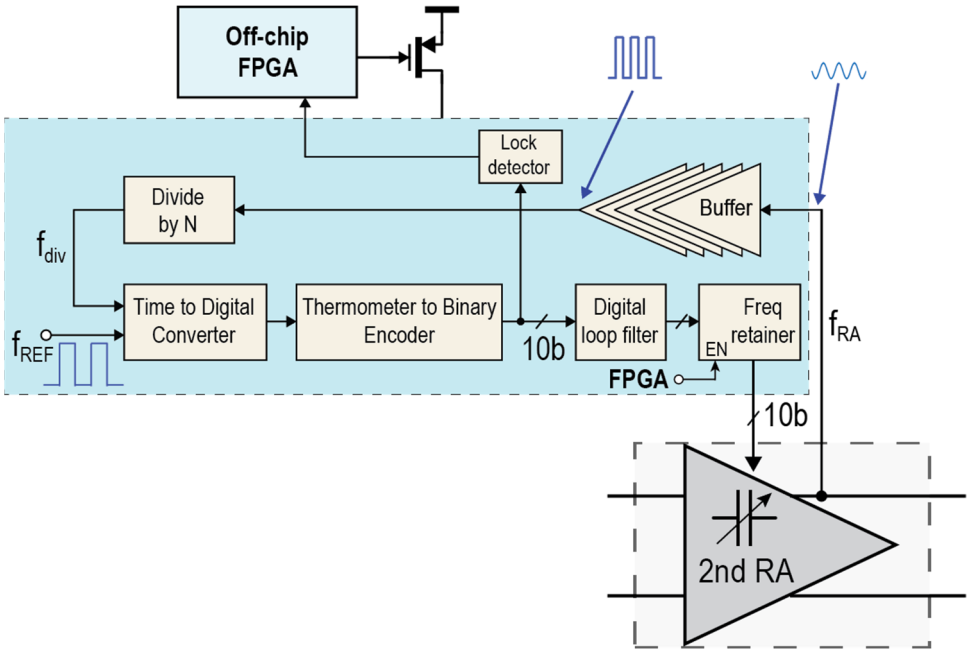


Figure 4.38: Block diagram of the ADPLL.

Fig. 4.39 shows the schematic of the buffer of the ADPLL. The buffer consists of five inverter-based amplifying stages to convert a small-amplitude sine wave of approximately 100 mV at 2.44 GHz into a rail-to-rail square wave. This topology where the gates of the NMOS and PMOS transistors are biased at certain voltages to effectively increase their drive strengths allows for a high speed and low voltage application. A similar topology has been adopted in [54].

Fig. 4.40 shows the block diagram of the divide-by-N [55]. It consists of a divide-by-2, which is implemented using true single phase clock D-flip flops (TSPC DFF). A prescaler with a

module of 8 or 9 follows. The rest of the divide-by-N consists of a program counter with the P value configurable from 1 to 150, and the S value configurable from 1 to 40. Therefore, the overall divide ratio of the divide-by-N can be set anywhere from 1150 to 4224.

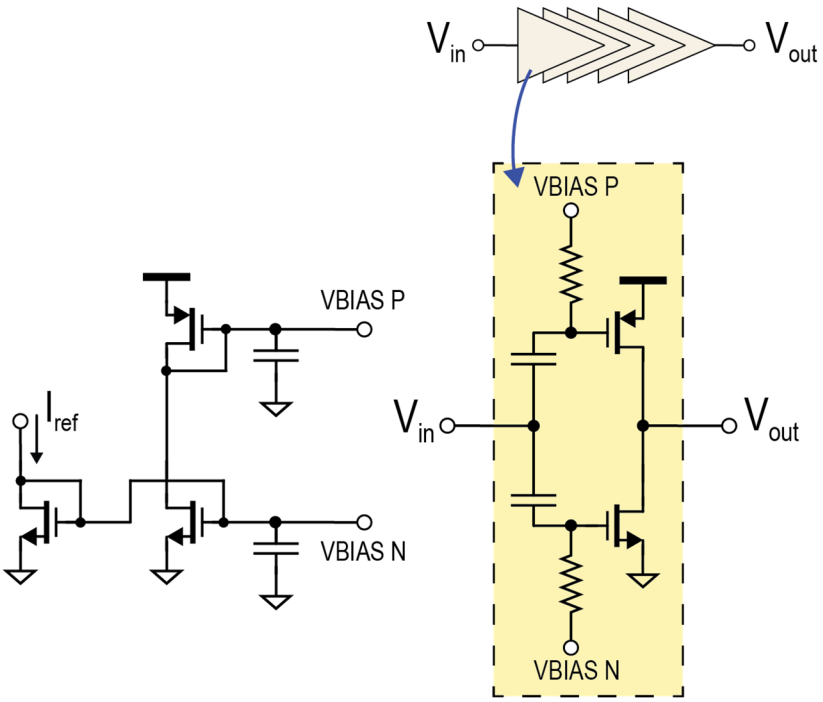


Figure 4.39: Schematic of the buffer of the ADPLL.

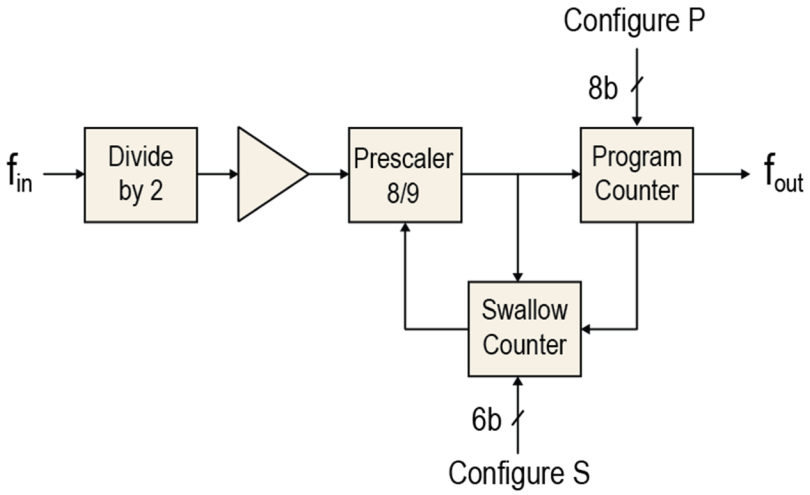


Figure 4.40: Block diagram of the divide-by-N block.

Fig. 4.41 illustrates how a typical TDC works to digitize the phase error. A chain of delay cells is connected in series to delay the input clock f_{in} by one unit delay as the input propagates along the chain. The output of each delay cell is sampled by a reference clock f_{REF} via the use of a D flip-flop (DFF). The overall output of the TDC will then be the combination of all the DFF outputs, which is a thermometer value equal to the digitized phase error of f_{in} and f_{REF}.

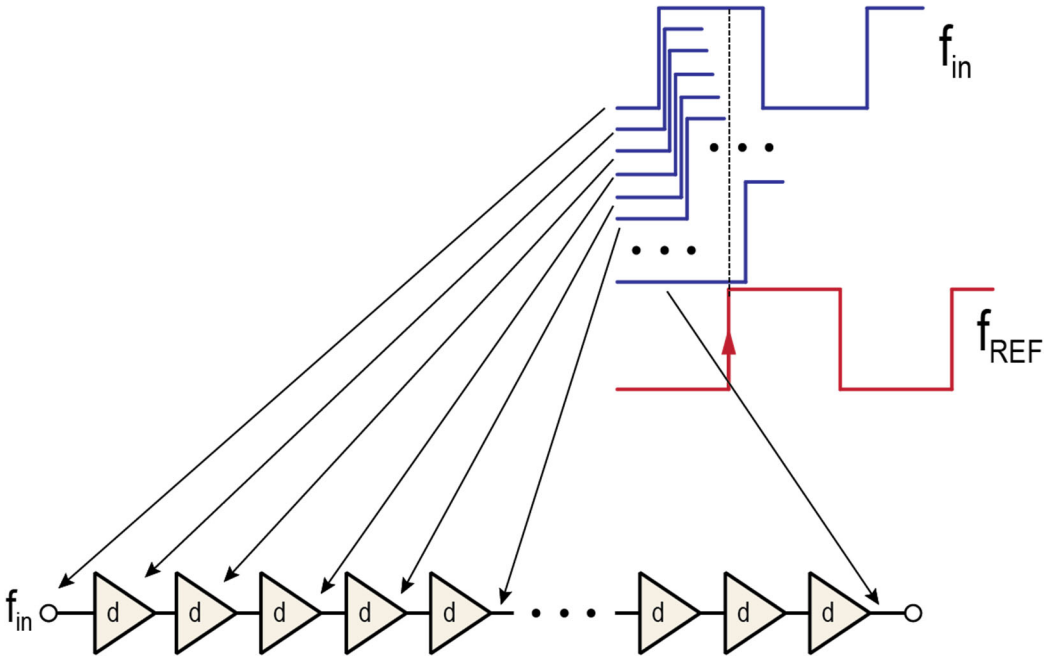


Figure 4.41: Simple diagram showing the operation of a typical TDC.

A challenge associated with the TDC is that each delay cell must have a fine resolution, i.e. the delay must be small enough, for example: a few ps, for low phase noise and low frequency variation. In addition, the TDC must be able to digitize a full clock period, e.g. 1μs of the reference frequency. These two requirements indicate that the TDC can potentially contain an extremely large number of delay cells and therefore be extremely large in terms of size, which will definitely incur mismatch between the delay cells, non-monotonicity, and nonlinearity [55].

In the design of the ADPLL, the TDC is divided into three smaller TDCs: a “coarse”, “medium”, and a “fine” TDCs. Their connection is illustrated in Fig. 4.42. In order to properly

digitize the phase error, the “5-bit” coarse TDC will first bring down the phase error to only less than 32 ns. Then “5-bit” medium TDC will then further bring this phase error down to only less than 1 ns. Finally, the “7-bit” fine TDC will be able to digitize this small phase error of less than 1 ns. The coarse TDC has a LOCK_C output to indicate when the excessive phase error has been reduced to lower than 32 ns, which will then enable the operation of the medium TDC.

The schematic of the coarse TDC is depicted in Fig. 4.43. Each delay element of the coarse TDC is made up of a current-starved inverter chain [56]. The coarse TDC topology allows for off-chip calibration of the delay of each element by simply asserting the Cal EN pin and observing the total delay of 31 elements from f_{REF}. Since there are 31 delay elements, the calibration should then be done to determine the bias voltage of each delay cell to obtain each delay of around 32 ns in order to cover the whole clock period. The output of the last DFF of the delay chain is not used but is there only to ensure matching between the delay elements. As usual, a 5-bit thermometer-to-binary converter is used to convert the thermometer output of the delay chain into a binary value, which will pass through an array of 5 D latches and then will control a 32-to-1 MUX. Based on the value of the control input, the MUX will pick the particular output of the delay chain that is closest in phase to the reference clock f_{REF}. A last block that consists of two identical delay elements to those in the delay chain is used to compare the final phases of the MUX output and f_{REF}, if the phases are close to each other, i.e. less than 32 ns, this comparing block will output a HIGH to freeze the D latches and to indicate that “phase lock” has been achieved. The MUX will then only let that particular delay element output to pass through to the total output of the coarse TDC. The “Lock indicator” will enable the operation of the medium TDC, which is implemented based on a similar topology.

Fig. 4.44 illustrates in detail how the excessive phase error at the coarse TDC input is brought down to only less than the delay of a single delay element. In Fig. 4.44, all the blue waveforms are the respective outputs of the first delay element, the second one, the third one, and so on. To the right of these blue waveforms are their respective outputs sampled by the reference clock f_{REF}. It can be seen that simply by summing up the outputs of all these delay elements, which is thermometer-coded, the result will be equal to the position of the delay element that is closest in phase to the reference clock. In this particular example, the sum of the thermometer output is 4, indicating that the output I4 is closest in phase to the reference clock f_{REF}. This output will then be selected by the MUX and sent to the medium TDC. Once the output I4 has been determined to be the right delayed version that is closest in phase to the reference clock, the control input of the MUX will immediately be frozen.

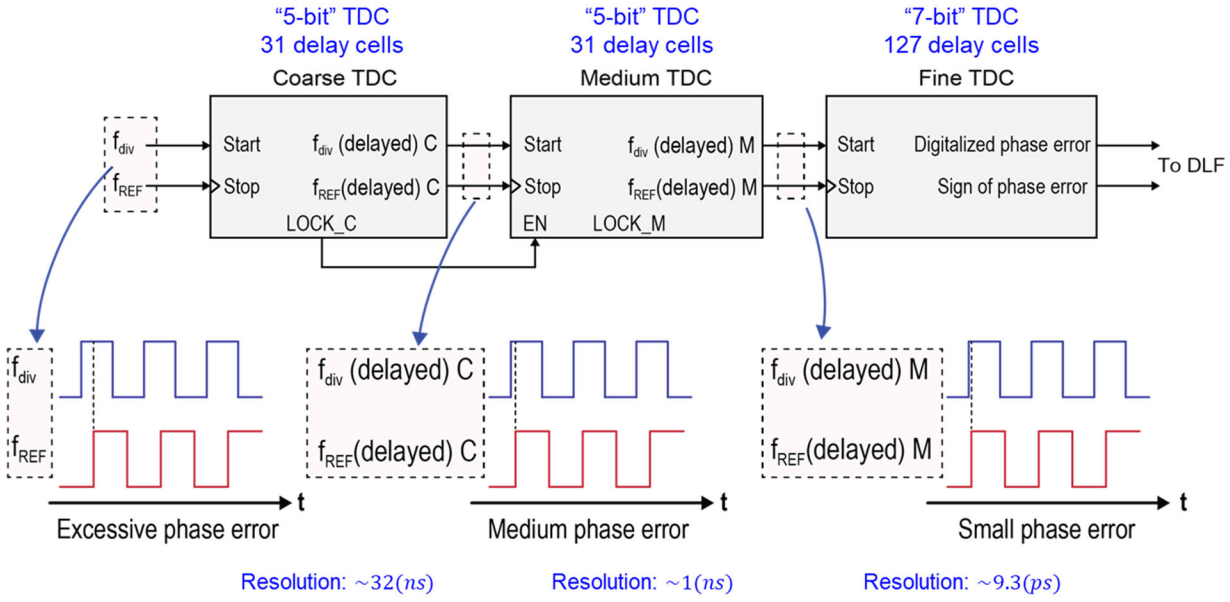


Figure 4.42: Connection between the coarse, medium, and fine TDCs and a diagram showing how the phases of f_{div} and f_{REF} are brought closer together for phase-error digitization by the fine TDC.

Once the LOCK_C pin from the coarse TDC is asserted, the medium TDC is now enabled and will continue the same operation to bring down the 32-ns phase error to even lower, only less than 1 ns and send it to the fine TDC. In order words, the main function of the two coarse and medium TDCs is to generate delayed versions of f_{div} (the divided frequency of the 2nd RA) and f_{REF} so that their phase error now falls within the range that the fine TDC is able to digitize and process. As a result, the frequency locking operation of the ADPLL is now being done on the delayed versions of the two clock signals, rather than their original versions.

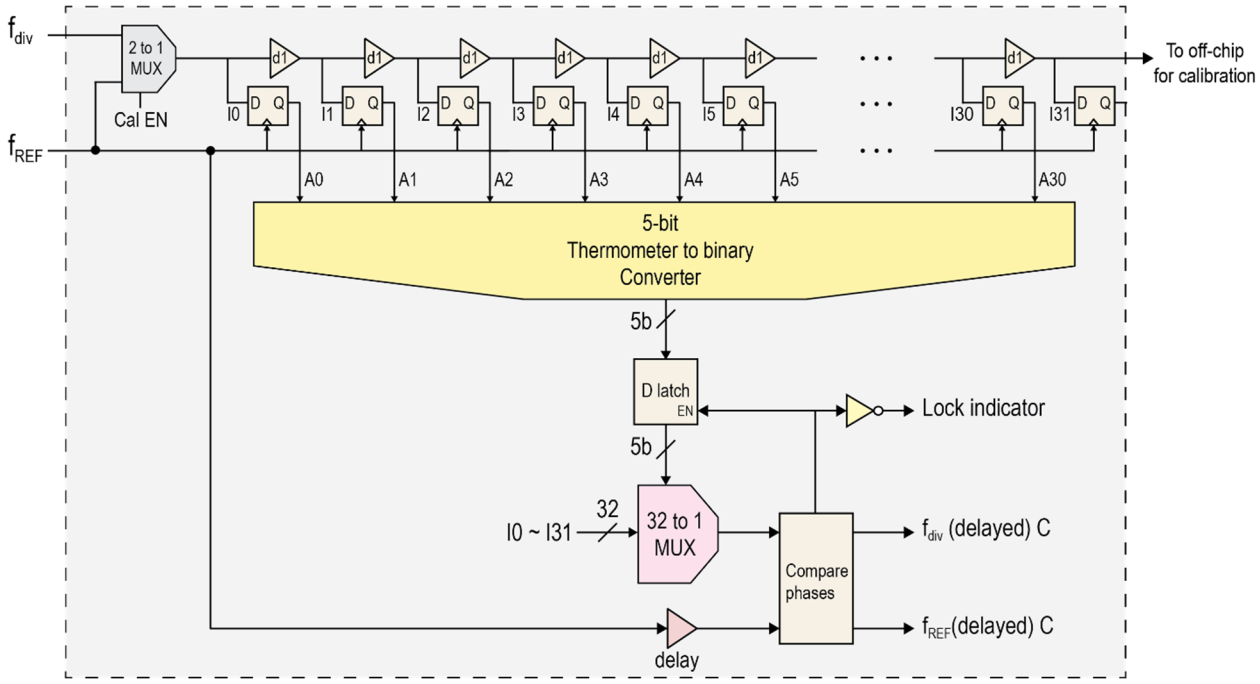


Figure 4.43: Simplified schematic of the coarse and medium TDCs.

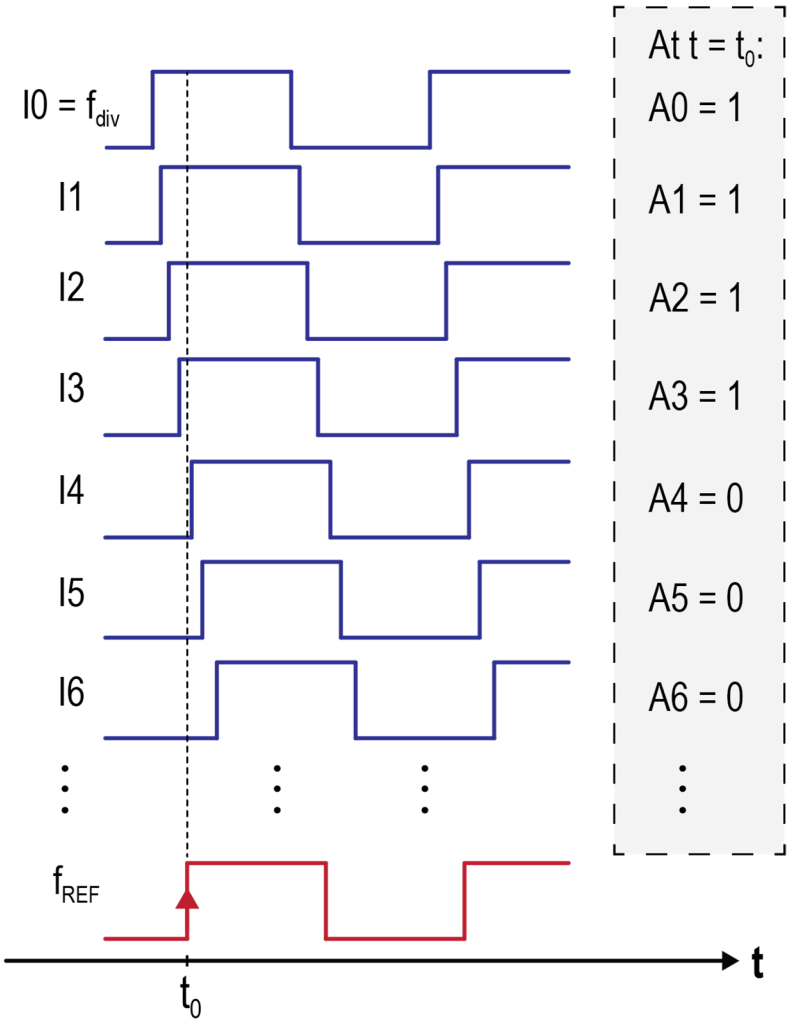


Figure 4.44: Timing diagram showing how the coarse TDC is able to pick the delayed version of f_{div} that is closest in phase to f_{REF}.

Fig. 4.45 shows a simulation of the operation of the coarse and medium TDCs to reduce the original phase error. Initially, the phase error is still excessive and the lock indicators of the coarse TDC and the medium TDC are still LOW, which means the phase lock has not been achieved. After approximately one reference clock cycle, the phase error at the output of the coarse TDC has now been brought down to less than 32 ns along with the coarse lock indicator being HIGH, enabling the operation of the medium TDC. Then, after approximately another clock cycle, the phase error at the output of the medium TDC is now less than 1 ns, along with its

respective lock indicator being HIGH, which means that the phase error has been “locked” down to less than 1 ns. Fig. 4.46 shows a magnified portion of the timing diagrams in Fig. 4.45.

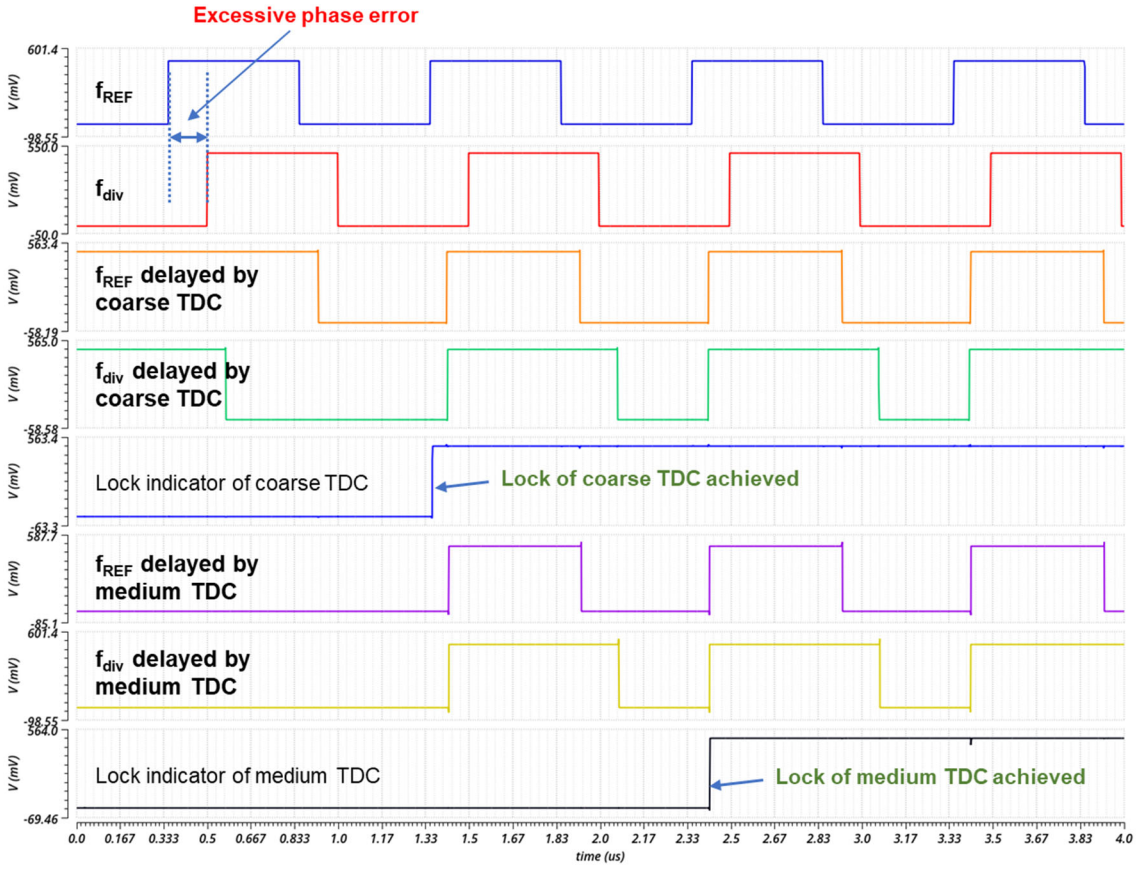


Figure 4.45: Simulation of the operation of the coarse TDC and medium TDC with regarding to bringing the phases of f_{div} and f_{REF} closer together for phase-error digitization by the fine TDC.

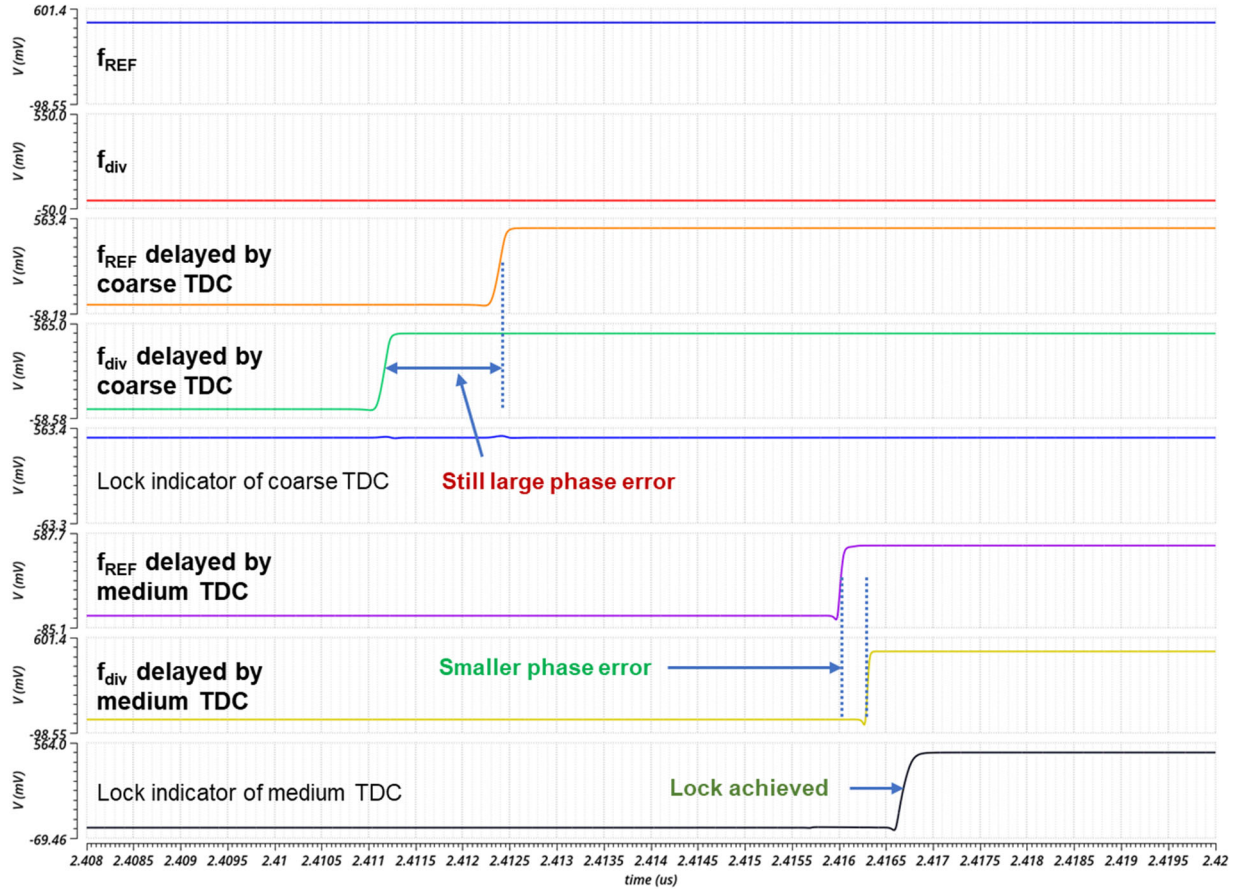


Figure 4.46: A magnified section of the simulation of the operation of the coarse TDC and medium TDC with regarding to bringing the phases of f_{div} and f_{REF} closer together for phase-error digitization by the fine TDC.

Fig. 4.47 shows the schematic of the fine TDC. The fine TDC is based on a Vernier configuration [55] where each delay element is identical and the delay difference is implemented based on the difference in the input capacitances of the D input and CLK input of each D flip flop. The fine TDC has 127 delay elements and is able to achieve a time resolution of ~9.3 ps of each element.

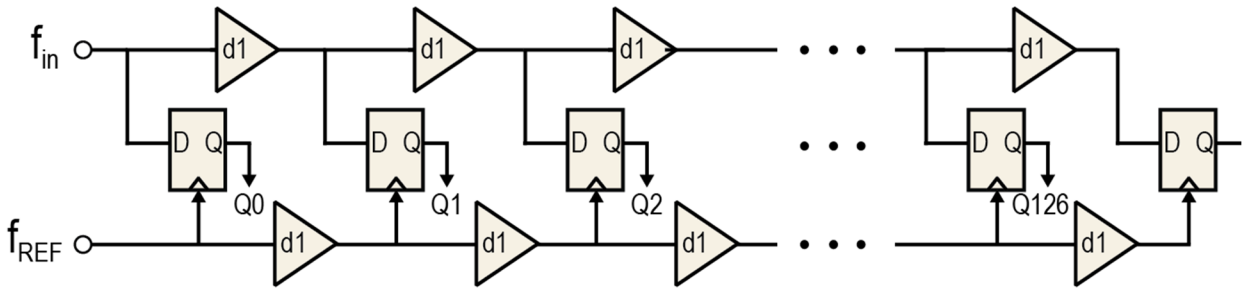


Figure 4.47: Schematic of the fine TDC.

Conventionally, a fine TDC can only digitize phase error in one direction [55], i.e. only when the phase error is positive. In this design, the overall fine TDC can digitize both positive and negative phase errors. Hence, the overall fine TDC structure is actually a combination of a fine TDC and its associated 7-bit thermometer-to-binary converter that handles the positive phase error, and another identical fine TDC and its 7-bit associated thermometer-to-binary converter that handles the negative phase error, as shown in Fig. 4.48. There is an adder at the output to sum up the two outputs of the two thermometer-to-binary converters. The adder has seven OR gates to prevent overflow from occurring, i.e. whenever the sum exceeds '1111111', it will simply be clamped at '1111111' and will not fluctuate to another lower value, which would potentially lead to an incorrect digitization of the phase error. A SIGN detector is also used to detect whether f_{div} leads f_{REF} or vice versa. If, for example, f_{div} leads f_{REF}, then the output of the top thermometer-to-binary converter will just be '0000000' whereas the output of the bottom thermometer-to-binary converter will be the digitized value of the phase error, and the output of the adder will simply take on this digitized phase error of f_{div} and f_{REF}, then the output of the SIGN detector will be '1' and vice versa. With the information of the adder output and the SIGN detector output, the phase error of the divided oscillation frequency of the 2nd RA f_{div} and the reference frequency f_{REF} of 1 MHz can be fully digitized and processed later.

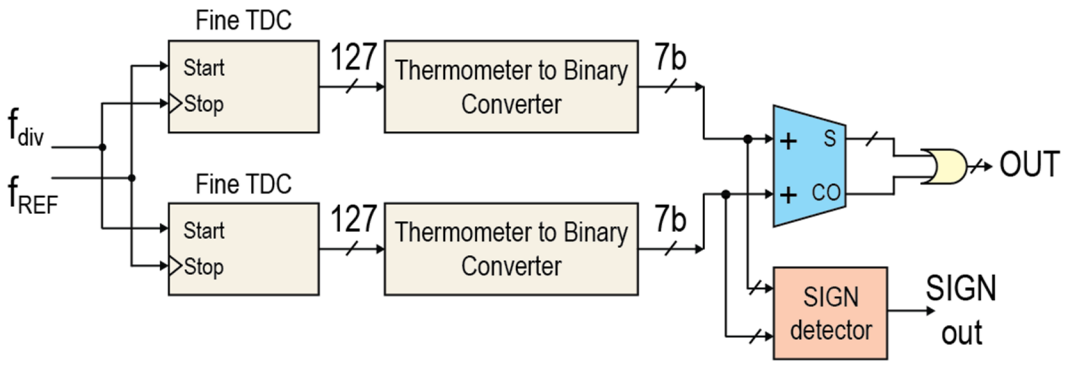


Figure 4.48: Block diagram of the overall fine TDC consisting of two fine TDCs and their associated thermometer-to-binary converters along with an adder and a SIGN detector.

In the architecture of the ADPLL, there is a lock detector to indicate when phase, and hence frequency, lock has been achieved. Fig. 4.49 shows the schematic of the lock detector. The 7-bit comparator compares the output of the fine TDC with a fixed threshold, that can be set by the off-chip FPGA. As soon as the fine TDC output is lower than this threshold, which indicates the phase error is close to zero, the lock detector generates a HIGH output at the next rising edge. Depending on how many successive HIGH values are generated, the FPGA will determine whether frequency lock has been achieved in order to power down the ADPLL operation accordingly. The FPGA will then disable the frequency retainer in order to freeze the instantaneous 10-bit word value to maintain the oscillation frequency of the 2nd RA at the corresponding desired value.

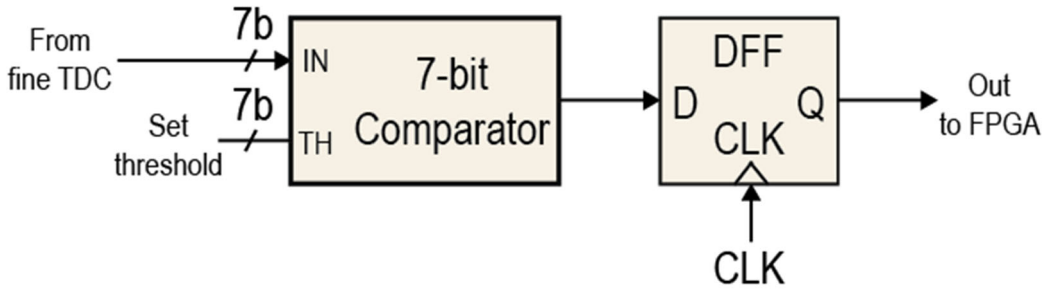


Figure 4.49: Schematic of the lock detector.

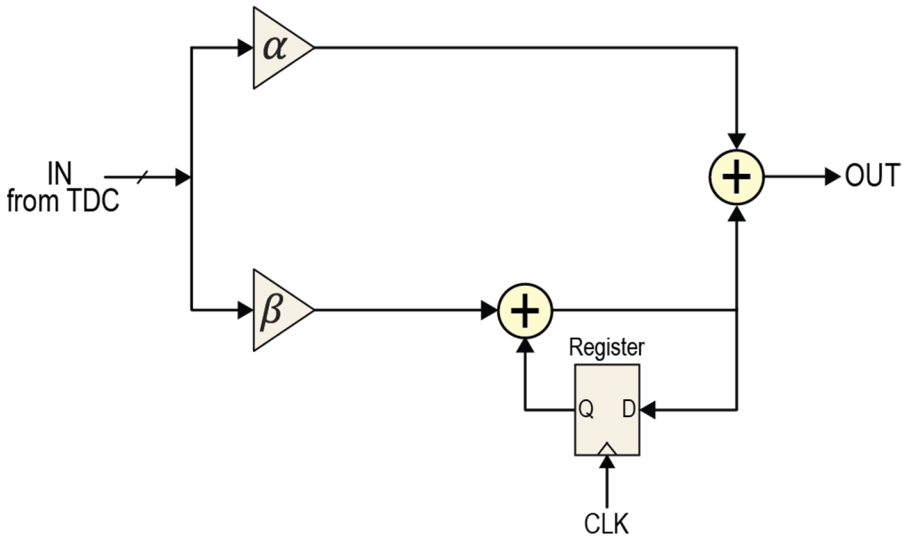


Figure 4.50: Conventional architecture of a DLF.

Conventionally, a digital loop filter (DLF) is implemented as shown in Fig. 4.50 [57]. In this architecture, the DLF only has adders and so is only able to properly deal with a positive phase error input. In addition, the adders do not have any logic to handle the situation where overflow occurs, leading to a potentially incorrect output. The design of the DLF in the ADPLL is improved significantly over such a conventional topology.

Fig. 4.51 shows the block diagram of the proposed DLF. As usual, the filter consists of two paths: the proportional path and the integration path. In order to ease the design, each coefficient factor α and β is implemented using a bit shifter [57]. As a result, shifting one bit to the right is equivalent to dividing the digital value by 2, and so on. Since the input phase error only has 7 bits, additional 3 bits of LOW values are added to the overall 10-bit input of the DLF to allow for bit shifting to the left. In addition to adders, subtractors are also incorporated into the design as shown in the figure. The two MUX's will pick and process the output of either the adders or the subtractors, based on the value of the SIGN input. Hence, both positive and negative phase error can be handled and processed properly. In order to address the issue of

overflow of an adder or underflow of a subtractor, additional logic gates are added as shown in the figure. For example, for a 10-bit adder, if the value of the sum (S) exceeds 10 bits, then the carry out (CO) will be 1; as a result, with ten OR gates connecting S and CO, the total output will simply be capped at '1111111111' rather than potentially dropping down to a very low inaccurate value.

The behavior of the improved DLF is analogous to that of the charge-pump in the analog PLL counterpart, as shown in Fig. 4.52. For the charge pump, the positive phase error will turn on the UP switch, leading to more current flowing into the capacitor, increasing the output voltage. When this output reaches VDD (similar to an overflow event in the DLF), it will simply be clamped at this VDD value and will not go any higher (similar to the output of an adder in the DLF being constant at '1111111111'). Conversely, when the phase error is negative, the DOWN switch will be closed, discharging the capacitor and reducing the output voltage, which will be clamped at 0 V whenever underflow occurs.

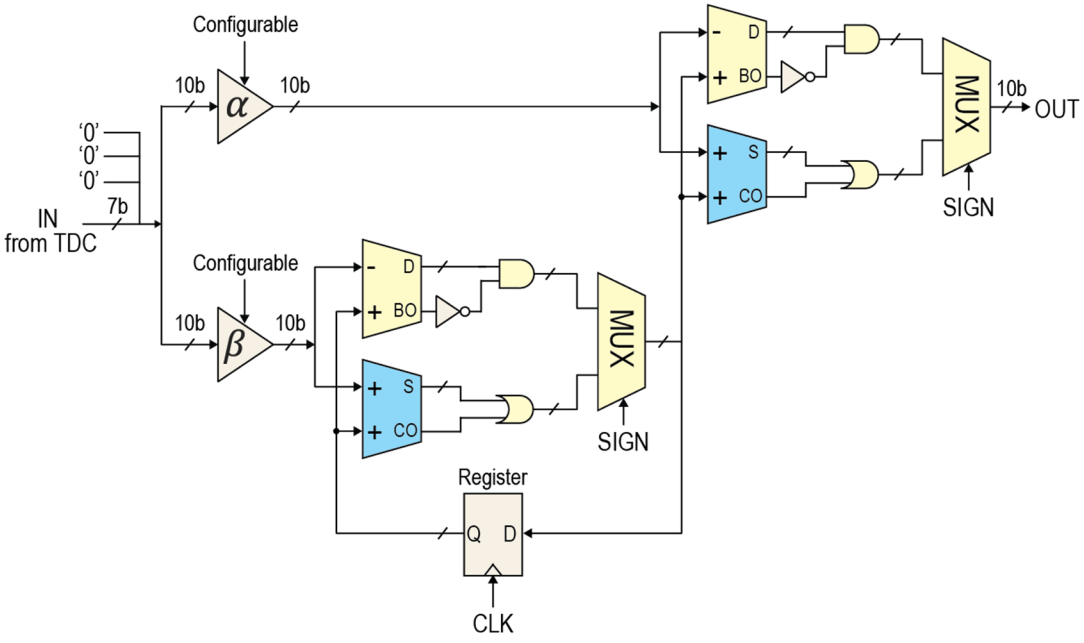


Figure 4.51: Block diagram of the digital loop filter (DLF).

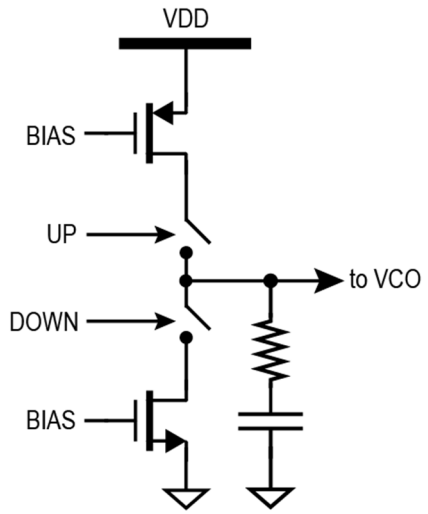


Figure 4.52: Block diagram of the connection between the fine TDC's and the thermometer-to-binary converters.

Fig. 4.53 shows the overall capacitor bank that controls the operation frequency of the 2nd RA. A 7-bit fine capacitor bank along with a "supplementary" medium capacitor array make up a 10-bit switched capacitor system in total. Another coarse 4-bit capacitor array is also implemented to flexibly control the center frequency of the 2nd RA to a different frequency range, depending on the target application.

Fig. 4.54 shows the schematic of each unit capacitor in the 7-bit fine capacitor bank of the 2nd RA [58]. The four capacitors are all inter-digitated capacitors implemented using lower metal layers M4 and M5 to obtain low capacitance. Each unit capacitor is able to achieve a capacitance difference of only 5.4 aF between the ON and the OFF states of the control signal, as given by:

$$\Delta C = C_{OFF} - C_{ON} = \frac{\Delta_F^2}{4C_F + 2\Delta_F} \tag{4.26}$$

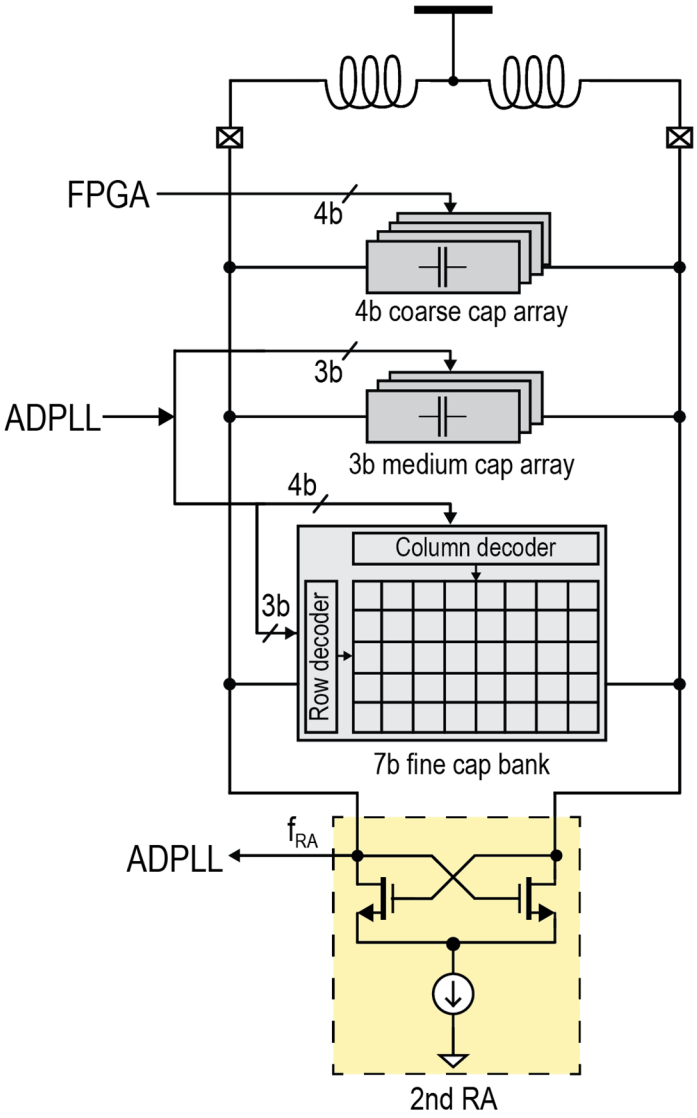


Figure 4.53: Schematic of the overall capacitor bank of the 2nd RA.

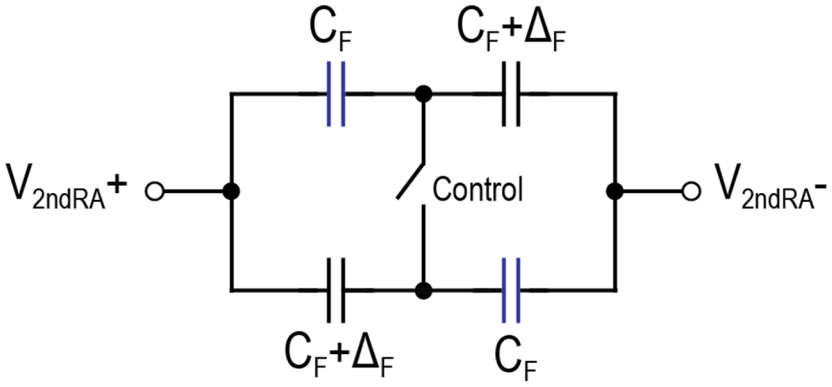


Figure 4.54: Schematic of each unit capacitor in the 7-bit capacitor bank of the 2nd RA, reproduced from [58].

Fig. 4.55 shows the schematic and the arrangement of the unit capacitors to implement the 7-bit fine capacitor bank of the 2nd RA. To achieve good matching, arrays of dummy unit capacitors are arranged around the perimeter of the capacitor bank; the dummy capacitors are not connected to the total capacitance of the bank. Fig. 4.56 shows the layout of the capacitor bank along with its dimensions.

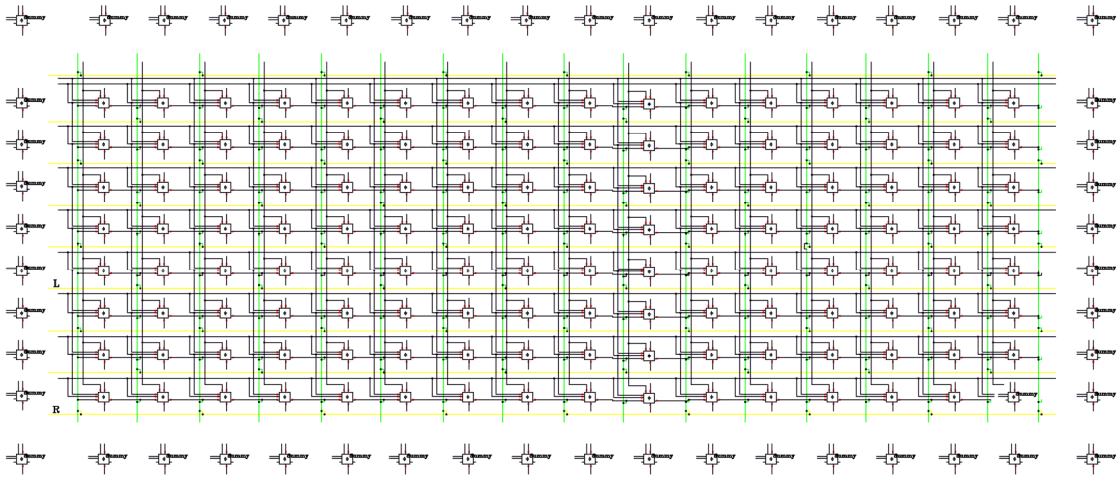


Figure 4.55: Schematic and arrangement of the unit capacitors to implement the 7-bit fine capacitor bank.

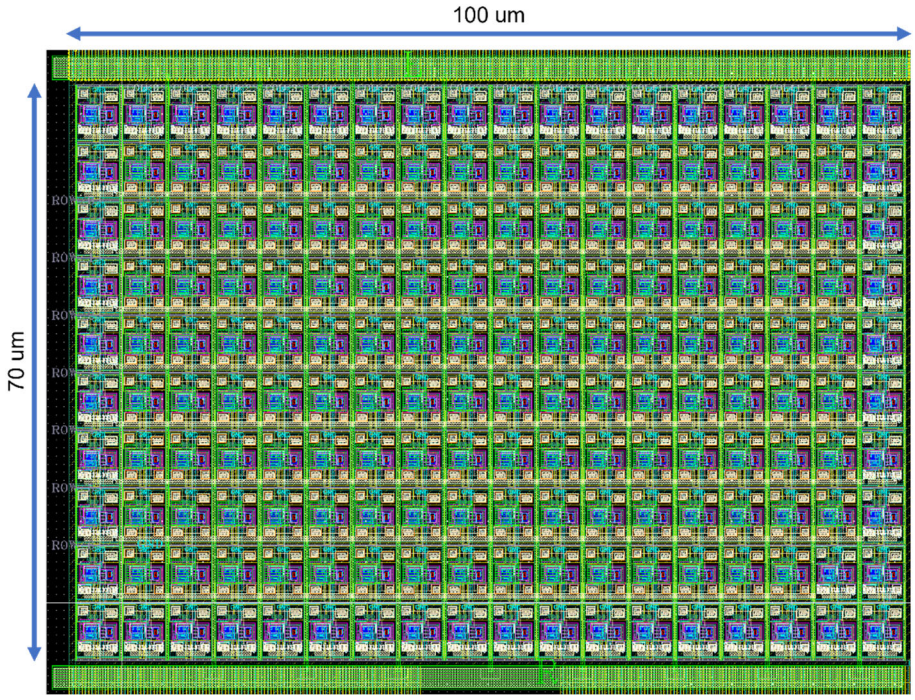


Figure 4.56: Layout of the 7-bit fine capacitor bank.

Figure 4.57 shows the 3-bit "supplementary" medium capacitor arrays. Each capacitor cell is identical with each other and is configured in a binary code for good matching. The capacitance difference between the ON and OFF states of each capacitor cell is chosen to be slightly lower than the total capacitance difference of the previous 7-bit fine capacitor bank of the 2nd RA, in order to ensure no frequency value is missing in the frequency range that the center frequency of the 2nd RA is allowed to take on. Together, the 7-bit fine capacitor bank and the 3-bit supplementary medium capacitor array extend the number of bits to 10 with a fine resolution of 5.4 aF. Fig. 4.58 shows the simulated capacitance of the combination of the 7-bit capacitor bank and the 3-bit supplementary capacitor array of the 2nd RA at a frequency of 2.44 GHz as a function of the controlling 10-bit word. It can be seen that monotonicity is ensured and there is no gap missing in the overall capacitance range of the 10-bit combination.

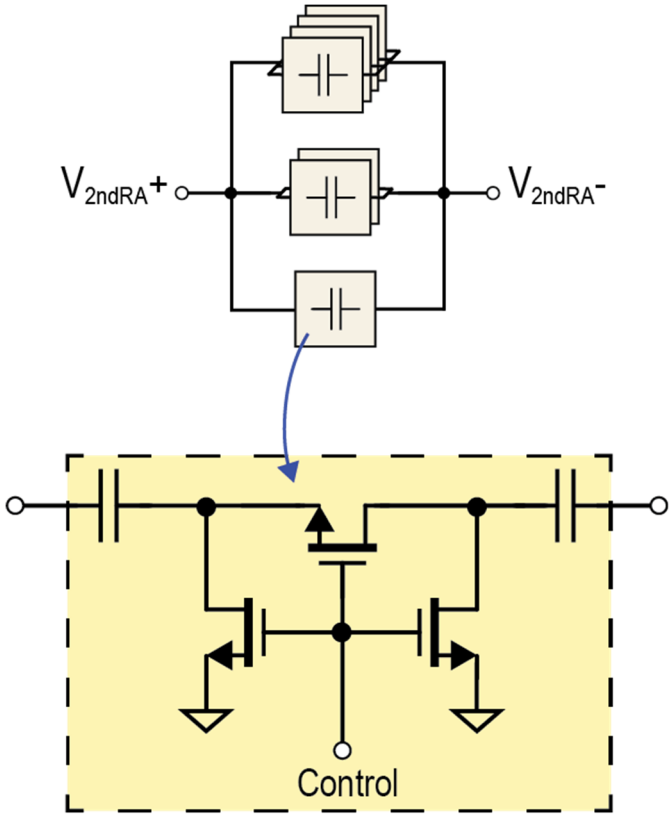


Figure 4.57: Schematic of the 3-bit supplementary medium capacitor array for the 7-bit fine capacitor bank of the 2nd RA.

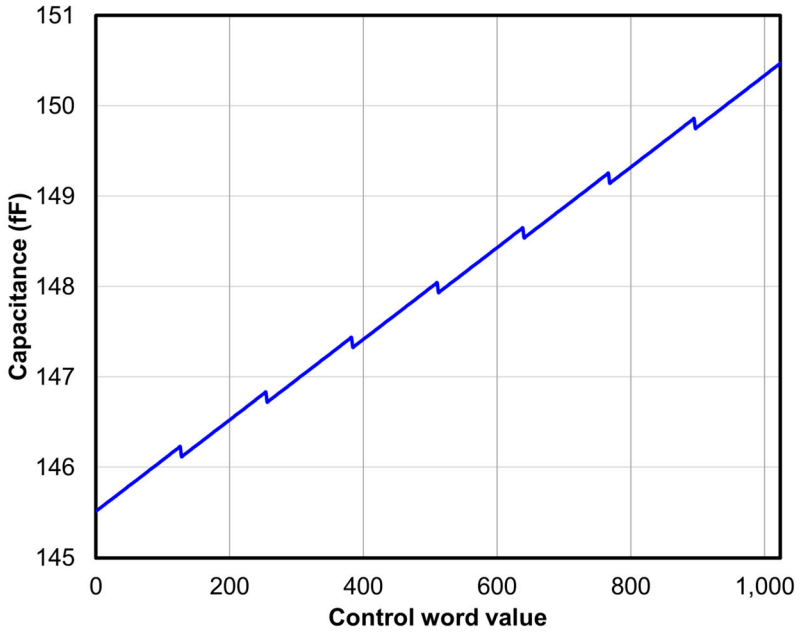


Figure 4.58: Simulation of the total capacitance of the 7-bit fine capacitor bank and the 3-bit supplementary capacitor array, showing consistent monotonicity, as a function of the control word value.

Fig. 4.59 is the model of the ADPLL along with all of its parameters. The open-loop transfer function of the ADPLL can be expressed as:

$$H(s) = \frac{T_{REF}}{2\pi\Delta_{TDC}} \times \frac{\left(s + \frac{1}{RC}\right)}{s} R \times \frac{K_{DCO}}{s} \times \frac{1}{N} = \frac{\frac{T_{REF}RK_{DCO}}{2\pi\Delta_{TDC}N}\boldsymbol{s} + \frac{T_{REF}K_{DCO}}{2\pi\Delta_{TDC}NC}}{\boldsymbol{s^2}} \tag{4.27}$$

Note that the equivalent values of the resistor R and capacitor C in the charge-pump PLL counterpart can be found from α and β by bi-linear transformation, as discussed in [57]. The open-loop transfer function is a system with two poles at the origin and one zero at a certain frequency away. The Bode plot for the transfer function is shown in Fig. 4.60, indicating a phase margin of approximately 60°. The phase margin can be tuned by the off-chip FPGA via the control of the α and β values, allowing for the flexible control of the lock time.

Parameter	Value
T_{REF}	$1e-6$ (s)
Δ_{TDC}	$9.3e-12$ (s)
α	2^{-1} (tunable)
β	2^{-2} (tunable)
R	0.625 (Ω)*
C	$4e-6$ (F)*
K_{DCO}	$2\pi 24e3$ (rad/LSB)
N	2440 (tunable)

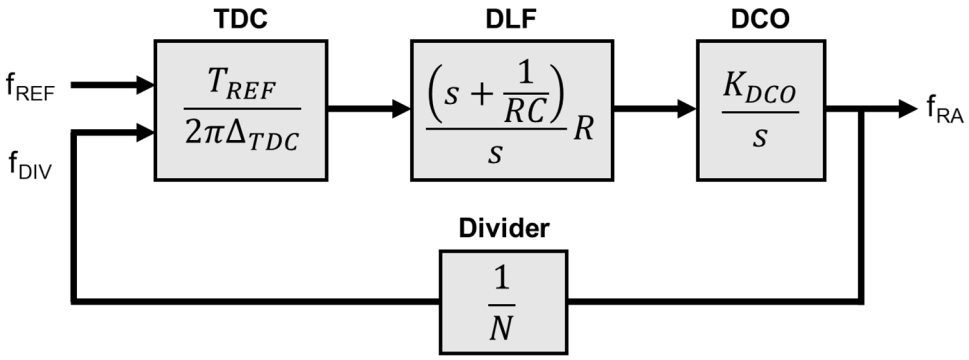


Figure 4.59: Model of the ADPLL including all the values of its parameters.

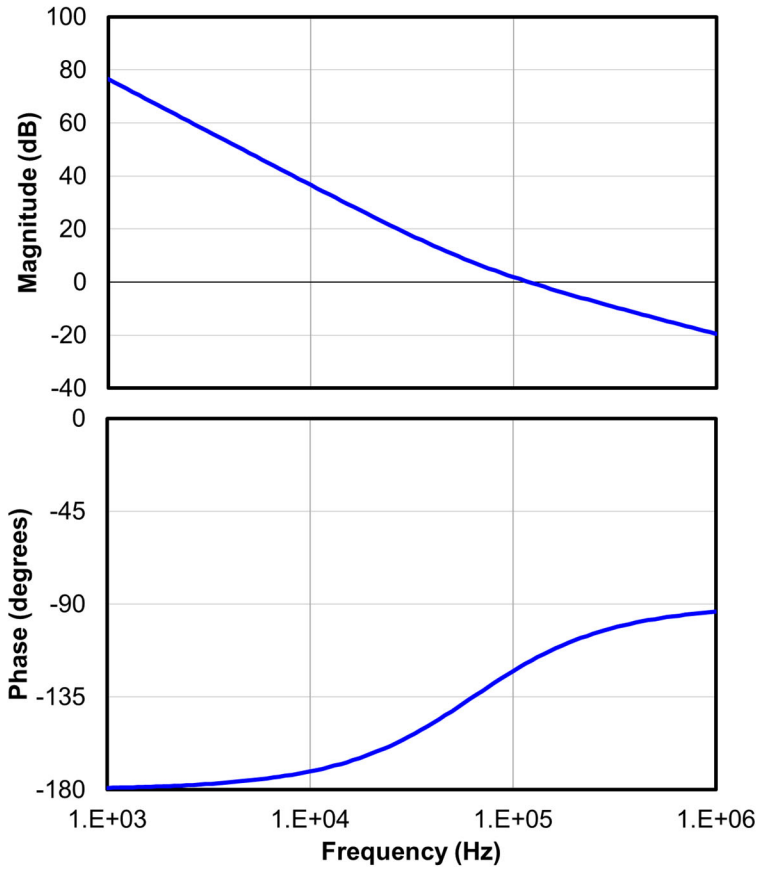


Figure 4.60: Bode plot of the open-loop transfer function showing a phase margin of ~60°.

An example of simulation of the frequency locking of the ADPLL is shown in Fig. 4.61. Here, the values of α and β are both $\frac{1}{4}$, i.e a shifting of 2 bits to the right is done both on the proportional path and the integrated path. The target frequency is chosen to be 2445 MHz. It can be seen that frequency locking is achieved at around 30~40 µs, depending on how the off-chip FPGA determines when it receives a significant number of HIGH values from the lock detector's output in order to power down the ADPLL and freeze the frequency. As expected, when the phase error is close to zero, the output of the TDC approaches zero whereas the output of the DLP approaches a certain value that sets the frequency of the 2nd RA to the target one.

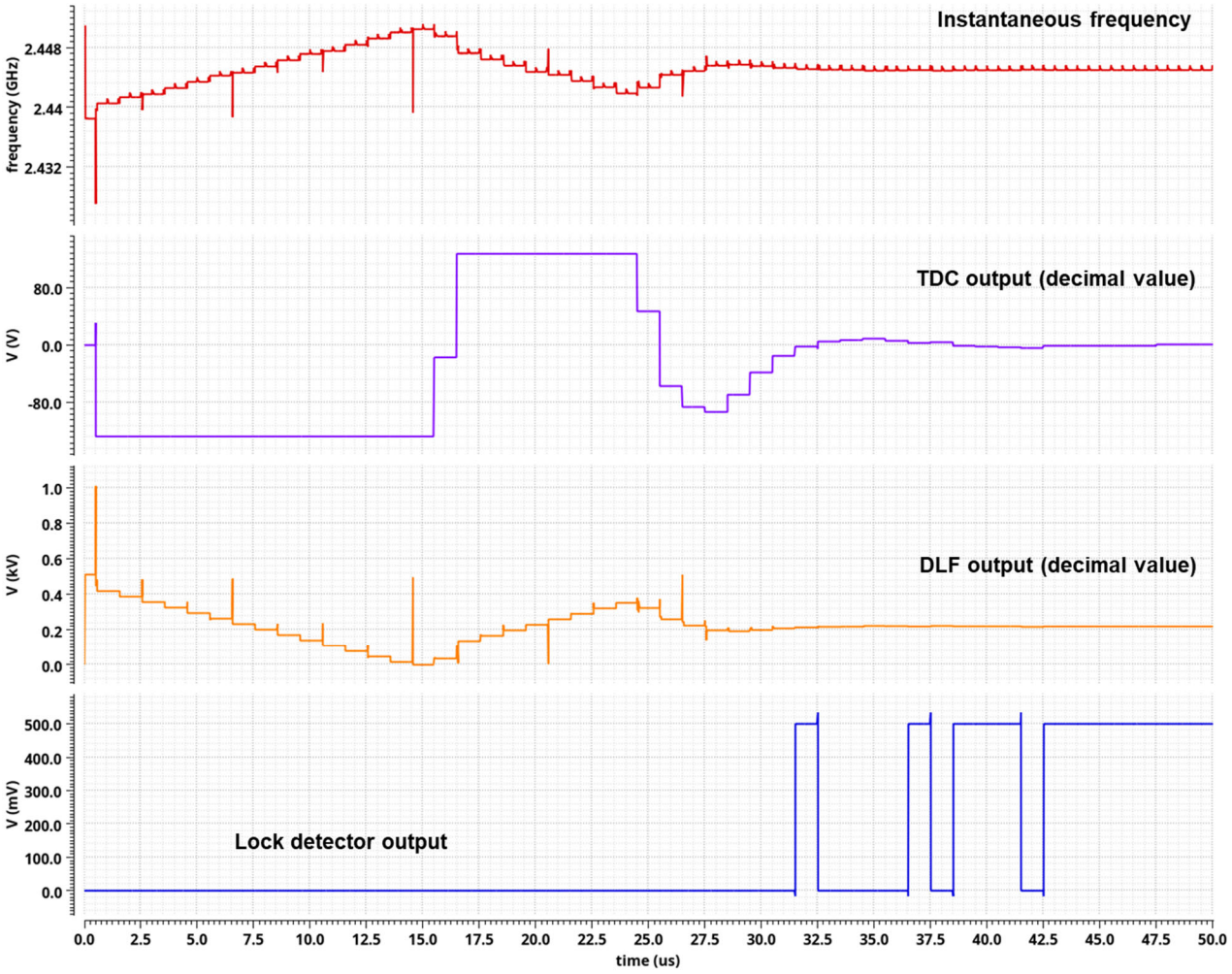


Figure 4.61: Simulation of the locking operation of the ADPLL for a target frequency of 2.445 GHz with $\alpha = \beta = 1/4$.

V – Summary of Receiver Performance and Conclusion

The proposed receiver is implemented in a 65nm CMOS technology. The layout of the overall chip is shown in Fig. 4.62. The total chip area is 1mm x 1mm. Fig. 4.63 shows the breakdown of the power consumption of the receiver. It can be seen that during normal operation, the DRAs and the ED consume the majority of the total power. During frequency calibration, the power consumption of the ALL and ADPLL is significant; however, since they will only be powered on intermittently and are therefore duty-cycled, their average power consumption is insignificant compared to the other blocks that are active during normal operation. At a VDD of 0.5 V, the active power consumption of the receiver is only around 30 µA.

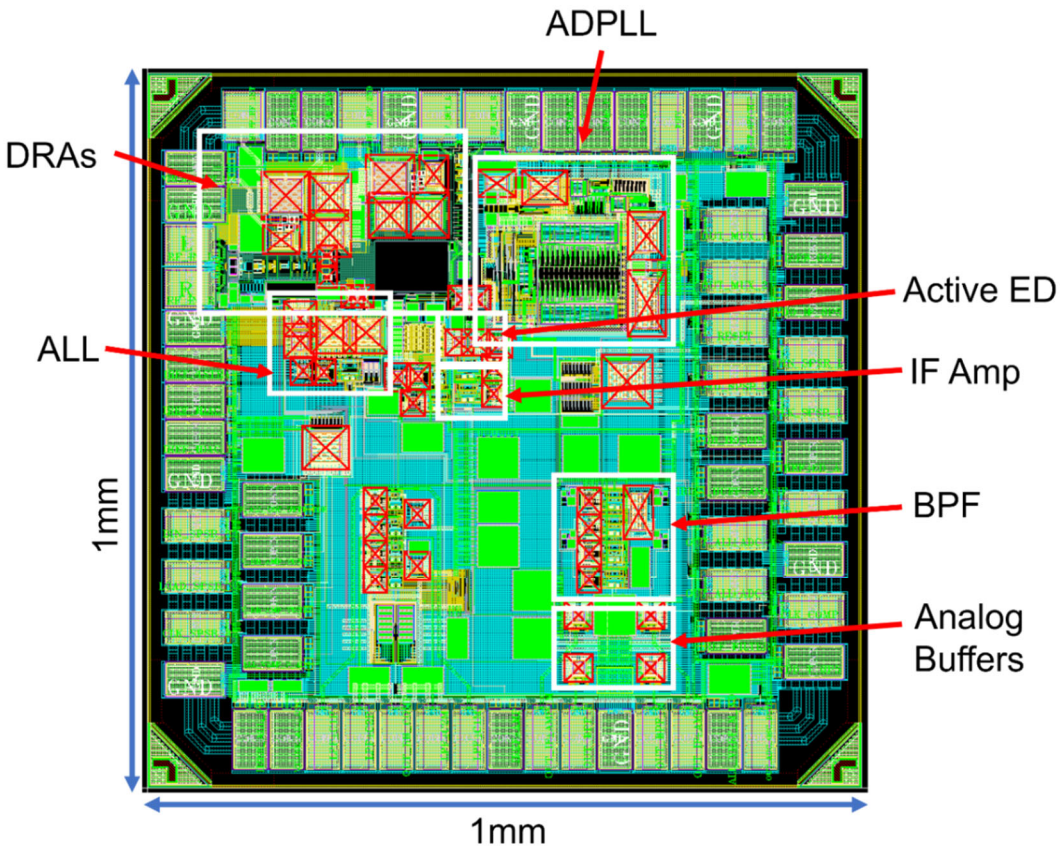


Figure 4.62: Overall layout of the proposed receiver.

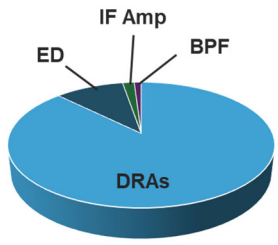
Active blocks during normal operation

Block	I_{DC} (µA)
DRAs	52
ED	5.9
IF Amp	1
BPF	0.6
Total	**59.5**

Blocks used for calibration

Block	I_{DC} (µA)
ALL	5.8
ADPLL	189

Parameter	Value
Process	65nm CMOS
VDD	0.5 V
Chip area	1mmx1mm



Power breakdown

Figure 4.63: Summary of the breakdown of the power consumption of the proposed receiver showing an average ultra-low power consumption of only 30 µW in normal operation.

Table 4.4 is a comparison of the proposed receiver with other BLE/WiFi-compatible receivers in the literature. It can be seen that the receiver achieves a state-of-the-art sensitivity with an ultra-low power consumption and especially the highest energy efficiency.

Table 4.4: Comparison with other BLE/WiFi-compatible receivers in the literature.

Reference	WiFi standard	Modulation	Sensitivity (dBm)	Pdc (µW)	Energy eff. (bits/µJ)	Chip prototype
[59] JSSC 2018	802.11g/n (2.4GHz)	OOK	-72	95	659	Yes
[60] TMTT 2019	802.11ba (5.8GHz)	OOK	-83	220	285	Yes
[51] ISSCC 2020	802.11b (2.4GHz)	OOK	-42.5	28	2286	Yes
[52] MobiCom 2021	802.11ax (2.4GHz)	64-QAM	-55	365	3248	No
This work	**802.11ax (2.4GHz)**	**16-QAM**	**-80***	**30***	**25000***	**Yes**

*Simulation results

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Chapter 4, in part, contains unpublished material coauthored with Manideep Dunna, Shih-Kai Kuo, Dinesh Bharadia, and Patrick Mercier. The dissertation author was the primary author of this chapter.

CHAPTER 5

Summary and Future Work

I – Summary of the Dissertation

In summary, an RA operating in the nonlinear condition with a high gain, a narrow bandwidth, and a compressive third-order nonlinearity in response to a CW input can exhibit an interesting phenomenon where the in-band noise floor is being suppressed, effectively leading to an augmentation of the output CNR. Chapter 2 has delved into the analysis of such a phenomenon and provided simulation and measurement results to demonstrate the existence of it. The chapter has also discussed a potential promising application as a CW-tone detector in an EMT device.

For ultra-low power receivers with a simple modulation such as OOK that employ an ED, it has been shown that the more gain there is prior to the ED, the better the sensitivity. An RA with an inferior NF of 30 dB but with a high gain of 60 dB can still outperform an LNA with an ideal NF of 0 dB but a lower gain of 20 dB. As a result, a state-of-the-art OOK receiver operating at 2.4 GHz based on a dual RA structure and a differential passive ED has been presented in Chapter 3 with a sensitivity of -101 dBm at a data rate of 5 kbps while consuming only 112 μW of power with an impressive SIR of -28 dB at an offset frequency of 3 MHz.

Lastly, Chapter 4 has presented yet another state-of-the-art ultra-low power receiver based on an active ED with the ability to demodulate signal coherently and be compatible with BLE and/or WiFi standards. Thanks to the clever use of an external CW tone that is sent along with the data from the transmitter, the ED can now down-convert the signal onto a non-zero, IF frequency for further coherent processing. In addition, the dual RA structure in front of the ED

again provides a high gain to help alleviate the noise contribution associated with the ED and to provide a narrow bandwidth for interference resiliency. Simulation results show that the receiver can achieve an excellent sensitivity of -80 dBm for 16QAM modulation while consuming only 30 µW. The receiver exhibits the highest energy efficiency compared with other ultra-low power, state-of-the-art BLE/WiFi-compatible works.

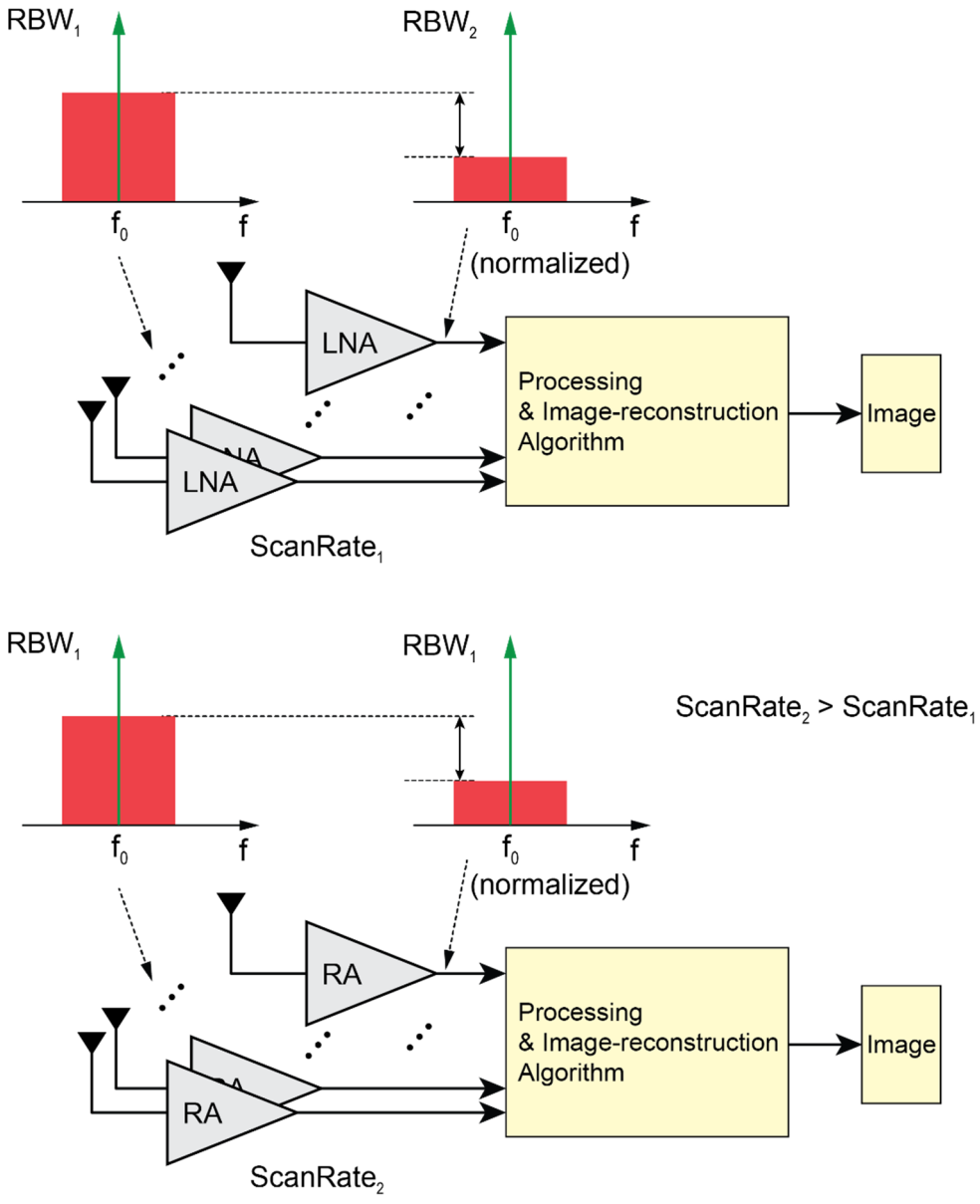

Figure 5.1: Future demonstration of the RA employed in an EMT device to obtain a high-quality reconstructed image of an object while maintaining a high scan rate, as opposed to a conventional LNA.

II – Future Work

As discussed in Chapter 2, future work on the application of noise suppression of an RA in an EMT device can be conducted as follows: an array of RAs can be used to replace conventional amplifiers, e.g. LNAs, to implement the detectors in an EMT device. Fig. 5.1 illustrates such a future demonstration. In the linear operation condition, the RA will help reduce the out-of-band noise, leading to a higher integrated SNR due to its inherent narrow bandwidth. Then in the nonlinear operation, the RA can be tuned to adjust the onset of noise suppression, at which point the in-band noise floor is pushed down, further improving the SNR. Hence, the image quality can also be improved. Alternatively, if the image quality is maintained, i.e. if the RBW needs to be increased to push back the noise floor to the same level as without noise suppression, then the scan rate can be sped up accordingly thanks to the improved SNR.

For the non-coherent, OOK receiver presented in Chapter 3, to increase energy efficiency further, one can potentially use a signal with a higher data rate while maintaining essentially the same power consumption. A higher data rate will entail a wider bandwidth of the 2^{nd} RA; as a result, the gain of the overall DRAs might need to be reduced accordingly. Care should then be taken such that the various noises stemming from the ED can still be alleviated with a smaller amount of gain.

Apart from the potential use of a higher-data-rate radio receiver, the design can also be extended into a low data-rate wakeup radio receiver (WuRX). For example, a comparator and a correlator can be incorporated into the overall architecture, at essentially no extra power consumption [61]. Fig. 5.2 depicts such an extended application of the receiver. Since the data rate of a typical WuRX is only on the order of a few hundreds of b/s or lower, the 3-dB bandwidth of the DRAs can even be further narrowed down. As a result, the interference

resiliency can potentially be improved. The lower data rate can also help achieve a better sensitivity level. The only caveat is that due to the narrow bandwidth of the DRAs, the center frequency might fluctuate due to process, voltage, and temperature (PVT). Therefore, for robustness, a PLL can then be incorporated into the receiver that connects with the output of the 2nd RA to sporadically calibrate the center frequency prior to the WuRX operation. This concept can also be adopted from Chapter 4 where an ADPLL and an ALL work in tandem to perform frequency calibration intermittently. The 1st RA, however, will not need rigorous frequency calibration thanks to its much wider bandwidth compared to that of the 2nd RA. Although a PLL working at GHz frequencies can potentially add more power to the overall power consumption of the design, the PLL will not be powered on continuously but will be duty-cycled such that its average power consumption will be significantly reduced. Similar works to calibrate center frequency has been done in [1, 4, 37, 38].

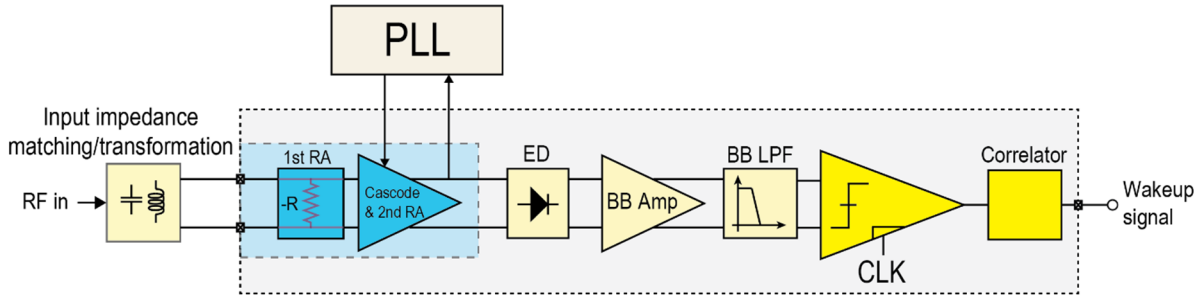

Figure 5.2: Example of incorporating a comparator and a correlator into the existing design presented in Chapter 3 at essentially no additional power cost, to extend it into a low data-rate wakeup receiver.

According to the discussion presented in Chapter 4, the image-noise issue of the BLE/WiFi-compatible receiver might worsen the SNR, potentially leading to a degradation of 6 dB or more on the sensitivity, depending on the filtering profile of the DRAs. In fact, there are

several ways to tackle this issue, e.g. adding additional identical subcarriers on both sides of the pilot tones as shown in Fig. 5.3. These identical subcarriers will be down-converted to the same IF frequency and will constructively add up, leading to a higher overall SNR.

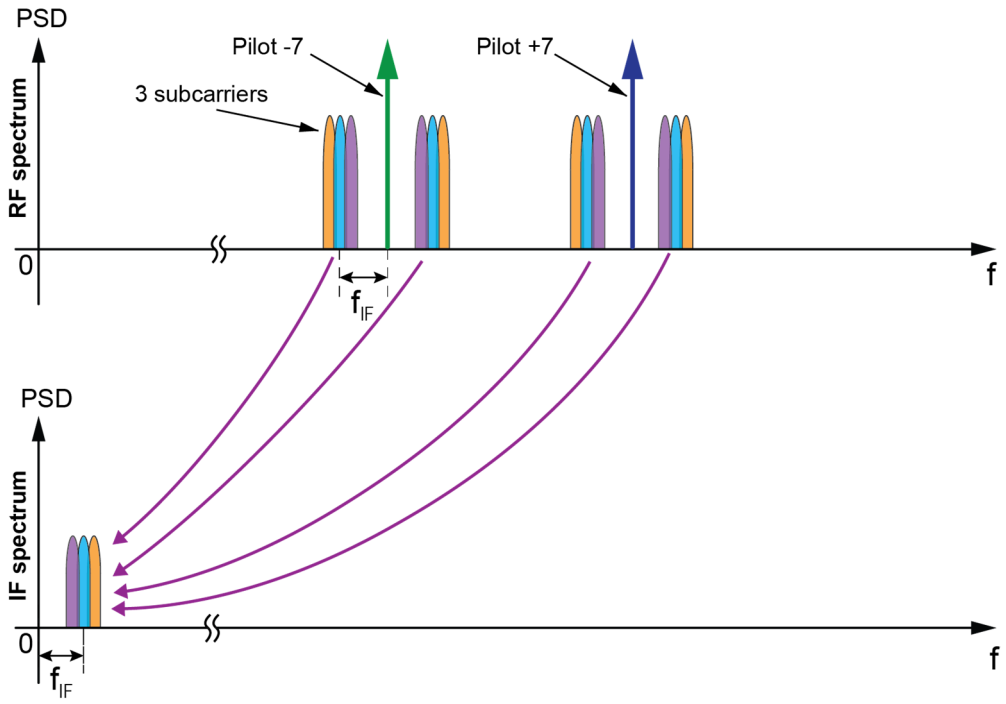

Figure 5.3: Example of placing three identical subcarriers on both sides of the pilot tones to increase the overall SNR at the IF spectrum and alleviate the image-noise issue.

In addition, the BLE/WiFi-compatible receiver can be further extended to be fully compatible with any BLE/WiFi standard and not just 802.11ax. To this end, in terms of WiFi, the original 26 subcarriers in a conventional spectrum can be deployed along with an external LO tone instead of just 3 subcarriers and 2 pilot tones. This way, the ED will perform the squaring operation which will multiple the 26 subcarriers with the added LO tone, as shown in Fig. 5.4. With this scheme, the data throughput and energy efficiency can then be further enhanced to almost 9 times higher. Care should be taken such that there will be no overlapping between the desired down-converted 26 subcarriers due to the LO tone and the mixing of these subcarriers

with each other that extends from DC. In addition, since the 26 subcarriers require a higher SNR for proper demodulation, the gain of the RA might have to be reduced in order to improve the IIP3 accordingly to extend the dynamic range of the receiver.

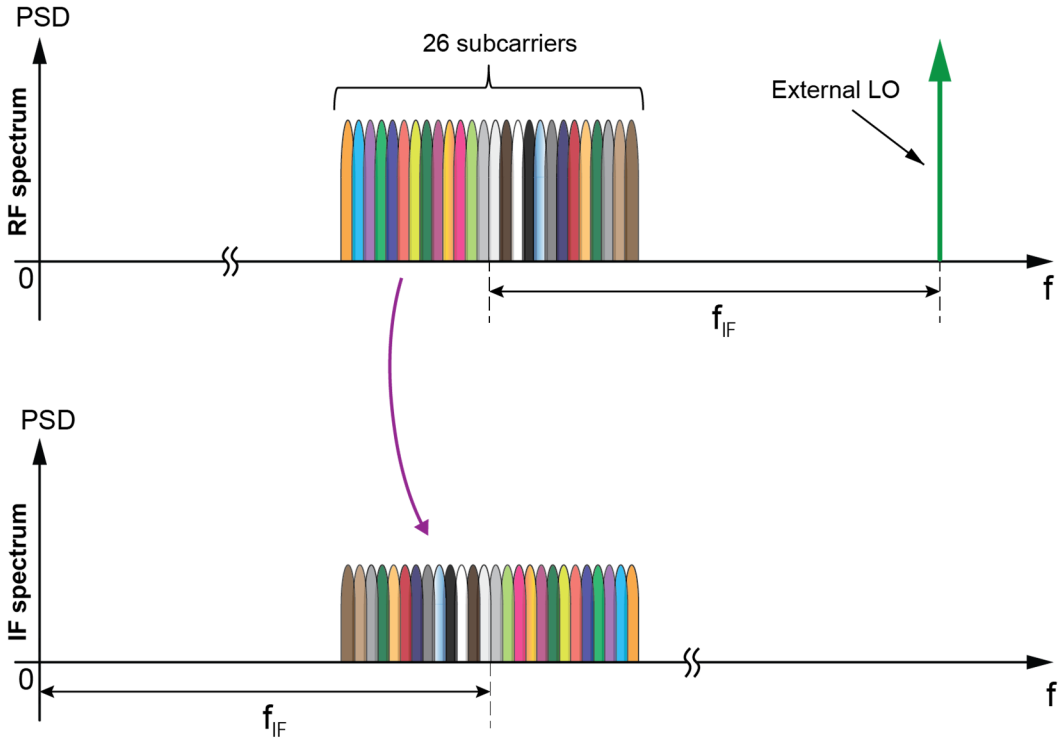

Figure 5.4: Example of deployment of 26 subcarriers in a conventional WiFi standard to extend the data throughput and energy efficiency of the receiver presented in Chapter 4.

All in all, there are definitely areas in which the works presented in this dissertation can be further improved and extended to achieve better performance, to be more robust, more versatile, and cover more applications. The RA with its high gain, narrow bandwidth, relatively low noise and low power consumption will still be an attractive candidate to realize ultra-low power, narrow-band, and high-performance integrated receiver solutions.

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