

**UCLA**

**UCLA Electronic Theses and Dissertations**

**Title**

Noise in Large-Signal, Time-Varying RF CMOS Circuits: Theory & Design

**Permalink**

<https://escholarship.org/uc/item/6tc6t9z2>

**Author**

Murphy, David Patrick

**Publication Date**

2012

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA  
Los Angeles

**Noise in Large-Signal, Time-Varying RF CMOS  
Circuits: Theory & Design**

A dissertation submitted in partial satisfaction  
of the requirements for the degree  
Doctor of Philosophy in Electrical Engineering

by

**David Patrick Murphy**

2012

© Copyright by  
David Patrick Murphy  
2012

ABSTRACT OF THE DISSERTATION

# Noise in Large-Signal, Time-Varying RF CMOS Circuits: Theory & Design

by

**David Patrick Murphy**

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2012

Professor Asad A. Abidi, Co-chair

Professor Mau-Chung Frank Chang, Co-chair

RF CMOS design is now a mature field and CMOS radio transceivers have become standard in most consumer wireless devices. Like any wireless RF design, at the heart of the endeavor is the requirement to frequency translate signals between baseband and RF with minimal introduction of noise and distortion. This translation is generally accomplished using time-varying, strongly nonlinear circuits, whose operation and noise performance cannot be understood using standard LTI circuit analysis techniques. This work seeks to address some of the design and analysis challenges posed by a variety of these non-linear, time-varying CMOS RF circuits, specifically in the context of low noise design.

First, a new wideband receiver architecture is proposed and analyzed. Using two separate passive-mixer-based down-conversion paths, noise cancelling is enabled, but voltage gain is avoided at unwanted blocker frequencies. This approach significantly relaxes the trade-off between noise, out-of-band linearity and wideband operation.

Second, using a phasor-based analysis method, new theoretical results relating to noise mechanisms in  $LC$  oscillators are described. Amplitude noise and  $Q$ -degradation is quantified for the first time, while the analysis method is also used to re-derive a fundamental limit to the achievable phase noise of any  $LC$  oscillator.

Finally, a low-noise, wideband PLL is described that is suitable for emerging mm-wave

standards. This design demonstrates that CMOS technology is capable of delivering a high-performance wideband VCO, even at mm-wave frequencies.

The dissertation of David Patrick Murphy is approved.

---

Songwu Lu

---

Sudhakar Pamarti

---

Hooman Darabi

---

Mau-Chung Frank Chang, Committee Co-chair

---

Asad A. Abidi, Committee Co-chair

University of California, Los Angeles

2012

# TABLE OF CONTENTS

<b>1</b>	<b>Thesis Overview</b>	<b>1</b>
<b>2</b>	<b>A Blocker-Tolerant Noise-Cancelling Receiver</b>	<b>4</b>
2.1	Introduction	4
2.2	Prior Art: Blocker-Tolerant Receivers	7
2.3	Proposed Noise-Cancelling Receiver	9
2.3.1	Noise-Cancelling Theory	9
2.3.2	The Frequency-Translational Noise-Cancelling Receiver	10
2.4	Linearity Bottleneck: The Class-AB Transconductance	12
2.5	Oversampling Mixers	16
2.6	Simplified Noise Analysis	19
2.7	Circuit Design	23
2.7.1	Receiver Topology	23
2.7.2	Multiphase Clock Generation	24
2.7.3	Baseband TIAs	28
2.8	Measurement Results	29
2.8.1	Noise Figure	29
2.8.2	Noise Figure Optimization	31
2.8.3	Blocker Noise Figure	33
2.8.4	Linearity	33
2.8.5	Input Matching	34
2.8.6	Comparison with Prior Art	35
2.9	Fully-Differential FTNC-RX Design	37

2.10	Conclusion . . . . .	41
<b>3</b>	<b>An LTV analysis of the Frequency-Translational Noise-Cancelling RX</b>	<b>42</b>
3.1	Introduction . . . . .	42
3.2	Downconversion in an $M$ -phase Passive Mixer . . . . .	45
3.3	Modeling the Passive Mixer . . . . .	48
3.3.1	The LTV Passive Mixer Model . . . . .	48
3.3.2	Passive Mixer with Infinite Load Impedance . . . . .	50
3.3.3	Passive Mixer with Finite Load Impedance . . . . .	52
3.4	Relating the Passive Mixer to the FTNC-RX Outputs . . . . .	53
3.4.1	Output of the Complete FTNC-RX . . . . .	53
3.4.2	Output of the Main Path . . . . .	55
3.4.3	Output of the Auxiliary Path . . . . .	55
3.5	The Mixer-First RX (or Main Path of the FTNC-RX) . . . . .	56
3.5.1	Mixer-First RX Conversion Gain . . . . .	57
3.5.2	Output Noise due to Norton Equivalent Load . . . . .	57
3.5.3	Output Noise due to Baseband Sources . . . . .	58
3.5.4	Noise Figure of Mixer-First RX . . . . .	59
3.5.5	Simulation Results . . . . .	60
3.6	The Complete FTNC-RX . . . . .	64
3.6.1	Auxiliary Path Conversion Gain . . . . .	65
3.6.2	Antenna Noise . . . . .	66
3.6.3	Switch Noise . . . . .	68
3.6.4	Baseband Noise . . . . .	70
3.6.5	$G_M$ Cell Noise . . . . .	72



3.6.6	Auxiliary Switch and Baseband Noise . . . . .	72
3.7	Noise Figure of FTNC-RX . . . . .	72
3.7.1	Noise Figure Assuming Resistive RF Node . . . . .	72
3.7.2	Noise Figure Assuming Large $M$ . . . . .	73
3.7.3	Noise Figure for Other Cases . . . . .	73
3.7.4	Simulation Results . . . . .	74
3.8	The FTNC-RX as a High- $Q$ Filter . . . . .	75
3.9	Conclusion . . . . .	76
<b>4</b>	<b>Phase Noise in <math>LC</math> Oscillators: A Phasor-Based Analysis of a General Result and of Loaded <math>Q</math></b> . . . . .	<b>79</b>
4.1	Introduction . . . . .	79
4.2	Oscillator Preliminaries . . . . .	81
4.2.1	The Negative-Gm Oscillator . . . . .	81
4.2.2	Constraints from Energy Conservation . . . . .	82
4.3	A “Noiseless” Oscillator Injected with a Small Current Source . . . . .	84
4.3.1	Recognizing Phase and Amplitude Modulating Sidebands . . . . .	84
4.3.2	Response of the Nonlinearity to AM/PM Modulated Carriers . . . . .	84
4.3.3	Response of the Negative-Gm Oscillator to an External Current Source . . . . .	86
4.4	Decomposition of a Resonator-Referred Cyclostationary White Noise Source . . . . .	91
4.5	The Noise Factor of the Negative-Gm Model . . . . .	95
4.5.1	Noise from Resonator Losses . . . . .	96
4.5.2	Noise from the Nonlinearity . . . . .	96
4.5.3	The General Result and Implications . . . . .	97
4.5.4	SpectreRF Simulations . . . . .	98

4.6	Applying the General Result to Popular Oscillators . . . . .	101
4.6.1	Noise Factor . . . . .	101
4.6.2	Extrinsic Noise . . . . .	107
4.6.3	Oscillation Amplitude . . . . .	108
4.7	$Q$ Degradation Analysis . . . . .	108
4.7.1	An Arbitrary Nonlinearity that Contributes Loss . . . . .	109
4.7.2	The Standard Voltage-Biased NMOS Topology . . . . .	110
4.7.3	The Standard Current-Biased CMOS Topology . . . . .	116
4.8	Reconciling the ISF and Phasor-Based Approaches . . . . .	121
4.9	Conclusion . . . . .	122
<b>5</b>	<b>A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver . . . . .</b>	<b>123</b>
5.1	Introduction . . . . .	123
5.2	PLL Topology . . . . .	126
5.3	Frequency Tuning using DiCAD . . . . .	129
5.3.1	The Motivation for DiCAD . . . . .	129
5.3.2	DiCAD Structure . . . . .	130
5.3.3	Switch-Selection . . . . .	132
5.4	Key Millimeter-Wave Design Choices . . . . .	133
5.4.1	mm-Wave VCO . . . . .	133
5.4.2	DiCAD-Based Injection-Locked Buffer and Divider . . . . .	136
5.5	Measurement Results . . . . .	136
5.6	Conclusion . . . . .	144
	<b>References . . . . .</b>	<b>146</b>

## LIST OF FIGURES

2.1	Effect of an out-of-band blocker on narrowband and wideband receivers. . .	5
2.2	Noise degradation due to reciprocal mixing in a perfectly linear wideband receiver. . . . .	6
2.3	The mixer-first receiver; RF input impedance is combination of mixer switch resistance ( $R_{SW}$ ) and upconverted TIA input impedance ( $Z_{BB}$ ). . . . .	8
2.4	Wideband receiver employing a voltage-sampling mixer. The input impedance of the mixer acts as a high- $Q$ filter. . . . .	8
2.5	Wideband receiver employing RF transconductance amplifier. The input impedance of mixer is kept small, which minimizes RF voltage gain. . . . .	9
2.6	Noise cancelling theory as applied to LNAs. . . . .	10
2.7	Selected noise-cancelling LNA topologies. . . . .	11
2.8	Evolution of the proposed frequency translational noise-cancelling receiver. . . . .	11
2.9	The proposed noise-cancelling receiver. . . . .	12
2.10	The class-AB transconductance (plots assume $R_{LOAD}=0$ ). . . . .	14
2.11	Limitation of the class-AB transconductance on the large-signal linearity of the FTNC-RX. . . . .	16
2.12	Traditional 50% I/Q mixer: LO approximation and aliasing terms. . . . .	17
2.13	Oversampling I/Q mixer: LO approximation and aliasing terms. . . . .	17
2.14	An oversampling downconversion mixer employing an 8-phase LO. By changing the baseband weighting constants, an effective LO with any arbitrary magnitude or phase can be realized. Two examples of possible LO waveforms are shown. . . . .	19
2.15	Simplified FTNC-RX model highlighting main noise sources. All noise sources, with the exception of the $G_M$ noise, can be nulled or contribute negligibly. . . . .	21

2.16	Simplified TIA model. . . . .	22
2.17	The complete frequency-translational noise-canceling receiver (FTNC-RX).	24
2.18	LO-to-RF noise coupling in passive mixers. . . . .	25
2.19	Johnson divider and associated simulation results. . . . .	27
2.20	Baseband TIAs (component values reflect those used in main path TIAs). .	28
2.21	Die micrograph of single-ended FTNC-RX. . . . .	29
2.22	Measured noise figure of the FTNC-RX in two modes of operation. . . . .	30
2.23	Noise-cancelling optimization via baseband phase and magnitude correction.	32
2.24	Measured receiver gain and noise figure assuming a wanted signal at 1.5GHz accompanied by a 1.58GHz continuous-wave blocker. . . . .	33
2.25	Measured receiver linearity at $f_{LO} = 2GHz$ . . . . .	34
2.26	Measured S11. . . . .	35
2.27	The fully-differential FTNC-RX. . . . .	38
2.28	Measured noise figure, blocker noise figure, IIP3 and S11 for the fully- differential FTNC-RX prototype. . . . .	39
3.1	A simplified LTI analysis of the FTNC-RX. . . . .	44
3.2	Time-domain representation of $sw(t)$ . . . . .	45
3.3	Harmonic folding in the passive mixer. . . . .	47
3.4	Modeling the $M$ -phase passive mixer. . . . .	49
3.5	Linear time-invariant (LTI) model around $m^{\text{th}}$ harmonic. . . . .	54
3.6	Model of the FTNC receiver. . . . .	56
3.7	LTI model of mixer-first receiver. . . . .	61
3.8	The simulated mixer-first RX model. (Harmonic recombination with $G_{MAIN}=3000$ is not shown.) . . . . .	62
3.9	Simulation and analysis results of the mixer-first RX model. . . . .	63

3.10	Noise figure of aggressive mixer-first design. (Solid lines correspond to analysis, markers correspond to simulation.) . . . . .	65
3.11	Simulated FTNC-RX model. (Not shown is the recombination of the main and auxiliary baseband currents with gains of $G_{MAIN}=3000$ and $G_{AUX}=450e^{j\frac{10\pi}{180}}$ respectively.) . . . . .	67
3.12	Gain of FTNC-RX. (Solid lines correspond to analysis, markers correspond to simulation.) . . . . .	68
3.13	Contribution of switch noise to the noise factor of the FTNC-RX. (LO frequency = 3GHz; Solid lines corresponds to analysis, markers correspond to simulation). . . . .	70
3.14	Contribution of baseband noise sources to the noise factor of the FTNC-RX. (LO frequency = 3GHz; Solid lines correspond to analysis, markers correspond to simulation.) . . . . .	71
3.15	Noise figure of complete FTNC-RX assuming $G_{MAIN} = G_M G_{AUX} Z_S \{m\omega_c + \Delta\omega\}$ . (Solid lines correspond to analysis, markers correspond to simulation.) . . .	74
3.16	Noise figure versus auxiliary path gain and phase correction. (LO frequency = 3GHz; Solid lines correspond to analysis, markers correspond to simulation.)	75
3.17	Receivers topologies employing high- $Q$ frequency translational bandpass filters (FT-BPF). . . . .	77
4.1	A generic negative-gm $LC$ oscillator model. . . . .	81
4.2	(a) Sideband magnitudes do not reveal modulation type; (b) PM sidebands: sum is orthogonal to carrier; (c) AM sidebands: sum is colinear with carrier; (d) A single sideband around can be decomposed into equal PM and AM sidebands. . . . .	85
4.3	Response of the nonlinearity to an AM and PM signal. . . . .	86
4.4	A noiseless negative-gm oscillator excited by an external current source. . .	87

4.5	Differential current source acting on a “noiseless” oscillator. . . . .	90
4.6	Squared impedance seen by phase and amplitude modulating currents. . .	91
4.7	Cyclostationary white noise modeled as a white noise source modulated by a periodic waveform. . . . .	92
4.8	Frequency spectrum of arbitrary waveform, $w(t)$ . . . . .	92
4.9	Phasor diagrams. . . . .	94
4.10	Generic negative-gm oscillator simulations. . . . .	99
4.11	The standard current-biased NMOS $LC$ oscillator. . . . .	102
4.12	The standard current-biased CMOS $LC$ oscillator. . . . .	105
4.13	The Colpitts oscillator. . . . .	106
4.14	A generic negative-gm $LC$ oscillator model. . . . .	109
4.15	The voltage-biased standard NMOS $LC$ oscillator. . . . .	112
4.16	The standard voltage-biased NMOS $LC$ oscillator: typical plots. . . . .	113
4.17	Predicted noise factors of the voltage-biased oscillator and the current-biased oscillator. . . . .	113
4.18	The standard voltage-biased NMOS $LC$ oscillator: simulation results. . . .	115
4.19	The standard current-biased CMOS $LC$ oscillator. . . . .	117
4.20	Phase noise performance of the CMOS standard current-biased $LC$ topol- ogy with a differential capacitor arrangement and a single-ended capacitor arrangement. . . . .	120
4.21	Amplitude of the CMOS standard current-biased $LC$ topology with a differ- ential capacitor arrangement and a single-ended capacitor arrangement. . .	120
5.1	The IEEE 802.15.3c channel specification. . . . .	124
5.2	A heterodyne 60GHz transceiver with separate TX/RX PLLs. . . . .	127

5.3	The fabricated integer-N type-II 48GHz PLL (with highlighted mm-wave blocks). . . . .	128
5.4	Mm-wave circuit blocks used in the PLL. All blocks employ DiCAD as frequency tuning element. . . . .	128
5.5	An overview of possible frequency tuning schemes. (a) Simplified $LC$ oscillator; wideband mm-wave VCOs are typically limited by loss associated with $C_{TUNE}$ (b) Digitally controlled varactor bank (c) Switch capacitor bank is best option at RF, but interconnect reduces performance at mm-wave. (d) $Q/TR$ trade-off of a switch cap array. . . . .	130
5.6	Digitally-Controlled-Artificial-Dielectric (DiCAD). . . . .	132
5.7	A comparison of switches that can be used in the programmable transmission line. . . . .	134
5.8	Measurement of the VCO's continuous tuning characteristics. . . . .	137
5.9	Measurement of the VCO's discrete tuning characteristic. . . . .	138
5.10	The performance metrics of the DiCAD-VCO across entire frequency band.	139
5.11	The closed loop phase noise measurements with a large off-chip loop filter.	139
5.12	The closed loop phase noise measurements with on-chip loop filter enabled.	141
5.13	The die micrographs. . . . .	143
5.14	The calibration algorithm used to align the center frequencies of the VCO, buffer and 1 <sup>st</sup> stage divider. . . . .	145

## LIST OF TABLES

2.1	Comparison with recently published blocker-tolerant receivers . . . . .	36
2.2	Comparison between single-ended and fully-differential FTNC-RX prototypes	40
5.1	Phase noise and figure of merit measurements @1MHz offset . . . . .	140
5.2	Comparison with other 65nm/90nm wideband mm-wave VCOs . . . . .	141
5.3	Comparison of PLL with recent state of the art . . . . .	142



## ACKNOWLEDGMENTS

I cannot overstate my gratitude to Prof. Abidi. It has been a privilege to learn from, work for and collaborate with him over these past years. I am equally grateful to Prof. Chang for introducing me to the exciting world of mm-wave design, supporting my research goals, and welcoming me into his lab during Prof. Abidi's sabbatical.

I am indebted to Hooman Darabi who served as a third de facto adviser. The receiver architecture described in this dissertation was developed under his day-to-day guidance at Broadcom.

Many others have had a direct influence on the work laid out in this dissertation. I am particularly grateful to Ahmad Mirzaei, Jacob Rael, Mohyee Mikhemar, Adrian Tang, Jane Gu, Bryan Wu, Henry Jian, Amr Hafez and Tim LaRocca. I would also like to thank my Masters adviser, Prof. Peter Kennedy, for suggesting that I continue my graduate studies and for supporting my application to UCLA.

Finally, I must thank my parents from whom I could not have asked for more support, love or opportunities in life. I dedicate this thesis to them.

## VITA

- 2004            B.E., Microelectronic Engineering,  
                  University College Cork, Ireland.
- 2006            M.Eng.Sc., Microelectronic Engineering,  
                  University College Cork, Ireland.

## PUBLICATIONS

D. Murphy, A. Hafez, A. Mirzaei, M. Mikhemar, H. Darabi, M.-C. F. Chang, and A. A. Abidi, "A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure," in *IEEE ISSCC Dig. 2012*, 19-23 Feb. 2012.

D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in  $LC$  oscillators: a phasor-based analysis of a general result and of loaded  $Q$ ," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 6, pp. 1187-1203, June 2010.

D. Murphy, Q. J. Gu, Y.-C. Wu, H.-Y. Jian, Z. Xu, A. Tang, F. Wang, Y.-L. Lin, H.-H. Chen, C. Jou, and M.-C. F. Chang, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15.3c TRX," in *Proc. ESSCIRC 2010*, 14-16 Sept. 2010.

D. Murphy, Q. J. Gu, Y.-C. Wu, H.-Y. Jian, Z. Xu, A. Tang, F. Wang, and M.-C. F. Chang, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15.3c TRX," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1606-1617, July 2011.

# CHAPTER 1

## Thesis Overview

This dissertation is concerned with noise in large signal, time-varying CMOS RF circuits, and consists of 3 distinct parts. Chapters 2 & 3 introduce and analyze a highly-linear noise-cancelling receiver. Chapter 4 presents new theoretical results relating to phase noise mechanisms in  $LC$  oscillators, while chapter 5 documents a low-noise, wideband PLL that is suitable for mm-wave applications. A more detail overview of each chapter is offered below. Each chapter (with the exception of this one) presents a self-contained contribution and, therefore, conclusions are drawn at the end of each chapter rather than at the end of the dissertation itself.

### Chapter 2: A Blocker-Tolerant Noise Cancelling Receiver

As narrowband off-chip RF filtering is not compatible with the design of wideband receivers, such receivers must be designed to tolerate large out-of-band blockers with minimal gain compression and noise figure degradation. Recently a number of wideband “blocker-tolerant” CMOS receivers have demonstrated that is possible to accommodate 0dBm blockers without passive RF-filtering, but all these approaches come at the expense of noise figure. To overcome this limitation, a new wideband receiver architecture is proposed that employs two separate passive-mixer-based downconversion paths, which enables noise cancelling, but avoids voltage gain at blocker frequencies. This approach significantly relaxes the trade-off between noise, out-of-band linearity and wideband operation. Prototypes with a single-ended RF input and a fully-differential RF input are fabricated. The single-ended version is functional from 80MHz to 2.7GHz and achieves a 2dB noise figure, which only degrades to 4.1dB in the presence of a 0dBm blocker.

### **Chapter 3: An LTV Analysis of the Blocker-Tolerant Noise-Cancelling RX**

The noise-cancelling receiver proposed in chapter 2 demonstrates exceptional out-of-band linearity, a low noise figure, and wideband operation. The central innovation of the receiver is that two passive-mixer-based downconversion paths are employed, which delays noise-cancelling until after aggressive baseband filtering. Although a simplified LTI analysis is sufficient to understanding the basic noise properties of the system, such an analysis cannot yield accurate closed-form expressions because it neglects the many signal and noise folding terms introduced by the two passive mixers. In chapter 3, a complete LTV analysis is presented, which accurately captures both the gain and the noise performance of the proposed receiver. Simulation results verify the analysis.

### **Chapter 4: A Phasor-Based Analysis of $LC$ Oscillators**

Recent work by Bank, and Mazzanti and Andreani has offered a general result concerning phase noise in nearly-sinusoidal  $LC$  oscillators; namely that the noise factor of such oscillators (under certain achievable conditions) is largely independent of the specific operation of individual transistors in the active circuitry. Both use the impulse sensitivity function (ISF). In Chapter 4, we show how the same result can be obtained by generalizing the competing phasor-based analysis method. Indeed, as applied to nearly-sinusoidal  $LC$  oscillators, we show how the two approaches are equivalent.

We analyze the negative-gm  $LC$  model and present a simple equation that quantifies output noise resulting from phase fluctuations. We also derive an expression for output noise resulting from *amplitude* fluctuations. Furthermore, we extend the analysis to consider the voltage-biased  $LC$  oscillator and fully differential CMOS  $LC$  oscillator, for which Bank's general result does not apply. This enables us to quantify the concept of loaded  $Q$ .

## Chapter 5: A Wideband, Low Noise Millimeter-wave PLL

In chapter 5, a low phase noise, wideband, mm-wave, integer-N PLL that is capable of supporting a 802.15.3c heterodyne transceiver is reported. The PLL can generate 6 equally spaced tones from 43.2GHz to 51.84GHz, which is suitable for a heterodyne architecture where the intermediate frequency ( $f_{IF}$ ) is one fifth the receive/transmit frequency ( $f_{TRX}$ ), i.e.  $f_{LO} = (4/5) \times f_{TRX} = 4 \times f_{IF}$ . Phase noise is measured directly at the PLL output frequency ( $f_{LO}$ ) and is better than -97.5dBc/Hz@1MHz across the entire band. The reported frequency synthesizer is smaller, exhibits less phase noise, and consumes less power than prior art. In addition, the  $f_{LO}$  tone corresponds to the fundamental of the VCO as opposed to a higher harmonic.

Central to the PLL performance is the design of a low-noise, wideband, mm-wave VCO with a 22.9% tuning range. Fine discrete tuning and minimization of parasitics is achieved using a programmable transmission line as a frequency tuning element.

## CHAPTER 2

# A Blocker-Tolerant Noise-Cancelling Receiver

### 2.1 Introduction

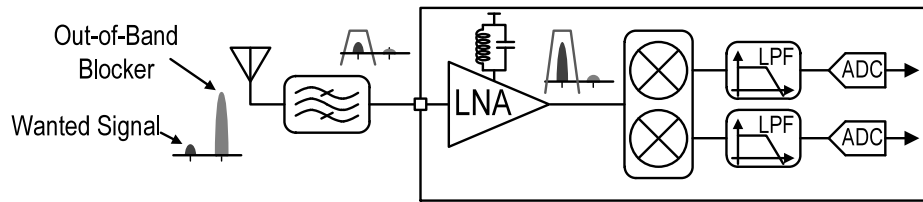
Narrowband receiver front-ends invariably make use of external RF filtering to prevent large out-of-band signals corrupting the wanted signal. Since RF filters are almost always fixed<sup>1</sup>, multiple front-ends are required to cover the large number of frequency bands serviced by a modern wireless device. The alternative is a single wideband receiver that is tunable over the entire the spectrum of interest, but since such a receiver must work without RF filtering it is easily desensitized by large unwanted signals. This inability to handle interferers has prevented wideband designs from being adopted in commercial products, but, if this issue could be overcome, a wideband approach would have some distinct advantages including: lower pin count, simplified package design, reduced number of off-chip components and faster design times. As well as simplifying conventional multi-band receiver designs, a highly-linear wideband receiver is fundamental to the flexible, universal radio platform known as Software-Defined-Radio (SDR) [1–4].

Avoiding the desensitization of a wideband receiver by large out-of-band blockers is challenging, particularly if it is to compete with a narrowband design. Consider this: A modern cellular receiver typically demonstrates close to a 2dB noise figure, while sustaining a blocker as large as 0dBm only 20MHz away from the desired channel. To achieve this noise figure in the cascade of circuits that make up the receiver, the LNA gain is usually at least 15dB. A conventional narrowband design (Fig 2.1(a)) makes use of an off-chip

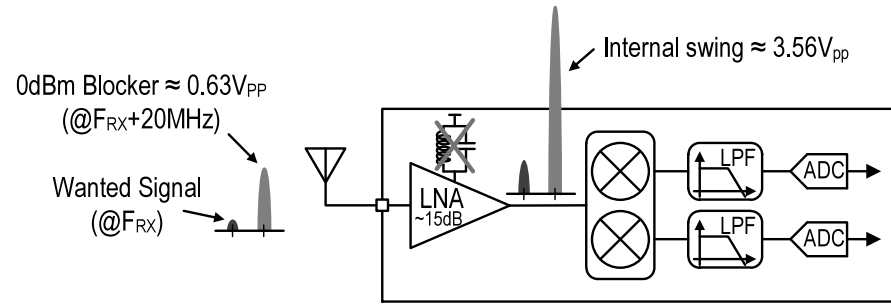
---

<sup>1</sup>The tracking filter in discrete TV receivers is a notable exception. It uses a passive filter with inductors and capacitors switched with low loss PIN diodes.

SAW filter and a tuned LNA to suppress blockers, whereas a wideband design will amplify both the wanted signal and any blocker present (Fig 2.1(b)). In this latter case, linear amplification of a 0dBm blocker would result in an internal voltage swing of 3.5V. Of course, in a modern CMOS process, gain saturation will occur long before this swing is reached, which will increase noise and distortion in the receiver.



(a) A narrowband direct-conversion narrowband receiver typically employs both off-chip and on-chip passive RF filtering to attenuate any unwanted signals.



(b) A wideband receiver cannot employ passive RF filtering and, therefore, a large blocker will saturate a conventional front-end design.

Figure 2.1: Effect of an out-of-band blocker on narrowband and wideband receivers.

Desensitization due to reciprocal mixing of LO phase noise by blockers is also a serious matter in a wideband receiver. Since passive filtering is prohibited, any blocker present (whether or not it causes gain compression) will be downconverted along with the wanted signal. When the blocker mixes with LO phase noise, it deposits additive noise in the receive channel proportional to the blocker amplitude (Fig 2.2). Thus, for a perfectly linear wideband receiver to maintain the same noise figure as an equivalent narrowband receiver, its LO phase noise must be reduced by one dB for every dB of filter attenuation that is removed at the blocker frequency.

The mechanisms of gain compression and reciprocal mixing just described imply that

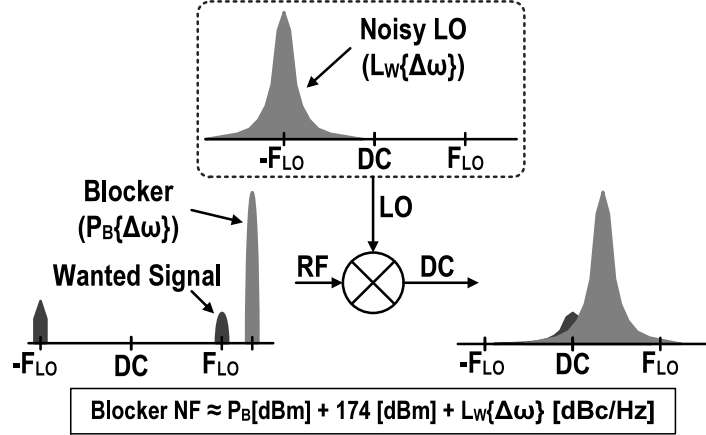


Figure 2.2: Noise degradation due to reciprocal mixing in a perfectly linear wideband receiver.

for a wideband receiver to be considered blocker-tolerant, it must avoid voltage gain at blocker frequencies and should generate LO signals with very low out-of-band phase noise.

While industry has shunned wideband receiver design, it has been the focus of academia for some years. A notable work [5, 6] shows how wideband operation and low noise can be simultaneously achieved through noise-cancelling, while another has presented a complete receiver solution for an SDR [2–4]. But, as the authors of [2–4] themselves acknowledge, these designs are incapable of meeting the stringent blocker specifications demanded by cellular standards. More recently, recognizing the high linearity of passive-mixers, a number of blocker-tolerant CMOS receivers have been developed [7–14], but in each case linearity and wideband operation comes at the expense of noise figure. What is needed is a wideband “blocker-tolerant” receiver that exhibits a sufficiently low noise figure that it may be used in place of multiple narrowband low-noise front-ends. Within this context, we describe a new receiver architecture [15] that can tolerate large out-of-band blockers without relying on SAW pre-filters, and *without* sacrificing noise performance. The design evolves from noise-cancelling theory, but avoids voltage gain at blocker frequencies by employing two separate downconversion paths. As a result, large out-of-band blockers can be tolerated while the benefits of noise-cancelling are retained, i.e. wideband operation and low noise. The next section first reviews relevant prior-art before the proposed receiver is introduced in Sec. 2.3.



Sections 2.4 and 2.5 discuss the design of key building blocks, namely the RF transconductance and oversampling mixers, while Sec. 2.6 presents a simplified noise analysis of the receiver. Section 2.7 discusses the circuit implementation of a single-ended prototype and Sec. 2.8 presents measurement results relating to that design. A fully-differential prototype is briefly discussed in Sec. 2.9, before conclusions are drawn in Sec. 2.10.

## 2.2 Prior Art: Blocker-Tolerant Receivers

A number of innovative designs have shown that a wideband CMOS front-end can tolerate blockers as large as 0dBm [7–14]. While different techniques are employed, all these circuits have two common features: they employ passive-mixers and they suppress voltage gain at blocker frequencies. One such topology is the “mixer-first” receiver, introduced in [16]. To prevent amplification of the blocker, the receiver eliminates RF amplification by connecting the antenna directly to the downconversion mixers, removing the LNA altogether. A more sophisticated mixer-first design [7–9], shown in Fig. 2.3, provides an appropriate  $50\Omega$  match using a property call N-path filtering [17, 18]. This approach results in an exceptionally linear receiver, however, the noise figure is high because there is no LNA. A noise figure of greater than 3dB at low frequencies is reported, which degrades significantly in the GHz. Also, since the incoming signals experience no gain prior to downconversion, the noise contribution of the baseband amplifiers can dominate and flicker noise can be unacceptably large at low-IF.

Another relevant receiver, shown in Fig. 2.4(a), utilizes a voltage sampling mixer to attenuate out-of-band signals [10, 11]. N-path filtering is again consciously employed such that the impedance looking into the downconversion mixers has a bandpass characteristic that tracks the LO frequency. However, in this case, the resultant high- $Q$  filter loads a wideband LNA instead of the antenna. The wanted signal, which falls inside the bandwidth of the filter, experiences full gain, while any out-of-band signals are attenuated. The LNA is a differential common-gate topology with partial noise-cancelling (Fig 2.4(b)). This circuit provides wideband matching, but it results in a moderate receiver noise figure of 3.2dB,

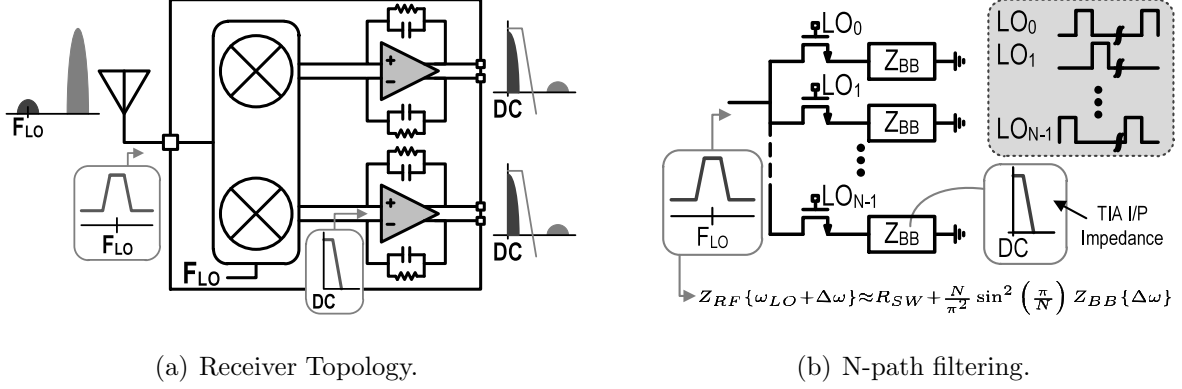


Figure 2.3: The mixer-first receiver; RF input impedance is combination of mixer switch resistance ( $R_{SW}$ ) and upconverted TIA input impedance ( $Z_{BB}$ ).

which degrades to 13dB in the presence of a 0dBm blocker. Another major drawback is that the LNA requires differential inputs, which necessitates the use of a wideband off-chip balun. A narrowband balun will introduce at least 1dB of insertion loss which adds directly to the receiver's NF, while practical low-cost wideband baluns are not readily available.

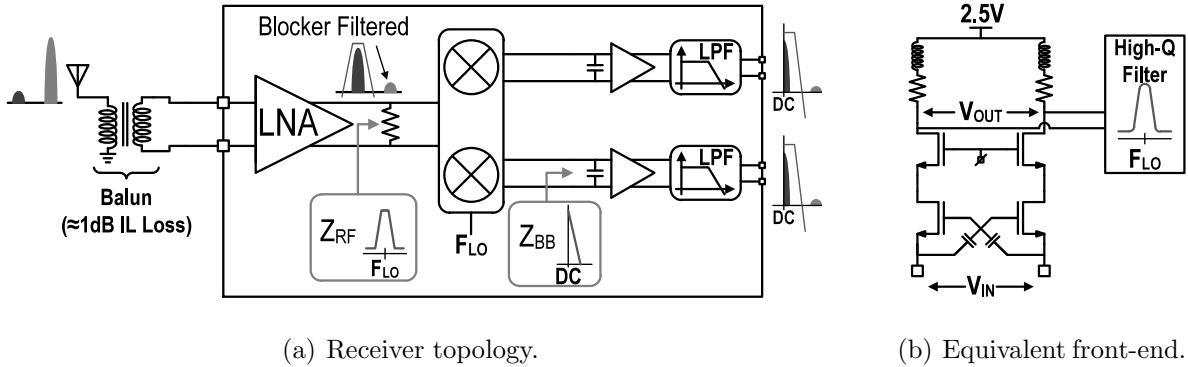
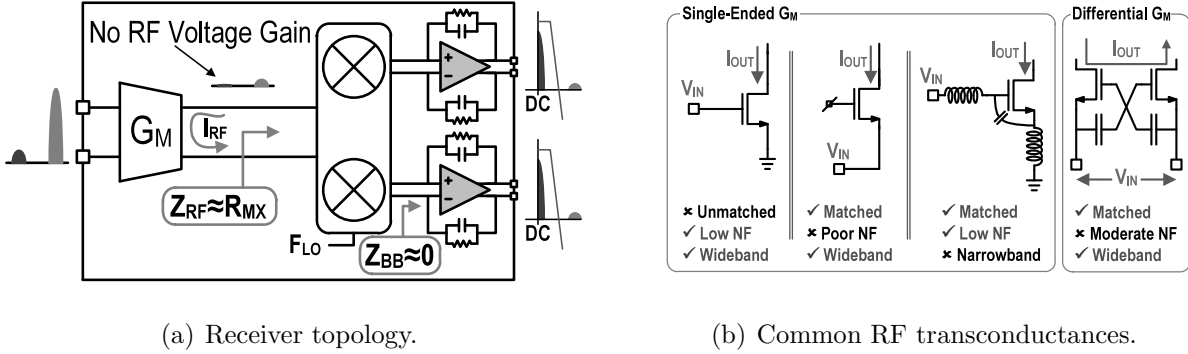


Figure 2.4: Wideband receiver employing a voltage-sampling mixer. The input impedance of the mixer acts as a high- $Q$  filter.

In [19] and later in [12–14] the LNA is replaced with a linear transconductance, which drives a current mode passive mixer (Fig 2.5(a)). In such an approach, RF voltage gain can be avoided by employing large passive mixer switches and ensuring the input impedance of the transimpedance amplifiers (TIAs) are close to zero, however, a trade-off between noise figure and wideband operation still exists; referring to Fig 2.5(b), it is clear that no single-ended  $G_M$  cell can simultaneously provide low-noise and wideband matching. If differential

inputs are used, a differential common-gate topology with partial noise-cancelling can be employed, but even in this case only moderate noise performance similar to [10, 11] can be expected.



(a) Receiver topology.

(b) Common RF transconductances.

Figure 2.5: Wideband receiver employing RF transconductance amplifier. The input impedance of mixer is kept small, which minimizes RF voltage gain.

## 2.3 Proposed Noise-Cancelling Receiver

Given the discussion in the previous section, it is fair to say that every wideband, blocker-tolerant CMOS receiver currently published compromises on noise performance. To break this trade-off between blocker-tolerance and noise figure, noise-cancelling theory must first be revisited [5, 6].

### 2.3.1 Noise-Cancelling Theory

A matched wideband LNA should present a real  $50\Omega$  impedance to the antenna, but this matching resistor generally limits the achievable noise figure to 3dB. This resistor noise can be nulled in a noise-cancelling LNA (NC-LNA) by measuring the voltage at the RF node *and* the current flowing through the matching resistor. Shown in Fig. 2.6, the output of the circuit is the difference between the voltage measurement path ( $\alpha V_{R_{IN}}$ ) and current measurement path ( $-r_m I_{R_{IN}}$ ). By appropriately setting the relative gain of these paths, i.e.  $r_m = \alpha R_S$ , the incoming signal appears differentially at the output, while the noise of the matching resistor appears as common-mode. Accordingly, the noise figure can theoretically

be zero dB.

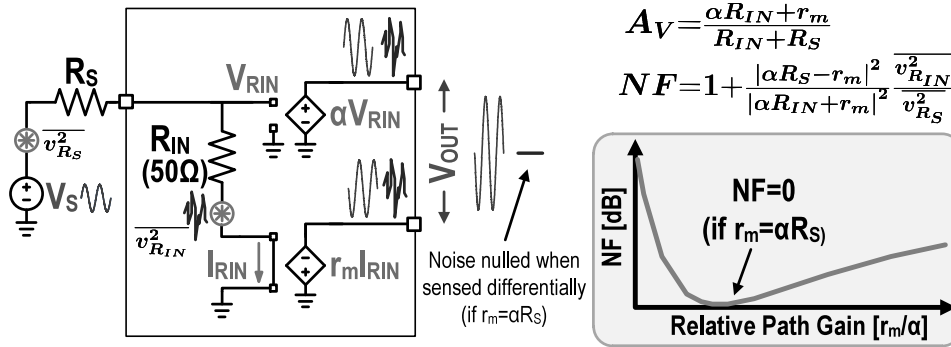


Figure 2.6: Noise cancelling theory as applied to LNAs.

Typically, noise-cancelling is realized using some variation of the topology shown in Fig. 2.7(a). A common-gate FET provides the real  $50\Omega$  impedance and the current measurement, while a much larger common-source FET, sized for low input-referred noise, provides the voltage measurement. The common-gate and common-source currents (which are unequal) are then converted to balanced voltages at RF. A significant drawback to this approach is that voltage gain is present across a wide bandwidth and, therefore, large blockers can drive the amplifier into saturation. Noting that there is no requirement to generate *voltages* at RF, one approach [20, 21] proposes stacking an active mixer on top of the input transistors, and converting the currents to voltages at a low IF (Fig. 2.7(b)). Although the topology extends the receive bandwidth, the use of active mixers results in a poor NF. The topology is also unlikely to be blocker-tolerant because of transistor stacking and large voltage swings at IF.

### 2.3.2 The Frequency-Translational Noise-Cancelling Receiver

In order to tolerate large blockers while still employing full noise-cancelling, this work proposes the use of two separate passive-mixer-based downconversion paths. Figure 2.8 shows the evolution of the proposed topology from the simple noise-cancelling model. Instead of converting the current measurement to a voltage at RF, a passive mixer immediately down-converts the RF-current to baseband. A TIA then converts any current in the receive-band

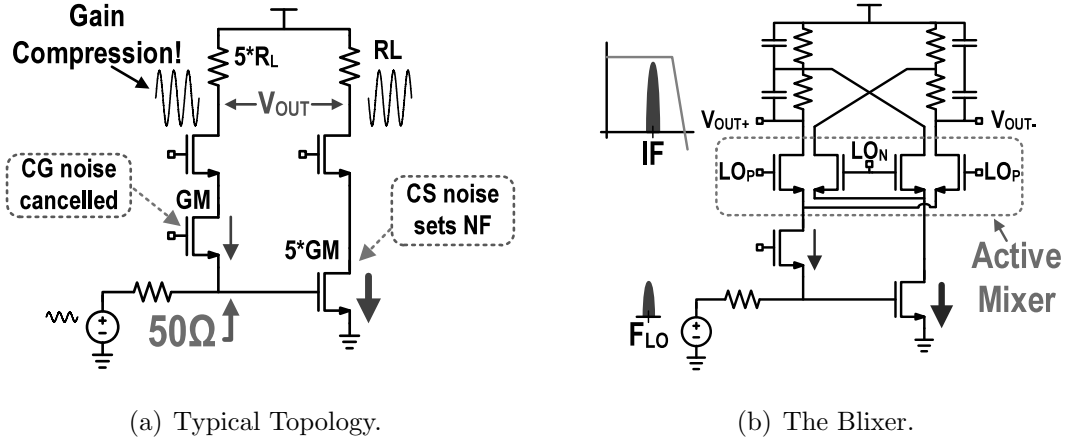


Figure 2.7: Selected noise-cancelling LNA topologies.

to voltage. The voltage measurement is provided by an auxiliary path, where an RF-transconductance converts the RF node voltage to a current, which is then downconverted by another passive mixer. Another TIA then converts any in-band current to voltage. As outlined in the remainder of this chapter, this *Frequency-Translational Noise-Cancelling Receiver* (FTNC-RX) can be both low-noise and blocker tolerant.

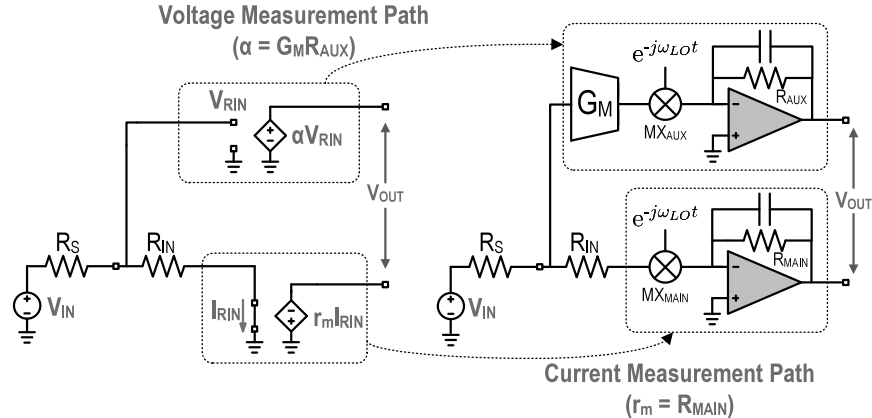


Figure 2.8: Evolution of the proposed frequency translational noise-cancelling receiver.

As shown in Fig. 2.9, if high-gain baseband operational amplifiers are employed, the input terminal of both TIAs appear as virtual grounds. Additionally, if large switches are used in the passive mixers, the impedance looking into the RF terminal of each mixer is small and, therefore, no RF voltage gain is experienced. While a large out-of-band blocker<sup>2</sup>

<sup>2</sup>It is assumed that the frequency offset of the blocker from the wanted signal is much larger than the

will result in a large current flowing into the mixers, particularly in the auxiliary path, this current once downconverted will appear outside the TIA bandwidth and, therefore, will not generate a large voltage. Since a blocker does not experience voltage amplification, the effect of gain compression is significantly reduced compared to a standard noise-cancelling LNA. In addition to their excellent linearity and low flicker noise [19,22], passive mixers can handle large downconversion currents [7–14,23–26] and, therefore, the auxiliary transconductance cell will ultimately limit the achievable large-signal linearity of the system. Importantly, unlike other receiver topologies, this transconductance does not need to provide impedance matching and, so, its design is greatly simplified. The design of this cell is discussed in the next section, followed by a discussion of the mixers in Sec. 2.5. In regard to noise, the noise associated with the matching resistor can of course be cancelled, however, the receiver has some other interesting noise properties, which are explored in Sec. 2.6.

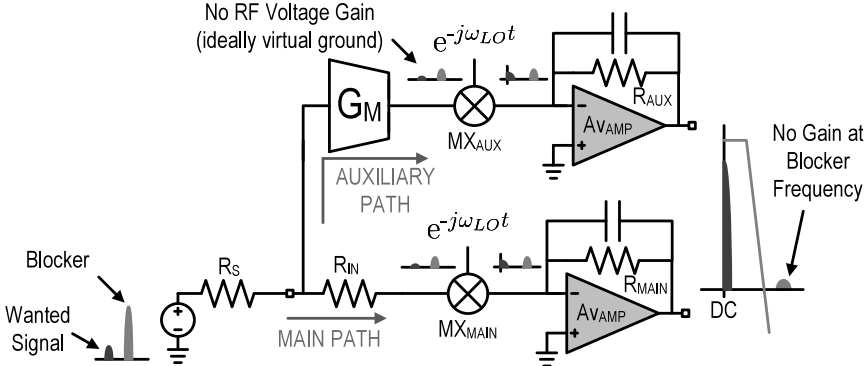


Figure 2.9: The proposed noise-cancelling receiver.

## 2.4 Linearity Bottleneck: The Class-AB Transconductance

The auxiliary transconductance was realized using the class-AB CMOS cell [27] of Fig. 2.10(a), commonly recognized as a CMOS inverter with a resistor load. It has been shown that by sizing the PMOS and NMOS devices such that their transconductances are equal, IIP2 is improved through push-pull drive and IIP3 through local distortion cancellation [28, 29].

---

bandwidth of the wanted signal (or equivalently the TIA bandwidth).

The cell's linearity is further boosted, by holding the voltage swing at the output node to the minimum. The gain at the output node is  $G_M R_{LOAD}$ , where  $R_{LOAD}$  is a combination of the mixer switch resistance and the (up-converted) TIA impedance in the auxiliary path (assuming the output impedance of the transconductance is much larger than  $R_{LOAD}$ ). If the load impedance is close to  $0\Omega$ , this class-AB stage can handle large swings at the input. Figure 2.10(b) is a plot of small-signal transconductance versus DC input bias, which demonstrates that  $G_M$  (assuming  $R_{LOAD} \approx 0$ ) is flat and reasonably independent of the bias point.

To investigate this more formally, let's define the output current as  $i_{OUT} = f(v_{IN}, v_{OUT})$ , where  $f(\cdot)$  is some nonlinear function of the two variables,  $v_{IN}$  and  $v_{OUT}$ . First, we examine the case when the input is of the form  $v_{IN}(t) = A_{IN} \cos(\omega_{LO}t)$  and the load impedance is  $0\Omega$ , which implies  $v_{OUT}(t) = 0$  and  $i_{OUT}(t) = f(v_{IN}(t), 0)$ . For a memoryless nonlinearity, the output current can be described by

$$i_{OUT}(t) = I_{OUT}[0] + \sum_{k=1}^{\infty} I_{OUT}[k] \cos(\omega_{LO}t), \quad (2.1)$$

where  $I_{OUT}[k]$  are the Fourier coefficients of  $i_{OUT}(t) = f(A_{IN} \cos(\omega_{LO}t), 0)$ . Now the large-signal transconductance is defined as

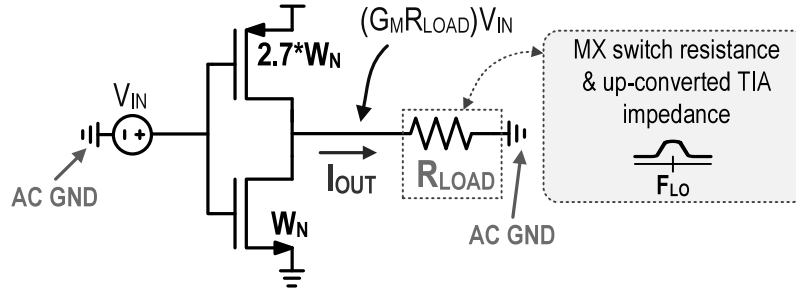
$$G_M = \frac{I_{OUT}[1]}{A_{IN}}, \quad (2.2)$$

which is plotted in Fig. 2.10(c) versus the input amplitude,  $A_{IN}$ . It is noted that  $G_M$  remains constant even for input swings which exceed the rail voltage, which implies that the circuit suffers from a very small transconductance nonlinearity<sup>3</sup>. However, this excellent linearity only holds true when  $R_{LOAD} = 0$  and  $v_{OUT} = 0$ . To explore the condition when  $v_{OUT}(t) \neq 0$ , we revert to the fundamental dependence,  $i_{OUT}(t) = f(v_{IN}(t), v_{OUT}(t)) = f(v_{IN}(t), i_{OUT}(t)R_{LOAD})$ , which has an implicit dependence of  $i_{OUT}$  on  $v_{IN}$ . In well-behaved nonlinearities, this can be re-defined as an explicit dependence on  $v_{IN}(t)$ , which can then be expressed as a power series

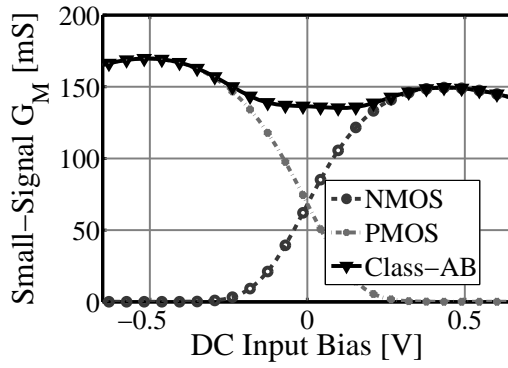
$$i_{OUT}(t) = g(v_{IN}(t), R_{LOAD}) = a_1 v_{IN}(t) + a_2 v_{IN}^2(t) + a_3 v_{IN}^3(t) + \dots \quad (2.3)$$

---

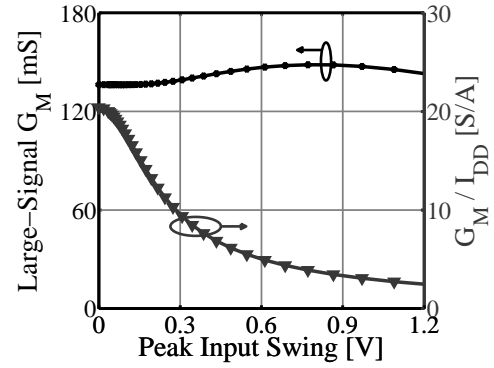
<sup>3</sup>The class-AB cell is able to maintain this constant  $G_M$  by drawing more power and, therefore, the transconductance per unit current drops (also shown in Fig. 2.10(c)).



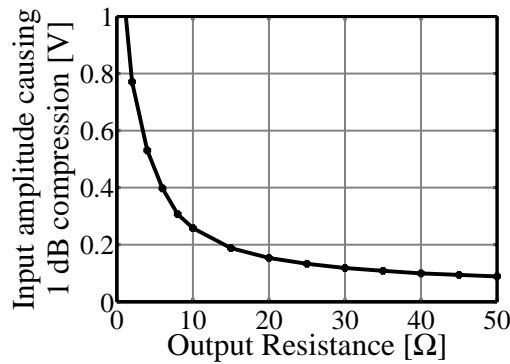
(a) Topology.



(b) Small-signal transconductance.



(c) Large-signal transconductance.



(d)  $P_{1dB}$  compression point.

Figure 2.10: The class-AB transconductance (plots assume  $R_{LOAD}=0$ ).



A standard method to specify the relative 3<sup>rd</sup>-order coefficient is in terms of the amplitude ( $V_{P1dB}$ ) of the sinewave input that causes  $G_M$  (defined as Eqn. (2.2) but for non-zero  $R_{LOAD}$ ) to drop by 1dB compared to its small signal value of  $a_1$ . It is readily shown that

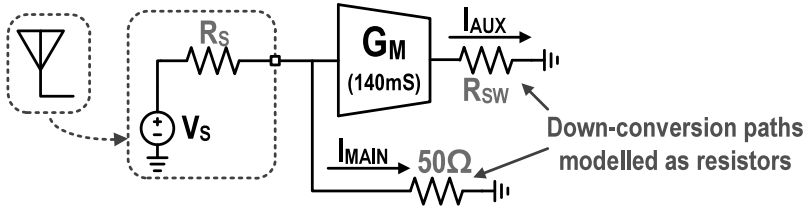
$$V_{P1dB} = \sqrt{0.145 \left| \frac{a_1}{a_3} \right|}. \quad (2.4)$$

Figure 2.10(d) plots the simulated  $V_{P1dB}$  versus  $R_{LOAD}$ , and shows that the dominant nonlinearity in  $i_{out}(t)$  arises from its dependence on  $v_{out}(t)$ .

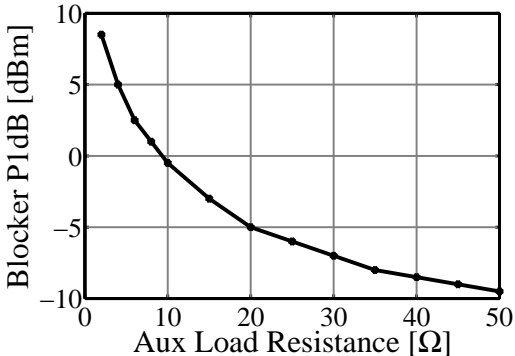
To get a sense of the achievable performance of this class-AB cell when embedded in the proposed receiver, the idealized test-bench of the receiver in Fig. 2.11(a) was simulated. The main path is modeled as an ideal  $50\Omega$  matching resistor, while the auxiliary downconversion path is also modeled as an ideal resistor. The output of the receiver is simply the weighted sum of both resistor currents, i.e.,  $I_{FTNC} = I_{AUX} - (G_M R_S) I_{MAIN}$ . As the main path is very linear (in this instance perfectly linear), the antenna-referred nonlinearity measurements of the receiver are better than the stand-alone class-AB transconductance. This test-bench does not model downconversion, and the only non-ideal component is the transconductance. The auxiliary resistor is then swept and the blocker performance assessed. In Fig. 2.11(b), the blocker power that causes 1dB of small-signal gain compression is plotted against the size of the load resistor. In the limit as the resistor becomes very small, the maximum allowed voltage on FET gate would have to be exceeded to reach the 1dB compression point. In order to tolerate a 0dBm blocker with only 1dB gain compression, an equivalent load resistor of less than  $10\Omega$  should be used. More importantly, with a  $10\Omega$  resistor, the NF only degrades very slightly in the presence of a 0dBm blocker (Fig. 2.11(c)). Degradation in the noise figure for a blocker greater than 0dBm can be attributed to the following: as  $G_M$  compresses, the circuit departs from the optimum noise-cancelling condition and the noise contribution of  $R_{MAIN}$  is no longer completely nulled. The reduced output impedance of the transconductance when the NMOS/PMOS transistors are forced into triode can also result in a non-negligible noise contribution of  $R_{AUX}$ .

Since downconversion is not modeled, this NF plot only shows the effect of gain compression, but not of reciprocal mixing with LO phase noise nor of noise in subsequent baseband

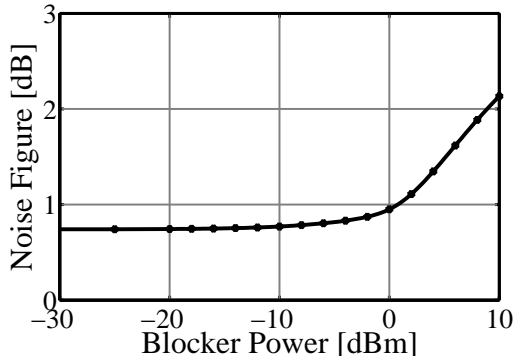
stages. However, we can conclude that the class-AB transconductance is sufficiently linear for the proposed blocker-tolerant receiver.



(a) Ideal FTNC-RX testbench.



(b) Blocker  $P_{-1dB}$  versus the auxiliary load resistance.



(c) Blocker noise figure assuming  $R_{SW}=10$ .

Figure 2.11: Limitation of the class-AB transconductance on the large-signal linearity of the FTNC-RX.

## 2.5 Oversampling Mixers

The design of the mixers is critical to the performance of the receiver. An ideal mixer multiplies an incoming RF signal with a complex LO sinusoid, which frequency shifts the wanted channel to DC. As shown in Fig. 2.12, a conventional I/Q hard-switched mixer approximates the complex sinusoid by two square waves that are offset by 90 degrees, however, this approximation results in the aliasing of signals around the  $-3^{\text{rd}}$ ,  $5^{\text{th}}$  and  $-7^{\text{th}}$  harmonic and so on. Although attenuated relative to the wanted frequency, this unwanted signal folding is unacceptable for a true wideband receiver. Of course, this folding also applies to noise, and will limit the NF to 0.9dB because of antenna noise folding alone.

The conventional I/Q mixer can be viewed as a multiplication of the RF signal with a complex sinewave that is sampled-and-held at twice the Nyquist frequency. Therefore, to shift these aliasing terms to higher frequencies, the sampling rate must be further increased. For instance, if the LO waveform is sampled-and-held at eight times the receive frequency (as was first done in [30,31]), the first alias is moved to  $-7^{\text{th}}$  harmonic and is attenuated by 17dB relative to the wanted signal (see Fig. 2.13). The conversion loss and the minimum achievable noise figure also improves to 0.2dB. This oversampling, while necessary in a wideband receiver, does come at the cost of an increased burden on LO generation circuitry.

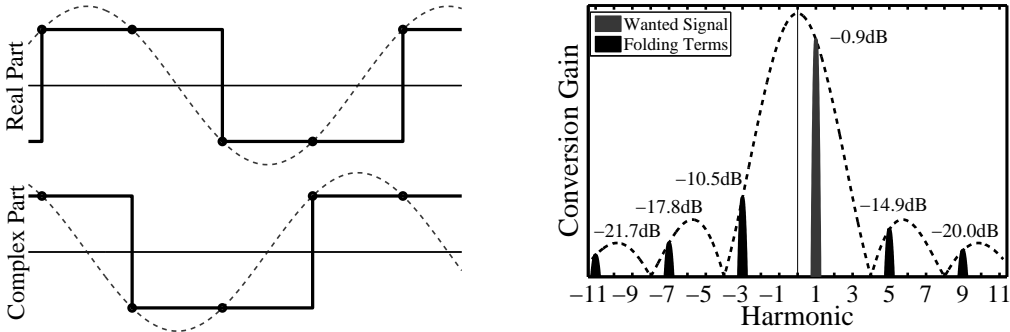


Figure 2.12: Traditional 50% I/Q mixer: LO approximation and aliasing terms.

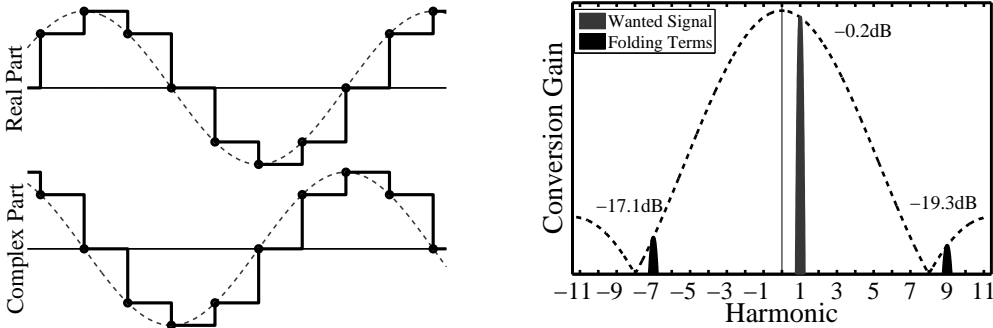


Figure 2.13: Oversampling I/Q mixer: LO approximation and aliasing terms.

In this work, the oversampling mixer is realized using the passive-mixer based approach [12, 13] shown in Fig. 2.14. An RF current is first downconverted by  $M$  mixer switches driven by non-overlapping clocks,  $sw(t - x/(MT))$ ,  $x \in [0, \dots, M - 1]$ . The downconverted currents are then converted to voltages, appropriately weighted and then

summed. The output of this process is given by

$$v_{OUT}(t) = i_{RF}(t) \sum_{x=0}^{M-1} K_x sw \left( t - \frac{x}{MT} \right), \quad (2.5)$$

which is the RF current multiplied by the summation of the product of the complex weighting constants,  $[K_0, \dots, K_{M-1}]$ , and their the associated clock pulse. These constants can be chosen such that summation generates a sampled version of an ideal complex sinusoid, which becomes the effective LO that downconverts the incoming RF signal. For example, by setting

$$K_x = |G_{ARB}| \left( \cos \left( \frac{2\pi x}{M} - \angle G_{ARB} \right) - j \sin \left( \frac{2\pi x}{M} - \angle G_{ARB} \right) \right) \quad \text{for } x = 0, 1, \dots, M - 1, \quad (2.6)$$

an oversampled complex LO with an arbitrary magnitude of  $|G_{ARB}|$  and an arbitrary phase of  $-\angle G_{ARB}$  will downconvert the RF signal. In the frequency domain, the output around baseband is given by:

$$V_{OUT}\{\Delta\omega\} = G_{ARB} \sum_{g=-\infty}^{\infty} \text{sinc} \left( \frac{1 - gM}{M} \pi \right) I_{RF}\{(1 - gM)\omega_{LO} + \Delta\omega\}, \quad (2.7)$$

where  $G_{ARB} = |G_{ARB}|e^{j\angle G_{ARB}}$  can be considered an arbitrary baseband gain,  $\omega_{LO}$  is the clock frequency and  $\Delta\omega$  is some carrier offset. Therefore, as well as receiving the wanted signal around  $\omega_{LO} + \Delta\omega$ , signals at offset of integer multiplies of  $M$  will also be downconverted. To limit this effect, this work chooses  $M = 8$ .

A nice feature of this approach is that by using the same clock pulses, but simply changing the baseband weighting constants, an arbitrary complex periodic waveform can be generated (see two such waveforms on right-hand side of Fig. 2.14). This is extremely useful in the proposed noise-cancelling receiver because it allows for the correction of phase (and magnitude) variations between the two downconversion paths without employing two separate LO chains, as discussed in more detail in Sec. 2.8.2 and chapter 3.

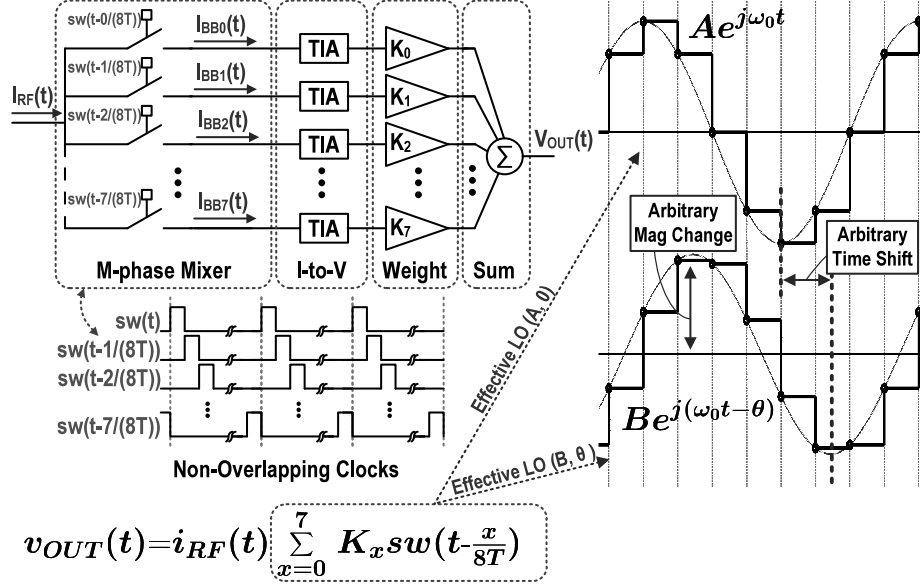


Figure 2.14: An oversampling downconversion mixer employing an 8-phase LO. By changing the baseband weighting constants, an effective LO with any arbitrary magnitude or phase can be realized. Two examples of possible LO waveforms are shown.

## 2.6 Simplified Noise Analysis

A detailed noise analysis of the proposed receiver requires a mathematically involved LTV-based analysis, which is described fully in chapter 3. In this section, only a qualitative overview of the noise performance is given and, where appropriate, results from chapter 3 are referred to.

The complete receiver model is shown in Fig. 2.15. The main path consists of a matching resistor ( $R_{IN}$ ), an  $M$ -phase passive mixer and a bank of baseband TIAs. The auxiliary path is the  $G_M$ -cell, another  $M$ -phase mixer, and another bank of TIAs. The I/Q signals are constructed from the TIA outputs. To simplify matters, we assume that the RF node is purely resistive and that the  $G_M$ -cell has an infinite output impedance. The TIAs are modeled as shown in Fig. 2.16. Assuming the I-V gain of each TIA is large (which is equivalent to a large receiver gain), we can ignore the noise contribution of the feedback resistors and model the noise of each op-amp as a voltage source that appears in series with each TIA. The mixer switches, which are NMOS transistors, are modeled as ideal

switches with some finite series resistance,  $R_{SW}$ . Like the mixer-first receiver [8], matching is provided by the impedance looking into the main path [32] and is given by:

$$Z_{IN}\{\omega_{LO} + \Delta\omega\} \approx R_{IN} + R_{SW} + \frac{1}{M}\text{sinc}^2\left(\frac{\pi}{M}\right) Z_{BB}\{\Delta\omega\}, \quad (2.8)$$

where  $Z_{BB}\{\Delta\omega\}$  is the input impedance of each baseband TIA. The gain of receiver is difference between the auxiliary and main paths and is given by:

$$\begin{aligned} A_{FTNC} &= A_{AUX} - A_{MAIN} \\ &= -\left(\frac{G_M G_{AUX}(R_{IN} + R_{SW} + Z_{BB}\{\Delta\omega\}/M) + G_{MAIN}}{R_{IN} + R_{SW} + R_S + Z_{BB}\{\Delta\omega\}/M}\right) \left(\text{sinc}\left(\frac{\pi}{M}\right)\right), \end{aligned} \quad (2.9)$$

where  $G_{MAIN}$  and  $G_{AUX}$  are, respectively, the baseband gain of main and auxiliary paths<sup>4</sup>. In chapter 3, the output noise due to the matching resistance is found to be

$$\overline{v_{out}^2} = \left| \frac{G_M G_{AUX} R_S - G_{MAIN}}{R_{IN} + R_{SW} + R_S + Z_{BB}\{\Delta\omega\}/M} \right|^2 \overline{v_{R_{IN}}^2}. \quad (2.10)$$

By appropriately setting the relative gain of the two paths, i.e.  $G_{MAIN} = G_{AUX} G_M R_S$ , the noise of this matching resistor is cancelled, but the input signal is preserved. In the case of perfect matching, i.e.  $R_S = Z_{IN}$ , this optimum noise-cancelling condition occurs when the absolute voltage gain of the main and auxiliary paths are equal, but 180° out of phase. The noise associated with the mixer switches appears in series with the matching resistor, exhibits an identical transfer function to the output as the matching resistor noise and, so, can also be nulled.

As discussed, the main-path amplifier noise is modeled as a noise source in series with the TIA input. Much like the upconversion of DAC and filter noise in an upconversion mixer [32], this low-frequency noise will be up-converted by the passive mixer to RF at the input node. This up-converted noise will then be suppressed via the auxiliary path. Indeed, the normalized transfer function of such a noise source to the output is identical to that of the matching resistor and the passive mixer switch noise sources and is given by:

$$\overline{v_{out}^2} = \left| \frac{G_{AUX} G_M R_S - G_{MAIN}}{R_{IN} + R_{SW} + R_S + Z_{BB}\{\Delta\omega\}/M} \right|^2 \frac{\overline{v_{BB}^2}}{M}. \quad (2.11)$$

---

<sup>4</sup>Alternatively, these terms can be viewed as the gain of the oversampling mixers, i.e. equivalent to  $G_{ARB}$  in Sec. 2.5.

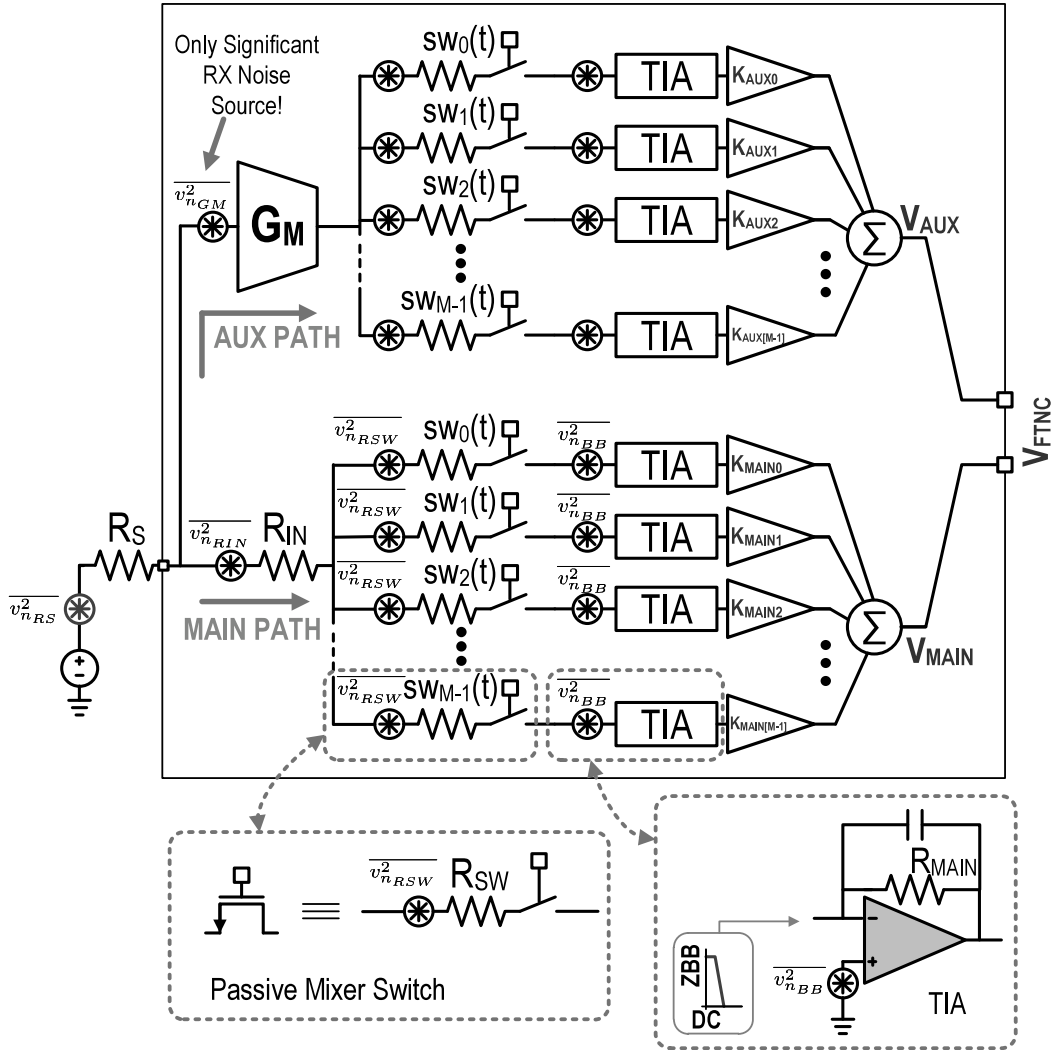


Figure 2.15: Simplified FTNC-RX model highlighting main noise sources. All noise sources, with the exception of the  $G_M$  noise, can be nulled or contribute negligibly.

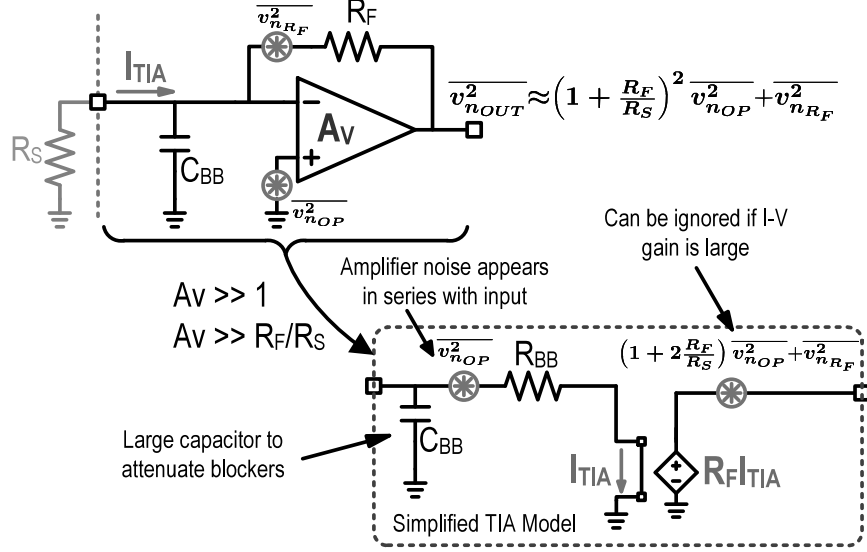


Figure 2.16: Simplified TIA model.

This noise is also nulled by setting  $G_{MAIN} = G_{AUX}G_MR_S$ . In the auxiliary path, if the output resistance of the  $G_M$ -cell is large, the noise associated with auxiliary mixer switches and the auxiliary op-amps will not contribute significantly to the total output noise. This is because the auxiliary TIAs are current driven, and since only one switch is on at any given time, the series voltage noise sources cannot generate a noise current. Therefore, when optimally configured, i.e.  $G_{MAIN} = G_{AUX}G_MR_S$ , the auxiliary transconductance is the only significant noise contributor and largely determines the receivers noise figure. Indeed, to a first order, the noise factor is given by

$$NF = \left( 1 + \frac{\overline{v_{GM}^2}}{\overline{v_{RS}^2}} \right) \frac{1}{\text{sinc}^2(\pi/M)}, \quad (2.12)$$

where  $\overline{v_{RS}^2}$  is antenna noise and, in the case of the class-AB transconductance,  $\overline{v_{GM}^2} = 4kT\gamma/G_M = 4kT\gamma/(g_{m_p} + g_{m_n})$ . If a large number of mixer phases are employed (i.e.  $M$  is large), the conversion gain of the passive mixers, which is given by the  $\text{sinc}^2(\pi/M)$  term in the above NF expression, approaches unity. Therefore, the noise factor can be made arbitrarily close to 1 by maximizing the size of the auxiliary transconductance. For instance, in this work  $G_M=120\text{mS}$  and  $M=8$ , which implies the theoretical noise figure is under 0.9dB.



Note that when the auxiliary path is powered down and noise cancelling is disabled, the receiver behaves like an equivalent mixer-first receiver and the NF is given by:

$$NF = \left( 1 + \frac{\overline{v_{R_{IN}}^2} + \overline{v_{R_{SW}}^2}}{\overline{v_{R_S}^2}} + \frac{\overline{v_{BB}^2}}{M\overline{v_{R_S}^2}} \right) \frac{1}{\text{sinc}^2(\pi/M)}. \quad (2.13)$$

If  $Z_{BB}\{\Delta\omega\}$  is small, matching requires that  $R_{IN} + R_{SW} = 50\Omega$  and the noise figure will be limited to 3dB. Even if this not the case and the up-converted TIA input impedance is used to provide matching, noise due to the baseband TIAs will contribute directly to the receiver's noise figure and flicker noise is likely to be significant. Flicker noise is not problematic when the auxiliary path is enabled as  $\overline{v_{BB}^2}$  will be cancelled.

## 2.7 Circuit Design

### 2.7.1 Receiver Topology

The complete schematic of the proposed noise-cancelling receiver, which was fabricated in 40nm CMOS, is shown in Fig. 2.17. The series resistance of the passive mixer switches ( $\approx 20\Omega$ ) and the up-converted input impedance of the main-path TIAs provide a  $50\Omega$  input resistance – an explicit matching resistor is not required. Due to the up-conversion of the TIA impedance, some very light filtering also occurs at the input of both passive mixers. In the auxiliary path, large passive mixer switches ensure that the out-of band impedance is small ( $\approx 15\Omega$ ), which in turn limits the RF voltage gain at the output of the transconductance.

The auxiliary class-AB transconductance is sized to give  $G_M=120\text{mS}$  and uses non-minimum length devices (70nm) to boost output impedance. A  $1/9^{\text{th}}$  scaled replica of this circuit with the input and output shorted generates the common-mode voltage, which biases the entire receiver close to the mid-rail voltage. This ensures that nominally zero DC current flows through the mixer switches and eliminates the need for large decoupling capacitors at the inputs of the passive mixers (similar to [33]). The outputs of the TIAs are appropriately weighted and summed with 16 separate 8-bit programmable  $G_M$  cells. These cells can

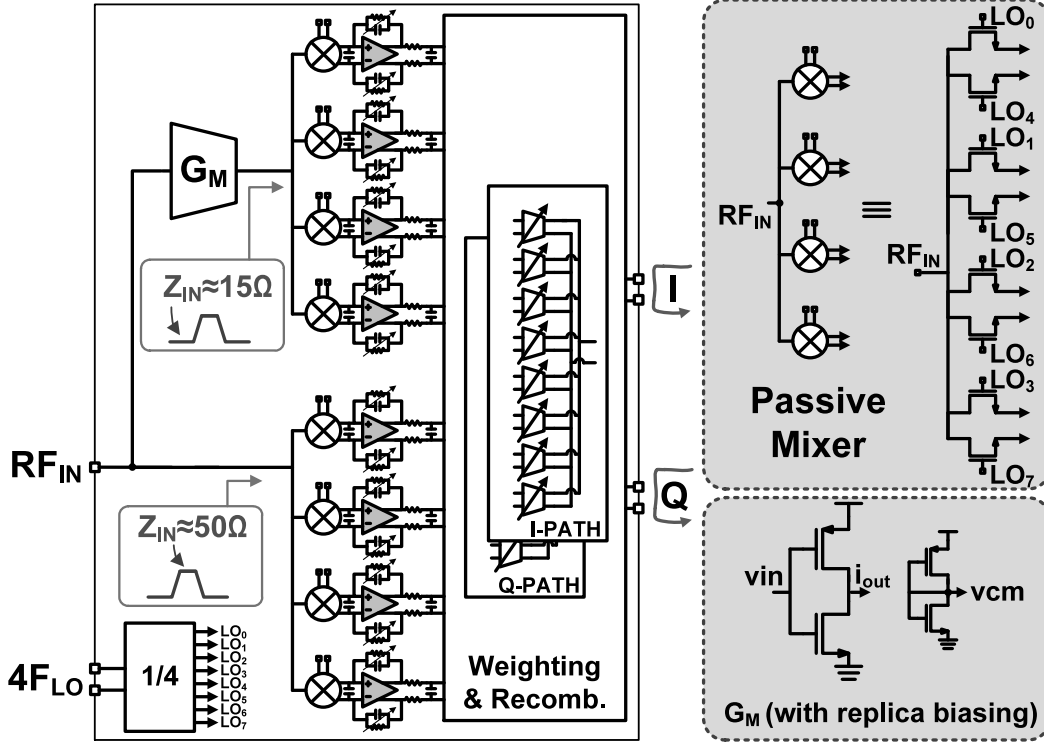
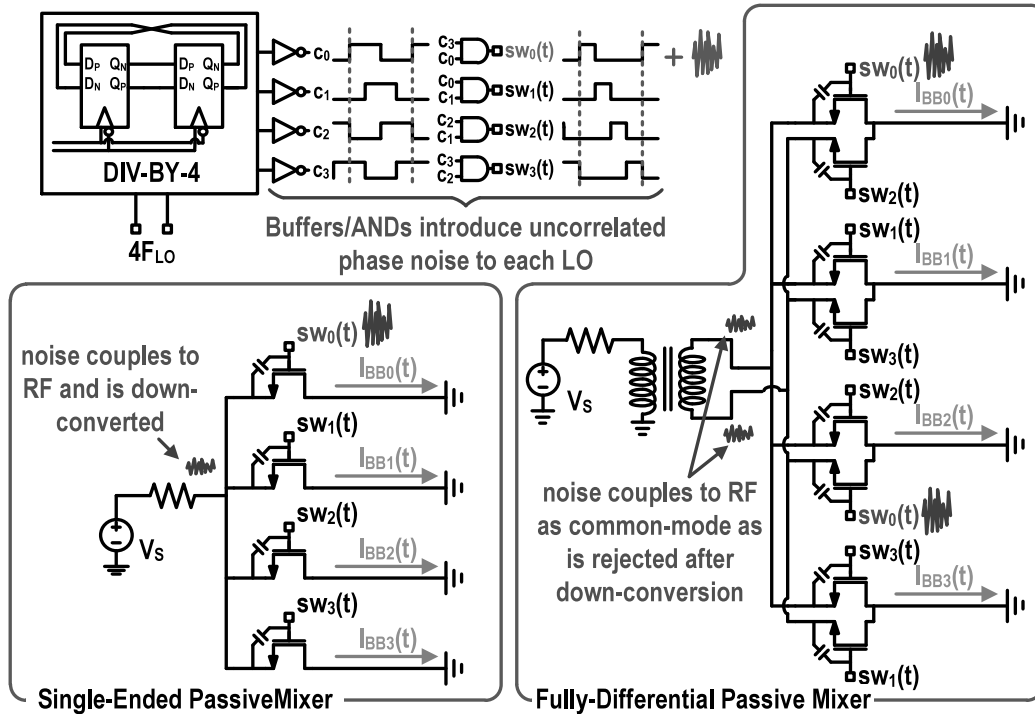


Figure 2.17: The complete frequency-translational noise-canceling receiver (FTNC-RX).

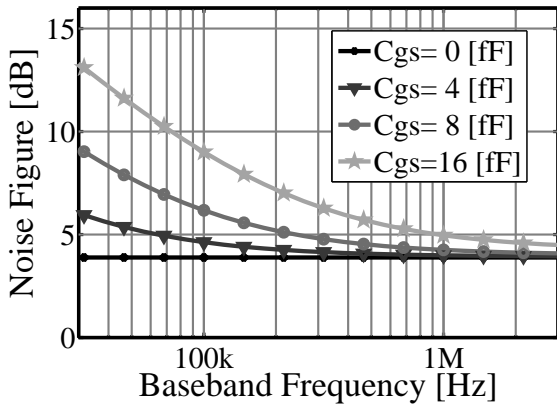
provide an arbitrary magnitude and phase shift between both downconversion paths. A divide-by-4 circuit generates the required eight-phase non-overlapping clock pulses.

### 2.7.2 Multiphase Clock Generation

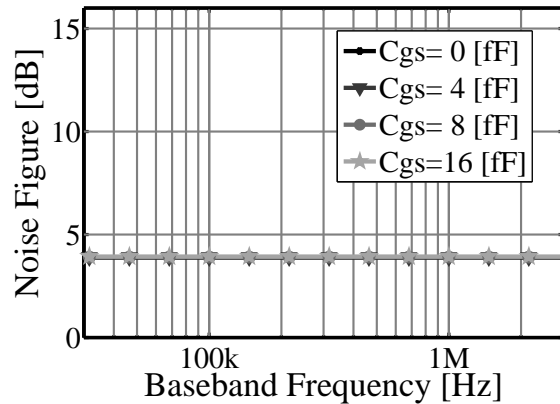
One of the advantages of the proposed topology is that it requires only a single RF input pin. However, this implies the use of single-ended passive mixers, which, as we will now explain, complicates the design of the LO chain. Consider the typical LO generation scheme shown in Fig. 2.18(a): a flip-flop based divider generates some required number of LO signals with 50% duty cycle clocks – a 4-phase scheme is shown for simplicity. These clocks are then buffered and AND’ed together to generate non-overlapping pulses. However, these logic gates will add phase noise to each clock pulse and, importantly, this noise is uncorrelated between differential pulses. Of particular interest is flicker noise in the logic gate transistors, which up-converts to the LO frequency when the clock transitions are not sharp.



(a) A single-ended and fully differential passive mixer driven with clocks containing uncorrelated phase noise.



(b) Simulated noise-figure of ideal single-ended mixer; noise figure is corrupted by LO-to-RF coupling of the LO phase noise.



(c) Simulated noise-figure of ideal fully-differential mixer; noise figure is uncorrupted by LO phase noise.

Figure 2.18: LO-to-RF noise coupling in passive mixers.

In a single-ended passive mixer, uncorrelated phase noise on a clock LO applied at the gate of a mixer switch couples onto the RF node through the gate-source capacitance, and is downconverted. Figure 2.18(b) plots the small-signal noise figure of an ideal mixer versus baseband frequency for different gate-source capacitance values that are typical of switches designed in 40nm CMOS. As the capacitance increases, the LO at the gate couples more strongly and the noise figure degrades. SpectreRF simulations show that this noise originates entirely in the buffers and the AND gates that follow the divider. The noise of the divider and buffers preceding the divider do not contribute, since this noise appears on differential LOs and couples onto the RF node at twice the receive frequency. Note this effect is *not* due to reciprocal mixing as no blocker is present. In a fully differential mixer, on the other hand, because each LO signal drives two mixer switches, the noise couples onto the differential RF input in common-mode, and is rejected after downconversion. Figure 2.18(c) plots the small-signal NF of a differential mixer, which, regardless of the gate-source capacitance value, is uncorrupted by LO-to-RF coupling.

Given this noise coupling mechanism, when using a single-ended passive mixer, we must lower the uncorrelated noise between differential LO pulses. To this end, the shift register-based (or Johnson) divider shown in Fig. 2.19 was employed. One register cell stores a logic HIGH, while all other registers store a LOW. Using external differential clocks at 4 times the receive frequency, this logic HIGH is moved along the register to generate the required 8-phase non-overlapping clocks. The novel register cell is designed with the following in mind: *a negative clock transition should propagate a HIGH present at the input, while a positive clock transition should always pull the output LOW*. The logic HIGH is propagated via the internal node  $Q_b$ . This node is pulled low by input  $D$  when the next output is HIGH, while inputs  $Q_{b+1}, \dots, Q_{b+4}$  pre-charge the internal node and enforce the condition that only one register outputs a HIGH at any given time. Importantly, this internal node only enables the pull-up PMOS transistor in the output stage and, so, the transistors to the left of  $Q_b$  ideally contribute no phase noise. The output of each cell is triggered by one of the high frequency clocks, and the same clock triggers differential register cells. This retiming limits the source of uncorrelated noise between differential clock pulses to the single

highlighted NMOS device, thereby limiting the deterioration in noise figure from LO-to-RF coupling. Because of retiming, the phase noise is also very low and was simulated at less than  $-172\text{dBc}/\text{Hz}$  at a  $80\text{MHz}$  offset from a  $1.5\text{GHz}$  carrier. The divider is functional from  $80\text{MHz}$  up to  $2.7\text{GHz}$  (limited by the capacitive load of the mixer switches), and consumes between  $3$  and  $36\text{mA}$ . Half this current is dissipated in the high frequency buffers.

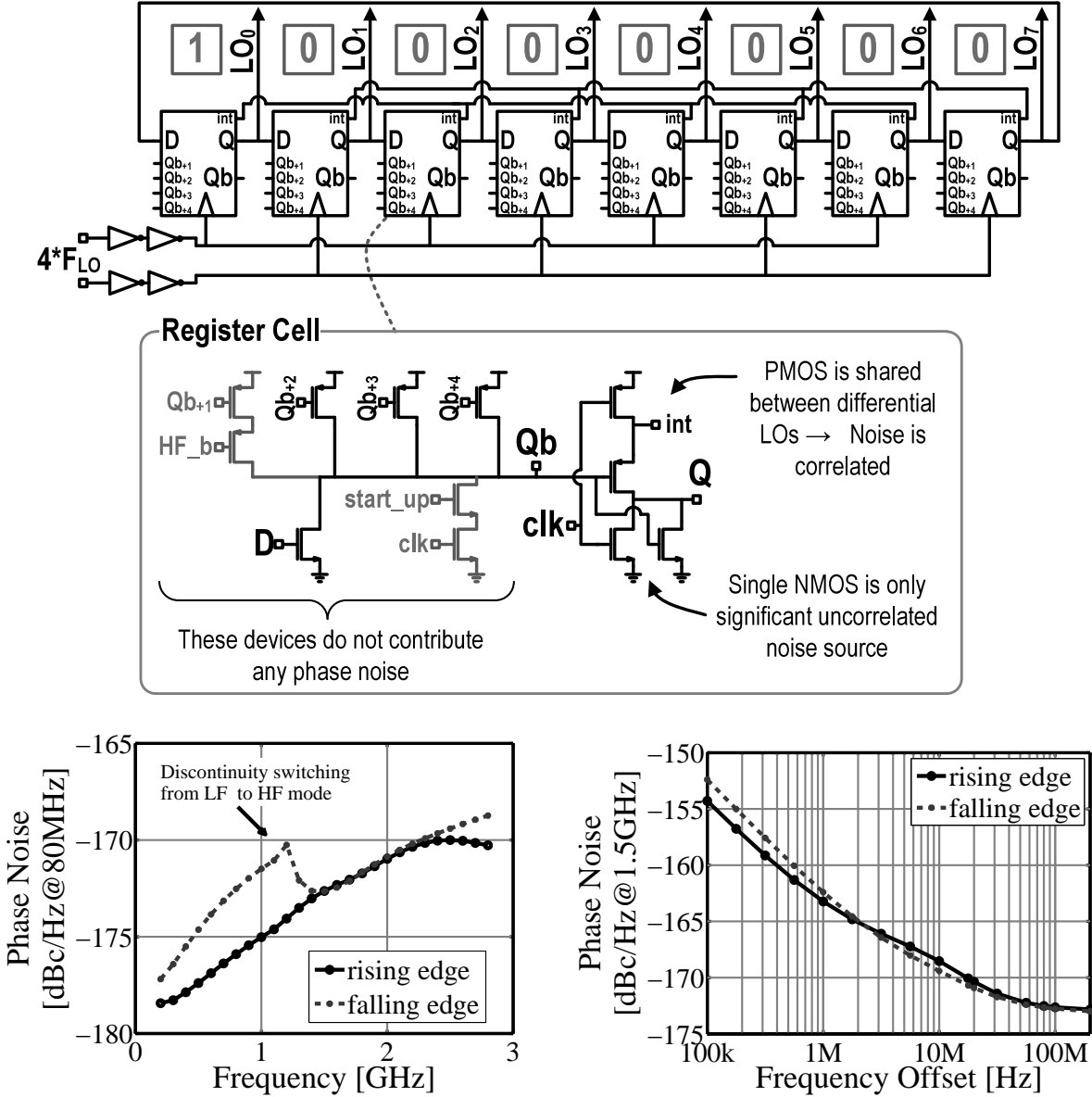


Figure 2.19: Johnson divider and associated simulation results.

### 2.7.3 Baseband TIAs

Figure 2.20 shows the circuit of the baseband TIA. Programmable feedback components set the RX bandwidth at around 2MHz. An additional  $RC$  pole follows the TIA, which further attenuates out-of-band blockers. A 3<sup>rd</sup> pole is provided by a large input capacitor at the TIA input. This prevents large blocker currents from entering the TIA.

The differential amplifier can be realized as a standard high-gain two-stage amplifier, but in this work a one-pole CMOS amplifier was used for two reasons. Firstly, since all the current is burned in one CMOS stage, its input-referred noise is much lower than in an equivalent two-stage amplifier that consumes the same power. This becomes important if the auxiliary path is powered down and noise cancelling is disabled, which can be done to save power. Secondly, the internal pole of a two-stage amplifier was found to be a source of degraded linearity at moderate carrier offsets. The amplifier is stabilized using the highlighted CMFB. This circuit functions as an active resistor (similar to [27]) with a large differential impedance, which preserves the differential gain, but a small common-mode impedance, which squelches common-mode gain.

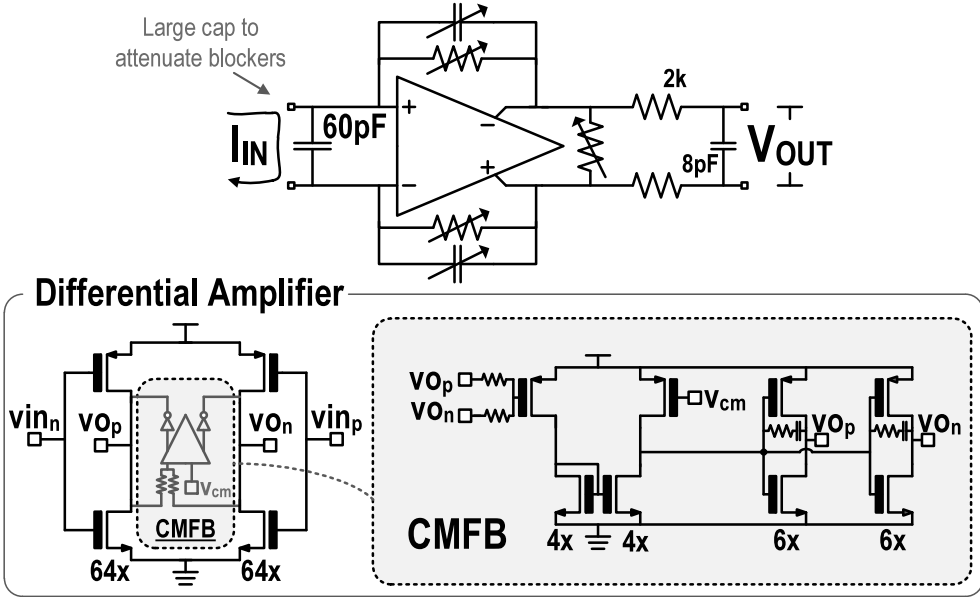


Figure 2.20: Baseband TIAs (component values reflect those used in main path TIAs).

## 2.8 Measurement Results

The die micrograph is shown in Fig. 2.21. The design occupies an active area of  $1.2\text{mm}^2$  in 40nm CMOS. Since an external signal generator is used in place of a VCO, no on-chip inductors are present.

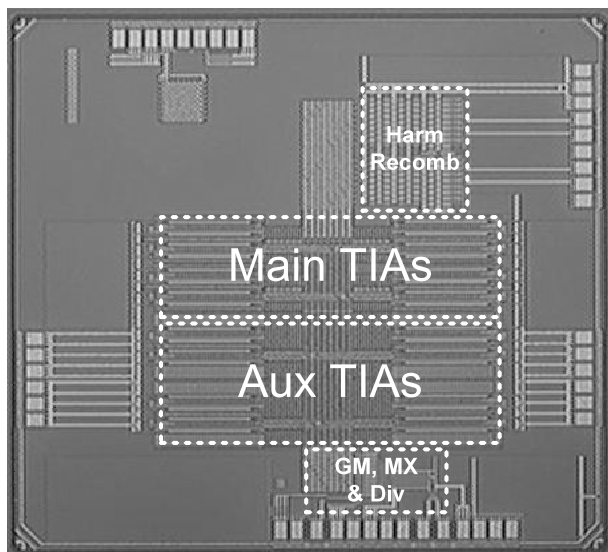
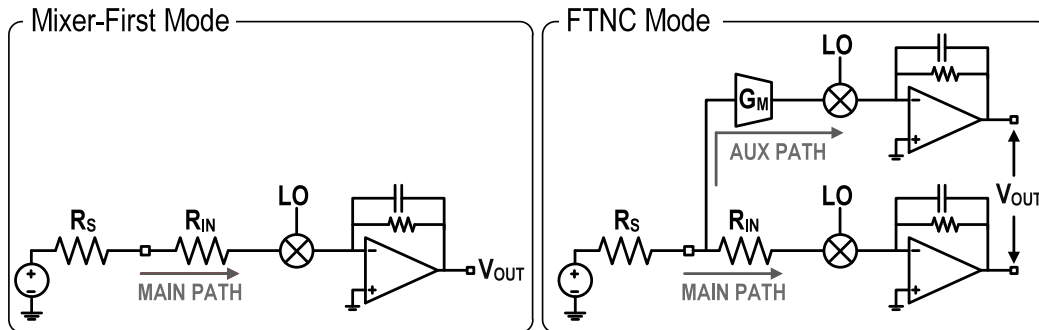


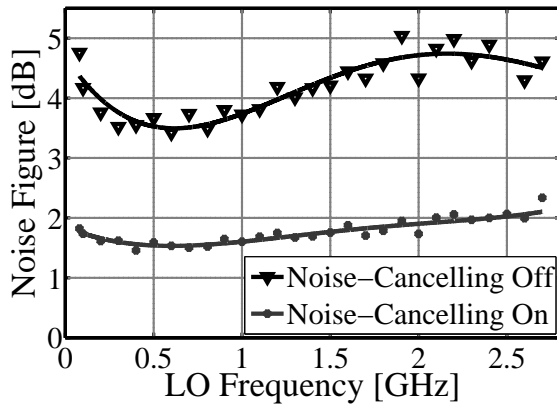
Figure 2.21: Die micrograph of single-ended FTNC-RX.

### 2.8.1 Noise Figure

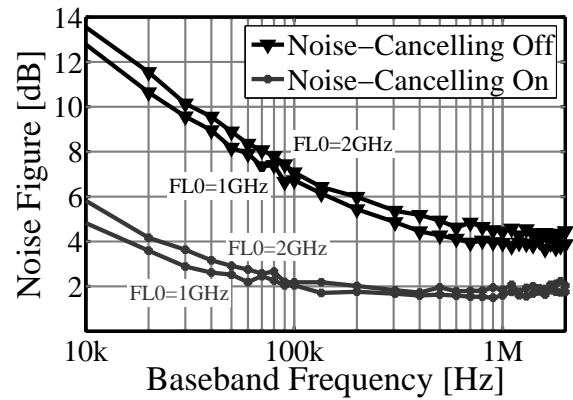
Figure 2.22 shows the measured receiver noise figure for two different modes of operation. In the first mode, the auxiliary path is powered down, no noise-cancelling takes place, and the receiver functions like any other mixer-first receiver. In this low power mode, the measured noise figure varies from 3.5dB at low frequencies to 5dB at 2GHz. Due to the contribution of the main-path TIAs, a flicker noise corner at more than 100kHz is visible. In the second-mode, the auxiliary path is powered up, noise-cancelling is enabled and the noise figure drops to 2dB or less across the entire band. Interestingly, the noise of the main-path TIA, which is up-converted to RF at the input node, is now suppressed by the auxiliary path and the flicker noise corner drops by 5X to below 20kHz.



(a) Modes of operation of the FTNC-RX.



(b) Measured noise figure versus receive frequency.



(c) Measured noise figure versus baseband frequency.

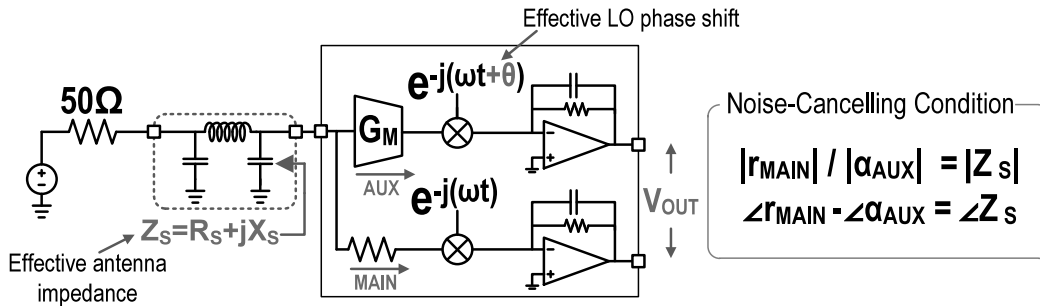
Figure 2.22: Measured noise figure of the FTNC-RX in two modes of operation.



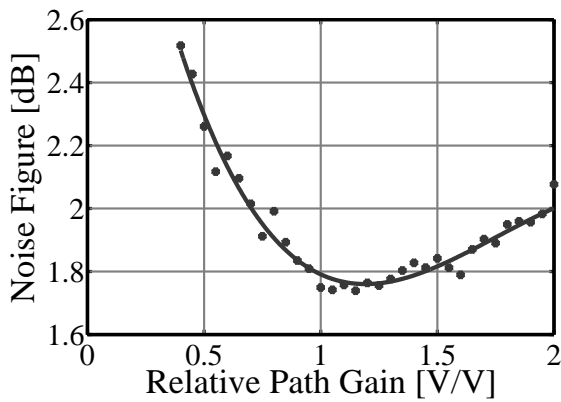
### 2.8.2 Noise Figure Optimization

In Sec. 2.6 we stated that the optimum noise-cancelling condition occurs when the current-to-voltage gain of the main path ( $r_{MAIN} = -G_{MAIN}$ ) divided by the voltage gain of the auxiliary path ( $\alpha_{AUX} = -G_M G_{AUX}$ ) is equal the antenna resistance ( $R_S$ ). However, this is a slight oversimplification: In the fabricated circuit, the RF node impedance is not completely real since device capacitance and bond wire inductance will effectively perform an impedance transformation on the  $50\Omega$  antenna. Accordingly, the noise-cancelling condition depends on the transformed antenna impedance,  $Z_S$ , which now has a reactive component [34]. Therefore, for best noise-suppression, the phase as well as the gain in both paths must be controlled. A standard noise-cancelling LNA cannot make such corrections, but because of the presence of mixers, our proposed receiver can. Gain correction is straightforward in the baseband, while the phase is corrected by introducing a phase difference between the effective LOs used in the two downconversions paths (see Fig. 2.23(a)). This is accomplished by changing the baseband weighting constants of the oversampling mixers as discussed in Sec. 2.5 and shown in Fig. 2.14. Note that only one LO generation path is still used, and that the phase shift is applied in the signal path, *not* in the LO path.

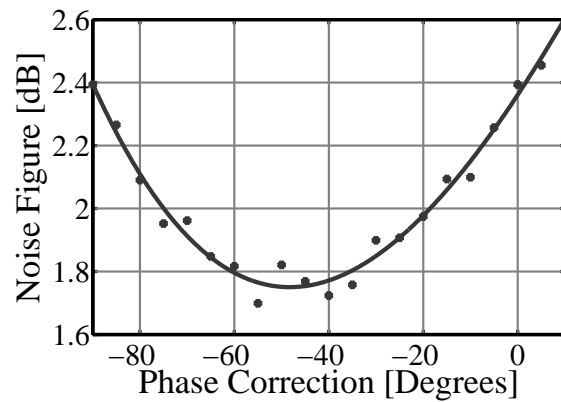
Figure 2.23(b) plots the measured noise figure at 2GHz for different relative gains. Clearly, there is a gain setting which optimizes noise figure. Figure 2.23(c) shows the measured noise figure versus phase correction in the auxiliary path. Again, there is optimum phase setting (around -45 degrees) which minimizes the noise figure. Without phase correction the noise figure would be worse by 0.6dB. Noise-cancelling is quite robust around the optimum point, and can tolerate variations in gain by  $\pm 20\%$  or phase by  $\pm 20^\circ$  without much change in noise figure. This suggests that phase and magnitude need only be calibrated at a few points across the receive band. As noise-cancelling is not particularly sensitive to mismatch between the two paths, this also implies that the receiver will not be very sensitive to changes in antenna impedance. Nevertheless, unlike a standard noise-cancelling LNA, the receiver can be re-optimized, if needed, to compensate for changes in the antenna impedance as the receiver moves within its environment during operation.



(a) Optimum noise cancelling conditions depends on the effective antenna impedance.



(b) Measured effect of gain correction on noise figure.



(c) Measured effect of phase correction on noise figure.

Figure 2.23: Noise-cancelling optimization via baseband phase and magnitude correction.

### 2.8.3 Blocker Noise Figure

To measure the noise figure in the presence of a blocker, a small wanted signal at 1.5GHz was accompanied by a sine-wave blocker located 80MHz away. The magnitude of the blocker was then slowly increased. Figure 2.24 plots the resulting receiver gain and noise figure. Remarkably, the noise figure degrades to only 4.1dB in the presence of a 0dBm blocker. This excellent performance can be ascribed to two features. Firstly, all the nodes in the system experience little or no voltage gain at the blocker frequency and, therefore, gain compression is limited. Secondly, the divider exhibited very low phase noise, which keeps the deleterious effect of reciprocal mixing small.

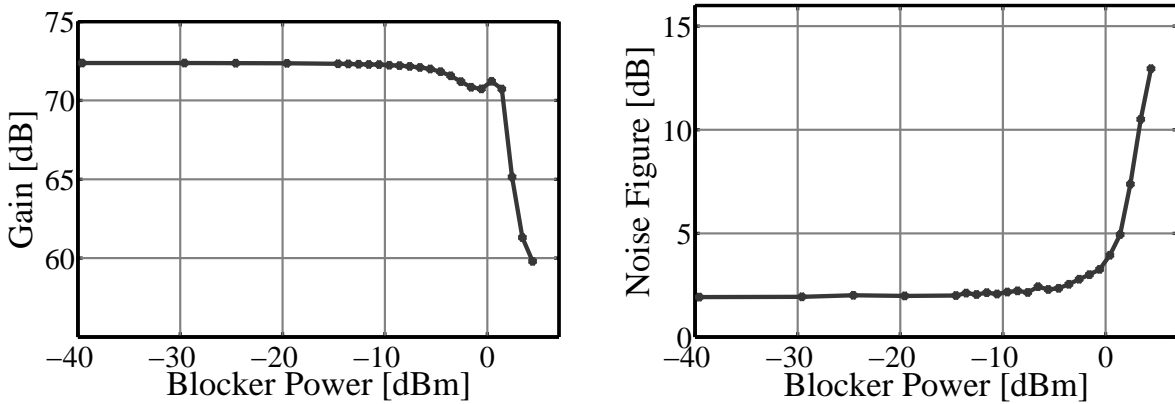
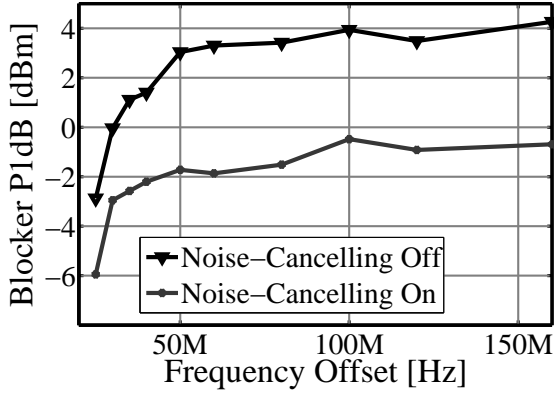


Figure 2.24: Measured receiver gain and noise figure assuming a wanted signal at 1.5GHz accompanied by a 1.58GHz continuous-wave blocker.

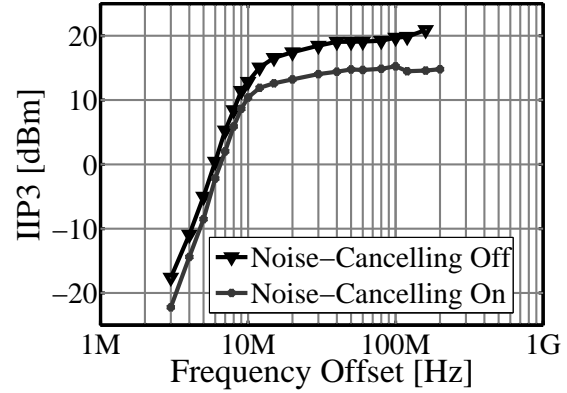
### 2.8.4 Linearity

Figure 2.25 shows the measured blocker  $P_{-1dB}$ , IIP3 and IIP2 all plotted against frequency offset from a 2GHz carrier at maximum gain. When noise cancelling is enabled, the out-of-band blocker  $P_{-1dB}$  is better than -2dBm, the out-of-band IIP3 is better than +13.5dBm and the out-of-band IIP2 is at least +54dBm. The out-of-band linearity is limited by distortion arising from non-zero voltage swing at the output of auxiliary  $G_M$  cell, while the degradation at in-band frequencies is due to distortion in the baseband circuits. If the auxiliary path is powered down and noise-cancelling is turned-off, the linearity improves

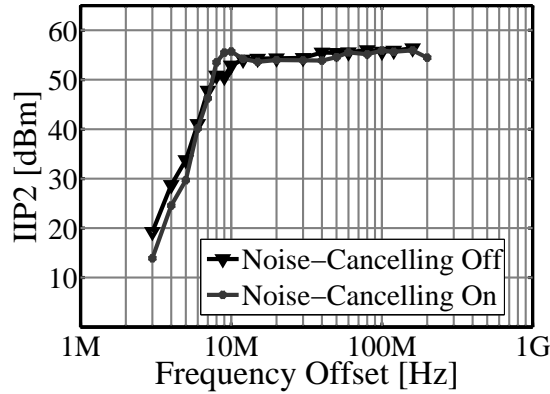
further.



(a) Measured blocker  $P_{1dB}$  with blocker located at  $f_{LO} + \Delta f$ .



(b) Measured IIP3 using two-tone test ( $f_1 = f_{LO} + \Delta f$ ,  $f_2 = f_{LO} + 2\Delta f - 800kHz$ ).



(c) Measured IIP2 using two-tone test ( $f_1 = f_{LO} + \Delta f$ ,  $f_2 = f_{LO} + \Delta f + 800kHz$ ).

Figure 2.25: Measured receiver linearity at  $f_{LO} = 2GHz$ .

### 2.8.5 Input Matching

When noise-cancelling is enabled, the  $s_{11}$  was measured at about -10dB across the receiver's passband, with a worst case of -8.8dB (Fig. 2.26). When the auxiliary path is powered down, the RF node capacitance is reduced and matching improves further.

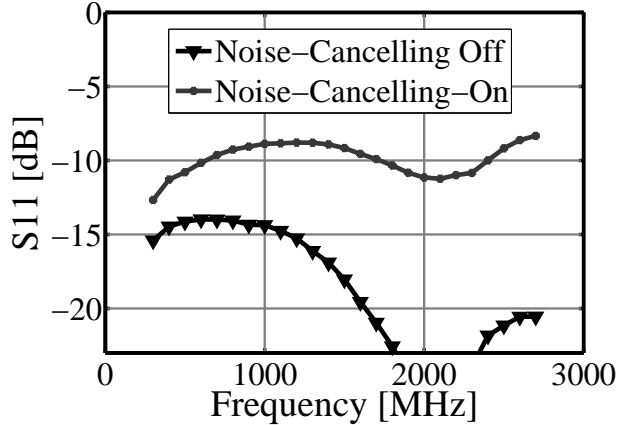


Figure 2.26: Measured S11.

### 2.8.6 Comparison with Prior Art

Table 2.1 compares the FTNC-RX prototype with other recently published blocker-tolerant receivers. The first two works are wideband receivers [7, 9–11], while the third work is a state-of-art SAW-less narrowband receiver [23, 24]. Even when compared to the narrowband receiver, the FTNC-RX shows improved effective small-signal noise figure, achieves comparable blocker performance, and consumes less battery current in the RX path.

When compared to the state-of-art wideband receiver [10, 11], the cascade small-signal noise figure, which must include any balun loss, improves from 4.4dB to 1.9dB, and the 0dBm blocker noise figure drops from 13dB to 4.1dB. This latter comparison is imperfect as [10, 11] assumes a 20MHz blocker, while our work assumes a 80MHz blocker and does not include the same degree of baseband filtering. In order for the FTNC-RX to tolerate a 20MHz blocker, increased baseband filtering will be required to limit the IF passband to 500kHz (similar to [10, 11]). Nevertheless, the results clearly show that blocker-tolerance does not have to come at the expense of small-signal noise figure. Additionally, this FTNC-RX has a single RF input, requires no external balun, and is immune to 3<sup>rd</sup> and 5<sup>th</sup> harmonic folding.

	ISSCC'10 [7, 9]	ISSCC'11 [10, 11]	ISSCC'11 [23, 24]	This Work
<b>Architecture</b>	Mixer-First	NC-LNA & voltage-sampling mixer	SAW-less narrowband	FTNC-RX
<b>RF Frequency [MHz]</b>	100-2400	400-6000	850/900/1800/1900	80-2700
<b>RF Input</b>	Single-Ended	Differential	Differential	Single-Ended
<b>Gain [dB]</b>	40-70	70	60	70
<b>NF@2GHz [dB]</b>	7	4.4*	4.1*	1.9
<b>0dBm Blocker NF [dB]</b>	-	13 (20MHz)	7 (80MHz)	4.1 (80MHz)
<b>3<sup>rd</sup>/5<sup>th</sup> Harmonic Rejection [dB]</b>	35.4/42.6 ( $f_{LO} < 1\text{GHz}$ Only)	No	No	42/45
<b>Out-of-band IIP3 [dBm]</b>	+25	+10	N/A	+13.5
<b>Active Area [mm<sup>2</sup>]</b>	2	2	1.4	1.2
<b>Supply Voltages [V]</b>	1.2/2.5	1.1/2.5	3.8	1.3
<b>RX Path Current** [mA]</b>	12	12	37	12
<b>CMOS Technology</b>	65nm	40nm	65nm	40nm

\*Includes assumed 1.2dB balun loss

\*\*Estimated Battery Current (excluding LOGEN), where  $I_{BATTERY} \approx I_{SUPPLY > 1.5V} + 0.5 \times I_{SUPPLY < 1.5V}$

Table 2.1: Comparison with recently published blocker-tolerant receivers

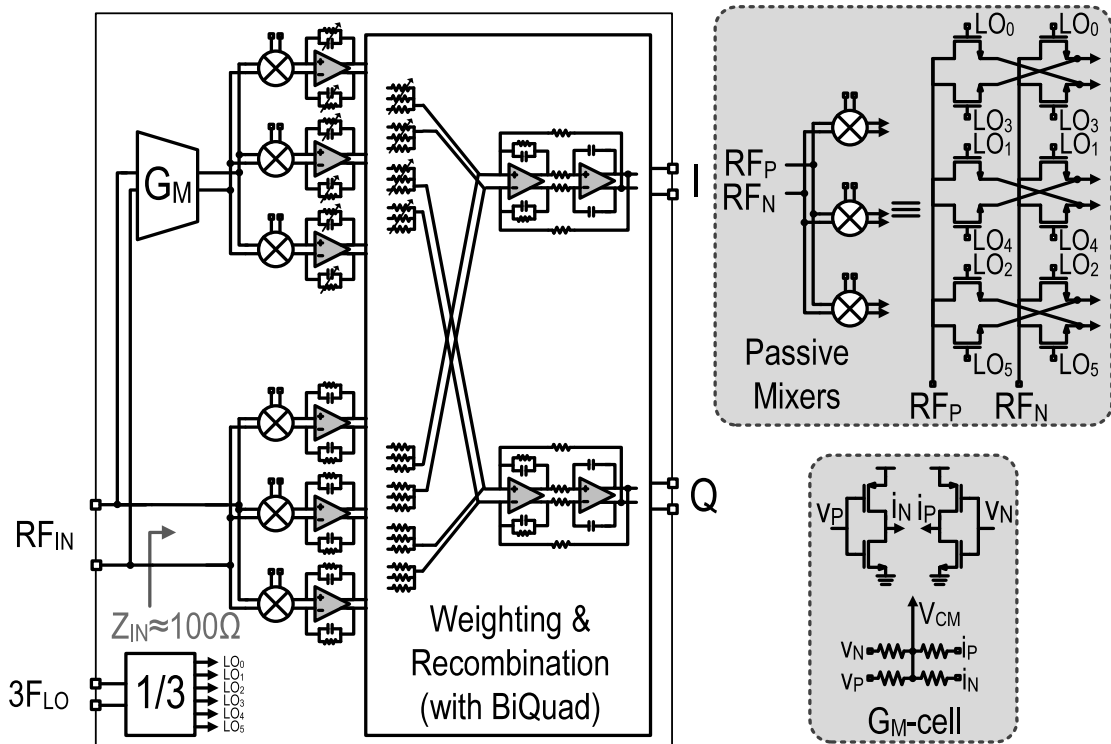
## 2.9 Fully-Differential FTNC-RX Design

A fully differential circuit requires an off-chip balun, which degrades NF and adds cost and board area. But it does offer improved common-mode rejection and higher IIP2. For these reasons, we have also realized the proposed FTNC-RX as a fully-differential circuit. This design, shown in Fig. 2.27(a), has a number of different features:

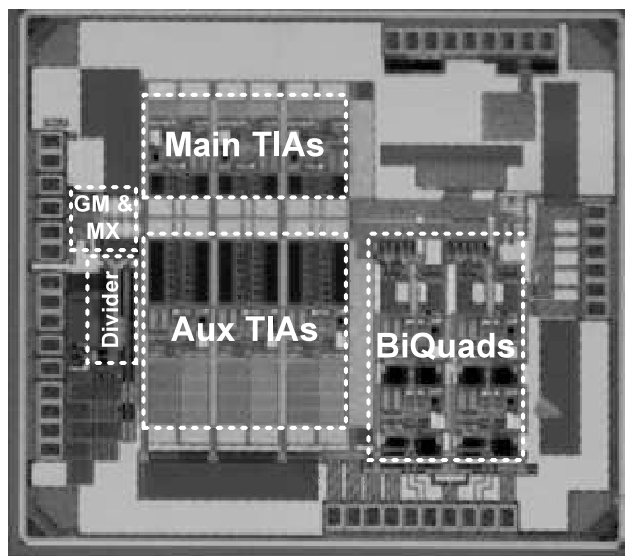
- The TIA outputs were combined using voltage-summing BiQuads, while standard two-stage, high-gain differential amplifiers were used in both the TIAs and BiQuads. This led to improved in-band linearity.
- 6-phase mixers were used as opposed to 8-phase mixers. This brought the first aliasing term down to the 5<sup>th</sup> LO harmonic, but reduced the capacitive burden on the LO chain.
- The divide-by-3 did not employ re-timing because LO-to-RF noise coupling is not problematic in a differential design (see Sec. 2.7.2).

The difficulty of finding an off-the-shelf practical wideband balun will ultimately limit the use of such a receiver, however, it is certainly suitable for SAW-less operation with moderate RF bandwidth. Another beneficial feature is that signals located at precisely  $2 \times f_{LO}$  are rejected before TIA amplification.

Figure 2.27(b) shows the die micrograph. Selected measurement results are plotted in Fig. 2.28. When noise-cancelling is disabled the NF is larger than in the single-ended design because the TIAs show larger input referred noise. However, with noise-cancelling enabled the NF drops to below 2dB. Despite a slightly improved blocker  $P_{-1dB}$ , the measured NF in the presence of a 0dBm blocker is worse than in the single-ended design because of higher divider phase noise. Table 2.2 compares the measured performance of the single-ended and fully-differential prototypes.



(a) Schematic.



(b) Die Micrograph.

Figure 2.27: The fully-differential FTNC-RX.



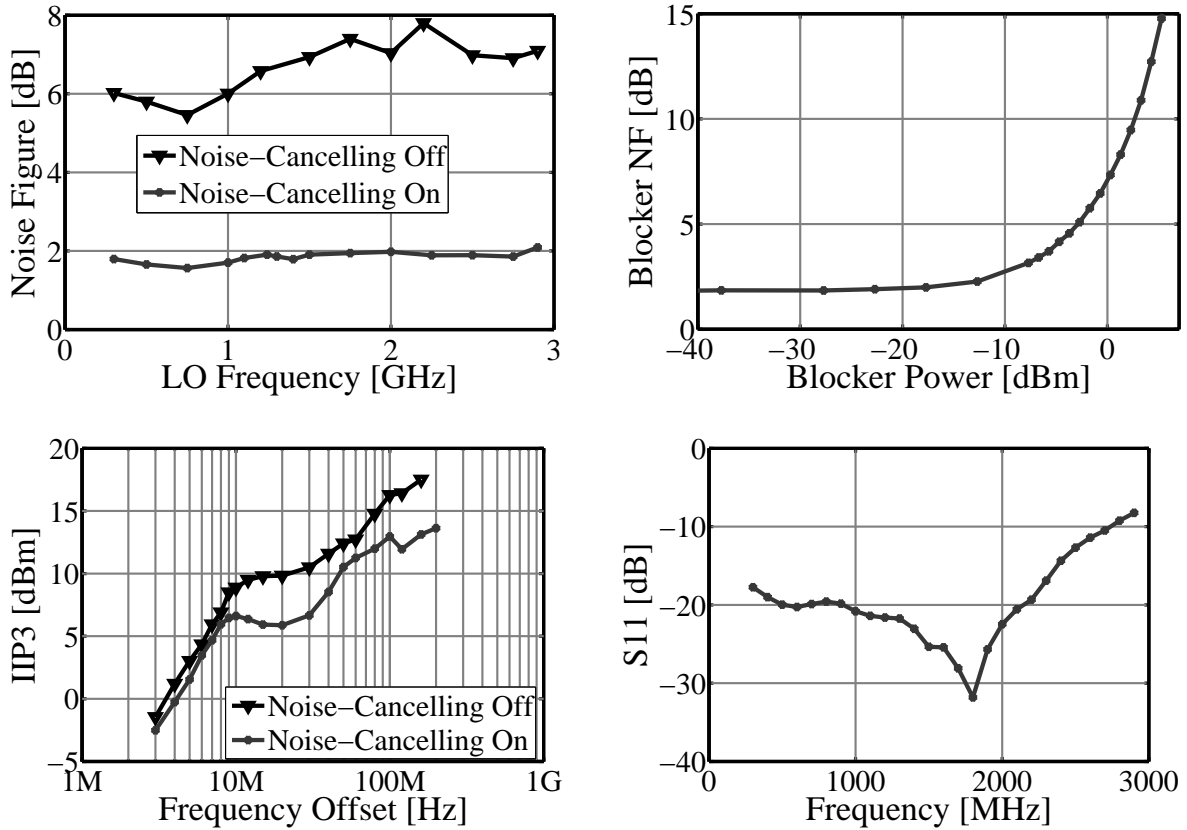


Figure 2.28: Measured noise figure, blocker noise figure, IIP3 and S11 for the fully-differential FTNC-RX prototype.

	<b>Singled-Ended FTNC-RX</b>	<b>Fully-Differential FTNC-RX</b>
<b>RF Frequency [MHz]</b>	80-2700	300-2900
<b>Gain [dB]</b>	70	58
<b>NF@2GHz [dB]</b>	1.9	1.9
<b>0 dBm Blocker NF [dB]</b>	4.1	7.2
<b>3<sup>rd</sup>/5<sup>th</sup> Harmonic Rejection [dB]</b>	42/45	43/No
<b>Out-of-band IIP3 [dBm]</b>	+13.5	+12
<b>Out-of-band IIP2 [dBm]</b>	+54	+68
<b>Active Area [mm<sup>2</sup>]</b>	1.2	1.1
<b>Supply Voltages [V]</b>	1.3	1.2/1.3/1.5
<b>Battery Current (excluding LOGEN) [mA]</b>	12	15
<b>CMOS Technology</b>	40nm	40nm

Table 2.2: Comparison between single-ended and fully-differential FTNC-RX prototypes

## 2.10 Conclusion

A new wideband, noise-cancelling receiver is introduced that employs two separate passive-mixer-based downconversion paths. By delaying noise-cancellation until after aggressive baseband filtering, it becomes possible to largely avoid voltage gain at blocker frequencies. Accordingly, the trade-off between noise, out-of-band linearity and wideband operation is significantly relaxed.

Single-ended and fully-differential prototypes of the proposed receiver have been fabricated. The single-ended design is blocker-tolerant, removes the balun requirement and does not compromise noise figure. State-of-the-art performance metrics, even compared to SAW-less narrowband designs, are reported.

## CHAPTER 3

# An LTV analysis of the Frequency-Translational Noise-Cancelling RX

### 3.1 Introduction

The standard noise cancelling LNA (NC-LNA) [5, 6] is able to provide both wideband impedance matching and a low noise figure. A conceptual model is shown in Fig. 2.6, which demonstrates how the noise of the matching resistor can be eliminated by taking a voltage measurement at the RF input *and* a measurement of the current flowing through the matching resistor. The problem with such an approach is that, in order to maintain a low noise figure, the output of both paths must be sensed differentially after significant voltage gain. Typical NC-LNA realizations apply this gain at RF frequencies and, so, any out-of-band blockers can easily desensitize the LNA. The frequency-translational noise-cancelling receiver (FTNC-RX) described in the previous chapter overcomes this limitation by employing two separate passive-mixer-based downconversion paths (Fig. 2.8). The RF node impedances (other than  $50\Omega$  node required for matching) are kept small, which prevents any RF voltage gain, while noise-cancelling only takes place after aggressive baseband filtering and, therefore, out-of-band blockers never experience any voltage gain and do not saturate the receiver (see Fig. 2.9).

Fundamental to operation of the FTNC-RX is the use of I/Q passive mixers prior to I-V conversion in the baseband. However, to first gain some insight into the noise performance of the system, let's ignore the mixers (or assume they are moved after the TIAs) and assume the amplifiers have infinite gain and bandwidth (as shown in Fig. 3.1). The result is a linear

time-invariant (LTI) system and, therefore, expressions for gain and NF are easily derived.

The gain of the receiver is

$$Av_{FTNC} = \frac{V_{OUT}}{V_{IN}} = \frac{G_M R_{AUX} R_{IN} + R_{MAIN}}{R_S + R_{IN}}, \quad (3.1)$$

while the noise figure is approximately given by

$$\begin{aligned} NF \approx 1 + & \left| \frac{G_M R_{AUX} (R_S + R_{IN})}{G_M R_{AUX} R_S + R_{MAIN}} \right|^2 \frac{\overline{v_{GM}^2}}{\overline{v_{RS}^2}} \\ & + \left| \frac{G_M R_{AUX} R_S - R_{MAIN}}{G_M R_{AUX} R_S + R_{MAIN}} \right|^2 \frac{\overline{v_{RIN}^2}}{\overline{v_{RS}^2}} \\ & + \left| \frac{G_M R_{AUX} R_S - R_{MAIN} - R_S - R_{IN}}{G_M R_{AUX} R_S + R_{MAIN}} \right|^2 \frac{\overline{v_{AMAIN}^2}}{\overline{v_{RS}^2}}, \end{aligned} \quad (3.2)$$

where  $\overline{v_{RS}^2}$ ,  $\overline{v_{AMAIN}^2}$ ,  $\overline{v_{RIN}^2}$  and  $\overline{v_{GM}^2}$  are the only significant noise contributors if the receiver gain is large. It is clear that the noise of the matching resistor can be cancelled if  $R_{MAIN} = G_M R_{AUX} R_S$ , while the noise of the main path amplifier will also be essentially nulled for the same condition if the receiver gain is large (i.e.  $R_{MAIN} \gg R_S + R_{IN}$ ). If this noise-cancelling condition is met, the receiver gain becomes  $Av_{FTNC} = G_M R_{AUX}$  and the noise figure becomes simply

$$NF \approx 1 + \frac{\overline{v_{GM}^2}}{\overline{v_{RS}^2}}. \quad (3.3)$$

Therefore, the noise figure can be minimized by minimizing  $\overline{v_{GM}^2}$ , which generally means maximizing  $G_M$ .

Now, the input and output ports of a passive mixer are reciprocal and, as a result, a passive mixer that downconverts an RF current flowing into one terminal, will also upconvert a baseband current flowing in the other terminal (and vice versa). Therefore, if the mixers are reintroduced into the model shown in Fig. 3.1, the RF currents will be downconverted to baseband before flowing into the TIAs, while the low frequency TIA noise will also be upconverted to RF. Indeed, if perfectly linear, unity gain passive mixers are used, the LTI model does capture the most important feature of the FTNC-RX, i.e., all noise sources are insignificant or can be nulled with the exception of  $\overline{v_{GM}^2}$ .

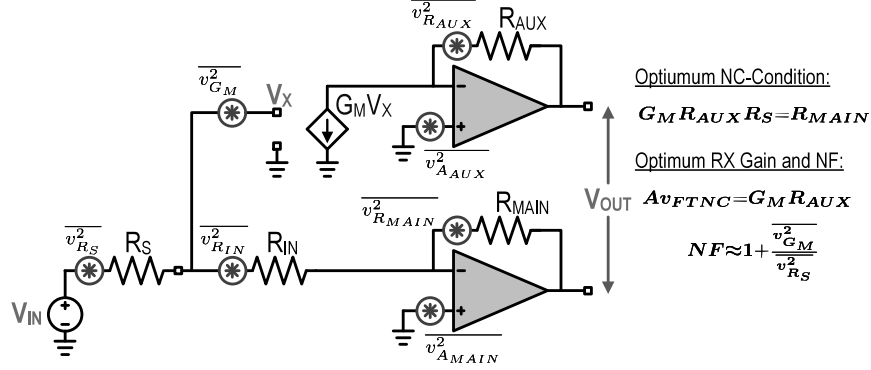


Figure 3.1: A simplified LTI analysis of the FTNC-RX.

Of course, this linear time-invariant (LTI) analysis ignores many of the frequency translational effects associated with non-ideal mixers. In reality, the passive mixers employed in the main and auxiliary paths, which are required for downconversion, will result in an infinite number of frequency shifting and folding terms that effect both wanted signals and noise. In this chapter, in order to capture such effects, the FTNC-RX is analyzed using a linear time-varying (LTV) approach. The approach presented is based on the LTV method used to analyze a variety of other circuits that utilize passive-mixers [35] [36] [32] [37] [38].

We begin by deriving expressions for the current-commutating passive mixer, and then use these expressions to characterize the gain and noise performance of the mixer-first receiver (or equivalently the main path of the FTNC). The auxiliary path is then characterized, which allows us to determine the performance of the complete FTNC-RX. This approach accounts for all frequency translational effects and, therefore, accounts for all signal and noise folding terms.

In order to gain some additional insight, the results are reconciled with the linearized model presented in [7] [9] [8]. A brief explanation of how the FTNC-RX can operate as a frequency-translational bandpass filters (FT-BPF) is also given.

### 3.2 Downconversion in an $M$ -phase Passive Mixer

As described in Sec. 2.5, the oversampling mixers in the FTNC-RX are realized using the passive-mixer based approach [12] shown in Fig. 2.14. A more detailed mathematical representation and derivation of this downconversion process is given here. As mentioned in Sec. 2.5, the output of this downconversion is given by

$$v_{OUT}(t) = i_{MX}(t) \sum_{x=0}^{M-1} K_x sw_x(t), \quad (3.4)$$

which is the RF current multiplied by the summation of the product of the complex weighting constants,  $[K_0, \dots, K_{M-1}]$ , and their the associated clock pulse  $[sw_0(t), \dots, sw_{M-1}(t)]$ . The complete a set of non-overlapping pulses being defined as

$$sw_x(t) = sw\left(t - \frac{xT}{M}\right), \quad (3.5)$$

where  $T = 2\pi/\omega_c$  is the clock frequency,  $x$  is the pulse number (i.e. 0, 1, ...,  $M - 1$ ) and  $sw(t)$  is the periodic waveform shown in Fig. 3.2, and defined as

$$sw(t) = \begin{cases} 1, & -T/(2M) < t < T/(2M) \\ 0, & \text{otherwise.} \end{cases} \quad (3.6)$$

The Fourier coefficients of this periodic waveform are given by

$$Sw[k] = \frac{\sin\left(\frac{k\pi}{M}\right)}{k\pi} = \frac{1}{M} \text{sinc}\left(\frac{k\pi}{M}\right), \quad (3.7)$$

and therefore the Fourier coefficients of the individual clock pulses is given by  $Sw_x[k] = Sw[k]e^{-j\frac{2\pi kx}{M}}$ .

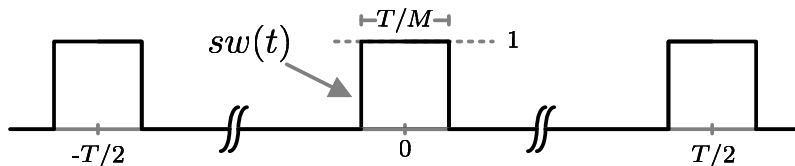


Figure 3.2: Time-domain representation of  $sw(t)$ .

The weighting constants can be chosen such that summation in Eqn. (3.4) generates a sampled version of an ideal complex sinusoid (with any arbitrary magnitude and any

arbitrary phase offset), which becomes the effective LO that is used to downconverted the incoming RF signal. For example, by setting

$$K_x = G_{ARB}e^{-j(\frac{2\pi mx}{M})} = |G_{ARB}|e^{-j(\frac{2\pi mx}{M} - \angle G_{ARB})} \quad (3.8)$$

an oversampled complex LO with a period of  $T/m$  will downconvert the RF signal. Typically, the signal around the LO frequency is required, which implies  $m = 1$ .  $|G_{ARB}|$  and  $\angle G_{ARB}$  are arbitrary constants which define the magnitude and phase of the LO. In the frequency domain, Eqn. (3.4) corresponds to the expression:

$$V_{out}\{\omega\} = \sum_{k=-\infty}^{\infty} I_{MX}\{\omega - k\omega_c\} \sum_{x=0}^{M-1} K_x Sw[k]e^{-j\frac{2\pi kx}{M}}, \quad (3.9)$$

where  $\omega_c$  is the fundamental of the LO waveform. Now the TIAs will invariably have a lowpass response and, therefore, the output around the baseband frequencies ( $\Delta\omega$ ) is the only concern:

$$V_{out}\{\Delta\omega\} = \sum_{k=-\infty}^{\infty} Sw[k]I_{MX}\{k\omega_c + \Delta\omega\} \sum_{x=0}^{M-1} K_x e^{j\frac{2\pi kx}{M}}, \quad (3.10)$$

where  $\Delta\omega \ll \omega_c$ . Substituting in the appropriate values for the weighting constants, the summation in Eqn. (3.10) simplifies to

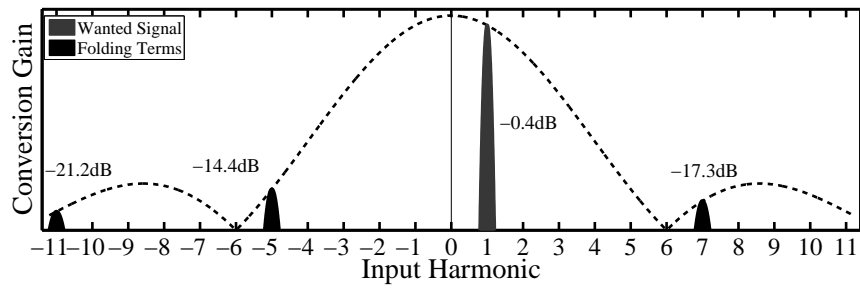
$$\begin{aligned} \sum_{x=0}^{M-1} K_x e^{j\frac{2\pi kx}{M}} &= G_{ARB} \sum_{x=0}^{M-1} e^{j(\frac{2\pi x(k-m)}{M})} \\ &= \begin{cases} M(G_{ARB}), & k = m - gM, g \in \mathcal{Z} \\ 0, & \text{otherwise} \end{cases} \end{aligned} \quad (3.11)$$

Therefore, the output (when the weighting constants are appropriately chosen to isolate the signal around the  $m^{\text{th}}$  harmonic) can be written as

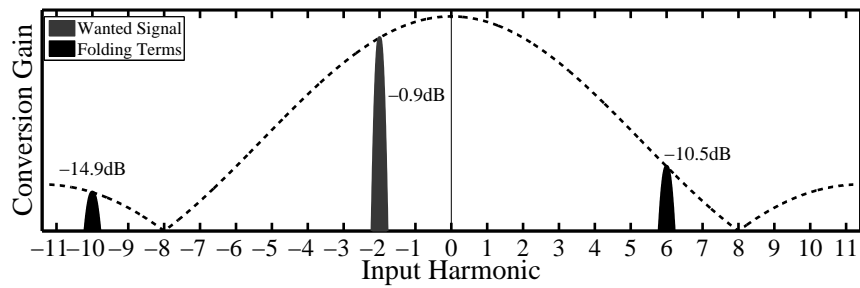
$$V_{OUT[m]}\{\Delta\omega\} = MSw[m]G_{ARB} \sum_{g=-\infty}^{\infty} \frac{Sw[m - gM]}{Sw[m]} I_{MX}\{(m - gM)\omega_c + \Delta\omega\}. \quad (3.12)$$

Thus, when receiving the fundamental ( $m = 1$ ), the nearest folding terms are  $1 - M$  and  $1 + M$ . Figure 3.3(a) shows the case of a 6-phase mixer, in which the weighting constants are chosen such that 1<sup>st</sup> harmonic is isolated (i.e.  $m = 1$ ,  $M = 6$ ), while Fig. 3.3(b) shows an example of an eight-phase mixer that is configured to receive a signal around the 2<sup>nd</sup> harmonic (i.e.  $m = -2$ ,  $M = 8$ ).





(a) Six-phase passive mixer configured to receive the USB signal around the 1<sup>st</sup> harmonic of  $f_{LO}$  ( $G_{ARB}=1$ ).



(b) Eight-phase passive mixer configured to receive the LSB signal around the 2<sup>nd</sup> harmonic of  $f_{LO}$  ( $G_{ARB}=1$ ).

Figure 3.3: Harmonic folding in the passive mixer.

### 3.3 Modeling the Passive Mixer

The previous section demonstrated the primary function of the passive-mixers used in this work, namely downconversion of an RF signal. With a view to quantifying gain and noise performance of the FTNC-RX, a more sophisticated physical model of the passive mixer is presented in this section. The analysis is the same as that used in [36] [32] [37] [38], but focuses on the results required for the FTNC-RX.

#### 3.3.1 The LTV Passive Mixer Model

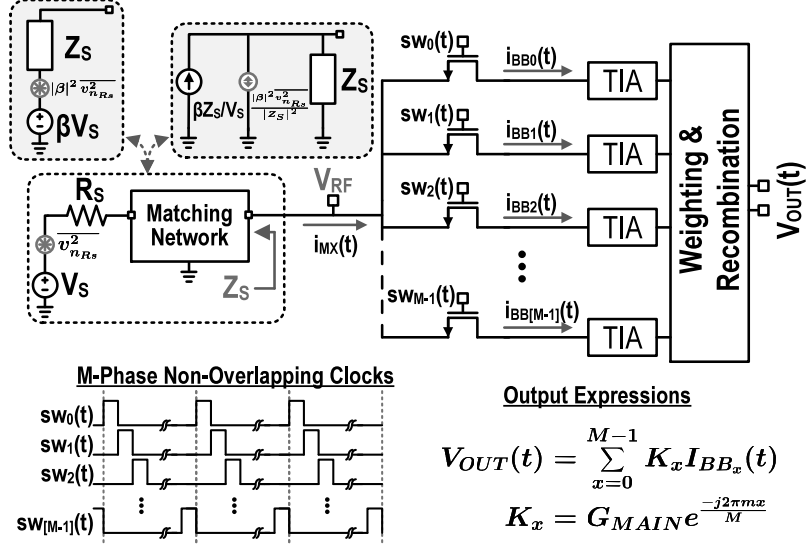
Consider the downconversion passive mixer shown in Fig. 3.4(a). The RF impedance and input signal can be modeled as either a Thevenin or Norton equivalent circuit. The primary noise sources are due to the load impedance, the baseband TIAs and the series resistance of each switch. The output of this downconversion mixer is the weighted recombination of the baseband currents ( $i_{BB_0}(t)$ ,  $i_{BB_1}(t)$ , ...,  $i_{BB_{M-1}}(t)$ ).

As shown in [36], the CMOS switches can be modeled as ideal switches with a common series resistance. Doing so introduces the non-physical (but mathematically useful) node  $V_P$  shown in Fig. 3.4(b). In the same figure, the implicit noise sources are represented with explicit voltage sources, i.e.  $V_{RSW}$  and  $V_{BB_0}$ ,  $V_{BB_1}$ , ...,  $V_{BB_{M-1}}$ . The noise performance of the system will be analyzed by deriving the transfer function from each of these sources to the output. Also shown in Fig. 3.4(b), the input impedance of the TIAs are modeled as baseband impedances  $Z_{BB_0}$ ,  $Z_{BB_1}$ , ...,  $Z_{BB_{M-1}}$ . The justification for modeling the TIAs in this way is given in Fig. 2.16.

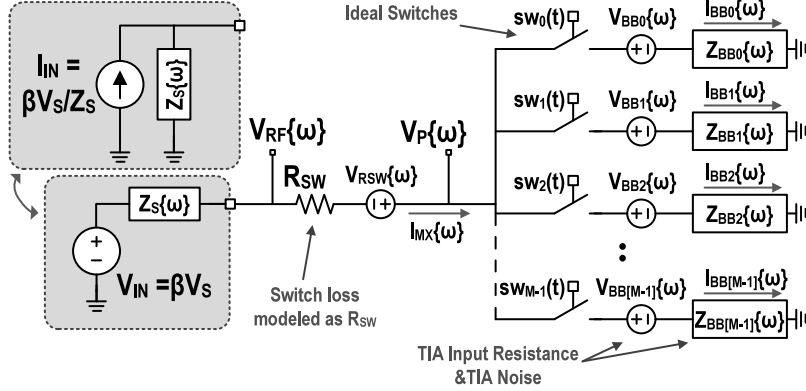
Since each switch is in series with a baseband voltage source, their positions can be swapped. Now, since only one switch is on at a time, these baseband voltage sources can be replaced with a single voltage source equal to

$$V_{BB_{RF}}\{\omega\} = \sum_{x=0}^{M-1} \sum_{k=-\infty}^{\infty} Sw_x[k]V_{BB_x}\{\omega - k\omega_c\}. \quad (3.13)$$

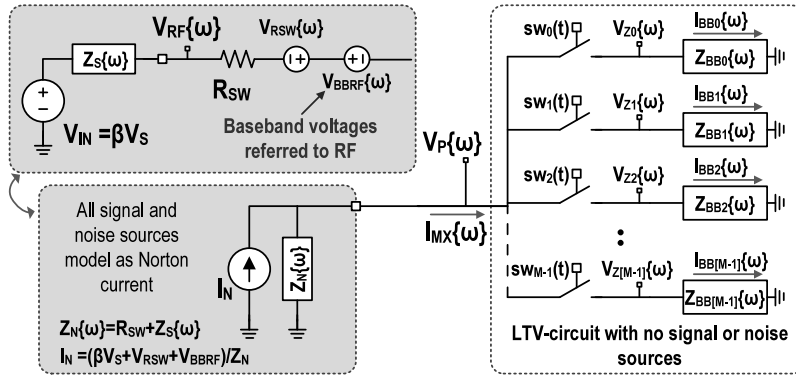
This is the same manipulation that was first performed during the analysis of the passive TX mixer [32]. The resulting circuit, shown in Fig. 3.4(c), can now be partitioned into an



(a) The schematic of the  $M$ -phase passive mixer.



(b) A simplified passive mixer model (weighted recombination of baseband currents is assumed, but not shown).



(c) Passive mixer decomposed into LTI and LTV portions. (Baseband voltage sources are referred to RF, baseband weighting and recombination is not shown.)

Figure 3.4: Modeling the  $M$ -phase passive mixer.

LTI circuit that can be easily modeled as Norton equivalent circuit and an LTV circuit that has no dependent or independent sources. This partition greatly simplifies the forthcoming analysis: Since every noise and signal source in the system can be referred to  $I_N$ , we need only calculate the transfer function from  $I_N$  to  $V_P$  in order to characterize the system. Although  $V_P$  is a non-physical node and the only output of interest is the recombined baseband currents, we will show that this current is easily derived from  $V_P$ . Additionally, it should be noted that since the baseband sources have been referred to the RF side of the side of the mixer, the baseband node voltages,  $V_{Z_x}$ , are also non-physical. However, in this work, the output is baseband current,  $I_{BB_x}$ , and baseband voltage is not sensed. Therefore, the introduction of these non-physical nodes does not affect the analysis.

### 3.3.2 Passive Mixer with Infinite Load Impedance

Referring to Fig. 3.4(c), we begin by solving  $V_P$  in terms of  $I_{MX}$ . This relationship is needed to solve the complete system, but is also equivalent to the condition when the mixer input is a high-impedance current source (i.e.  $Z_S$  in Fig. 3.4(b) is infinite, and  $I_{IN} = I_{MX}$ ). Using the approach outlined in [36], we note the following identities

$$\begin{aligned}
i_{BB_x}(t) &= i_{MX}(t)sw(t) \\
v_{Z_x}(t) &= z_{BB_x}(t) * i_{BB_x}(t) \\
v_P(t) &= \sum_{x=0}^{M-1} v_{BB_x}(t)sw_x(t),
\end{aligned} \tag{3.14}$$

and their Fourier transforms:

$$\begin{aligned}
I_{BB_x}\{\omega\} &= \sum_{k=-\infty}^{\infty} Sw_x[k]I_{MX}\{\omega - k\omega_c\} \\
V_{Z_x}\{\omega\} &= Z_{BB_x}\{\omega\}I_{BB_x}\{\omega\} \\
V_P\{\omega\} &= \sum_{x=0}^{M-1} \sum_{n=-\infty}^{\infty} Sw_x[n]V_{Z_x}\{\omega - n\omega_c\}
\end{aligned} \tag{3.15}$$

Using the above equations, and solving for  $V_P$  in terms of  $I_{MX}$  gives

$$V_P\{\omega\} = \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} I_{MX}\{\omega - (n+k)\omega_c\} \sum_{x=0}^{M-1} Sw_x[n]Sw_x[k]Z_{BB_x}\{\omega - n\omega_c\}. \tag{3.16}$$

Ultimately, we are concerned with the mixer's performance around specific harmonics of the LO. Accordingly, we can define  $V_P$  around the  $m^{\text{th}}$  harmonic (i.e.  $\omega = m\omega_c + \Delta\omega$ ) as

$$V_P\{m\omega_c + \Delta\omega\} = \sum_{k=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} I_{MX}\{(m-n-k)\omega_c + \Delta\omega\} \sum_{x=0}^{M-1} Sw_x[n]Sw_x[k]Z_{BB_x}\{(m-n)\omega_c + \Delta\omega\}. \quad (3.17)$$

Typically, a circuit is designed such that  $Z_{BB_x}$  is a lowpass impedance, i.e.  $Z_{BB_x}\{\omega\} \neq 0$ , only if  $\omega \approx 0$ . We will further assume that all the baseband impedances are identical. Therefore, the above expression can be written as:

$$V_P\{m\omega_c + \Delta\omega\} = \sum_{k=-\infty}^{\infty} Z_{BB}\{\Delta\omega\}I_{MX}\{k\omega_c + \Delta\omega\} \sum_{x=0}^{M-1} Sw_x[m]Sw_x[-k] \quad (3.18)$$

Now, the summation term  $\sum_{x=0}^{M-1} Sw_x[m]Sw_x[-k]$  is equal to  $M(Sw[m]Sw[-k])$  when  $k = m - gM$ ,  $g \in \mathcal{Z}$  and zero otherwise. Therefore,  $V_P$  in terms of  $I_{MX}$  is given by:

$$V_P\{m\omega_c + \Delta\omega\} = M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \times \sum_{g=-\infty}^{\infty} \frac{Sw[m-gM]}{Sw[m]} I_{MX}\{(m-gM)\omega_c + \Delta\omega\}. \quad (3.19)$$

The above expression is interesting. The fundamental (as well as harmonics) of  $I_{MX}$  down-convert to baseband and generate the baseband voltages. These baseband voltages are, in turn, sampled by the mixer and define the voltage  $V_P$ . As a result,  $V_P$  is not linearly related to  $I_{MX}$ , but depends on weighted and folded versions of  $I_{MX}$ . For instance, the voltage  $V_P$  around  $m\omega_c$  depends not only on  $I_{MX}$  around  $m\omega_c$ , but also the  $I_{MX}$  around  $(m \pm M)\omega_c$ ,  $(m \pm 2M)\omega_c$ ,  $(m \pm 3M)\omega_c$ , etc. An interesting result of this process, is that values of  $V_P$  around harmonics offset by  $M$  are completely correlated and are related as follows:

$$\frac{V_P\{(m-gM)\omega_c + \Delta\omega\}}{V_P\{m\omega_c + \Delta\omega\}} = \frac{Sw[(m-gM)]}{Sw[m]} = \frac{m(-1)^g}{m-gN} \quad (3.20)$$

If the RF impedance is not infinite, these voltages at higher order harmonics will induce additional RF currents, which will be downconverted and alter  $V_P$  around the fundamental [36]. Therefore, when analyzing the complete system, the RF load impedance must be accounted for.

### 3.3.3 Passive Mixer with Finite Load Impedance

As mentioned in the previous section, because of frequency translational effects, the load impedance has a significant effect on the performance of the passive mixer. Referring to Fig. 3.4(c), since the LTI portion of the model is characterize using an Norton equivalent model, we may write

$$I_N\{\omega\} = I_{MX}\{\omega\} + \frac{V_P\{\omega\}}{Z_N\{\omega\}}. \quad (3.21)$$

And, therefore  $V_P$  can be written as

$$\begin{aligned} V_P\{m\omega_c + \Delta\omega\} = & + M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \sum_{g=-\infty}^{\infty} \left( \frac{Sw[m-gM]}{Sw[m]} \right) I_N\{(m-gM)\omega_c + \Delta\omega\} \\ & - M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \sum_{g=-\infty}^{\infty} \left( \frac{Sw[m-gM]}{Sw[m]} \right) \frac{V_P\{(m-gM)\omega_c + \Delta\omega\}}{Z_N\{(m-gM)\omega_c + \Delta\omega\}} \end{aligned} \quad (3.22)$$

Employing the identity defined in Eqn. (3.20), the above equation simplifies to

$$\boxed{V_P\{m\omega_c + \Delta\omega\} = \frac{M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \sum_{g=-\infty}^{\infty} \left( \frac{Sw[m-gM]}{Sw[m]} \right) I_N\{(m-gM)\omega_c + \Delta\omega\}}{1 + M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \sum_{g=-\infty}^{\infty} \frac{|Sw[m-gM]|^2}{|Sw[m]|^2} \frac{1}{Z_N\{(m-gM)\omega_c + \Delta\omega\}}} } \quad (3.23)$$

Although Eqn. (3.23) is clumsy, it can be used to completely characterize the performance of the mixer. All signal and noise sources have already been mapped into the Norton equivalent circuit. The voltage  $V_{RF}$  can be determined from  $V_P$ , while it is shown in Sec. 3.4.2 that when the downconverted currents are weighted and recombined, they dependent solely  $V_P$  and some arbitrary gain constant. To better understand this expression, lets define the following:

$$\begin{aligned} Z_{MX}\{m\omega_c + \Delta\omega\} &= M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} \\ \frac{1}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}} &= \sum_{g=-\infty}^{\infty} \frac{\frac{|Sw[m-gM]|^2}{|Sw[m]|^2}}{Z_N\{(m-gM)\omega_c + \Delta\omega\}} \end{aligned} \quad (3.24)$$

The mixing action up-converts the low-pass baseband impedances to the RF impedance,  $Z_{MX}$ , which has a *bandpass* characteristic. In addition, the mixing action effectively frequency translates weighted versions of the Norton equivalent load impedance seen around

higher harmonics. This causes a reduction in the effective load impedance from  $Z_N$  to  $Z_{NFOLD}$ . Using a different approach, [7] [9] [8] modeled this same additional loss with a shunt impedance  $Z_{sh}$ , where  $Z_{NFOLD} = Z_N || Z_{sh}$ . Given this notation, voltage  $V_P$  is now written as:

$$V_P\{m\omega_c + \Delta\omega\} = I_{NFOLD}\{m\omega_c + \Delta\omega\}(Z_{MX}\{m\omega_c + \Delta\omega\} || Z_{NFOLD}\{m\omega_c + \Delta\omega\}) \quad (3.25)$$

where the “folded” Norton current is given by

$$I_{NFOLD}\{m\omega_c + \Delta\omega\} = \sum_{g=-\infty}^{\infty} \frac{Sw[(m - gM)]}{Sw[m]} I_N\{(m - gM)\omega_c + \Delta\omega\} \quad (3.26)$$

In [7] [9] [8], a linearized model was introduced, which is useful for visualizing signal, noise and impedance folding. Although the analysis presented here is different to that work, the resulting expressions are equivalent and, therefore, we can utilize their linearized model. Assuming we are only interested in the  $V_P$  around the  $m^{\text{th}}$  harmonic, Eqn. (3.25) can be represented using the LTI model shown in Fig. 3.5(a). The model can also be re-drawn to explicitly show the original signal and noise sources as shown in Fig. 3.5(b).

As the number of mixer phases increases the folding effects (which are generally unwanted and deleterious to performance) become less pronounced. In the limit as  $M$  becomes very large, folding effects can be completely ignored and therefore:

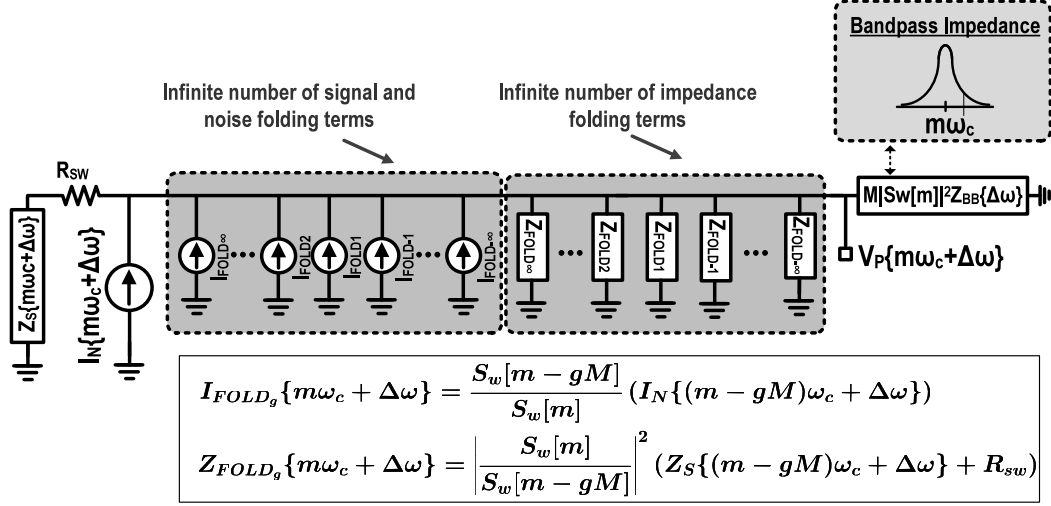
$$\lim_{M \rightarrow \infty} V_P\{m\omega_c + \Delta\omega\} = \left( \frac{Z_{BB}\{\Delta\omega\}}{M} || Z_N\{m\omega_c + \Delta\omega\} \right) I_N\{m\omega_c + \Delta\omega\} \quad (3.27)$$

Now, of course,  $V_P$  is a non-physical node voltage, and we ultimately want to calculate either  $V_{RF}$ ,  $I_{BB_e}$  or, in the case of the FTNC-RX, both. These outputs as a function of  $V_P$  are derived in the next section.

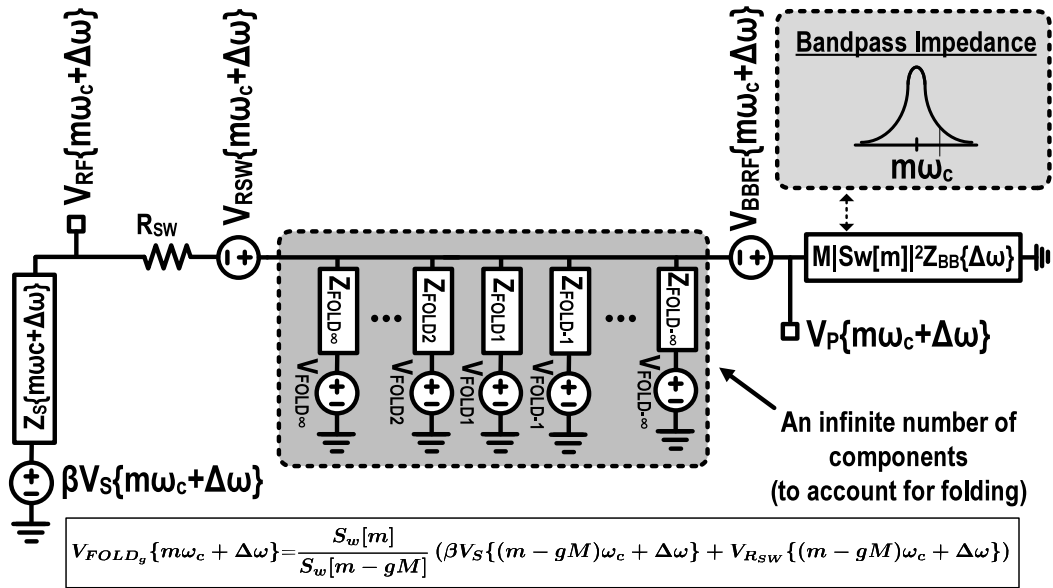
## 3.4 Relating the Passive Mixer to the FTNC-RX Outputs

### 3.4.1 Output of the Complete FTNC-RX

Referring to Fig. 3.6, the output of the FTNC receiver is the difference between the recombined baseband currents in the auxiliary path, and the recombined baseband currents in



(a) LTI model with Norton equivalent current.



(b) LTI model with explicit voltage sources.

Figure 3.5: Linear time-invariant (LTI) model around  $m^{\text{th}}$  harmonic.



the main path. This can be expressed as:

$$V_{FTNC[m]}{\Delta\omega} = V_{AUX[m]}{\Delta\omega} - V_{MAIN[m]}{\Delta\omega}, \quad (3.28)$$

where the subscript  $m$  corresponds to the harmonic that receiver is configured to receive. The value of  $m$  is changed by changing the weighting constants in the recombination circuitry. In most practical cases, the receiver is required to downconvert signals around the fundamental and therefore  $m$  will be equal to 1.

The goal is to find expressions for  $V_{AUX}$  and  $V_{MAIN}$  in terms of both the input signal and the noise sources in the system.

### 3.4.2 Output of the Main Path

The output of the main path of the FTNC receiver is simply the output of a mixer-first receiver. Assuming the baseband weighting constants are chosen appropriately in order to isolate the  $m^{\text{th}}$  harmonic, Eqn. (3.12) and Eqn. (3.19) can be combined to define the output in terms of  $V_P$ :

$$V_{MAIN[m]}{\Delta\omega} = \frac{MSw[m]G_{MAIN}}{Z_{MX}\{m\omega_c + \Delta\omega\}}V_P\{m\omega_c + \Delta\omega\}, \quad (3.29)$$

where  $G_{MAIN}$  is the recombination gain of the baseband circuitry (equivalent to  $G_{ARB}$  of the oversampling mixer defined by Eqn. (3.8)). Therefore, once  $V_P$  is calculated, the down-converted and recombined current can be easily deduced. Combining the above equation with Eqn. (3.25), the output of the main path due to the Norton current is calculated as:

$$V_{MAIN[m]}{\Delta\omega} = G_{MAIN}\alpha\{m\omega_c + \Delta\omega\}I_{NFOLD}\{m\omega_c + \Delta\omega\}, \quad (3.30)$$

where

$$\alpha\{m\omega_c + \Delta\omega\} = \frac{MSw[m]Z_{NFOLD}\{m\omega_c + \Delta\omega\}}{Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}}. \quad (3.31)$$

### 3.4.3 Output of the Auxiliary Path

In the auxiliary path, the node voltage  $V_{RF}$  drives a conductance,  $G_M$ . The output current of this conductance is then downconverted by a current-commutating passive mixer, and

the resulting baseband currents are recombined. Assuming the output impedance of the conductance is very large (relative to the auxiliary switch impedance and upconverted auxiliary TIA impedance), downconversion will be close to ideal, and we can write:

$$V_{AUX[m]}{\Delta\omega} = -MSw[m]G_{AUX}G_M \sum_{g=-\infty}^{\infty} \frac{Sw[m-gM]}{Sw[m]} V_{RF}\{(m-gM)\omega_c + \Delta\omega\}, \quad (3.32)$$

where  $G_{AUX}$  is the recombination gain of the baseband circuitry in the auxiliary path.

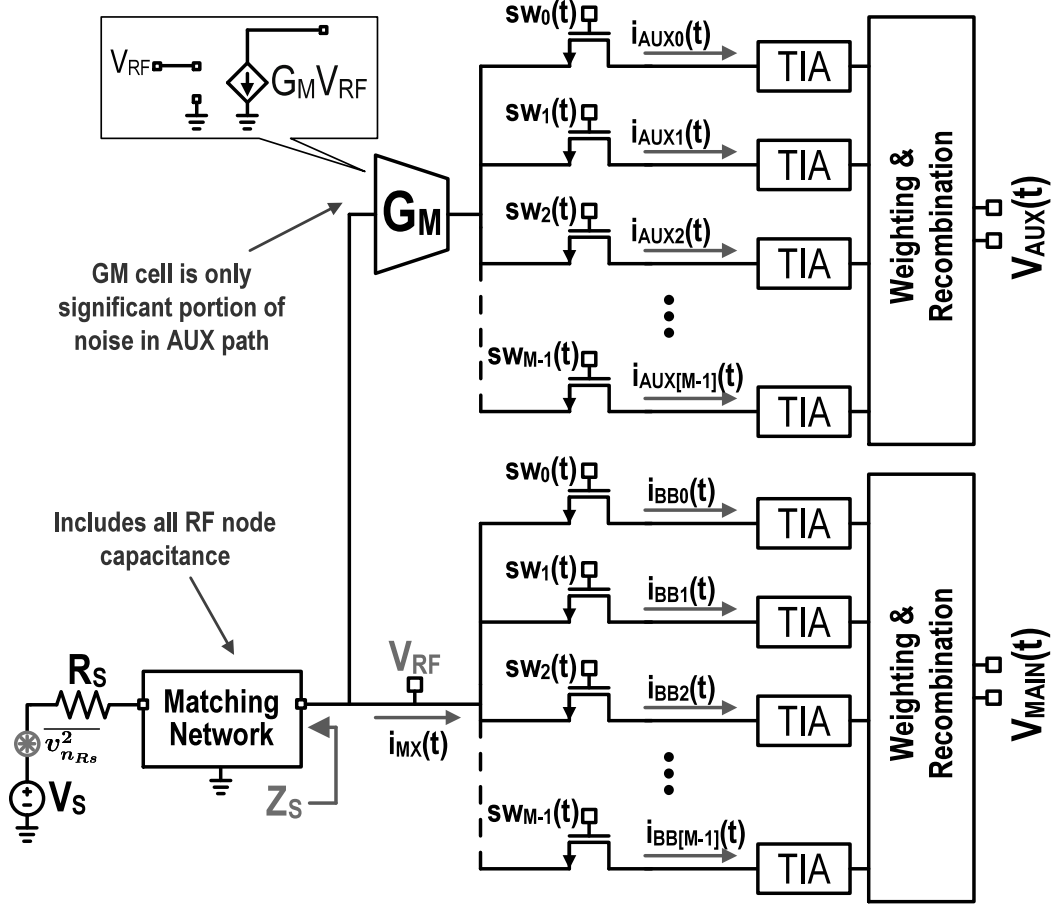


Figure 3.6: Model of the FTNC receiver.

### 3.5 The Mixer-First RX (or Main Path of the FTNC-RX)

With the foundations of the LTV analysis laid in the previous sections, it is now possible to analyze the FTNC-RX. We first derive the gain and noise figure of the main path of the

FTNC-RX (which is equivalent to a mixer-first RX shown in Fig. 3.4).

### 3.5.1 Mixer-First RX Conversion Gain

Assuming the receiver is configured to receive the  $m^{\text{th}}$  harmonic, the conversion gain from around the  $v^{\text{th}}$  harmonic of the RF signal to mixer first receiver output is defined as

$$Av_{MAIN[m,v]}{\Delta\omega} = \frac{V_{MAIN[m]}{\Delta\omega}}{V_S\{v\omega_c + \Delta\omega\}} \quad (3.33)$$

Now, using Eqn. (3.30) if we refer the input voltage source to the Norton Equivalent current (i.e.  $I_N = \beta V_S/Z_S$ ), the conversion gain from the signal around the  $v^{\text{th}}$  harmonic is given by:

$$Av_{MAIN[m,v]}{\Delta\omega} = G_{MAIN} \frac{Sw[v]}{Sw[m]} \frac{\alpha\{m\omega_c + \Delta\omega\}\beta\{v\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}}. \quad (3.34)$$

This expression assumes  $v = m - gM$  and  $g \in \mathcal{Z}$ . If  $v \neq m - gM$ ,  $Av_{MAIN[m,v]}{\Delta\omega}$  will be zero. In other words, only harmonics that are offset by  $M$  will fold on top of one another. For the remainder of the text, unless otherwise specified, we will assume that  $v = m - gM$ ,  $g \in \mathcal{Z}$ .

Note the gain from the voltage source representing the mixer switch noise experiences a similar gain and is given by:

$$\frac{V_{MAIN[m]}{\Delta\omega}}{V_{RSW}\{v\omega_c + \Delta\omega\}} = G_{MAIN} \frac{Sw[v]}{Sw[m]} \frac{\alpha\{m\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}}. \quad (3.35)$$

### 3.5.2 Output Noise due to Norton Equivalent Load

Just as signals around higher harmonics fold down and appear in the wanted band, noise can also fold down from higher harmonics and degrade the receiver's noise performance. Accordingly, to calculate output noise from  $Z_N$ , we should account for folding from all relevant harmonics. Using Eqn. (3.26), the Norton referred noise due to  $Z_{NFOLD}$  can be

calculated as

$$\begin{aligned} \overline{i_{n_{ZFOLD}}^2} &= \sum_{g=-\infty}^{\infty} \left| \frac{Sw[(m-gM)]}{Sw[m]} \right|^2 \Re \left\{ \frac{4kT}{Z_N\{(m-gM)\omega_c + \Delta\omega\}} \right\} \\ &= \Re \left\{ \frac{4kT}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}} \right\} \end{aligned} \quad (3.36)$$

Therefore, output noise due to both the switch resistance and the load impedance (which are both capture by  $Z_N$ ) is given by:

$$\overline{v_{MAIN}^2} = \frac{|G_{MAIN}MSw[m]|^2 4kT \Re\{Z_{NFOLD}\{m\omega_c + \Delta\omega\}\}}{|Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}|^2}. \quad (3.37)$$

Interestingly, as first noted in [8], this is the same noise as would be present, if we ignored the frequency translation effects, and replaced  $Z_N$  with  $Z_{NFOLD}$ . If the RF node is purely resistive the output noise is given by:

$$\overline{v_{MAIN}^2} = \left| \frac{G_{MAIN}}{Z_{BB}\{\Delta\omega\}/M + R_{SW} + R_S} \right|^2 4kT(R_{SW} + R_S). \quad (3.38)$$

While, if  $M$  is sufficiently large that we can ignore folding effects, the output noise becomes:

$$\overline{v_{MAIN}^2} = \frac{|G_{MAIN}MSw[m]|^2 4kT \Re\{Z_N\{m\omega_c + \Delta\omega\}\}}{|Z_{MX}\{m\omega_c + \Delta\omega\} + Z_N\{m\omega_c + \Delta\omega\}|^2}. \quad (3.39)$$

### 3.5.3 Output Noise due to Baseband Sources

In this work, we modeled the TIA noise as input voltage source that appear in series with the equivalent baseband impedance (Fig. 3.4(b)). These baseband voltages were then mapped to the RF side of the mixers in Fig. 3.4(c) using Eqn. (3.13). Since, the baseband voltages only have components around DC, we can further simplify the RF referred voltage around  $m\omega_c$  as

$$V_{BB_{RF}}\{m\omega_c + \Delta\omega\} = Sw_x[m] \sum_{x=0}^{M-1} V_{BB_x}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}. \quad (3.40)$$

This corresponds to an equivalent Norton current of

$$I_N\{m\omega_c + \Delta\omega\} = -\frac{Sw[m] \sum_{x=0}^{M-1} V_{BB_x}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}}{Z_N\{m\omega_c + \Delta\omega\}}, \quad (3.41)$$

which results in a “folded” Norton current given by

$$I_{NFOLD}\{m\omega_c + \Delta\omega\} = -\frac{Sw[m] \sum_{x=0}^{M-1} V_{BB_x}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}}. \quad (3.42)$$

Accordingly, using Eqn. (3.30), the output due to the baseband voltage sources is calculated as

$$V_{MAIN[m]}\{\Delta\omega\} = -\frac{G_{MAIN}M|Sw[m]|^2 \sum_{x=0}^{M-1} V_{BB_x}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}}{Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}}. \quad (3.43)$$

Of course, these baseband voltages are not signals, but rather uncorrelated noise sources. Assuming that each baseband noise source has the same power spectral density,  $\overline{v_{BB}^2}$ , the output noise is given by

$$\overline{v_{out}^2} = \frac{|G_{MAIN}|^2 M^3 |Sw[m]|^4 \overline{v_{BB}^2}}{|Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}|^2}. \quad (3.44)$$

### 3.5.4 Noise Figure of Mixer-First RX

When the auxiliary path is powered down, the FTNC-RX is essentially a mixer-first receiver. Given this, the noise figure of the main path and a mixer-first receiver are equivalent. At this point, we have enough information to derive this noise figure. The noise figure when the receiver is configured to receive the  $m^{\text{th}}$  harmonic is:

$$NF = \frac{\overline{v_{out}^2}}{|Av_{MAIN[m,m]}\{\Delta\omega\}|^2 4kTR_S}, \quad (3.45)$$

which is expanded to become

$$NF = \left( \frac{\Re\{Z_{NFOLD}\{m\omega_c + \Delta\omega\}\}}{R_S} + \frac{|Sw[m]|^2 M \overline{v_{BB}^2}}{4kTR_S} \right) \times \left| \frac{Z_N\{m\omega_c + \Delta\omega\}}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}} \right|^2 \left| \frac{1}{\beta\{m\omega_c + \Delta\omega\}} \right|^2. \quad (3.46)$$

If the antenna is purely resistive, the above expression simplifies to:

$$NF = \left( 1 + \frac{R_{SW}}{R_S} + \frac{\overline{v_{BB}^2}}{M(4kTR_S)} \right) \frac{1}{M^2 |Sw[m]|^2} \quad (3.47)$$

It is interesting to note that even if the mixer-first receiver is completely noiseless (i.e. the switch resistance is zero, and the baseband TIAs have negligible noise), antenna noise

folding will still limit the noise figure to  $NF = 1/(M^2 |Sw[m]|^2)$  at low frequencies. In order to reconstruct the I/Q signals, we required  $M \geq 3$ , however, increasing  $M$  further also improves NF by reducing noise folding and increasing the conversion gain. If  $M$  is sufficiently large, we can ignore all folding effects, and the noise figure simplifies to

$$NF = 1 + \left( \frac{R_{SW}}{R_S} + \frac{\overline{v_{BB}^2}}{M(4kTR_S)} \right) \left| \frac{1}{\beta\{m\omega_c + \Delta\omega\}} \right|^2, \quad (3.48)$$

where the relationship  $|\beta\{m\omega_c + \Delta\omega\}|^2 = \Re\{Z_S\{m\omega_c + \Delta\omega\}\}/R_S$  was used in the simplification. Note that assuming that  $\overline{v_{BB}^2}$  is decoupled from the baseband impedances,  $Z_{BB}$ , the noise figure of the current-commutating passive mixer is independent of the baseband impedance (this is typically the case in a well-designed mixer-first receiver). While these formulas are derived, formulated and presented differently, they are mathematically equivalent to the expressions presented in Andrew's work [8] (with the exception that Andrew's includes a baseband noise current source that is correlated with the baseband noise voltage source).

In Fig. 3.7, the linearized model is redrawn to explicitly show the noise sources. Note that as  $Z_{SH}$  becomes small (with respect to  $Z_{MX}$ ), conversion gain decreases and noise figure degrades.

### 3.5.5 Simulation Results

The mixer-first receiver model shown in Fig. 3.8 was used to verify the above expressions. A 4-phase, 8-phase and  $\infty$ -phase (i.e.  $M = 4$ ,  $M = 8$ ,  $M = \infty$ ) version of the circuit was simulated. In each version, the switch resistance was constant ( $30\Omega$ ), while each baseband resistance was set at  $M \times 20\Omega$ . The baseband bandwidth was 10MHz, and the PSD of each baseband noise source was  $\overline{v_{BB}^2} = 4kT\gamma M/0.02$ . Using these values ensures that the RX path current and the chip area (which is dominated by baseband capacitors and transistors) is constant regardless of the number of mixer phases. It also ensures the input impedance (and thus S11) of each version of the receiver is approximately the same. The baseband gain of the main path was set at  $G_{MAIN} = 3000$ .

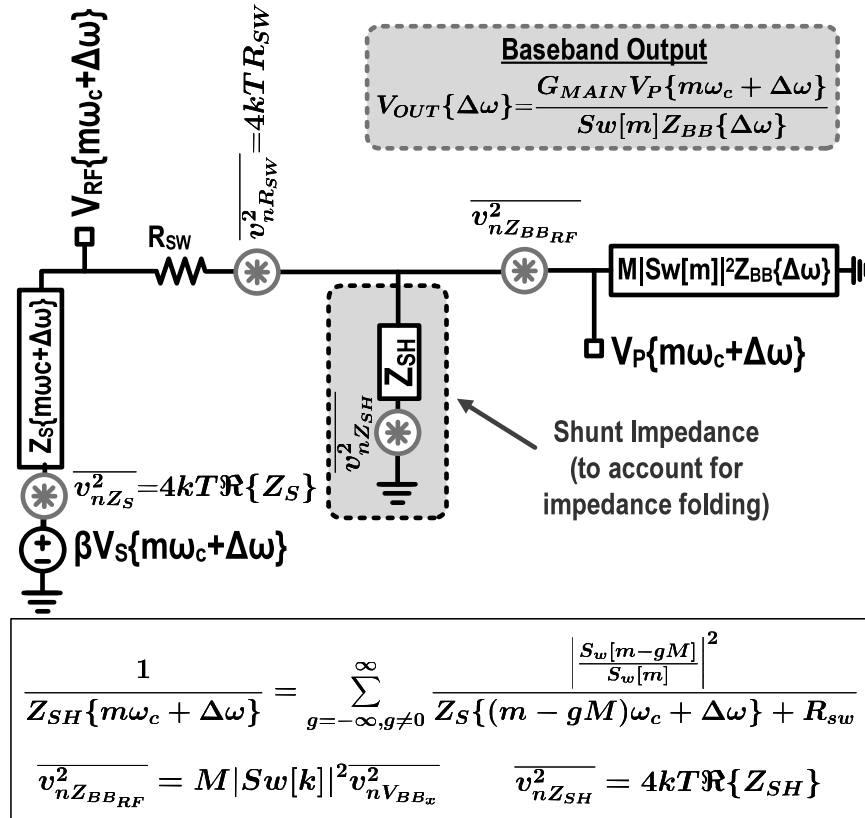


Figure 3.7: LTI model of mixer-first receiver.

The simulated noise figure, gain and S11 are plotted in Fig. 3.9(a) and Fig. 3.9(b). The values predicted by the preceding analysis are also plotted and are indistinguishable from simulation. Note that although S11 for each version of the receiver is similar, the noise figure and the gain of the circuit degrade as the number of mixer phases is reduced. Moreover, when a relatively few number of phases are used (i.e.  $M = 4$ ), the gain and noise performance degrade substantially at higher frequencies. This degradation in performance is because of increased noise and impedance folding effects.

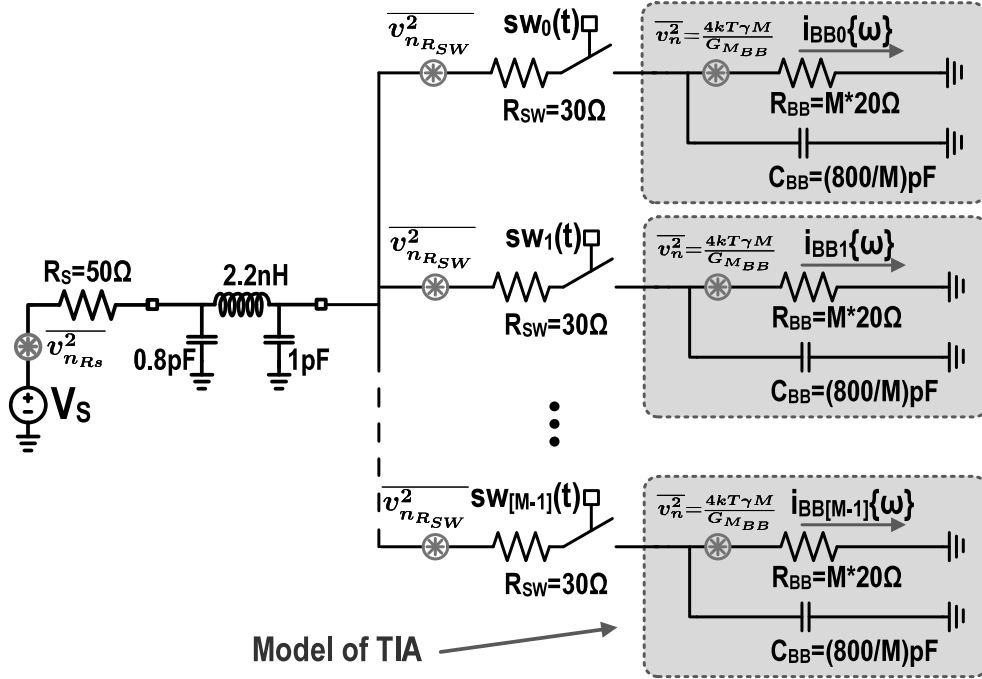
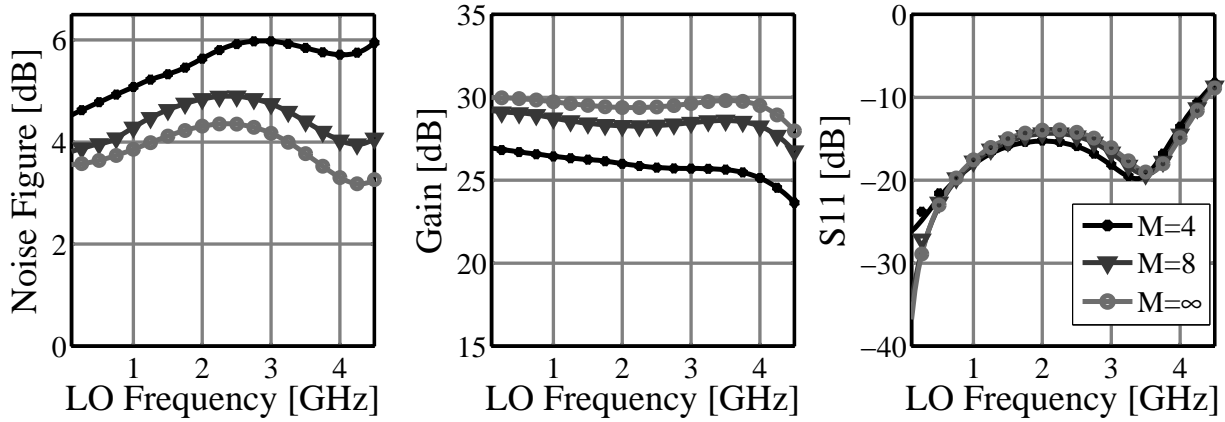


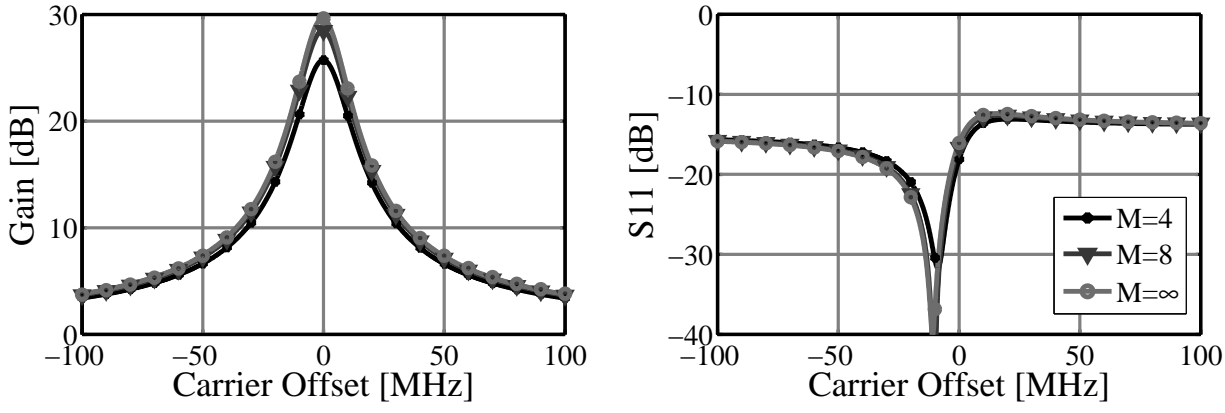
Figure 3.8: The simulated mixer-first RX model. (Harmonic recombination with  $G_{MAIN}=3000$  is not shown.)

Remarkably, Eqn. (3.46) suggests that the mixer-first receiver does not have a fundamental lower bound on its noise performance. For instance if we used a large number of phases, make the mixer switches arbitrarily small, and burn a lot of current in the baseband such that baseband noise is negligible, the noise figure would come close to 0dB. However, in a practical implementation, this is only feasible at very low frequencies. To demonstrate why, the circuit in Fig. 3.8 was re-simulated, but with switches that were 15 times larger (i.e.  $R_{SW}=2\Omega$ ). The TIAs were assumed to be noiseless and their input resistance were





(a) Noise Figure, Gain and S11 of mixer-first receiver versus carrier frequency. (Solid lines correspond to analysis, markers correspond to simulation.)



(b) Gain and S11 of mixer-first RX versus carrier offset at 3GHz. (Solid lines correspond to analysis, markers correspond to simulation.)

Figure 3.9: Simulation and analysis results of the mixer-first RX model.

set at  $M \times 48\Omega$ . The resulting noise figure, gain and S11 are plotted in Fig. 3.10. Note that even though the only sources of noise are the  $2\Omega$  switch resistances, the noise figure degrades to above 2dB at 3GHz for a 4-phase RX. The low frequency performance predicted by Eqn. (3.47) is not maintained at high frequencies, because the small switch resistance coupled with a non-resistive RF node results in a very small value of  $Z_{NFOLD}\{m\omega_c + \Delta\omega\}$ , which degrades conversion gain and increases the downconverted noise current.

In addition to poor noise performance at high frequencies, this aggressive mixer-first design is also not practical. Firstly, since the switches are 15 times larger than in the original design, the capacitive loading will also increase by a factor of 15. This will dramatically increase the power dissipation in the LO buffers. Secondly, while it may be possible to make the baseband thermal noise very small by burning a large amount of power, the size of the baseband component are likely to be unacceptably large in order to minimize the flicker noise contribution.

It is worth noting another interesting aspect of this aggressive mixer-first receiver: In order for the mixer-first to have a low noise figure, all significant higher order harmonics (3<sup>rd</sup> and 5<sup>th</sup> harmonic in the case of the 4-phase RX) must be inside the RF bandwidth otherwise  $Z_{NFOLD}\{m\omega_c + \Delta\omega\}$  degrades. However, if these harmonics are inside the RF bandwidth, any signals at these harmonics will be downconverted along with the wanted signal at the fundamental. Therefore, unlike other commonly used receiver topologies, sharp RF filtering is not compatible with a low-noise mixer-first receiver.

### 3.6 The Complete FTNC-RX

We now calculate the gain and noise transfer functions of the auxiliary path. These expressions coupled with the expressions for the mixer-first receiver allow us to characterize the performance of the complete FTNC receiver.

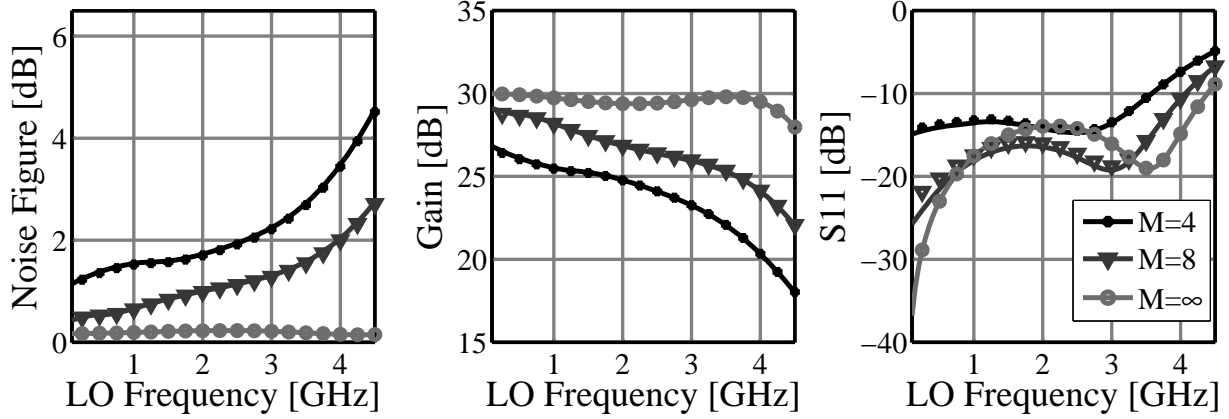


Figure 3.10: Noise figure of aggressive mixer-first design. (Solid lines correspond to analysis, markers correspond to simulation.)

### 3.6.1 Auxiliary Path Conversion Gain

Assuming the receiver is configured to receive the  $m^{\text{th}}$  harmonic, the conversion gain from the  $v^{\text{th}}$  harmonic of the RF signal to output of the auxiliary path is defined as

$$Av_{AUX[m,v]}{\Delta\omega} = \frac{V_{AUX[m,v]}{\Delta\omega}}{V_S\{v\omega_c + \Delta\omega\}}. \quad (3.49)$$

The output expression  $V_{AUX[m,v]}{\Delta\omega}$  can be written in terms of  $V_{RF}$  using Eqn. (3.32). Referring back to Fig. 3.4(c), the voltage at  $V_{RF}$  can be expressed in terms of the input voltage  $V_S$  through the following expression

$$V_{RF}\{\omega\} = \frac{R_{SW}\beta\{\omega\}V_S\{\omega\} + Z_S\{\omega\}V_P\{\omega\}}{R_{SW} + Z_S\{\omega\}}. \quad (3.50)$$

Given the above expression and some straightforward, but tedious mathematical manipulations, the auxiliary path conversion gain can be written as:

$$\begin{aligned} & Av_{AUX[m,v]}{\Delta\omega} \\ &= -G_{AUX}G_M \frac{Sw[v] \beta\{v\omega_c + \Delta\omega\} \alpha\{m\omega_c + \Delta\omega\}}{Sw[m] Z_N\{v\omega_c + \Delta\omega\}} (R_{SW} + Z_{BB}\{\Delta\omega\}/M) \end{aligned} \quad (3.51)$$

And, since the gain of the complete FTNC-RX is given by

$$Av_{FTNC[m,v]}{\Delta\omega} = Av_{AUX[m,v]}{\Delta\omega} - Av_{MAIN[m,v]}{\Delta\omega}, \quad (3.52)$$

the gain of the FTNC from the  $v^{\text{th}}$  harmonic is given by

$$\begin{aligned}
Av_{FTNC[m,v]\{\Delta\omega\}} = & \\
& - (G_{AUX}G_M (R_{SW} + Z_{BB}\{\Delta\omega\}/M) + G_{MAIN}) \frac{Sw[v]}{Sw[m]} \frac{\alpha\{m\omega_c + \Delta\omega\}\beta\{v\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}}.
\end{aligned} \tag{3.53}$$

To verify this expression, the model shown in Fig. 3.11 was simulated. Figure 3.12 plots the resulting receiver gain ( $m = 1$ ) as a function of carrier frequency and also frequency offset from a 3GHz carrier. Both simulation results and values predicted by analysis are indistinguishable.

### 3.6.2 Antenna Noise

Since the conversion gain from the input is identical to the conversion gain from antenna noise, the total output noise due to the antenna is calculated as

$$\overline{v_{out}^2} = \sum_{g=-\infty}^{\infty} |Av_{FTNC[m,m-gM]\{\Delta\omega\}}|^2 \overline{v_{Rs}^2}. \tag{3.54}$$

Using this expression and assuming the antenna is the only source of noise, the noise figure becomes

$$\begin{aligned}
NF &= \frac{\sum_{g=-\infty}^{\infty} |Av_{FTNC[m,m-gM]\{\Delta\omega\}}|^2}{|Av_{FTNC[m,m]\{\Delta\omega\}}|^2} \\
&= \left| \frac{Z_N\{m\omega_c + \Delta\omega\}}{Sw[m]\beta\{m\omega_c + \Delta\omega\}} \right|^2 \sum_{g=-\infty}^{\infty} \left| \frac{Sw[m-gM]\beta\{(m-gM)\omega_c + \Delta\omega\}}{Z_N\{(m-gM)\omega_c + \Delta\omega\}} \right|^2
\end{aligned} \tag{3.55}$$

Now if  $Z_S$  is frequency independent, the noise figure becomes

$$NF = \frac{1}{M^2 |Sw[m]|^2} \tag{3.56}$$

and so even if the circuit is completely noiseless, antenna noise folding will increase the noise figure above 1. In order to minimize this noise-folding,  $M$  should be made as large as practical. Note, as expected, the FTNC-RX does not cancel any of the antenna noise, even noise that folds from higher-order harmonics.

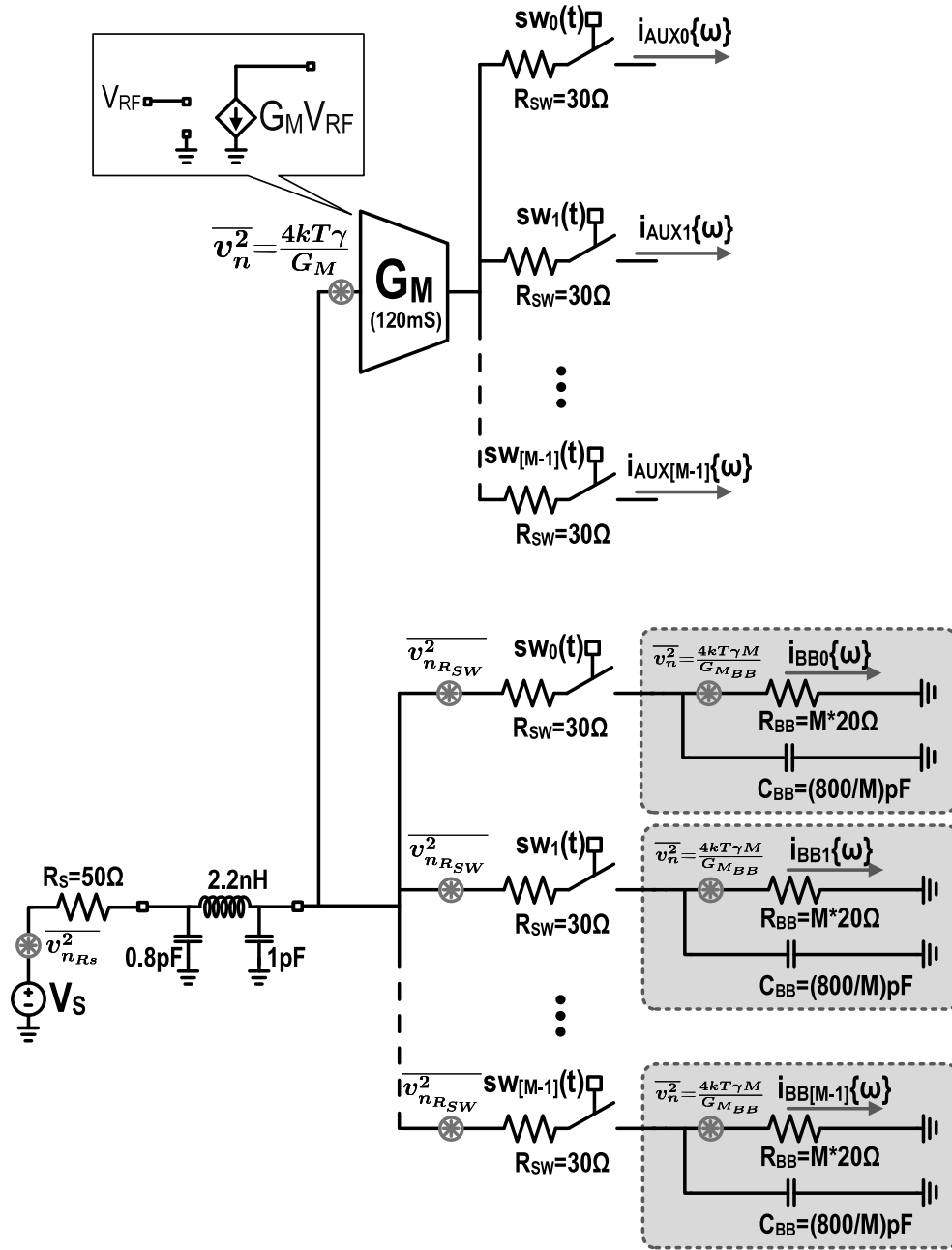


Figure 3.11: Simulated FTNC-RX model. (Not shown is the recombination of the main and auxiliary baseband currents with gains of  $G_{MAIN}=3000$  and  $G_{AUX}=450e^{j\frac{10\pi}{180}}$  respectively.)

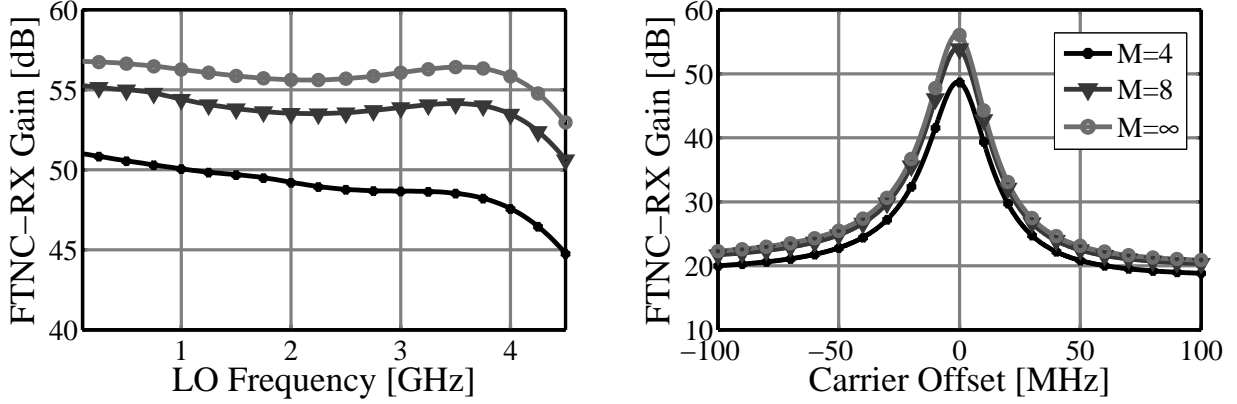


Figure 3.12: Gain of FTNC-RX. (Solid lines correspond to analysis, markers correspond to simulation.)

### 3.6.3 Switch Noise

The switch noise is first analyzed by deriving the transfer function from  $V_{RSW}$  to  $V_{AUX}$ . We note that  $V_{RF}$  can be defined in terms of  $V_{RSW}$

$$V_{RF}\{\omega\} = \frac{Z_S\{\omega\} (V_P\{\omega\} - V_{RSW}\{\omega\})}{R_{SW} + Z_S\{\omega\}} \quad (3.57)$$

Given this, and using the same approach that was used to calculate the conversion gain from the RF input, the auxiliary output due to  $V_{RSW}$  is given by

$$\frac{V_{AUX[m,v]}\{\Delta\omega\}}{V_{RSW}\{v\omega_c + \Delta\omega\}} = -\frac{G_{AUX}G_M\alpha\{m\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}} \frac{Sw[v]}{Sw[m]} \times \left( \frac{Z_{MX}\{m\omega_c + \Delta\omega\}}{M^2|Sw[m]|^2} - \frac{Z_{MX}\{m\omega_c + \Delta\omega\}Z_N\{v\omega_c + \Delta\omega\}}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}} - Z_S\{v\omega_c + \Delta\omega\} \right). \quad (3.58)$$

Now, in order for the signal  $V_{RSW}\{v\omega_c + \Delta\omega\}$  (which represents the switch noise around the  $v^{\text{th}}$  harmonic) to be cancelled, it required that:

$$\frac{V_{MAIN[m,v]}\{\Delta\omega\}}{V_{RSW}\{v\omega_c + \Delta\omega\}} = \frac{V_{AUX[m,v]}\{\Delta\omega\}}{V_{RSW}\{v\omega_c + \Delta\omega\}} \quad (3.59)$$

This noise cancelling condition results in the following identity:

$$G_{MAIN} = +G_{AUX}G_MZ_S\{v\omega_c + \Delta\omega\} - G_{AUX}G_MZ_{MX}\{m\omega_c + \Delta\omega\} \left( \frac{1}{M^2|Sw[m]|^2} - \frac{Z_N\{v\omega_c + \Delta\omega\}}{Z_{NFOLD}\{m\omega_c + \Delta\omega\}} \right). \quad (3.60)$$

Notice that unless  $Z_S\{v\omega_c + \Delta\omega\}$  (and thus  $Z_N\{v\omega_c + \Delta\omega\}$ ) is constant across frequency (i.e. resistive), the switch noise that folds down from higher frequencies cannot be simultaneously nulled. In reality, while perfect cancellation of noise from all harmonics cannot be achieved, a significant reduction will occur. In general, the output noise due to the switch resistance is given by:

$$\overline{v_{out}^2} = \overline{v_{R_{SW}}^2} \sum_{g=-\infty}^{\infty} \left| \frac{V_{AUX[m,m-gM]\{\Delta\omega\}} - V_{MAIN[m,m-gM]\{\Delta\omega\}}}{V_{R_{SW}}\{(m-gM)\omega_c + \Delta\omega\}} \right|^2. \quad (3.61)$$

If  $M$  is large, the antenna is purely resistive and/or the baseband impedance is zero, the output noise due to the switch resistance is given by

$$\overline{v_{out}^2} = \overline{v_{R_{SW}}^2} \sum_{g=-\infty}^{\infty} \left( \left| \frac{\alpha\{m\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}} \frac{Sw[v]}{Sw[m]} \right|^2 \times |G_{AUX}G_M Z_S\{v\omega_c + \Delta\omega\} - G_{MAIN}|^2 \right) \quad (3.62)$$

and, so, the noise cancelling condition becomes:

$$G_{MAIN} = G_{AUX}G_M Z_S\{v\omega_c + \Delta\omega\} \quad (3.63)$$

To verify this analysis, the contribution of the mixer switches to the noise factor (NF) of the FTNC-RX (i.e. mixer switch noise normalized to the receiver's gain) was simulated. The model shown in Fig. 3.11 was again used and the carrier frequency was assumed to be 3GHz. Both the magnitude and phase of  $G_{AUX}$  was swept. The simulation results and values predicted by analysis are plotted in Fig. 3.13. We note the following:

- Since  $Z_S$  is frequency dependent (i.e. not purely resistive), switch noise cannot be completely nulled unless a very large number of phases is used. However, a significant portion of the noise can always be cancelled.
- The optimum value of  $G_{AUX}$  is very close to the solution of Eqn. (3.63), and slight variations in  $G_{AUX}$  around this point do not significantly affect noise cancellation.

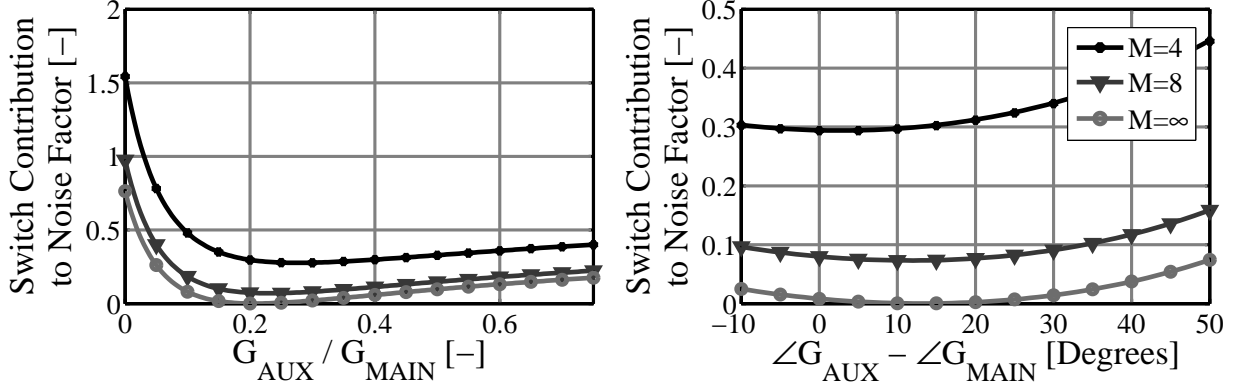


Figure 3.13: Contribution of switch noise to the noise factor of the FTNC-RX. (LO frequency = 3GHz; Solid lines corresponds to analysis, markers correspond to simulation).

### 3.6.4 Baseband Noise

The baseband noise due to the main path TIAs is analyzed in a similar fashion. The transfer function from the baseband voltage sources to  $V_{RF}$  is given by

$$V_{RF}\{\omega\} = \frac{Z_{RF}\{\omega\} (V_P\{\omega\} + V_{BBRF}\{\omega\})}{R_{SW} + Z_{RF}\{\omega\}}, \quad (3.64)$$

which simplifies to

$$V_{RF}\{m\omega_c + \Delta\omega\} = \frac{Z_S\{m\omega_c + \Delta\omega\}}{R_{SW} + Z_S\{m\omega_c + \Delta\omega\}} \frac{Z_{NFOLD}\{m\omega_c + \Delta\omega\} Sw[m] \sum_{x=0}^{M-1} V_{BBx}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}}{Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}}. \quad (3.65)$$

Using this expression for  $V_{RF}$ , the auxiliary output as a function of the baseband voltage sources is calculated as

$$V_{AUX[m,v]}\{\Delta\omega\} = -G_{AUX}G_M \left( \frac{Z_{NFOLD}}{M^2|Sw[m]|^2} - R_{SW} \right) \times \left( \frac{M|Sw[m]|^2 \sum_{x=0}^{M-1} V_{BBx}\{\Delta\omega\} e^{-j\frac{2\pi mx}{M}}}{Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}} \right). \quad (3.66)$$

Given this, output noise due to the baseband noise sources is given by:

$$\overline{v_{out}^2} = \left| G_{AUX}G_M \left( \frac{Z_{NFOLD}\{m\omega_c + \Delta\omega\}}{M^2|Sw[m]|^2} - R_{SW} \right) - G_{MAIN} \right|^2 \times \frac{M^3|Sw[m]|^4 \overline{v_{BB}^2}}{|Z_{MX}\{m\omega_c + \Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}|^2}. \quad (3.67)$$



And the noise cancelling condition for the baseband noise is thus:

$$G_{MAIN} = G_{AUX} G_M \left( \frac{Z_{NFOLD} \{m\omega_c + \Delta\omega\}}{M^2 |S_W[m]|^2} - R_{SW} \right). \quad (3.68)$$

Notice that baseband noise, unlike the switch noise, can always be completely nulled regardless of the value of  $Z_S$ . If the RF node is purely resistive, this noise cancelling condition becomes

$$G_{MAIN} = G_{AUX} G_M R_S. \quad (3.69)$$

While, if the  $M$  is large, the noise cancelling condition becomes

$$G_{MAIN} = G_{AUX} G_M Z_S \{m\omega_c + \Delta\omega\}. \quad (3.70)$$

Again, to verify this analysis the model shown in Fig. 3.11 was simulated, and the noise contribution of the baseband noise sources was deduced. Results from analysis and simulation are plotted in Fig. 3.14. Unlike the switch noise, which cannot be completely nulled (unless  $Z_S$  is purely resistive), there is an optimum  $G_{AUX}$  which completely nulls the baseband noise. This means that flicker noise arising from the main-path TIAs (which can dominate in a mixer-first receiver) can *always* be nulled in the FTNC-RX.

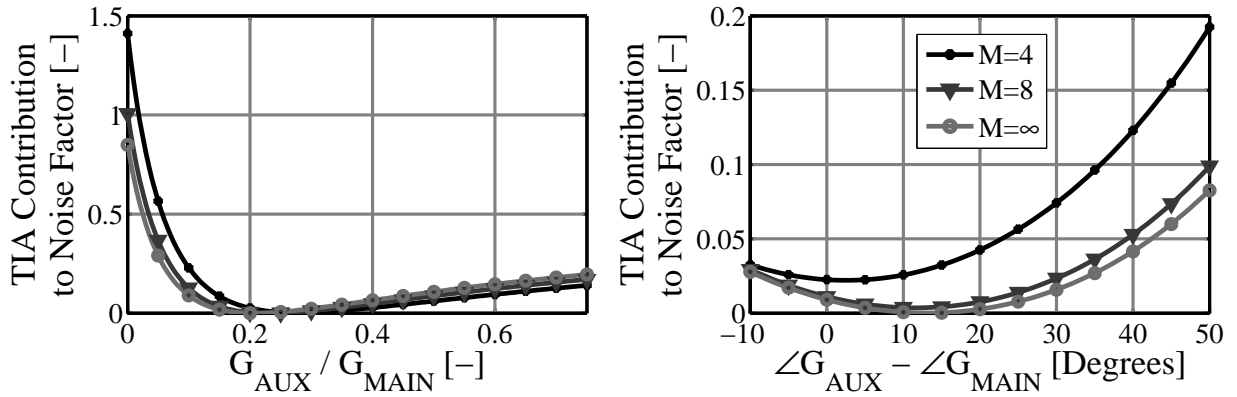


Figure 3.14: Contribution of baseband noise sources to the noise factor of the FTNC-RX. (LO frequency = 3GHz; Solid lines correspond to analysis, markers correspond to simulation.)

### 3.6.5 $G_M$ Cell Noise

Noise is also contributed by the RF transconductance in the auxiliary path, indeed, it is the only significant noise contributor that cannot be at least partially cancelled. The output noise due the  $G_M$  cell is given by:

$$\overline{v_{OUT}^2} = |G_{AUX}G_M|^2\overline{v_{GM}^2} \quad (3.71)$$

Assuming  $\overline{v_{GM}^2} = 4kT\gamma/G_M$ , the only way to minimize the contribution of this noise source is to make  $G_M$  as large as practically possible.

### 3.6.6 Auxiliary Switch and Baseband Noise

If the output impedance of the RF trans-conductance is large and the receiver gain is large, the noise associated with auxiliary mixer switches and the auxiliary op-amps will not contribute significantly to the total output noise. This is because the auxiliary TIAs are current driven, and since only one switch is on at any given time, the series voltage noise sources cannot generate a noise current.

## 3.7 Noise Figure of FTNC-RX

At this point, we have enough information to derive a close form expression for the noise figure of the FTNC-RX. However, the resultant expression contains infinite summations and does not provide much insight. Instead, we will look at 2 limiting cases: A FTNC-RX with a purely resistive RF node and a FTNC-RX with a large number of mixer phases.

### 3.7.1 Noise Figure Assuming Resistive RF Node

At low frequencies, all significant folding terms will be within the RF bandwidth. Under such conditions, the RF node can be considered to be purely resistive. If this is the case,

and we set  $G_{MAIN} = G_M G_{AUX} R_S$ , the gain of receiver becomes

$$Av_{FTNC[m]} \{ \Delta\omega \} = -MSw[m]G_M G_{AUX} \quad (3.72)$$

and the noise figure becomes

$$NF = \left( 1 + \frac{\overline{v_{GM}^2}}{\overline{v_{RS}^2}} \right) \frac{1}{M^2 |Sw[m]|^2} \quad (3.73)$$

Therefore, the only noise contributor within the receiver is the  $G_M$  cell. All other noise sources are cancelled. This is the same noise figure as an un-matched common-source amplifier. However, unlike the simple common-source amplifier, the FTNC-RX provides matching and has the added advantage of reducing the swing at the RF node by 6dB.

### 3.7.2 Noise Figure Assuming Large $M$

Alternatively, if we assume  $M$  is large and we set  $G_{MAIN} = G_M G_{AUX} Z_S \{ m\omega_c + \Delta\omega \}$ , the gain of receiver becomes

$$Av_{FTNC[m]} \{ \Delta\omega \} = -\beta \{ m\omega_c + \Delta\omega \} G_M G_{AUX} \quad (3.74)$$

and the noise figure becomes

$$NF = 1 + \left( \frac{\overline{v_{GM}^2}}{\overline{v_{RS}^2}} \right) \frac{1}{|\beta \{ m\omega_c + \Delta\omega \}|^2}. \quad (3.75)$$

Again, the only noise contributor in the receiver is the  $G_M$  cell.

### 3.7.3 Noise Figure for Other Cases

For other cases, switch noise is not cancelled completely, but it can be significantly reduced. For instance if the baseband impedance is close to zero, the noise due the baseband elements and switch noise around the fundamental harmonic can be simultaneously cancelled, if  $G_{MAIN} = G_M G_{AUX} Z_S \{ m\omega_c + \Delta\omega \}$ . While switch noise arising from higher order harmonics will not be completely nulled, they will be significantly reduced. A good design methodology is to set  $G_{MAIN} = G_M G_{AUX} Z_S \{ m\omega_c + \Delta\omega \}$ , and use as large a number of

LO phase as possible and, if small-signal noise performance is the only concern, make the TIA input impedance as small as possible.

### 3.7.4 Simulation Results

To demonstrate the effectiveness of the auxiliary path at reducing the receiver’s noise figure, the simulated and predicted results of the model in Fig. 3.11 are plotted in Fig. 3.15. Also plotted is the noise figure of the main path only (i.e. the equivalent mixer-first receiver). Clearly, the auxiliary path significantly reduces the noise figure, even when only 4-phases are used.

It is also informative to compare these results to the aggressive-mixer first design shown in Fig. 3.10 where the only noise sources were the  $2\Omega$  switches. Compared to that aggressive mixer first design, the low frequency noise figure is comparable, but the FTNC-RX has significantly better noise performance at high frequencies, does not require power and area-hungry baseband devices, and reduces the capacitive burden on the LO chain.

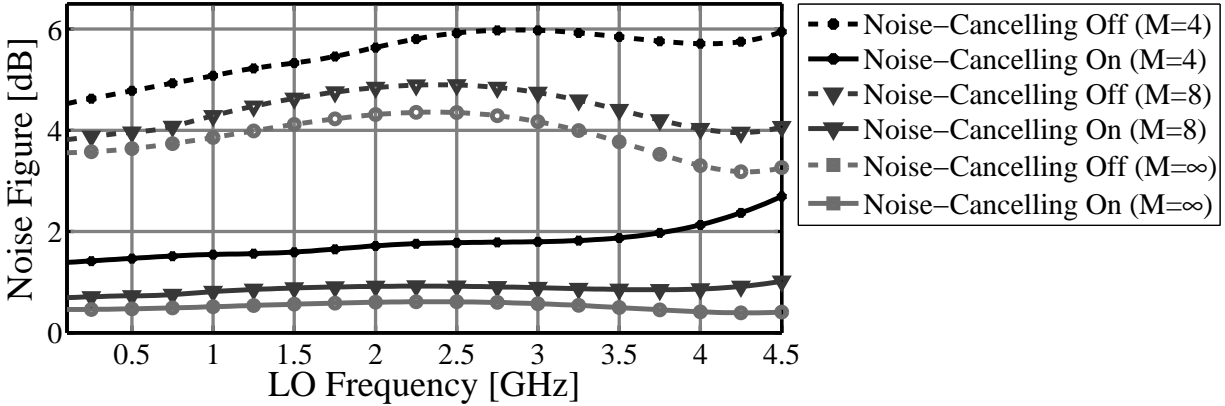


Figure 3.15: Noise figure of complete FTNC-RX assuming  $G_{MAIN} = G_M G_{AUX} Z_S \{m\omega_c + \Delta\omega\}$ . (Solid lines correspond to analysis, markers correspond to simulation.)

While the noise cancelling condition for the switch noise and baseband impedance are not always the same, they will be very similar if the switch resistance ( $R_{SW}$ ) is not much smaller than the upconverted TIA impedance ( $Z_{MX} \{m\omega_c + \Delta\omega\}$ ). The noise figure of

the complete FTNC-RX versus the auxiliary path phase and gain correction is plotted in Fig. 3.16. Notice that around optimum point, noise-cancelling is quite robust; variations in gain by  $\pm 20\%$  or phase by  $\pm 20^\circ$  does not lead to significant degradation.

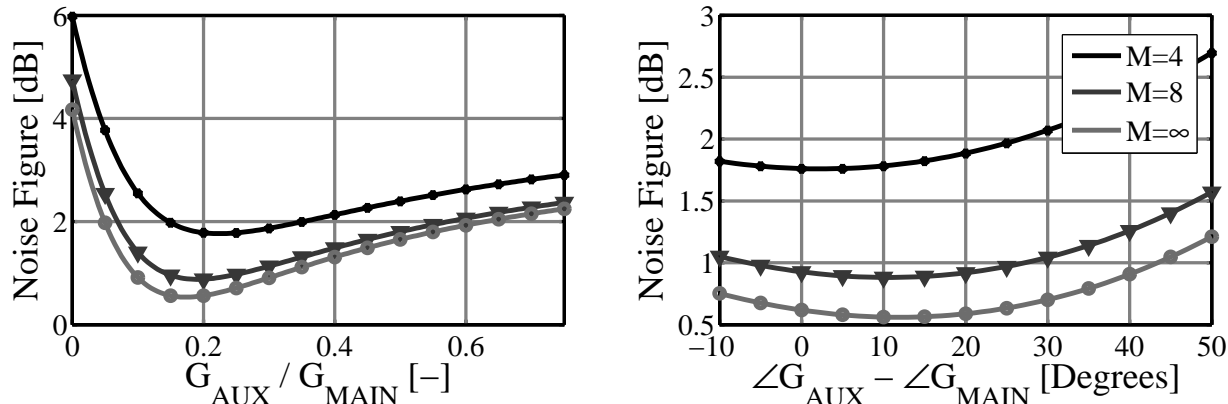


Figure 3.16: Noise figure versus auxiliary path gain and phase correction. (LO frequency = 3GHz; Solid lines correspond to analysis, markers correspond to simulation.)

### 3.8 The FTNC-RX as a High- $Q$ Filter

High- $Q$  frequency translational bandpass filters (FT-BPF) have recently been proposed as a means of filtering blockers close to the receive band [39] [40] [25]. The performance of such filters have been extensively studied elsewhere using a variety of methods [8] [37] [38] [41] and, so, will not be repeated here. However, it should be noted that the passive mixers employed in the FTNC-RX can be configured to operate as high- $Q$  filters. Since the LTV analysis used in this work is the same as that use in the analysis of FT-BPFs [37] [38], this effect is easily quantified.

First, consider the case where a high- $Q$  filter is placed directly at the input of an RX as shown in Fig. 3.17(a). Reference [37] determines the amount of filtering which occurs directly at the fundamental of  $V_{RF}$ . This is the correct approach provided the LNA has voltage gain at RF and has some passive filtering at the output. If instead an RF transconductance is employed and the output current is directly downconverted to

baseband, as shown in Fig. 3.17(b), the output will also depend on higher order harmonics present at  $V_{RF}$ . In such a case, it can be shown that the conversion gain is given by the Eqn. (3.51), which describes the conversion gain of the auxiliary path of the FTNC RX. If we write that equation in terms of Fig. 3.17(b), the conversion gain is described as

$$\begin{aligned}
A_{v_{FTBPF[m,v]}}\{\Delta\omega\} = & \\
& - G_{ARB}G_M \frac{MSw[v]\beta\{v\omega_c + \Delta\omega\}}{Z_N\{v\omega_c + \Delta\omega\}} \left( \frac{Z_{NFOLD}\{m\omega_c + \Delta\omega\} (R_{SW} + Z_{BB}\{\Delta\omega\}/M)}{M|Sw[m]|^2 Z_{BB}\{\Delta\omega\} + Z_{NFOLD}\{m\omega_c + \Delta\omega\}} \right).
\end{aligned} \tag{3.76}$$

While if a large number of mixer phases are employed the gain becomes

$$\begin{aligned}
\lim_{M \rightarrow \infty} A_{v_{FTBPF[m,m]}}\{\Delta\omega\} = & \\
& - G_{ARB}G_M \left( \frac{(R_{SW} + Z_{BB}\{\Delta\omega\}/M)}{Z_S\{m\omega_c + \Delta\omega\} + R_{SW} + Z_{BB}\{\Delta\omega\}/M} \right).
\end{aligned} \tag{3.77}$$

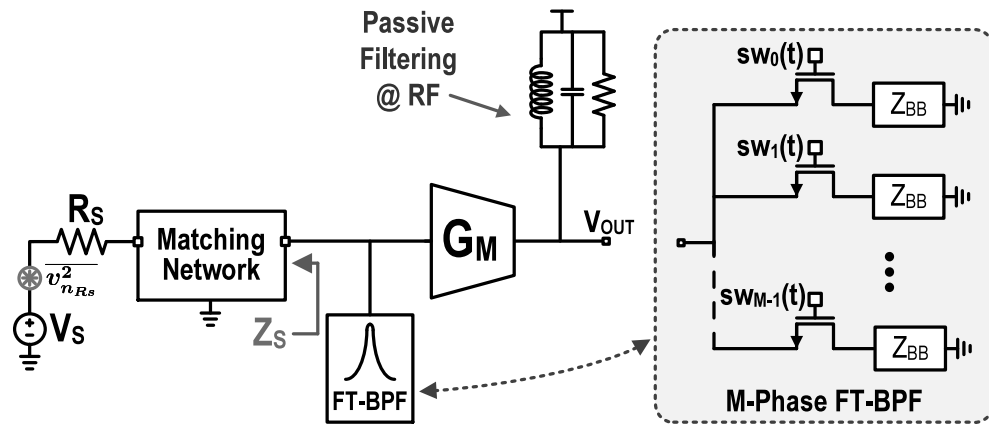
This transfer function implies high- $Q$  filtering provided  $R_{SW}$  is small and  $Z_{BB}\{\Delta\omega\}$  has a narrow bandwidth.

Relating this expression to the FTNC-RX, it can be noted that the main path can potentially function as a FT-BPF and can provide filtering to the auxiliary path signals. However, any filtering is generally limited to a few dB, since the noise-cancelling is optimized by making switch resistance close to  $50\Omega$  and the baseband impedance small. By contrast, a good FT-BPF requires a small switch resistance and a large baseband impedance (ideally a capacitor).

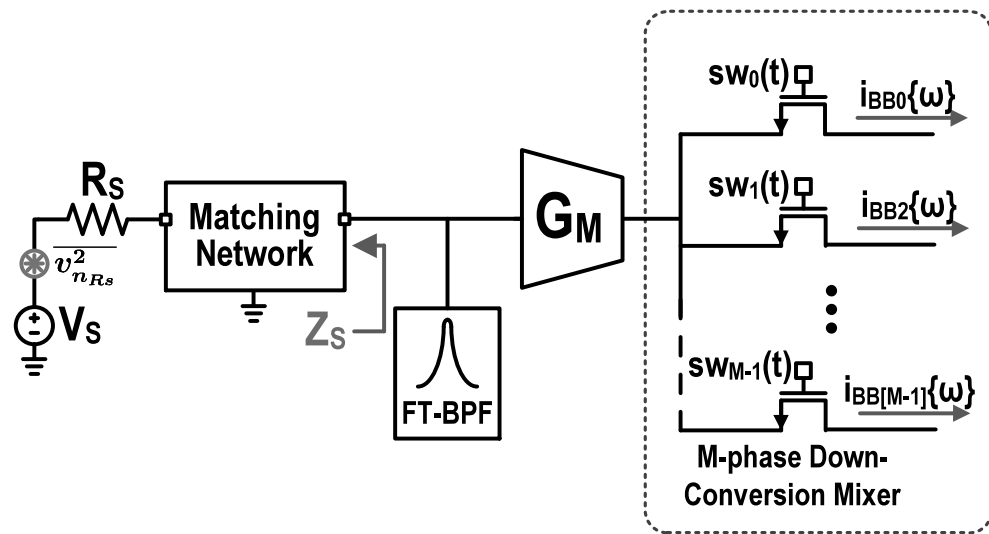
### 3.9 Conclusion

A complete LTV analysis of the proposed *frequency-translational noise-cancelling* receiver (FTNC-RX) has been presented. Accurate expressions for both the gain and the noise of system have been derived.

While it is theoretically possible to design a mixer-first receiver with arbitrarily low noise figure, practical issues ultimately limit the achievable noise performance of such a



(a) Receiver with RF voltage gain.



(b) Direct downconversion of RF current.

Figure 3.17: Receivers topologies employing high- $Q$  frequency translational bandpass filters (FT-BPF).

design. The FTNC-RX is less susceptible to these issues and is, therefore, a more suitable topology for low noise, wideband applications.



## CHAPTER 4

# Phase Noise in $LC$ Oscillators: A Phasor-Based Analysis of a General Result and of Loaded $Q$

### 4.1 Introduction

The past twenty years have seen significant progress in the understanding of noise in electrical oscillators. During this period, the design community has advanced beyond Leeson's classic linear analysis [42] and adopted analysis methods that more appropriately capture the time-varying and large-signal nature of any realizable oscillator. While lacking the rigour of mathematically involved analysis [43] [44] [45], the linear-time variant (LTV) approach to analyzing noise in oscillators has gained the most traction in the circuit design community. This is no doubt attributable to the high accuracy of its predictions and the relative simplicity of the mathematical tools employed. Two LTV methods stand out: the impulse-response-based approach proposed by Hajimiri and Lee [46] [47], and the phasor-based approach pioneered by Samori et al. [48], Huang [49], and Rael and Abidi [50].

Central to Hajimiri and Lee's work is the derivation of the impulse sensitivity function (ISF) that shows how the phase disturbance produced by a current impulse depends on the time at which the impulse is injected; for example, a current impulse injected at a zero-crossing will generate a greater phase shift than if injected at the peak of an oscillation. The work is very intuitive and, if applied correctly, results in accurate predictions; notably Andreani et al. [51] [52] [53] [54] have used the ISF to develop closed form expressions for the most common  $LC$  oscillators. More recently, Bank [55] used the ISF to derive a remarkable result, namely that the noise factor of a nearly-sinusoidal  $LC$  oscillator, under

certain common conditions, is largely independent of the specific operation of individual transistors in the active circuitry. Mazzanti and Andreani [56] then, aware of Bank’s work, provided a novel proof of this same general result. Their work also employed the ISF.

The alternative phasor-based analysis method, which is adopted in [48] [50] [57] [58], looks at phase noise generation mechanisms in the frequency domain. While this approach is practical only for nearly-sinusoidal  $LC$  oscillators, it offers an alternative perspective and does not require the development of specific theoretical concepts such as Hajimiri and Lee’s ISF. Nevertheless, published work expanding on this method appears curiously to have dried up after Kouznetsov and Meyer [57]. As in the ISF approach, all noise sources are considered stationary or cyclostationary (with respect to the oscillation frequency) [59], and both calculations involve a given source acting on a “noiseless” oscillator. Thus one would expect that the two approaches would yield the same results, with neither approach exhibiting an obvious advantage over the other. In this work we are able to show that this is, indeed, the situation.

Building on previous results [50] [58] [60], and drawing from the work of Samori et al. [48], we re-derive the general result using phasor-based analysis, which does not rely on the ISF. In doing so, we reconcile the two widely cited approaches (ISF & phasor-based) and show how they are fundamentally the same<sup>1</sup>; both approaches result in equivalent expressions and suffer the same limitations. We focus on the negative-gm  $LC$  model (Fig. 4.1), for which we present simple equations that quantify output noise resulting from phase fluctuations. Moreover, we derive a closed form expression for output noise arising from *amplitude* fluctuations, something the ISF approach has so far failed to do. Finally, we show how the analysis can be extended to account for topologies, such as the voltage-biased oscillator, for which the general result is not applicable. This enables us to gain insight into tank loading and derive equations to quantify  $Q$  degradation.

Section 4.2 introduces the negative-gm model, and outlines our approach.

---

<sup>1</sup>As applied to phase fluctuations in  $LC$  oscillators.

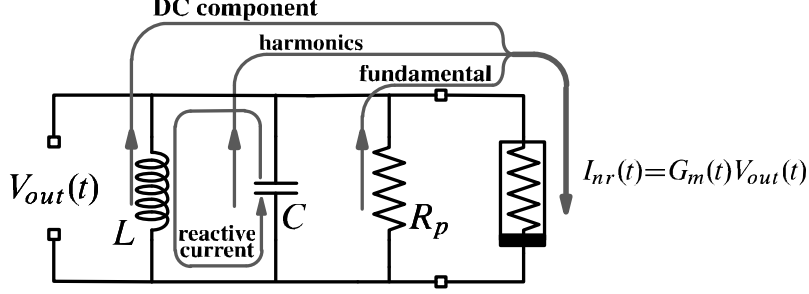


Figure 4.1: A generic negative-gm  $LC$  oscillator model.

## 4.2 Oscillator Preliminaries

### 4.2.1 The Negative-Gm Oscillator

A nearly-sinusoidal  $LC$  oscillator can be modeled as a lossy resonator in parallel with an energy-restoring nonlinearity, as shown in Fig. 4.1. Assuming oscillation conditions are satisfied, Leeson [42] describes the output noise PSD resulting from phase fluctuations as

$$\widehat{v_{n_{PM}}^2} = 2kTFR_p \left( \frac{\omega_0}{2Q\omega_m} \right)^2, \quad (4.1)$$

where  $Q$  is the quality factor of the resonator,  $\omega_0$  is the oscillation frequency, and  $\omega_m$  is a frequency offset from  $\omega_0$ . The noise factor  $F$ , left unspecified by Leeson, is the focus of this chapter. Leeson assumes that output noise arising from amplitude fluctuations,  $\widehat{v_{n_{AM}}^2}$ , is negligible. Phase noise is then defined as the total single-sideband output noise normalized to the power in the oscillator's sinusoidal output, i.e.

$$\mathcal{L}\{\omega_m\} = \frac{\widehat{v_n^2}}{A_c^2/2} = \frac{\widehat{v_{n_{PM}}^2} + \widehat{v_{n_{AM}}^2}}{A_c^2/2}, \quad (4.2)$$

where  $A_c$  is the oscillation amplitude<sup>2</sup>.

Employing the quasi-sinusoidal approximation [61], any single-phase nearly-sinusoidal  $LC$  topology can be redrawn (by means of a Norton or Thevenin transformation) in the form of this negative-gm  $LC$  model. This approximation also allows us to refer every noise

<sup>2</sup>Output noise consists of two components: output noise due to phase fluctuations and output noise due to *amplitude* fluctuations. As such, the term “phase noise” is somewhat of a misnomer as it is a measure of normalized output noise. However, this ambiguity is generally unimportant, since noise resulting from amplitude fluctuations is generally small at close-in offsets.

source (cyclostationary or stationary) to an appropriate current noise source that appears differentially across the model’s resonator. These manoeuvres are permissible because tones and noise at other frequencies are significantly attenuated by the resonator and so do not contribute to the output<sup>3</sup>.

Given this simplification, our approach is as follows: two transfer functions are derived that map a small AM or a PM resonator-referred current source to the oscillator’s output (Sec. 4.3). We then show, in Sec. 4.4, how an arbitrary cyclostationary white noise source can be decomposed into its AM and PM components, which can make use of these transfer functions. In Sec. 4.5, we apply this theory to the negative-gm *LC* model to generate expressions for output noise; in doing so, we quantify  $F$  and re-derive the Bank’s general result [55]. These expressions are applied to well-known topologies in Sec. 4.6. Section 4.7 deals with topologies where the general result is not applicable.

We conclude this section by looking at the energy conservation requirement of an *LC* oscillator, which will be used to simplify later analysis.

#### 4.2.2 Constraints from Energy Conservation

To sustain oscillation, the average power dissipated in the lossy tank must equal the average power delivered to the tank by the nonlinearity, i.e.,

$$\frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} P_{tank}(t) dt = -\frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} P_{nr}(t) dt, \quad (4.3)$$

where  $P_{tank}(t)$  is the instantaneous power dissipated in the lossy tank, and  $P_{nr}(t)$  is the instantaneous power dissipated in nonlinearity. The instantaneous conductance of the nonlinearity is defined as

$$G_m(t) = \frac{dI_{nr}(t)}{dV_{out}(t)} = \frac{dI_{nr}(t)}{dt} \frac{dt}{dV_{out}(t)}. \quad (4.4)$$

---

<sup>3</sup>This approach is similar to that adopted by Kouznetsov and Meyer [57]. However their work considers only stationary noise sources, which is a serious limitation.

Using this expression, and assuming the output is of the form  $V_{out} = A_c \cos(\omega_0 t)$ , the current drawn by the nonlinearity can be described as

$$\begin{aligned} I_{nr}(t) &= I_{nrDC} + \int_{-\infty}^t G_m(\tau) \frac{dV_{out}(\tau)}{d\tau} d\tau \\ &= I_{nrDC} - \omega_0 A_c \int_{-\infty}^t G_m(\tau) \sin(\omega_0 \tau) d\tau, \end{aligned} \quad (4.5)$$

and the average power dissipated by the nonlinearity is

$$\begin{aligned} \langle P_{NR} \rangle &= \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} V_{out}(t) I_{nr}(t) dt \\ &= \frac{-\omega_0 A_c^2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \cos(\omega_0 t) \left( \int_{-\infty}^t G_m(\tau) \sin(\omega_0 \tau) d\tau \right) dt. \end{aligned} \quad (4.6)$$

If we switch the order of the integrals, we may write

$$\begin{aligned} \langle P_{NR} \rangle &= -\frac{\omega_0 A_c^2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} \int_{\tau}^{\frac{T}{2}} \cos(\omega_0 t) G_m(\tau) \sin(\omega_0 \tau) dt d\tau \\ &= \frac{A_c^2}{2T} \int_{-\frac{T}{2}}^{\frac{T}{2}} G_m(\tau) (1 - \cos(2\omega_0 \tau)) d\tau. \end{aligned} \quad (4.7)$$

It is assumed that the nonlinearity is purely resistive and thus memoryless. Any memoryless nonlinear resistance excited by a zero-initial-phase cosine wave, as in this case, will produce an output that is a real and even function of time. Accordingly, the above expression may be written as

$$\langle P_{NR} \rangle = \frac{A_c^2}{2} (G_M[0] - G_M[2]), \quad (4.8)$$

where  $G_M[k]$  describes the Fourier series coefficients of the instantaneous conductance,  $G_m(t)$ <sup>4</sup>. As per Eqn. (4.3), sustained oscillations mandate that  $\langle P_{TANK} \rangle + \langle P_{NR} \rangle = 0$ . Combining this requirement with Eqn. (4.8), and noting that  $\langle P_{TANK} \rangle = A_c^2 / (2R_p)$  leads to the identity

$$G_{MEFF} = G_M[0] - G_M[2] = -\frac{1}{R_p}, \quad (4.9)$$

which is the effective conductance derived by Samori et al. [48]. The mixing action of the ideal sinusoidal output with the time-varying conductance ensures that only components

---

<sup>4</sup>This work uses the complex exponential form of the Fourier series that defines the coefficients in terms of the double-sided frequency spectrum, i.e.,  $x(t) = \sum_{k=-\infty}^{\infty} X[k] e^{jk\omega_0 t}$ .

at DC and the 2<sup>nd</sup> harmonic ultimately contribute to  $G_{MEFF}$ . This energy-conservation requirement (i.e. power dissipated in the tank is equal to power returned by the nonlinearity), is central to our re-derivation of the Bank’s general result. It is interesting to note the similarity between the  $G_{MEFF}$  of the time-varying conductance derived above and the  $C_{EFF}$  of the time-varying capacitance derived in [61].

### 4.3 A “Noiseless” Oscillator Injected with a Small Current Source

We now analyze the effect of a small external current injected differentially into a “noiseless” negative-gm oscillator. We assume that noise does not shift the average frequency of oscillation but merely spreads the spectrum across symmetrical noise sidebands. This analysis leads to transfer functions that maps a small differentially-referred current source to the oscillator’s output.

#### 4.3.1 Recognizing Phase and Amplitude Modulating Sidebands

Consider a pair of sidebands around a large carrier, as in Fig 4.2(a). Assume the magnitudes of the sidebands are equal and small with respect to the carrier. If the relative phases of the sidebands are such that their sum is orthogonal at all times with the carrier, phase modulation results. This modulation is shown in the phasor plot, Fig. 4.2(b). Alternatively, if the sum is always colinear to the carrier, amplitude modulation results, as shown in Fig. 4.2(c). A single-sideband around a carrier can always be decomposed into equal PM and AM sidebands as shown in Fig. 4.2(d) [62].

#### 4.3.2 Response of the Nonlinearity to AM/PM Modulated Carriers

To properly quantify noise in the negative-gm model, a correct understanding of the response of the nonlinearity to both AM and PM modulated carriers is required. The most

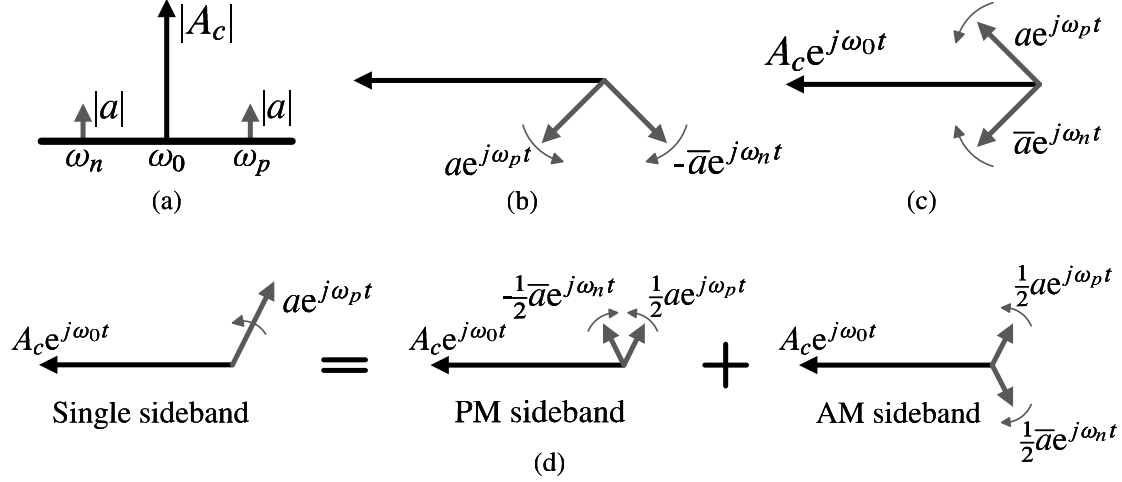


Figure 4.2: (a) Sideband magnitudes do not reveal modulation type; (b) PM sidebands: sum is orthogonal to carrier; (c) AM sidebands: sum is colinear with carrier; (d) A single sideband around can be decomposed into equal PM and AM sidebands.

general explanation we have encountered is that presented by Samori et al. [48]<sup>5</sup>. Essentially, Samori et al. model the nonlinearity as an arbitrary nonlinear conductance followed by a bandpass filter, as shown in Fig. 4.3(a). The bandpass filter, which is simply the oscillator's tank, suppresses terms that do not lie close to the carrier frequency.

Using this approach, Samori et al. demonstrate that, in the case of a phase modulated signal, the sideband-to-carrier ratio at the input is identical to the sideband-to-carrier ratio at the output, i.e.,

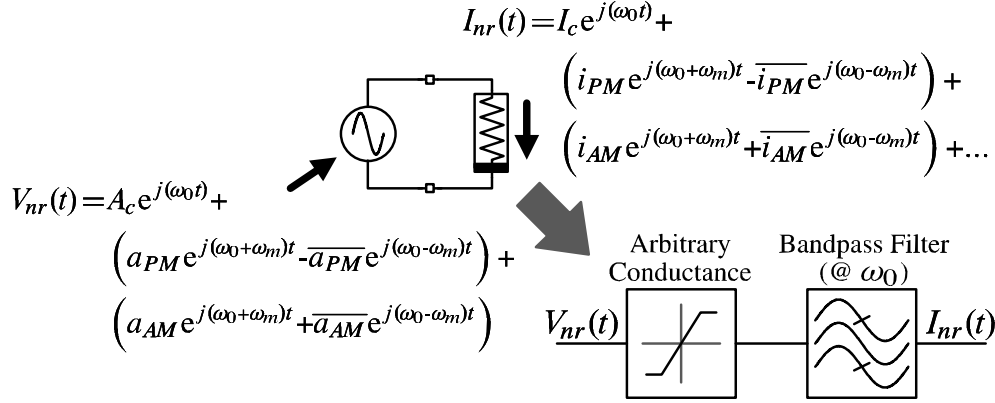
$$\frac{i_{PM}}{I_c} = \frac{a_{PM}}{A_c}. \quad (4.10)$$

The above expression differs in notation from Samori et al.; a complete proof and discussion of the above expression is given in [58]. Extending this analysis to the case of an AM signal, Samori et al. show that the sideband-to-carrier ratio at the input is related to the sideband-to-carrier ratio at the output as follows

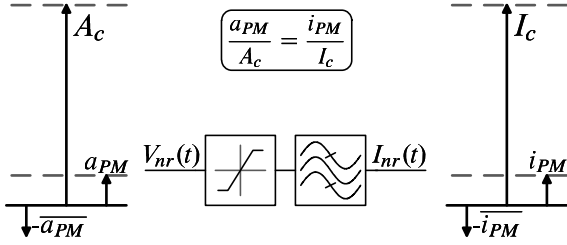
$$\frac{i_{AM}}{I_c} = \left( \frac{G_M[0] + G_M[2]}{G_M[0] - G_M[2]} \right) \frac{a_{AM}}{A_c}. \quad (4.11)$$

<sup>5</sup>The narrowband response of a nonlinearity to a noisy signal has been investigated by many others (see discussion in [58]). Indeed, using an analysis method developed for mixers [63], [50] quantified such a response for the specific case of the current-biased topology.

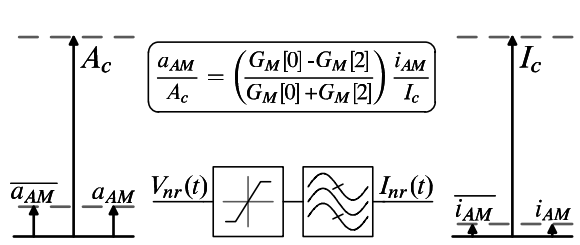
The response of the nonlinearity to a PM carrier is visualized in Fig. 4.3(b), while the nonlinearity's response to an AM carrier is visualized in Fig. 4.3(c).



(a) Nonlinearity modeled as a memoryless conductance followed by a bandpass filter.



(b) Response of the band-limited nonlinearity to phase modulated carrier.



(c) Response of the band-limited nonlinearity to amplitude modulated carrier.

Figure 4.3: Response of the nonlinearity to an AM and PM signal.

### 4.3.3 Response of the Negative-Gm Oscillator to an External Current Source

Consider a current source,  $i_n$ , in parallel with a noiseless negative-gm oscillator, as shown in Fig. 4.4. Assume the circuit supports a sustained oscillation and the current source has two frequency components at  $\omega_0 \pm \omega_m$ . As shown in the previous section, the nonlinearity can be viewed as a voltage-to-current transfer function that preserves the frequency and phase (but not the magnitude) of a carrier and any sidebands, and does not produce frequency components with significant amplitudes at other frequencies<sup>6</sup>. This simplification coupled

<sup>6</sup>Since the conductance is, in general, strongly nonlinear, current components of significant magnitudes are generated at frequencies other than the fundamental. These components, however, are far from the oscillation frequency and are greatly attenuated by the tank.



with the assumption of a linear tank, ensures that the output of the oscillator is of the form

$$V_{out}(t) = A_c e^{j\omega_0 t} + (a_{PM} e^{j\omega_p t} - \overline{a_{PM}} e^{j\omega_n t}) + (a_{AM} e^{j\omega_p t} + \overline{a_{AM}} e^{j\omega_n t}) , \quad (4.12)$$

where  $\bar{a}$  denotes the conjugate of complex number  $a$ ,  $\omega_p = \omega_0 + \omega_m$ ,  $\omega_n = \omega_0 - \omega_m$ ,  $a_{PM}$  is the PM sideband component, and  $a_{AM}$  is the AM sideband component. This output

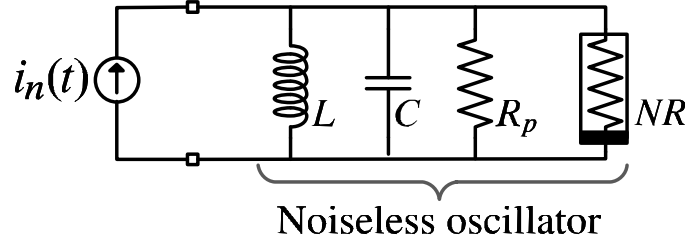


Figure 4.4: A noiseless negative-gm oscillator excited by an external current source.

waveform excites the following current from the nonlinearity

$$\begin{aligned} I_{nr}(t) &= I_c e^{j\omega_0 t} + (i_{PM} e^{j\omega_p t} - \overline{i_{PM}} e^{j\omega_n t}) \\ &\quad + (i_{AM} e^{j\omega_p t} + \overline{i_{AM}} e^{j\omega_n t}) \\ &= -\frac{A_c}{R_p} e^{j\omega_0 t} - \frac{1}{R_p} (a_{PM} e^{j\omega_p t} - \overline{a_{PM}} e^{j\omega_n t}) \\ &\quad + (G_M[0] + G_M[2]) (a_{AM} e^{j\omega_p t} + \overline{a_{AM}} e^{j\omega_n t}) . \end{aligned} \quad (4.13)$$

Applying KCL to the oscillator in Fig. 4.4, we can extract an expression for the phasor  $V_{out}$ , in terms of the injected noise current and the nonlinearity current

$$V_{out}(s) = -\frac{(-i_n(s) + I_{NR}(s))sLR_p}{R_p + sL + s^2LR_pC} . \quad (4.14)$$

The Laplace transform is valid because we are relating the voltage and current by means of a linear tank. Assuming  $s = j(\omega_0 \pm \omega_m)$  and  $\omega_m \ll \omega_0$ ,

$$V_{out}\{\omega_0 \pm \omega_m\} \approx \frac{j(-i_n\{\omega_0 \pm \omega_m\} + I_{NR}\{\omega_0 \pm \omega_m\})\omega_0 LR_p}{-j\omega_0 L \pm 2R_p \left(\frac{\omega_m}{\omega_0}\right)} . \quad (4.15)$$

We can view the injected current source,  $i_n$ , as a signal that modulates the amplitude and/or phase of the fundamental of the current from the nonlinear resistor,  $I_c$ . In order to modulate the phase of  $I_c$ , the injected current needs to be of the form:

$i_n(t) = \frac{i_x}{2}e^{j(\omega_0+\omega_m)t} - \frac{\bar{i}_x}{2}e^{j(\omega_0-\omega_m)t}$ . Using Eqn. (4.12), Eqn. (4.13), and Eqn. (4.15) and solving for specific frequencies results in

$$\begin{aligned} a_{PM} + a_{AM} &= \frac{j\left(-\frac{i_x}{2} - \frac{a_{PM}}{R_p} + \left(2G_M[0] + \frac{1}{R_p}\right)a_{AM}\right)\omega_0LR_p}{-j\omega_0L + R_p\left(2\frac{\omega_m}{\omega_0}\right)} \\ -\bar{a}_{PM} + \bar{a}_{AM} &= \frac{j\left(\frac{\bar{i}_x}{2} + \frac{\bar{a}_{PM}}{R_p} + \left(2G_M[0] + \frac{1}{R_p}\right)\bar{a}_{AM}\right)\omega_0LR_p}{-j\omega_0L - R_p\left(2\frac{\omega_m}{\omega_0}\right)}. \end{aligned} \quad (4.16)$$

Solving for  $a_{PM}$  and  $a_{AM}$  gives

$$\begin{aligned} a_{PM} &= -j\frac{(i_x/2)\omega_0^2L}{2\omega_m} = (i_x/2)Z_{PM}\{\omega_0 + \omega_m\} \\ a_{AM} &= 0, \end{aligned} \quad (4.17)$$

where  $Z_{PM}\{\omega_0 + \omega_m\}$  is the impedance of the *lossless* tank. Therefore, a current source in parallel with the tank that modulates the phase of  $I_c$  will flow through an impedance defined by the lossless tank. In doing so, it will generate PM sidebands around the output carrier. External current of this form cannot cause AM sidebands. The impedance seen by this “phase modulating” injected current is shown in Fig. 4.5(a).

Similarly, it can be shown that a current source that modulates the amplitude of  $I_c$  (i.e.,  $i_n(t) = \frac{i_x}{2}e^{j(\omega_0+\omega_m)t} + \frac{\bar{i}_x}{2}e^{j(\omega_0-\omega_m)t}$ ), will generate the following sideband components

$$\begin{aligned} a_{PM} &= 0 \\ a_{AM} &= \frac{i_x/2}{\left(G_M[0] + G_M[2] + \frac{1}{R_p}\right) - \frac{2\omega_m}{j\omega_0^2L}}. \end{aligned} \quad (4.18)$$

Thus an “amplitude modulating” injected current will see the impedance shown in Fig. 4.5(b). External current of this form will generate AM sidebands only. In the extreme case of a linear oscillator (i.e. the conductance of the energy-restoring mechanism is linear,  $G_M[0] \approx -1/R_p$  and  $G_M[2] \approx 0$ ) amplitude noise will flow into the lossless tank and produce sidebands equal in magnitude to that produced by an equivalent PM current source. While a truly linear oscillator is unrealizable, it can be approximated using automatic gain control (as discussed in [57]). However, in more conventional circuits, AM sidebands at close-in offsets are generally negligible compared to PM sidebands.

While the calculations presented so far are somewhat tedious, the results are remarkably simple:

- an injected current that modulates the phase of the fundamental of the nonlinearity current will be shaped by the impedance of the *lossless* tank and generate PM sidebands around the output carrier.
- an injected current that modulates the amplitude of the fundamental of the nonlinearity current will be shaped by the *lossy* resonator of Fig. 4.5(b) and generate AM sidebands around the output carrier.

The squared impedances “seen” by phase and amplitude modulating currents are plotted in Fig. 4.6, and given by

$$\boxed{|Z_{PM}\{\omega_0 \pm \omega_m\}|^2 = \left(\frac{\omega_0^4 L^2}{4\omega_m^2}\right) = \left(\frac{\omega_0}{2Q\omega_m}\right)^2 R_p^2} \quad (4.19)$$

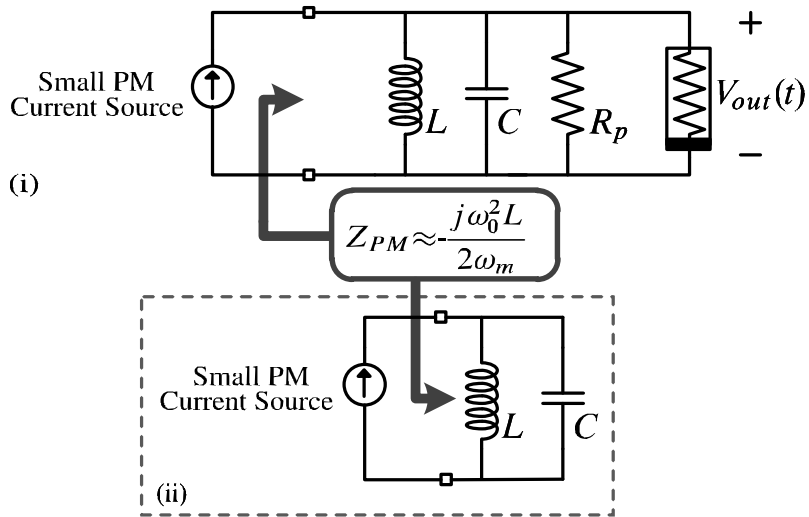
$$\boxed{|Z_{AM}\{\omega_0 \pm \omega_m\}|^2 = \frac{1}{(G_M[0] + G_M[2] + \frac{1}{R_p})^2 + \left(\frac{2\omega_m}{\omega_0^2 L}\right)^2}}, \quad (4.20)$$

where  $G_M[k]$  is calculated with respect to a zero-initial-phase cosine output voltage. Since we will ultimately deal with current noise, the above equations can be viewed as transfer functions that map the AM and PM components of resonator-referred differential noise current to output noise.

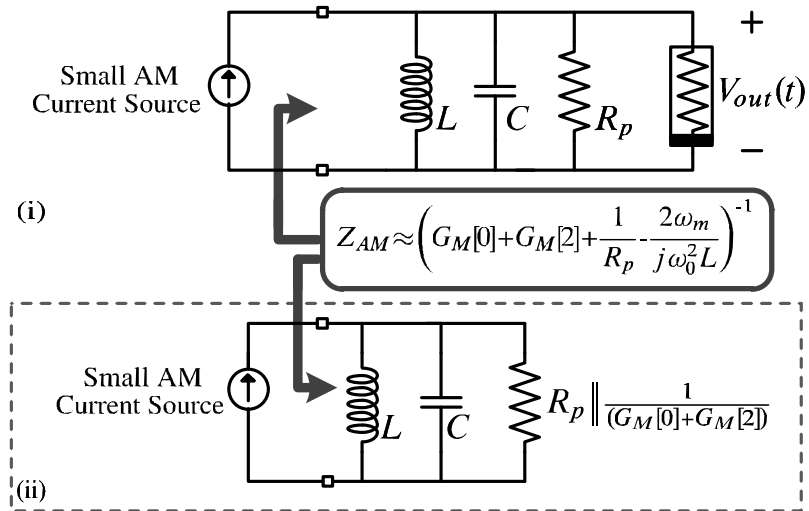
This analysis can be viewed as an extension of the work of Samori et al. [48] and Kouznetsov and Meyer [57]. The approach is similar in spirit to that presented by Samori et al. [48], although he did not frame the theory in terms of generalized transfer functions; Kouznetsov and Meyer [57] derived a transfer function that maps a stationary current noise to output noise, but did not consider correlated sidebands (i.e. AM/PM sidebands). The exact approach, however, is a generalized version of that laid out in [58], which was itself a refinement of [50]. Indeed, in the limiting case of a “hard-switching” linearity, the above analysis degenerates into that presented in [50]<sup>7</sup>.

---

<sup>7</sup> [50] was based on previous work on mixers [63] and used ABCD parameters to deal with carrier sidebands. In [58], the approach was simplified by adopting complex phasor notation, and further refined using results from [64] and Samori et al. [48].



(a) Phase modulating case: (i) PM current injected into oscillator; (ii) Impedance seen by PM current source.



(b) Amplitude modulating case: (i) AM current injected into oscillator; (ii) Impedance seen by AM current source.

Figure 4.5: Differential current source acting on a “noiseless” oscillator.

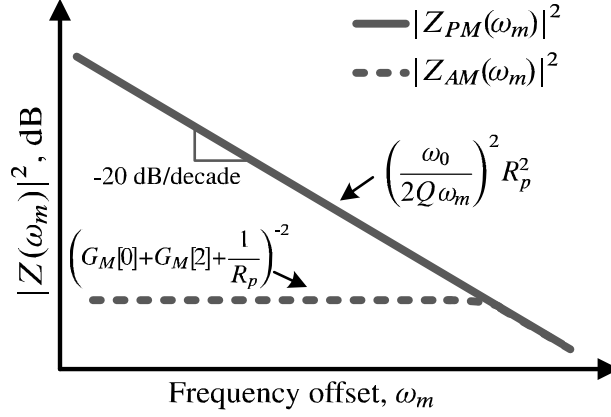


Figure 4.6: Squared impedance seen by phase and amplitude modulating currents.

#### 4.4 Decomposition of a Resonator-Referred Cyclostationary White Noise Source

In the previous section, we derived transfer functions (Eqn. (4.19) & Eqn. (4.20)) that facilitate the mapping of small AM and PM current sources (referred across the tank) to the oscillator's output. In this section, we show how to decompose an arbitrary cyclostationary white noise source [59] into its AM and PM components. These AM/PM components can then be applied directly to Eqn. (4.19) & Eqn. (4.20).

Consider again the noiseless oscillator shown in Fig. 4.4. In this instance, assume that the external current source,  $i_n$ , is a noise source that is cyclostationary at the oscillation frequency. We can model this current source as a stationary white noise source,  $i_x$ , modulated by an arbitrary periodic real-valued waveform,  $w(t)$  [59]. Accordingly,  $i_n$  will have a time-varying power spectral density equal to

$$\widehat{i}_n^2 = \widehat{i}_x^2 w^2(t). \quad (4.21)$$

The modulation of  $i_x(t)$  and  $w(t)$  is shown in Fig. 4.7. The Fourier coefficients of the  $\omega_0$ -periodic signal  $w(t)$  are shown in Fig. 4.8. The cyclostationary spectrum is found by first modelling white noise as an infinite number of sinusoids separated in frequency by 1 Hz and uncorrelated in phase [62]. Consider one such sinusoid located close to  $k^{\text{th}}$  harmonic

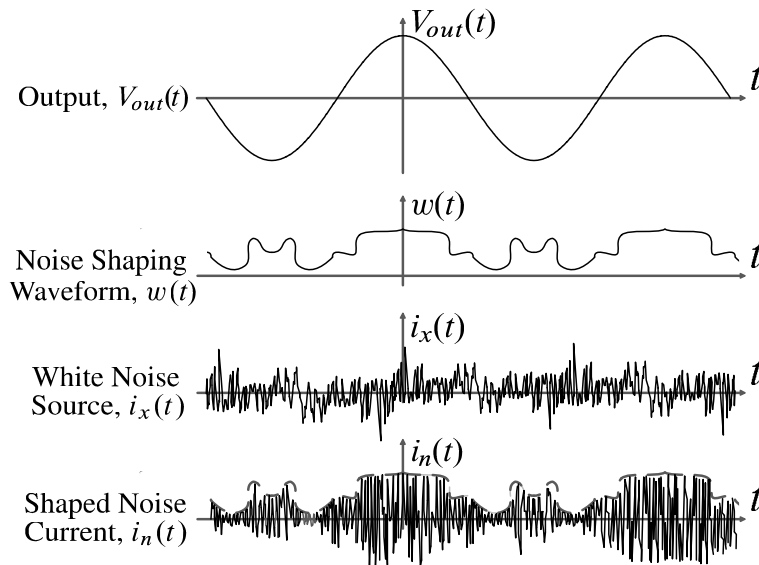


Figure 4.7: Cyclostationary white noise modeled as a white noise source modulated by a periodic waveform.

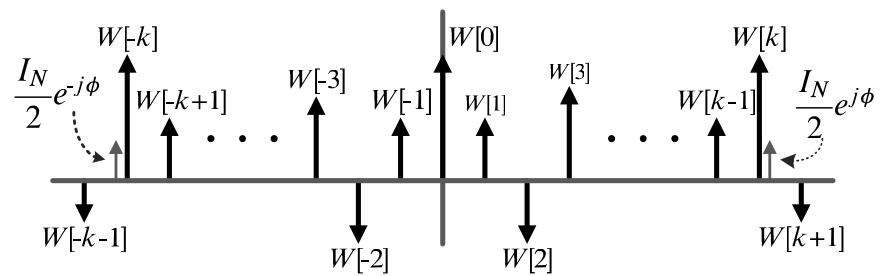


Figure 4.8: Frequency spectrum of arbitrary waveform,  $w(t)$ .

of the periodic modulation waveform (see Fig. 4.8),

$$\begin{aligned} i_{n_k}(t) &= I_N \cos((k\omega_0 + \omega_m)t + \phi) \\ &= \frac{I_N}{2} e^{j\phi} e^{j(k\omega_0 + \omega_m)t} + \frac{I_N}{2} e^{-j\phi} e^{-j(k\omega_0 + \omega_m)t}, \end{aligned} \quad (4.22)$$

where  $I_N$  is an arbitrary constant, and  $\phi$  is an arbitrary phase. Mixing  $i_{n_k}(t)$  with the waveform  $w(t)$  results in the following components around the fundamental:

$$\left. \begin{aligned} @ \omega_0 + \omega_m &: a = W[-k + 1] \frac{I_N}{2} e^{j\phi} \\ @ \omega_0 - \omega_m &: b = W[k + 1] \frac{I_N}{2} e^{-j\phi} \end{aligned} \right\} \text{pos freqs.} \\ \left. \begin{aligned} @ -\omega_0 + \omega_m &: \bar{b} = W[-k - 1] \frac{I_N}{2} e^{j\phi} \\ @ -\omega_0 - \omega_m &: \bar{a} = W[k - 1] \frac{I_N}{2} e^{-j\phi} \end{aligned} \right\} \text{neg freqs.} \quad (4.23)$$

The output voltage,  $V_{out}(t) = A_c \cos(\omega_0 t)$  excites a current from the nonlinearity whose fundamental component is  $I_c(t) = -(A_c/R_p) \cos(\omega_0 t)$ . Knowing this, we can construct the phasor diagrams shown in Fig. 4.9, which enables us to decompose the resulting sidebands into AM and PM sidebands. As a result of  $i_{n_k}$ , the total power<sup>8</sup> of the phase modulating sidebands around the fundamental is calculated as

$$\mathcal{S}_{PM}(k) = \frac{1}{4} \left( |a - \bar{b}|^2 + |\bar{a} - b|^2 \right) = \frac{1}{2} \left( |a - \bar{b}|^2 \right). \quad (4.24)$$

Substituting the values for  $a$  and  $\bar{b}$  from Eqn. (4.23) gives

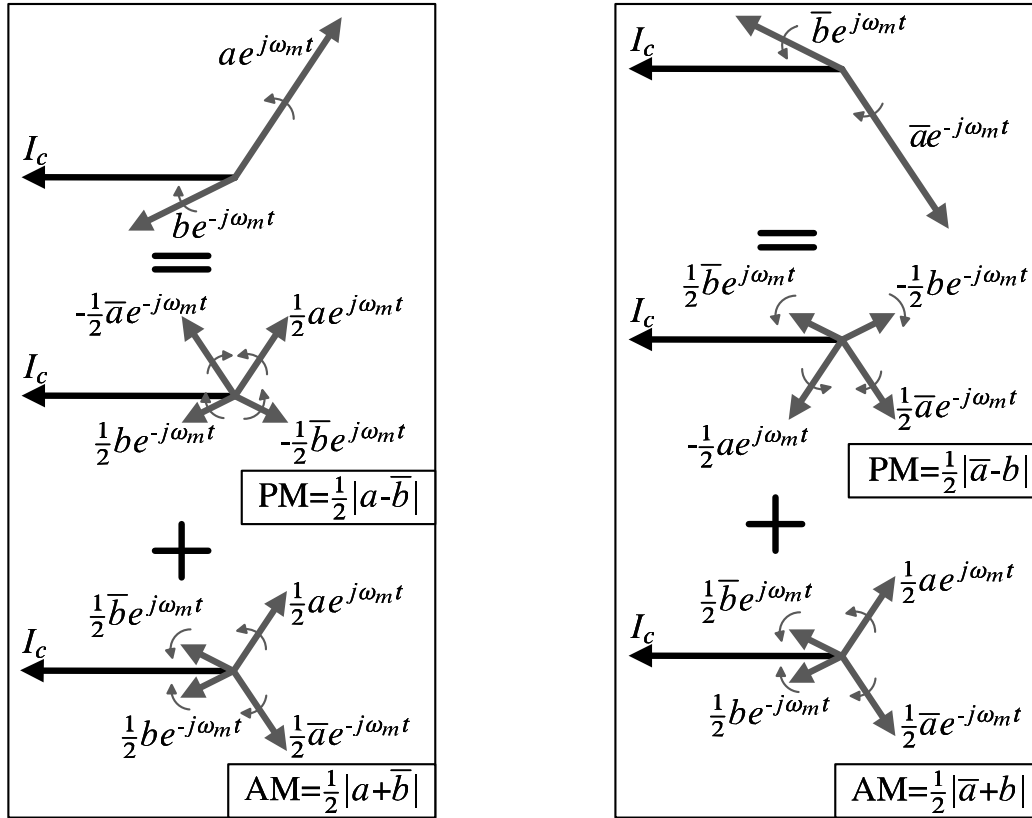
$$\mathcal{S}_{PM}(k) = \left( \frac{I_N^2}{8} \right) |W[-k + 1] - W[-k - 1]|^2. \quad (4.25)$$

Summing  $k$  from  $-\infty$  to  $\infty$  accounts for noise around all harmonics at both  $k\omega_0 - \omega_m$  and  $k\omega_0 + \omega_m$ ,

$$\begin{aligned} \mathcal{S}_{PM_{TOT}} &= \sum_{k=-\infty}^{\infty} \mathcal{S}_{PM}(k) \\ &= \left( \frac{I_N^2}{8} \right) \sum_{k=-\infty}^{\infty} \left( 2|W[k]|^2 - W[-k + 1] \overline{W[-k - 1]} - W[-k - 1] \overline{W[-k + 1]} \right) \\ &= \left( \frac{I_N^2}{8} \right) \sum_{k=-\infty}^{\infty} \left( 2|W[k]|^2 - W[-k + 1]W[k + 1] - W[-k - 1]W[k - 1] \right). \end{aligned} \quad (4.26)$$

---

<sup>8</sup>Defined in terms of the single-sided frequency spectrum.



(a) Positive frequencies ( $e^{j\omega_m t}$  component of each phasor is not shown, but is assumed).

(b) Negative frequencies ( $e^{-j\omega_m t}$  component of each phasor is not shown, but is assumed).

Figure 4.9: Phasor diagrams.



Substituting  $(I_N^2/2) = \widehat{i_x^2}$  into the above expression gives the PSD of the noise current that modulates the phase of the fundamental of the nonlinear current,

$$\widehat{i_{n_{PM}}^2} = \frac{\widehat{i_x^2}}{4} \left( \sum_{k=-\infty}^{\infty} 2|W[k]|^2 - \sum_{k=-\infty}^{\infty} W[k]W[2-k] - \sum_{k=-\infty}^{\infty} W[k]W[-2-k] \right). \quad (4.27)$$

To simplify further, we recognize that

$$p(t) \doteq w(t)w(t) \xrightarrow{FS; \omega_0} P[k] = \sum_{l=-\infty}^{\infty} W[l]W[k-l] \quad (4.28)$$

and therefore, we may write  $\widehat{i_{n_{PM}}^2}$  as follows:

$$\boxed{\widehat{i_{n_{PM}}^2} = \left( \frac{1}{2}P[0] - \frac{1}{4}P[2] - \frac{1}{4}P[-2] \right) \widehat{i_x^2}}, \quad (4.29)$$

where  $P[k]$  is the Fourier series component of the square of the noise shaping function,  $w(t)$ . Using a similar derivation and employing the same assumptions, it can be shown that the AM component is given by

$$\boxed{\widehat{i_{n_{AM}}^2} = \left( \frac{1}{2}P[0] + \frac{1}{4}P[2] + \frac{1}{4}P[-2] \right) \widehat{i_x^2}}. \quad (4.30)$$

Thus, if we know the noise shaping waveform (i.e.  $w(t)$ ), we can easily decompose a noise source into its AM/PM components. This decomposition, coupled with the transfer functions described by Eqn. (4.19) & Eqn. (4.20), allow us to quantify a given source's contribution to output noise.

## 4.5 The Noise Factor of the Negative-Gm Model

In this section, we use the preceding analysis to derive an expression for noise in the negative-gm oscillator (Fig. 4.1). In doing so, we are using our phasor-based approach instead of Bank's ISF analysis to re-derive his general result [55] [56]. Our approach also enables us to quantify, for the first time, noise due to amplitude fluctuations.

### 4.5.1 Noise from Resonator Losses

Decomposing the noise associated with the tank resistance,  $R_p$ , is a trivial case of the noise analysis presented in the previous section; the noise current,  $i_{res} = 4kT/R_p$ , is simply a white noise source, modulated by the constant window,  $w(t) = 1$ . Accordingly,

$$p(t) = w(t)w(t) = 1 \xleftrightarrow{FS; \omega_0} P[k] = \delta[k]. \quad (4.31)$$

Therefore

$$\widehat{i_{resPM}^2} = \widehat{i_{resAM}^2} = \frac{2kT}{R_p}, \quad (4.32)$$

which is half the total resistor current noise.

### 4.5.2 Noise from the Nonlinearity

The noise from the nonlinearity is modeled as a cyclostationary white noise current source,  $i_{nr}$ , in parallel with the tank. We assume, further, that the time-varying PSD of this current source is proportional to the instantaneous conductance of the nonlinearity itself<sup>9</sup>, i.e.,

$$\widehat{i_{nr}^2} = -\widehat{i_x^2} G_m(t), \quad (4.33)$$

where

$$\widehat{i_x^2} = 4kT\alpha \quad (4.34)$$

is an arbitrary stationary white noise source,  $\alpha$  is an arbitrary noise intensity constant, and  $G_m(t)$  is the instantaneous conductance. Accordingly, the noise current,  $i_{nr}$ , is simply the white noise source,  $i_x$ , modulated by the window  $w(t) = \sqrt{-G_m(t)}$ . In general, a memoryless nonlinearity excited by a zero-initial-phase cosine wave will generate a  $G_m(t)$  waveform that is a real and even function of time. We further assume that  $G_m(t) \leq 0$  at

---

<sup>9</sup>As will be shown in Sec. 4.6, this is typically the case for CMOS oscillators when only channel noise is considered. It is also a good approximation for high-beta bipolar oscillators where collector shot noise typically dominates. However, if noise due to gate resistance (in CMOS oscillators) or noise arising from parasitic base resistance (in bipolar oscillators) dominates, the resultant conductance noise will be proportional to  $G_m^2(t)$ . The latter case is examined in [48].

all times<sup>10</sup>. Therefore,

$$p(t) = w(t)w(t) = \sqrt{-G_m(t)}\sqrt{-G_m(t)} = -G_m(t), \quad (4.35)$$

and thus we can deduce from Eqn. (4.29) and Eqn. (4.30) that

$$\begin{aligned} \widehat{i_{nrPM}^2} &= -\frac{1}{2} (G_M[0] - G_M[2]) \widehat{i_x^2} \\ \widehat{i_{nrAM}^2} &= -\frac{1}{2} (G_M[0] + G_M[2]) \widehat{i_x^2}, \end{aligned} \quad (4.36)$$

since  $G_M[2] = G_m[-2]$ . Recognizing that the PM component is directly proportional to the effective conductance of the nonlinearity defined in Eqn. (4.9) we write

$$\widehat{i_{nrPM}^2} = \frac{\widehat{i_x^2}}{2R_p} = \frac{2kT\alpha}{R_p}. \quad (4.37)$$

Amazingly, given the above assumptions, the component of  $i_{nr}$  that is responsible for phase modulation of the carrier current (and thus phase noise) is completely *independent* of the shape of the nonlinear characteristic. Put another way: a hard-limiting and soft-limiting nonlinearity will inject exactly the same PM noise into the oscillator.

### 4.5.3 The General Result and Implications

The phase modulating components of the resistor and nonlinearity noise will be shaped by Eqn. (4.19), while the amplitude modulating components will be shaped by Eqn. (4.20). Thus the output voltage noise that causes phase fluctuations is

$$\widehat{v_{nPM}^2} = \left( \widehat{i_{resPM}^2} + \widehat{i_{nrPM}^2} \right) |Z_{PM}\{\omega_0 \pm \omega_m\}|^2, \quad (4.38)$$

which evaluates to

$$\boxed{\widehat{v_{nPM}^2} = 2kT(1 + \alpha)R_p \left( \frac{\omega_0}{2Q\omega_m} \right)^2}. \quad (4.39)$$

Equating this expression with Eqn. (4.1), we see that the noise factor depends only on the noise intensity constant  $\alpha$  and is given by

$$\boxed{F = 1 + \alpha}. \quad (4.40)$$

---

<sup>10</sup>This is not always the case (see Sec. 4.7), and is merely a criterion of the general result.

Equivalently, the output noise due to amplitude fluctuations is

$$\widehat{v_{n_{AM}}^2} = \left( \widehat{i_{res_{AM}}^2} + \widehat{i_{nr_{AM}}^2} \right) |Z_{AM}(\omega_0 \pm \omega_m)|^2, \quad (4.41)$$

which evaluates to

$$\widehat{v_{n_{AM}}^2} = \frac{2kT/R_p - 2kT\alpha(G_M[0] + G_M[2])}{\left(G_M[0] + G_M[2] + \frac{1}{R_p}\right)^2 + \left(\frac{2\omega_m}{\omega_0^2 L}\right)^2}, \quad (4.42)$$

where  $G_M[k]$  is calculated with respect to a zero-initial-phase cosine output voltage. As stated before,  $\widehat{v_{n_{AM}}^2} \ll \widehat{v_{n_{PM}}^2}$  at close-in offsets and can be ignored. Therefore: In a nearly sinusoidal  $LC$  oscillator, if the energy restoring nonlinearity is memoryless, possesses an instantaneous small-signal conductance that is negative throughout the oscillation, and has a noise current whose PSD is proportional to the instantaneous small-signal conductance, then that oscillator's noise factor will be independent of the non-linear characteristic.

Although presented in a different form, this is the general result derived by Bank [55] and Andreani and Mazzanti [56]<sup>11</sup>. Indeed, there appears to be no quantitative difference between the phasor-based approach and the ISF approach, as it applies to output noise resulting from phase fluctuations in nearly  $LC$  sinusoidal oscillators. This is discussed in greater detail in Sec. 4.8. Output noise resulting from amplitude fluctuations has not yet been quantified using the ISF approach.

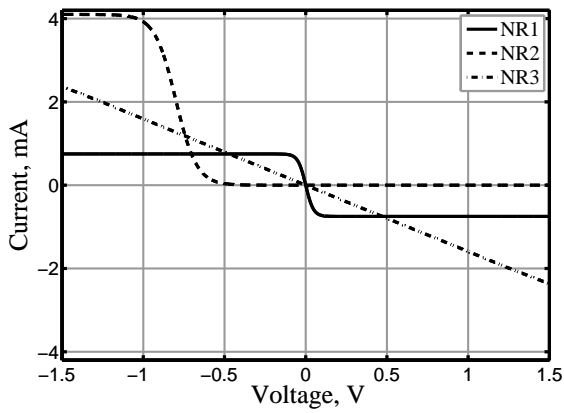
Many popular CMOS  $LC$  oscillators – notably the standard current-biased NMOS/CMOS and Colpitts topologies – satisfy Bank's general result, and thus quantifying the output noise of a given oscillator becomes a simple matter of determining the noise intensity constant  $\alpha$ .

#### 4.5.4 SpectreRF Simulations

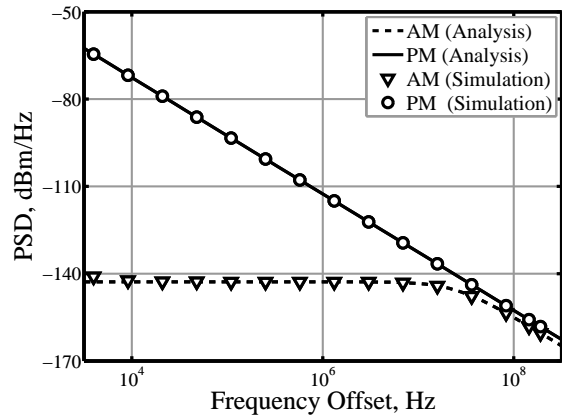
The generic negative-gm  $LC$  oscillator, shown in Fig. 4.1, was simulated using SpectreRF. The negative-gm resistor was modeled in Verilog-A, and the tank components were chosen

---

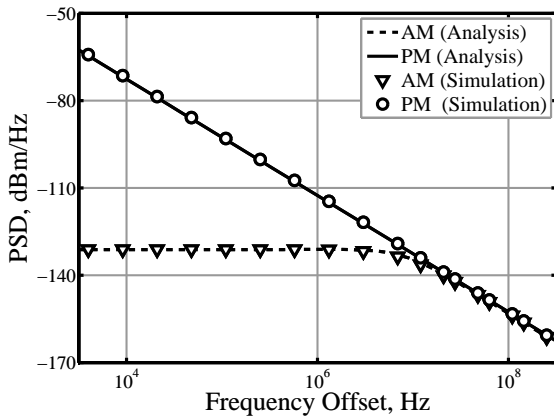
<sup>11</sup>In [56], the noise factor is presented as  $F = 1 + \gamma\eta/\alpha_m$ , where  $\gamma$  is an intensity factor,  $\eta$  is a feedback factor, and  $\alpha_m$  is a gain factor. By redrawing in the form of the negative-gm model, we do not make these distinctions, and so  $\alpha = \gamma\eta/\alpha_m$ .



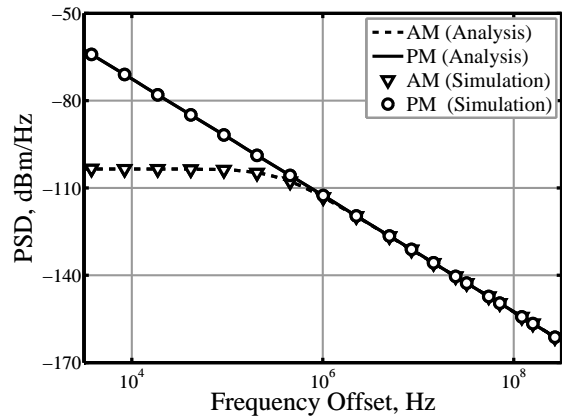
(a) Simulated IV characteristics.



(b) NR1 - AM and PM sidebands.



(c) NR2 - AM and PM sidebands.



(d) NR3 - AM and PM sidebands.

Figure 4.10: Generic negative-gm oscillator simulations.

as  $R_p = 628\Omega$ ,  $L = 5\text{nH}$ , and  $C = 5\text{pH}$ . Three different I-V characteristics, shown in Fig. 4.10(a), were simulated:

- NR1: Hard-limiting ( $\approx$  standard topology, see Fig. 4.11)
- NR2: Asymmetric ( $\approx$  Colpitts topology, see Fig. 4.13(a))
- NR3: Soft-limiting<sup>12</sup> ( $\approx$  linear, or ALC-assisted)

In each case, the associated noise current,  $i_{nr}$ , had a PSD equal to  $-4kT\alpha G_m(t)$ , with  $\alpha = 2/3$ . The predicted and simulated output noise (in dBm/Hz) due to AM and PM for the three oscillators are plotted in Figs. 4.10(b)-4.10(d). We see that:

- All nonlinearities lead to the same output noise (in dBm/Hz) due to phase fluctuations.
- The output noise (in dBm/Hz) due to amplitude fluctuation varies considerably depending on the nonlinearity.
- The oscillator employing the linear negative resistance (NR3) exhibits the largest  $\widehat{v_{n_{AM}}^2}$  component. Since NR3 possesses a very weak nonlinearity, it struggles to suppress amplitude disturbances;  $G_M[0] \approx -1/R_p$  and  $G_M[2] \approx 0$ .
- The oscillator employing NR1 has a very small  $\widehat{v_{n_{AM}}^2}$  component. In this case,  $G_M[0] \approx -G_M[2]$ , the nonlinearity contributes no AM noise current, and the AM noise current due to the resistor flows into the lossy resonator only.

The choice of nonlinearity (e.g. hard-limiting or soft-limiting) has no effect on output noise resulting from phase fluctuations. However, it does make a difference to output noise arising from amplitude fluctuations, oscillation amplitude for a given current, and potentially other attributes such as frequency stability and harmonic content [50].

---

<sup>12</sup>The characteristic is a piecewise approximation of a linear resistance. Convergence issues set the limit as to how much the characteristic deviates from a straight line.

All these observations relate to absolute noise (dBm/Hz) but not relative phase noise normalized to the oscillation amplitude (dBc/Hz); oscillation amplitude depends on the I-V characteristic, and will affect the phase noise measurement when quoted in dBc/Hz<sup>13</sup>.

## 4.6 Applying the General Result to Popular Oscillators

The noise factors derived in this section are already known. Rael [50] derived the noise factor for the current-biased NMOS standard topology under hard-switching conditions. Later, Andreani et al., using the ISF, derived the same noise factor but under more general conditions [51], as well as the noise factors for the Colpitts topology [51] and current-biased CMOS standard topology [52]. Our intent is simply to show how the general result, and specifically our interpretation of it, can be applied to these oscillators.

### 4.6.1 Noise Factor

#### 4.6.1.1 The Standard Current-Biased NMOS Topology

The standard NMOS *LC* topology is shown in Fig. 4.11(a). The energy-restoring non-linearity is composed of a cross-coupled differential NMOS pair, displayed separately in Fig. 4.11(b). If we assume an ideal noiseless current source and square law models, and also assume  $V_{nr}$  is small enough that both transistors remain in saturation, we can write:

$$\begin{aligned} I_L &= \frac{1}{2} \mu_n \frac{W_L}{L_L} C_{ox} (V_{GS_L} - V_{t_L})^2 \\ I_R &= \frac{1}{2} \mu_n \frac{W_R}{L_R} C_{ox} (V_{GS_R} - V_{t_R})^2, \end{aligned} \tag{4.43}$$

---

<sup>13</sup>It can be shown that, for a given power budget, the largest oscillation amplitude will be attained if the restoring current is injected as an impulse at the peak (or trough) of an oscillation [65]. Mazzanti and Andreani [66] made use of this fact to develop a topology, which, from a theoretical viewpoint at least, promises better phase noise performance, for a given current, than any other NMOS-only topology currently conceived. The improved phase noise performance of the topologies proposed by Shekhar et al. [67], and Soltanian and Kinget [68] can also be attributed to this fact.

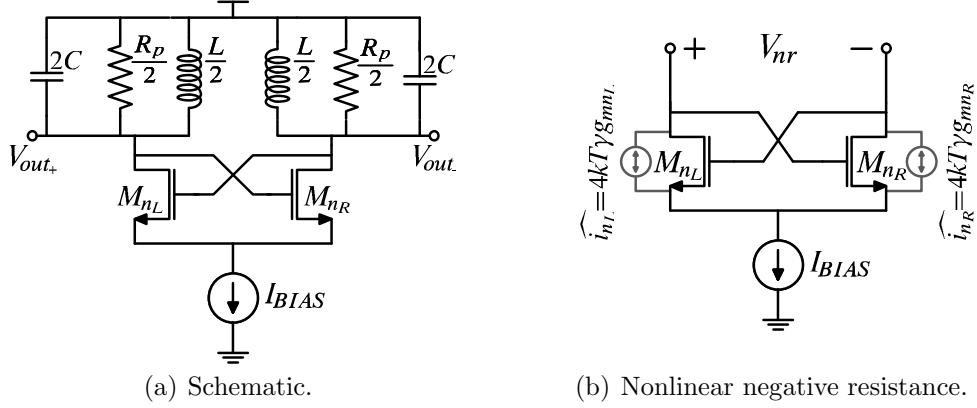


Figure 4.11: The standard current-biased NMOS  $LC$  oscillator.

where  $V_{GS_L} = V_{DD} - V_{nr}/2 - V_{CM}$ ,  $V_{GS_R} = V_{DD} + V_{nr}/2 - V_{CM}$ ,  $I_{BIAS} = I_L + I_R$ ,  $I_{NR} = (I_L - I_R)/2$  and  $V_{CM}$  is the source voltage of each transistor. Using

$$g_{mn_R} = \frac{\partial I_L}{\partial V_{GS_L}}, \quad g_{mn_L} = \frac{\partial I_R}{\partial V_{GS_R}}, \quad G_m = \frac{\partial I_{NR}}{\partial V_{nr}}, \quad (4.44)$$

and solving for  $G_m$  in terms of  $g_{mn_R}$  and  $g_{mn_L}$  results in

$$G_m(t) = -\frac{g_{mn_R}(t)g_{mn_L}(t)}{g_{mn_R}(t) + g_{mn_L}(t)}, \quad (4.45)$$

where  $g_{mn_R}(t)$  and  $g_{mn_L}(t)$  are the instantaneous transconductance of the transistors  $M_{nR}$  and  $M_{nL}$  respectively. If the  $V_{nr}$  is large enough that the pair is fully-switched, the transconductance of each transistor (and the conductance of differential pair) drops to zero and Eqn. (4.45) remains valid. Furthermore, since the pair will be fully-switched before at least one transistor drops into triode, Eqn. (4.45) is valid for all regions of operation. When both transistor are saturated, we can associated the noise currents  $\widehat{i_{n_L}^2} = 4kT\gamma g_{mn_L}$  and  $\widehat{i_{n_R}^2} = 4kT\gamma g_{mn_R}$  to the appropriate transistors. The resulting PSD of differential noise current is

$$\begin{aligned} \widehat{i_{nr}^2} &= \frac{1}{2} \left( \widehat{i_{n_R}^2} \frac{g_{mn_L}}{g_{mn_L} + g_{mn_R}} + \widehat{i_{n_L}^2} \frac{g_{mn_R}}{g_{mn_L} + g_{mn_R}} \right) \\ &= 4kT\gamma \frac{g_{mn_L}g_{mn_R}}{g_{mn_L} + g_{mn_R}}, \end{aligned} \quad (4.46)$$

where  $\gamma$  is the channel noise coefficient of an NMOS transistor. When fully-switched, the pair contributes no noise and so the above equation remains valid in all regions, and can



be written as a time varying power spectral density equal to

$$\widehat{i_{nr}^2} = -4kT\gamma G_m(t) \quad (4.47)$$

As per Eqn. (4.33), the noise associated with the differential pair is proportional to its conductance, which is memoryless and always negative. Therefore, the general result applies, and by mere inspection we see that the noise intensity constant,  $\alpha$ , in Eqn. (4.39) is equal to  $\gamma$ . Thus, the output power spectral density of the oscillator is equal to

$$\widehat{v_n^2} = 2kTR_p(1 + \gamma) \left( \frac{\omega_0}{2Q\omega_m} \right)^2. \quad (4.48)$$

Comparing this expression with Eqn. (4.2), the minimum possible noise factor of this topology evaluates to

$$\boxed{F_{\text{NMOS}_{\text{MIN}}} = 1 + \gamma.} \quad (4.49)$$

What is remarkable about the above derivation is how little we know about the differential pair. We have said nothing about the size of the transistors, technology or biasing. In fact, we haven't even remarked about matching between the two transistors; the general result suggests that a badly matched pair will have exactly the same output noise as a perfectly matched differential pair<sup>14</sup>! The amplitude of oscillation is also irrelevant, as the noise factor remains constant whether the differential pair is hard-switched or not (as stated but not shown in [51].)

#### 4.6.1.2 The Standard Current-Biased CMOS Topology

A full CMOS implementation of the standard current-biased topology is shown in Fig. 4.12(a). The addition of cross-coupled PMOS transistors facilitates the commutation of the bias current across the entire tank (not just half); this doubles the oscillation amplitude for a given current and results in increased oscillator efficiency. Assuming a nearly-sinusoidal oscillation, the negative resistance shown in Fig. 4.12(b), will have a time-varying conductance of

$$G_m(t) = -\frac{g_{mn_R}(t)g_{mn_L}(t)}{g_{mn_R}(t) + g_{mn_L}(t)} - \frac{g_{mp_R}(t)g_{mp_L}(t)}{g_{mp_R}(t) + g_{mp_L}(t)}, \quad (4.50)$$

---

<sup>14</sup>We have verified this in simulation.

where  $g_{mn_R}$ ,  $g_{mn_L}$ ,  $g_{mp_R}$  and  $g_{mp_L}$  are the transconductances of  $M_{n_R}$ ,  $M_{n_L}$ ,  $M_{p_R}$  and  $M_{p_L}$  respectively. It can be shown that this topology injects a noise current,  $i_{nr}$ , into the tank whose PSD is

$$\widehat{i_{nr}^2} = 4kT \left( \gamma_n \frac{g_{mn_R}(t)g_{mn_L}(t)}{g_{mn_R}(t) + g_{mn_L}(t)} + \gamma_p \frac{g_{mp_R}(t)g_{mp_L}(t)}{g_{mp_R}(t) + g_{mp_L}(t)} \right). \quad (4.51)$$

Assuming  $\gamma \approx \gamma_n \approx \gamma_p$ ,

$$\widehat{i_{nr}^2} = -4kT\gamma G_m(t). \quad (4.52)$$

Again, by inspection we see that the noise intensity constant  $\alpha$  is equal to  $\gamma$ . Thus, from our analysis above the oscillator's output PSD is given by

$$\widehat{v_n^2} = 2kTR_p(1 + \gamma) \left( \frac{\omega_0}{2Q\omega_m} \right)^2, \quad (4.53)$$

with the minimum noise factor again evaluating to

$$\boxed{F_{\text{CMOS}_{\text{MIN}}} = 1 + \gamma.} \quad (4.54)$$

This is identical to the noise factor of the NMOS only topology<sup>15</sup>; the PMOS transistors double the oscillation amplitude without introducing extra noise into the system. This result was derived previously under the assumption of hard-switching [52].

However, and this is of practical importance, it was noted in [52] that this noise factor can only be obtained if the tank capacitance appears only *between the output terminals*. Capacitance, parasitic or otherwise, from the output terminals to ground offers a path for high frequency noise in the PMOS devices and this can degrade the phase noise factor significantly.

### 4.6.1.3 The Colpitts Topology

The Colpitts oscillator, shown in Fig. 4.13(a), can be analyzed in a similar fashion. To facilitate such analysis it is first necessary to redraw the circuit in the form of a negative-gm oscillator. It is assumed that, at the oscillation frequency and above, the transistor

---

<sup>15</sup>If  $\gamma_n \neq \gamma_p$ , the general result does not apply; the calculation of  $F$  is significantly complicated, and becomes a function of amplitude and transistor sizing. As shown in [52], however, if the circuit is hard-switched,  $F \approx 1 + (\gamma_n + \gamma_p)/2$  is a good approximation when  $\gamma_n \neq \gamma_p$ .

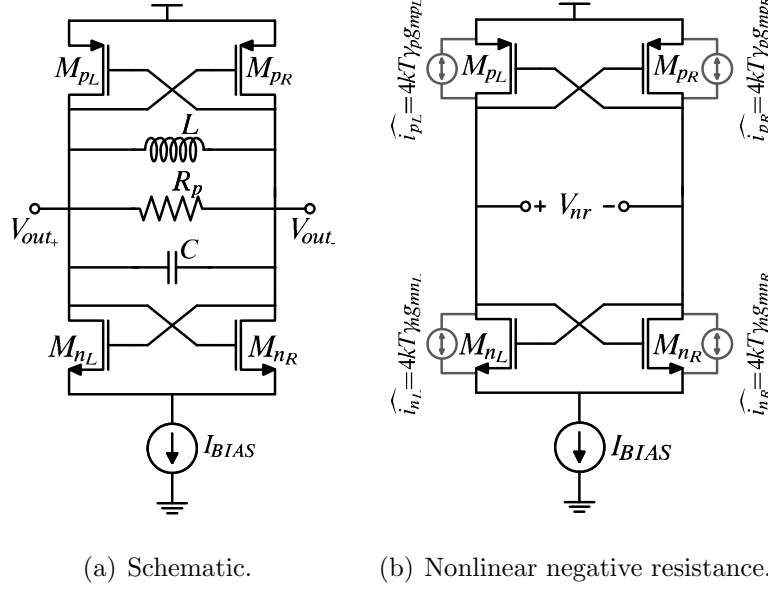


Figure 4.12: The standard current-biased CMOS  $LC$  oscillator.

is not loaded by the capacitors, i.e., at  $\omega_0$  the capacitors act as a perfect voltage divider,  $g_m \ll \omega_0(C_1 + C_2)$  and  $V_x \approx V_{out}(C_1/(C_1 + C_2))$ . Under this assumption, redrawing the circuit becomes a straightforward task, as shown in Fig. 4.13. Again, we assume the current source is ideal and noiseless. The conductance of the nonlinearity in the redrawn circuit is

$$G_{nr}(t) = -\frac{C_1 C_2}{(C_1 + C_2)^2} g_m(t). \quad (4.55)$$

Assuming the transistor is either off or operates in the saturation region, the noise current  $i_n$  between its drain and source has a time-varying PSD given by  $4kT\gamma g_m(t)$ . This noise current may be transformed in an identical manner into a differential current across the resonator, and results in a noise current  $i_{nr}$  with a power spectral density of

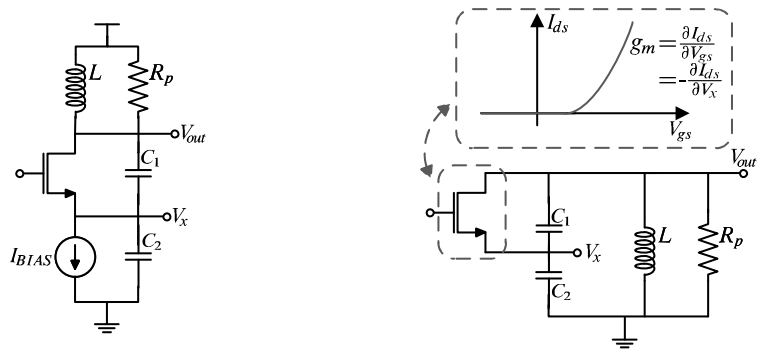
$$\widehat{i_{nr}^2} = 4kT\gamma \left( \frac{C_2}{C_1 + C_2} \right)^2 g_m(t) = -4kT\gamma \left( \frac{C_2}{C_1} \right) G_{nr}(t). \quad (4.56)$$

Since the circuit is now in the form of a generalized negative-gm oscillator, we know, by inspection, that  $\alpha = \gamma \left( \frac{C_2}{C_1} \right)$  and thus

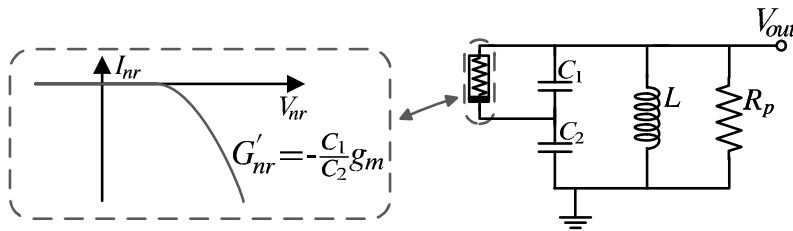
$$\widehat{v_n^2} = 2kT R_p \left( 1 + \gamma \frac{C_2}{C_1} \right) \left( \frac{\omega_0}{2Q\omega_m} \right)^2 \quad (4.57)$$

and

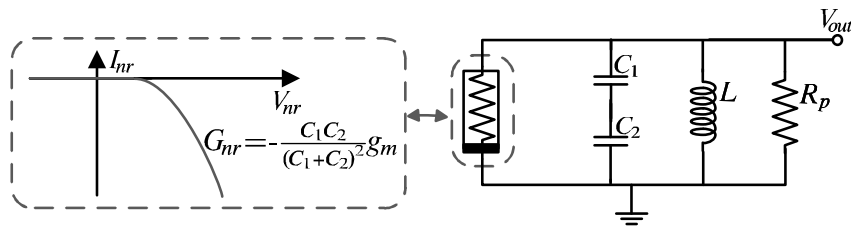
$$\boxed{F_{\text{Colpitts}_{\text{MIN}}} = 1 + \frac{C_2}{C_1} \gamma} \quad (4.58)$$



(a) Schematic. (b) Simplified schematic - biasing information ignored.



(c) Simplified schematic - conducting transistor modeled as a nonlinear negative resistor.



(d) Simplified schematic - negative-gm equivalent.

Figure 4.13: The Colpitts oscillator.

Again, it is remarkable that we are able to predict phase noise with almost no information about the specifics of the transistor and its biasing. Does  $I_{ds}$  relate to  $V_x$  by means of a linear, cubic or higher order polynomial? For what value of  $V_x$  does the transistor switch on? To the first order, it doesn't matter. Most notably, the above calculations demonstrate that output noise is independent of the conduction angle. The original derivation [51] is accompanied with a useful discussion on why this topology is inferior to the standard  $LC$ .

#### 4.6.2 Extrinsic Noise

So far we have not addressed noise associated with the bias currents. Again, the effects of these sources are well-known, and are easily accounted for using our technique. Consider first the current-biased NMOS topology with a MOS current source: if the differential pair is hard-switched the current source noise,  $\widehat{i_{cs}^2} = 4kT\gamma g_{m_{cs}}$ , will be modulated by a square wave of amplitude  $\pm\frac{1}{2}$ , and injected across the tank. Therefore  $p(t)$  will be a constant of value  $\frac{1}{4}$  and  $P[k]$  will evaluate to  $\delta[k]/4$ . This gives

$$\begin{aligned}\widehat{i_{cs_{PM}}^2} &= \left(\frac{1}{2}P[0] - \frac{1}{4}P[2] - \frac{1}{4}P[-2]\right)\widehat{i_{cs}^2} = \frac{\widehat{i_{cs}^2}}{8} = \frac{kT\gamma g_{m_{cs}}}{2} \\ \widehat{i_{cs_{AM}}^2} &= \left(\frac{1}{2}P[0] + \frac{1}{4}P[2] + \frac{1}{4}P[-2]\right)\widehat{i_{cs}^2} = \frac{\widehat{i_{cs}^2}}{8} = \frac{kT\gamma g_{m_{cs}}}{2},\end{aligned}\tag{4.59}$$

resulting in a noise factor (including all intrinsic sources) of

$$\boxed{F_{\text{NMOS}} = 1 + \gamma + \frac{\gamma g_{m_{cs}} R_p}{4}}.\tag{4.60}$$

Similarly, the noise factor of the CMOS topology becomes

$$\boxed{F_{\text{CMOS}} = 1 + \gamma + \gamma g_{m_{cs}} R_p}.\tag{4.61}$$

The noise associated with the biasing current source in the Colpitts topology is not modulated, and can be simply referred across the tank (using a Norton Equivalent transformation) as a stationary noise source. Including this source the noise factor becomes

$$\boxed{F_{\text{Colpitts}} = 1 + \frac{C_2}{C_1}\gamma + \gamma g_{m_{cs}} R_p \left(\frac{C_1}{C_1 + C_2}\right)^2}.\tag{4.62}$$

### 4.6.3 Oscillation Amplitude

Phase noise is always quoted in dBc/Hz, which is simply the single-sideband output PSD normalized to the carrier power (see Eqn. (4.2)). Expressions for the amplitudes of the oscillator topologies discussed in this work are well-known, but in the interest of completeness they are restated here. Under hard-switching the amplitude of the NMOS/CMOS standard topologies are

$$\begin{aligned} A_{\text{NMOS}} &= \frac{2}{\pi} I_{\text{BIAS}} R_p \\ A_{\text{CMOS}} &= \frac{4}{\pi} I_{\text{BIAS}} R_p, \end{aligned} \quad (4.63)$$

while the amplitude of the Colpitts oscillator [69] (as the conduction angle,  $\theta$ , tends to zero) is

$$A_{\text{Colpitts}} = 2I_{\text{BIAS}} R_p \frac{C_2}{C_1 + C_2}. \quad (4.64)$$

## 4.7 $Q$ Degradation Analysis

There has always been much concern in oscillator design on how the active elements in the circuit may add to the resonator loss, particularly at the extremes of large oscillation waveforms which may push transistors into their triode regions. The term “loaded  $Q$ ” refers to these hard to quantify effects which may degrade, sometimes substantially, the inherent resonator  $Q$ . Here the general result cannot be used because it requires the conductance of the active nonlinearity to be always negative and/or the associated noise to be proportional to its instantaneous conductance. Our analysis, however, can be extended to deal very neatly with many interesting cases that do not fulfill these criteria. In this work, we investigate the standard voltage-biased NMOS  $LC$  oscillator and also the standard current-biased CMOS oscillator when subjected to tank loading [52]. “Loaded  $Q$ ” acquires a quantitative meaning.

### 4.7.1 An Arbitrary Nonlinearity that Contributes Loss

Let's consider the negative-gm model when the conductance is not always negative. We redraw the circuit, as shown in Fig. 4.14, where the nonlinearity is decomposed into two nonlinear resistances: one that is always *positive*,  $G_p(t)$ , and one that is always *negative*,  $G_n(t)$ . Further, we assume that we can associate a noise current with each of these resistors that has a PSD proportional to its instantaneous conductance<sup>16</sup>: the noise intensity constants assigned to  $G_n(t)$  and  $G_p(t)$  are  $\alpha$  and  $\beta$  respectively. Calculating the PM con-

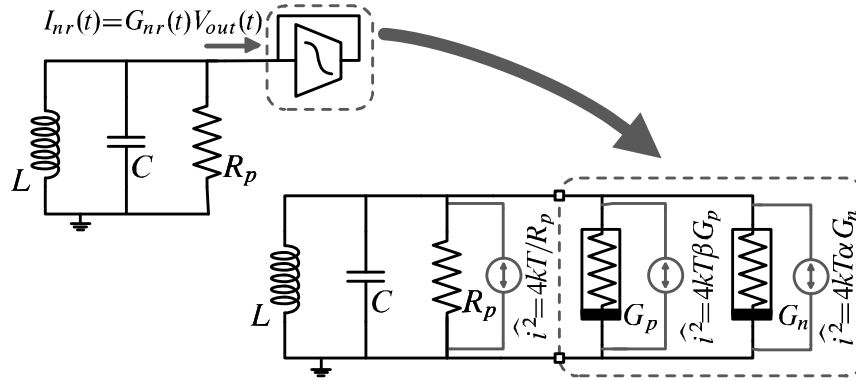


Figure 4.14: A generic negative-gm  $LC$  oscillator model.

tribution of each noise current source using Eqn. (4.29) and multiplying by Eqn. (4.19), the output noise of the oscillator is calculated as

$$\begin{aligned} \widehat{v}_n^2 &= \left( \widehat{i_{resPM}^2} + \widehat{i_{GnPM}^2} + \widehat{i_{GpPM}^2} \right) |Z_{PM}\{\omega_0 \pm \omega_m\}|^2 \\ &= 2kTR_p (1 - \alpha G_{N_{\text{eff}}} R_p + \beta G_{P_{\text{eff}}} R_p) \left( \frac{\omega_0}{2Q\omega_m} \right)^2, \end{aligned} \quad (4.65)$$

where  $G_{N_{\text{eff}}} = G_N[0] - G_N[2]$  and  $G_{P_{\text{eff}}} = G_P[0] - G_P[2]$ . We can simplify further, by noting in Fig. 4.14 that the energy conservation requirement is now

$$G_{N_{\text{eff}}} = - \left( G_{P_{\text{eff}}} + \frac{1}{R_p} \right), \quad (4.66)$$

<sup>16</sup>Of course, since the nonlinearity is memoryless, it can be decomposed into an arbitrary number of real-valued nonlinear resistances. However, as will be shown shortly, decomposing the nonlinearity into a positive and a negative resistance (with the associated proportional noise sources) has some physical significance.

and so, depending on whether it is easier to calculate  $G_{N_{\text{eff}}}$  or  $G_{P_{\text{eff}}}$ , we may write the noise factor as

$$\begin{aligned}
 F &= 1 - \alpha G_{N_{\text{eff}}} R_p + \beta G_{P_{\text{eff}}} R_p \\
 &= (1 + \alpha) + (\alpha + \beta) G_{P_{\text{eff}}} R_p \\
 &= (1 - \beta) - (\alpha + \beta) G_{N_{\text{eff}}} R_p.
 \end{aligned} \tag{4.67}$$

We now have method for investigating topologies in which the nonlinearity contributes loss to the system for some portion of the oscillation period.

### 4.7.2 The Standard Voltage-Biased NMOS Topology

Let's apply the preceding theory to the standard voltage-biased oscillator topology shown in Fig. 4.15(a) that was used in early CMOS  $LC$  oscillators [70] for its large output amplitude. In this circuit, the transistors conduct in all three regimes: triode, saturation, off. We employ a number of simplifications to make the problem tractable. We assume the transistors adhere to the square law model, and exhibit no second-order effects such as velocity saturation. Further we assume the PSD of channel noise,  $i_d$ , across all three regions is<sup>17</sup>

$$\widehat{i_d^2} = 4kT (\gamma g_m + g_{ds}). \tag{4.68}$$

#### 4.7.2.1 Noise Factor

The nonlinearity in this topology arises simply from the cross-coupled differential pair. The I-V characteristic and conductance of this differential pair are plotted in Fig. 4.16(a). It is straightforward to show that the instantaneous conductance of the nonlinearity is given by

$$\begin{aligned}
 G_{nr}(t) &= \frac{1}{4} (-g_{mn_R}(t) - g_{mn_L}(t) + g_{dsn_R}(t) + g_{dsn_L}(t)) \\
 &= G_m(t) + G_{ds}(t),
 \end{aligned} \tag{4.69}$$

---

<sup>17</sup>This is a good approximation of the default SPICE2 noise model used in the BSIM3 model. As we have done throughout this work, we omit the contribution of  $g_{mbs}$ , and assume it can be accounted for in the value of  $\gamma$ . The more sophisticated charge based model available in BSIM3 (which is the default in the BSIM4), while more accurate, is not suitable for hand calculations.



where  $G_m = -(1/4)(g_{mn_R}(t) + g_{mn_L}(t))$  and  $G_{ds}(t) = (1/4)(g_{dsn_R}(t) + g_{dsn_L}(t))$ . The associated noise current is given by

$$\widehat{i_{nr}^2}(t) = 4kT\gamma G_m(t) + 4kTG_{ds}(t), \quad (4.70)$$

Since the conductance of the nonlinearity is not always negative, and since its associated noise (see Eqn. (4.70)) is no longer proportional to the conductance (see Eqn. (4.69)), the general result cannot be applied. However, the nonlinearity can be decomposed into a *positive* nonlinear resistive component,  $G_{ds}$ , and a *negative* nonlinear component,  $G_m$ , which possess the characteristics shown in Fig. 4.16(b). This allows us to redraw the circuit in the form of the simplified negative-gm model shown in Fig. 4.15(b), which is in the same general form as Fig. 4.14.

Intuitively, it is now possible to see why the voltage-biased oscillator is a noisy oscillator: the nonlinear positive resistance contributes loss and noise to the system; additionally the effective conductance of the system needs to be larger to overcome these losses, and therefore the noise due to  $G_m$  also increases.

Referring to Eqn. (4.67) & Eqn. (4.68), we note that  $\alpha = \gamma$  and  $\beta = 1$ . Thus the output noise is

$$\widehat{v_n^2} = 2kTR_p(1 + \gamma)(1 + G_{DS_{\text{eff}}}R_p) \left( \frac{\omega_0}{2Q\omega_m} \right)^2, \quad (4.71)$$

where  $G_{DS_{\text{eff}}}$  takes the place of  $G_{P_{\text{eff}}}$  in (4.67). The noise factor is given by

$$\boxed{F_{\text{VB}} = (1 + \gamma)(1 + G_{DS_{\text{eff}}}R_p)}, \quad (4.72)$$

We must now calculate  $G_{DS_{\text{eff}}}$ . Assuming square-law transistors,

$$G_{ds}(t) = \begin{cases} (K/4)(V_{out}(t) - V_t), & V_{out}(t) \leq V_t \\ (K/4)(-V_{out}(t) - V_t), & V_{out}(t) \leq -V_t \\ 0, & \text{otherwise,} \end{cases} \quad (4.73)$$

where  $K = 0.5\mu_n C_{ox}W/L$  and  $V_{out}(t) = A_c \cos(\omega_0 t)$ . The effective positive conductance

contributed by the differential pair is, therefore, calculated as

$$G_{DS_{\text{eff}}} = G_{DS}[0] - G_{DS}[2] = \text{Re} \left\{ \frac{K}{6A_c\pi} \left( (2A_c^2 + V_t^2) \sqrt{1 - \frac{V_t^2}{A_c^2}} - 3A_cV_t \cos^{-1} \left( \frac{V_t}{A_c} \right) \right) \right\}. \quad (4.74)$$

Fig. 4.17 compares the noise factor versus oscillation amplitude for a typical voltage-biased oscillator (using Eqn. (4.72) and Eqn. (4.74)) and the current-biased oscillator. The voltage noise factor of the current-biased oscillator remains constant with oscillation amplitude, while the noise factor of the voltage-biased topology rises dramatically.

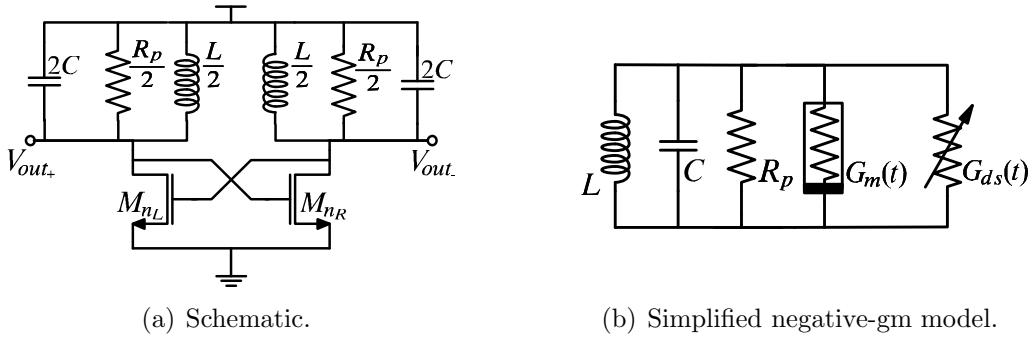


Figure 4.15: The voltage-biased standard NMOS  $LC$  oscillator.

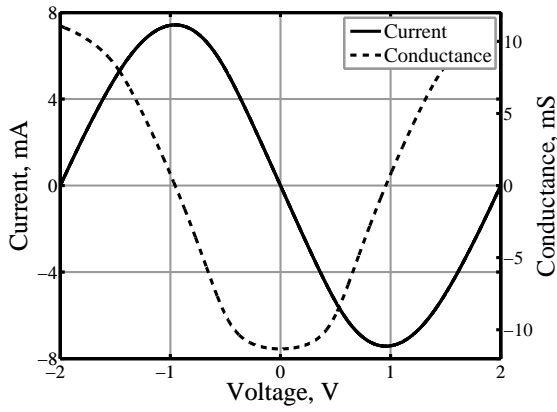
#### 4.7.2.2 Oscillation Amplitude

Unlike the other oscillator topologies addressed in this work, the noise factor of the voltage-biased topology depends on the oscillation amplitude; in order to calculate  $F$ , one must first calculate  $G_{DS_{\text{eff}}}$ , which depends on  $A_c$ . A simple method to predict the oscillation amplitude of the voltage-biased topology, adapted from [71], is now presented.

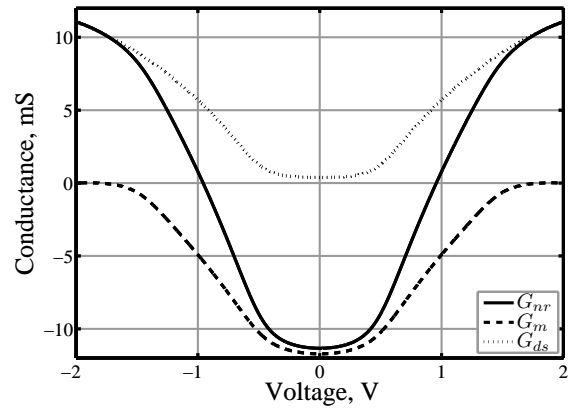
In general, the amplitude of any  $LC$  oscillator is of the form

$$A_c = -I_{NR}[1]R_p, \quad (4.75)$$

where  $I_{NR}[1]$  is the first harmonic of the current drawn by the nonlinearity. How accurately we can predict the oscillation amplitude depends on how accurately we can quantify the



(a) Current and conductance characteristics.



(b) Conductance characteristic decomposed as positive and negative nonlinear resistances, i.e.,  $G_{nr} = G_m + G_{ds}$ .

Figure 4.16: The standard voltage-biased NMOS  $LC$  oscillator: typical plots.

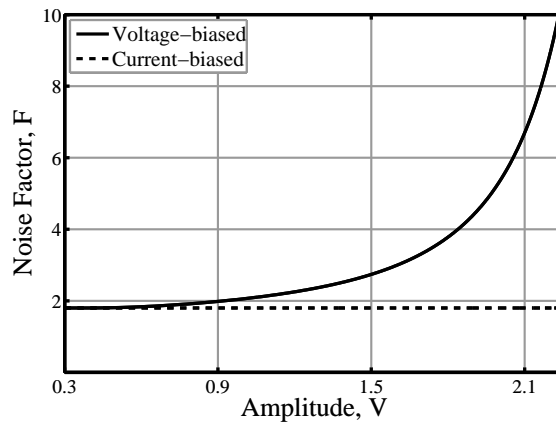


Figure 4.17: Predicted noise factors of the voltage-biased oscillator and the current-biased oscillator.

I-V characteristic of the nonlinearity, and thus  $I_{NR}[1]$ . In the case of the voltage-biased topology, the I-V characteristic is accurately represented using the fifth order polynomial<sup>18</sup>

$$I_{nr} = g_0 V_{nr} - \frac{3g_0}{8V_{dd}^2} V_{nr}^3 + \frac{g_0}{32V_{dd}^4} V_{nr}^5, \text{ if } g_0 = \left. \frac{\partial I_{nr}}{\partial V_{nr}} \right|_{V_{nr}=0}, \quad (4.76)$$

with  $g_0$  always being negative. For near sinusoidal oscillation,  $V_{nr} = A_c \cos(\phi)$ ,

$$\begin{aligned} I_{NR}[1] &= \frac{1}{\pi} \int_{-\pi}^{\pi} I_{nr}(\phi) \cos(\phi) d\phi \\ &= g_0 A_c - \frac{9g_0}{32V_{dd}^2} A_c^3 + \frac{5g_0}{256V_{dd}^4} A_c^5. \end{aligned} \quad (4.77)$$

Substituting this value into Eqn. (4.75) and solving for  $A_c$  gives

$$A_c = 2V_{dd} \sqrt{\frac{9}{5} - \frac{1}{5} \sqrt{1 - \frac{80}{g_0 R_p}}}. \quad (4.78)$$

Simulation results suggest that this expression is a good approximation for both square law and short channel transistor models.

#### 4.7.2.3 Effective, or Loaded, $Q$

The literature sometimes accounts for a higher than expected noise in an oscillator by pointing to an empirically fitted “effective”  $Q$  and  $R_p$  parameters, denoted as  $Q_{\text{eff}}$  and  $R_{p_{\text{eff}}}$  respectively. Given the above derivation we are able to quantify these parameters. If we rewrite Eqn. (4.71), in the form of the ideal current-biased oscillator Eqn. (4.48):

$$\widehat{v}_n^2 = 2kTR_{p_{\text{eff}}} (1 + \gamma) \left( \frac{\omega_0}{2Q_{\text{eff}}\omega_m} \right)^2, \quad (4.79)$$

then we must define  $Q_{\text{eff}}$  and  $R_{p_{\text{eff}}}$  as:

$$\begin{aligned} Q_{\text{eff}} &= \frac{Q}{1 + G_{DS_{\text{eff}}} R_p} \\ R_{p_{\text{eff}}} &= \frac{R_p}{1 + G_{DS_{\text{eff}}} R_p} = R_p \parallel \frac{1}{G_{DS_{\text{eff}}}}. \end{aligned} \quad (4.80)$$

---

<sup>18</sup>The coefficients of the polynomial are found by noting that the slope of the characteristic at  $-2V_{dd}$ , 0 and  $2V_{dd}$  is, respectively,  $-g_0$ ,  $g_0$  and  $-g_0$ .

#### 4.7.2.4 SpectreRF Simulations

The phase noise performance of the voltage-biased NMOS topology predicted by analysis was verified in SpectreRF. The oscillator was simulated using 90nm CMOS models and a 1V supply. An ideal linear tank with a  $Q$  of 13 and resonant frequency of 500MHz ( $L=10\text{nH}$ ,  $C=10.1\text{pF}$ ,  $R_p=400\Omega$ ) was used, while the dimensions of each finger comprising the FETs in the differential pair fingers were  $W=3\mu\text{m}$ ,  $L=0.5\mu\text{m}$ . The amplitude was controlled by varying the number of transistor fingers from 4 to 25. Noise measurements were taken at a 100kHz offset. Two simulations were run: one used the unaltered BSIM3v3 model card, which utilized the charge-based noise model; in a second simulation, we toggled the NOIMOD parameter of the model card to switch to the SPICE2 noise model, and increased the VSAT parameter to infinity to eliminate velocity saturation effects. Figs. 4.18(a) and 4.18(b) plot the simulated and predicted output PSD and phase noise of the oscillator versus amplitude. Both sets of simulation results are in good agreement with the model. As a reference, the predicted noise performance of an equivalent current-biased oscillator is also plotted. The oscillation amplitude used in theoretical predictions was obtained using Eqn. (4.78). Notice that there is a phase noise optimum, after which, any improvement in phase noise due to a larger carrier,  $A_c$ , is negated by an increase in the noise factor,  $F$ .

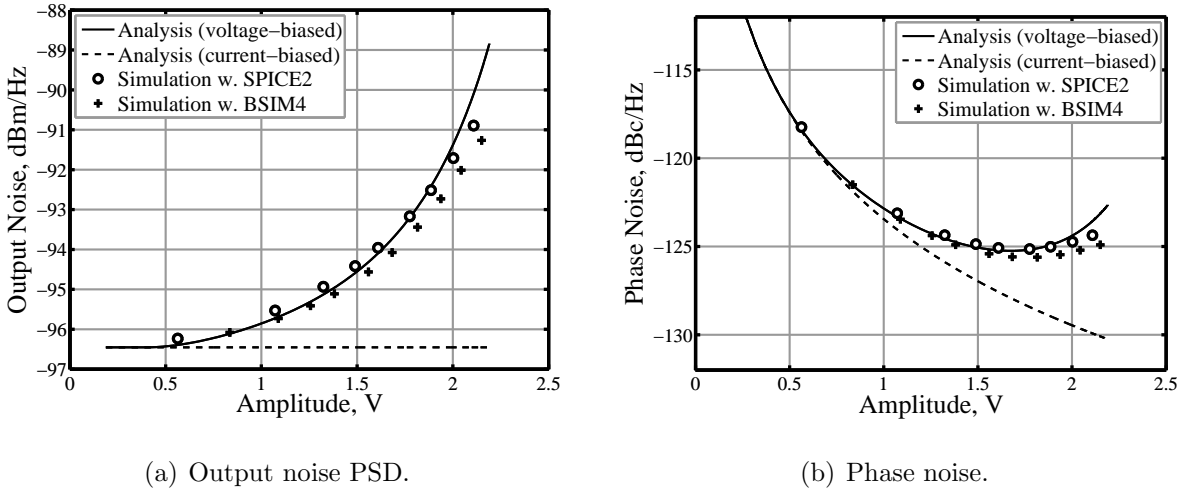


Figure 4.18: The standard voltage-biased NMOS  $LC$  oscillator: simulation results.

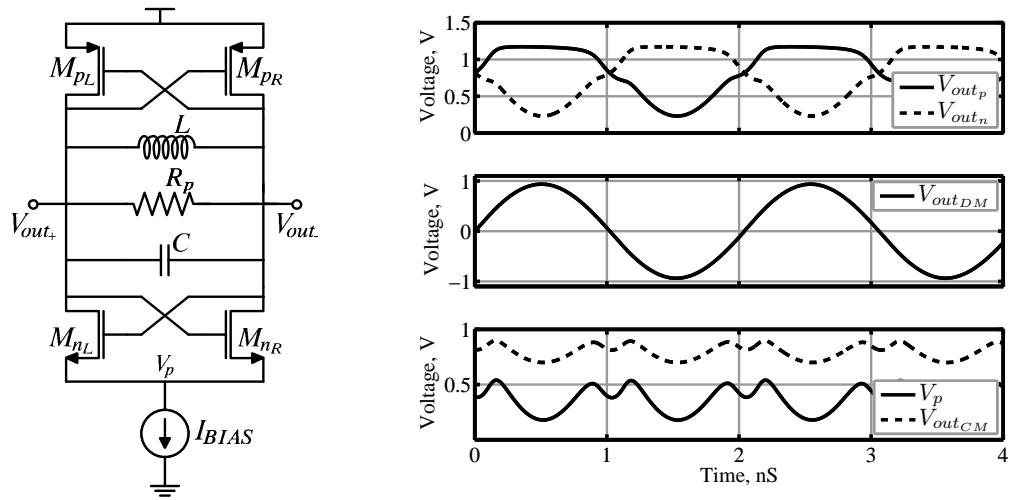
### 4.7.3 The Standard Current-Biased CMOS Topology

We now quantify, for the first time, a tank loading mechanism that can occur in all current-biased CMOS RF oscillators [52]. We demonstrate how the complementary FETs load the  $LC$  tank to the detriment of the noise factor *and* oscillation amplitude.

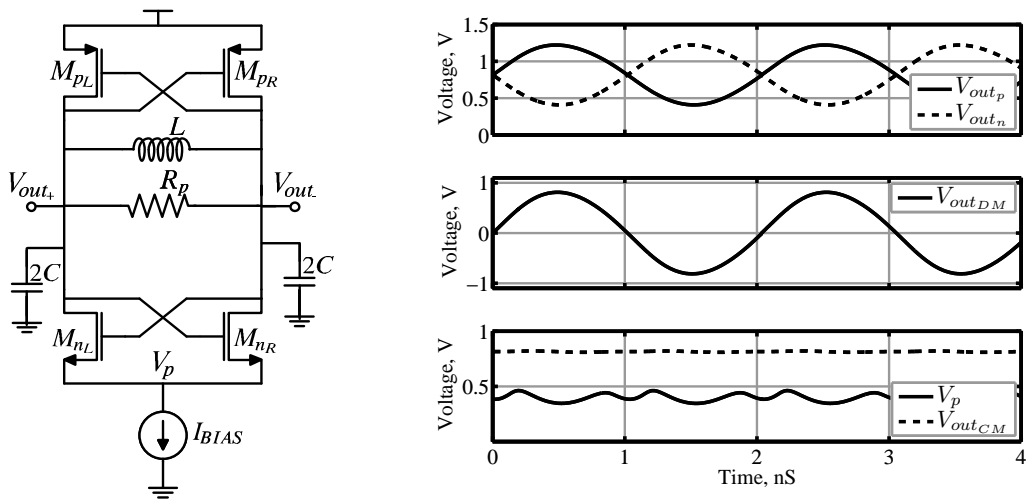
#### 4.7.3.1 Noise Factor

Consider the current-biased CMOS topology as it is generally represented in Fig. 4.19(a). In the presence of a large oscillation the PMOS pair will be hard switched; for a small time around the zero-crossing both PMOS transistors will be saturated, while elsewhere one transistor will be off and the other transistor will be driven into deep triode. In this situation, current through the PMOS transistor in triode has no path to ground other than through the corresponding hard-switched NMOS transistor (via the tank). This induces a common mode oscillation on the output, which ensures that the current through both the PMOS and NMOS transistors is exactly equal to  $I_{BIAS}$  (see Fig. 4.19(a)). Additionally, since the current through the PMOS transistor is set by  $I_{BIAS}$ , the transistor contributes no noise while in this regime. In this case, the conductance of the nonlinearity is given by Eqn. (4.50), the noise factor is given by  $F = 1 + \gamma$  and the oscillation amplitude is given by  $A_c = (4/\pi)I_{BIAS}R_p$ .

However, if the tank capacitance does not appear across the tank, but rather as two single-ended capacitors connected to ground (Fig. 4.19(b)), the oscillator will behave very differently [52]. This is, in fact, generally the situation at RF, when the resonator is made up of an on-chip spiral inductor tuned by the capacitances to ground at the drain junctions and at the PMOS gates, with only the NMOS gates offering a small portion of the total capacitance that floats in parallel with the inductor. If the single-ended capacitors are sufficiently large, they can suppress the common mode oscillation, as shown in Fig. 4.19(b), and the current through a hard-switched PMOS transistor will have two paths to ground: through the corresponding hard-switched NMOS transistor and through the capacitors. In this instance, the oscillator is more appropriately viewed as a *voltage-biased PMOS*



(a) Fully differential capacitor arrangement.



(b) Single-ended capacitor arrangement.

Figure 4.19: The standard current-biased CMOS  $LC$  oscillator.

pair (as in Fig. 4.15(a)), in parallel with the hard-limiting nonlinearity provided by the *current-biased NMOS* pair. Now the time-varying conductance is given by

$$\begin{aligned}
G_{nr}(t) &= - \left[ \frac{g_{mn_R}(t)g_{mn_L}(t)}{g_{mn_R}(t) + g_{mn_L}(t)} \right] - \left[ \frac{1}{4} (g_{mp_R}(t) + g_{mp_L}(t)) \right] \\
&\quad + \left[ \frac{1}{4} (g_{dsp_R}(t) + g_{dsp_L}(t)) \right] \\
&= G_{m_n}(t) + G_{m_p}(t) + G_{ds_p}(t).
\end{aligned} \tag{4.81}$$

Here we have three nonlinear conductances: a *negative* conductance,  $G_{m_n}(t)$ , due to the current-biased NMOS differential pair, a *negative* conductance,  $G_{m_p}(t)$ , due to the transconductance of the PMOS transistors, and a *positive* conductance,  $G_{ds_p}(t)$ , due to the drain-source conductance of the PMOS transistors. If we lump together  $G_{m_n}(t)$  and  $G_{m_p}(t)$  as a single negative nonlinear resistor, the noise factor of the oscillator can be obtained in the same way as the noise factor of the voltage-biased topology (see in Sec. 4.7.2). Working through the calculations the output PSD is found to be

$$\widehat{v}_n^2 = 2kTR_p(1 + \gamma)(1 + G_{DSEFF}R_p) \left( \frac{\omega_0}{2Q\omega_m} \right)^2, \tag{4.82}$$

where the effective conductance,  $G_{DSEFF}$ , responsible for tank loading, is given by

$$\begin{aligned}
G_{DSEFF} &= G_{DS}[0] - G_{DS}[2] = \\
&\text{Re} \left\{ \frac{K}{6A_c\pi} \left( (2A_c^2 + V_{t_p}^2) \sqrt{1 - \frac{V_{t_p}^2}{A_c^2}} + 3A_cV_{t_p} \cos^{-1} \left( \frac{|V_{t_p}|}{A_c} \right) \right) \right\}.
\end{aligned} \tag{4.83}$$

Again, this expression assumes the tank capacitance is single-ended and the common-mode oscillation is completely suppressed. The noise factor then equals

$$\boxed{F_{\text{CMOS}_{\text{loaded}}} = (1 + \gamma)(1 + G_{DSEFF}R_p)}, \tag{4.84}$$

and this depends on both biasing and technology.

### 4.7.3.2 Oscillation Amplitude

When the tank capacitors are tied to ground, the oscillation amplitude is no longer given by  $A_c = (4/\pi)I_{BIAS}R_p$ . Instead, we derive the amplitude by calculating the fundamental



of the current drawn by the NMOS pair and the voltage-biased PMOS pair, summing the result, and multiplying by  $-R_p$ . The current-biased NMOS pair draws a differential current whose fundamental component is approximately

$$I_{NR_{NMOS}}[1] = -\frac{2}{\pi}I_{BIAS}, \quad (4.85)$$

while the voltage-biased PMOS pair draws a differential current whose fundamental component is

$$I_{NR_{PMOS}}[1] = g_{0p}A_c - \frac{9g_{0p}}{32V_{DG_p}^2}A_c^3 + \frac{5g_{0p}}{256V_{DG_p}^4}A_c^5, \quad (4.86)$$

where  $V_{DG_p} = V_{dd} - V_{out_{CM}}$ , and  $g_{0p}$  is conductance of the differential PMOS pair ( $-g_{mp}/2$ ) measured at DC. This expression is derived by modeling the PMOS nonlinearity as a 5<sup>th</sup> order polynomial<sup>19</sup>, as was done in Sec. 4.7.2. The oscillation amplitude is therefore calculated by finding the appropriate root of the implicit equation

$$\begin{aligned} A_c &= -(I_{NR_{NMOS}}[1] + I_{NR_{PMOS}}[1]) R_p \\ &= \left( \frac{2}{\pi}I_{BIAS} - g_{0p}A_c + \frac{9g_{0p}A_c^3}{32V_{DG_p}^2} - \frac{5g_{0p}A_c^5}{256V_{DG_p}^4} \right) R_p. \end{aligned} \quad (4.87)$$

Numerical methods are required to solve for  $A_c$ .

### 4.7.3.3 SpectreRF Simulations

The predicted noise performance of the CMOS voltage-biased topology, for the two capacitor arrangements discussed, was verified in SpectreRF. The oscillator was simulated using 90nm models, a 1.2V supply, and an ideal noiseless current source. An ideal linear tank with a  $Q$  of 19 and a resonant frequency of 500MHz ( $L=5\text{nH}$ ,  $C=20.2\text{pF}$ ,  $R_p=300\Omega$ ) was used. The dimensions of the differential NMOS and PMOS pair fingers were  $W=1.5\mu\text{m}$ ,  $L=0.2\mu\text{m}$ . The NMOS transistors had 50 fingers while the PMOS transistor had 225. Fig. 4.20 plots the simulated and predicted phase noise of the two topologies, measured at a 100kHz offset. The simulated and predicted amplitudes are plotted in Fig. 4.21 and are

---

<sup>19</sup>If there were no grounded capacitors, the differential current drawn by the PMOS transistors would equal  $-\frac{2}{\pi}I_{BIAS}$ .

in good agreement. The predicted and simulated results only diverge once the amplitude of oscillation reaches the rail voltage.

The results presented here show a substantial degradation in both amplitude and noise-performance, while the extent of this degradation depends on the size, biasing and technology parameters of the PMOS transistors.

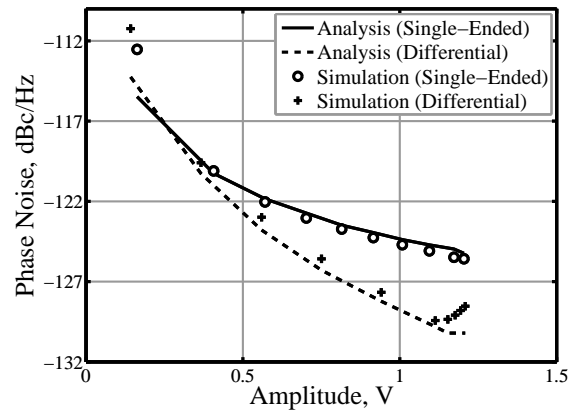


Figure 4.20: Phase noise performance of the CMOS standard current-biased  $LC$  topology with a differential capacitor arrangement and a single-ended capacitor arrangement.

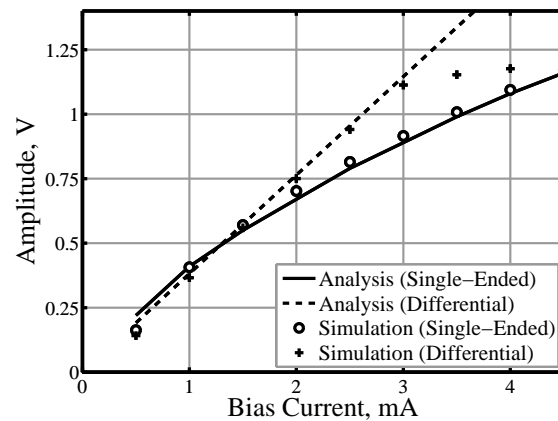


Figure 4.21: Amplitude of the CMOS standard current-biased  $LC$  topology with a differential capacitor arrangement and a single-ended capacitor arrangement.

## 4.8 Reconciling the ISF and Phasor-Based Approaches

The preceding analysis and results suggest that there is no fundamental difference between the ISF and phasor-based analysis methods. To truly reconcile the two approaches, we consider a small single-tone current, shaped by an arbitrary waveform, and injected into the negative-gm model (Fig. 4.4). We assume the injected tone is of the form  $i_k(t) = I_N \cos((k\omega_0 + \omega_m)t + \phi)$ , and is modulated by the function  $w(t)$ . Using the approach laid out in this work, the power in the resulting PM sideband is:

$$\begin{aligned} P_{\text{phasor}}\{\omega_m\} &= \mathcal{S}_{PM}\{k\} |Z_{PM}|^2 \\ &= \left(\frac{I_N^2}{8}\right) |W[-k+1] - W[-k-1]|^2 |Z_{PM}|^2. \end{aligned} \quad (4.88)$$

This is simply the PM component of  $i_k(t)$  (see (4.25)), multiplied by the PM transfer function given by Eqn. (4.19). On the other hand, Hajimiri and Lee's approach shows that the power in the resulting PM sideband is given by

$$\begin{aligned} P_{ISF}\{\omega_m\} &= \frac{A^2}{2} \left(\frac{I_n |\Gamma_{\text{eff}}[k]|}{2q_{\text{max}}\omega_m}\right)^2 \\ &= \frac{(I_n |\Gamma_{\text{eff}}[k]|)^2}{2} \left(\frac{\omega_0}{2Q\omega_m}\right)^2 R_p^2, \\ &= \frac{(I_n |\Gamma_{\text{eff}}[k]|)^2}{2} |Z_{PM}|^2 \end{aligned} \quad (4.89)$$

where  $q_{\text{max}} = CA_c$ ,  $\Gamma_{\text{eff}}(t) = \Gamma(t)\text{NTF}(t)$  and  $\Gamma(t)$  is the ISF. Now, Hajimiri and Lee's noise-transfer function (NTF) is the same as our noise-shaping function  $w(t)$ . While, Andreani and Wang [72] make the approximation that, in a nearly-sinusoidal oscillator, if the output is of the form  $V_{\text{out}}(x) = A_c \cos(x)$ , the ISF is given by  $\Gamma(x) = -\sin(x)$ . Using this approximation, the effective ISF Fourier coefficients are given by

$$\begin{aligned} \Gamma_{\text{rms}}[k] &= \frac{1}{T} \int_{T/2}^{-T/2} w(t)\Gamma(\omega_0 t)e^{-jk\omega_0 t} dt \\ &= \frac{j}{2} (W[k-1] - W[k+1]). \end{aligned} \quad (4.90)$$

Therefore

$$P_{ISF}\{\omega_m\} = \left(\frac{I_n}{8}\right)^2 |W[k-1] - W[k+1]|^2 |Z_{PM}|^2, \quad (4.91)$$

which is exactly the same as the expression obtained using the phasor-based approach (see Eqn. (4.88)). Again, unlike the phasor approach, the ISF has not yet been used to develop a closed form expression for AM sidebands.

Given the above analysis, the parallels between the two approaches are as follows: our noise-shaping function  $w(t)$  is identical to Hajimiri and Lee's NTF; the phasor decomposition of the sidebands around the carrier frequency (Sec. 4.4) performs the same operation as the ISF,  $\Gamma(x) = -\sin(x)$ ; and the preservation of the PM sideband-to-carrier ratio through the nonlinearity (Sec. 4.3.2), takes the place of the unit step in Hajimiri and Lee's phase impulse response function.

## 4.9 Conclusion

Using a phasor-based analysis method, we have re-derived the general result presented by Banks [55], and Mazzanti and Andreani [56]. With only a few steps, this can predict phase noise in a range of popular oscillator circuits and guide their optimal design. The phasor-based analysis also leads to simple expressions for amplitude noise in  $LC$  oscillators. In addition, the analysis sheds new light on the loaded  $Q$  of oscillators, in particular on the widely used fully differential CMOS  $LC$  oscillator.

Finally, we show that the two competing methods of phase noise analysis used today, ISF and phasor-based, are, in fact, equivalent.

## CHAPTER 5

# A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver

### 5.1 Introduction

The past few years have seen a dramatic rise in the number of mm-wave publications targeting the unlicensed 57-66GHz spectrum. This is with good reason: the unprecedented amount of available bandwidth should facilitate the emergence of a host of new products that utilize this band for short range, exceptionally high speed, wireless transmission. Sub-micron CMOS has already demonstrated adequate performance at these frequencies and, so, given well known semiconductor trends, will inevitably establish itself as the technology of choice for low-cost, high volume 60GHz products [73].

Current standards governing wireless communication at 60GHz are typically based on the IEEE 802.15.3c specification, which divides the band into four distinct channels with center frequencies ranging from 58.32GHz to 64.8GHz (Fig. 5.1). Modulation rates and schemes vary, but each channel should permit transmission rates of at least 2Gbit/s up to a distance of about 10 meters. Naturally, any transceiver (TRX) that is to be standard compliant requires a circuit to synthesize each of these carrier frequencies. As only four distinct tones are required, the integer-N PLL topology is sufficient, however, as in all mm-wave research, the challenge lies in the design of the blocks operating at very high frequencies, namely: the VCO, buffer and dividers, which all require an output-referred tuning range in excess of 7GHz. Moreover, as systems move away from single-carrier modulation and adopt more complex schemes (such as OFDM), achieving good phase

noise performance coupled with wideband tuning will become increasingly necessary and challenging. Within this context, we present a low noise, integer-N PLL that is capable of supporting a heterodyne 802.15.3c TRX where the receive/transmit frequency ( $f_{TRX}$ ) is 1.25 times the main synthesizer tone ( $f_{LO}$ ) and 5 times the intermediate frequency ( $f_{IF}$ ), i.e.  $f_{TRX} = (5/4)f_{LO} = 5f_{IF}$  [74].

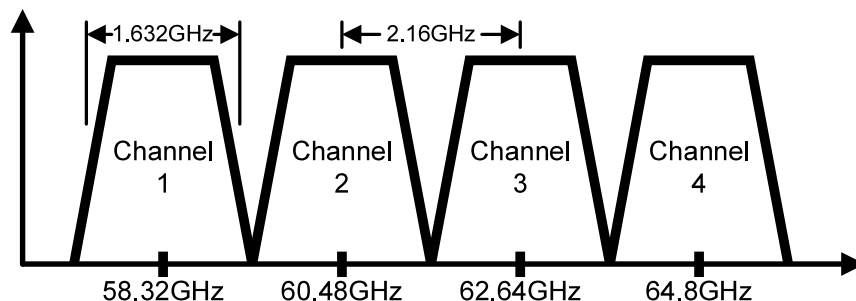


Figure 5.1: The IEEE 802.15.3c channel specification.

Previous work has already demonstrated the feasibility of CMOS mm-wave synthesizer design. In [75], the authors used injection locking to reduce area and power while maintaining good in-band noise performance. Later, in [76], a synthesizer that generated quadrature outputs directly at 60GHz with a 9GHz tuning range was realized, although the authors were unable to measure quadrature accuracy. Both these publications report poor phase noise measurements for frequency offsets outside the PLL’s loop bandwidth. More recent work has employed a quadrature-VCO running at 20GHz and a push-push technique to isolate the 2<sup>nd</sup> harmonic [77]. This work, which specifically targeted the IEEE 802.15.3c specifications, could cover three of the required four 60GHz channels and demonstrated very good phase noise (-94dBc/Hz@1MHz normalized to Band 3). Despite good performance metrics, drawbacks to this approach exist: Quadrature oscillators add substantial design complexity and introduce issues such as the potential for uncertain mode behaviour and reduced quadrature accuracy. In addition, techniques that isolate the 2<sup>nd</sup> harmonic typically provide poor drive strength, or require power hungry buffers prior to the down-conversion mixers. Compared to [77], we achieve a wider tuning range and lower phase noise using a VCO to directly generate the  $f_{LO}$  frequency. This simpler and more robust

approach avoids the aforementioned issues.

Central to this endeavour is the design of a wideband, mm-wave VCO. While standard RF design techniques can be applied to mm-wave designs, one should be aware of certain changes to the design paradigm. Most notably, resonator loss is typically determined by the quality of the capacitive-tuning elements rather than the inductor and, therefore, the choice and design of this tuning element has a large impact on the performance of the VCO itself. Moreover, while second-order effects such as tank loading and flicker noise up-conversion can dominate in any wideband CMOS VCO, the situation is even more deleterious in mm-wave oscillators, since it is difficult to realize a high impedance node at twice the oscillation frequency across the entire tuning range [78] [79]. The problem is further exacerbated if a single large varactor is used to cover the very wide tuning ranges typically demanded at mm-wave; the poor  $Q$  of CMOS varactors at mm-wave degrade the  $Q$  of the resonator, while the resultant large and nonlinear  $K_{VCO}$  values increases AM-to-PM conversion [80]. To minimize such effects, it is necessary to linearize the resonator as much as possible and limit the size of the varactor, which typically means introducing some form of digital tuning into the design [81]. Another important practical concern at mm-wave frequencies is routing parasitics, which can result in large discrepancies between simulation and measurement. To address these problems, this work utilizes Digitally-Controlled-Artificial-Dielectric (DiCAD) as a frequency tuning element in all mm-wave circuit blocks. DiCAD originated as a method to control the permittivity of a differential transmission line using CMOS switches [82]. When used in resonators, DiCAD is a useful technique that enables fine and linear digital frequency tuning, minimizes routing parasitics, and facilitates “first-time right” design [83].

As with many published mm-wave CMOS circuits, both lumped-element techniques and distributed-element techniques [84] have been successfully employed in mm-wave VCOs. Generally speaking, a purely lumped-element approach results in more compact designs, whereas a distributed-element approach results in better matching between simulation and measurement (transmission lines give more precise control over small reactances and in-

terconnect wiring can be incorporated into the model [85]). The approach outlined in this work, specifically the use of DiCAD, can be viewed as a hybrid approach that uses a programmable transmission line to realize very fine resonator tuning while accurately modelling interconnect routing, but uses lumped-element design elsewhere to reduce area.

Section 5.2 introduces the choice of PLL topology and discusses the frequency plan of the TRX for which the PLL was designed. Section 5.3 discusses the advantages of using DiCAD as a frequency tuning element, while Sec. 5.4 documents other key mm-wave design choices. Measurements are provided in Sec. 5.5 and conclusions are drawn in Sec. 5.6.

## 5.2 PLL Topology

The PLL described in this work was designed to support a heterodyne transceiver that employs separate, but identical PLLs for the receive and transmit paths (Fig. 5.2). A dual PLL solution was used to reduce the LO routing between the VCO buffer and the RF mixers, which can result in drive strength issues at 48GHz. Referring to the receive path: the incoming 60GHz signal ( $f_{RX}$ ) is first downconverted through a single-phase 48GHz tone ( $f_{LO}$ ) to a 12GHz intermediate-frequency ( $f_{IF}$ ), before being downconverted again to the baseband through I/Q paths. While this architecture requires an anti-aliasing filter to suppress the image and minimise noise-folding, it has the advantage of greatly relaxing the design of the frequency synthesizer. A direct conversion transceiver would require I/Q generation at 60GHz, which would necessitate either a 120GHz VCO, or a 60GHz QVCO complete with its many shortcomings including: I/Q routing and accuracy issues, and potential uncertainty in mode selection. By contrast, the two-step (or heterodyne) approach requires only a single-phase 48GHz VCO, while the 12GHz I/Q signals are generated through a CML divider.

There is also some performance advantage to operating the VCO at 48GHz as opposed to 60GHz. As you move to higher frequencies, capacitor- $Q$  degrades linearly with frequency, while inductor- $Q$  ideally increases as a linear function of frequency. In CMOS technolo-



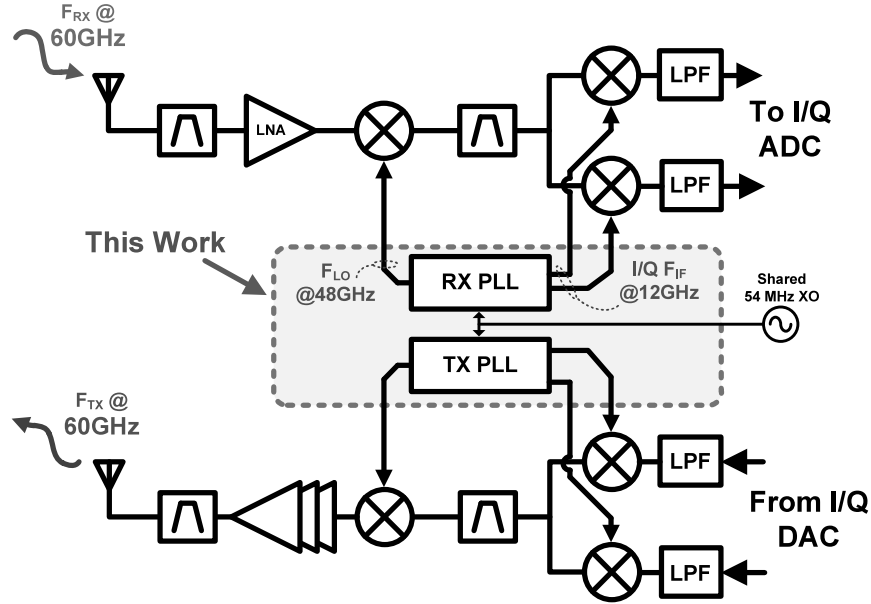


Figure 5.2: A heterodyne 60GHz transceiver with separate TX/RX PLLs.

gies, however, inductor-Q's are typically limited by skin effects and substrate losses and, so, while there might be some benefit to operating a narrowband mm-wave oscillator at higher frequencies (in terms of oscillator figure of merit), it is deleterious for very wideband oscillators where capacitive tuning elements determine the resonator-Q.

The proposed programmable integer-N, Type-II, 3<sup>rd</sup> order PLL is shown in Fig. 5.3. The focus of this work is the mm-wave blocks consisting of a DiCAD-based VCO, injection-locked buffer and injection-locked frequency divider (shown separately in Fig. 5.4). The rest of the divider chain consists of CML-based logic; a prescaler divides the 24GHz divider output by 16 while also generating I/Q phases at 12GHz, and a multi-modulus divider further divides the signal by  $16+N$  (where N is a 4-bit binary code). Using this scheme, any divide ratio from 512 to 992 in steps of 32 can be obtained. This divide ratio together with a 54MHz reference enables synthesis of the required tones. A PFD, current-steering charge pump and 2<sup>nd</sup> order on-chip loop filter complete the block. To increase flexibility during testing, the on-chip loop filter can be disabled and an off-chip loop filter can be employed.

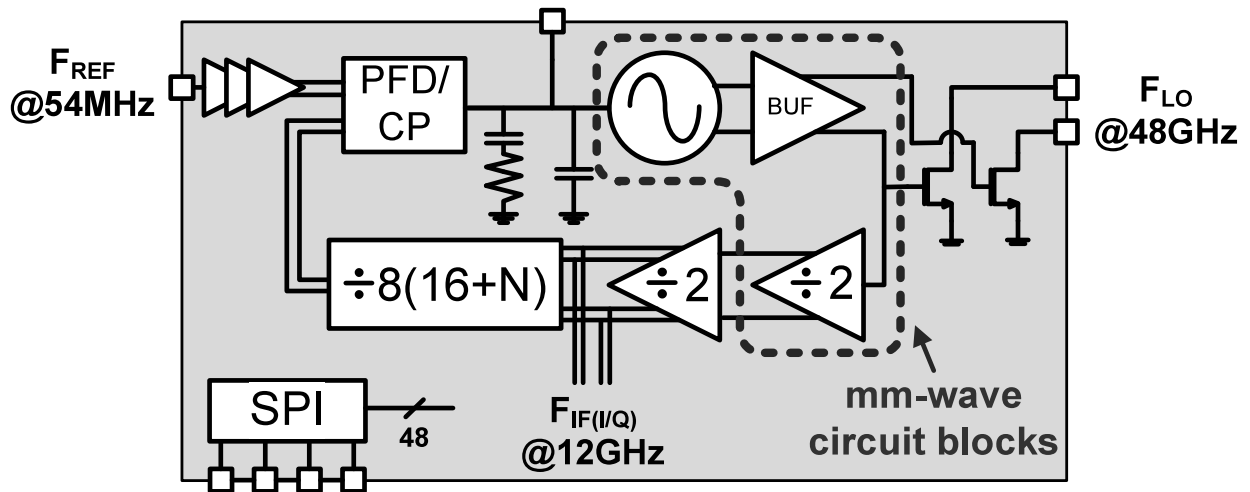


Figure 5.3: The fabricated integer-N type-II 48GHz PLL (with highlighted mm-wave blocks).

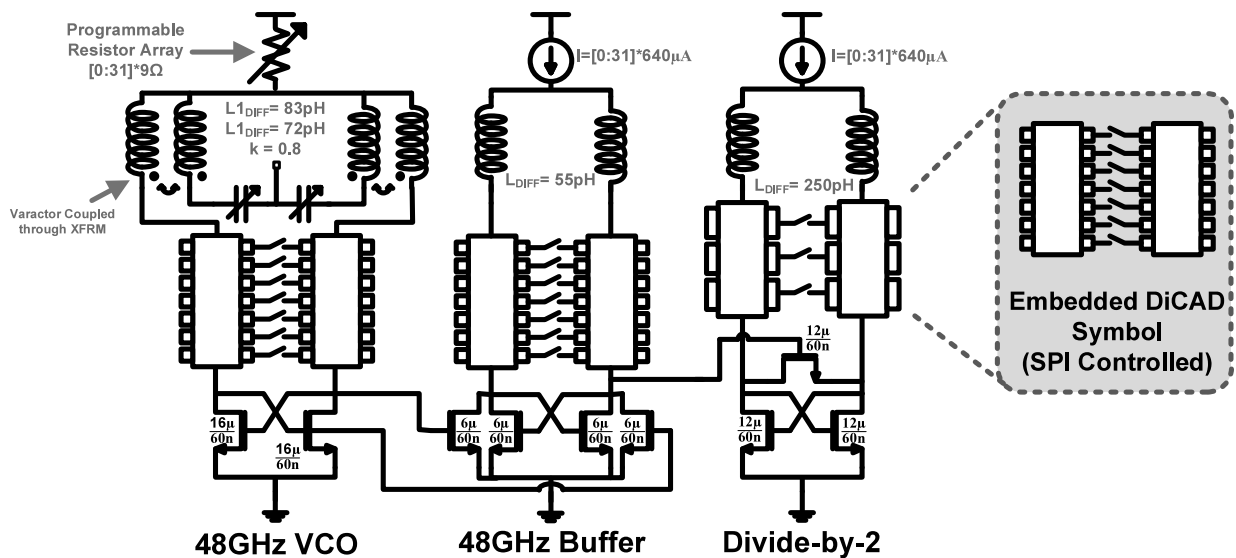


Figure 5.4: Mm-wave circuit blocks used in the PLL. All blocks employ DiCAD as frequency tuning element.

## 5.3 Frequency Tuning using DiCAD

In this work all the mm-wave resonators employ DiCAD as a digital frequency tuning element. Its origin, structure and advantages are outlined in this section.

### 5.3.1 The Motivation for DiCAD

A simplified lumped equivalent model of an  $LC$  oscillator is shown Fig. 5.5(a). Losses in the inductor and capacitive-tuning element as well as any equivalent positive resistance in the energy restoring circuitry will degrade the resonator's  $Q$  [86]. Compared to RF, inductor- $Q$ 's at mm-wave frequencies can be very good; in the process used in this work, i.e. a 6-metal layer process with an ultra thick top metal layer ( $3.4\mu\text{m}$ ), it is possible to obtain  $Q$ 's in excess of 25 at 48GHz for a single turn inductor. Further, since  $Q$ -degradation due to transistors in the energy restoring circuit is hard to avoid in mm-wave designs, this work has focused on the design of the capacitive tuning element, which typically limits performance. The simplest way to obtain the required frequency tuning is to use a single large varactor, but this comes at the cost of a substantial degradation in resonator- $Q$ . Its large  $K_{VCO}$  value also results in a large up-conversion of flicker noise and, when employed in a PLL, a large up-conversion of noise from the charge pump and loop filter. The standard approach to minimizing these effects is to employ both discrete tuning and continuous tuning [81], where linear capacitors provide discrete tuning, and a small varactor (with an accompanying small  $K_{VCO}$  and reduce effective loss) provides continuous tuning. Such discrete-linear tuning can be realised using a bank of varactors, which are digitally controlled such that are always biased in their linear region (Fig. 5.5(b)). A better approach to use a bank of switchable capacitors (Fig. 5.5(c)), which exhibits an improved trade-off between  $Q$  and tuning range (TR); a large switch gives better  $Q$ , but a reduced  $C_{ON}/C_{OFF}$  ratio and vice versa [87] (Fig. 5.5(d)). While this approach works well at RF frequencies, it is problematic at mm-wave where interconnect traces contribute a significant portion of inductance and capacitance to the resonator, which can significantly shift the center frequency. Accounting for all these traces, while possible [88], is difficult and becomes increasingly problematic at

higher frequencies. To speed design times, one can always overdesign the switch capacitor bank with a large overlap between switch code and a large margin at either side of the band, but this unnecessarily reduces the resonator's  $Q$  and thus reduces the oscillator's figure of merit (FOM). The goal is therefore to realize a capacitive-tuning scheme that not only minimizes parasitics, but also accurately accounts for them.

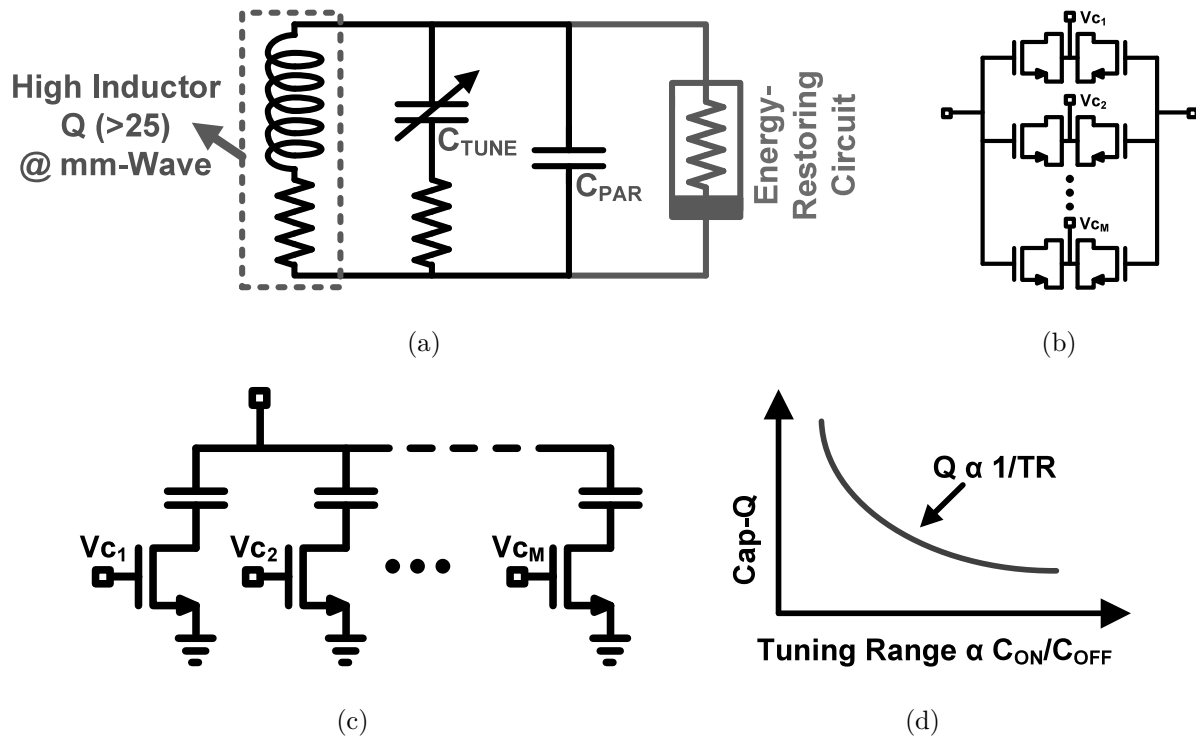


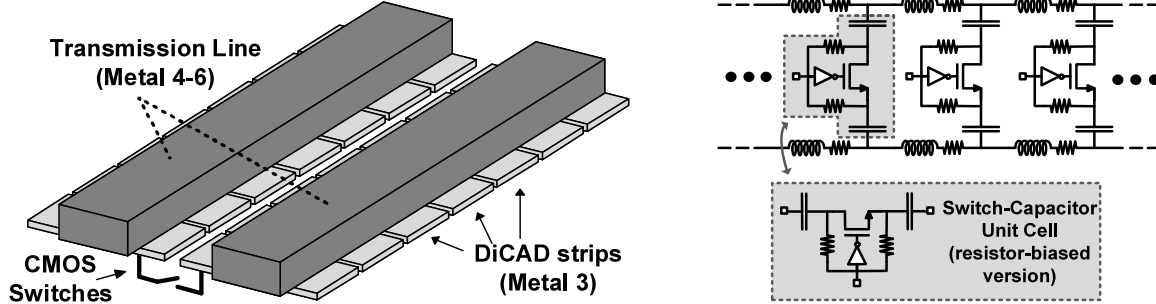
Figure 5.5: An overview of possible frequency tuning schemes. (a) Simplified  $LC$  oscillator; wideband mm-wave VCOs are typically limited by loss associated with  $C_{TUNE}$  (b) Digitally controlled varactor bank (c) Switch capacitor bank is best option at RF, but interconnect reduces performance at mm-wave. (d)  $Q/TR$  trade-off of a switch cap array.

### 5.3.2 DiCAD Structure

Early publications reporting CMOS 60GHz circuits, had as much in common with discrete microwave design as it had with standard RF CMOS lumped-element design. Quarter-wave resonators, transmission lines and inter-stage matching techniques were common. In an effort, to provide flexibility for such designs, the idea of DiCAD (or Digitally controlled

Artificial Dielectric [82] [83]) was developed. DiCAD consists of a transmission line constructed from the top metal layers in a CMOS process, underneath which are placed metal strips (see Fig. 5.6(a)). By placing a CMOS switch between these strips, the equivalent dielectric constant of the transmission line can be altered and thus its electric length can be changed. For our purposes, this structure can be viewed as a distributed capacitor array (Fig. 5.6(b)) and, therefore, when used in an mm-wave VCO, DiCAD can reduce the varactor size (and  $K_{VCO}$ ) in the same way as switched-tuning of a VCO [81], i.e., the DiCAD structure provides discrete linear tuning and, therefore, only a small varactor is needed to provide continuous tuning. Using this structure as a frequency tuning element at mm-wave has a number of advantages:

- It is easily modelled: By importing the structure (with ideal open and shorts between the strips) into an electromagnetic (EM) simulator, the equivalent transmission line model in Fig. 5.6(b) can be obtained. Once the CMOS switches are included, it can be used in all circuit level simulations.
- It is EM friendly: The structure is very regular and results in short EM simulation times.
- It eliminates/accounts for routing parasitic: Routing parasitics are inherent in the structure and, so, are completely captured in the transmission line model. For instance, in our final design, the differential inductance of the transmission line with all switches open is approximately 34pH. Given that the equivalent inductance of the transformer (XFMR) used in the resonator is only 83pH, neglecting the effect of routing would create a significant difference between the simulated and measured oscillation frequencies.
- It is accurate: Each pair of DiCAD strips function as a capacitor, which in our design is calculated as approximately 3fF differentially. Such small values allow us to sacrifice area (compared to MIM or finger caps), with reduced variability.



(a) The physical structure of (DiCAD); when all switches are closed, the structure can be viewed as a “slow-wave” transmission line [85].

(b) The circuit equivalent model of DiCAD can be viewed as a distributed switch capacitor bank.

Figure 5.6: Digitally-Controlled-Artificial-Dielectric (DiCAD).

Embedding this structure into all the mm-wave resonators enables fine digital tuning (down to a few fFs) and “first-time right” design promised by distributed element design. Indeed, in the final design, the discrete tuning resolution and was not limited by the DiCAD structure, instead excessively small steps were avoided in order to prevent the PLL falling out of locked due to frequencies variations arising from temperature or amplitude changes.

### 5.3.3 Switch-Selection

In the same way that a transmission line is schematically indistinguishable from its  $RLCG$  frequency dependant model, DiCAD is schematically indistinguishable from a distributed switched capacitor bank. Given this, its performance is fundamentally limited by the CMOS transistors in the equivalent switched-capacitor unit cell (Fig. 5.6(b)). Two common switch-capacitor unit cells are shown in Fig. 5.7. The self-biased switch (Fig. 5.7(a)) was used in the first realisation of a switched-tuning VCO [81]. The resistor-biased version (Fig. 5.7(b)) is also commonly used and has been shown to exhibit an enhanced  $Q$  and, thus, exhibits a better trade-off between tuning range and phase noise [87].

In addition, we have also observed a reduction in phase noise degradation due to drain-to-source leakage currents when the resistor-biased switch is used. Consider the self-biased switch: When the switch is in the OFF state, the oscillation waveform at the drain node is

such that at the trough of an oscillation, the drain voltage briefly drops below the source. This causes the device to pull current from the ground. Under steady-state conditions, the amount of charge pulled from ground must equal the charge lost due to device leakage current. Noise associated with these currents can degrade the overall phase noise performance of the VCO. By contrast, the resistor-biased switch does not suffer from this effect; when OFF, both the  $V_{GS}$  and the  $V_{GD}$  of the transistor are biased around a large negative potential ( $-V_{DD}$ ) and, so, the amount of leakage current is greatly reduced. Fig. 5.7(c) shows simulation results for our finalized VCO with both the self-biased and resistor-biased switches. As expected, when the switches are on, the performance is similar. However, when all 32 switches are off, the resistor-biased switch achieves a 7.5dB improvement in phase noise. Using SpectreRF, it was deduced that this degradation was due to noise current flowing in the OFF switches. This mechanism is likely to be apparent only in deep-scaled general-purpose (GP) CMOS technologies where significant leakage currents are present, as opposed to the low-power (LP) CMOS process option. Based on these simulation results, the resistor-biased switch was implemented in our design and sized such that the OFF capacitance was  $\approx 1.3\text{fF}$  while the ON capacitance was  $\approx 3\text{fF}$ .

## 5.4 Key Millimeter-Wave Design Choices

A central focus of this work has been on the design of mm-wave blocks shown in Fig. 5.4, since performance metrics of these blocks translate directly into important integer-N PLL performance metrics such as tuning range, power consumption, and phase noise. The remaining circuit blocks that operate at lower frequencies, while important, are well understood and have been extensively studied elsewhere.

### 5.4.1 mm-Wave VCO

The VCO was realized using the standard voltage-biased NMOS topology. Compared to the current-biased topology, the voltage-biased topology is known to result in  $Q$ -degradation of

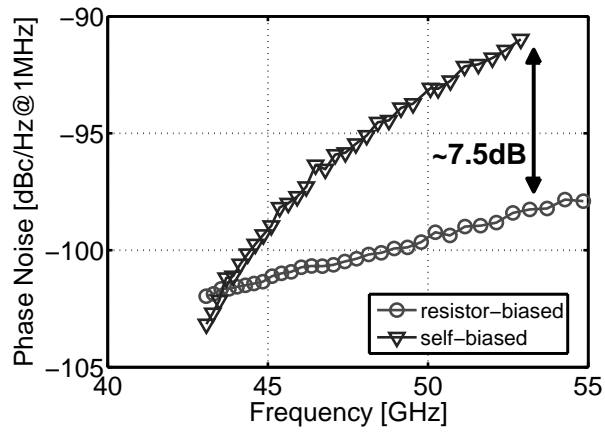
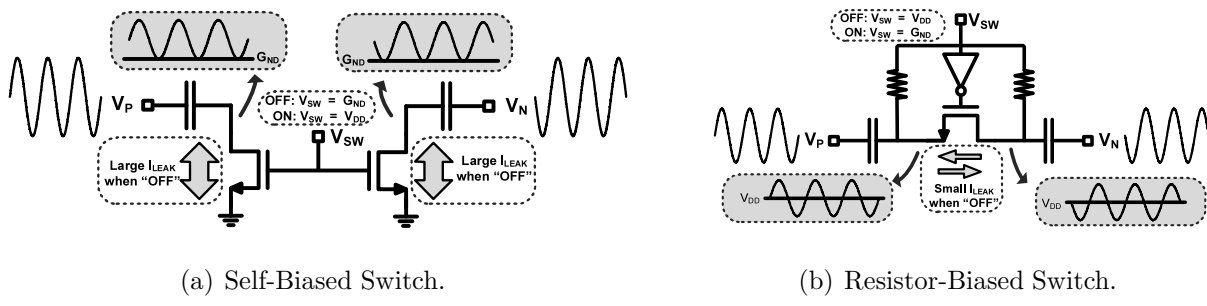


Figure 5.7: A comparison of switches that can be used in the programmable transmission line.



the resonator (explained in [78] and quantified in [86]). However,  $Q$ -degradation will also occur in current-limited topologies if the current source does not present a high impedance around the 2<sup>nd</sup> harmonic [78]. For this design, this criterion would require a current source with a high impedance that is tunable from 86GHz to 104GHz. Given the difficulty of realizing such a design, the voltage-biased topology was instead chosen with a programmable resistor to control the amplitude. Compared to a standard current source, the programmable resistor has the advantage of being flicker noise free. Excessive  $Q$ -degradation was avoided by limiting the VCO amplitude. The VCO resonator consists of:

- 5-bit DiCAD: DiCAD is used to provide fine digital tuning. The differential series inductance of the transmission line is calculated as 34pH, while the differential capacitance (when closed) of each of 31 strips is approximately 3fF. Since DiCAD is a distributed structure, the unit capacitor-cells, although identical, do not have the same effect on the oscillation frequency. Therefore, to ensure monotonicity, a thermometer code is used to digitally control the DiCAD.
- Varactor: To maximize the varactor tuning range for a given size and to eliminate variation with the core bias point, the varactor is typically AC-biased through large capacitors to the resonator. To save area and eliminate top/bottom plate capacitance, we coupled the varactor to the resonator through a transformer (XFMR). This is possible because of the large XFMR coupling coefficient observed at mm-wave ( $>0.8$ ). The effective small-signal capacitance of the varactor ranges from 3fF to 9fF.
- Single Turn Transformer: The XFMR used to couple the varactor to the VCO core, also contributes an effective 84pH of inductance. The primary coil consists of a single turn inductor drawn on metal 6, while the secondary coil is an identically dimensioned and positioned inductor drawn on metal 5.

### 5.4.2 DiCAD-Based Injection-Locked Buffer and Divider

Since the PLL is intended for use in a TRX, a buffer is required to isolate the VCO from the signal path. To keep power consumption low, an injection-locked oscillator is employed as the buffer (Fig. 5.4). To ensure good frequency alignment, the injection-locked buffer has a very similar design approach and layout style to that of the oscillator. To account for the different load capacitance, there are, however, differences: the equivalent inductance used in the resonator is smaller, while the DiCAD switches are also reduced in size to maintain the require frequency range. (We are less concerned with resonator- $Q$  in the buffer as it does not impact phase noise.)

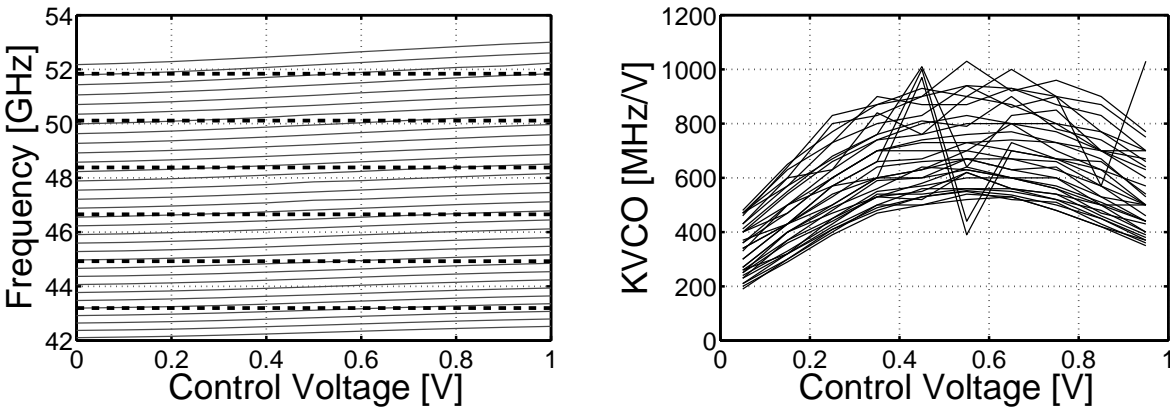
The first divide-by-2 stage is also an injection-locked topology [89] (Fig. 5.4). Although the divider could be realized by an aggressive CML design, the injection-logic topology is a low power option. As in the design of the buffer, precise frequency alignment is needed to ensure that the PLL lock over the entire VCO tuning range. This requires that the free running frequency of divider is close to half that of the VCO/buffer. Accordingly, DiCAD is employed in both designs to tune the resonators to the appropriate frequency. As in the VCO, 5-bit DiCAD is used in the buffer. The divider locking range is wide enough that only 4-bit DiCAD is required. Naturally, when employed in a full system, the DiCAD states of the VCO, buffer and divider need to be calibrated on chip. Provided locking time is not critical, this calibration can be accomplished using the straightforward scheme presented in Sec. 5.5.

## 5.5 Measurement Results

The PLL, shown in Fig. 5.3, was fabricated in a 65nm GP process. An on-chip Serial-to-Parallel Interface (SPI) controls 48 bit-lines that are used for digital control current, digital frequency tuning and other various control lines. A PTAT current reference is used to provide accurate bias currents. The 48GHz injection-locked buffer drives two open drain buffers that are probed directly using GSSG probes. The control voltage is connected

directly to a pad so that VCO tuning curves can be measured and the loop bandwidth can be modified during testing. The reference is provided by an ultra-low noise 54MHz Crystek XO.

The measured VCO tuning curves are shown in Fig. 5.8. Continuous tuning from 42.1GHz-to-53GHz is achieved with a  $K_{VCO}$  of less than 1GHz/V. The worst case band overlap is approximately 50%. Figure 5.9 plots the VCO frequency versus the DiCAD state and clearly shows the distributed nature of DiCAD; a conventional switched capacitor bank would result in non-uniform frequency steps that widen at higher frequencies, by contrast, DiCAD tuning results in very fine, monotonic digital tuning that is remarkably linear, as shown in the digital INL/DNL plots of Fig. 5.9(b). This is due solely to the distributed nature of DiCAD, since the effective capacitance of identical DiCAD strips (as observed from the differential pair) reduces as you move along the DiCAD structure. Because of this, a thermometer code is used where the LSB is closest to the inductor and the MSB is closest to the differential pair; reversing the direction would result in a frequency spacing that is even more non-uniform than would be expected in a lumped switched capacitor-bank.



(a) The continuous tuning curves. (Heavy dotted lines correspond to frequencies that can be synthesized.) (b)  $K_{VCO}$  overlaid for all 32 DiCAD states. Discontinuities are due to measurement error.

Figure 5.8: Measurement of the VCO's continuous tuning characteristics.

Under closed-loop operation, the PLL is capable of generating 6 equally spaced tones: 43.2GHz, 44.928GHz, 46.656GHz, 48.384GHz, 50.112GHz and 51.84GHz. The latter 4

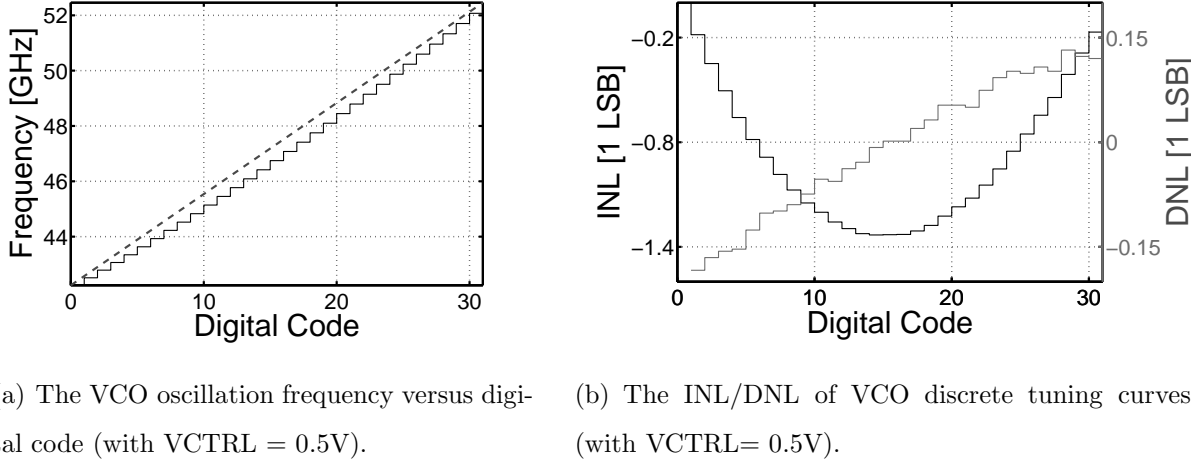
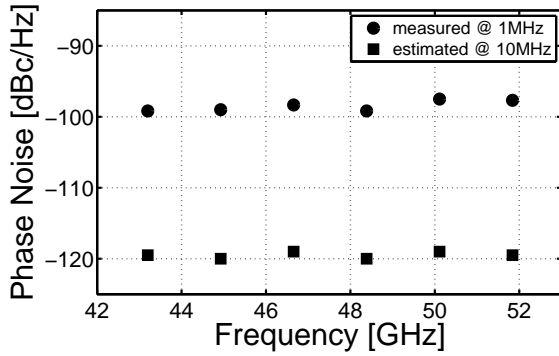


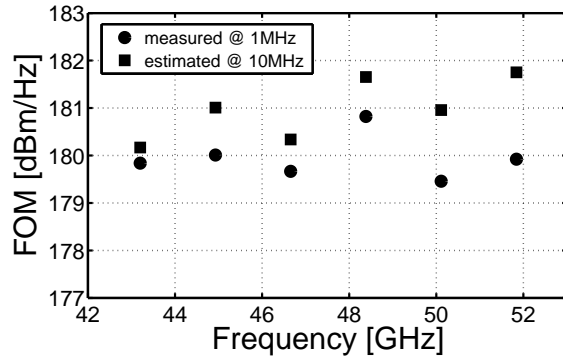
Figure 5.9: Measurement of the VCO's discrete tuning characteristic.

tones are precisely  $4/5$  of the channel frequencies defined in the IEEE 802.15.3c standard and are suitable for a heterodyne IEEE 802.15.3c TRX with  $f_{TRX} = (5/4)f_{LO} = 5f_{IF}$ . The achievable out-of-band noise (i.e. noise which appears outside the loop bandwidth of the PLL) is measured using a large off-chip loop filter that reduces the PLL loop bandwidth to less than 100kHz. Phase noise measurements and other performance metrics are shown in Table 5.1 and Fig. 5.10, and typical outputs from the spectrum analyzer are shown in Fig. 5.11. Note that the noise performance is maintained across the entire band. This fact is important, as a wideband PLL that employs a large varactor to cover the entire tuning range will experience a flicker-noise null at a single point [81]. Since the out-of-band noise is basically the noise contribution of the VCO itself, Table 5.2 compares the DiCAD-VCO with recently reported mm-wave CMOS VCOs. When performance across the entire band is considered, the DiCAD-VCO achieves the best performance in terms of tuning range and oscillator figure of merit, i.e.  $FOM_T$ .

When the on-chip loop filter is enabled, the loop bandwidth sits around 1MHz and the inband noise is measured at -81dBc/Hz (Fig. 5.12). This number is as good as or better than other standard integer-N topologies that employ similar divide ratios [75] [92], and can be reduced further by increasing the charge pump current (although charge pump noise dominates the inband noise profile of this design, only  $400\mu A$  is currently dissipated in the

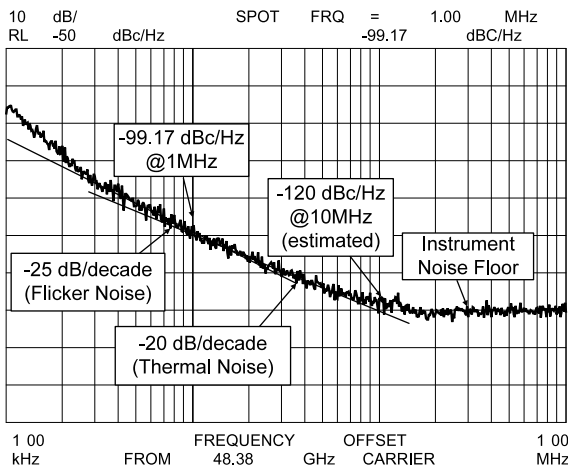


(a) Phase Noise Measurements.

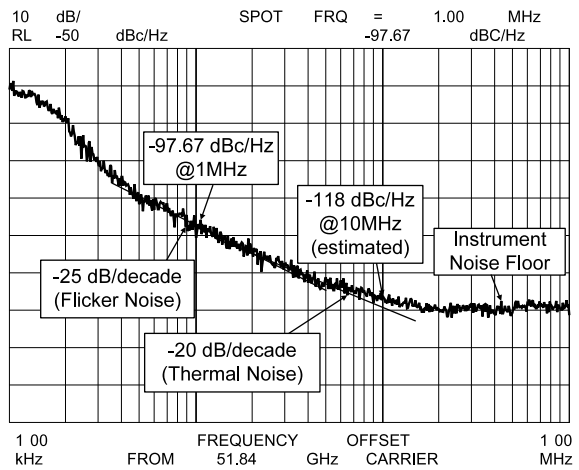


(b) Figure of Merit.

Figure 5.10: The performance metrics of the DiCAD-VCO across entire frequency band.



(a) Phase noise @ 48.384GHz.



(b) Phase noise @ 51.84GHz.

Figure 5.11: The closed loop phase noise measurements with a large off-chip loop filter.

Table 5.1: Phase noise and figure of merit measurements @1MHz offset

Frequency [GHz]	$\mathcal{L}\{\Delta\omega\}$ [dBc/Hz]	FOM <sup>†</sup>	FOM <sub>T</sub> <sup>‡</sup>
43.2	-99.17	179.84	187.04
44.928	-99	180.01	187.21
46.656	-98.33	179.67	186.87
48.384	-99.17	180.82	188.02
50.112	-97.5	179.46	186.66
50.84	-97.67	179.92	187.12

$$^{\dagger}\text{FOM} = -\mathcal{L}\{\Delta\omega\} + 20 \log_{10}(\omega_0/\omega_m) - 10 \log_{10}(P_{\text{DC[mW]}})$$

$$^{\ddagger}\text{FOM}_T = \text{FOM} + 20 \log_{10}(TR/10)$$

charge pump, which is relatively small compared to the total power consumption of the chip). The I/Q signals were not brought off-chip and could not be measured.

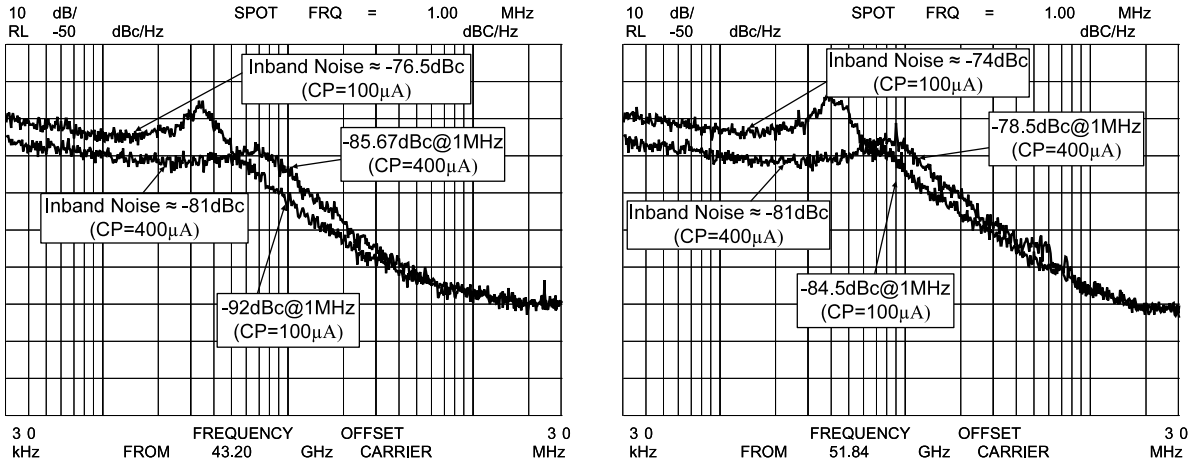
Table 5.3 compares our PLL design with the recent publications. Compared to the state-of-the-art [77], our work improves normalized phase noise, covers an additional 60GHz band, consumes less power and 64% less area, and operates at a higher frequency. More importantly, the VCO also directly generates the  $f_{LO}$  frequency. This is in contrast to [77], which isolates the 2<sup>nd</sup> harmonic of a push-push QVCO operating at  $f_{LO}/2$ . Therefore, we avoid the problem of limited 2<sup>nd</sup> harmonic drive strength and all issues associated with QVCOs (unpredictable mode behaviour, increased I/Q mismatch, increased area). The die micrograph of the testchip is shown in Fig. 5.13(a). The PLL was used a dual-synthesizer TRX [93] and a micrograph of that chip is shown in Fig. 5.13(b).

As with any PLL, the free-running frequency of the VCO must be close to the desired synthesized frequency to allow the control voltage to lock the PLL. In this design, the same is true for the mm-wave buffer and 24GHz divider, which are also capable of operating as free-running oscillators. This means the DiCAD states in the VCO, buffer and divider must be appropriately chosen in order for the PLL to successfully lock. A method to calibrate injection locked dividers within the PLL has already been demonstrated [94]. In our 60GHz solution, we are less concerned with locking time and, therefore, intend to use a far simpler

Table 5.2: Comparison with other 65nm/90nm wideband mm-wave VCOs

	[84] JSSC '07	[90] VLSI-DAT '09	[91] JSSC '09	[88] RFIC '10	This Work
Technology	0.18 $\mu$ m CMOS	0.18 $\mu$ m CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Center Frequency [GHz]	40.0	47.9	58.4	39.9	47.55
Supply [V]	1.5	1.2	0.7	1.2	1
$\mathcal{L}\{\Delta\omega\}@1\text{MHz}$ [dBc/Hz]	-100.2	-102.5	-91	-98.1	-97.5
Power [mW]	27	5.6	8.1	14.4	16
Core Area [ $\mu\text{m}^2$ ]	900 $\times$ 200 <sup>†</sup>	N/A	96 $\times$ 80	300 $\times$ 500	220 $\times$ 125
Tuning Range [%]	20	1.59	9.32	15.1	22.9
FOM <sub>T</sub> [dBc/Hz]	183.9	172.7	176.6	182.1	186.6

<sup>†</sup>Estimated from dimension of die micrograph.



(a) Phase noise @ 43.20GHz.

(b) Phase noise @ 51.84GHz.

Figure 5.12: The closed loop phase noise measurements with on-chip loop filter enabled.

Table 5.3: Comparison of PLL with recent state of the art

	[75] ESSCIRC '07	[76] ISSCC '09	[77] ISSCC '10	This Work
Technology	90nm CMOS	45nm LP CMOS	65nm LP CMOS	65nm GP CMOS
Architecture	Integer-N (VCO @ 60GHz)	Integer-N (QVCO @ 60GHz)	Integer-N (QVCO @ 20.88GHz)	Integer-N (VCO @ 50.112GHz)
Frequency Range [GHz]	61.1-63.1	57-66	35-41.88	42.1-53
Supply [V]	1.2	1.1	1.2 <sup>§</sup>	1
$\mathcal{L}\{\Delta\omega\}@1\text{MHz}$ [dBc/Hz]	-80	-75	-90.46 <sup>†</sup> -93.98 <sup>‡</sup>	-95.56 <sup>†</sup>
Reference Frequency [MHz]	60	100	36	54
Power [mW]	78	78	80	72
IEEE 802.15.3c Band Coverage	1 Band	All 4 Bands	3 Bands	All 4 Bands
Core Area [ $\mu\text{m}^2$ ]	600 $\times$ 600	N/A	1100 $\times$ 1000	680 $\times$ 550
Tuning range [%]	3.2	14.6	17.9	22.9
$\mathcal{L}_{\text{inband}}\{\Delta\omega\}$ [dBc/Hz]	-72	-75	N/A	-81

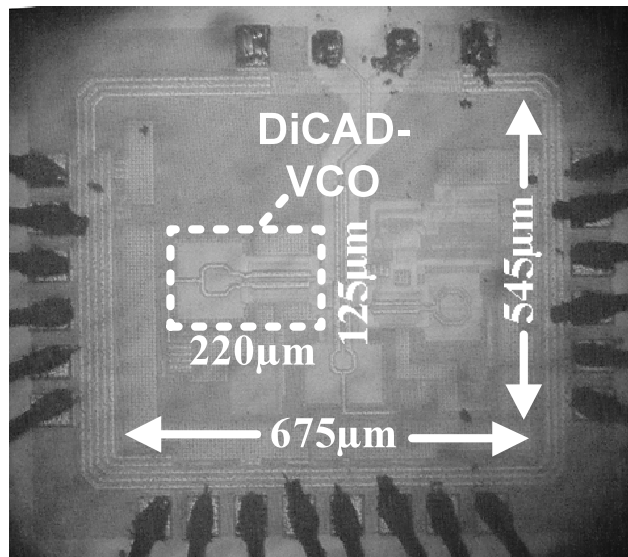
<sup>§</sup> 1.8V used for CP/PFD

<sup>†</sup> Normalized to 62.64GHz from 50.112Hz measurement

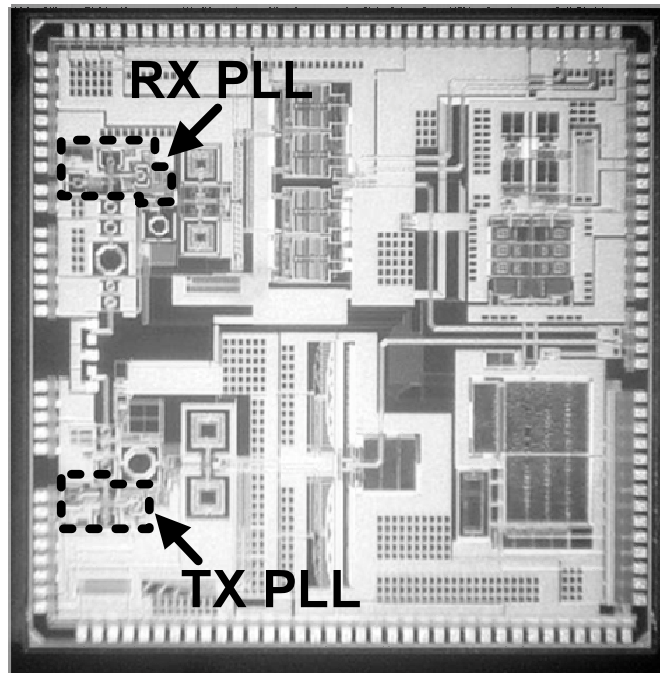
<sup>‡</sup> Normalized to 62.64GHz from 20.88Hz measurement

<sup>‡</sup> Normalized to 62.64GHz from 41.96Hz measurement





(a) PLL Testchip with DiCAD-VCO highlighted.



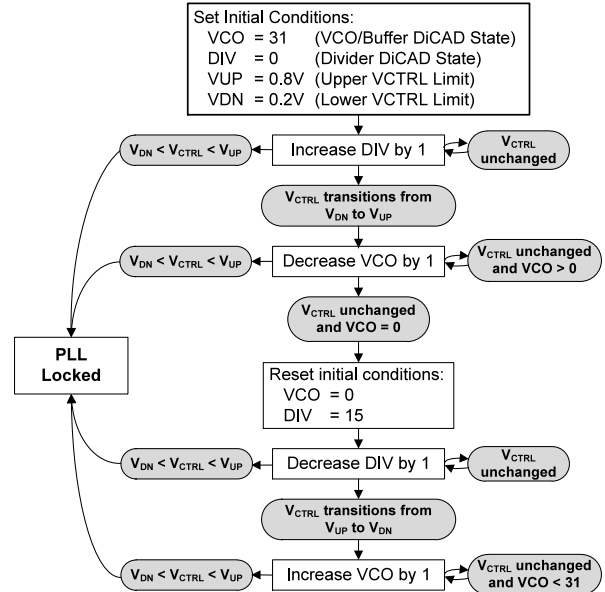
(b) Dual PLL TRX.

Figure 5.13: The die micrographs.

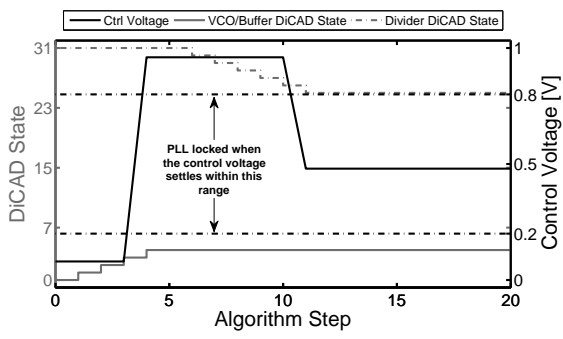
closed-loop calibration scheme. Firstly, we assume that the VCO and buffer frequencies are closely aligned and are always set to the same bit. Then, using the trivial algorithm outlined in Fig. 5.14(a), we sweep the VCO/buffer and divider control bits while monitoring the control voltage. Once the control voltage settles to a value that is not either ground or the power rail, the PLL can be considered locked. To replicate a complete TRX SOC, the control voltage is digitized using an off-chip ADC. The algorithm (which can be run in a microcontroller) monitors the digitized control voltage and changes the frequency settings using the on-chip SPI. Four chips were tested and all of them successfully locked across all 4 bands. Examples of the locking algorithm are shown in Fig. 5.14(b) and Fig. 5.14(c). More sophisticated schemes, such as [95], can be employed if a faster locking time is required.

## 5.6 Conclusion

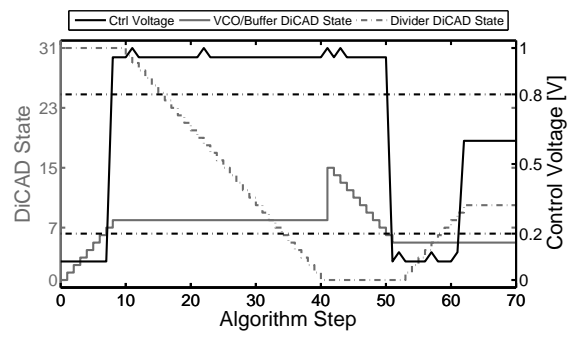
A low-noise, wideband PLL that can support a complete IEEE 802.15.3c TRX is reported. The circuit is simple and robust, and the LO tone is generated by the fundamental of the VCO rather than by some harmonic. Further, by embedding a tunable transmission line in all mm-wave blocks, the synthesizer achieves state-of-art performance (i.e. phase noise, area, frequency coverage, power) that is maintained across the entire band.



(a) Algorithm Outline; VCO, buffer and divider DiCAD states are swept until the control voltage settles within the 0.2V-0.8V range.



(b) Calibration of testchip 1 locking to 50.112GHz.



(c) Calibration of testchip 2 locking to 44.928GHz.

Figure 5.14: The calibration algorithm used to align the center frequencies of the VCO, buffer and 1<sup>st</sup> stage divider.

## REFERENCES

- [1] J. Mitola, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, no. 5, pp. 26–38, May 1995.
- [2] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, M. Tang, and A. Abidi, "An 800MHz to 5GHz software-defined radio receiver in 90nm CMOS," in *IEEE ISSCC Dig. 2006*, Feb. 2006, pp. 1932–1941.
- [3] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi, "An 800-mhz ndash;6-ghz software-defined wireless receiver in 90-nm cmos," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.
- [4] A. Abidi, "The path to the software-defined radio receiver," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.
- [5] F. Bruccoleri, E. Klumperink, and B. Nauta, "Noise cancelling in wideband CMOS LNAs," in *IEEE ISSCC Dig. 2002*, Feb. 2002, pp. 406–407.
- [6] —, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
- [7] C. Andrews and A. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, <6dB NF, and >27dBm wideband IIP3," in *IEEE ISSCC Dig. 2010*, Feb. 2010, pp. 46–47.
- [8] —, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
- [9] —, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [10] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40nm CMOS highly linear 0.4-to-6GHz receiver resilient to 0dBm out-of-band blockers," in *IEEE ISSCC Dig. 2011*, Feb. 2011, pp. 62–64.
- [11] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, B. Verbruggen, and J. Craninckx, "A 40 nm CMOS 0.4-6GHz receiver resilient to out-of-band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, July 2011.
- [12] Z. Ru, E. Klumperink, G. Wienk, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *IEEE ISSCC Dig. 2009*, Feb. 2009, pp. 230–231,231a.
- [13] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.

- [14] Z. Ru, “Frequency translation techniques for interference-robust software-defined radio receivers,” Ph.D. dissertation, University of Twente, Enschede, November 2009.
- [15] D. Murphy, A. Hafez, A. Mirzaei, M. Mikhemar, H. Darabi, M.-C. Chang, and A. Abidi, “A blocker-tolerant wideband noise-cancelling receiver with a 2dB noise figure,” in *IEEE ISSCC Dig. 2012*, Feb. 2012, pp. 74–75.
- [16] M. Soer, E. Klumperink, Z. Ru, F. van Vliet, and B. Nauta, “A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving >11dBm IIP3 and <6.5 dB NF,” in *IEEE ISSCC Dig. 2009*, Feb. 2009, pp. 222–223,223a.
- [17] L. Franks and I. Sandberg, “An alternative approach to the realizations of network functions: N-path filter,” *Bell Syst. Tech. J.*, pp. 1321–1350, 1960.
- [18] D. von Grunigen, R. Sigg, J. Schmid, G. Moschytz, and H. Melchior, “An integrated CMOS switched-capacitor bandpass filter based on N-path and frequency-sampling principles,” *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 753–761, Dec. 1983.
- [19] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, “A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver,” in *Proc. CICC 2003*, Sept. 2003, pp. 459–462.
- [20] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, “A wideband balun LNA I/Q-mixer combination in 65nm CMOS,” in *IEEE ISSCC Dig. 2008*, Feb. 2008, pp. 326–617.
- [21] —, “The blixer, a wideband balun-LNA-I/Q-mixer topology,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, Dec. 2008.
- [22] S. Zhou and M.-C. Chang, “A cmos passive mixer with low flicker noise for low-power direct-conversion receiver,” *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [23] I.-C. Lu, C.-Y. Yu, Y. horng Chen, L. chou Cho, C.-h. Sun, C.-C. Tang, and G. Chien, “A SAW-less GSM/GPRS/EDGE receiver embedded in a 65nm CMOS SoC,” in *IEEE ISSCC Dig. 2011*, Feb. 2011, pp. 364–366.
- [24] C.-Y. Yu, I. Lu, Y.-H. Chen, L.-C. Cho, C. Sun, C.-C. Tang, H.-H. Chang, W.-C. Lee, S.-J. Huang, T.-H. Wu, C.-S. Chiu, and G. Chien, “A SAW-less GSM/GPRS/EDGE receiver embedded in 65-nm SoC,” *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3047–3060, Dec. 2011.
- [25] A. Mirzaei, A. Yazdi, Z. Zhou, E. Chang, P. Suri, and H. Darabi, “A 65nm CMOS quad-band SAW-less receiver for GSM/GPRS/EDGE,” in *Proc. Symp. VLSI Circuits 2010*, June 2010, pp. 179–180.
- [26] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, “A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.

- [27] B. Nauta, “A CMOS transconductance-C filter technique for very high frequencies,” *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.
- [28] H. Zhang and E. Sandnchez-Sinencio, “Linearization techniques for CMOS low noise amplifiers: A tutorial,” *IEEE Trans. Circuits Syst. I*, vol. 58, no. 1, pp. 22–36, Jan. 2011.
- [29] D. Im, I. Nam, H.-T. Kim, and K. Lee, “A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner,” *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, Mar. 2009.
- [30] J. Weldon, J. Rudell, L. Lin, R. Sekhar Narayanaswami, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray, “A 1.75 GHz highly-integrated narrow-band CMOS transmitter with harmonic-rejection mixers,” in *IEEE ISSCC Dig. 2001*, 2001, pp. 160–161,442.
- [31] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. Gray, “A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers,” *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003–2015, Dec. 2001.
- [32] A. Mirzaei, D. Murphy, and H. Darabi, “Analysis of direct-conversion IQ transmitters with 25% duty-cycle passive mixers,” *IEEE Trans. Circuits Syst. I*, vol. 58, no. 10, pp. 2318–2331, Oct. 2011.
- [33] N. Poobuapheun, W.-H. Chen, Z. Boos, and A. Niknejad, “A 1.5V 0.7-2.5GHz CMOS quadrature demodulator for multiband direct-conversion receivers,” *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1669–1677, Aug. 2007.
- [34] D. Murphy, “Noise in large-signal, time-varying RF CMOS circuits: Theory and design,” Ph.D. dissertation, University of California, Los Angeles, [in press].
- [35] A. Mirzaei, H. Darabi, J. Leete, X. Chen, K. Juan, and A. Yazdi, “Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers,” *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.
- [36] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, “Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers,” *IEEE Trans. Circuits Syst. I*, vol. 57, no. 9, pp. 2353–2366, Sept. 2010.
- [37] A. Mirzaei and H. Darabi, “Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers,” *IEEE Trans. Circuits Syst. I*, vol. 58, no. 5, pp. 879–892, May 2011.
- [38] A. Mirzaei, H. Darabi, and D. Murphy, “Architectural evolution of integrated M-phase high-Q bandpass filters,” *IEEE Trans. Circuits Syst. I*, vol. PP, no. 99, p. 1, 2011.

- [39] A. El Oualkadi, M. El Kaamouchi, J.-M. Paillot, D. Vanhoenacker-Janvier, and D. Flandre, “Fully integrated high-Q switched capacitor bandpass filter with center frequency and bandwidth tuning,” in *Proc. RFIC Conf. 2007*, June 2007, pp. 681–684.
- [40] A. Ghaffari, E. Klumperink, and B. Nauta, “A differential 4-path highly linear widely tunable on-chip band-pass filter,” in *Proc. RFIC Conf. 2010*, May 2010, pp. 299–302.
- [41] A. Ghaffari, E. Klumperink, M. Soer, and B. Nauta, “Tunable high-Q n-path band-pass filters: Modeling and verification,” *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
- [42] D. B. Leeson, “A simple model of feedback oscillator noise spectrum,” *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.
- [43] F. X. Kaertner, “Determination of the correlation spectrum of oscillators with low noise,” *IEEE Trans. Microw. Theory and Tech.*, vol. 37, no. 1, pp. 90–101, Jan. 1989.
- [44] A. Demir, A. Mehrotra, and J. Roychowdhury, “Phase noise in oscillators: a unifying theory and numerical methods for characterization,” *IEEE Trans. Circuits Syst. I, Fundam. Theory Applicat.*, vol. 47, no. 5, pp. 655–674, May 2000.
- [45] A. Demir, “Phase noise and timing jitter in oscillators with colored-noise sources,” *IEEE Trans. Circuits Syst. I, Fundam. Theory Applicat.*, vol. 49, no. 12, pp. 1782–1791, Dec. 2002.
- [46] A. Hajimiri and T. H. Lee, “A general theory of phase noise in electrical oscillators,” *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [47] ———, “Corrections to “a general theory of phase noise in electrical oscillators”,” *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 928–928, Jun. 1998.
- [48] C. Samori, A. L. Lacaita, F. Villa, and F. Zappa, “Spectrum folding and phase noise in LC tuned oscillators,” *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Process*, vol. 45, no. 7, pp. 781–790, Jul. 1998.
- [49] Q. Huang, “Phase noise to carrier ratio in LC oscillators,” *IEEE Trans. Circuits Syst. I, Fundam. Theory Applicat.*, vol. 47, no. 7, pp. 965–980, Jul. 2000.
- [50] J. J. Rael and A. A. Abidi, “Physical processes of phase noise in differential LC oscillators,” *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 569–572, 2000.
- [51] P. Andreani, X. Wang, L. Vandi, and A. Fard, “A study of phase noise in Colpitts and LC-tank CMOS oscillators,” *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [52] P. Andreani and A. Fard, “More on the  $1/f^2$  phase noise performance of CMOS differential-pair LC-tank oscillators,” *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.

- [53] A. Fard and P. Andreani, “An analysis of  $1/f^2$  phase noise in bipolar Colpitts oscillators (with a digression on bipolar differential-pair LC oscillators),” *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 374–384, Feb. 2007.
- [54] P. Andreani and A. Fard, “A 2.3GHz LC-tank CMOS VCO with optimal phase noise performance,” *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, pp. 691–700, Feb. 6-9, 2006.
- [55] J. Bank, “A harmonic-oscillator design methodology based on describing functions,” Ph.D. dissertation, Chalmers University of Technology, Sweden, 2006.
- [56] A. Mazzanti and P. Andreani, “Class-C harmonic CMOS VCOs, with a general result on phase noise,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- [57] K. A. Kouznetsov and R. G. Meyer, “Phase noise in LC oscillators,” *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1244–1248, Aug. 2000.
- [58] E. Hegazi, J. J. Rael, and A. A. Abidi, *The Designer’s Guide to High-Purity Oscillators*. Springer, 2004.
- [59] J. Phillips and K. Kundert, “Noise in mixers, oscillators, samplers, and logic an introduction to cyclostationary noise,” *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 431–438, 2000.
- [60] J. Rael, “Phase noise in LC oscillators,” Ph.D. dissertation, University of California, Los Angeles, 2007.
- [61] E. Hegazi and A. A. Abidi, “Varactor characteristics, oscillator tuning curves, and AM-FM conversion,” *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.
- [62] W. P. Robins, *Phase Noise in Signal Sources: Theory and Applications*. Institution of Electrical Engineers, 1984.
- [63] H. Darabi and A. A. Abidi, “Noise in RF-CMOS mixers: a simple physical model,” *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.
- [64] E. Hegazi, H. Sjoland, and A. A. Abidi, “A filtering technique to lower LC oscillator phase noise,” *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
- [65] H. Wang, “A solution for minimizing phase noise in low-power resonator-based oscillators,” *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. 3, pp. 53–56, 2000.
- [66] A. Mazzanti and P. Andreani, “A 1.4mW 4.90-to-5.65GHz class-C CMOS VCO with an average FoM of 194.5dBc/Hz,” *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, pp. 474–629, Feb 2008.



- [67] S. Shekhar, J. Walling, S. Aniruddhan, and D. Allstot, "CMOS VCO and LNA using tuned-input tuned-output circuits," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1177–1186, May 2008.
- [68] B. Soltanian and P. Kinget, "Tail current-shaping to improve phase noise in LC voltage-controlled oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1792–1802, Aug. 2006.
- [69] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press; 2nd edition, 2003.
- [70] A. Rofougaran, G. Chang, J. Rael, J.-C. Chang, M. Rofougaran, P. Chang, M. Djafari, M.-K. Ku, E. Roth, A. Abidi, and H. Samueli, "a single-chip 900-MHz spread-spectrum wireless transceiver in 1- $\mu$ m CMOS. I. Architecture and transmitter design," *IEEE J. of Solid-State Circuits*, vol. 33, no. 4, pp. 515–530, 1998.
- [71] D. Murphy, M. P. Kennedy, J. Buckley, and M. Qu, "The optimum power conversion efficiency and associated gain of an LC CMOS oscillator," *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 2633–2636, 21-24 May 2006.
- [72] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multi-phase LC CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.
- [73] B. Razavi, "Gadgets gab at 60 GHz," *IEEE Spectrum*, vol. 45, no. 2, pp. 46–58, Feb. 2008.
- [74] D. Murphy, Q. Gu, Y.-C. Wu, H.-Y. Jian, Z. Xu, A. Tang, F. Wang, Y.-L. Lin, H.-H. Chen, C. Jou, and M.-C. Chang, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15.3c TRX," in *Proc. ESSCIRC Conf. 2010*, Sept. 2010, pp. 258–261.
- [75] H. Hoshino, R. Tachibana, T. Mitomo, N. Ono, Y. Yoshihara, and R. Fujimoto, "A 60-GHz phase-locked loop with inductor-less prescaler in 90-nm CMOS," in *Proc. ESSCIRC Conf. 2007*, Sept. 2007, pp. 472–475.
- [76] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66GHz quadrature pll in 45nm digital CMOS," in *IEEE ISSCC Dig. 2009*, Feb. 2009, pp. 494–495,495a.
- [77] O. Richard, A. Siligaris, F. Badets, C. Dehos, C. Dufis, P. Busson, P. Vincent, D. Belot, and P. Urard, "A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for wireless HD applications," in *IEEE ISSCC Dig. 2010*, Feb. 2010, pp. 252–253.
- [78] E. Hegazi, H. Sjoland, and A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
- [79] K. Hoshino, E. Hegazi, J. Rael, and A. Abidi, "A 1.5v, 1.7mA 700 MHz CMOS LC oscillator with no upconverted flicker noise," in *Proc. ESSCIRC Conf. 2001*, Sept. 2001, pp. 337–340.

- [80] E. Hegazi and A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, June 2003.
- [81] A. Kral, F. Behbahani, and A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proc. CICC 1998*, May 1998, pp. 555–558.
- [82] T. LaRocca, J. Liu, F. Wang, and F. Chang, "Embedded DiCAD linear phase shifter for 57-65GHz reconfigurable direct frequency modulation in 90nm CMOS," in *Proc. RFIC Conf. 2009*, June 2009, pp. 219–222.
- [83] T. LaRocca, J. Liu, F. Wang, D. Murphy, and F. Chang, "CMOS digital controlled oscillator with embedded DiCAD resonator for 58-64GHz linear frequency tuning and low phase noise," in *Proc. Microwave Symp. (MTT-S) 2009*, June 2009, pp. 685–688.
- [84] J.-C. Chien and L.-H. Lu, "Design of wide-tuning-range millimeter-wave CMOS VCO with a standing-wave architecture," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1942–1952, Sept. 2007.
- [85] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology: 60 GHz and Beyond*. Springer, 2008.
- [86] D. Murphy, J. Rael, and A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 6, pp. 1187–1203, June 2010.
- [87] H. Sjoland, "Improved switched tuning of differential CMOS VCOs," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Process*, vol. 49, no. 5, pp. 352–355, May 2002.
- [88] M. Nariman, R. Rofougaran, and F. De Flaviis, "A switched-capacitor mm-wave VCO in 65 nm digital CMOS," in *Proc. RFIC Conf.*, May 2010, pp. 157–160.
- [89] M. Tiebout, "A cmos direct injection-locked oscillator topology as high-frequency low-power frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1170–1174, July 2004.
- [90] Y.-S. Lin, T.-H. Chang, C.-Z. Chen, C.-C. Chen, H.-Y. Yang, and S. Wong, "Low-power 48-GHz CMOS VCO and 60-GHz CMOS LNA for 60-GHz dual-conversion receiver," in *Proc. VLSI-DAT 2009*, April 2009, pp. 88–91.
- [91] L. Li, P. Reynaert, and M. Steyaert, "Design and analysis of a 90 nm mm-wave oscillator using inductive-division LC tank," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1950–1958, July 2009.
- [92] C. Marcu, D. Chowdhury, C. Thakkar, L.-K. Kong, M. Tabesh, J.-D. Park, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, A. Niknejad, and E. Alon, "A 90nm CMOS low-power 60GHz transceiver with integrated baseband circuitry," in *IEEE ISSCC Dig. 2009*, Feb. 2009, pp. 314–315,315a.

- [93] A. Tang, F. Hsiao, D. Murphy, I.-N. Ku, J. Liu, S. D'Souza, N.-Y. Wang, H. Wu, Y.-H. Wang, M. Tang, G. Virbila, M. Pham, D. Yang, Q. Gu, Y.-C. Wu, Y.-C. Kuan, C. Chien, and M. Chang, "A low-overhead self-healing embedded system for ensuring high yield and long-term sustainability of 60ghz 4Gb/s radio-on-a-chip," in *IEEE ISSCC Dig. 2009*, Feb. 2012, pp. 316–318.
- [94] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.
- [95] K.-H. Tsai, J.-H. Wu, and S.-I. Liu, "A digitally calibrated 64.3-66.2GHz phase-locked loop," in *Proc. RFIC Conf. 2008*, April 2008, pp. 307–310.