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Development of a Parallel-FET Linearization Technique for High Efficiency GaN Power Amplifiers

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***Abstract*—We demonstrate the design of a linear and high efficient power amplifier (PA) by using different gate bias voltages for parallelly combined Gallium Nitride (GaN) high electron mobility transistors (HEMTs). The experimental results show that the linearized PA achieves the gain flatness of 0.3 dB over a 40 dB power range and has a measured sharp output power at 1 dB compression point (P_{1dB}) of 38 dBm, less than 2 dB below the saturated power (P_{SAT}). The measured adjacent channel power ratio (ACPR) of the proposed linearized PA shows up to 8 dB improvements over the PA biased ~ class A (47% I_{dss})**

***Index Terms*—Linearity, AM/AM, AM/PM, high efficiency, power amplifiers (PAs).**

I. Introduction

GaN devices provide high power density and efficiency and are a very attractive technology. On the other hand, GaN devices suffer from soft compression, AM/AM, and AM/PM distortions [1]. Due to soft compression, GaN PAs have P_{1dB} way below P_{SAT} and the efficiency for linear power is not competitive. Several attempts have been reported on the linearization of GaN transistors from device to circuit levels [2-5]. The designs presented in [2] and [3] show linearization for only AM/AM by tuning the bias points of the driver and output stages. In [2], the tuning was performed after fabrication to improve AM/AM distortions. Also, the output stage in [2] was biased in class A which results in lower total efficiency. In [4], the device size ratio of the driver and main amplifier is 1:7.5 which imposes realization difficulty. In [5], a balanced high-power Doherty amplifier was linearized by optimum adjustment of the peaking compensation line, shunt capacitors, and gate biases. This technique shows good results if the Doherty configuration is adopted for the design.

In this paper, we present the development of a novel linearization technique for GaN PAs to reduce soft compression and to improve efficiency at a higher linear power. We have developed a parallel pair of transistors with different gate bias voltages to reduce both AM/AM and AM/PM distortions. Using our linear pair of transistors, we have designed and implemented a balanced power amplifier from 2.8 to 3.2 GHz to demonstrate the linearity improvement. The experimental results demonstrate that our linearized PA has the lowest ACPR compared to class A all the way to class B and 10% better efficiency than that of class A. In addition, the soft compression is significantly reduced with a sharp P_{1dB} of 38 dBm less than 2 dB only below P_{SAT}.

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II. GaN Device Nonlinearity and Linearization Scheme

Fig. 1 shows the simulated AM/AM and AM/PM behavior of a GaN transistor with a part number TGF-2023-2-01 from Qorvo [7]. The GaN HEMT on a SiC substrate has a gate length of 0.25 µm and a total gate width of 1.25 mm. Simulated AM/AM and AM/PM curves are plotted at 3 GHz and V_{DS} = 28 V drain bias voltage with different quiescent current (I_q) values expressed in percentage of saturation current (I_{dss}). The simulations were carried out using NI AWR software with a transistor nonlinear Angelov based model from Modelithics [8].

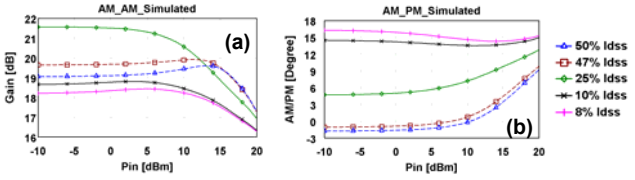

Fig. 1 a) Simulated AM/AM and b) Simulated AM/PM of the GaN transistor at 3 GHz and V_{DS} = 28 V.

Gain and phase plots deliver some important remarks. Firstly, gain curves suffer from soft compression and expansion beyond class A to class B. The AM/AM distortion starts from 15 dB to 10 dB PBO from P_{1dB}. Secondly, the AM/AM and AM/PM distortions vary for different classes of operation from classes A, AB to B. From class A to B, AM/AM changes from expansion to compression, and AM/PM moves from a positive to negative slope.

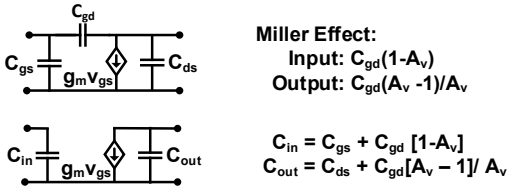

Fig. 2. Transistor equivalent circuit and Miller effect

AM/AM and AM/PM are interrelated. In the case of gain compression, there is an associated positive phase shift in AM/PM whereas with gain expansion, there is a negative phase shift in AM/PM. These behaviors are related to the Miller effect of gate-drain capacitance (C_{gd}). C_{gd} can be resolved into 2 capacitors at the gate and the drain, respectively. C_{gd} is reflected at the gate to be $C_{gd}(1-A_v)$, where A_v is the voltage gain of the transistor. Total capacitance at the input is given by: $C_{in} = C_{gs}+$

C_{gd} (1-A_v). As gain expands or A_v rises, C_{in} increases and causes a negative phase shift. On the other hand, when gain is compressed, C_{in} decreases and causes a positive phase shift (Fig. 2).

Fig. 3.a shows our proposed linearized pair of transistors at two different gate voltages to increase output power and to reduce AM/AM and AM/PM distortions. Fig. 3.b shows conventionally combined transistors at the same gate bias. When the combined GaN HEMTs are biased at different gate voltages, the gain expansion of one device is cancelled by gain compression of the other device. The combined linearized GaN HEMTs result in flatter gain and overcome the soft compression problem. Similarly, the AM/PM positive slope of a GaN HEMT is compensated by the negative slope of the other GaN HEMT. Linearity improvements are achieved when the AM/AM and AM/PM distortions are reduced.

From Fig. 1a, we can choose transistor M1 biased at I_{dss} = 47% (brown dashed line) and transistor M2 biased at I_{dss} = 10% (black solid line). Gain expansion of the brown dashed line will be compensated with gain compression of the black solid line. Similarly, AM/PM positive slope of the brown dashed line will be compensated with the negative slope of the black solid line (Fig. 1b). Therefore, the combined transistors M1 and M2 will have minimal AM/AM and AM/PM distortions and much better linearity.

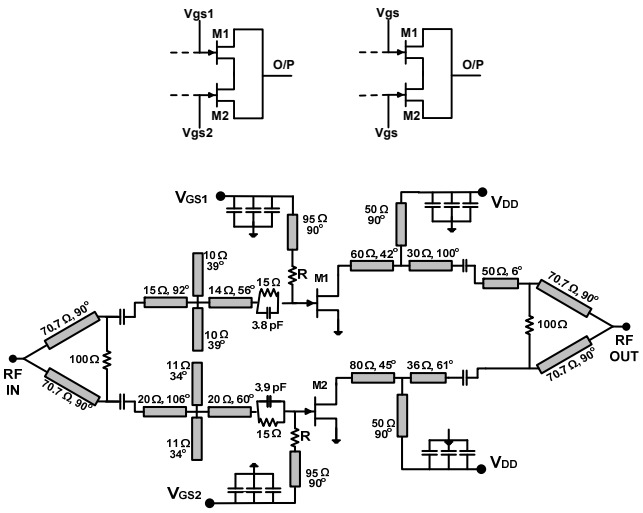

Fig. 3. Gate biasing a) Proposed and b) conventional, and c) Proposed GaN power amplifier with an AM/AM and AM/PM linearization scheme

III. HIGH EFFICIENT AND LINEARIZED POWER AMPLIFIER

Fig. 3c demonstrates the schematic diagram of the proposed linearized power amplifier. AM/AM and AM/PM distortion compensation is achieved by proper selections of gate bias voltages of transistors M1 and M2. Since transistors M1 and M2 have different phases (Fig. 1b) and matching networks are different, a delay line is added to one of the branches for phase compensation and to ensure maximum power combining. A Wilkinson power divider and a combiner are used at input and output for equal power splitting and combining, respectively and for isolation between branches. Drain and gate biases are achieved using quarter wave transformers (λ_o/4) and a gate bias resistor is added for stability purposes. DC blocking capacitors are used at input and output matching circuits before the Wilkinson divider and combiner in order to isolate gate bias voltages and to prevent any current flow through the Wilkinson resistors. Each GaN HEMT is matched to 50 ohm, therefore the Wilkinson resistor R_w is of 100 ohm value. Simulated power dissipated in the Wilkinson resistor is about 0.15 Watt resulting in less than 2% PAE drop.

A single stage PA is fabricated on 10 mil RT/Duroid 5880 using Qorvo GaN HEMTs with a part number of TGF2023-2-01. Fig. 4 shows a picture of the fabricated circuit. Wire bonding is used to connect gate and drain pads of the GaN HEMTs to traces on the printed circuit board (PCB). Several bypass capacitors of different values (10 pf, 100 pF, 0.1 μF and 10 μF) are connected at gate and drain DC bias pads.

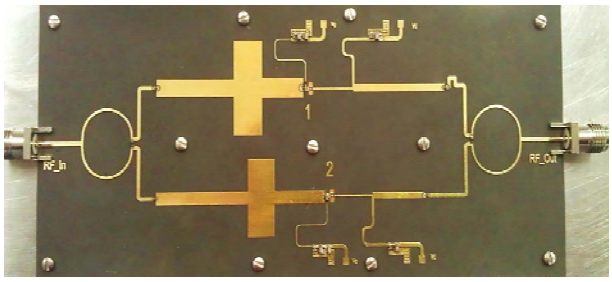

Fig.4. Fabricated circuit prototype

Table 1 shows the gate biases for our linearized power amplifier indicated by PA-Linearized. We have also designed and measured two conventional PAs for comparison. In PA-V_{g1}, both gates are biased at I_q = 47% I_{dss} and in PA-V_{g2}, both gates are biased at I_q=10% I_{dss}.

TABLE I
LIST OF POWER AMPLIFIERS AND GATE BIASSES

Power Amplifier	Gate bias
1. PA-linearized	V_{g1} (M1) at 47 % I_{dss} & V_{g2} (M2) at 10 % I_{dss}
2. PA-V_{g1}	Both Iq (M1&M2) = 47 % I_{dss}
3. PA-V_{g2}	Both Iq (M1&M2) = 10 % I_{dss}

IV. MEASUREMENTS

All measurements were carried out using a Keysight network analyzer PNA-X N5247A, a Keysight signal analyzer PXA-N9030, and a Keysight signal generator E4437B. Fig. 5a shows the measured small signal S-parameters of the linearized-PA. The measured small signal gain is ~20dB and input and output return losses are less than 10 dB from 2.6 GHz to 3.2 GHz. Fig. 5b shows P_{in}-P_{out} measurements at 2.8, 3, and 3.2 GHz and P_{1dB} is more than 38 dBm.

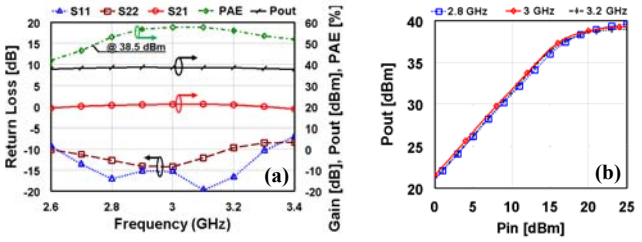

Fig. 5. a) Measured S-parameters, Pout, and PAE @ Pout=38.5 dBm, b) Measured P_{in}-P_{out} of the PA-linearized at V_{DS} = 28 V

Fig. 6 shows AM/AM measurement results. The proposed PA has achieved ~ 0.3 dB gain fluctuations over a 35 dB output power range and gain starts to compress at 3 dB PBO. When the PA is biased with V_{g1} or V_{g2} for both transistors M1 and M2, gain fluctuate ons are more than 0.6 dB and gain starts to compress and expand at > 10 dB PBO. The advantage of the proposed PA is best seen at higher power levels. Our experimental results show that PA-Linearized gain is almost flat at output power levels higher than 25 dBm, while the PA-V_{g1} and PA-V_{g2} have gain fluctuations more than 0.5 dB.

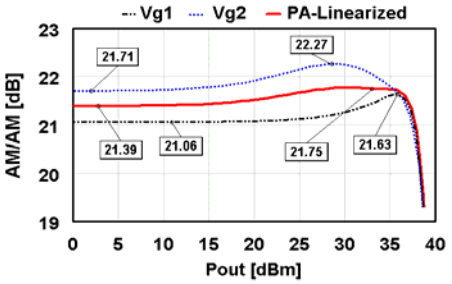

Fig. 6. Measured AM/AM of the PA's: PA-Vg1 (dashed black), PA-Vg2 (dotted blue), and PA-linearized (red solid), f = 3 GHz and V_{DS} = 28 V.

AM-PM measurements (Fig. 7) show phase distortion enhancements by more than 1 degree for the PA-Linearized when compared with PA-V_{g1} and PA-V_{g2}. Fig. 9 shows that PA-Linearized has 10% higher PAE than that of PA-V_{g1}, which is biased close to class-A (Iq = 47% I_{dss}). Likewise, PA-V_{g2} has higher PAE than that of PA-Linearized because it is biased close to class-B (Iq = 10 % I_{dss}).

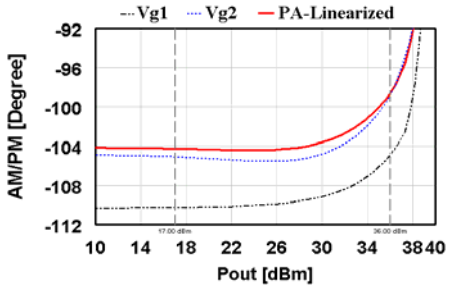

Fig. 7. Measured AM/PM of the PA's: PA-Vg1 (dashed black), PA-Vg2 (dotted blue), and PA-linearized, f = 3 GHz and V_{DS} = 28 V.

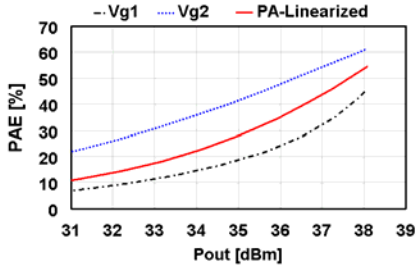

Fig. 8. Measured PAE of PA's: PA-Vg1 (~class A) (dashed black), PA-Vg2 (dotted blue), and PA-linearized (red solid), f = 3 GHz , V_{DS} = 28 V.

ACPR measurements were carried out using digitally modulated waveform (QAM 64) of 20 MHz bandwidth, a raised cosine filter of roll off factor 0.35, and 25 MHz adjacent channel offset (center-to-center). Measurements show that the ACPR of PA-Linearized is enhanced by 5 to 8 dB when compared to the ACPR of PA-V_{g1} (~ class-A) and PA-V_{g2}. Also, the ACPR of PA-V_{g1} and PA-V_{g2} are close to each other. As can be seen from Fig. 1, the AM/AM and AM/PM of the single device has significant distortions from class A all the way to class B. Hence, the cumulative effects of the distortion have resulted in worse ACPR for PA-V_{g1} and PA-V_{g2} as compared to our PA-Linearized.

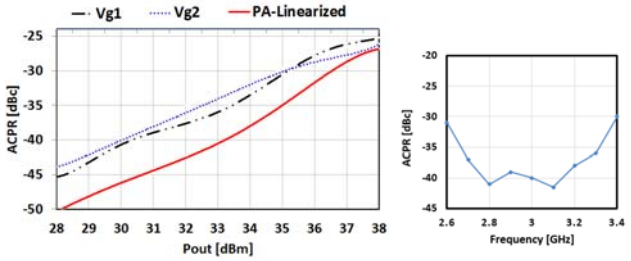

Fig. 9. a) Measured ACPR of PA's: PA-Vg1 (dashed black), PA-Vg2 (dotted blue), and PA-linearized (red solid) at 3 GHz and V_{DS} = 28 V, b) Measured ACPR vs. Frequency at Pout = 36 dBm, and 33 dBm

TABLE II
PERFORMANCE COMPARISON OF REPORTED CIRCUIT LEVEL LINEARIZED PAS

Ref	Freq [GHz]	Tech.	Psat [dBm]	PAE [%]	Gain [dB]	Gain Fluctuation [dB]
[1]	32.5	GaN	37.7	N.A.	15	2
[3]	0.8	GaN	46	70	N.A.	N.A.
[5]	2.14	LDMOS	50	26.9	N.A.	N.A.
This Work	3	GaN	38.5	56	20	0.3

V. CONCLUSION

We demonstrate the design of a linear GaN PA with high efficiency using parallel combined transistors at different gate bias voltages at 3 GHz. The experimental results demonstrate that the proposed PA has the lowest ACPR compared to Class-A with more than 10% higher PAE and significantly reduced the soft compression while maintaining high efficiency. We achieve a record flat gain of 0.3 dB fluctuations over a 35 dB output power range.

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