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Comparative Performance Analysis of Regulated Hybrid Switched-Capacitor Topologies for Direct 48 V to Point-of-Load Conversion

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ABSTRACT Hybrid switched-capacitor (SC) converters have received increased attention for point-of-load (PoL) applications because they can effectively leverage the superior energy density of capacitors and the improved figures-of-merit of low-voltage switching devices. This article introduces an analytical framework for characterizing and comparing regulated hybrid SC topologies for direct 48-V-to-PoL conversion. In the proposed framework, a regulated hybrid SC topology is generally represented as a fixed-ratio SC stage merged with a subsequent regulated buck-type stage, with the total conversion ratio allocated between them. Three metrics are used for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. This framework reveals that increasing the SC stage conversion ratio reduces switch stress and passive component volume while accelerating the falling slew rate of the total inductor current, thereby improving efficiency, power density, and load step-down transient performance concurrently. Although a larger SC step-down ratio typically decreases the rising slew rate of the total inductor current, potentially impairing the load step-up transient performance, proper designs can achieve balanced load step-up and step-down transient performances.

INDEX TERMS Comparative analysis, high conversion ratio, hybrid switched-capacitor (SC) converter, point-of-load (PoL), voltage regulation module (VRM).

I. Introduction

HYBRID switched-capacitor (SC) converters have attracted increased attention for 48-V step-down conversion in data center [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35] and automotive [36], [37] applications, due to their potential to provide improved solutions with higher efficiency and power density compared to conventional designs. As an emerging class of power converters, hybrid SC converters can leverage the greatly superior energy density of capacitors compared to inductors [38], while simultaneously benefiting from the improved figures-of-merit (FOM) of low-voltage switching devices over high-voltage counterparts [39]. For unregulated, fixed-ratio voltage step-down applications (e.g., 48-V-to-12-V intermediate bus converters), various resonant switched-capacitor (ReSC) [29], [30], [31], [32], [33] and multi-resonant switched-capacitor (MRSC) [34], [35] converters operating at or above resonance have been proposed, demonstrating their advantages over existing dc-dc solutions, such as multi-phase buck converters [40] and LLC converters [41]. Previous studies [42], [43], [44], [45] have shown how to analyze and compare different ReSC topologies and strategi-

cally size the passive components in each topology to achieve optimal performance. Additionally, multiple regulated hybrid SC topologies [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28] have been proposed for direct 48 V to point-of-load (PoL) conversion, particularly for 48-V voltage regulation modules (VRMs), where output voltage regulation is typically required. However, there is a lack of a method to theoretically compare the performance of regulated hybrid SC topologies, which could be useful for informing topology selection and converter design.

To fill this gap, this work aims to establish an analytical framework for the topological characterization and performance comparison of regulated hybrid SC topologies in direct 48-V-to-PoL applications. In the proposed framework, each topology is captured with topology-dependent characteristic vectors, which are then utilized to calculate three metrics for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. Building on our previous conference paper [46], this article provides an additional comparative analysis of transient performance, as well as in-depth discussions on the comparison results. Based on this analytical framework, a comprehensive comparative analysis reveals that increasing the SC stage conversion ratio can reduce switch stress and passive component volume while speeding up the falling slew rate of the total inductor current, thereby improving efficiency, power density, and load step-down transient performance at the same time. Although a larger SC conversion ratio typically slows down the rising slew rate of the total inductor current, potentially impairing the load step-up transient performance, a converter with a larger SC conversion ratio can be properly designed to achieve balanced load step-up and step-down transient performances.

The remainder of this paper is organized as follows: Section II provides a general representation of regulated hybrid SC topologies consisting of a fixed-ratio SC stage merged with a subsequent regulated buck-type stage. Section III introduces the analytical framework with the three metrics for performance comparison, including a formalized analysis procedure using topology-dependent characteristic vectors. Based on the proposed framework, Section IV conducts a comparative analysis of the state-of-the-art 48-V-to-PoL regulated hybrid SC topologies and demonstrates the benefits of a larger SC stage conversion ratio. Finally, Section V concludes this article.

II. General Representation of Regulated Hybrid SC Topologies

A regulated hybrid SC topology can be captured by the general representation depicted in Fig. 1. It consists of two stages: 1) a fixed-ratio SC stage for efficient and compact voltage conversion and 2) a regulated buck-type stage for the remainder of the voltage conversion task and output voltage regulation. Moreover, when designed properly, the buck-type stage serves as an inductive load to the preceding SC stage, ensuring complete soft-charging operation [47]. It should be noted that a distinctive feature of high-performance hybrid SC topologies is that the two stages are not independent; instead, their operations are merged to achieve improved performance [48]. Additionally, although the buck-type stage can regulate the output voltage with duty cycle control and achieve multi-phase interleaving similar to a buck converter, it does not necessarily require dedicated pull-up switches due to its strategic merging with the preceding SC stage.

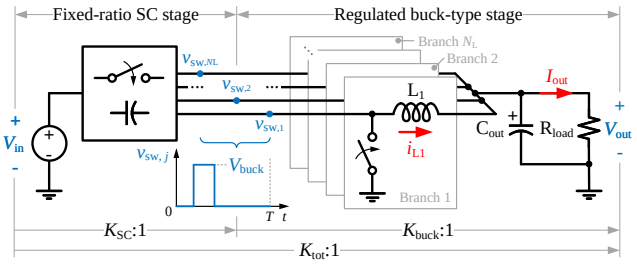


FIGURE 1. General representation of a regulated hybrid SC topology consisting of a fixed-ratio SC stage and a regulated buck-type stage. The input voltage (V_{in}) is first stepped down to V_{buck} by the SC stage. The buck-type stage then performs the remaining voltage conversion from V_{buck} to the output voltage (V_{out}) with regulation. The total conversion ratio K_{tot} : 1 is allocated between the SC stage and the buck-type stage.

As is consistent with all previously cited works, this analysis considers only topologies where all switch-node voltages in Fig. 1 ($v_{sw,1}$, $v_{sw,2}$, $\cdots$, $v_{sw,NL}$, where N_L denotes the total number of inductors) switch between the same two voltage levels: V_{buck} and 0. V_{buck} is the highest voltage that the buck-type stage experiences (ignoring flying capacitor voltage ripples), thereby defined as the voltage stress on the buck-type stage. The input voltage (V_{in}) is first stepped down to V_{buck} by the SC stage, where V_{buck} can be calculated as

$$V_{buck} = \frac{V_{in}}{K_{SC}}, \tag{1}$$

and K_{SC} is the SC stage conversion ratio, also interchangeably referred to as the SC step-down ratio. The buck-type stage then performs the remaining voltage conversion from V_{buck} to the output voltage (V_{out}) with regulation. Fig. 2 illustrates a four-branch series-capacitor buck (SCB) converter as an example of the general representation depicted in Fig. 1, where $V_{in} = 48$ V and $V_{out} = 1$ V. The high-side switches (S_{1H-4H}) and flying capacitors ($C_{fly1-fly3}$) constitute the SC stage with a step-down ratio of 4:1 ($K_{SC} = 4$). According to (1), the voltage stress on the buck-type stage can be obtained as $V_{buck} = 12$ V. The buck-type stage, consisting of the low-side switches (S_{1L-4L}) and inductors (L_{1-4}), completes the remaining 12-V-to-1-V voltage conversion ($K_{buck} = 12$) with regulation.

Since the total conversion ratio (K_{tot}), defined as $K_{tot} = V_{in}/V_{out}$, is allocated between the SC stage and the buck-

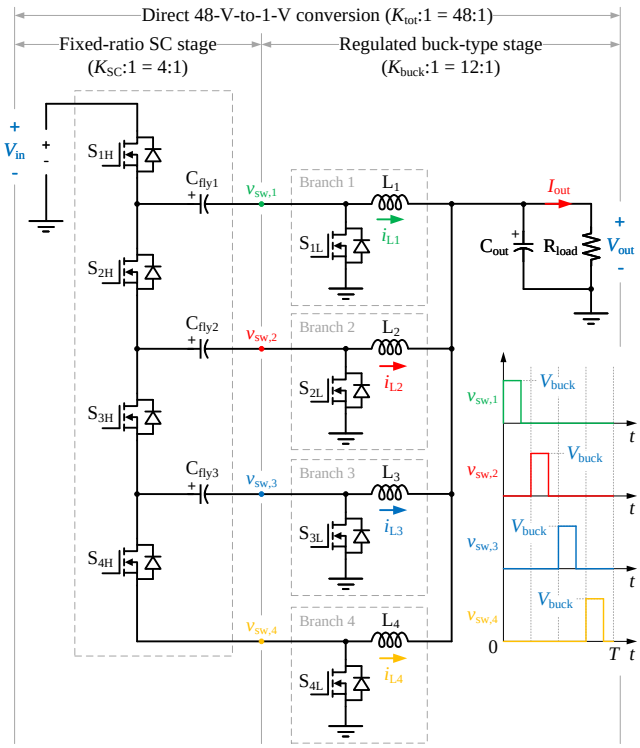


FIGURE 2. Four-branch SCB converter for direct 48-V-to-1-V conversion as an example of the general representation depicted in Fig. 1. The high-side switches (S_{1H-4H}) and flying capacitors ($C_{fly1-fly3}$) constitute the $4:1$ SC stage; the low-side switches (S_{1L-4L}) and inductors (L_{1-4}) form the buck-type stage which performs the remaining 12-V-to-1-V voltage conversion with regulation. In this example, the voltage stress on the buck-type stage is $V_{buck} = 12$ V.

type stage, if the SC stage achieves a larger step-down ratio (K_{SC}), the voltage conversion burden on the buck-type stage (K_{buck}) can be reduced. At the same output voltage, buck converters with lower step-down ratios typically require smaller inductors and achieve higher efficiency. Given that magnetic components typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden so that the inductor volume of the buck-type stage can be reduced.

Although it is clear that a larger SC stage conversion ratio (K_{SC}) benefits the buck-type stage, there is still a concern that increasing K_{SC} can impair overall efficiency. This is because achieving a larger SC step-down ratio generally requires more switching devices, which can lead to higher conduction and switching losses. Moreover, higher-order SC networks typically require more flying capacitors, potentially offsetting the inductor volume reduction seen in the buck-type stage. These concerns are addressed in the following sections.

III. Analytical Framework for Topological Characterization and Performance Comparison

The proposed analytical framework focuses on three metrics for performance comparison: a) normalized switch stress (M_S) as an indicator of efficiency, b) normalized passive component volume (M_P) as an indicator of power density, and c) normalized falling and rising slew rates ($\widehat{SR}_F$ and $\widehat{SR}_R$) of the total inductor current as indicators of transient performance. In the proposed framework, all three metrics are normalized and independent of output power and current levels, ensuring fair comparisons across different topologies. This section first discusses the key assumptions of the proposed framework, then provides the definitions and derivations of the three metrics, and finally introduces a formalized analytical procedure using topology-dependent characteristic vectors.

A. Key Assumptions

The proposed analytical framework is based on the following assumptions:

- *Small-ripple approximation:* It is selectively assumed that the magnitude of the switching ripple is much smaller than the dc component of capacitor voltages and inductor currents, which enables three subsequent assumptions:
  - In the analysis of normalized switch stress, inductor current ripples and capacitor voltage ripples are assumed to be negligible.
  - In the analysis of normalized passive component volume (where ripple cannot meaningfully be ignored), inductor current ripples and capacitor voltage ripples are assumed to be piecewise linear. In other words, capacitor voltage ripples are assumed to be negligible in inductor volume analysis, and inductor current ripples are assumed to be negligible in capacitor volume analysis.
  - In the analysis of normalized total inductor current slew rate, all capacitor voltage ripples (including the output voltage ripple) are again assumed to be negligible.
- *Uniform ripple ratios:* Ripple ratios of all inductor currents (α_I) are assumed to be the same. Ripple ratios of all capacitor voltages (α_V) are assumed to be the same.
- *Lossless energy transfer:* Duty ratio is calculated based on the assumption that the converter is lossless with no requirement for output voltage droop compensation.
- *Uniform energy density:* All inductors are assumed to have the same volumetric energy density ($\rho_{E,L}$). All capacitors are assumed to have the same volumetric energy density ($\rho_{E,C}$).

The symbols used in this framework are defined in Table 1. Later symbols with the hat notation ($\hat{\cdot}$) are normalized values with respect to their base values listed in Table 2.

TABLE 1. Symbol definitions

Symbol	Definition
N_{S}	Total number of switching devices
N_{L}	Total number of inductors
N_{C}	Total number of flying capacitors
V_{in}	Input voltage (base value for voltage)
V_{buck}	Buck-type stage input voltage (illustrated in Fig. 1)
V_{out}	Output voltage
I_{out}	Total output current (base value for current)
K_{tot}	Total conversion ratio ($K_{\mathrm{tot}} = V_{\mathrm{in}}/V_{\mathrm{out}}$)
K_{SC}	SC stage conversion ratio ($K_{\mathrm{SC}} = V_{\mathrm{in}}/V_{\mathrm{buck}}$)
K_{buck}	Buck-type stage conversion ratio ($K_{\mathrm{buck}} = V_{\mathrm{buck}}/V_{\mathrm{out}}$)
$V_{\mathrm{ds},i}$	Peak blocking voltage across switch i
$I_{\mathrm{d(rms)},i}$	RMS value of the current through switch i
$\mathrm{Vol}_{\mathrm{tot}}$	Total passive component volume
$\mathrm{Vol}_{\mathrm{L},j}$	Volume of inductor j
$\mathrm{Vol}_{\mathrm{C},k}$	Volume of capacitor k
L_j	Value of inductor j
$I_{\mathrm{L},j}$	Average current of inductor j
$\Delta i_{\mathrm{L},j,\mathrm{pp}}$	Peak-to-peak current ripple of inductor j
T	Switching period of the buck-type stage
D	Duty ratio of the buck-type stage
$D_{\max}$	Maximum duty ratio of the buck-type stage
$E_{\mathrm{L},j,\mathrm{peak}}$	Peak energy stored in inductor j
C_k	Value of capacitor k
$V_{\mathrm{C},k}$	Mid-range voltage of capacitor k
$\Delta v_{\mathrm{C},k,\mathrm{pp}}$	Peak-to-peak voltage ripple of capacitor k
$q_{\mathrm{C},k}$	Accumulative charge flowing into capacitor k between the peak and valley of capacitor k's voltage waveform
$E_{\mathrm{C},k,\mathrm{peak}}$	Peak energy stored in capacitor k
α_{I}	Inductor current ripple ratio ($\alpha_{\mathrm{I}} = \Delta i_{\mathrm{L},j,\mathrm{ap}}/I_{\mathrm{L},j}$)
α_{V}	Capacitor voltage ripple ratio ($\alpha_{\mathrm{V}} = \Delta v_{\mathrm{C},k,\mathrm{ap}}/V_{\mathrm{C},k}$)
$\rho_{\mathrm{E,L}}$	Volumetric energy density of inductors
$\rho_{\mathrm{E,C}}$	Volumetric energy density of capacitors
β	Volumetric energy density ratio of capacitors to inductors ($\beta = \rho_{\mathrm{E,C}}/\rho_{\mathrm{E,L}}$)
$\mathrm{SR}_{\mathrm{F},j}$	Maximum current falling slew rate of inductor j
SR_{F}	Maximum total inductor current falling slew rate
$\mathrm{SR}_{\mathrm{R},j}$	Maximum current rising slew rate of inductor j
SR_{R}	Maximum total inductor current rising slew rate

TABLE 2. Base values for normalization

Quantity	Voltage	Current	Charge	Volume	Current Slew Rate
Base value	V_{in}	I_{out}	$I_{\mathrm{out}}T$	$\frac{V_{\mathrm{out}}I_{\mathrm{out}}T}{\rho_{\mathrm{E,L}}}$	$\frac{2\alpha_{\mathrm{I}}I_{\mathrm{out}}}{T}$

B. Normalized Switch Stress

The normalized switch stress (M_{S}) is defined as the total switch stress normalized to the output power

$$M_{\mathrm{S}} = \frac{\sum\limits_{\text{switches}} V_{\mathrm{ds},i} I_{\mathrm{d(rms)},i}}{V_{\mathrm{out}} I_{\mathrm{out}}} = \underbrace{\frac{V_{\mathrm{in}}}{V_{\mathrm{out}}}}_{K_{\mathrm{tot}}} \cdot \sum_{i=1}^{N_{\mathrm{S}}} \underbrace{\frac{V_{\mathrm{ds},i}}{V_{\mathrm{in}}}}_{\widehat{V}_{\mathrm{ds},i}} \cdot \underbrace{\frac{I_{\mathrm{d(rms)},i}}{I_{\mathrm{out}}}}_{\widehat{I}_{\mathrm{d(rms)},i}}$$

$$= K_{\mathrm{tot}} \sum_{i=1}^{N_{\mathrm{S}}} \widehat{V}_{\mathrm{ds},i} \widehat{I}_{\mathrm{d(rms)},i}, \tag{2}$$

where $V_{\mathrm{ds},i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{\mathrm{d(rms)},i}$ is the root mean square (RMS) value of the current flowing through switch i when assuming no inductor current ripple.

The normalized switch stress M_{S} indicates how much volt-ampere (VA) stress the switches in a topology experience when transferring one per-unit watt of power from the input to the output. It commonly serves as a proxy for switching device losses or semiconductor areas in a topology [42], [44], [45], [49]. A lower M_{S} is desirable, as it indicates lower switching and conduction losses, thus contributing to higher efficiency. In addition, a lower M_{S} indicates smaller switching device areas, which is favorable to higher power density.

C. Normalized Passive Component Volume

The total passive component volume ($\mathrm{Vol}_{\mathrm{tot}}$) is the combined volume of all inductors and capacitors:

$$\mathrm{Vol}_{\mathrm{tot}} = \sum_{\text{inductors}} \mathrm{Vol}_{\mathrm{L},j} + \sum_{\text{capacitors}} \mathrm{Vol}_{\mathrm{C},k}, \tag{3}$$

where $\mathrm{Vol}_{\mathrm{L},j}$ and $\mathrm{Vol}_{\mathrm{C},k}$ represent the volumes of inductor j and capacitor k, respectively.

This work adopts an energy-based approach to passive component volume assessment by analyzing the peak energy stored in each passive component [44], [45]:

$$\mathrm{Vol}_{\mathrm{L},j} = \frac{E_{\mathrm{L},j,\mathrm{peak}}}{\rho_{\mathrm{E,L}}} \tag{4}$$

$$\mathrm{Vol}_{\mathrm{C},k} = \frac{E_{\mathrm{C},k,\mathrm{peak}}}{\rho_{\mathrm{E,C}}}, \tag{5}$$

where $E_{\mathrm{L},j,\mathrm{peak}}$ and $E_{\mathrm{C},k,\mathrm{peak}}$ represent the peak energies stored in inductor j and capacitor k, respectively. The parameter $\rho_{\mathrm{E,L}}$ and $\rho_{\mathrm{E,C}}$ are the volumetric energy densities of inductors and capacitors, respectively [38], [50]. To determine the total passive component volume that a topology requires, this section first finds the minimum inductor and capacitor values that can meet chosen current and voltage ripple requirements and then calculates the peak energy stored in these passive components.

1) Inductor Volume Calculation

Fig. 3 illustrates the current and voltage waveforms of inductor j. Define the current ripple ratio (α_{I}) as the ratio of the peak current ripple amplitude to the average inductor current:

$$\alpha_{\mathrm{I}} = \frac{\frac{1}{2}\Delta i_{\mathrm{L},j,\mathrm{pp}}}{I_{\mathrm{L},j}}, \tag{6}$$

where $I_{\mathrm{L},j}$ and $\Delta i_{\mathrm{L},j,\mathrm{pp}}$ are the average inductor current and peak-to-peak inductor current ripple, respectively, as annotated in Fig. 3. In this analysis, ripple ratios of all inductor currents are assumed to be the same for simplicity, but may be otherwise extended.

By integrating the inductor's current-voltage relation over $t \in [DT, T]$, we can obtain the peak-to-peak inductor current

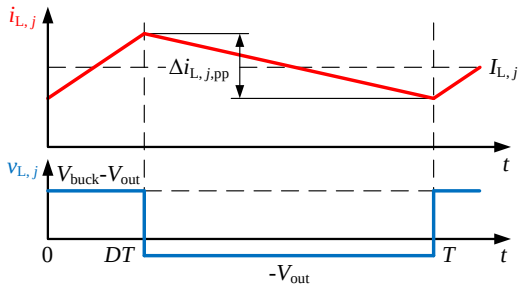


FIGURE 3. Current (top, red) and voltage (bottom, blue) waveforms of inductor j. $I_{L,j}$ and $\Delta i_{L,j,pp}$ are the average inductor current and peak-to-peak inductor current ripple, respectively. The voltage applied across the inductor jumps between $V_{buck} - V_{out}$ and $-V_{out}$.

ripple as

$$\Delta i_{L,j,pp} = \frac{V_{out}}{L_j}(1-D)\,T, \tag{7}$$

where D is the duty ratio of the buck-type stage. Based on the assumption of lossless energy transfer, D can be calculated as

$$D = \frac{1}{K_{buck}} = \frac{K_{SC}}{K_{tot}}. \tag{8}$$

We can obtain the minimum inductor value required to meet the chosen current ripple requirement (α_I) by substituting (6) and (8) into (7), which yields

$$L_j = \frac{V_{out}T}{2\alpha_I I_{L,j}}\left(1-\frac{K_{SC}}{K_{tot}}\right). \tag{9}$$

Therefore, the peak energy stored in the inductor is

$$\begin{aligned} E_{L,j,peak} &= \frac{1}{2}L_j\left(I_{L,j}+\frac{1}{2}\Delta i_{L,j,pp}\right)^2 \\ &= \frac{1}{2}L_j(1+\alpha_I)^2 {I_{L,j}}^2. \end{aligned} \tag{10}$$

Substituting (9) into (10) and dividing by inductor volumetric energy density ($\rho_{E,L}$), as shown in (4), yields the required inductor volume:

$$\mathrm{Vol}_{L,j} = \frac{(1+\alpha_I)^2 V_{out} I_{L,j} T}{4\alpha_I \rho_{E,L}}\left(1-\frac{K_{SC}}{K_{tot}}\right). \tag{11}$$

According to the passive component survey in [38], it is a reasonable approximation to assume a constant volumetric energy density ($\rho_{E,L}$) for the most energy-dense inductors rated between 1 A and 100 A, which are typically used to implement the regulated hybrid SC topologies for PoL applications discussed in this paper.

2) Capacitor Volume Calculation

Fig. 4 illustrates the voltage and current waveforms of capacitor k for two scenarios: when the SC stage and the buck-type stage operate at the same frequency (Fig. 4(a)), and when the SC stage operates at a lower frequency than the buck-type stage (Fig. 4(b)). Define the voltage ripple ratio (α_V) as the ratio of the peak voltage ripple amplitude

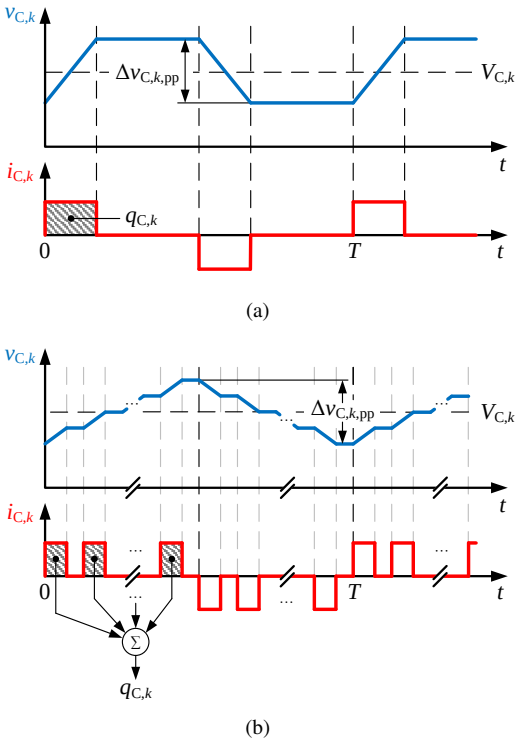


FIGURE 4. Voltage (top, blue) and current (bottom, red) waveforms of capacitor k (C_k). (a) When the SC stage and the buck-type stage operate at the same frequency. (b) When the SC stage operates at a lower frequency than the buck-type stage. $V_{C,k}$ and $\Delta v_{C,k,pp}$ are the mid-range capacitor voltage and peak-to-peak capacitor voltage ripple, respectively. $q_{C,k}$ is the accumulative charge flowing into capacitor k between the peak and valley of capacitor k's voltage waveform and is illustrated as the shaded area.

to the mid-range capacitor voltage:

$$\alpha_V = \frac{\frac{1}{2}\Delta v_{C,k,pp}}{V_{C,k}}, \tag{12}$$

where $V_{C,k}$ and $\Delta v_{C,k,pp}$ are the mid-range capacitor voltage and peak-to-peak capacitor voltage ripple, respectively, as annotated in Fig. 4. The *mid-range* voltage is the average of the maximum and minimum values of the capacitor voltage waveform and is distinct from the time-averaged or dc voltage of a capacitor [51]. In this analysis, ripple ratios of all capacitor voltages are assumed to be the same.

Illustrated as the shaded area on the capacitor current waveform in Fig. 4, $q_{C,k}$ represents the accumulative charge flowing into capacitor k between the peak and valley of capacitor k's voltage waveform. When the SC stage operates at a lower frequency than the buck-type stage, a flying capacitor can be charged multiple times before being discharged (e.g., the LEGO [7], [8] and Mini-LEGO [18], [19] topologies), as shown in Fig. 4(b). In this scenario, all charges flowing into the capacitor should be summed together when calculating $q_{C,k}$. It should be noted that the capacitor does not necessarily need to absorb charge consecutively, as depicted in Fig. 4(b). If the capacitor charging and discharging events are interspersed, $q_{C,k}$ is the

net charge flowing into the capacitor between the peak and valley of the capacitor's voltage waveform. Therefore, this analysis does not rely on the assumption that the SC stage and the buck-type stage operate at the same frequency. The effect of asynchronous operating frequencies between the two stages on the size of flying capacitors can be captured by $q_{\mathrm{C},k}$. With $q_{\mathrm{C},k}$, the peak-to-peak capacitor voltage ripple can be obtained as

$$\Delta v_{\mathrm{C},k,\mathrm{pp}} = \frac{q_{\mathrm{C},k}}{C_k}. \tag{13}$$

We can obtain the minimum capacitor value required to meet the chosen voltage ripple requirement (α_{V}) by substituting (12) into (13), which yields

$$C_k = \frac{q_{\mathrm{C},k}}{2\alpha_{\mathrm{V}} V_{\mathrm{C},k}}. \tag{14}$$

Thus, the peak energy stored in the capacitor is

$$\begin{aligned} E_{\mathrm{C},k,\mathrm{peak}} &= \frac{1}{2} C_k \left(V_{\mathrm{C},k} + \frac{1}{2}\Delta v_{\mathrm{C},k,\mathrm{pp}} \right)^2 \\ &= \frac{1}{2} C_k (1+\alpha_{\mathrm{V}})^2 {V_{\mathrm{C},k}}^2. \end{aligned} \tag{15}$$

Substituting (14) into (15) and dividing by capacitor volumetric energy density ($\rho_{E,C}$), as shown in (5), yields the required capacitor volume:

$$\mathrm{Vol}_{\mathrm{C},k} = \frac{E_{\mathrm{C},k,\mathrm{peak}}}{\rho_{\mathrm{E,C}}} = \frac{(1+\alpha_{\mathrm{V}})^2 V_{\mathrm{C},k} q_{\mathrm{C},k}}{4\alpha_{\mathrm{V}} \rho_{\mathrm{E,C}}}. \tag{16}$$

Similar to $\rho_{E,L}$, the volumetric energy density ($\rho_{E,C}$) for the most energy-dense capacitors rated between 10 V and 100 V, which are typically used to implement the regulated hybrid SC topologies for PoL applications discussed in this paper, can be assumed to be constant, according to [38].

3) Normalization of Passive Component Volume

The normalized passive component volume (M_{P}) is defined as the total passive component volume ($\mathrm{Vol}_{\mathrm{tot}}$) normalized to the base volume ($\mathrm{Vol}_{\mathrm{base}}$) and is equal to the combined normalized volume of all inductors ($\widehat{\mathrm{Vol}}_{\mathrm{L},j}$) and capacitors ($\widehat{\mathrm{Vol}}_{\mathrm{C},k}$):

$$\begin{aligned} M_{\mathrm{P}} &= \frac{\mathrm{Vol}_{\mathrm{tot}}}{\mathrm{Vol}_{\mathrm{base}}} = \frac{\sum\limits_{\text{inductors}} \mathrm{Vol}_{\mathrm{L},j} + \sum\limits_{\text{capacitors}} \mathrm{Vol}_{\mathrm{C},k}}{\mathrm{Vol}_{\mathrm{base}}} \\ &= \sum_{j=1}^{N_{\mathrm{L}}} \widehat{\mathrm{Vol}}_{\mathrm{L},j} + \sum_{k=1}^{N_{\mathrm{C}}} \widehat{\mathrm{Vol}}_{\mathrm{C},k}. \end{aligned} \tag{17}$$

As listed in Table 2, in this analysis, the base value for volume is chosen as

$$\mathrm{Vol}_{\mathrm{base}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}} T}{\rho_{\mathrm{E,L}}}, \tag{18}$$

where T is the switching period of the buck-type stage and $\rho_{E,L}$ is the volumetric energy density of inductors. This base value is chosen because it ensures that the normalized passive component volume (M_{P}) is dimensionless and independent of the output power ($V_{\mathrm{out}} I_{\mathrm{out}}$). It is worth noting that this base volume is arbitrarily defined relative to the inductor density, $\rho_{E,L}$. Alternatively, the capacitor density, $\rho_{E,C}$, can be used to produce consistent relative results. The ratio of the volumetric energy density of capacitors to that of inductors is defined as

$$\beta = \frac{\rho_{\mathrm{E,C}}}{\rho_{\mathrm{E,L}}}, \tag{19}$$

and is typically in the range of 50-1000, depending on the specific passive component technologies used [38].

Normalizing the inductor volume in (11) and the capacitor volume in (16) to the base value for volume in (18) yields the normalized inductor volume ($\widehat{\mathrm{Vol}}_{\mathrm{L},j}$) and the normalized capacitor volume ($\widehat{\mathrm{Vol}}_{\mathrm{C},k}$) as

$$\begin{aligned} \widehat{\mathrm{Vol}}_{\mathrm{L},j} = \frac{\mathrm{Vol}_{\mathrm{L},j}}{\mathrm{Vol}_{\mathrm{base}}} &= \frac{(1+\alpha_{\mathrm{I}})^2}{4\alpha_{\mathrm{I}}} \cdot \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) \cdot \underbrace{\frac{I_{\mathrm{L},j}}{I_{\mathrm{out}}}}_{\widehat{I}_{\mathrm{L},j}} \\ &= \frac{(1+\alpha_{\mathrm{I}})^2}{4\alpha_{\mathrm{I}}} \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) \widehat{I}_{\mathrm{L},j}. \end{aligned} \tag{20}$$

$$\begin{aligned} \widehat{\mathrm{Vol}}_{\mathrm{C},k} = \frac{\mathrm{Vol}_{\mathrm{C},k}}{\mathrm{Vol}_{\mathrm{base}}} &= \frac{(1+\alpha_{\mathrm{V}})^2}{4\alpha_{\mathrm{V}}} \cdot \underbrace{\frac{\rho_{\mathrm{E,L}}}{\rho_{\mathrm{E,C}}}}_{1/\beta} \cdot \underbrace{\frac{V_{\mathrm{in}}}{V_{\mathrm{out}}}}_{K_{\mathrm{tot}}} \cdot \underbrace{\frac{V_{\mathrm{C},k}}{V_{\mathrm{in}}}}_{\widehat{V}_{\mathrm{C},k}} \cdot \underbrace{\frac{q_{\mathrm{C},k}}{I_{\mathrm{out}} T}}_{\widehat{q}_{\mathrm{C},k}} \\ &= \frac{(1+\alpha_{\mathrm{V}})^2}{4\alpha_{\mathrm{V}}\beta} K_{\mathrm{tot}} \widehat{V}_{\mathrm{C},k} \widehat{q}_{\mathrm{C},k}, \end{aligned} \tag{21}$$

where β is the volumetric energy density ratio of capacitors to inductors defined in (19).

Summing the normalized volumes of all inductors and capacitors by substituting (20) and (21) into (17) yields

$$\begin{aligned} M_{\mathrm{P}} = &\sum_{j=1}^{N_{\mathrm{L}}} \frac{(1+\alpha_{\mathrm{I}})^2}{4\alpha_{\mathrm{I}}} \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) \widehat{I}_{\mathrm{L},j} \\ &+ \sum_{k=1}^{N_{\mathrm{C}}} \frac{(1+\alpha_{\mathrm{V}})^2}{4\alpha_{\mathrm{V}}\beta} K_{\mathrm{tot}} \widehat{V}_{\mathrm{C},k} \widehat{q}_{\mathrm{C},k}. \end{aligned} \tag{22}$$

Applying Kirchhoff's current law (KCL) to the average currents at the output node (i.e., the positive terminal of the load), we can obtain:

$$I_{\mathrm{out}} + \langle i_{\mathrm{Cout}} \rangle = \sum_{j=1}^{N_{\mathrm{L}}} I_{\mathrm{L},j}, \tag{23}$$

where $\langle i_{\mathrm{Cout}} \rangle$ denotes the average value of the current through the output capacitor ($\mathrm{C_{out}}$). Note that the average value of the current through a capacitor in a periodic steady state is zero. Therefore, $\langle i_{\mathrm{Cout}} \rangle = 0$, meaning

$$I_{\mathrm{out}} = \sum_{j=1}^{N_{\mathrm{L}}} I_{\mathrm{L},j}. \tag{24}$$

As a result, the sum of all normalized average inductor currents can be simplified as

$$\sum_{j=1}^{N_{\mathrm{L}}} \widehat{I}_{\mathrm{L},j} = \frac{1}{I_{\mathrm{out}}} \sum_{j=1}^{N_{\mathrm{L}}} I_{\mathrm{L},j} = 1. \tag{25}$$

Equation (22) can be simplified using (25) as

$$M_{\mathrm{P}} = \frac{(1+\alpha_{\mathrm{I}})^2}{4\alpha_{\mathrm{I}}}\left(1-\frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) + \frac{(1+\alpha_{\mathrm{V}})^2}{4\alpha_{\mathrm{V}}\beta}K_{\mathrm{tot}}\sum_{k=1}^{N_{\mathrm{C}}}\widehat{V}_{\mathrm{C},k}\widehat{q}_{\mathrm{C},k}. \tag{26}$$

Note that the derivation of M_{P} does not rely on balanced inductor currents (i.e., $I_{\mathrm{L},1} = I_{\mathrm{L},2} = \cdots = I_{\mathrm{L},N\mathrm{L}}$). Instead, the final expression for M_{P} in (26) also applies to topologies where inductor currents are not equal (e.g., the DIH topology presented in [52], [53]), since the KCL equation in (25) always holds.

The normalized passive component volume (M_{P}) is a dimensionless value that indicates the relative volume of passive components required to meet the specified ripple requirements across various topologies when transferring one per-unit watt of power from input to output, at a given switching frequency and inductor volumetric energy density. A smaller normalized passive component volume is desirable, as it indicates higher power density.

D. Normalized Total Inductor Current Slew Rate

Fast dynamic response to load transients is typically required for PoL power converters [54], [55]. When a step change in the load current occurs, the maximum total inductor current slew rate determines the fastest response a converter can achieve to recover the output voltage, regardless of the control scheme. Therefore, the maximum total inductor current slew rate represents the physical limit of a converter's transient performance. In the proposed analytical framework, the falling and rising slew rates of the total inductor current are chosen as indicators of transient performance.

1) Total Inductor Current Falling Slew Rate

Fig. 5 illustrates the key waveforms of a regulated hybrid SC converter, as shown in Fig. 1, during a load step-down transient. The load transient begins at t_0 when the load current (i_{out}) suddenly drops. The output voltage (v_{out}) reaches its peak at t_1 when the inductor current ($i_{\mathrm{L},j}$) crosses the load current flowing through branch j ($i_{\mathrm{out},j}$); it recovers to the nominal value (V_{out}) at t_2. Note that although the output voltage overshoot ($V_{\mathrm{out(max)}} - V_{\mathrm{out}}$) is exaggerated in Fig. 5 for clear illustration, it is assumed to be much smaller than V_{out}.

The fastest way of recovering v_{out} during the load step-down transient is by grounding all switch nodes and allowing the inductor currents to fall at the maximum rate. The maximum total inductor current falling slew rate ($\mathrm{SR_F}$) represents the physical limit of a topology's performance during load step-down transients. Therefore, $\mathrm{SR_F}$ is chosen as a metric to compare the transient performance of different topologies. To derive $\mathrm{SR_F}$, we first need to obtain the maximum inductor current falling slew rate for each branch and then sum them together. Assuming the output voltage

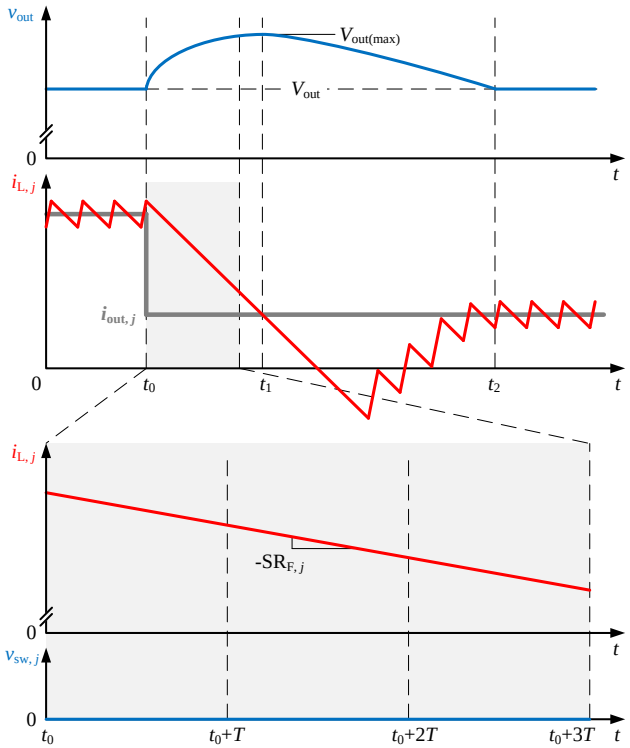


FIGURE 5. Load step-down transient waveforms of branch j. From top to bottom: the output voltage waveform (v_{out}), the waveforms of the current flowing through inductor j ($i_{\mathrm{L},j}$) and the load current flowing through branch j ($i_{\mathrm{out},j}$), the zoomed-in waveform of the inductor current over three switching cycles, and the switch-node voltage waveform seen by inductor j ($v_{\mathrm{sw},j}$). The fastest way of recovering v_{out} to the nominal value (V_{out}) is by grounding all switch nodes and allowing the inductor currents to fall at the maximum rate.

overshoot is much smaller than the nominal output voltage (V_{out}) due to the existence of the large output capacitor ($\mathrm{C_{out}}$), the maximum current falling slew rate of inductor j ($\mathrm{SR}_{\mathrm{F},j}$) can be approximated as

$$\mathrm{SR}_{\mathrm{F},j} = \frac{V_{\mathrm{out}}}{L_j}, \tag{27}$$

which can be rewritten as

$$\mathrm{SR}_{\mathrm{F},j} = \frac{K_{\mathrm{tot}}}{K_{\mathrm{tot}} - K_{\mathrm{SC}}} \cdot \frac{2\alpha_{\mathrm{I}} I_{\mathrm{L},j}}{T} \tag{28}$$

with the expression for L_j in (9) substituted into (27).

Therefore, the total inductor current falling slew rate can be obtained using the average KCL relationship in (24) as

$$\mathrm{SR_F} = \sum_{j=1}^{N_{\mathrm{L}}} \mathrm{SR}_{\mathrm{F},j} = \frac{K_{\mathrm{tot}}}{K_{\mathrm{tot}} - K_{\mathrm{SC}}} \cdot \frac{2\alpha_{\mathrm{I}} \sum_{j=1}^{N_{\mathrm{L}}} I_{\mathrm{L},j}}{T} = \frac{K_{\mathrm{tot}}}{K_{\mathrm{tot}} - K_{\mathrm{SC}}} \cdot \frac{2\alpha_{\mathrm{I}} I_{\mathrm{out}}}{T}. \tag{29}$$

2) Total Inductor Current Rising Slew Rate

Fig. 6 depicts the load step-up transient waveforms of a regulated hybrid SC converter. Similar to the load step-

down transient illustrated in Fig. 5, this load step-up transient begins at t_0 when the load current ($i_{\rm out}$) suddenly increases. The output voltage reaches its valley ($V_{\rm out(min)}$) at t_1 when the inductor current crosses the load current flowing through branch j ($i_{{\rm out},j}$); it recovers to the nominal value ($V_{\rm out}$) at t_2. The output voltage undershoot ($V_{\rm out}-V_{\rm out(min)}$) is assumed to be much smaller than $V_{\rm out}$, although it is exaggerated in Fig. 6 for clear illustration.

The fastest way of recovering $v_{\rm out}$ is by operating all branches at the maximum duty ratio ($D_{\max}$) and forcing the inductor currents to rise at the maximum rate. Unlike the conventional multi-phase buck converter, many regulated hybrid SC topologies have an upper limit on the achievable duty ratio. For, example, the SCB converter with multi-phase operation shown in Fig. 2 has a maximum duty ratio of $1/N_{\rm L}$. A discussion of how this upper limit on the duty ratio affects the load step-up transient performance of regulated hybrid SC topologies will be provided in Section IV.

The maximum total inductor current rising slew rate ($\mathrm{SR_R}$) represents the physical limit of a topology's performance during load step-up transients. Therefore, $\mathrm{SR_R}$ is chosen as a metric for the performance comparison of load step-up transients. Based on the small-ripple approximation, the maximum current rising slew rate of inductor j ($\mathrm{SR}_{{\rm R},j}$) can be obtained as

$$\mathrm{SR}_{{\rm R},j}=\frac{\langle v_{{\rm sw},j}\rangle-V_{\rm out}}{L_j}, \tag{30}$$

where $\langle v_{{\rm sw},j}\rangle$ denotes the average value of the switch-node voltage, $v_{{\rm sw},j}$, over a switching period:

$$\langle v_{{\rm sw},j}\rangle=D_{\max}V_{\rm buck}. \tag{31}$$

Substituting (9) and (31) into (30) and recognizing that $V_{\rm buck}/V_{\rm out}=K_{\rm tot}/K_{\rm SC}$ yields

$$\mathrm{SR}_{{\rm R},j}=\left(D_{\max}\frac{K_{\rm tot}}{K_{\rm SC}}-1\right)\cdot\frac{K_{\rm tot}}{K_{\rm tot}-K_{\rm SC}}\cdot\frac{2\alpha_{\rm I}I_{{\rm L},j}}{T}. \tag{32}$$

Therefore, the total inductor current rising slew rate can be obtained as

$$\begin{aligned}\mathrm{SR_R}&=\sum_{j=1}^{N_{\rm L}}\mathrm{SR}_{{\rm R},j}\\&=\left(D_{\max}\frac{K_{\rm tot}}{K_{\rm SC}}-1\right)\cdot\frac{K_{\rm tot}}{K_{\rm tot}-K_{\rm SC}}\cdot\frac{2\alpha_{\rm I}\sum_{j=1}^{N_{\rm L}}I_{{\rm L},j}}{T}\\&=\left(D_{\max}\frac{K_{\rm tot}}{K_{\rm SC}}-1\right)\cdot\frac{K_{\rm tot}}{K_{\rm tot}-K_{\rm SC}}\cdot\frac{2\alpha_{\rm I}I_{\rm out}}{T}.\end{aligned} \tag{33}$$

3) Normalization of Total Inductor Current Slew Rate

As listed in Table 2, in this analysis, the base value for the current slew rate is chosen as

$$\mathrm{SR_{base}}=\frac{2\alpha_{\rm I}I_{\rm out}}{T}. \tag{34}$$

This base value is chosen because it is a common term in the expressions for the total inductor current falling and rising slew rates ($\mathrm{SR_F}$ and $\mathrm{SR_R}$) shown in (29) and (33), respectively. More importantly, it ensures that the expressions for the normalized current slew rates are dimensionless and independent of the output current ($I_{\rm out}$).

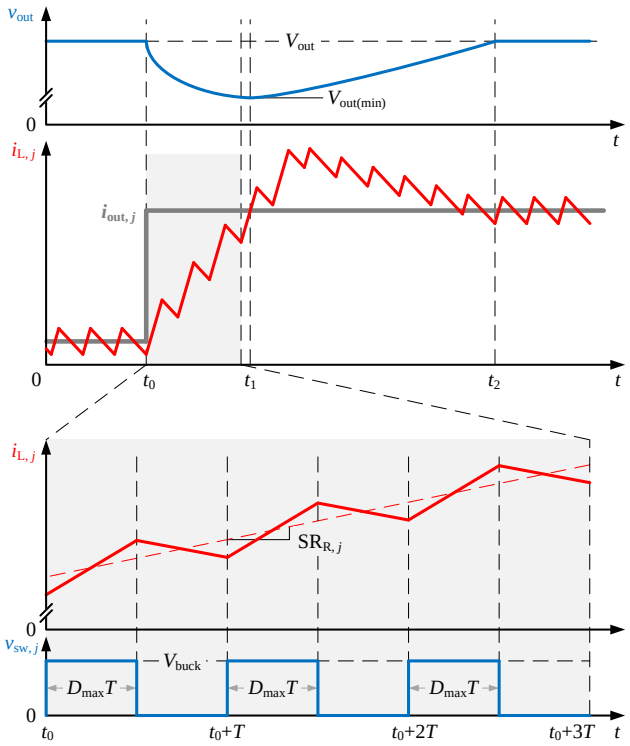


FIGURE 6. Load step-up transient waveforms of branch j. From top to bottom: the output voltage waveform ($v_{\rm out}$), the waveforms of the current flowing through inductor j ($i_{{\rm L},j}$) and the load current flowing through branch j ($i_{{\rm out},j}$), the zoomed-in waveform of the inductor current over three switching cycles, and the switch-node voltage waveform seen by inductor j ($v_{{\rm sw},j}$). The fastest way of recovering $v_{\rm out}$ to the nominal value ($V_{\rm out}$) is by operating all branches at the maximum duty ratio ($D_{\max}$) and forcing the inductor currents to rise at the maximum rate.

Normalizing the total inductor current falling and rising slew rates in (29) and (33) to the base value in (34) yields the normalized total inductor current falling slew rate ($\widehat{\mathrm{SR}}_{\rm F}$) and the normalized total inductor current rising slew rate ($\widehat{\mathrm{SR}}_{\rm R}$) as

$$\widehat{\mathrm{SR}}_{\rm F}=\frac{\mathrm{SR_F}}{\mathrm{SR_{base}}}=\frac{K_{\rm tot}}{K_{\rm tot}-K_{\rm SC}} \tag{35}$$

$$\widehat{\mathrm{SR}}_{\rm R}=\frac{\mathrm{SR_R}}{\mathrm{SR_{base}}}=\left(D_{\max}\frac{K_{\rm tot}}{K_{\rm SC}}-1\right)\cdot\frac{K_{\rm tot}}{K_{\rm tot}-K_{\rm SC}}. \tag{36}$$

Since $K_{\rm tot}$ is a constant determined by the application, $\widehat{\mathrm{SR}}_{\rm F}$ is a function of the SC stage conversion ratio ($K_{\rm SC}$) only, as can be seen in (35). Additionally, equation (36) shows that $\widehat{\mathrm{SR}}_{\rm R}$ is a function of the SC stage conversion ratio ($K_{\rm SC}$) and the maximum duty ratio ($D_{\max}$).

E. Formalized Analysis Procedure

According to (2) and (26), the following topology-dependent characteristic parameters are needed to calculate the normalized metrics $M_{\rm S}$ and $M_{\rm P}$: $\widehat{V}_{{\rm ds},i}$, $\widehat{I}_{{\rm d(rms)},i}$, $\widehat{V}_{{\rm C},k}$, and $\widehat{q}_{{\rm C},k}$. To

formalize the analytical procedure, we define the following four topology-dependent characteristic vectors:

- Switch voltage stress vector: $\widehat{\mathbf{V}}_{\rm ds} = \left(\widehat{V}_{{\rm ds},i}\right)_{1\leqslant i\leqslant N_{\rm S}}$
- Switch current stress vector: $\widehat{\mathbf{I}}_{\rm d(rms)} = \left(\widehat{I}_{\rm d(rms),i}\right)_{1\leqslant i\leqslant N_{\rm S}}$
- Capacitor voltage vector: $\widehat{\mathbf{V}}_{\rm C} = \left(\widehat{V}_{{\rm C},k}\right)_{1\leqslant k\leqslant N_{\rm C}}$
- Capacitor charge vector: $\widehat{\mathbf{q}}_{\rm C} = (\widehat{q}_{{\rm C},k})_{1\leqslant k\leqslant N_{\rm C}}$

with which we can rearrange (2) and (26) as

$$M_{\rm S} = K_{\rm tot}\widehat{\mathbf{V}}_{\rm ds}^{\top}\widehat{\mathbf{I}}_{\rm d(rms)}, \tag{37}$$

and

$$M_{\rm P} = M_{\rm P,L} + M_{\rm P,C}, \tag{38}$$

where $M_{\rm P,L}$ is the normalized inductor volume

$$M_{\rm P,L} = \frac{(1+\alpha_{\rm I})^2}{4\alpha_{\rm I}}\left(1-\frac{K_{\rm SC}}{K_{\rm tot}}\right), \tag{39}$$

and $M_{\rm P,C}$ is the normalized capacitor volume

$$M_{\rm P,C} = \frac{(1+\alpha_{\rm V})^2}{4\alpha_{\rm V}\beta}K_{\rm tot}\widehat{\mathbf{V}}_{\rm C}^{\top}\widehat{\mathbf{q}}_{\rm C}, \tag{40}$$

in which $\cdot^{\top}$ denotes the transpose of a vector. The characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies are listed in Appendix A.

Equations (37) and (38) provide a formalized analytical procedure of $M_{\rm S}$ and $M_{\rm P}$ that can be automated. Equations (39) and (40) reveal two properties of $M_{\rm P,L}$ and $M_{\rm P,C}$:

- As the SC stage conversion ratio ($K_{\rm SC}$) increases, the normalized inductor volume ($M_{\rm P,L}$) decreases and the normalized capacitor volume ($M_{\rm P,C}$) increases. This is intuitive because increasing the SC stage conversion ratio means shifting more voltage conversion burden from the buck-type stage to the SC stage, reducing the inductor volume but necessitating a higher-order SC network, which requires more and larger flying capacitors.
- Topologies with the same SC stage conversion ratio ($K_{\rm SC}$) have the same normalized inductor volume ($M_{\rm P,L}$) because the only topology-independent parameter in (39) is $K_{\rm SC}$, while $K_{\rm tot}$, $\alpha_{\rm I}$, $\alpha_{\rm V}$ and β are all constants. Therefore, the difference in the normalized passive component volume among different topologies with the same SC stage conversion ratio only comes from the difference in the normalized capacitor volume ($M_{\rm P,C}$).

These two properties will be used in the comparative analysis of the normalized passive component volume in Section IV-C.

IV. Comparative Performance Analysis of 48-V-to-PoL Regulated Hybrid SC Topologies

Based on the analytical framework established in Section III, this section performs a comparative analysis of state-of-the-art 48-V-to-1-V hybrid SC topologies and demonstrates the benefits of a larger SC stage conversion ratio.

A. Performance Comparison

Tables 3 and 4 summarize the key characteristics and the three normalized metrics of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. The year listed for each topology is when it was first proposed. If a topology has yielded more than one publication, the two most representative references are provided in the citation: 1) the earliest publication where the topology was first proposed, and 2) the latest publication that provides the most thorough explanation of the topology and/or includes experimental results from the best-performing hardware prototype.

The normalized passive component volume ($M_{\rm P}$) of each topology is calculated using the following ripple ratios: $\alpha_{\rm I} = 15\%$ and $\alpha_{\rm V} = 5\%$. The reasons for selecting these ripple ratios are explained below. As a rule of thumb, the peak-to-peak inductor current ripple ($\Delta i_{\rm L,pp}$) of a buck converter is typically designed to be between 20% and 40% of the full-load output current [56]. In this analysis, it is assumed that $\Delta i_{\rm L,pp}$ is 30% (average of 20% and 40%) of the per-branch averaged current at full load, resulting in $\alpha_{\rm I} = 15\%$. In addition, the peak-to-peak capacitor voltage ripple ($\Delta v_{\rm C,pp}$) is assumed to be 10% of the mid-range capacitor voltage, following the rule of thumb for the small-ripple approximation to be valid, which yields $\alpha_{\rm V} = 5\%$.

The normalized switch stress ($M_{\rm S}$) of each topology is calculated under the assumption of negligible inductor current ripples and capacitor voltage ripples, as mentioned in Section III-A. Inductor current ripples can be ignored in the analysis of the normalized switch stress because their influence on switch RMS current stress is typically very small. For example, the RMS value of the current flowing through the high-side switch in a buck converter, which exhibits a pulsating current waveform with linear ripple, can be given as

$$I_{\rm d(rms)} = I_{\rm L}\sqrt{D}\sqrt{1+\frac{1}{3}\alpha_{\rm I}^2}, \tag{41}$$

where $I_{\rm L}$ is the average inductor current, D is the duty ratio, and $\alpha_{\rm I}$ is the inductor current ripple ratio as defined in (6). Even if $\alpha_{\rm I} = 20\%$ (i.e., $\Delta i_{\rm L,pp} = 0.4I_{\rm L}$), the RMS current ($I_{\rm d(rms)}$) changes by only 0.7% ($\sqrt{1+\frac{1}{3}\times 0.2^2} = 1.007$). Therefore, inductor current ripples are typically negligible in the calculation of switch RMS current stress. Similarly, capacitor voltage ripples are ignored in the calculation of switch voltage stress because they are assumed to be small compared to the mid-range voltages ($\alpha_{\rm V} = 5\%$).

B. Analysis of Normalized Switch Stress

To better visualize the influence of the SC stage conversion ratio ($K_{\rm SC}$), Fig. 7 plots the normalized switch stress ($M_{\rm S}$) of different topologies against their SC stage conversion ratio ($K_{\rm SC}$). Solid dots represent topologies with hardware

TABLE 3. Key characteristics of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion

Year	Topology	SC Stage Conversion Ratio (K_{SC} : 1)	Buck-Type Stage Conversion Ratio (K_{buck} : 1)	Buck-Type Stage Duty Ratio		Complete Soft-Charging?
				Nominal (D)	Maximum (D_{max})	
2005	Series-capacitor buck with multi-phase operation [1]	2:1	24:1	0.042	0.5	Yes
		3:1	16:1	0.063	0.333	
2011	Series-capacitor buck with two-phase operation [2]	4:1	12:1	0.083	0.5	Yes
2020	Crossed-coupled QSD buck [12]	4:1	12:1	0.083	0.5	Yes
2018	DIH [4], [5]	6:1	8:1	0.125	0.5	Yes, with split-phase control
2019 2023	LEGO [7], [8] Mini-LEGO [18], [19]	6:1	8:1	0.125	1.0	No
2020	SDIH [13], [14]	6:1	8:1	0.125	0.5	Yes, with split-phase control
2021	CaSP [15]	6:1	8:1	0.125	0.333	Yes
2020	MLB [9], [10]	8:1	6:1	0.167	0.5	Yes
2020	VIB [20], [21]	8:1	6:1	0.167	0.25	No
2022	MSC [22], [23]	8:1	6:1	0.167	0.25	Yes
2022	Dickson^2 [24]	9:1	5.33:1	0.188	0.333	Yes
2023	16-to-1 switching bus converter (SBC) [25], [26]	16:1	3:1	0.333	0.5	Yes
2023	20-to-1 switching bus converter (SBC) [27], [28]	20:1	2.4:1	0.417	0.5	Yes

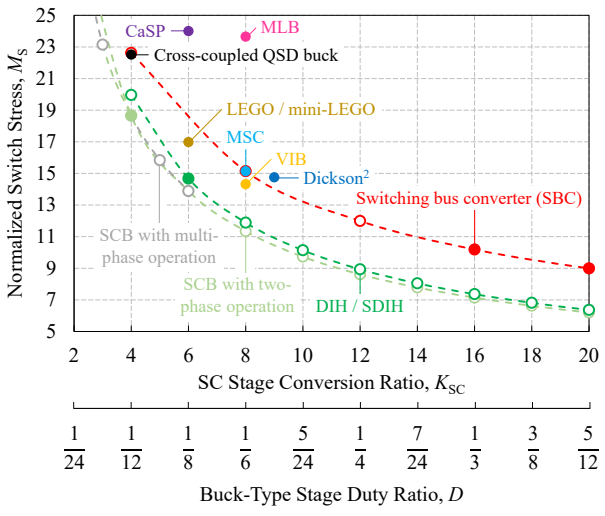


FIGURE 7. Normalized switch stress (M_S) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A lower normalized switch stress (M_S) is more desirable.

demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. Some extendable topologies are plotted with dashed curves connecting different possible implementations at different SC stage conversion ratios. As shown in Fig. 7, with a larger SC stage conversion ratio, the buck-type stage duty ratio (D) can be extended.

The maximum achievable SC stage conversion ratio ($K_{SC(max)}$) of a regulated hybrid SC topology is limited by its maximum duty ratio (D_{max}) and the total conversion ratio (K_{tot}). More specifically, the maximum output voltage of a regulated hybrid SC topology is given by

$$V_{out(max)} = \frac{D_{max} V_{in}}{K_{SC}}. \tag{42}$$

Since $V_{out(max)}$ must be greater than V_{out}, the SC stage conversion ratio must not exceed

$$K_{SC} < \frac{D_{max} V_{in}}{V_{out}} = D_{max} K_{tot}. \tag{43}$$

The series-capacitor-buck (SCB) topology was first proposed in [1] with multi-phase operation and then extended in [2] with two-phase operation. Fig. 8(a) shows a four-phase SCB converter as an example. In the multi-phase operation illustrated in Fig. 8(b), each inductor operates in an individual phase; in the two-phase operation illustrated in

TABLE 4. Performance comparison of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion

Year	Topology	Normalized Switch Stress (M_S)	Normalized Passive Component Volume (M_P)			Normalized Total Inductor Current Slew Rate	
			$\beta = 500$	$\beta = 100$	$\beta = 50$	Falling Slew Rate ($\widehat{SR}_F$)	Rising Slew Rate ($\widehat{SR}_R$)
2005	Series-capacitor buck with multi-phase operation [1]	31.6	2.12	2.14	2.17	1.04	11.5
		23.1	2.08	2.12	2.18	1.07	4.62
2011	Series-capacitor buck with two-phase operation [2]	18.7	2.04	2.10	2.19	1.09	5.45
2020	Crossed-coupled QSD buck [12]	24.2	2.03	2.08	2.13	1.09	5.45
2018	DIH* [4], [5]	14.7	2.02	2.40	2.87	1.14	3.43
2019 2023	LEGO† [7], [8] Mini-LEGO† [18], [19]	17.6	2.03	2.41	2.89	1.14	8.00
2020	SDIH* [13], [14]	14.7	2.02	2.40	2.84	1.14	3.43
2021	CaSP [15]	23.5	1.95	2.02	2.11	1.14	1.90
2020	MLB [9], [10]	23.7	1.88	2.03	2.22	1.20	2.40
2020	VIB‡ [20], [21]	14.3	1.88	2.07	2.3	1.20	0.60
2022	MSC [22], [23]	15.1	1.86	1.95	2.06	1.20	0.60
2022	Dickson^2 [24]	14.8	1.81	1.90	2.01	1.23	0.96
2023	16-to-1 switching bus converter (SBC) [25], [26]	10.2	1.51	1.69	1.91	1.50	0.75
2023	20-to-1 switching bus converter (SBC) [27], [28]	8.99	1.34	1.56	1.84	1.71	0.34

* In the DIH [4], [5] and SDIH [13], [14] topologies, all flying capacitor voltage ripples are designed to have equal magnitude, which enables simple split-phase control timing. Since the mid-range voltages across different flying capacitors are different, the voltage ripple ratios of different flying capacitors in these two works are not uniform. Nevertheless, the normalized passive component volume (M_P) listed in this table assumes uniform voltage ripple ratios for all flying capacitors, which requires more complex split-phase control timing.

† Small filter capacitors (C_{filter}) are not taken into account in the capacitor volume analysis, although they are used in the hardware prototypes of the LEGO [7], [8] and Mini-LEGO [18], [19] topologies to filter the high-frequency pulsating current from the buck-type stage. Additionally, the charge-sharing loss between the filter capacitors and the flying capacitors is not captured in this analysis.

‡ In addition to flying capacitors, an intermediate bus capacitor (C_{IB}) is included in the capacitor volume calculation for the VIB topology [20], [21] as well. As mentioned in [20], [21], its value is chosen to be $C_{IB} = C_F/2.34$, where C_F is the charge pump capacitance. The normalized voltage stress on C_{IB} is $1/2$. The charge-sharing loss between the intermediate bus capacitor and the flying capacitors is not captured in this analysis.

Fig. 8(c), the inductors are divided into two groups: the odd-numbered group and the even-numbered group, each operating in an individual phase with a 180° phase shift. Compared to the multi-phase operation, the two-phase operation can extend the maximum duty ratio from $D_{\mathrm{m-ph(max)}} = \frac{1}{N}$ to $D_{\mathrm{2-ph(max)}} = \frac{1}{2}$, where N is the number of branches. Because the SC stage conversion ratio of a SCB converter is equal to its number of branches (i.e., $N = K_{\mathrm{SC,m-ph}}$), the maximum duty ratio for multi-phase operation can be expressed as $D_{\mathrm{m-ph(max)}} = \frac{1}{K_{\mathrm{SC,m-ph}}}$. According to (43), the SC stage conversion ratio ($K_{\mathrm{SC,m-ph}}$) for multi-phase operation is limited by

$$K_{\mathrm{SC,m-ph}} < D_{\mathrm{m-ph(max)}} K_{\mathrm{tot}} = \frac{K_{\mathrm{tot}}}{K_{\mathrm{SC,m-ph}}}, \tag{44}$$

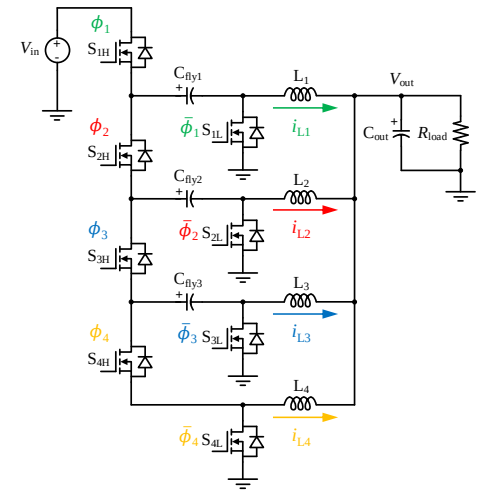
which can be rearranged as

$$K_{\mathrm{SC,m-ph}} < \sqrt{K_{\mathrm{tot}}}. \tag{45}$$

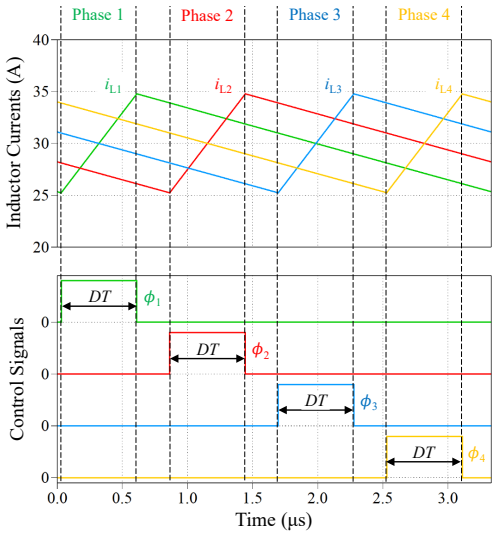
Similarly, the SC stage conversion ratio ($K_{\mathrm{SC,2-ph}}$) for two-phase operation is limited by

$$K_{\mathrm{SC,2-ph}} < D_{\mathrm{2-ph(max)}} K_{\mathrm{tot}} = \frac{K_{\mathrm{tot}}}{2}. \tag{46}$$

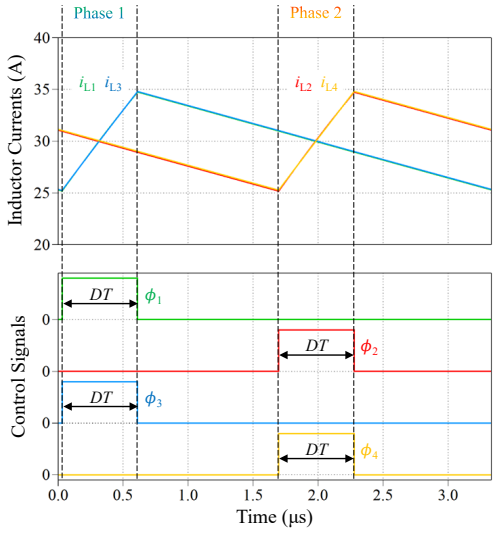
For 48-V-to-1-V conversion ($K_{\mathrm{tot}} = 48$), these upper limits are $K_{\mathrm{SC,m-ph}} < 6.9$ and $K_{\mathrm{SC,2-ph}} < 24$, respectively. Since $K_{\mathrm{SC,m-ph}}$ must be an integer and $K_{\mathrm{SC,2-ph}}$ must be an even number, the maximum achievable SC stage conversion ratios for multi-phase operation and two-phase operation are $K_{\mathrm{SC,m-ph(max)}} = 6$ and $K_{\mathrm{SC,2-ph(max)}} = 22$, respectively. As K_{SC} increases, the voltage stress on all switches decreases while the current stress on most switches increases. Nevertheless, the increase in switch current stress does not offset the voltage stress reduction. Therefore, as shown in Fig. 7, the net result is that the normalized switch stress of a SCB converter decreases as K_{SC} increases. This means that a SCB converter with a larger SC stage



(a)



(b)



(c)

FIGURE 8. Four-branch SCB converter. (a) Schematic drawing. (b) Multi-phase operation. (c) Two-phase operation.

conversion ratio has the theoretical potential of achieving higher efficiency. Compared to multi-phase operation, two-phase operation can better leverage the benefits of a larger SC stage conversion ratio since it extends the upper limit on the number of branches.

Although two-phase operation does result in a larger net output current ripple than multi-phase operation, this does not necessarily require a larger output capacitor in PoL applications. The size of the output capacitor in these applications is mainly dictated by transient performance requirements, such as limiting the maximum output voltage overshoot and undershoot. Typically, an output capacitor that is sufficiently large to meet these transient requirements also ensures that the steady-state output voltage ripple stays well below the maximum acceptable levels. Therefore, there is no need to increase the output capacitance when changing from multi-phase operation to two-phase operation. In fact, as will be explained in Section IV-D, since two-phase operation enables a faster transient response than multi-phase operation, the output capacitance can potentially be reduced.

The DIH [4], [5] and SDIH[1] [13], [14] topologies can be viewed as SCB topologies under two-phase operation, but with the inductors operating in the same phase merged into one large inductor by short-circuiting the odd-numbered and even-numbered switch nodes, respectively [14]. Given that the scaling law of magnetics favors larger components [57], combining multiple small inductors into one large inductor can typically improve the overall performance of magnetic components. However, short-circuiting the switch nodes can bring about the hard-charging of flying capacitors. In DIH and SDIH topologies with an even SC conversion ratio, this can only be overcome by the split-phase control [58]. The additional secondary phases introduced by the split-phase control reduce the effective duty ratio, resulting in slightly higher normalized switch stress for the DIH and SDIH topologies compared to a SCB topology under two-phase operation, as shown in Fig. 7. Due to the sensitivity of split-phase control timing to component sizing, either capacitors with high stability, such as Class I multilayer ceramic capacitors (MLCCs) that have lower energy densities, or active split-phase control [59], [60] must be used to ensure complete soft-charging.

The switching bus converter (SBC) [25], [26], [27], [28] merges a 2-to-1 SC front-end with two SCB modules through two *switching buses*, which allows for the removal of intermediate bus capacitors and redundant switches. Reference [26] provides a detailed illustration of the two-stage merging process in Fig. 4 and explains the advantages of the switching-bus-based architecture over the existing dc-bus-based architecture. Each downstream SCB module operates in the two-phase fashion illustrated in Fig. 8(c). Therefore, the SBC extends the maximum duty ratio ($D_{\max}$) to 50% and similarly enables a larger SC stage conversion ratio. For 48-

[1]The SDIH topology was first proposed in [13] under the alias *D-2L-ni_Reg*.

V-to-1-V conversion ($K_{\text{tot}} = 48$), the SC stage conversion ratio of the SBC cannot exceed

$$K_{\text{SC,SBC}} < D_{\max} K_{\text{tot}} = 24, \tag{47}$$

according to (43). Given that the SBC merges a 2-to-1 SC front-end with two SCB modules under two-phase operation, the SC stage conversion ratio of the SBC must be a multiple of 4. Therefore, the maximum achievable SC stage conversion ratio is $K_{\text{SC,SBC(max)}} = 20$. As discussed in [26], the switching-bus-based architecture ensures complete soft-charging operation, thus avoiding the need for split-phase control. The switching bus concept was first introduced in [24] with the Dickson^2 topology. Other switching-bus-based topologies include MLB [9], [10] and CaSP [15] topologies.

Fig. 7 shows that, in general, increasing the SC stage conversion ratio of a regulated hybrid SC topology reduces its normalized switch stress, thereby improving efficiency. One possible concern about using the normalized switch stress as an indicator of efficiency is that it only captures the power losses in semiconductor switches but excludes the losses in flying capacitors and inductors. Flying capacitor equivalent series resistance (ESR) conduction loss is typically lower than 5% of total loss and is thereby negligible. However, inductor core loss and winding loss cannot be neglected. As the SC stage conversion ratio increases, the voltage stress (V_{buck}) on the subsequent buck-type stage is reduced, and therefore, the inductor size is decreased, resulting in a smaller core volume and lower dc resistance (DCR). This means that the inductor losses are reduced when the SC stage conversion ratio is increased. Consequently, the conclusion that increasing the SC stage conversion ratio is favorable for efficiency improvement holds, even with the inductor losses taken into consideration.

C. Analysis of Normalized Passive Component Volume

Fig. 9 shows the normalized passive component volume (M_{P}) of different topologies against their SC stage conversion ratio (K_{SC}), assuming an inductor current ripple ratio of $\alpha_{\text{I}} = 15\%$, a capacitor voltage ripple ratio of $\alpha_{\text{V}} = 5\%$, and three different energy density ratios of capacitors to inductors: $\beta = 500,\ 100,\ 50$. Table 5 lists three practical examples for calculating the energy density ratio (β) between capacitors and inductors. The commercial capacitor component TDK C3216X7R1H106K160AE [61] is rated at 50 V and is assumed to withstand a peak voltage of 25 V. Under a dc bias of 25 V, its capacitance derates to 3.5 μF. Therefore, the volumetric energy density of this capacitor component, when biased at a dc voltage of 25 V, is calculated as $\frac{1}{2}CV^2$ divided by its volume, which is equal to 134 μJ/mm^3. Similarly, the volumetric energy density of a commercial discrete inductor component, Coilcraft SLR1065-301KEC [62], at its saturation current (32 A) is calculated as $\frac{1}{2}LI^2$ divided by its volume, yielding 0.256 μJ/mm^3. Therefore, in this example, the energy density ratio between these two commercial components is $\beta_{\text{DL}} = \frac{134}{0.256} = 523$, which is representative of the energy density ratios between

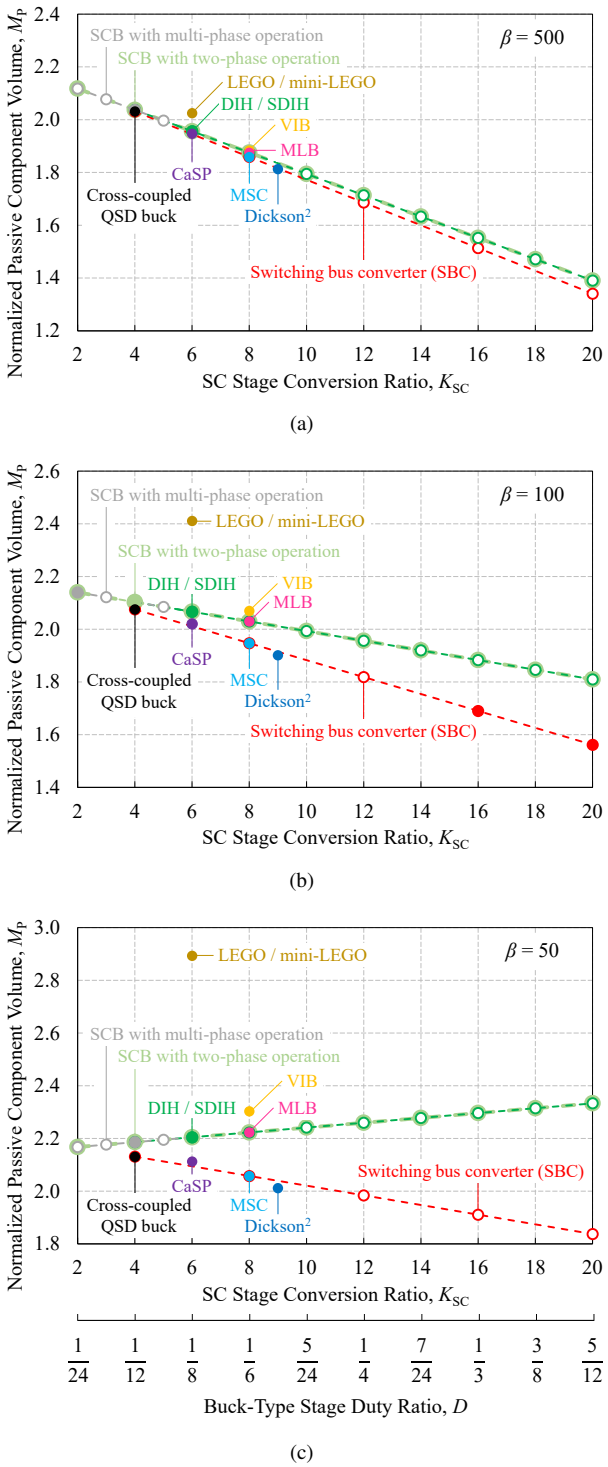


FIGURE 9. Normalized passive component volume (M_{P}) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion ($\alpha_{\text{I}} = 15\%$, $\alpha_{\text{V}} = 5\%$). (a) $\beta = 500$. (b) $\beta = 100$. (c) $\beta = 50$. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A smaller normalized passive component volume (M_{P}) is more desirable.

TABLE 5. Practical examples for calculating the energy density ratio (β) between capacitors and inductors

Component	Part Number	Parameters	Dimensions	Volumetric Energy Density
Capacitor	TDK C3216X7R1H106K160AE [61]	Rated voltage: 50 V Capacitance: 3.5 µF (@ 25 V)	$3.2 \times 1.6 \times 1.6$ mm^3	134 µJ/mm^3 (@ 25 V)
Discrete Inductor	Coilcraft SLR1065-301KEC [62]	Saturation current: 32 A Inductance: 275 nH (@ 32 A) DCR: 0.48 mΩ	$10.4 \times 8.0 \times 6.6$ mm^3	0.256 µJ/mm^3 (@ 32 A) $(\beta_{\mathrm{DL}} = \frac{134}{0.256} = 523)$
Coupled Inductor	Customized four-phase coupled inductor presented in [27]	Saturation current: 45 A Inductance: 260 nH* (@ 45 A) DCR: 0.16 mΩ	$18.5 \times 10.5 \times 3.2$ mm^3	1.69 µJ/mm^3 (@ 45 A) $(\beta_{\mathrm{CL}} = \frac{134}{1.69} = 79)$

* Per-phase steady-state inductance (four-phase average value at $D = 0.417$).

commercial Class II MLCCs and discrete inductors. Note that this example assumes 50% voltage utilization of the capacitor component, meaning that it is assumed to operate at 50% of its rated voltage. When fully utilized, commercial Class II MLCCs can achieve an approximately 1000 times higher energy density compared to commercial discrete inductors [38]. Due to DC flux cancellation, coupled inductors can achieve the same per-phase steady-state inductance with a smaller core volume compared to discrete inductors [63]. As listed in Table 5, the customized four-phase coupled inductor presented in [27] achieves a volumetric energy of 1.69 µJ/mm^3 at its saturation current, which is 6.6 times higher than the commercial discrete inductor component. The energy density ratio between the commercial capacitor component (TDK C3216X7R1H106K160AE) and this customized four-phase coupled inductor is $\beta_{\mathrm{CL}} = \frac{134}{1.69} = 79$. These practical examples demonstrate that $\beta = 500$ can be used in topological comparisons involving commercial discrete inductors, while β may decrease to 100 or even 50 when customized coupled inductors are used.

As can be seen in Fig. 9(a), when $\beta = 500$ (for example, when discrete inductors are used), the normalized passive component volume (M_{P}) of the regulated hybrid SC topologies decreases as their SC stage conversion ratio (K_{SC}) increases. The normalized passive component volume is the sum of the normalized inductor volume and the normalized capacitor volume (i.e., $M_{\mathrm{P}} = M_{\mathrm{P,L}} + M_{\mathrm{P,C}}$). Recall the first property of $M_{\mathrm{P,L}}$ and $M_{\mathrm{P,C}}$ mentioned at the end of Section III-E: as K_{SC} increases, $M_{\mathrm{P,L}}$ decreases and $M_{\mathrm{P,C}}$ increases. However, since capacitors have much higher volumetric energy densities compared to discrete inductors, as demonstrated in Table 5, the increase in capacitor volume does not offset the inductor volume reduction. As a result, the total passive component volume decreases as the SC stage conversion ratio increases. This shows that when discrete inductors are used, increasing the SC stage conversion ratio of a regulated hybrid SC topology reduces its passive component volume, thereby improving power density.

As β decreases (for example, when coupled inductors with higher energy densities are used), the inductor volume reduction rate with respect to the SC stage conversion ratio (K_{SC}) drops and gradually approaches the capacitor volume increase rate. As a result, the slope of the M_{P} lines becomes less negative when β decreases from 500 to 100, as can be observed in Figs. 9(a) and (b). This means that the increase in the capacitor volume plays a more important role in the total volume change as K_{SC} increases when inductors are more energy-dense (i.e., when β decreases). It can be anticipated that when β decreases to a certain extent, the inductor volume reduction rate with respect to K_{SC} will be smaller than the capacitor volume increase rate. As a result, the increase in the capacitor volume will dominate the total volume change, meaning that M_{P} will rise as K_{SC} increases. This is indeed what happens when β decreases from 100 to 50. As shown in Fig. 9(c), when $\beta = 50$, the normalized passive component volume of the SCB [1], [2], DIH [4], [5], and SDIH [13], [14] topologies rises as the SC stage conversion ratio increases, resulting from the increase in the capacitor volume. Therefore, these topologies cannot leverage the benefits of a larger SC stage conversion ratio when high-density coupled inductors are used. Distinct from the SCB, DIH, and SDIH topologies, the switching bus converter (SBC) [25], [26], [27], [28] maintains a decreasing normalized passive component volume as the SC stage conversion ratio increases, even when $\beta = 50$. This demonstrates the SBC's ability to achieve higher power density by leveraging the benefits of a larger SC stage conversion ratio and the high energy densities of coupled inductors simultaneously.

Recall the second property of $M_{\mathrm{P,L}}$ and $M_{\mathrm{P,C}}$ mentioned at the end of Section III-E: topologies with the same SC stage conversion ratio have the same normalized inductor volume. Therefore, at the same SC stage conversion ratio, the difference in the normalized passive component volume among different topologies only comes from the difference in the normalized capacitor volume. In the SCB, DIH, and SDIH topologies, the mid-range flying capacitor voltages are $\frac{k}{K_{\mathrm{SC}}} V_{\mathrm{in}}$ $(k = 1, 2, \cdots, K_{\mathrm{SC}} - 1)$, with half of the capacitor voltages beyond $\frac{1}{2} V_{\mathrm{in}}$. In contrast, the flying capacitor voltages in the SBC are $\frac{1}{2} V_{\mathrm{in}}$ and

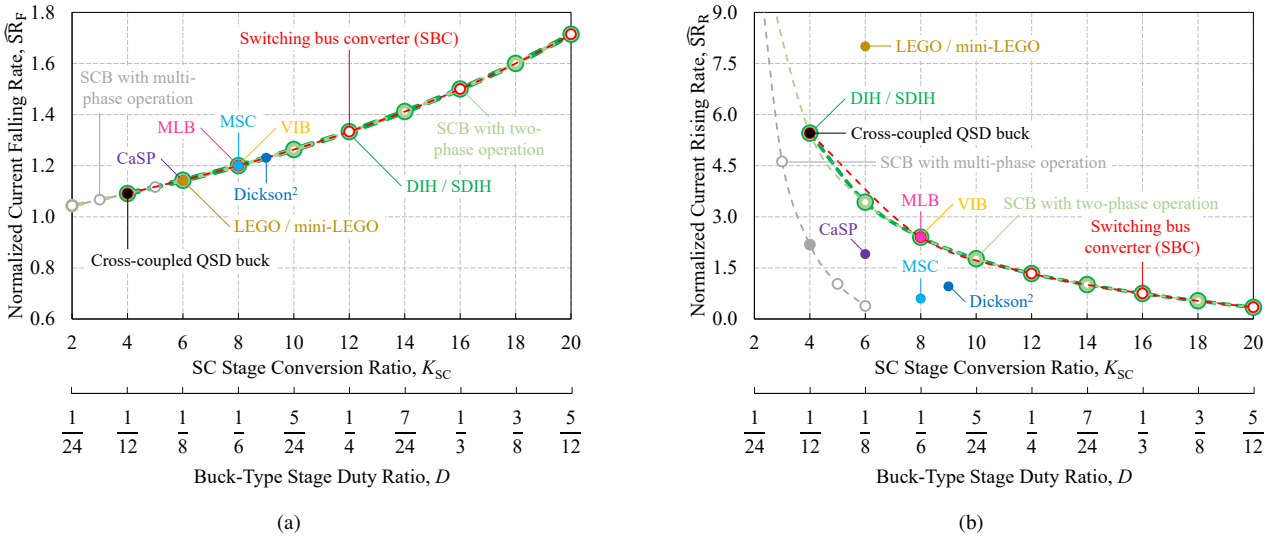


FIGURE 10. **Normalized total inductor current slew rate. (a) Normalized total inductor current falling slew rate ($\widehat{SR}_F$). (b) Normalized total inductor current rising slew rate ($\widehat{SR}_R$). Larger current slew rates are more desirable since they indicate faster dynamic response and better transient performance.**

$\frac{k}{K_{SC}}V_{in}$ $(k = 1, 2, \cdots, K_{SC}/2 - 1)$, with all capacitor voltages lower than or equal to $\frac{1}{2}V_{in}$. Consequently, by first halving the input voltage with its initial 2-to-1 SC front-end, the SBC reduces the requirement for capacitive energy storage, thereby reducing the flying capacitor volume and total passive component volume. Note that this advantage comes at the cost of relatively increased switch stress, as can be observed in Fig. 7.

It should be noted that the aforementioned analysis assumes continuous capacitor voltage mode (CCVM) operation for all converters. However, when the flying capacitor voltage ripples are significantly large, reverse conduction in the switching devices can lead to capacitor voltage clamping, driving the converter into discontinuous capacitor voltage mode (DCVM) [64]. In DCVM, automatic inductor current balancing can no longer be maintained. Instead, a modified duty cycle strategy must be employed to restore inductor current balancing. A detailed discussion of the DCVM operation of hybrid SC topologies is beyond the scope of this paper but can be found in [64].

In addition, it is worth noting that the overall converter volume includes not only the passive component volume but also the volume of power switches, their associated gate drive circuitry, and the printed circuit board (PCB). Although passive components typically dominate the overall converter volume, the size of power switches, gate drive circuitry, and PCB can become considerable as the SC stage conversion ratio increases, since a larger SC stage conversion ratio necessitates a higher-order SC network, which requires more power switches, additional gate drive circuitry, and a larger PCB area. While this theoretical work aims to analyze the required passive component volume for each topology as a key indicator of achievable power density, the volume of power switches, gate drive circuitry, and PCB should not be entirely overlooked when evaluating practical converter designs.

D. Analysis of Normalized Total Inductor Current Slew Rate

Fig. 10 presents the normalized falling and rising slew rates ($\widehat{SR}_F$ and $\widehat{SR}_R$) of the total inductor current for different topologies against their SC stage conversion ratio (K_{SC}).

As can be seen in Fig. 10(a), the normalized total inductor current falling slew rate ($\widehat{SR}_F$) increases with the SC stage conversion ratio (K_{SC}), which implies that a larger K_{SC} is favorable for better load step-down transient performance. This is because as K_{SC} increases, the inductor value required to maintain the same current ripple ratio (α_I) is reduced, as shown in (9). The magnitude of the voltage applied across the inductors during an optimally-controlled load step-down transient, as illustrated in Fig. 5, remains constant at the output voltage (V_{out}), regardless of either the circuit topology or K_{SC}. Consequently, benefiting from a reduced inductor value, a regulated hybrid SC topology with a larger SC stage conversion ratio (K_{SC}) can achieve faster load step-down transient response. In addition, it is not surprising that the $\widehat{SR}_F$ of all topologies fall on the same trend line, since the only topology-dependent parameter in (29) is K_{SC}.

Fig. 10(b) depicts how the normalized total inductor current rising slew rate ($\widehat{SR}_R$) of different topologies change with their SC stage conversion ratios (K_{SC}). In general, the $\widehat{SR}_R$ of these regulated hybrid SC topologies decreases with a larger K_{SC}, meaning slower dynamic response. This is mainly because an increased K_{SC} leads to a decrease in V_{buck}, which is applied to the inductors during the load step-up transient to ramp up the inductor current. Although the inductor value in the buck-type stage reduces as K_{SC} increases, which helps improve the load step-up transient

performance, the inductor size reduction does not offset the impact of a lower $V_{\rm buck}$ voltage.

Moreover, many of these regulated hybrid SC topologies have an upper limit on the duty ratio of the buck-type stage that is lower than 100%. The maximum duty ratio ($D_{\max}$) of each topology is listed in Table 4. This constraint on the duty ratio limits the maximum average voltage applied to the inductors during a load step-up transient, which reduces the current rising slew rate. For example, as mentioned earlier in Section IV-B, the maximum duty ratio of a SCB converter with multi-phase operation is $\frac{1}{N}$, where N is the number of branches, and that of a SCB converter with two-phase operation is $\frac{1}{2}$. Benefiting from the extended duty ratio enabled by the two-phase operation, the SCB with two-phase operation achieves a faster current rising slew rate and improved load step-up performance compared to the SCB with multi-phase operation, as demonstrated in Fig. 10(b). The SBC also achieves improved load step-up transient performance through two-phase operation due to the same reason. Additionally, since the buck-type stage of the LEGO topology is a conventional multi-phase buck converter, the LEGO topology can operate at a duty ratio of 100% and thus achieve a much higher $\widehat{\rm SR}_{\rm R}$ compared to other hybrid SC topologies with a maximum duty ratio less than 100%.

One noticeable difference between Fig. 10(a) and Fig. 10(b) is that $\widehat{\rm SR}_{\rm R}$ is typically larger than $\widehat{\rm SR}_{\rm F}$. This is mainly because the magnitude of the average voltage applied to the inductors during a load step-up transient ($D_{\max}V_{\rm buck}$, as shown in (31)) is typically higher than that during a load step-down transient ($V_{\rm out}$). For a 12-V-to-1-V buck converter, the inductor current rising slew rate is 11 times faster than its falling slew rate, meaning that the step-down transient is typically much worse than the step-up transient. Therefore, in the design of existing multi-phase-buck-based VRMs, the step-down transient is usually the primary concern [55]. In contrast, regulated hybrid SC topologies offer the opportunity to equalize the rising and falling slew rates of the total inductor current, which balances the load step-up and step-down transient performances. This can be achieved by matching the normalized falling and rising slew rates ($\widehat{\rm SR}_{\rm F}$ and $\widehat{\rm SR}_{\rm R}$) shown in (35) and (36) (i.e., $\widehat{\rm SR}_{\rm F} = \widehat{\rm SR}_{\rm R}$), which yields

$$K_{\rm SC} = \frac{1}{2} D_{\max} K_{\rm tot}. \tag{48}$$

For example, a SC stage conversion ratio of $K_{\rm SC} = 12$ enables the SCB with two-phase operation [2], the SBC [25], [26], [27], [28], and the DIH [4], [5] and SDIH [13], [14] topologies to equalize $\widehat{\rm SR}_{\rm F}$ and $\widehat{\rm SR}_{\rm R}$ and achieve balanced step-up and step-down transient performances.

E. Summary of Comparative Performance Analysis

The conclusions from this comparative performance analysis can be summarized as follows:

- Increasing the SC stage conversion ratio decreases the normalized switch stress, which is beneficial for lowering power losses and achieving higher efficiency. The maximum achievable SC stage conversion ratio is limited by $K_{\rm SC} < D_{\max} K_{\rm tot}$.
- Increasing the SC stage conversion ratio typically reduces the normalized passive component volume (assuming the used capacitors have greatly superior energy densities compared to those of inductors), which is favorable for converter miniaturization and achieving higher power density.
- A larger SC stage conversion ratio speeds up the falling slew rate of the total inductor current, which improves load step-down transient performance. Conversely, a larger SC stage conversion ratio slows down the rising slew rate of the total inductor current, leading to slower load step-up dynamic responses. However, regulated hybrid SC topologies offer the opportunity to achieve balanced load step-up and step-down transient performances when $K_{\rm SC} = \frac{1}{2} D_{\max} K_{\rm tot}$.

V. Conclusion

This article proposed an analytical framework for comparing the performance of 48-V-to-PoL regulated hybrid SC topologies. In this framework, a regulated hybrid SC topology is depicted as a fixed-ratio SC stage merged with a subsequent regulated buck-type stage. The total conversion ratio is allocated between these two conversion stages. Three metrics are defined and calculated for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. Through comprehensive comparative analysis, this framework reveals the benefits of a larger SC stage conversion ratio: increasing the SC stage conversion ratio reduces switch stress and passive component volume while accelerating the falling slew rate of the total inductor current, thereby improving efficiency, power density, and load step-down transient performance simultaneously. Although a larger SC step-down ratio typically slows down the rising slew rate of the total inductor current, which can potentially impair the load step-up transient performance, properly designed regulated hybrid SC topologies can achieve balanced load step-up and step-down transient performances with similar rising and falling slew rates of the total inductor current.

Appendix A
Characteristic Vectors of State-of-the-Art 48-V-to-PoL Regulated Hybrid SC Topologies

Table 6 lists the characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature, including switch voltage stress vector $\widehat{\mathbf{V}}_{\rm ds}$, switch current stress vector $\widehat{\mathbf{I}}_{\rm d(rms)}$, capacitor voltage vector $\widehat{\mathbf{V}}_{\rm C}$ and capacitor charge vector $\widehat{\mathbf{q}}_{\rm C}$.

TABLE 6. Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\widehat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\widehat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
Switching bus converter (SBC) [25], [26], [27], [28]	$K_{SC} \in \{4k \mid k \in \mathbb{N}, 1 \le k \le 6\}$ $[N_S \quad N_L \quad N_C] = [2K_{SC}+2 \quad K_{SC} \quad K_{SC}-1]$	$\frac{1}{K_{SC}} \begin{bmatrix} \frac{K_{SC}}{2} \\ \frac{K_{SC}}{2}+1 \\ \frac{K_{SC}}{2}-1 \\ \frac{K_{SC}}{2} \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \\ \\ \\ \\ \\ \} K_{SC}-2 \\ \\ \} K_{SC} \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \\ \\ \} K_{SC}+2 \\ \\ \\ \} K_{SC}-2 \\ \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} \frac{K_{SC}}{2} \\ 1 \\ 1 \\ 2 \\ 2 \\ \vdots \\ \frac{K_{SC}}{2}-1 \\ \frac{K_{SC}}{2}-1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_C$
SCB [1], [2]	• Multi-phase operation [1]: $K_{SC} \in \{k \mid k \in \mathbb{N}, 2 \le k \le 6\}$ • Two-phase operation [2]: $K_{SC} \in \{2k \mid k \in \mathbb{N}, 1 \le k \le 12\}$ $[N_S \quad N_L \quad N_C] = [2K_{SC} \quad K_{SC} \quad K_{SC}-1]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \\ \\ \\ \} K_{SC}-1 \\ \\ \\ \} K_{SC}-1 \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \\ \\ \\ \} K_{SC}-1 \\ \\ \\ \} K_{SC}-1 \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ N_C \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_C$
Dickson[2] [24]	$K_{SC} = 9$ $[N_S \quad N_L \quad N_C] = [22 \quad 9 \quad 8]$	$\frac{1}{K_{SC}} \begin{bmatrix} 3 \\ 3 \\ 3 \\ 6 \\ 4 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \\ \\ \\ \\ \\ \\ \} 8 \\ \\ \} 9 \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \\ \\ \\ \} 13 \\ \\ \} 6 \\ \\ \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} 6 \\ 3 \\ 2 \\ 2 \\ 2 \\ 1 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_C$
CaSP [15]	$K_{SC} = 6$ $[N_S \quad N_L \quad N_C] = [11 \quad 3 \quad 3]$	$\frac{1}{K_{SC}} \begin{bmatrix} 3 \\ \vdots \\ 3 \\ 2 \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \\ \\ \} 5 \\ \\ \\ \} 4 \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D/2} \\ \vdots \\ \sqrt{D/2} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \\ \\ \} 4 \\ \\ \\ \} 4 \\ \\ \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$
MLB [9], [10]	$K_{SC} = 8$ $[N_S \quad N_L \quad N_C] = [10 \quad 2 \quad 3]$	$\frac{1}{K_{SC}} \begin{bmatrix} 4 \\ \vdots \\ 4 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{bmatrix} \begin{matrix} \\ \\ \} 4 \\ \\ \\ \} 4 \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D/2} \\ \vdots \\ \sqrt{D/2} \\ \sqrt{D/2} \\ \sqrt{D/2} \\ \sqrt{D/2} \\ \sqrt{D} \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \\ \\ \} 4 \\ \\ \\ \\ \\ \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} 4 \\ 2 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$

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TABLE 6. (continued) Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $\begin{bmatrix} N_{\mathrm{S}} & N_{\mathrm{L}} & N_{\mathrm{C}} \end{bmatrix}$	$\widehat{\mathbf{V}}_{\mathrm{ds}} \in \mathbb{R}^{N_{\mathrm{S}} \times 1}$	$\widehat{\mathbf{I}}_{\mathrm{d(rms)}} \in \mathbb{R}^{N_{\mathrm{S}} \times 1}$	$\widehat{\mathbf{V}}_{\mathrm{C}} \in \mathbb{R}^{N_{\mathrm{C}} \times 1}$	$\widehat{\mathbf{q}}_{\mathrm{C}} \in \mathbb{R}^{N_{\mathrm{C}} \times 1}$
LEGO* [7], [8] Mini-LEGO* [18], [19]	$K_{\mathrm{SC}} = 6$ $\begin{bmatrix} N_{\mathrm{S}} & N_{\mathrm{L}} & N_{\mathrm{C}} \end{bmatrix} = \begin{bmatrix} 40 & 12 & 5 \end{bmatrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \} 4 \\ \\ \\ \} 36 \end{matrix}$	$\frac{1}{N_{\mathrm{L}}} \begin{bmatrix} \sqrt{2D} \\ \vdots \\ \sqrt{2D} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1-D} \\ \vdots \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \} 16 \\ \\ \\ \} 12 \\ \\ \\ \} 12 \end{matrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 5 \\ 4 \\ 3 \\ 2 \\ 1 \end{bmatrix}$	$\frac{7D}{N_{\mathrm{L}}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_{\mathrm{C}}$
VIB [20], [21]	$K_{\mathrm{SC}} = 8$ $\begin{bmatrix} N_{\mathrm{S}} & N_{\mathrm{L}} & N_{\mathrm{C}} \end{bmatrix} = \begin{bmatrix} 40 & 16 & 15 \end{bmatrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 4 \\ \vdots \\ 4 \\ 1 \\ \vdots \\ 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \} 8 \\ \\ \\ \} 4 \\ \\ \\ \} 12 \\ \\ \\ \} 16 \end{matrix}$	$\frac{1}{N_{\mathrm{L}}} \begin{bmatrix} \sqrt{D/2} \\ \vdots \\ \sqrt{D/2} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \vdots \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \} 8 \\ \\ \\ \} 16 \\ \\ \\ \} 12 \\ \\ \\ \} 4 \end{matrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 6 \\ 3 \\ 2 \\ 2 \\ 2 \\ 1 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_{\mathrm{L}}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_{\mathrm{C}}$
MSC [22], [23]	$K_{\mathrm{SC}} = 8$ $\begin{bmatrix} N_{\mathrm{S}} & N_{\mathrm{L}} & N_{\mathrm{C}} \end{bmatrix} = \begin{bmatrix} 18 & 8 & 7 \end{bmatrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 4 \\ 5 \\ 3 \\ 4 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \} 6 \\ \\ \\ \\ \\ \\ \} 8 \end{matrix}$	$\frac{1}{N_{\mathrm{L}}} \begin{bmatrix} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{bmatrix} \begin{matrix} \} 10 \\ \\ \\ \} 6 \\ \\ \\ \\ \\ \end{matrix}$	$\frac{1}{K_{\mathrm{SC}}} \begin{bmatrix} 4 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \\ 3 \end{bmatrix}$	$\frac{D}{N_{\mathrm{L}}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_{\mathrm{C}}$

* The normalized accumulative charge vector $\widehat{\mathbf{q}}_{\mathrm{C}}$ for the LEGO [7], [8] and Mini-LEGO [18], [19] topologies listed in this table is only applicable to the scenario where the switching frequency of the buck units switch is 3.5 times faster than that of the SC units, as implemented in [7], [8], [18], [19].

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TABLE 6. (continued) Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\widehat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\widehat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
Crossed-coupled QSD buck [12]	$K_{SC} = 4$ $[N_S \quad N_L \quad N_C] = [8 \quad 2 \quad 3]$	$\frac{1}{K_{SC}} \begin{bmatrix} 2 \\ \vdots \\ 2 \\ 3 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \begin{matrix} \} 4 \\ \\ \\ \\ \} 3 \end{matrix}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D}/2 \\ \vdots \\ \sqrt{D}/2 \\ \sqrt{1+D/4} \\ \sqrt{1+D/4} \end{bmatrix} \} 6$	$\frac{1}{K_{SC}} \begin{bmatrix} 2 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$
DIH [4], [5]	$K_{SC} \in \{2k \mid k \in \mathbb{N}, 2 \le k \le 12\}$ $[N_S \quad N_L \quad N_C] = [K_{SC}+2 \quad 2 \quad K_{SC}-1]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{bmatrix} \} K_{SC}-1$	$\frac{1}{N_L} \begin{bmatrix} 2\sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ 2\sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ 2\sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \vdots \\ 2\sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \end{bmatrix} \} K_{SC}-2$	$\frac{1}{K_{SC}} \begin{bmatrix} K_{SC}-1 \\ K_{SC}-2 \\ \vdots \\ 1 \end{bmatrix}$	$\frac{2D}{N_L K_{SC}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_C$
SDIH [13], [14]	$K_{SC} \in \{2k \mid k \in \mathbb{N}, 2 \le k \le 12\}$ $[N_S \quad N_L \quad N_C] = [2K_{SC}+2 \quad 2 \quad 2K_{SC}-2]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{bmatrix} \} 2K_{SC}-2$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ \vdots \\ \sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ \sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \vdots \\ \sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \end{bmatrix} \begin{matrix} \} 4 \\ \\ \\ \} 2K_{SC}-4 \\ \\ \\ \end{matrix}$	$\frac{1}{K_{SC}} \begin{bmatrix} K_{SC}-1 \\ K_{SC}-1 \\ K_{SC}-2 \\ K_{SC}-2 \\ \vdots \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L K_{SC}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \} N_C$

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