Title

"FlexTrate^TM" - Scaled Heterogeneous Integrationon Flexible Biocompatible Substrates using FOWLP

Authors

Fukushima, Takafumi
Alam, Arsalan
Wan, Zhe
et al.

Publication Date

2017-06-01

Peer reviewed

"FlexTrate™" - Scaled Heterogeneous Integration on Flexible Biocompatible Substrates using FOWLP

Takafumi Fukushima [1,2], Arsalan Alam[1], Zhe Wan[1], Siva C. Jangam[1], Saptadeep Pal[1], Goutham Ezhilarasu[1], Adeel Bajwa[1], and Subramanian S. Iyer[1]

1 Center for Heterogeneous Integration and Performance Scaling (CHIPS), EE Dept. UCLA, Los Angeles, USA,
e-mail: s.s.iyer@ucla.edu

2 Department of Mechanical Systems Engineering, Tohoku University, Sendai, Miyagi, Japan
fukushima@lbc.mech.tohoku.ac.jp
takfukushima@ucla.edu

***Abstract*— We have developed a novel fan-out wafer level packaging (FOWLP) technology for high-performance and scalable flexible and biocompatible substrates that we call FlexTrate™. We demonstrate the technology with the assembly of 1-mm-sqaure 625 (25 by 25) Si dielets on a biocompatible Polydimethylsiloxane (PDMS). By using the new FOWLP technology, die-die interconnects with a pitch of 10 μm or less were implemented on the array of the Si dielets embedded in the PDMS.**

Keywords-Flexible device integration, Biocompatible, FOWLP, Bendable interconnect, Metallization of PDMS

I. INTRODUCTION

Flexible electronics have been increasingly important in IoT, wearable, and medical applications. Roll-to-roll sheet-level processing including additive printable techniques is highly expected for flexible device fabrication. However, the large-area sheet processes cause serious size deformation and the resulting alignment errors [1]. Therefore, high-performance device fabrication and high-density interconnect formation are still challenging for the industrial use of the flexible devices. On the other hand, semiconductor packaging is undergoing a renascence with the adoption of wafer-level Si processing to integrate both single and multi-dies using FOWLP. Its variants on rigid substrates greatly increases both connectivity and form factor compared with classical laminate based packaging. We propose a new flexible FOWLP technology to fabricate highly integrated (biocompatible) flexible substrates called FlexTrate™ which allows much tighter interconnects than that fabricated in roll-to-roll and sheet-level processing. FlexTrate™ leverages flexible substrates as well as "dielets" that are small dies and semi-rigid (not extremely thinned). Although inorganic single crystalline semiconductor wafers/dielets are typically rigid, extremely thin dies show a flexible property. However, bending of the dies gives high mechanical stress to the devices, resulting in degradation of their performance [2]. FlexTrate™ is similar to a chain link concept where the links themselves have some flexibility as depicted schematically in one dimension in Fig. 1. Heterogeneous dielets are embedded in a flexible substrate and they are electrically connected with high-density interconnects formed by wafer-level processing. No wire bonding and solder bumping are required to integrate this flexible system consisting of the semi-rigid inorganic dielets and flexible polymeric substrates. The use of organic semiconductors and printable wirings are optional.

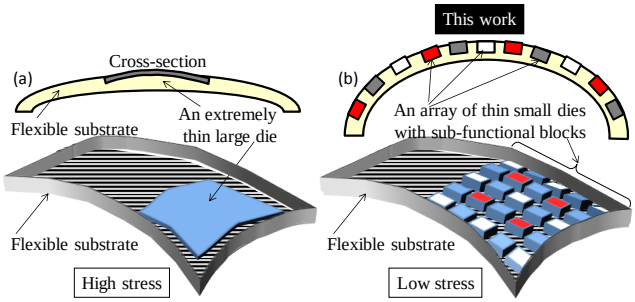

Fig. 1 Configuration of single crystalline dies embedded in a flexible substrate: extremely thin/large die (left) and thin/small dielets array (right) based on FOWLP.

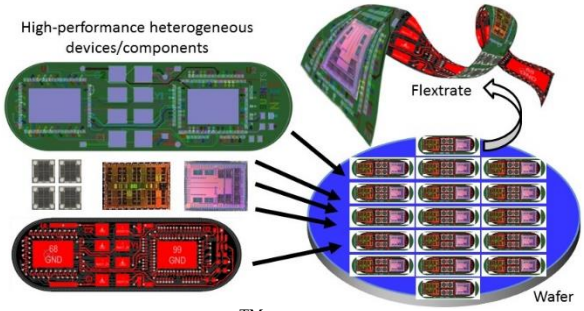

Fig. 2 Concept of FlexTrate™: a new high-performance & scalable flexible device heterointegration based on wafer-level processing.

Fig. 2 shows the concept of our FlexTrate™ technology where thinned heterogeneous dielets are integrated using FOWLP processes on a flexible substrate. We limit the die size to at most a few mm on a side to aid the flexible link concept [3]. The dielets are created by system-level partitioning of SoCs into their component modules. These thinned dies flex a bit but the space between the links can flex more. The smaller thinner die can follow the flexure with low stress and less total warpage. This helps in minimizing stress-

induced performance impact on devices on these dies compared with large dies on flexible substrates. In addition, nowadays, small dies such as sensors, laser diodes, μ-LEDs, and passives are required for heterogeneous system integration, and also have the advantage of higher yield.

In the present study, we demonstrate a new flexible FOWLP processes including multichip assembly/transfer from a handler wafer to another handler. Based on wafer-level processing, we evaluate the feasibility of the FlexTrate™ processes and characterize fine-pitch wirings formed on a biocompatible PDMS as a flexible substrate in which hundreds of 1-mm-sqaure small dies are embedded and interconnected.

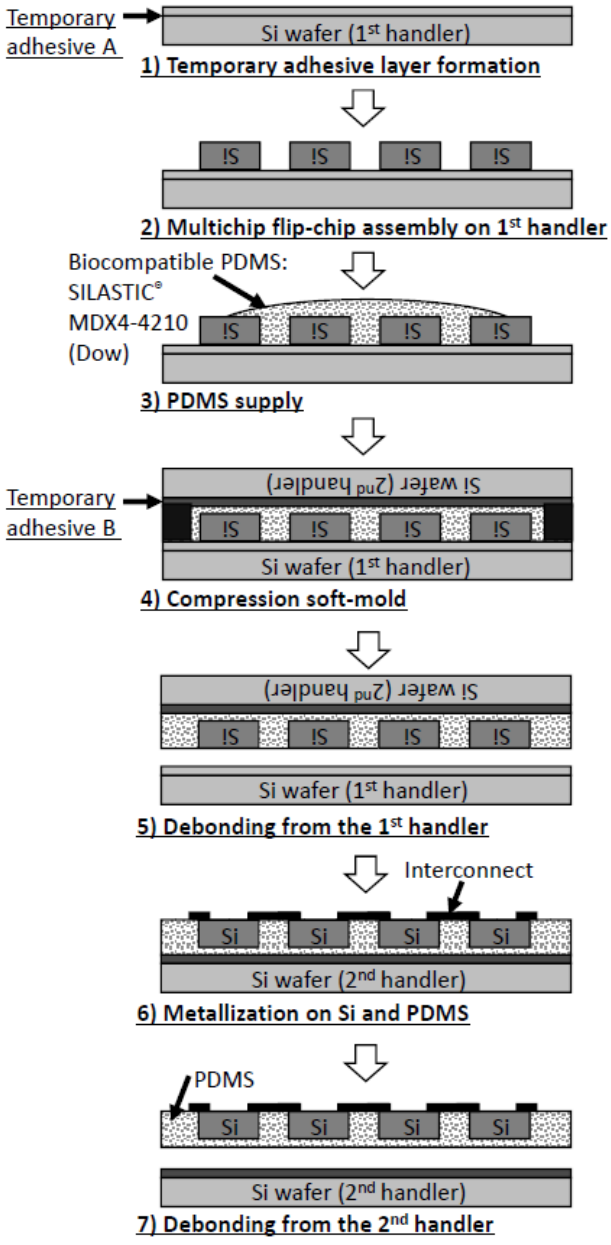

Fig. 3 A process flow of FlexTrate™ fabrication using flexible FOWLP with a biocompatible PDMS.

II. Experimental

A. *Flexible FOWLP process*

Fig. 3 shows a process flow for the FlexTrate™ using flexible FOWLP technologies. First, a temporary adhesive layer was formed on a first Si handler. Then, small dielets were precisely self-assembled, active side down, on the adhesive surface of the handler. After that, a biocompatible PDMS was applied on the multichip-on-wafer structure, followed by curing and compression soft-mold with a second silicon handler having another temporary adhesive layer. After multichip transfer from the first handler to the second handler, metallization processes were performed on the array of the Si dielets and the surrounding PDMS at the wafer-level. Prior to the metallization processes, a key process "stress buffer layer formation" was inserted in the new FOWLP scheme. The high-reliable fabrication of bendable wirings on high-CTE soft materials like PDMSs was allowed by the formation of a thin stress buffer layer. Finally, the FlexTrate™ was thermally removed from the second handler to yield the heterogeneous multi-die assembly process on flexible substrates.

B. *Biocompatible PDMS*

The thermomechanical and electrical characteristics of the biocompatible PDMS "Silastic MDX4-4210 (Dow)" are summarized in Table 1. The PDMS shows good electrical properties such as low dielectric constant, low dissipation factor, and high breakdown voltage as well as typical epoxy resins used in FOWLP like InFO technology [4]. However, this material has high CTE with respect to both Si and Cu (300 vs. 3 and 17 ppm). However, since the glass transition temperature and Young's modulus are very low, the resultant structure induces low-stress over the entire FlexTrate™ with minimal global wafer bow. In addition, the PDMS is thermally stable at 200 ° C or above. The biocompatible PDMS consisting of a base resin and a curing agent was uniformly mixed and defoamed with a planetary centrifugal mixer (THINKY, ARE-310) prior to compression soft-molding.

Table 1 Properties of a biocompatible PDMS.

Properties	SILASTIC® MDX4-4210
Hardness	30 (Shore A)
Tensile strength	5 (MPa)
Elongation at break	~500%
Dielectric constant @ 100kHz	3.0 (3.01@100Hz)
Dissipation factor @ 100KHz	0.001 (0.0009@100Hz)
Volume resistivity	2×10^{15} (Ω·cm)
CTE	~300 (ppm/K)
Young modulus	0.5 (MPa)
Tg	-120 (℃)
Thermal decomposition temp.	200 (℃) or more
Screening test for implant	Passed up to 29 (days)

III. Results and Discussion

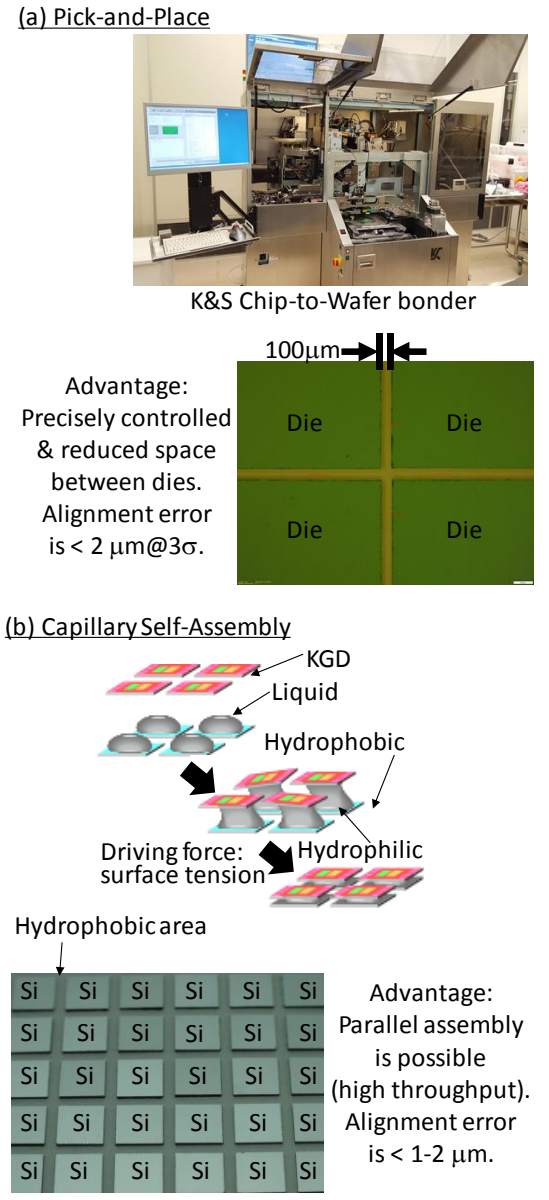

Fig. 4 Multi-die placement by a commercially available CtW flip-chip bonder (a) and capillary self-assembly (b).

As shown in Fig. 4(a), a flip-chip bonder (KNS, APAMA) can precisely align dielets and place them with precision on the temporary adhesive layer formed on the first Si handler. By optimizing the sequential assembly conditions, high alignment accuracies within 3σ of ±2 μm are obtained. The space between assembled dielets can be well controlled by this assembly approach. On the other hand, the massively parallel capillary self-assembly of dielets can be also applied in this process. This self-assembly technology can solve a serious tradeoff between assembly throughput and accuracy. As shown in Fig.4 (b), the surface tension of water droplets drives large numbers of dielets and accurately places them at once on a temporary adhesive layer. High alignment accuracies are obtained within 1-2 μm by conditioning the key parameters such as die size accuracy, pre-alignment position, liquid volume, and wettability contrast between hydrophilic assembly areas and the surrounding hydrophobic region [5].

By using the flexible FOWLP technology, dielets having different height can be assembled face-down on a temporary adhesive layer formed on handlers, and their top surfaces flipped them are planarized/levelled by low-temperature compression mold with PDMS as shown in Fig. 5 (a). In Figs. 5 (b) and (c), different dies ranging in thickness from 100 μm to 775 μm are self-assembled on the host handlers. There is a tradeoff between the interconnect performance (wire length) and flexure limits – greater inter-die spaces having longer wires have greater flexural stability. We can compensate for wire resistance by increasing interconnect wire width.

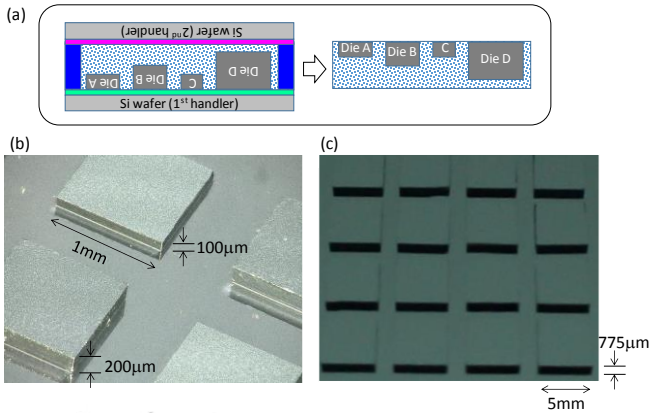

Fig. 5 Hetero integration of multi-dies with various thickness (a)-(c).

Fig. 6 shows a surface profile of the adjacent dielets placed on the first temporary adhesive layer. Here, we use 100-μm-thick 1-mm-square Si dielets with a total thickness variation (TTV) of 1.5 μm. These dies are kindly provided from GINTI (Tohoku Univ./T-Micro). As seen from this figure, there is very small die tilt. The maximum height difference among the Si dies is approximately 1.5 μm, similar to the dielet TTV values. After compression mold with the PDMS, the small die array is transferred to the second Si handler, followed by the debonding of the first handler. The surface profiles are evaluated in the following figures: Fig. 7 shows the impact of curing temperature on the coplanarity of Si dies and height gap among the Si and PDMS top surfaces, whereas Fig. 8 shows the effect of adhesive thickness on the geometrical properties. As seen from Fig. 7, the height gap is gradually reduced with the decrease in curing temperature. This is probably due to diminished Brownian motion of the PDMS backbones used as a mold resin because the glass transition temperature of the PDMS is much below room temperature. On the other hand, as seen from Fig. 8, a thinner adhesive layer (10μm) can further reduce the height gap down to 1 μm whereas a thicker adhesive layer (50μm) enlarges the gap. Although the edges of the dielets show locally high topography, these embossments result from low adhesion

between the temporary adhesive and Si dielets, leading to infiltration of the uncured PDMS. However, the small embossments can be further compensated with a spin-on passivation layer prior to metallization processes. In this work, two measures of co-planarity are defined: one is the maximum distance between the highest and lowest point of all the dies embedded on the PDMS. The other is defined as the gap between the highest and lowest point of each die. The former coplanarity is 1.3 μm at most, and is not affected by curing temperature and adhesive thickness. The latter co-planarity is found to be < 1 μm. Due to the low-temperature compression mold process, a big concern regarding die shift as seen in typical FOWLP using rigid resins can be also suppressed.

In addition to die shift, the wafer bow is quite small compared with typical FOWLP using rigid epoxies. Fig. 9 shows a line profile of the array of the 1-mm-square dielets embedded in the transparent PDMS. Due to the low curing temperature, Young's modulus, and glass transition temperature of the biocompatible PDMS, the wafer bow is approximately 50 μm in a 4-inch wafer, as shown in Fig. 9. Both the die shift and wafer bow was optically evaluated with a surface metrology systems (cyberTECHNOLOGIES, CT100) equipped with confocal white light.

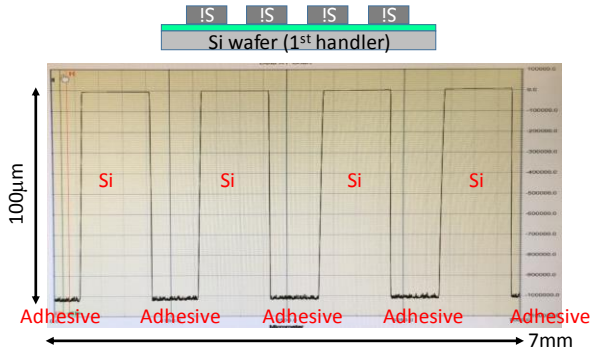

Fig. 6 A surface profile of multi-dies placed on the 1st temporary adhesive formed on the 1st Si handler.

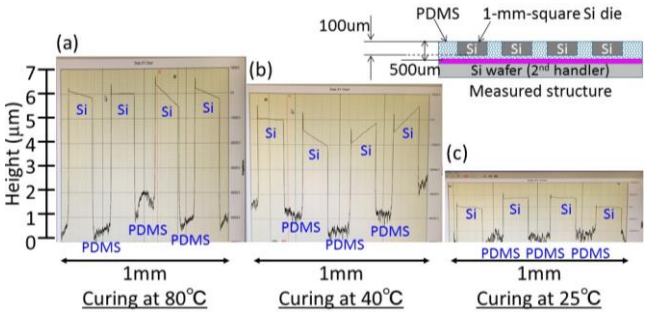

Fig. 7 Impact of curing temperature on surface profiles of Si/PDMS after transfer to the 2nd temporary adhesive (Si handler).

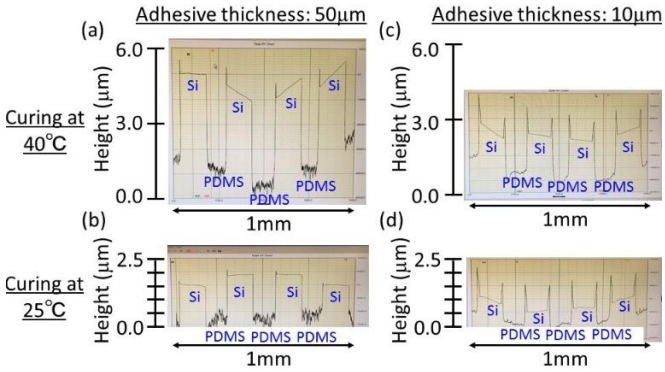

Fig. 8 Impact of the 1st adhesive thickness on surface profiles of Si/PDMS after transfer to the 2nd temporary adhesive (Si handler).

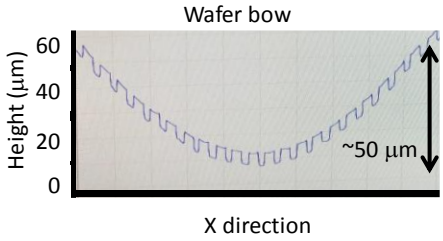

Fig. 9 An optically measured surface profile of 625 piece of Si dies and PDMS after transfer to the 2nd temporary adhesive (Si handler).

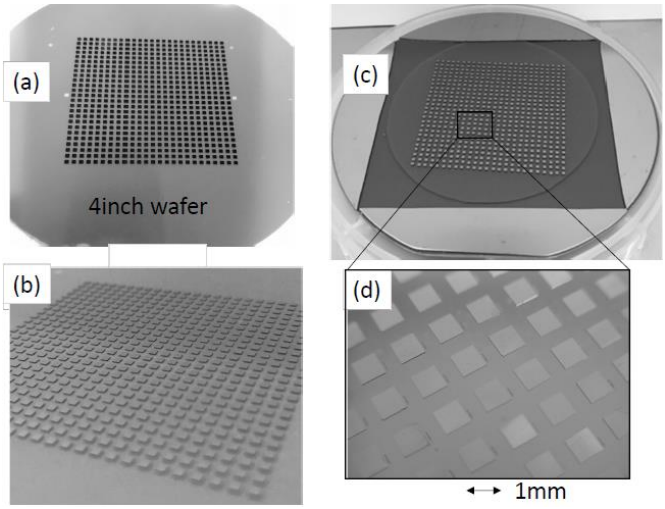

Fig. 10 Photomicrographs of 1-mm-square multi-dies placed on the 1st Si handler (die pitch: 1.8 mm): top view (a) and bird-eye view (b). Photomicrographs of 1-mm-square multi-dies transferred to the 2nd Si handler: top view (c) and magnified bird-eye view (d).

As shown in Fig. 10, 625 square 1mmx1mm dielets were assembled on the first Si handler, and were successfully transferred to the second handler. Then, the metallization with evaporated Cr/Au or Ti/Au is performed on the PDMS and Si dielets covered with an oxide layer. Surface modification was carried out to enhance the adhesion between the metal and PDMS. By using a UV/O_3 treatment, the water contact angle is dramatically decreased, and consequently, the surface is rendered highly hydrophilic as shown in Fig. 11. These

hydrophilic surfaces can increase the adhesion strength between the metal and PDMS as seen from picture insets in Fig. 11.

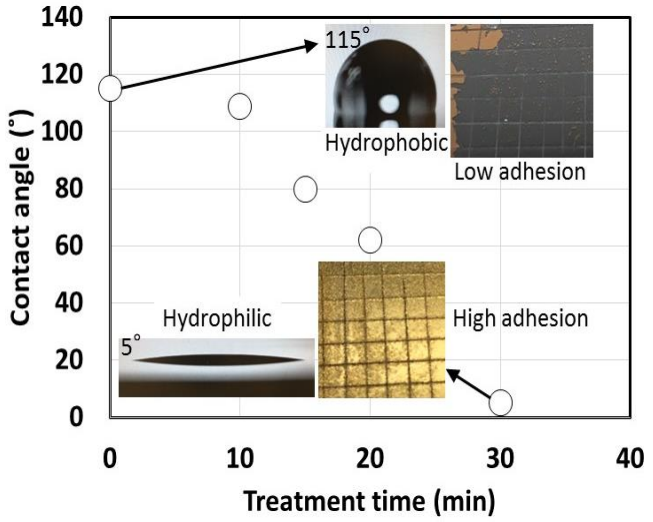

Fig. 11 Water contact angle shift on the bare biocompatible PDMS as a function of surface modification time with UV/O_3, and their adhesion properties with Ti/Au.

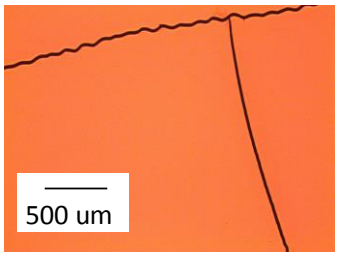

Fig. 12 A photomicrograph of large cracks formed on a pre-baked photoresist after cooling: the photoresist is coated on a Ti/Au layer directly deposited on the biocompatible PDMS without a stress buffer layer.

However, the serious CTE mismatch between the metals and PDMS makes it difficult for FlexTrate™ to photolithographically form fine-pitch wirings. Typical photoresists cannot endure the high thermal stress applied when cooling after the prebaking step. Consequentially, large cracks are generated on the photoresist surface as shown in Fig. 12. Thus, we propose the use of a stress buffer layer between the metals and PDMS. As a result, Ti/Au wirings with the stress buffer layer are electrically connected between the adjacent dielets as shown in Fig.13. Furthermore, 8-μm-pitch Ti/Au wirings with a line/space of 3.6/4.4 μm can be also successfully formed on the biocompatible PDMS using wet etching techniques without any damages such as cracks and delamination. The electrical properties of the Ti/Au wirings were shown in Fig. 14. The resulting resistance is proportional to the wire length. The theoretical value of the 100-nm-thick/10-mm-long/18-μm-wide Au wiring is 122 Ω, which is nearly 60% of the measured resistances. As seen from Fig. 15, good electrical properties were obtained after bending with a curvature radius of 2.5 mm. The resistivity of the 1.8-mm-long Ti/Au wirings with a thickness of 10/100 nm was approximately 134 Ω and 148 Ω before and after bending, respectively. The increase in resistance is found to be nearly 10% after bending. Finally, the FlexTrate™ is removed from the second handler. As shown in Fig. 16, the flexible substrate embedding a large number of 100-μm-thick/1-mm-sqaure Si dies in the biocompatible PDMS is obtained, and can be attached on the curved surfaces such as the human arm.

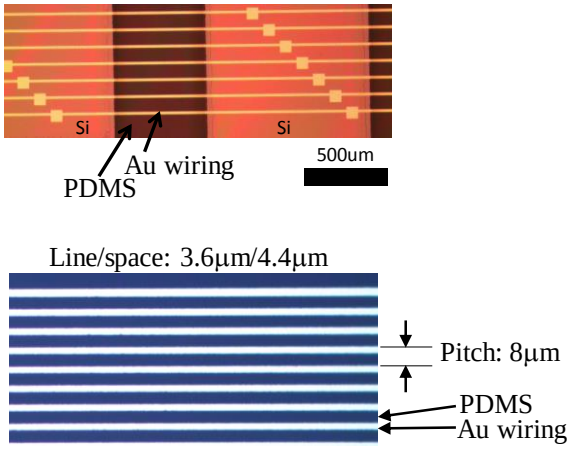

Fig. 13 Optical images of inter-dielet/fine-pitch wirings formed on Si/PDMS in wafer-level processing.

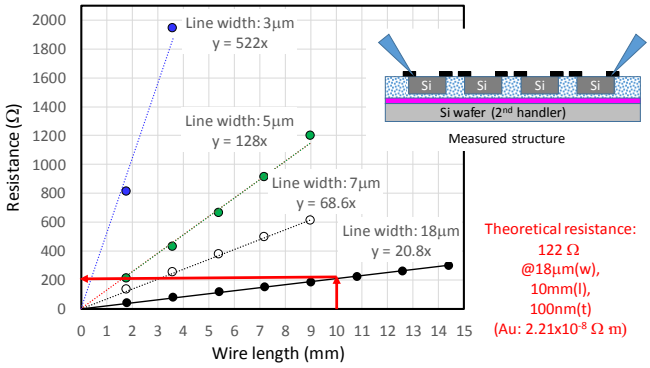

Fig. 14 The relationship between the resistances and wire lengths formed on PDMS before removal from the 2nd handler.

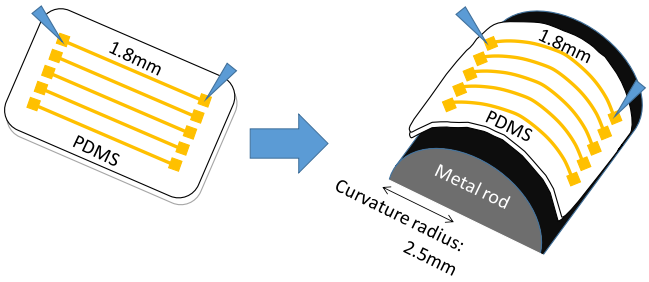

Fig. 15 Resistance measurement of FlexTrate™ before and after bending.

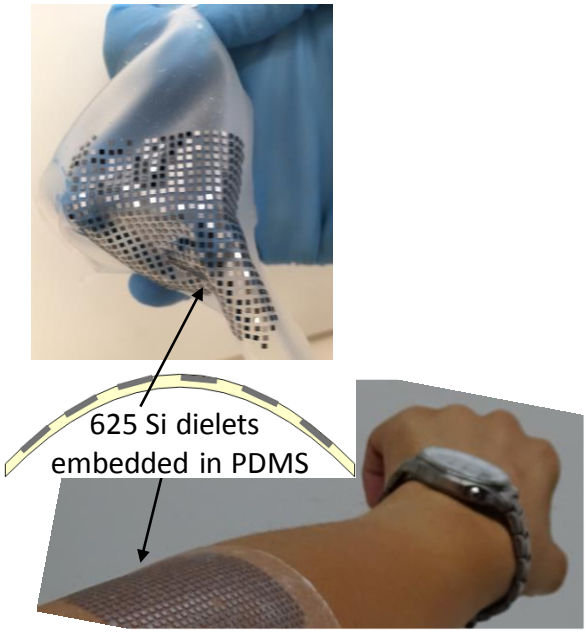

Fig. 16 Pictures of the wearable/implantable demonstrator of FlexTrate™.

IV. Conclusion

We have presented a novel flexible device integration technology to fabricate highly integrated flexible substrates called "FlexTrate™" based on FOWLP. Fine-pitch inter-dielet interconnects were successfully formed on a large number of Si dielets embedded in a biocompatible PDMS. The fabrication of FlexTrate™ was achieved by using multichip assembly, low-temperature compression soft-mold, and multichip transfer technologies. The heterointegration scheme can enable next-generation IoT systems having various sensors and high-density interconnect networks on flexible substrates as well as wearable and implantable devices.

Acknowledgment

The Defense Advanced Research Projects Agency (DARPA) through ONR grant N00014-16-1-263 and the UCLA CHIPS Consortium supported this work. The authors would like to also thank the support from UCOP through grant MRP-17-454999. Part of the experimental work was performed in the Integrated Systems Nanofabrication Cleanroom (ISNC) of California NanoSystem Institute (CNSI) in UCLA and the Nanoelectronics Research Facility (NRF). The authors gratefully acknowledge the support of K&S and staff at ISNC and NRF. The views, opinions and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government. The authors gratefully acknowledge the support of Global INTegration Initiative (GINTI) in Tohoku University, Japan. We also would like to acknowledge Dow Corning and NITTO for their material support and cyberTECHNOLOGIES for their measurement support.

References

[1] K. Jain, M. Klosner. M. Zemel, and S. Raghunandan, "Flexible Electronics and Displays: High-Resolution, Roll-to-Roll, Projection Lithography and Photoablation Processing Technologies for High-Throughput Production", *Proc. IEEE*, vol. 93, pp. 1500-1510, 2005.

[2] K. Lee, S. Tanikawa, M. Murugesan, H. Naganuma, H. Shimamoto, T. Fukushima, T. Tanaka, and M. Koyanagi, "Degradation of Memory Retention Characteristics in DRAM Chip by Si Thinning for 3-D Integration", *IEEE Electron Device Lett*., vol. 34, pp. 1038-1040, 2013

[3] S. S. Iyer, "Heterogeneous Integration for Performance and Scaling", *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, pp. 973-983, 2016.

[4] C.-F. Tseng, C.-S. Liu, C.-H. Wu, and D. Yu, "InFO (Wafer Level Integrated Fan-Out) Technology" *in Proc. 2016 IEEE 66th Electronic Components and Technology Conf. (ECTC)*, pp.1-6.

[5] T. Fukushima and Jicheol Bea, "Chapter 6.6, Self-Assembly-Based 3D and Heterointegration" in Handbook of 3D Integration – Volume 3: 3D Process Technology (Wiley-VCH), Editors: Phil Garrou, Mitsumasa Koyanagi, Peter Ramm, June 2014, pp. 325-334.