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High precision thermal stress study on flip chips by synchrotron polychromatic X-ray microdiffraction

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Abstract

The bending and residual stress of flip chips caused by the mismatch of thermal expansion between the chip and the substrate have been measured by polychromatic micro-focused synchrotron X-ray beam. Precise orientation information as a function of position on the chip was obtained from Laue diffraction patterns, so that the bending angle with respect to a reference position at the center of the chip can be calculated at each position. This in turn allows deducing the local curvature of the entire flip chip. Local stress distribution was then mapped by applying a modified Stoney's stress-strain equation to the measured curvature. Our study shows that thermal stress on the circuits and the solder joints in a flip chip strongly depends on temperature and the distance from the center of the chip, indicating that interconnects at the corner and edge of a flip chip are of reliability concerns.

I. Introduction

Flip chip is the dominant technology in high-end electronic packaging due to its high packaging density, high speed, and low costs [1]. In this technology, Si chips are attached to organic substrates by an array of solder bumps. Several heating and cooling cycles (reflow) are required during the fabrication procedure. The mismatch of the coefficients of thermal expansion (CTE) of Si and organic substrate will cause thermal stress in the flip chips during the reflow. This thermal stress is known to induce failure, especially in the solder joints at the corners of the flip chip [2] and it is one of the major factors limiting the reliability of flip chip devices. To reduce the thermal stress, a substrate material having the same CTE as Si is ideal. Flame Retardant 4 (FR-4) is currently widely used as the substrate. Furthermore, underfill has been induced between the Si chip and the organic substrate to improve the mechanical behaviors of the assembly [3].

The residual stresses have been studied both experimentally [4] and theoretically [5, 6, 7]. The FleXus technique used for the measurement of residual stresses by conventional wafer curvature technique requires the wafer to be at least 3 inch in diameter, and therefore can not be employed in our case where the wafer is less than 1 cm^2. To our knowledge, no high spatial resolution measurements of the stress distribution on flip chips with less than 1 cm^2 area are reported in the literature. In this article, we report the bending and stress distribution on a flip chip sample as obtained by using the synchrotron X-ray microdiffraction technique at room temperature (RT), 50, 75 and 100 ^{o}C [8, 9, 10]. In this technique, a highly brilliant polychromatic X-ray beam produced by a synchrotron radiation source is focused by a pair of Kirkpatrick-Baez mirrors to micron / submicron size. When the microfocused X-ray beam impinges on a crystalline sample where the grain size is bigger than the

1 X-ray beam size, discrete Laue diffraction reflections are produced. With a two-
2 dimensional (2D) X-ray CCD detector Laue diffraction patterns are recorded while
3 the sample is raster-scanned under the microfocused X-ray beam. Laue patterns
4 contain a wealth of information, including phase distribution, crystal orientation,
5 elastic strain / stress, and dislocation densities [11, 12]. The spatial resolution of this
6 technique is only limited by the X-ray spot size and scanning step size.
7

8 ## II. Experimental

9 The Si flip chip used in this study has an area of about 7.6 mm × 7.6 mm, and a
10 thickness of about 750 μm and has the (100) face parallel to the chip surface. The
11 composition of the solder balls is eutectic Sn-Pb, and their dimensions are about 80
12 μm (height) by 90 μm (contact opening). The trilayer thin films of the under bump
13 metallurgy (UBM) on the chip side are Al (~0.3 μm) / Ni (V) (~0.3 μm) / Cu (~0.7
14 μm). On the substrate side, the bond-pad metal layers are Ni (5 μm) / Au (0.05 μm).
15 The substrate is a 320 μm thick FR-4 board, and the length of its side is 2.7 cm [13].
16 The flip chip sample was glued on the substrate side to a copper plate, so that the Si
17 chip was on the top. A copper cartridge heater was clamped under the copper plate,
18 as shown in Figure 1 (a). The dimensions of the copper plate are 3.4 cm × 3.4 cm ×
19 0.9 cm. Its area is thus much larger than the flip chip sample, ensuring a uniform
20 heating of the sample. To measure the bending and stress evolution, the sample was
21 heated to 50 ^{o}C, 75 ^{o}C and 100 ^{o}C. The temperature of the cartridge heater was
22 controlled within an accuracy of ± 2 ^{o}C.
23 The microdiffraction experiment was conducted on Beamline 12.3.2 at the
24 Advanced Light Source (ALS) in Lawrence Berkeley National Laboratory (LBNL)
25 [14]. The energy range of the X-ray beam on this beamline is about 5 keV to 24 keV.

The X-ray beam size was about 1 μm^2 at the focal point. The flip chip sample together with the whole heating system was mounted on the sample stage and tilted by 45° with respect to the incident beam [15]. Three cross-lines at the center of the Si chip were scanned each in horizontal and vertical directions with 10 μm step size and 0.4 sec exposure time as shown schematically by the red dashed lines in Figure 1 (a). The separation between two neighboring scanning lines in either direction was 2 μm. A Laue diffraction pattern was recorded at each position where the focused X-ray beam interacted with the single crystal Si chip. A MAR133 X-ray CCD detector which served as diffraction detector was mounted about 8 cm above the sample and 90° with respect to the incidence beam. An example of the recorded patterns is shown in Figure 1 (b). Note that the scanning step size in this experiment (10 μm) was much larger than the X-ray beam spot size (about 1 μm), so that the spatial resolution for this experiment is only limited by the step size. Higher resolution on the same total range is unpractical due to rather long readout time (~ 5 sec) of the CCD detector available.

III. Results and discussions

The Laue patterns collected during the raster scan were automatically indexed and analyzed using the software package XMAS (X-ray Microdiffraction Analysis Software). Indexing the patterns reveals for every scanned point the orientation information with 0.01 degree resolution and expresses it as a 3×3 matrix. From the example shown in Figure 1 (b), one can see that the Si was oriented with <001> more or less parallel to the out-of-plane (z) direction, and <110> parallel to the in-plane horizontal (x) and vertical (y) directions. The insert in the top right corner of Figure 1 (b) shows the shape of the $(\bar{2}06)$ peak. The peak was streaked significantly due to

1 the fact that the high brilliance and high energy synchrotron X-ray beam penetrate
2 very deep into the Si chip sample. A 15 keV X-ray beam penetrates about 450 μm
3 through Si [16]. We found that most of the peaks were streaked like this in the
4 diffraction patterns. This poses severe limitations on the accuracy and precision of
5 strain / stress values deduced from the relative positions of the diffracted spots as
6 routinely done with X-ray microdiffraction data. Firstly, the precise position of the
7 streaked peaks is ambiguous thus posing a direct limitation on the measurement.
8 Furthermore, the penetrating X-ray beam probes the strain at varying depth levels.
9 From strain theory, the strain distribution along the depth of a bent material is non-
10 uniform with the sign of the strain changing across the neutral plane. A strain tensor
11 directly deduced from the diffraction pattern represents a strain average over the
12 whole diffraction volume. Thus, this value tends to be close to zero due to
13 cancellation, since the penetration depth of the X-rays reaches below the neutral plane.
14 There are two possible ways to circumvent this problem: one is to apply three-
15 dimensional microdiffraction technique [17, 18, 19, 20, 21], which directly provides
16 depth resolved strain / stress information. The drawback is a complicated and time-
17 consuming experimental and data analysis procedure. The second way offers a
18 simpler alternative by calculating the strain / stress indirectly from the curvature of
19 the Si surface, as shown in this report.

20 While the penetration of the X-rays deep into the sample severely decreases the
21 strain resolution obtained from the diffraction spots, its effect on the relative
22 orientation is negligible. This is because the diffraction volume is uniform over the
23 entire scan range. Any artifact in orientation stemming from the streaked reflections
24 is thus constant over the measured range. Therefore, the relative change of
25 orientation, which is a measure of the curvature of the Si chip remains unaffected.

1 Taking the orientation matrix at the center spot of the Si chip as reference and
2 comparing the orientation matrix at each individual diffraction spot to this reference
3 point, the bending angle and bending direction of the entire Si chip can be precisely
4 calculated.

5 The bending direction study showed that the sample is bent along the negative y
6 direction (in sample coordinates) on the left half and along the positive y direction on
7 the right half of the scanning-line (clockwise rotation is defined as positive bending).
8 The total bending of the Si chip is therefore dome-like. This is consistent with the
9 fact that the FR-4 substrate has a much bigger CTE than Si, thus the lower surface of
10 the Si chip will be under compression when cooling down from high temperature.

11 The bending angles at each position along the horizontal scanning lines are
12 averaged over the three lines and shown in Figure 2 (a) as black and red dots for the
13 room temperature (RT) and 50 ºC measurements, respectively. The error bars are
14 deduced from the data scatter of the 3 independent measurements. We find the errors
15 to be very small, which confirms that the sample stage is stable and the data
16 reproducible. Furthermore, the separation among the three scanning lines (4 μm) is
17 negligible with respect to the width of the Si chip (7.6 mm), so that the curvature
18 along these lines is identical within the accuracy of the measurements. The bigger
19 errors at 50 ^{o}C compared to RT is assumed to be due to temperature fluctuation. The
20 curves seem discontinuous where the bending angles are below the resolution of this
21 technique. The diffraction data collected from the vertical scans were also analyzed
22 and it was found that the bending angles are very similar to the horizontal scans,
23 which means that the bending of the Si chip was axisymmetric (radial symmetric) and
24 the symmetry axis was the center point of the Si chip. Therefore, the two curves
25 shown in Figure 2 (a) are best fitted by a polynomial of odd order:

1 $$\theta = ar + br^3 \qquad (1)$$

2 where θ is the bending angle, r is the distance from the diffraction spot to the center of
3 the Si chip, and a and b are constants. The bending angle θ indicates the slope angle
4 at each position on the Si surface. The shape of the Si chip can be expressed by
5 integrate the bending angle over the distance from the center:

6 $$z = -\int \theta dr = -(\frac{1}{2}ar^2 + \frac{1}{4}br^4) \qquad (2)$$

7 where z is the relative height of the Si chip surface. Since the Si chip is dome-shaped,
8 which means the center point is the highest and the edge is the lowest, a negative sign
9 is added in Eqn. (2). The shapes of the Si chip at RT and 50 ^{o}C are shown in Figure 2
10 (b) with black and red curves, respectively.

11 Since the bending is caused by the thermal stress coming from the mismatch of
12 CTE between the Si chip and the FR-4 substrate, and solders and underfill were
13 employed to join the chip and the substrate, we approximate solders, underfill, and
14 FR-4 substrate as a continuous film, allowing Stoney's equation to estimate the local
15 stress on this film [22]. However, some of the assumptions underlying the original
16 Stoney's equation (e.g. that all surviving stress and curvature are spatially uniform
17 over the system surface which is studied) are obviously violated in our case. During
18 the last decades, various modifications of Stoney's equations were derived calculating
19 the residual stress in the bent materials with non-uniform temperature [23], non-
20 uniform film thickness [24, 25], and non-uniform curvature [26]. In this report we
21 apply the modified Stoney's approach for our non-uniform material. The two
22 surviving components of curvature in our axisymmetric system are expressed by:

23 $$\begin{aligned} \kappa_{rr} &= \frac{\partial^2 z}{\partial r^2} = a + 3br^2 \\ \kappa_{\theta\theta} &= \frac{1}{r}\frac{\partial z}{\partial r} = a + br^2 \end{aligned} \qquad (3)$$

1 where κ is the curvature, and the subscripts rr and θθ refer to radial and

2 circumferential directions, respectively. The average equibiaxial film stress σ_{film} is

3 calculated from:

4 $$\sigma_{\mathrm{film}} = \frac{1}{2}(\sigma_{rr} + \sigma_{\theta\theta}) = \frac{Y_s t_s^2}{12 t_f (1-\nu_s)}[\kappa_{rr} + \kappa_{\theta\theta} + \frac{1-\nu_s}{1+\nu_s}(\kappa_{rr} + \kappa_{\theta\theta} - \overline{\kappa_{rr} + \kappa_{\theta\theta}})] \quad (4)$$

5 where Y, t, and ν are the Young's modulus, thickness, and Poisson's ratio,

6 respectively, the subscripts s and f denote the substrate (Si chip in this case) and the

7 film, $\overline{\kappa_{rr} + \kappa_{\theta\theta}} = \frac{1}{A}\iint_A (\kappa_{rr} + \kappa_{\theta\theta}) dA$, respectively (A is the area of the chip). The

8 substitution of Eqn (3) into Eqn (4) yields:

9 $$\sigma_{\mathrm{film}} = \frac{Y_s t_s^2}{12 t_f (1-\nu_s)}[2a + 4br^2 + \frac{1-\nu_s}{1+\nu_s}(4br^2 - \frac{2}{3}bA)] \quad (5)$$

10 Because the curvature is not spatially uniform over the entire Si surface, in-

11 plane shear stress σ_{film} exists in the film, as well as the shear stress $\tau_{\mathrm{interface}}$ at the

12 interface of the Si and the film, which are estimated by applying:

13 $$\sigma_{\mathrm{shear}} = \frac{1}{2}(\sigma_{rr} - \sigma_{\theta\theta}) = -\frac{Y_f t_s}{3(1+\nu_f)}[\kappa_{rr} - \kappa_{\theta\theta}] = -\frac{2 Y_f t_s}{3(1+\nu_f)} br^2 \quad (6)$$

14 $$\tau_{\mathrm{interface}} = \frac{Y_s t_s^2}{6(1-\nu_s^2)} \frac{d[\kappa_{rr} + \kappa_{\theta\theta}]}{dr} = \frac{4 Y_s t_s^2}{3(1-\nu_s^2)} br \quad (7)$$

15 We notice that similarly to the original Stoney's equation, the average

16 equibiaxial stress in the film is independent of Young's modulus and Poisson's ratio

17 of the film (Eqn 5), but the in-plane shear stress in the film is depending on the

18 mechanical properties of the film materials (Eqn 6 and Eqn 7). We take the Young's

19 modulus for the mixed film equal to the modulus of tin, which is 50 GPa, and the

20 Poisson's ratio equal to 0.5, and we assume the Young's modulus and Poisson's ratio

21 to be constant as a function of temperature, then the components of the stress are

1 estimated and shown in Figure 3. From Figure 3 (a), we can see that the film is under
2 tensile stress and stress level at the center is about 40 MPa at RT, while stress at the
3 edge is ~ 5 times lower. When temperature is increased, the tension is greatly relaxed.
4 At 50 ^{o}C, the stress at the edge is almost completely relaxed, comparing to half
5 relaxation at the center of the flip chip. Figure 3 (b) shows that the shear stress at the
6 interface of the Si chip and the mixed film is about twice as high as the in-plane shear
7 stress in the mixed film, which indicates a severe reliability concern that the
8 integrated circuits which are deposited on the Si chip are subjected to higher shear
9 stress than the solder joints. Shear stress is also relaxed at enhanced temperature;
10 however, the relaxation rate is much slower than the equibiaxial stress. For example,
11 only 30% of the interface shear stress is relaxed at the edge when the temperature is
12 increased from RT to 50 ^{o}C. The estimation of the errors caused by the inaccuracy of
13 curvature measurement and the repeatability of the sample position is found to be
14 smaller than 0.3 % of the calculated values, which indicate that the main errors of this
15 method are not caused by the experimental measurements.
16 The bending was also measured as the flip chip sample was heated to 75 ^{o}C and
17 100 ^{o}C; however, the bending angle was below the angular resolution (0.01 degree) of
18 the synchrotron X-ray microdiffraction technique since the thermal stress was relaxed
19 at high temperature. As a result, the curvature and the stress distribution on the
20 sample surface couldn't be detected.
21 To estimate the stress resolution by using this technique, we assume the bending
22 angle from the center to the edge of the Si chip to be equal to the orientation
23 resolution, 0.01 degree, and the curvature to be uniform over the entire chip surface,
24 then the curvature radius is calculated to be 22 m. Therefore the average stress on the

solder / underfill / substrate mixed film is calculated by applying the original Stoney's equation:

$$\sigma_{film} = \frac{t_s^2}{6rt_f}\left(\frac{Y}{1-\nu}\right)_s = 2.0MPa$$

This estimation indicates that the stress measurement averages based on the curvature detection by synchrotron polychromatic x-ray microdiffraction is very sensitive even to values as low as 2.

IV. Conclusion

In this article, we reported the application of the synchrotron X-ray microdiffraction technique on the stress measurement of the non-uniformly bent Si surface on flip chips. The local stress distribution over the flip chip was calculated based on the measured curvature distribution and a modified Stoney's equations. The calculation error mainly comes from the unknown mechanical property constants of mixed film (Y_f and ν_f), and deviations from the assumptions based on which the modified Stoney's equations were derived. For example, the thickness of the Si chip is much larger than that of the film ($t_s >> t_f$). We can conclude from the estimation that the average equibiaxial stress, which comes from the mismatch of the CTE of different layers of the flip chip structure, strongly depends on temperature. More than 50% of the stress is relaxed when temperature is increased by 25 ^{o}C from RT. The shear stress at the interface of the Si chip and the mixed film, caused by the non-uniformity of the bending curvature, is linearly proportional to the distance from the sample center, so that the printed circuits and the solder joints at the edge of the chip are subjected to a higher level of shear stress.

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7

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Figure captions:

Figure 1 (a) Flip chip sample attached on copper plate. The scanned lines are indicated by the dashed red lines. The sample coordinates used in this article are shown below the photo. (b) A Laue diffraction pattern taken at the center of the Si chip, with the enlarged $(\bar{2}06)$ peak shown in the inserted box.

Figure 2 (a) Experimentally measured bending angles and (b) fitted sample surface shapes as a function of the distance to the center of the Si chip at RT and 50 ^{o}C, respectively.

Figure 3 Spatial distributions of (a) average equibiaxial stress in the underfill / solder / substrate film and (b) in-plan and interface shear stress.

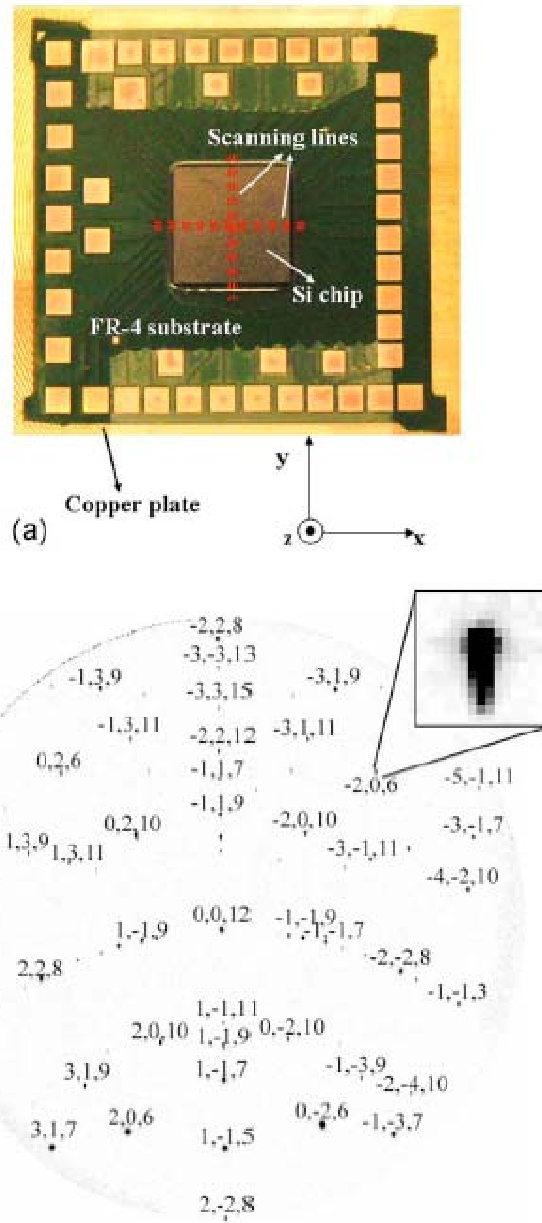
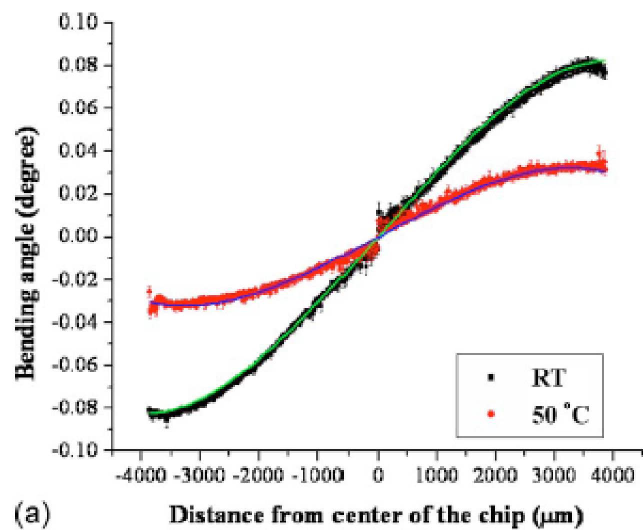


FIG. 1. (Color online) (a) Flip chip sample attached on copper plate. The scanned lines are indicated by the dashed red lines. The sample coordinates used in this article are shown below the photo. (b) A Laue diffraction pattern taken at the center of the Si chip, with the enlarged ($\bar{2}06$) peak shown in the inserted box.



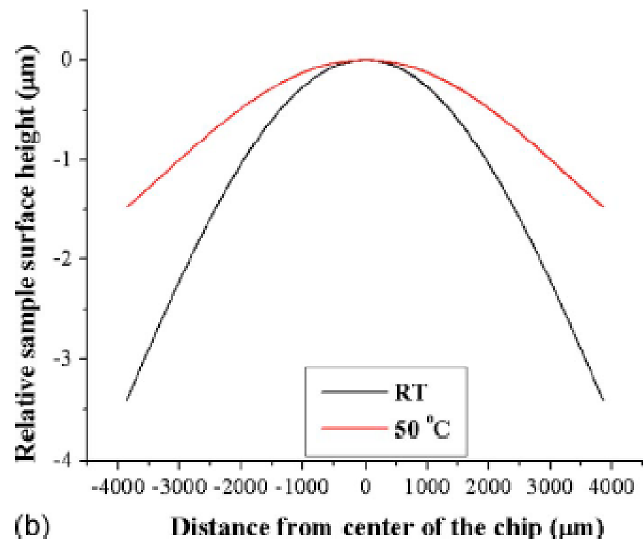


FIG. 2. (Color online) (a) Experimentally measured bending angles and (b) fitted sample surface shapes as a function of the distance to the center of the Si chip at RT and 50 °C, respectively.

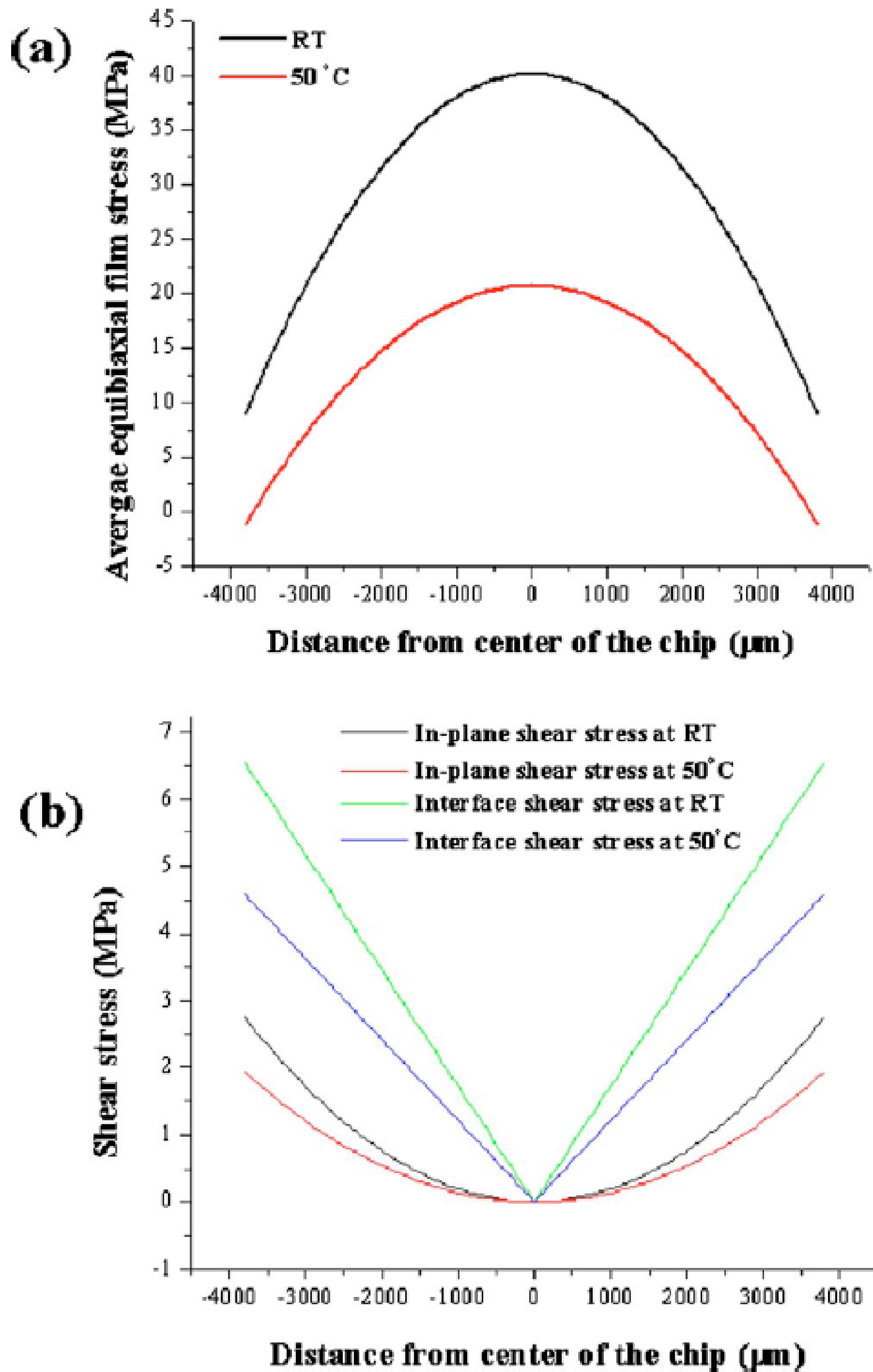


FIG. 3. (Color online) Spatial distributions of (a) average equibiaxial stress in the underfill/solder/substrate film and (b) in-plan and interface shear stress.