UNIVERSITY OF CALIFORNIA,
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# Machine Learning Assisted Design of mmWave Wireless Transceiver Circuits

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical and Computer Engineering

by

Xuzhe Zhao

Thesis Committee:
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# DEDICATION

To my parents and my friends, for their unwavering support and encouragement.

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Portions of Chapter 3 to 5 are adapted to form the paper that is currently under review as "AICircuit: A Multi-Level Dataset and Benchmark for AI-Driven Analog Integrated Circuit Design", in the 38th Conference on Neural Information Processing Systems (NeurIPS 2024) Track on Datasets and Benchmarks. The co-authors listed in this conference paper are Asal Mehradfar, Yue Niu, Sara Babakniya, Mahdi Alesheikh, Hamidreza Aghasi, and Salman Avestimehr. Professor Hamidreza Aghasi and Professor Salman Avestimehr of USC directed this work.

# ABSTRACT OF THE THESIS

Machine Learning Assisted Design of mmWave Wireless Transceiver Circuits

By

Xuzhe Zhao

Master of Science in Electrical and Computer Engineering

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Assistant Professor Hamidreza Aghasi, Chair

As fifth-generation (5G) and upcoming sixth-generation (6G) communications exhibit tremendous demands in providing high data throughput with a relatively low latency, millimeter-wave (mmWave) technologies manifest themselves as the key enabling components to achieve the envisioned performance and tasks. In this context, mmWave integrated circuits (IC) have attracted significant research interests over the past few decades, ranging from individual block design to complex system design. However, the highly nonlinear properties and intricate trade-offs involved render the design of analog or RF circuits a complicated process. The rapid evolution of fabrication technology also results in an increasingly long time allocated in the design process due to more stringent requirements. In this thesis, 28-GHz transceiver circuits are first investigated with detailed schematics and associated performance metrics. In this case, two target systems comprising heterogeneous individual blocks are selected and demonstrated on both the transmitter and receiver sides. Subsequently, some conventional and large-scale machine learning (ML) approaches are integrated into the design pipeline of the chosen systems to predict circuit parameters based on desired specifications, thereby circumventing the typical time-consuming iterations found in traditional methods. Finally, some potential research directions are discussed from the perspectives of circuit design and ML algorithms.

# Chapter 1

# Introduction

## 1.1 Background

Since the first generation (1G) of mobile communication was implemented to transfer the voice signal between different users, tremendous technologies relevant to wireless communication have evolved incredibly over the past several decades. To cope with the significantly increasing demands for wireless connectivity, the promising fifth generation (5G) and upcoming sixth generation (6G) wireless networks are deployed to alleviate spectrum crowding at lower frequencies with higher data throughput and lower latency [1]. From a numerical point of view, 5G and 6G communications are envisioned to provide the capacity of a data rate greater than 1-10 Gb/s, a latency on the order of 1 ms or less, and a high volume of traffic density from the unlicensed available bandwidth up to a few hundred GHz, which facilitates three major application scenarios comprising enhanced mobile broadband (eMBB), massive machine-type communication (mMTC), and ultra-reliable low latency communication (URLLC) [2]. Compared to previous communication technologies, 5G and 6G utilize millimeter-wave (mmWave) frequencies due to abundant spectrum resources. In that regard,

many countries have allocated several mmWave bands within the frequency range 2 (FR2) from 24.25 to 52.6 GHz, and the higher band named WR-08 that is designated for 6G communication systems from 90 to 140 GHz [3] [4]. Despite these benefits shown above, some key challenges should also be taken into consideration to employ the mmWave frequencies. For example, the mmWave signal suffers from large free space loss stated by Friis' transmission law (Eq. (1.1)):

$$P_r = P_t G_t G_r \left( \frac{c}{2\pi f_c d} \right)^2 \tag{1.1}$$

in which the power of the received signal is inversely proportional to the square of carrier frequency. Moreover, the shadowing issue coming from various outdoor materials and large processing power consumption further impede the deployment of mmWave systems [1] [5]. Given that scenario, some key-enabling technologies have been called for overcoming these difficulties and achieving the necessary performance in the mmWave frequency bands, which consists of all-spectrum access, massive multiple-input multiple-output (MIMO), ultra dense networking, and semiconductor technologies [6] [7].

As an indispensable and promising path to achieve high-speed wireless communications, silicon based integrated circuit has been validated by designing wideband amplifiers over 30 GHz utilizing the mainstream CMOS technologies [8]. Since then, analog or radio frequency (RF) integrated circuits operating in mmWave or sub-terahertz frequency bands have attracted a lot of research interest. In terms of individual circuit block, a Q-band low-noise amplifier (LNA), a dual-band linear up-conversion mixer, a compact super-harmonic voltage-controlled oscillator (VCO), and a three-way Doherty power amplifier (PA) are presented for various mmWave applications and fabricated in 90-nm, 40-nm, 65-nm, and 45-nm CMOS processes [9] [10] [11] [12]. Benefit from advanced transistor technologies and reduced size of passive components, antenna manifests itself as a pivotal entity to provide efficient power transmission and reception with the expected radiation pattern operating in the mmWave

and sub-terahertz frequency bands [13] [14]. To cope with severe path loss in these high frequency bands, a systematic design methodology is explored to maximize power generation and transfer with the nonlinear device model for GHz and THz applications [15] [16] [17]. Pertaining to system-level implementation based on complex analog or RF integrated circuit blocks, a spatial-orthogonal Amplitude-Shift Keying (ASK) transmitter and a high-power transmitter equipped with phase locking techniques are demonstrated to mitigate the power limitation in the terahertz range [18] [19]. In addition, some dedicated receiver architectures using nonlinear analog operators are exhibited in mmWave single-input single-output (SISO) and multiple-input multiple-output (MIMO) communication systems [20] [21]. As the size of transistors scales down, some advanced devices and sophisticated transceivers are utilized for high-speed communications, pattern recognition, molecular spectroscopy, real-time imaging, local-area sensing, and high resolution applications by leveraging the merits of the mmWave or THz frequency bands [22] [23] [24] [25] [26] [27].

## 1.2 Motivation

Despite the fact that analog and RF integrated circuits are ubiquitous in mmWave wireless communication, the corresponding design pipeline can still be regarded as the significantly time-consuming and complicated process, even for experienced circuit designers. In general, there are three main steps in pre-layout circuit design. Firstly, circuit designers need to select the appropriate topology to meet the desired performance metrics by leveraging their prior knowledge and experience. Then, the initial size of each component shown in chosen topology is calculated according to a large number of approximations and simplifications. Following that, the specific circuit parameters are confirmed to meet a group of target specifications by performing the simulations countless times [28]. As the complexity of realized functions keeps growing and CMOS technology continues scaling, designing analog and RF integrated

circuits in mmWave frequency bands has become more arduous. Recently, machine learning techniques have been significantly developed by means of high-performance computing hardware, which entails an accessible solution to a large number of interdisciplinary research in diversified domains [29]. Regrading this approach, the digital circuit benefits from the established automation process by employing mature VLSI Computer-Aided Design (CAD) tools equipped with pre-sized defined logic libraries [30]. In contrast, analog design automation tools are not developing at the same pace as their digital counterpart, since there are a broad range of circuit topologies and intricate trade-offs involved in a variety of performance specifications, which makes design rules more complicated when layout parasitics are taken into account [31]. Therefore, it is pivotal to accelerate analog and RF design procedures via identifying and automating the time-consuming and resource-intensive parts in an accurate and efficient manner. In this thesis, some conventional and large-scale machine learning algorithms are leveraged to assist the design of wireless transceiver circuits at 28 GHz from block-level and system-level perspectives.

## 1.3 Organization of This Thesis

The remainder of this thesis is organized as follows. Chapter 2 investigates the overview of recent growing research works in analog circuit design enhanced by diversified machine learning algorithms. Chapter 3 and 4 demonstrate the 28 GHz transmitter and receiver design respectively, which comprises the performance analysis and the corresponding ocean scripts implementation. Chapter 5 presents a workflow involving different machine learning algorithms to optimize the system-level mmWave circuit design supported by the benchmark dataset. In the end, Chapter 6 concludes and summaries this work with some potential research directions in the future.

# Chapter 2

# Literature Review

The aforementioned content indicates the feasibility and necessity of automated design flows applied in the analog and RF integrated circuit domain. In this section, some related work and representative methods will be discussed and reviewed.

Figure 2.1 outlines the different categories of prior automating techniques for the analog and RF circuit design. These prevalent methods can first be divided into knowledge-based and optimization-based approaches [32]. In terms of knowledge-based techniques, the prior domain knowledge of experienced circuit designers is transcribed into the corresponding equations and algorithms, which means the complete design plan for a certain circuit topology needs to be well-defined with the detailed sizing solution of each component to fulfill the desired specifications [33]. As an interactive design system based on knowledge-based techniques, IDAC is capable of sizing more than 40 analog schematics by means of providing some design knowledge regarding the relationship between the different technologies and block specifications [34]. However, as the functions for analog and RF circuits become more sophisticated, it is significantly difficult to obtain the hand-crafting equations to describe

the circuit knowledge in the corresponding programs. In that case, another main category named

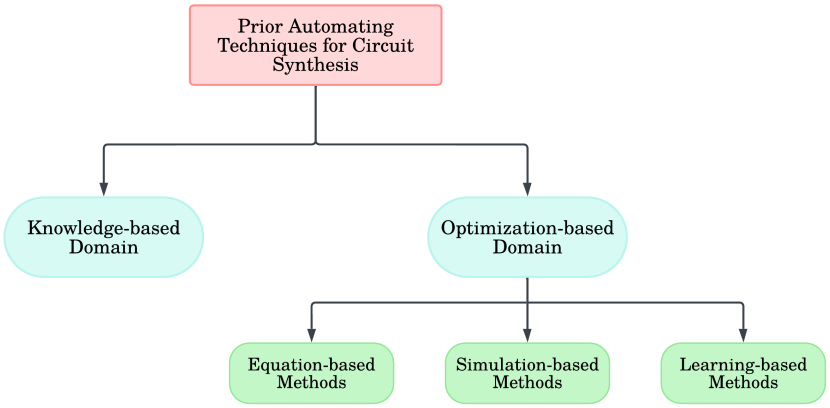


Figure 2.1: Classification for prior automating techniques for circuit synthesis.

optimization-based approach will be introduced. Rather than the need for a completed design plan, the design parameters and variables are updated at each iteration in optimization process, which will be finalized when the desired performance metrics are fulfilled [32]. According to different engines for optimization and evaluation, optimization-based technique can be further classified into three subsections including the equation-based, simulation-based, and learning-based methods as depicted in Figure 2.1. From the perspective of equation-based methods, the analytic constraint equations can be obtained manually or automatically with the aid of geometric programming and this circuit problem can be optimized using a numerical algorithm, such as GPCAD and TAGUS [35] [36]. The main issue for this method is substantially time-consuming to derive the appropriate equations and difficult to update them with the latest technology. Another popular approach used in analog circuit design optimization is simulation-based method. Typically, an initial population is selected following the stochastic sampling. After mutating the best children, the corresponding offspring will be examined and sampled from a new iteration. In the inner loop of the optimization cycle, a circuit simulator tool, such as SPICE, is leveraged to determine and evaluate the performance of various circuits [37]. Some representative works are presented through the

implementation of Bayesian Optimization (BO), Evolutionary Algorithms (EA), and Particle Swarm Optimization (PSO) [38] [39] [40]. Based on the above investigation, this simulation-based approaches lead to higher accuracy since they conduct the optimization by directly collecting the simulated data. However, this method is subject to the convergence issue due to insufficient samples. Moreover, the entire optimization process needs to start over even though there is a slight change in desired performance specifications. With the significant development of relevant techniques, learning-based approaches obtain plenty of attraction in analog circuit domain. They primarily rely on the various machine learning methods to accurately establish the relationship between the circuit parameters and target performance metrics, and further solve the analog circuit problems, which entails the inverse process compared to the circuit simulator. Some supervised and reinforcement learning algorithms are used in prior works [37] [41] [28].

In addition to the top-level overview for diversified automation techniques, the in-depth review for some innovative works is investigated in the following part. As depicted in Figure 2.2, the main methods utilized in these works come from supervised learning, reinforcement learning, and hybrid approaches combining neural network and optimization algorithms.

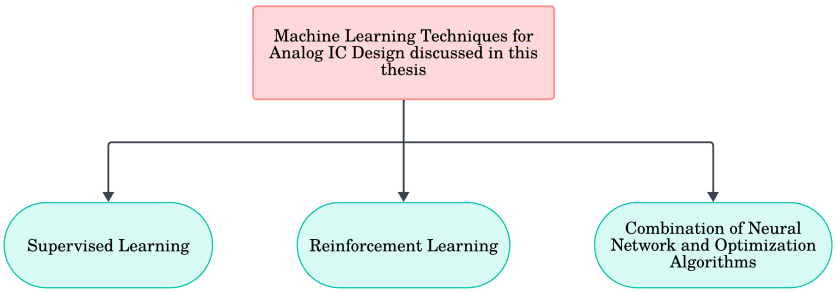


Figure 2.2: Machine learning techniques for analog circuit design reviewed in this thesis.

## 2.1 Supervised Learning

As a typical and indispensable technique in the supervised learning domain, Neural Networks (NN) are attracting great attention in both industry and academia, such as speech recognition, imaging process, and natural language processing [42]. Inspired by human brain activity, NN have the fundamental linear threshold units whose name is perceptron to receive the input signal processed by proper weights and bias, then a specific activation function will be applied to deal with nonlinear problems. In general, there are two steps defined by the training and testing phases during the establishment of NN. In the first place, the real solution for different types of problem is approximated based on the labeled dataset. After that, some new outputs are accurately predicted for unknown data points as supported by the trained NN model [43].

From the perspective of analog and RF circuit design, NN is employed to estimate the functionality of different circuit topologies, which involves the relationship between the circuit parameters and performance metrics. Since Glenn Wolfe and Ranga Vemuri demonstrated the NN can be successfully used to assist the design of various CMOS operational amplifier (op-amp) in 2003, there are tremendous research works shown in analog circuit design based on the NN and its variants [44]. According to [45], the Deep Neural Network (DNN) and the Recurrent Nural Network (RNN) are applied to solve the two-stage op-amp sizing problem. With appropriate sweeping for the aspect ratio of each MOSFET instance, the DNN and RNN models can achieve the accuracy of 95.6% and 92.6% for the 900 test circuit, which concludes that the DNN model has more stability than the RNN model attributed to less dependence of training data. Another disruptive work relies on the Artificial Neural Network (ANN) to predict the analog amplifier with voltage combiners that are utilized to boost the voltage gain. During the training phases, three different ANN models are trained with the same dataset. In the end, the model with 500 epochs has the best performance since it benefits from the value of weights shown in the ANN model validated through the

entire dataset. Another contribution for this work is that the specification trade-offs are taken into consideration, which indicates the trained ANN model is capable of predicting the performance metrics outside the original training dataset with 0.0124 mean squared error [41].

## 2.2 Reinforcement Learning

As a pathway to access the general forms of artificial intelligence, reinforcement learning (RL) is an instrumental technique inspired by human learning mechanisms [43]. Compared to the supervised learning method, RL is driven by different rewards and penalties and does not require the collection of labeled datasets. In Figure 2.3, a general RL learning loop is presented. In each iteration, an RL agent is deployed to convert the current state (St) to a new action (At) given the corresponding reward (Rt). After that, the environment is employed to transform the current action (At) to a new state (St+1) and reward (Rt+1). This sequence of states and actions will lead to the maximum rewards ultimately. With this tight interaction between the agent and the environment, RL becomes prevalent in game-playing, self-driving cars, and intelligent robots [46].

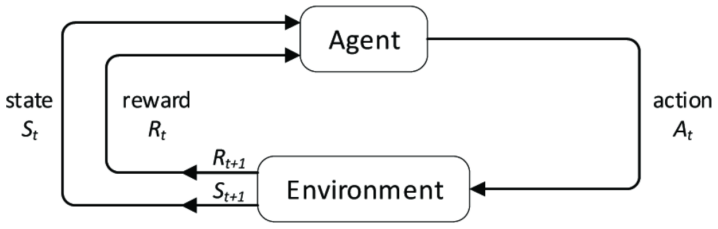


Figure 2.3: General learning loop for RL [46].

In light of analog circuit design, RL agent is initialized by the performance metrics that can be regarded as the state of a circuit. Then, the action generated by the agent will

be injected into the circuit simulator served as the environment. After comparing the predicted performance features with the desired specifications, the rewards will be computed and carry out the new state when their value increases. In contrast, the revised action will be generated due to lower rewards. The working flow for this process is shown in Figure 2.4 [29].

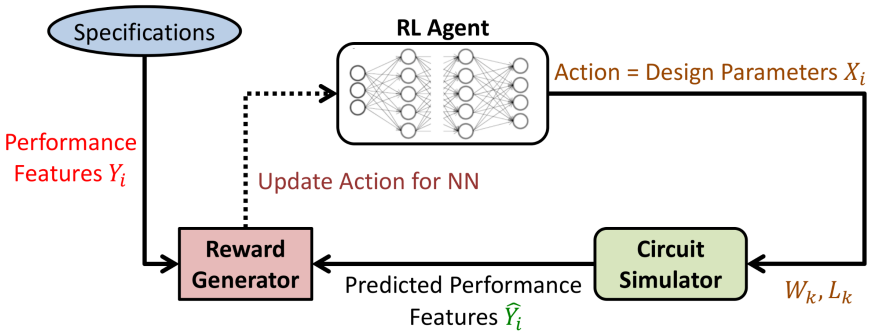


Figure 2.4: Design flow for RL used in analog circuit design [29].

One representative work presented by Keertana Settaluri et al. shows a machine learning optimization framework that employes deep reinforcement learning can be deployed to design the transimpedance amplifier and two-stage op-amp [37]. Aiming to improve the design efficiency and learning generalization, a sparse subsampling technique is utilized in this work to obtain the knowledge about the entire design space. Therefore, average 40× more sample efficient demonstrated here compared to prior optimization approaches. Another main contribution for this work is that they also take the layout parasitics into consideration by leveraging transfer learning, which mimics the more realistic design scenarios. For the experimental results of layout parasitics prediction, the two-stage op-amp with negative gm load is used to validate this AutoCkt model, which entails this framework has an ability to design 40 candidates that pass the LVS rules in under 3 days [37]. In line with the same target to improve the sample efficiency, another ML model comprising the RL and the sensitivity analysis was proposed in 2023 [47]. This work relies on the universal value function approximator (UVFA) in RL model training to convert the design space with high dimensions to one dimension of Figure of Merits (FoM) covering all performance specifications [48].

Apart from the method used in the RL model, a novel sampling method for data selection is described with reference to the 'Pick sampling' and 'PZ sampling' criteria. Furthermore, $g_m/I_D$ sizing methodology is applied to mitigate the short channel effect and alleviate the nonlinearity for prediction tasks. In the end, this proposed method is capable of optimizing the analog circuit sizing problems by 42.2% improvement with the respect to convergence presented in a baseline work [47] [49].

## 2.3 Combination of NN and Optimization Algorithms

In addition to the supervised learning and reinforcement learning approaches articulated above, some automation techniques in analog circuit design are adopted to deploy the NN coupled with the various optimization algorithms. The general purpose for this combination is to benefit from both the efficiency and accuracy shown in NN and optimization algorithms respectively. For instance, there is a two-model chain implemented to predict the optimal performance under the new contexts including the loads and supply voltage, along with the trade-offs between them [50]. In that work, a multi-variate polynomial regression is deployed to estimate the performance metrics and their trade-offs in the first layer. Following that, an ANN is invoked to find out the component sizing according to the desired specifications. Since data from the optimized sizing solution are used in the training stage, this framework can provide near-optimal predictions instantly even if the boundaries of desired performance are expanded, which is validated by sizing the folded cascade amplifier [50]. Another strategy to incorporate the NN and different optimization algorithms is to accelerate the process of global optimization through replacing the circuit simulator by well-trained NN model. In that case, a fully-automated analog circuit generator framework named AnGeL is presented to cover all important steps in analog circuit schematic design involving the circuit topology determination and the circuit components sizing [51]. To cope with the entire design space

and diversified potential topologies, NN is applied to estimate the functionality for more complicated circuit topologies by leveraging the knowledge from the simpler ones. During this phase, the complex circuit is divided into several small sub-sections, in which the less design parameters and smaller labeled training data are taken into consideration to obtain the optimum points in a fraction of the time. Moreover, these sub-circuits can be investigated in parallel as a result that this framework can support various circuit topologies efficiently. The interaction between the complicated topologies and the corresponding simpler sub-circuits is depicted in Figure 2.5. As a population-based approach, Particle Swarm Optimization (PSO) is also utilized in this work to enhance accuracy during the local optimization procedure. In the end, the experimental results demonstrate that AnGeL is capable of retaining the same accuracy but 2.9× to 75× faster than the state-of-the-art works, whereby testing more than 1450 different circuits [51].

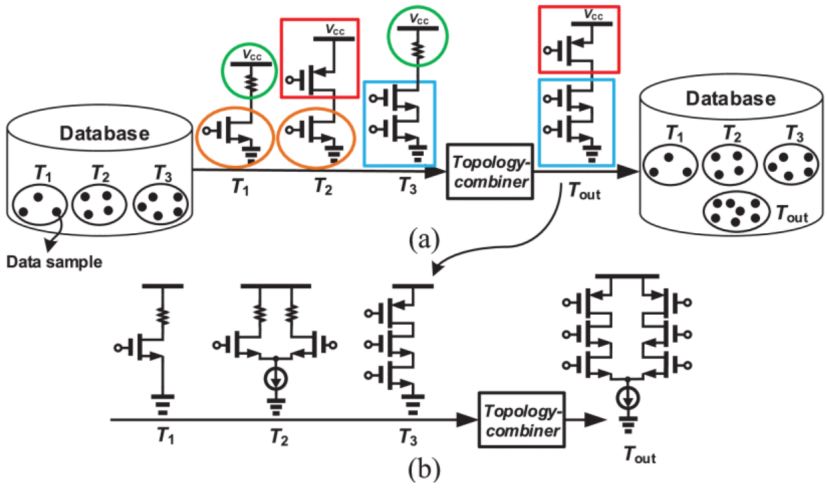


Figure 2.5: An example of leveraging the knowledge from (a) simpler circuits to (b) more complex one [51].

# Chapter 3

# A 28-GHz Transmitter Design

Since the market demands are increasing for high data rate systems, mmWave communication shows the reliable capability to enhance the data rate to over 1 Gb/s. However, there are some inherent risks for electromagnetic waves propagating in such a high frequency band, which primarily comes from the large path loss and shadowing effect [52]. Aiming to overcome these detrimental effects, an RF transmitter is envisioned to deliver the mmWave signal with higher gain and output power while not degrading efficiency. For the sake of regulation, some indispensable functions and specifications are defined by different wireless standards for transceiver design, which ensures that the information can be successfully exchanged among various types of devices. As these requirements become more stringent in mmWave frequency, machine learning assisted methods are applied to facilitate the transmitter design. The target circuits and their desired performance metrics are presented in this section with the corresponding ocean scripts implementation.

## 3.1 Transmitter Architecture

In this work, the direct conversion architecture is deployed in the transmitter design due to its higher linearity and lower power consumption, which eliminates the need for additional structure to convert Intermediate Frequency (IF) to Radio Frequency (RF) [53]. With the intention of covering diversified circuit blocks in system-level design assisted by the ML approach, the combination of Voltage-Controlled Oscillator (VCO) and Power Amplifier (PA) is presented as a typical 'signal generator - amplifier' system on the transmitter side. As illustrated in Figure 3.1, the sustainable signal is first generated by the VCO with a tunable frequency controlled by an external voltage signal across a certain range. Then, this periodic signal is amplified via the PA with considerable gain and output power. Finally, the transmitting antenna allows this amplified signal to propagate into free space with a relatively long distance. Pertaining to the structure of individual blocks, the LC cross-coupled configuration is utilized in the VCO design to generate the oscillated signal by leveraging the DC supply power to counteract the parasitic losses in the LC resonator, as shown in Figure 3.2 and 3.3. Owing to its low phase noise and large output swing, this type of VCO has become popular in high-speed wireless communication systems [54]. For the sake of system stability, a source-follower buffer is placed following the VCO to maintain the continuous oscillation. As the most power-hungry building block in the transmitter, PA is implemented by the two-stage differential cascode structure illustrated in Figure 3.4 and 3.5 as a result to amplify the signal with high power gain without compromising efficiency [55].

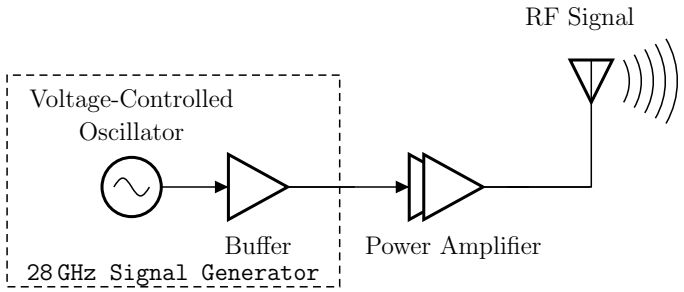


Figure 3.1: A 28 GHz direct conversion transmitter architecture involving VCO and PA.

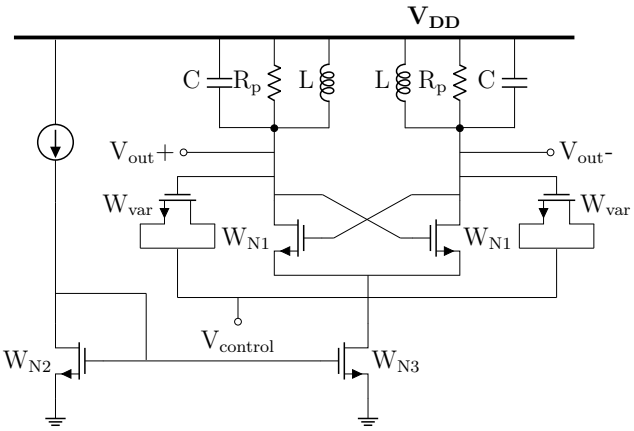


Figure 3.2: LC cross-coupled VCO schematic.

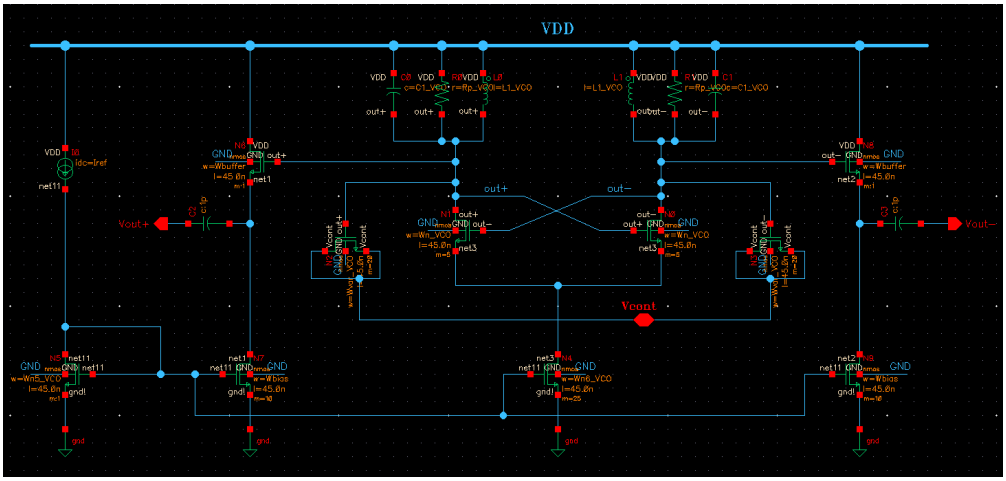


Figure 3.3: VCO implementation with buffer using NCSU 45 nm PDK in Cadence Virtuoso

## 3.2 Performance Specifications Analysis

### 3.2.1 Individual Performance

In this section, some representative performance metrics are investigated for VCO and PA individually. These candidates are also used to train the ML model and further predict the related circuit parameters.

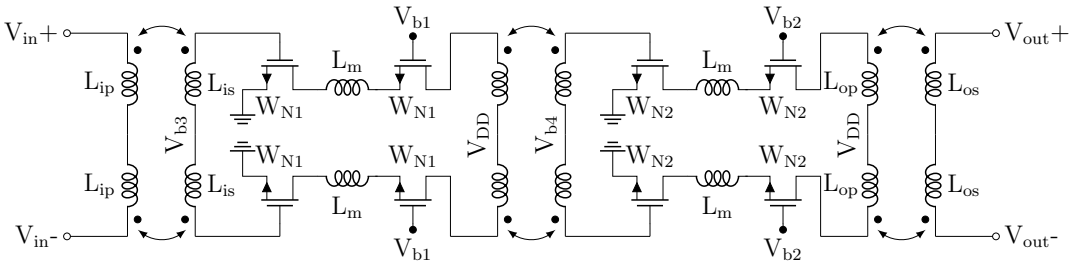


Figure 3.4: Two-stage differential cascode PA schematic.

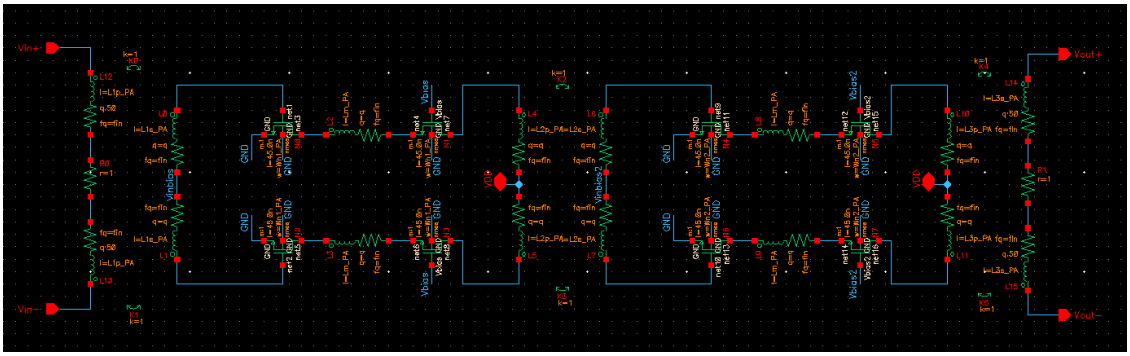

Figure 3.5: PA implementation using NCSU 45 nm PDK in Cadence Virtuoso

Since VCO is required to output sustainable signals whose frequency is varied across a certain range, the first important specification should be intended to quantify frequency variation, called the 'tuning range'. During the tuning process, MOS varactors are deployed to vary the resonance frequency in LC cross-coupled VCO by means of changing their capacitance with different control voltage. According to an approximation of $C_{\text{var}} << C_1$, this specification can be expressed as Eq. (3.1):

$$\Delta\omega \approx \frac{1}{\sqrt{L_1 C_1}} \frac{C_{\text{var2}} - C_{\text{var1}}}{2C_1} \tag{3.1}$$

Another essential characteristic is identified as the "phase noise", indicating the small phase deviation due to the noise of different components in the VCO. This random departure is quantified by normalizing the noise power to the carrier power with the respect to specific offset frequency. The unit "dBc/Hz" also captures the relationship between these two types

of power by integrating the in-band and out-of-band components as a result to further signify the signal-to-noise ratio (SNR) performance of the system with the VCO inside [56]. In order to cover the multiple noise sources comprising the thermal noise from the LC tank and transistors, along with the flicker noise, Lesson's model is leveraged to represent the noise effect through indicating the relationship between the high frequency noise floor and the flicker noise up-conversion, as shown in Eq. (3.2) [57]:

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{\text{sig}}}\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \text{ (dBc/Hz)} \tag{3.2}$$

Moreover, there is an intrinsic trade-off between the tuning range and the phase noise primarily coming from the different optimum scenarios regarding the capacitance ratio between the switching capacitors and tuning varactors, which leads to more complicated design procedure [58].

As a key enabling block to increase the power level of the output signal, there are several critical characteristics that should be taken into consideration during the design of PA. The first performance metric called the "large-signal power gain" is employed to describe the ratio of output power to input power when PA reaches the saturation region with increased input power. Given the great amount of power consumption by the PA, efficiency is also an important characteristic for evaluating power-intensive devices. The detailed assessment of PA efficiency is defined by two metrics, including "drain efficiency" (Eq. (3.3)) and "power-added efficiency (PAE)" (Eq. (3.4)):

$$\text{Drain Efficiency}\,(\eta) = \frac{P_{\text{out}}}{P_{\text{DC}}} \times 100\% \tag{3.3}$$

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \times 100\% \tag{3.4}$$

The former is utilized to measure the delivered output power with the respect to the DC power. Considering the power used by the amplifier itself, the PAE examines the efficiency for the RF power that is added to the device by subtracting the input RF power. In this work, both types of efficiency are investigated with the variation of circuit parameters.

### 3.2.2 System Performance

For the RF transmitter system design, the output power level is specified by a rule named "spectral mask", in which the maximum transmission power is limited by a certain level and out-of-channel emissions are also required to decrease within the dedicated bandwidth, thereby reducing adjacent-channel interference. In that regard, the output power of the system combining VCO and PA is taken into account with the measurement of the 3 dB bandwidth. Besides these two specifications, the dc power consumption is applied to assess the power utilized by the system during its operation. Finally, the voltage swing performance implies the ability of the system to deal with large input signals without distortion, which directly determines the working range of the transmitter.

## 3.3 Ocean Scripts Implementation

In light of performing repetitive tasks in Cadence, conventional ADE simulations are not suitable for large-scale simulations, which is a relatively essential step for collecting the training data during the ML model training process. In that case, the new entity called OCEAN scripts is implemented to perform the parametric analysis and process the simulation data from the command line in the specified UNIX shell [59]. As a subset of the SKILL language, OCEAN abbreviated from Open Command Environment for Analysis is deployed

to facilitate the various simulations and establish the interface between Cadence and the Python environment in this work.

By leveraging the ocean scripts and the defined schematic netlist, the various analysis and simulation results can be encapsulated into different commands. During the system design on the transmitter side, dc and transient analysis are employed to acquire the power consumption and voltage swing performance from the peak-to-peak value of the output waveform. As for the 3dB bandwidth, S Parameters (SP) analysis is used to select the frequency difference across the points decreased by 3dB with reference to the maximum amplitude. Another critical analysis commonly deployed in the RF circuit domain is periodic steady-state (PSS) analysis, in which the device under test is excited by a large periodic signal or the system has the periodic operating point. In that regard, the Harmonic Balance (HB) engine is applied to evaluate the system output power in the PSS analysis, which also includes the VCO performance comprising the phase noise and tuning range, and the PA specifications consisting of power gain, drain efficiency, and PAE. The system schematic in Cadence and its performance metrics with the ocean scripts implementation are demonstrated in Figure 3.6 and Table 3.1 respectively.

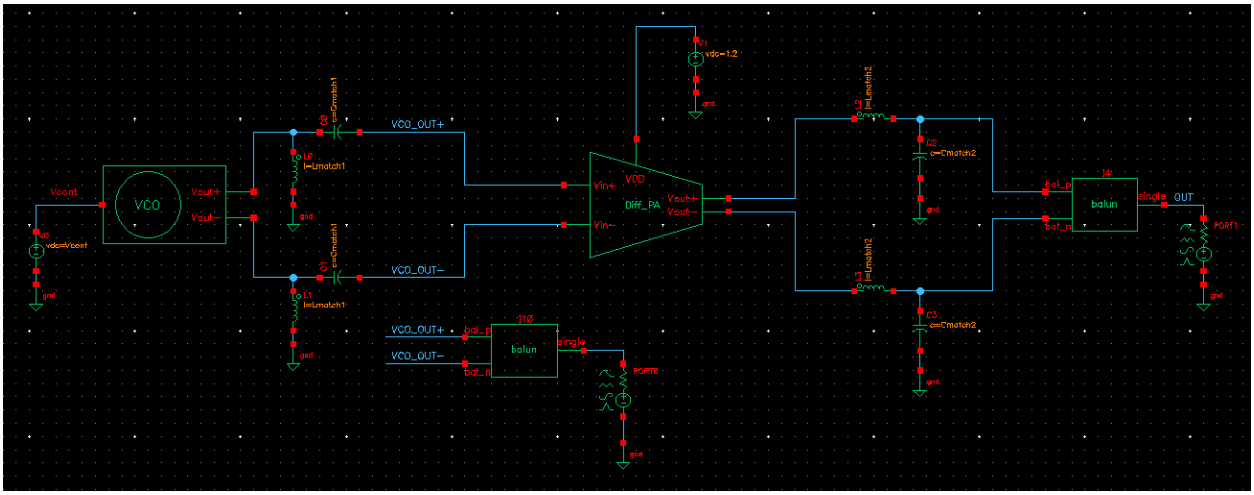


Figure 3.6: Schematic of target system on transmitter side in Cadence Virtuoso.

| **Performance Metrics** | **Ocean Scripts** |
|---|---|
| Power Consumption | `getData(":pwr" ?result "dcOp")` |
| Bandwidth | `(ymax(cross(db10(gt(sp(1 1 ?result "sp") sp(1 2 ?result "sp") sp(2 1 ?result "sp") sp(2 2 ?result "sp"))) (ymax(db10(gt(sp(1 1 ?result "sp") sp(1 2 ?result "sp") sp(2 1 ?result "sp") sp(2 2 ?result "sp")))) - 3) 2 "either" t "time" nil)) - ymin(cross(db10(gt(sp(1 1 ?result "sp") sp(1 2 ?result "sp") sp(2 1 ?result "sp") sp(2 2 ?result "sp"))) (ymax(db10(gt(sp(1 1 ?result "sp") sp(1 2 ?result "sp") sp(2 1 ?result "sp") sp(2 2 ?result "sp")))) - 3) 2 "either" t "time" nil)))` |
| Output Power | `ymax(dbm(pvr('pss "/OUT" "/gnd!" 50.0 '(1))))` |
| Voltage Swing | `ymax(v("/OUT" ?result "tran")) - ymin(v("/OUT" ?result "tran"))` |
| Tuning Range for VCO | `ymax(harmonic(xval(getData("/VCO_OUT+" ?result "pss_fd")) '1)) - ymin(harmonic(xval(getData("/VCO_OUT+" ?result "pss_fd")) '1))` |
| Phase Noise for VCO | `value(leafValue(pn('pnoise) "Vcont" 0.6) 1000000)` |
| Power Gain for PA | `ymax(db10((pvi('pss "/net7" "/net4" "/I19/Vout+" 0 '(1)) / (- pvi('pss "/VCO_OUT+" "/VCO_OUT-" "/I19/Vin+" 0 '1)))))` |
| Drain Efficiency for PA | `ymax(((- (pvi('pss "/net7" "/net4" "/I19/Vout+" 0 '(1)) / (- pvi('pss "/net8" "/gnd!" "/V1/PLUS" 0 '0)))) * 100))` |
| PAE for PA | `ymax((- ((100.0 * harmonic((spectralPower (i("/I19/Vout+" ?result "pss_fd") (v("/net7" ?result "pss_fd") - v("/net4" ?result "pss_fd"))) + spectralPower(i("/I19/Vin+" ?result "pss_fd") (v("/VCO_OUT+" ?result "pss_fd") - v("/VCO_OUT-" ?result "pss_fd")))) '(1))) / (- harmonic(spectralPower(i("/V1/PLUS" ?result "pss_fd") (v("/net8" ?result "pss_fd") - 0.0)) '(0))))))` |

Table 3.1: Ocean scripts implementation for different analysis of system in transmitter.

# Chapter 4

# A 28-GHz Receiver Design

In order to accelerate the commercialization of high-definition video and self-driving vehicles, the mmWave frequency bands have been the great attraction over the past several decades. In addition to the increasing market needs, more advanced CMOS processes provide a feasible solution to establish the integrated circuit at this relatively high frequency, which leads to the active research area in both industry and academia [60]. A successful communication process relies on many aspects and components, such as frequency planning, transmitter design, and receiver design. Despite the fact that these devices should be optimized concurrently, the design of the dedicated receiver is worth more consideration from the perspective of signal environment and system adaptability [61]. With the evolution of wireless standards and fabrication technology, it is becoming more important to design the mmWave receiver with low power dissipation and reasonable cost, regulated by stringent requirements. In that regard, this section reveals a receiver architecture operating at 28 GHz and its typical performance specifications. The relevant ocean scripts implementation is also included to pave the way for the ML assisted receiver design presented in Chapter 5.

## 4.1 Receiver Architecture

Owing to its great tolerance and enhanced selectivity for strong interference, the heterodyne receiver manifests itself as a prevalent architecture in today's commercial mmWave applications. The word "heterodyne" means that the Local Oscillation (LO) frequency is different from the input frequency when a mixer is applied to conduct the downconversion from Radio Frequency (RF) to Intermediate Frequency (IF) [62]. In this work, a standard frequency conversion chain is established on the receiver side by integrating the Low-Noise Amplifier (LNA) with a mixer and cascode amplifier, which can be regarded as the target system whose design process will be optimized by the ML approach later. Beginning with the receiver path, the LNA is first deployed to amplify the weak input signal from the receiving antenna without introducing excessive noise into the system. After that, the mixer is involved to carry out frequency translation as a result to generate the IF output. This output signal is then boosted by the cascode amplifier served as an IF amplifier, thereby preparing the signal for further processing. The diagram of this target system is depicted in Figure 4.1. In terms of the topology used in each individual block, the cascode LNA with an inductive degeneration, serving as the series feedback as shown in Figure 4.2 and 4.3, is deployed to provide substantial power gain while maintaining relatively low noise across a wide bandwidth [63]. As illustrated in Figure 4.4 and 4.5, the double-balanced active mixer implemented by a Gilbert cell topology is responsible for translating the frequency with the conversion gain [64]. Connecting to the output of the mixer, a low-pass filter (LPF) is implemented by a resistor and capacitor to eliminate the undesired high-frequency components. Lastly, the differential cascode amplifier is utilized to further amplify the signal with a high gain and enhanced bandwidth, which is presented in Figure 4.6 and 4.7 [65].

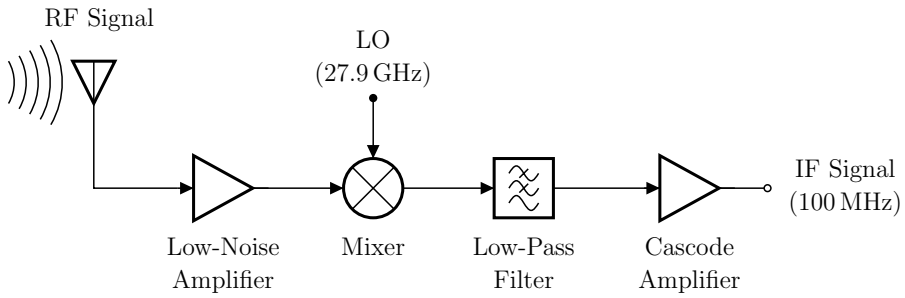


Figure 4.1: A 28 GHz heterodyne architecture comprising LNA, mixer and cascode amplifier.

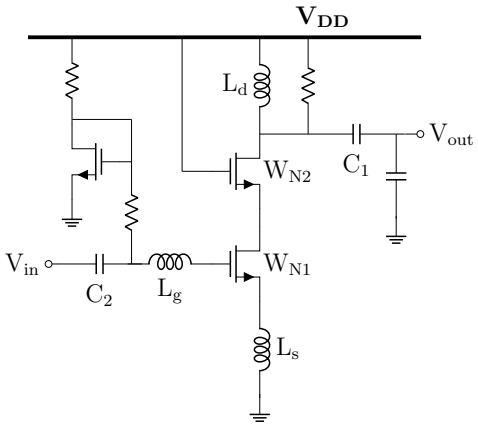


Figure 4.2: Cascode LNA schematic with an inductive degeneration.

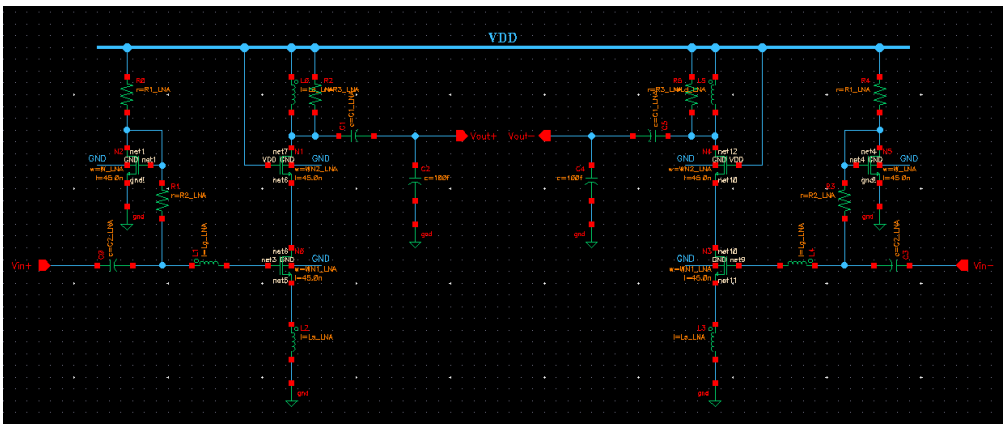


Figure 4.3: LNA implementation with differential configuration using NCSU 45 nm PDK in Cadence Virtuoso

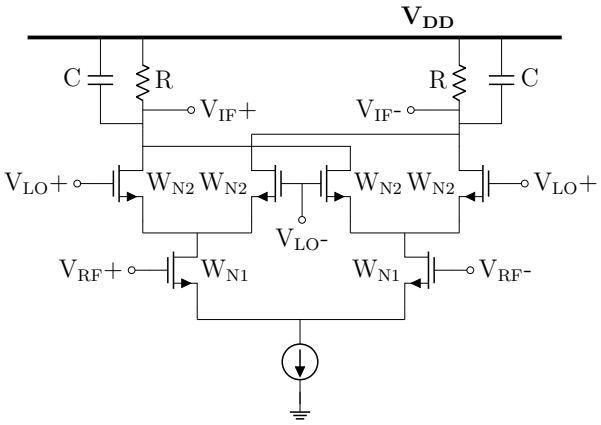


Figure 4.4: Double-balanced Gilbert cell mixer schematic.

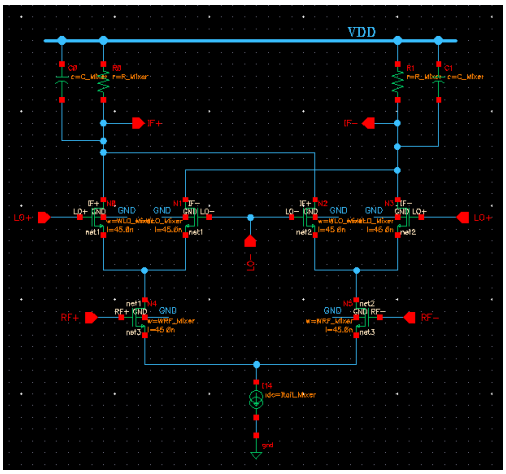


Figure 4.5: Mixer implementation using NCSU 45 nm PDK in Cadence Virtuoso

## 4.2 Performance Specifications Analysis

### 4.2.1 Individual Performance

This part mainly relies on detailed performance specifications of the individual blocks in the receiver systems. These metrics manifest themselves as critical considerations both in the conventional circuit design process and in the new method using the ML approach demonstrated in this work.

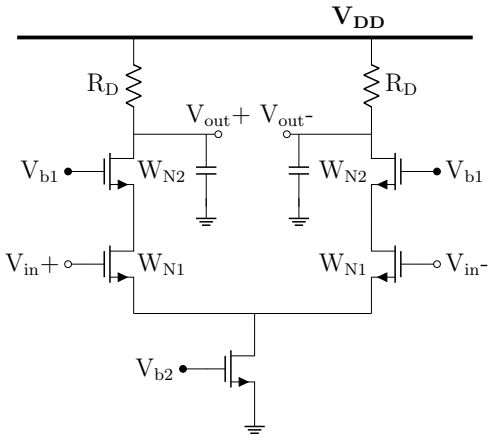


Figure 4.6: Differential cascode amplifier schematic.

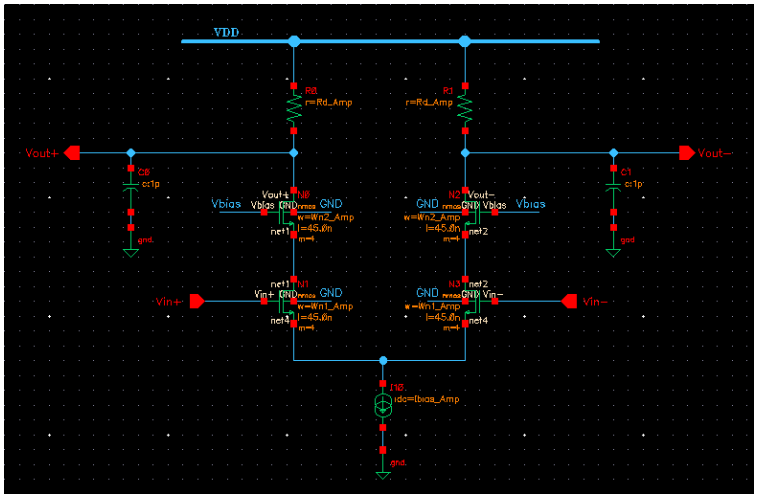


Figure 4.7: Cascode Amplifier implementation using NCSU 45 nm PDK in Cadence Virtuoso

As the first active building block in the receiver front-end, the primary goal of the LNA is to amplify the signal from the receiving antenna with significant gain and relatively low noise. In that respect, the specification related to power gain should first be taken into consideration. In order to clearly indicate this performance, the transducer power gain is used in the LNA to obtain the ratio between the power delivered to the load and the power

available from the source (Eq. (4.1)):

$$G_T = \frac{(1-|\Gamma_S|^2)|S_{21}|^2}{|1-S_{11}\Gamma_S|^2} \times \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{4.1}$$

In conjunction with the power gain, noise figure is another important metric to evaluate the ability to suppress the excessive noise in LNA, which is quantified by the ratio of signal-to-noise ratio between the input and output (Eq. (4.2)):

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i/N_i}{S_o/N_o} = \frac{S_i/N_i}{GS_i/(N_a+GN_i)} = 1 + \frac{N_a}{GN_i} \tag{4.2}$$

Since the noise comes from the random process and it cannot be completely eliminated, the value of noise figure is always larger than 1. In addition, an essential entity called the scattering parameters is implemented to determine the relationships between the inputs and outputs in multi-port system. Specifically, the input port voltage reflection coefficient ($S_{11}$) is worth further consideration in the LNA design at 28 GHz since it can be employed to derive other important specifications, such as input impedance and return loss.

In terms of mixer performance metrics, the primary specification should be conversion gain due to its active configuration. The term "conversion" indicates that the value of this entity comes from the ratio between the output voltage in IF band and the input voltage in RF band (Eq. (4.3)):

$$\frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m R_D \tag{4.3}$$

Besides the conversion gain, voltage swing can be also regarded as an important metric in the mixer design to evaluate the ability to tolerate the large input signal without clipping or compression, thereby examining the stability.

Concerning the relatively simple topology and straightforward relationship between the circuit parameters and relevant performance specifications, the voltage gain is the only selected metric to signify the capability of amplification in the cascode amplifier design, which is calculated based on the ratio between the output voltage and the input voltage.

### 4.2.2 System Performance

For the RF receiver design, the performance named sensitivity manifests itself as a critical specification due to the hostile wireless communication environment, in which the minimum signal level for detecting the inputs with tolerable quality is derived from the noise figure and the output signal-to-noise ratio, as shown in Eq. (4.4):

$$S_{sen}|_{dBm} = -174 + NF_{dB} + 10\log\Delta f + SNR_{out} \tag{4.4}$$

In addition to the sensitivity, the maximum receiving signal power is constrained by 1 dB compression point to signify the high end for the linear operating range when the real output power decreases by 1 dB from the theoretical value. The above two metrics constitute an essential specification called the dynamic range to identify the desired range for successfully detecting the receiving signal with acceptable noise and distortion. In this work, the power consumption and voltage gain are first investigated to examine the energy efficiency and dynamic range of the system comprising the LNA, mixer, and cascode amplifier on receiver side. Moreover, the noise figure is applied to measure the sensitivity performance of the target system, which is based on the Friis' equation (Eq. (4.5)):

$$NF_{Total} = NF_1 + \frac{NF_2 - 1}{G_{A1}} + \cdots + \frac{NF_N - 1}{G_{A1} \times G_{A2} \times \cdots \times G_{A_{N-1}}} \tag{4.5}$$

## 4.3 Ocean Scripts Implementation

The aforementioned contents present the necessity and benefits of utilizing ocean scripts to facilitate repetitive simulations and parametric analysis, it is becoming increasingly more important to conduct the simulation of the complicated system with relatively low time cost and bridge the gap between the Cadence simulator and Python environment.

After integrating the different analysis settings with the corresponding circuit netlists, the ocean file is run from the command line to collect the performance of the target receiver system. Specifically, dc analysis is used to obtain system power consumption with 1.2 V supply voltage. As the indispensable approaches to simulate the periodically-varying circuits, some processes adhered to the periodic steady-state (PSS) analysis are employed to capture the system performance including the voltage gain and noise figure through the Periodic AC (PAC) analysis and Periodic S Parameters (PSP) analysis respectively. In light of the individual block specifications, the Quasi-Periodic Steady State (QPSS) analysis equipped with the shooting engine is adopted to access the gain capability of the system on the receiver side, comprising the power gain of LNA, the conversion gain of mixer, and the voltage gain of cascode amplifier. In addition, SP analysis is leveraged to quantify the noise figure and $S_{11}$ of LNA. For the voltage swing of the mixer, it can be determined by the transient analysis. The schematic of the target system in Cadence and the relevant performance metrics with the ocean scripts implementation are presented in Figure 4.8 and Table 4.1.

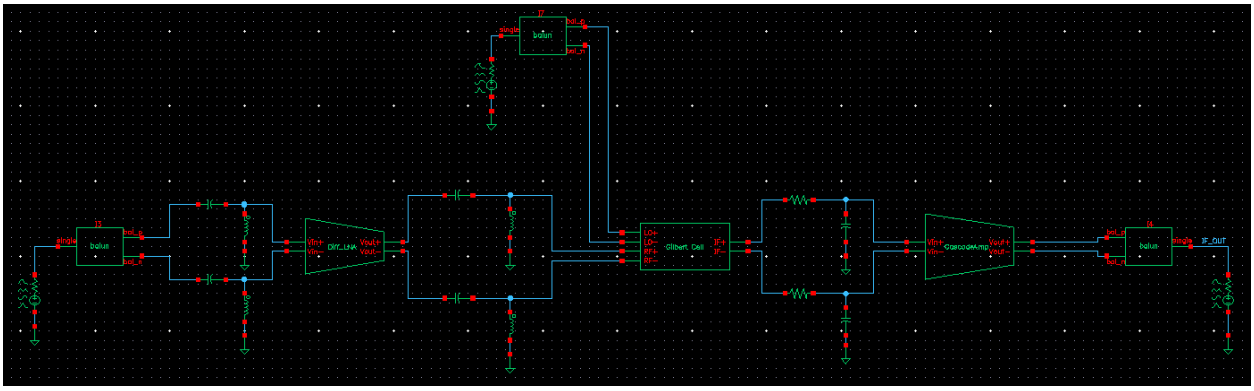


Figure 4.8: Schematic of target system on receiver side in Cadence Virtuoso.

| **Performance Metrics** | **Ocean Scripts** |
|---|---|
| Power Consumption | `getData(":pwr" ?result "dcOp")` |
| Voltage Gain | `ymax(db(vh('pac "/IF_OUT" '-1)))` |
| Noise Figure | `ymin(getData("NF" ?result "psp"))` |
| Power Gain for LNA | `ymax(db10((pvi('qpss "/LNA_OUT+" "/LNA_OUT-" "/I0/Vout+" 0) / (- pvi('qpss "/LNA_IN+" "/LNA_IN-" "/I0/Vin+" 0 '(0 1))))))` |
| Noise Figure for LNA | `ymin(db10(getData("F" ?result "sp_noise")))` |
| $S_{11}$ for LNA | `ymin(db(spm('sp 1 1)))` |
| Conversion Gain for Mixer | `ymax(db10((pvi('qpss "/Mixer_OUT+" "/Mixer_OUT-" "/I1/IF+" 0) / (- pvi('qpss "/Mixer_IN+" "/Mixer_IN-" "/I1/RF+" 0 '(0 1))))))` |
| Voltage Swing for Mixer | `(ymax((vtime('tran "/Mixer_OUT+") - vtime('tran "/Mixer_OUT-") - (v("/Mixer_OUT+" ?result "dcOp") - v("/Mixer_OUT-" ?result "dcOp")))) - ymin((vtime('tran "/Mixer_OUT+") - vtime('tran "/Mixer_OUT-") - (v("/Mixer_OUT+" ?result "dcOp") - v("/Mixer_OUT-" ?result "dcOp"))))) / 2` |
| Voltage Gain for Cascode Amplifier | `ymax(db((vh('qpss "/Amp_OUT+") / harmonic(vh('qpss "/Amp_IN+") '((-1 1))))))` |

Table 4.1: Ocean scripts implementation for different analysis of system in receiver.

# Chapter 5

# Machine Learning Based Transceiver Circuits Design

The previous contents have elaborated the architecture of two systems on both the transmitter and receiver sides whose operating frequency is 28 GHz. Since these systems include heterogeneous blocks, such as the LNA, mixer, and cascode amplifier in the receiver architecture, the direction of optimizing their performance cannot be obtained in a straightforward way. In addition, more sophisticated CMOS processes and relatively intricate trade-offs lead to other impediments to the mmWave circuit design. In that regard, this section primarily concentrates on the ML approaches consisting of the problem statement, benchmark data collection, and model evaluation leveraging the conventional and large-scale algorithms, which are employed to accelerate the design process of mmWave circuits.

## 5.1 Problem Statement

Typically, the circuit design starts with the selection of the appropriate topology confined by the desired performance, such as the power consumption and the voltage gain. Following that, the key circuit parameters in the chosen topology are identified and determined by experienced circuit designers leveraging their knowledge to find the approximate solution and then conduct iteration for the values of diversified parameters until the required specifications are fulfilled. In contrast, ML-based circuit design carries out a reverse process, as formulated in Eq. (5.1):

$$\boldsymbol{x} = \mathcal{M}(\boldsymbol{y}), \tag{5.1}$$

In particular, $\mathcal{M}$ represents the dedicated ML model to predict the output $\boldsymbol{x}$ that entails a set of circuit parameters given the performance specification vectors denoted by $\boldsymbol{y}$. This approach is deployed to directly learn the relationship between the desired performance and circuit parameters, thereby accelerating the design process rather than implementing the time-consuming iterations.

## 5.2 Data Collection

For the two target systems with five different individual blocks, the corresponding circuit schematics are first created in Cadence Virtuoso using NCSU 45 nm Processing Design Kit (PDK). Then, the initial circuit parameters are set to reasonable values developed by the prior knowledge of the circuit designer as a result to provide a reliable starting point for ML model training later. For each parameter, the value is swept with a small step size in a certain variation range, and the related performance metrics are obtained from the simulation results shown in Cadence spectre simulator. Based on the complexity of each circuit block,

a different number of parameters are selected during the process of simulation. In addition, the length of each transistor is fixed at 45 nm to simplify the design space and mitigate short-channel effects. In order to facilitate the training process, the circuit parameters are merged with the corresponding specifications to establish the dataset that will be further split by the training and testing components. The entire data collection procedure is illustrated in Figure 5.1, and the sweeping range of circuit parameters presented in the created dataset is listed in Table 5.1.

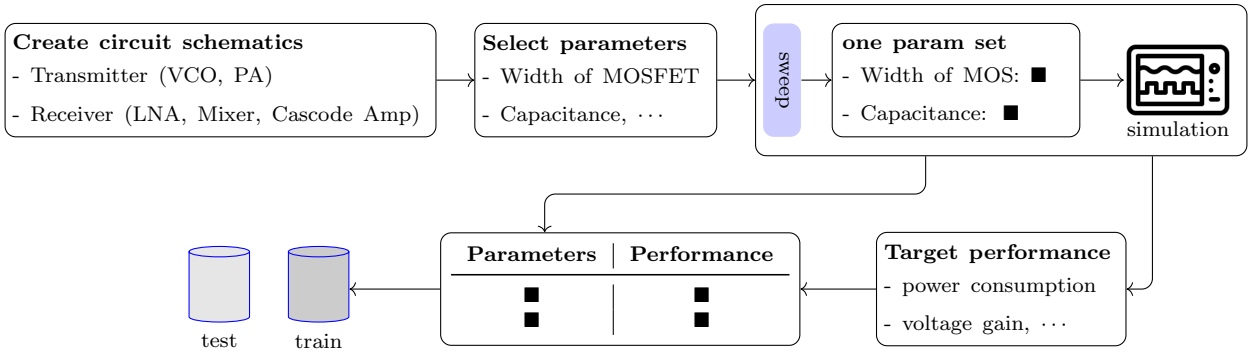


Figure 5.1: Procedure for creating datasets for 28 GHz transceiver circuits

## 5.3 Model Evaluation

With the dataset collected from the two mmWave systems following the procedure illustrated above, some conventional and modern large-scale ML algorithms are employed to determine the relationship between the input specifications and the output parameters. In particular, the Random Forest (RF), Support Vector Regression (SVR), Multi-layer Perceptron (MLP), and Transformer are utilized to develop the predictions for diversified circuit parameters based on desired performance metrics. To cope with high nonlinearity and intricate trade-offs of mmWave system design, the most nonlinear kernel named rbf is selected for SVR model, and a rectified linear unit (ReLU) activation function is utilized in MLP model. The detailed characteristics for each model are itemized in Table 5.2 and the evaluation of these

| System-Level Circuits | Individual Block | Parameter | Sweeping Range |
|---|---|---|---|
| Transmitter system<br>**specs**:<br>dc power \| bw \| output power \| voltage swing | Voltage-Controlled Oscillator (VCO)<br>**specs**:<br>phase noise \| tuning range | C | 50:50:150 (fF) |
| | | L | 60:60:180 (pH) |
| | | $R_p$ | 300:100:500 (Ω) |
| | | $W_{N1}$ | 7.5:2.5:12.5 (μm) |
| | | $W_{N2}$ | 187.5:12.5:212.5 (μm) |
| | | $W_{var}$ | 70:10:90 (μm) |
| | Power Amplifier (PA)<br>**specs**:<br>power gain \| drain efficiency \| PAE | $L_{ip}$ | 175:175:350 (pH) |
| | | $L_{is}$ | 60:60:120 (pH) |
| | | $L_{op}$ | 360:353:713 (pH) |
| | | $L_{os}$ | 45:45:90 (pH) |
| | | $W_{N1}$ | 22:5:32 (μm) |
| | | $W_{N2}$ | 16:5:26 (μm) |
| Receiver system<br>**specs**:<br>dc power \| gain \| noise figure | Low-Noise Amplifier (LNA)<br>**specs**:<br>power gain \| $S_{11}$ \| noise figure | $C_1$ | 130:50:180 (fF) |
| | | $C_2$ | 170:50:220 (fF) |
| | | $L_d$ | 180:50:230 (pH) |
| | | $L_g$ | 850:100:950 (pH) |
| | | $L_s$ | 80:10:90 (pH) |
| | | $W_{N1}$ | 20:3:26 (μm) |
| | | $W_{N2}$ | 37.5:2.5:42.5 (μm) |
| | Mixer<br>**specs**:<br>voltage swing \| conversion gain | C | 1:0.1:1.1 (pF) |
| | | R | 400:100:500 (Ω) |
| | | $W_{N1}$ | 14:2:18 (μm) |
| | | $W_{N2}$ | 6:2:10 (μm) |
| | Cascode Amplifier<br>**specs**:<br>gain | $R_D$ | 300:100:400 (Ω) |
| | | $W_{N1}$ | 26:2:30 (μm) |
| | | $W_{N2}$ | 14:2:18 (μm) |

Table 5.1: The chosen parameters and specifications for transceiver circuits and each individual block. The sweeping range of selected design parameters is written in the form of [begin, increment, end].

models is also presented using the mean-square loss as an objective function. As shown in Eq. (5.2), the difference between the performance based on the predicted parameters $\hat{\boldsymbol{y}}$ and the desired counterpart $\boldsymbol{y}$ is formulated by means of individual error in each specification and the aggregated error.

$$\text{individual error} : err_i = \|\boldsymbol{y}_i - \hat{\boldsymbol{y}}_i\|/\boldsymbol{y}_i \quad \text{aggregated error} : err = \|\boldsymbol{y} - \hat{\boldsymbol{y}}\|/\boldsymbol{y} \tag{5.2}$$

In terms of Python implementation, an end-to-end model training and evaluation pipeline is adopted in this work, which facilitates the interaction between the ML workflow and

| Model | Parameter | Value |
|---|---|---|
| Random Forest (RF) | n_estimators | 100 |
| | criterion | squared_error (L2 Loss) |
| Support Vector Regressor (SVR) | kernel | rbf |
| | multi_target_regression_type | MultiOutputRegression |
| Multi-layer Perception (MLP) | num_layers | 7 |
| | dim_layers | [200, 300, 500, 500, 300, 200] |
| Transformer | dim_model | 200 |
| | num_heads | 2 |
| | dim_hidden | 200 |
| | dropout_p | 0.1 |
| | num_encoder_layers | 6 |
| | activation | relu |

Table 5.2: Various ML models and their selected parameters.

train

```
def Train(model, trainset):
  for _ in range(maxIter):
    x, y = loadData(trainset)
    xPred = model(y)
    loss = MSE(x, xPred)
    # update model
    model.fit(x, y)
```

evaluation

```
def Eval(model, evalset, simulator):
  for _ in range(maxIter):
    x, y = loadData(evalset)
    xPred = model(y)
    # circuit workflow
    # simulator: all circuit information
    yPred = simulator.run(xPred)
    error = calcError(y, yPred)
```

simulation

```
class Simulator():
  ...
  def run(self, xPred):
    alterCircParam(xPred)
    # call Cadence simulator
    call(cadenceCommand)
    yPred = parseResults()
```

Figure 5.2: An end-to-end model training and evaluation pipeline.

the circuit design process, as depicted in Figure 5.2. By employing the trained model, the predicted parameters based on the desired specifications are obtained in the first place. Then, the simulator in Cadence Virtuoso is invoked to conduct the simulation and compare the theoretical performance with the predicted performance, thereby calculating the relative error by virtue of the mean-square loss function mentioned above.

# Chapter 6

# Conclusion and Future Works

## 6.1 Conclusion

In this thesis, the background of 5G wireless communication using the mmWave frequency band is introduced comprising top-level technologies and integrated circuit application. Following that, the motivation and literature review sections indicate the necessity of establishing the automation pipeline for analog/RF circuit design. In that case, two target mmWave systems are investigated on the transmitter and receiver sides with the schematic design and the performance metrics selection, in which the chosen specifications are implemented by ocean scripts leveraging various analysis methods. Consequently, ML approaches are explored to facilitate circuit design with different models consisting of conventional and large-scale algorithms, which entails superior performance for both accuracy and efficiency.

## 6.2 Future Works

In this section, some possible directions of future work are specified from the perspective of circuit design and ML algorithms. In terms of circuit design, topology selection and layout establishment can be regarded as other critical tasks that need to be optimized by ML approaches attributed to time-consuming and labor-intensive processes. For the ML algorithms point of view, the reinforcement learning and graph convolutional neural network (GCN) can also be considered as the powerful candidates to optimize the design process for mmWave integrated circuits. Finally, the sampling methods leading to the enhanced data efficiency are worth more research efforts in the future, especially for more complicated system design.

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