Title
Low Resistance Contact to P–Type Monolayer WSe2

Journal
Nano Letters, 24(20)

ISSN
1530-6984

Authors
Xie, Jingxu
Zhang, Zuocheng
Zhang, Haodong
et al.

Publication Date
2024-05-22

DOI
10.1021/acs.nanolett.3c04195

Peer reviewed

Low Resistance Contact to P-type Monolayer WSe2

Journal:	*Nano Letters*
Manuscript ID	nl-2023-04195c.R4
Manuscript Type:	Communication
Date Submitted by the Author:	30-Apr-2024

Complete List of Authors:	Xie, Jingxu; UC Berkeley, Physics Zhang, Zuocheng; University of California Berkeley Zhang, Haodong; UC Berkeley Nagarajan, Vikram; UC Berkeley Zhao, Wenyu; University of California Berkeley, Physics Kim, Ha-Leem; UC Berkeley, Sanborn, Collin; UC Berkeley Qi, Ruishi; Peking University, School of Physics Chen, Sudi; UC Berkeley Kahn, Salman; UC Berkeley Watanabe, Kenji; National Institute for Materials Science, Taniguchi, Takashi; National Institute for Materials Science, Zettl, Alex; University of California Berkeley, Physics Crommie, Michael; University of California Berkeley, Physics analytis, james; University of California Berkeley, Physics Wang, Feng; University of California Berkeley, Department of Physics

Low Resistance Contact to P-type Monolayer WSe_2

Jingxu Xie[1,2,3*], Zuocheng Zhang[1*], Haodong Zhang[1*], Vikram Nagarajan[1], Wenyu Zhao[1], Ha-Leem Kim[1,3], Collin Sanborn[1], Ruishi Qi[1,3], Sudi Chen[1], Salman Kahn[1], Kenji Watanabe[4], Takashi Taniguchi[5], Alex Zettl[1,3,6], Michael F. Crommie[1,3,6], James Analytis[1,3,6], Feng Wang[1,3,6]†

[1] Department of Physics, University of California at Berkeley, Berkeley, California 94720, United States

[2] Graduate Group in Applied Science and Technology, University of California at Berkeley, Berkeley, California 94720, United States

[3] Material Science Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States

[4] Research Center for Electronic and Optical Materials, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan

[5] Research Center for Materials Nanoarchitectonics, National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan

[6] Kavli Energy NanoSciences Institute at University of California Berkeley and Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States

* These authors contributed equally to this work

† Correspondence to: fengwang76@berkeley.edu

Abstract

Advanced microelectronics in the future may require semiconducting channel materials beyond silicon. Two-dimensional (2D) semiconductors with their atomically thin thickness, hold great promise for future electronic devices. One challenge to achieving high-performance 2D semiconductor field effect transistors (FET) is the high contact resistance at the metal-semiconductor interface. In this study, we develop a charge-transfer doping strategy with WSe_2/α-$RuCl_3$ heterostructures to achieve low-resistance ohmic contact for p-type monolayer WSe_2 transistors. We show that hole doping as high as 3×10^{13} cm^{-2} can be achieved in the WSe_2/α-$RuCl_3$ heterostructure due to its type-III band alignment, resulting in an ohmic contact with resistance of 4 kΩ μm. Based on that, we demonstrate p-type WSe_2 transistors with an on-current of 35 $\mu A \cdot \mu m^{-1}$ and an I_{ON}/I_{OFF} ratio exceeding 10^9 at room temperature.

Keywords:

Ohmic contacts, p-type monolayer WSe_2 FET, charge transfer, type-III band alignment, α-$RuCl_3$

The family of transition-metal dichalcogenide (TMD) materials possesses exceptional characteristics, including atomically thin structures and the absence of dangling bonds, that make them ideal candidates for advanced electronic applications[1-12]. However, it is challenging to form low-resistance electrical contact to TMD monolayers due to the Schottky barrier between the three-dimensional metal and the two-dimensional (2D) semiconductors. This issue can limit the ultimate scaling and performance of TMD-based 2D electronic devices[3, 13-17]. Heavy substitutional doping, widely used to achieve low resistance ohmic contact to bulk semiconductors, does not work well for atomically thin 2D materials[3]. A variety of new contact strategies have been explored to realize ohmic contact to TMD materials[18-21]. For n-type TMD monolayers such as MoS_2, there has been impressive progress where a contact resistance as low as 123 Ω μm has been demonstrated[20]. In contrast, low-resistance ohmic contact to p-type monolayer semiconductors is more challenging. Recently, there have been various methods developed to improve p-type contacts to monolayer WSe_2, such as metal-hBN transfer[22], MOCVD synthesis[23], and NO_x doping at the contact regions[24]. However, further research is still needed to achieve reliable and low-resistance p-type contact to TMD monolayers.

Here we present a new alternative approach to achieving ohmic contact to monolayer WSe_2 and demonstrate p-type WSe_2 field-effect transistors. Our approach utilizes charge-transfer doping in the WSe_2/α-$RuCl_3$ heterostructure with type-III band alignment. Figure 1a illustrates the type-III band alignment between monolayer WSe_2 and α-$RuCl_3$, wherein the conduction band minimum of α-$RuCl_3$ is positioned lower than the valence band maximum of monolayer

WSe_2. The energy difference between these two levels is approximately 0.8 eV[25]. When WSe_2 is in close proximity to α-$RuCl_3$, electrons in WSe_2 will spontaneously transfer to α-$RuCl_3$ which has lower energy. As a result, the WSe_2 contact regions are heavily hole-doped. The increase in the doping level leads to a narrower depletion region such that field emission takes place to reduce the barrier height (Supplementary Figure S1)[26-28]. Previously, highly efficient charge transfer doping of graphene by α-$RuCl_3$ has been observed[29-31]. Recent optical spectroscopy shows that strong charge transfer doping of WSe_2 is present in WSe_2/α-$RuCl_3$ heterostructures[32] and this doping could improve electrical contact to the WSe_2 layer[33]. Here we quantify charge transfer charge density in WSe_2 monolayer through Hall measurements and demonstrate good p-type field effect transistor performance using the charge-transfer doped electrical contacts.

To examine the contact resistance of monolayer WSe_2 with an α-$RuCl_3$ charge transfer interface, we fabricated monolayer WSe_2 devices for the transmission line method[34] (TLM) measurement, which is a commonly used technique for determining the contact resistance in electronic devices. Figure 1b shows the schematic side view of the TLM device and Figure 1c presents the optical image of the device where the sample width is 7 μm (WSe_2 is outlined by the blue solid line). The 10nm-thick platinum electrodes[35-37] were pre-patterned on a SiO_2/Si substrate with separation ranging from 0.3 μm to 3 μm. A monolayer WSe_2 that was fully covered by a few-layer α-$RuCl_3$ flake (outlined by the orange solid line) was then released on top of the platinum electrodes. During this process, we didn't intend to align WSe_2 and α-$RuCl_3$, and the twist angles are random in different devices. The bottom contact was used to avoid

direct evaporation of metals to monolayer WSe_2 because the evaporation requires high energy for sublimation and the transfer of this energy to monolayer TMD leads to the formation defects that pin the Fermi level near the conduction band and results in poor contacts[18].

The I-V curves of different electrodes at room and low temperatures were measured and plotted in Figure 2a, b. Linear characteristics were observed at both room temperature (Figure 2a) and low temperature (Figure 2b), indicating the absence of the Schottky barrier at the contact interface and the presence of ohmic contacts. The contact resistance values extracted from the TLM method at different temperatures are presented in Figure 2c, d, showing the contact resistance values (R_C) of 4 kΩ μm at room temperature and 4.5 kΩ μm at low temperature (extracted after subtracting the resistance of Platinum electrodes). We also evaluated the contact resistance using gold/graphite/WSe_2/α-$RuCl_3$ contacts (Supplementary Figure S2) as well as another TLM device (Supplementary Figure S3). Similar results were observed in all these devices, suggesting the robustness and consistency of the contact interface. This low contact resistance value could contribute to more efficient charge carrier injection, which may in turn enhance device performance and overall functionality. We also note that the contact resistance between metal and α-$RuCl_3$ is above 40 kΩ μm at room temperature, and the flake itself has a resistance > 1 MΩ μm at low temperature[38], thus its contribution to the contact resistance of WSe_2 is negligible.

To quantify the charge transfer doping level in the WSe_2/α-$RuCl_3$ heterostructure, the Hall measurement was employed. We fabricated monolayer WSe_2/α-$RuCl_3$ devices with standard

Hall-bar electrodes (Figure 3a) which are made of prepatterned few-layer graphite (outlined by the purple lines). We note that the ideal Hall bar would be point contacts and aligned perpendicular to the current to avoid the pickup of R_{XX}. We use the anti-symmetrized Hall resistance to remove the effect of non-ideal geometry. Figure 3b shows the Hall resistance R_{XY} as a function of perpendicular magnetic field B at room and low temperatures. The R_{XY} increases linearly with the perpendicular magnetic field. The positive sign of the Hall slope confirms the hole doping in the monolayer WSe_2. From the linear fit to Hall resistance, we estimate a hole carrier density of 3.1×10^{13} cm^{-2} at room temperature and 3.3×10^{13} cm^{-2} at low temperature. Similar charge-transfer hole densities are observed in another two monolayer WSe_2/α-$RuCl_3$ Hall bar devices (Supplementary Figure S4 and S5). The three devices give an average hole density of 2.9×10^{13} cm^{-2} with a standard deviation of 0.1×10^{13} cm^{-2} at room temperature. This confirms that the monolayer WSe_2 contact region has undergone heavy hole doping through the charge transfer mechanism with α-$RuCl_3$. Compared to other charge transfer methods like NO_2[39] and WO_x[40] whose charge transfer hole doping is in the level of $1\sim2\times10^{12}$ cm^{-2}, we achieved an order of magnitude higher hole doping. It is also higher than what can typically be achieved by conventional gate injection methods using hBN as the dielectric[41], where the hole carrier density is typically less than 1×10^{13} cm^{-2}. From the TLM and Hall measurements, we get a mobility of 21 $cm^{-1}V^{-1}s^{-1}$ in the contact regions. This value is low because the WSe_2 monolayer is in direct contact with α-$RuCl_3$ in the TLM and Hall bar devices, and charges on the interface of α-$RuCl_3$ can scatter the carriers in WSe_2 effectively.

The low contact resistance to monolayer WSe_2 could enable us to achieve high-performance p-type monolayer WSe_2 field-effect transistors (FETs). Figure 4a depicts the schematic side view of an FET device and Figure 4b presents the corresponding optical image. The contact regions of WSe_2 are positioned between few-layer graphite and few-layer α-$RuCl_3$, forming a sandwich structure. The α-$RuCl_3$ flakes were pre-patterned by AFM cutting[42] to make an FET channel length of around 0.5 μm. Then chromium and gold (typically 5 nm and 50nm) were sequentially deposited on the few-layer graphite contacts to make the electrodes.

The switching behavior of our monolayer WSe_2 FET was characterized at room temperature in the configuration presented in Figure 4a. A few-layer graphene and a 30 nm hBN were used as a top gate and a gate dielectric, respectively. We swept both the top gate voltage (V_{GS}) and the drain-source bias voltage (V_{DS}) across the monolayer WSe_2 conductive channel. Figure 4c shows the 2D color plot of drain-source current I_{DS} as a function of V_{DS} and V_{GS} at room temperature. A typical FET behavior is observed: as the top gate voltages V_{GS} increases, the FET undergoes a transition from the off state to the on state. The on-state drain-source current can be as high as 31 μA μm^{-1} at V_{GS} = -16 V, where the gate-induced carrier density in the monolayer WSe_2 channel is 0.7×10^{13} cm^{-2}, and the overall two-terminal resistance is 28 kΩ μm. We also extracted the Schottky barrier height to be 1.5 meV at the flat-band voltage[3, 43, 44] (Supplementary Figure S6).

Figure 4d depicts the measured drain-source I_{DS}-V_{DS} curves, corresponding to the horizontal line cuts in Figure 4c, where the drain-source current I_{DS} varies linearly with V_{DS}. The reliable

and ohmic nature of the contact is crucial for the practical utilization electronic devices, providing its potential in various technological applications.

Figure 4e presents the transfer characteristics of the monolayer WSe_2 FET device, corresponding to the vertical line cuts in Figure 4c. The observed current variation for different values of top gate voltages V_{GS} suggests that the field-effect behavior of our transistor is primarily governed by the monolayer WSe_2 channel rather than the contacts. For a drain-source bias voltage V_{DS} = -100mV, we observe an on-current of 4 μA μm^{-1}. At drain-source bias voltage V_{DS} = -1V, the maximal measured on-current is 31 μA μm^{-1}, indicating the device's ability to conduct current in the on state. From the slope of the I_{DS}-V_{GS} curve, we get a mobility of 287 $cm^{-1}V^{-1}s^{-1}$ for the pristine WSe2 channel. This mobility is higher than that of the TLM and Hall devices because the WSe_2 channel layer is sandwiched between hBN and not affected by the α-$RuCl_3$. Additionally, the device exhibits a low off-state current of approximately 10^{-8} μA μm^{-1}, making it suitable for applications in devices with low standby power dissipation. The measured drain current modulation, with an on/off current ratio I_{ON}/I_{OFF} exceeding 10^9, highlights the performance of the monolayer WSe_2 transistor with α-$RuCl_3$ contacts. Low-temperature characteristics are shown in Supplementary Figure S7. The observed high on/off current ratio is beneficial for achieving rapid switching and short latency devices if the on-state current is further increased by optimizing the device structure. Simultaneously, the low off-state current is helpful for minimal static power consumption, making it promising for applications in digital electronics.

The subthreshold swing is a measure of the efficiency of a transistor in controlling the current flow when it operates in the subthreshold region[45]. We observed a subthreshold swing of approximately 0.7 V per decade in our monolayer WSe_2 transistor with α-$RuCl_3$ contacts, which is higher compared to that in commercial silicon-based devices (~70 mV per decade at room temperature). We suspect the rather big subthreshold swing may be attributed to the large thickness of the hBN dielectric (~30 nm) used in this device. Further optimization by using a thinner hBN of about 15nm can reduce the subthreshold swing to approximately 0.2 V per decade (Supplementary Figure S8). And another device showed a subthreshold swing of 0.3V per decade (Supplementary Figure S9). These improvements suggest that the choice of gate dielectric can play an important role in optimizing the subthreshold swing and overall device performance. Therefore we can further reduce the subthreshold swing by using a gate dielectric with a thinner thickness or higher dielectric constant, such as HfO_2[46] or Bi_2SeO_5[47], allowing for more efficient modulation of the carrier density in the monolayer WSe_2 channel. Another possible explanation is that there is a jump of the doping profile at the edge between the contact region (heavily hole-doped ~3×10^{13} cm^{-2}) and the channel region (moderately hole-doped 10^{11} ~ 10^{12} cm^{-2}) that may introduce some energy barrier and limit the current. A further optimization of the device structure with a partial gate to smooth the doping profile near the edge may be helpful.

For potential applications in digital and radiofrequency devices, saturation of the drain current is crucial for achieving maximum operation speeds[48]. At room temperature, a current saturation can be achieved at all gate voltages within the high drain-source bias region (Figure

4f). And the saturation current can be as high as 39 μA μm^{-1}. Furthermore, the electrical contacts exhibit ohmic behavior within the linear region at low drain-source biases. The presence of this saturation behavior, which is not typically observed in graphene-based FET devices[48], is important for achieving high power gains. Because our channel material is a 0.7 nm thick monolayer WSe_2[39], it would be resilient against short-channel effects when the channel length is scaled down to the nanometer range. Therefore, monolayer WSe_2 with α-$RuCl_3$ contacts could be promising for high-speed field-effect device applications. We note that our device exhibits relatively low on-state conductance and relatively high threshold drain-source bias compared to typical silicon-based devices. These characteristics might be limited by the long channel length in our current device. By reducing the channel length to the nanometer scale and utilizing a thinner gate dielectric or a high-k dielectric, we could anticipate improved device performance, including larger saturation current and lower threshold bias. Further investigations are required to explore and evaluate the limits of device performance for monolayer WSe_2 FETs with α-$RuCl_3$ contacts.

To summarize, we provide a proof-of-principle demonstration of low-resistance p-type ohmic contact to monolayer WSe_2 by utilizing α-$RuCl_3$ as a charge transfer interface, which enables the heavy hole doping of the contact region with the hole density of ~3×10^{13} cm^{-2}. The contact resistance to monolayer WSe_2 can be as low as 4 kΩ μm. Functional p-type FET devices were fabricated using this new contact technique. Our samples exhibit a drain saturation current at on-state up to 35 μA μm^{-1}, and an on-off ratio of ~10^9 at room temperature.

Supplementary Information: Measurements for additional samples, including low-temperature behaviors.

Methods

Sample preparation and device fabrication. Two-dimensional flakes (monolayer WSe_2, graphite, hBN, α-$RuCl_3$) were prepared in the air by mechanical exfoliation from the bulk crystal on a 90nm SiO_2/Si substrate via the Scotch tape method. The crystal and substrate are heated to 90 ℃ to increase the yield. Monolayer and multilayer flakes were identified with optical microscopy. All the flakes are stored in vacuum desiccators before transfer. We note that the α-$RuCl_3$ flakes will degrade and cannot be picked up if exposed in air for one day. Polypropylene carbon (PPC) and polyethylene terephthalate glycol (PETG) based dry transfer technology were used to subsequently pick up the flakes at 45 ℃ and 70 ℃ in the air. The α-$RuCl_3$ flakes were pre-patterned by atomic force microscopy (AFM) cutting to have a gap of around 0.5 μm before the stacking process to make the monolayer WSe_2 FET. The devices are stable in the air since they are encapsulated by the top hBN flakes. Then photolithography and electron-beam lithography were used to pattern the electrodes, during which the devices are heated at 180℃ for 5 minutes after spin-coating the photoresist and e-beam resist. Chromium and gold were sequentially evaporated on the few-layer graphene contact and gate to make electrodes. For the TLM device, the chromium/platinum (typically 3nm and 10nm) electrodes were pre-patterned on a SiO_2/Si substrate before releasing the sample on them. The devices are stable for more than one month after the fabrication process.

Measurements. The transport measurements were performed in a Cryomagnetics superconducting magnet system with a variable temperature insert. Samples were in a Helium environment of around 0.3 bar. Transport characteristics were mainly measured by applying DC voltage with the Keithley 2612B SourceMeter and Keithley 6482 picoammeter. The Hall measurements were performed by the standard four-probe AC lock-in method using an SRS 830 lock-in amplifier with an AC current of 10nA and frequency of around 17Hz.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Competing interests

The authors declare that they have no competing interests.

Acknowledgments

The electrical transport measurements are supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, Materials Sciences and Engineering Division (DE-AC02-05-CH11231), within the van der Waals Heterostructure Program (KCWF16). The lithography patterning is supported by Army Research Office award W911NF2110176. The WSe2 monolayer-RuCl3 heterostructure fabrication is supported by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Quantum Systems Accelerator. K.W. and T.T. acknowledge support from the JSPS KAKENHI (Grant

Numbers 21H05233 and 23H02052) and World Premier International Research Center Initiative (WPI), MEXT, Japan.

Author contributions

F. W. conceived the research. F. W. and J. A. supervised the project. J. X., H. Z., and Z. Z. fabricated the device and performed most of the experimental measurements together. W. Z., C. S., R. Q., S. C., S. K., M. C., and A. Z. contributed to the fabrication of van der Waals heterostructures. H. K. contributed to the electrical transport measurements. J. X., Z. Z., and F. W. performed data analysis. K. W. and T. T. grew hBN crystals. V. N. grew α-$RuCl_3$ crystals. All authors discussed the results and wrote the manuscript.

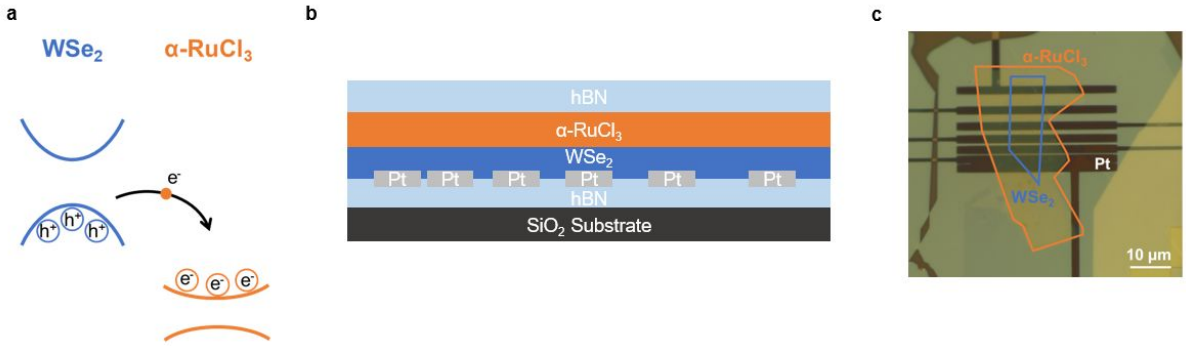


Figure 1: WSe_2/α-$RuCl_3$ band alignment and contact resistance measurements. (a) Type-III band alignment of WSe_2 and α-$RuCl_3$. The conduction band minimum of α-$RuCl_3$ is lower than the valence band maximum of WSe_2 and there is a spontaneous charge transfer between WSe_2 and α-$RuCl_3$, resulting in a heavily doped WSe_2 layer. (**b**) Schematic side view of the device for transmission line method (TLM). (**c**) Optical image of the TLM device. The separation between electrodes ranges from 0.3 μm to 3 μm. The blue and orange shapes mark the monolayer WSe_2 and α-$RuCl_3$ region, respectively.

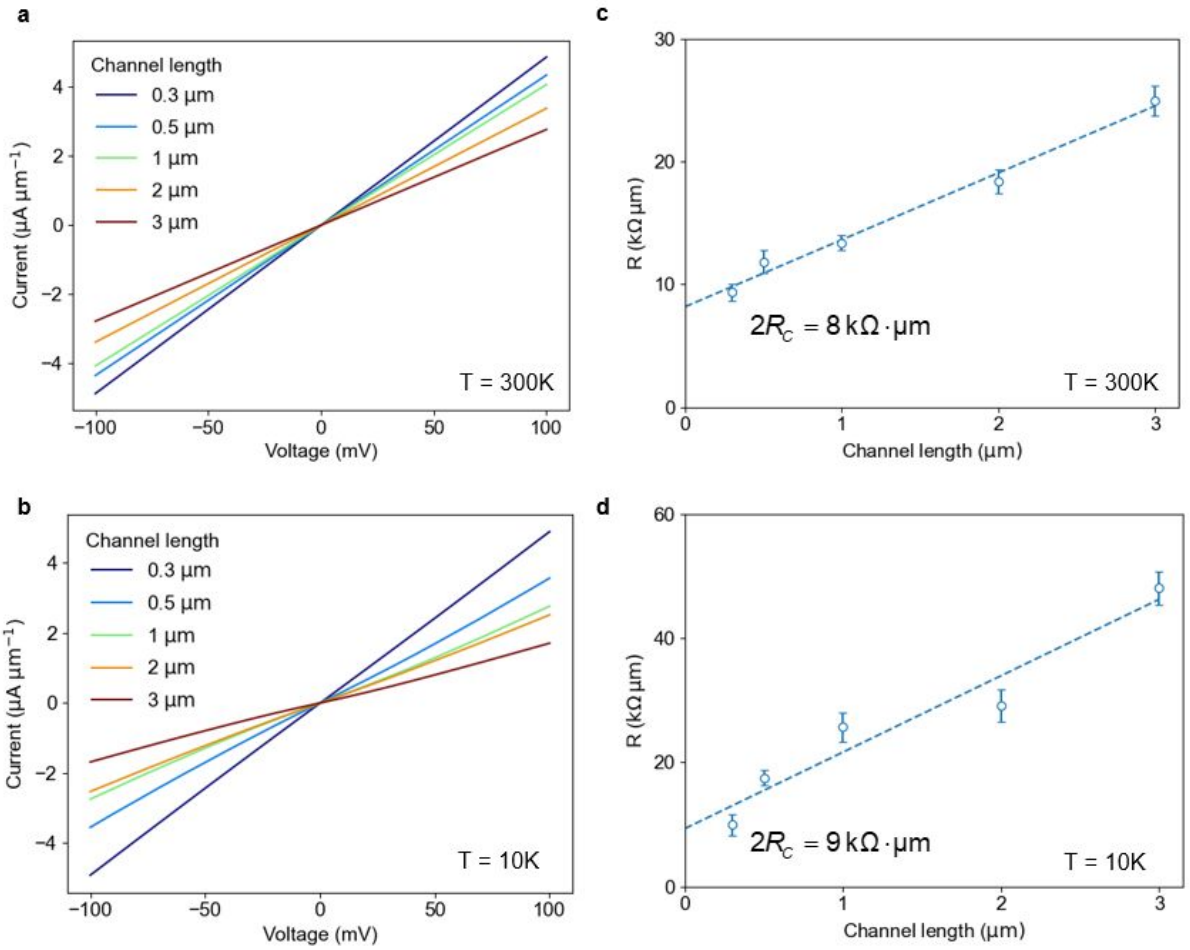


Figure 2: Contact resistance to a monolayer WSe_2 with the Pt/WSe_2/α-$RuCl_3$ contact. (**a** and **b**) I-V curves for different channel lengths at room temperature (**a**) and T = 10K (**b**). Linear behavior is observed at both room temperature and low temperature, indicating the absence of a contact barrier. (**c**) and (**d**) Contact resistance R_C extracted using TLM at room temperature (**c**) and T = 10K (**d**).

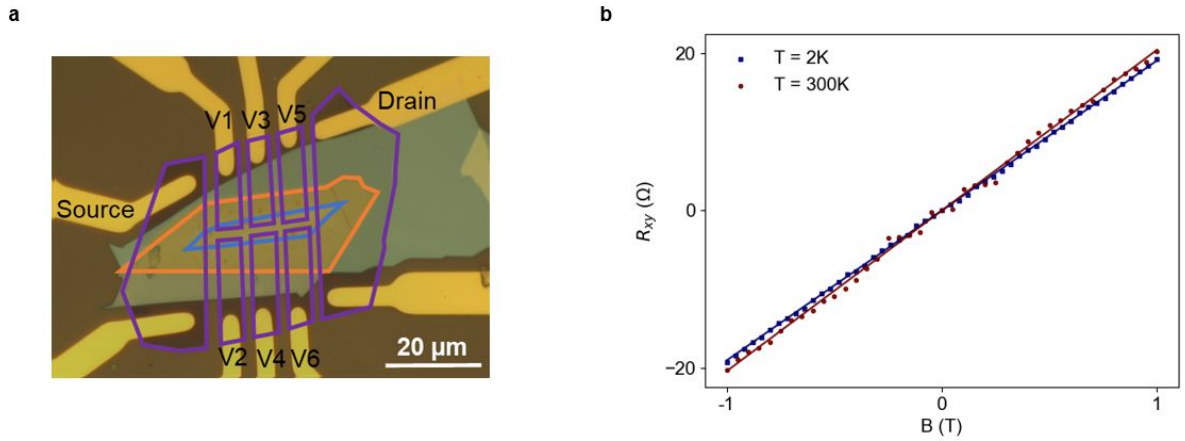


Figure 3: Determination of carrier density in the charge-transfer doped WSe_2 with α-$RuCl_3$. (**a**) Optical image of the multi-terminal monolayer WSe_2/α-$RuCl_3$ device for the Hall measurements. Blue, orange and purple boxes outline the monolayer WSe_2, α-$RuCl_3$, and graphite electrodes, respectively. (**b**) Hall resistance R_{xy} as a function of magnetic field where solid lines are linear fits to the experiment data. The positive sign of Hall slope confirms the hole doping in the monolayer WSe_2. We estimate a hole carrier density of 3.1×10^{13} cm^{-2} at room temperature and of 3.3×10^{13} cm^{-2} at low temperature from the Hall slope.

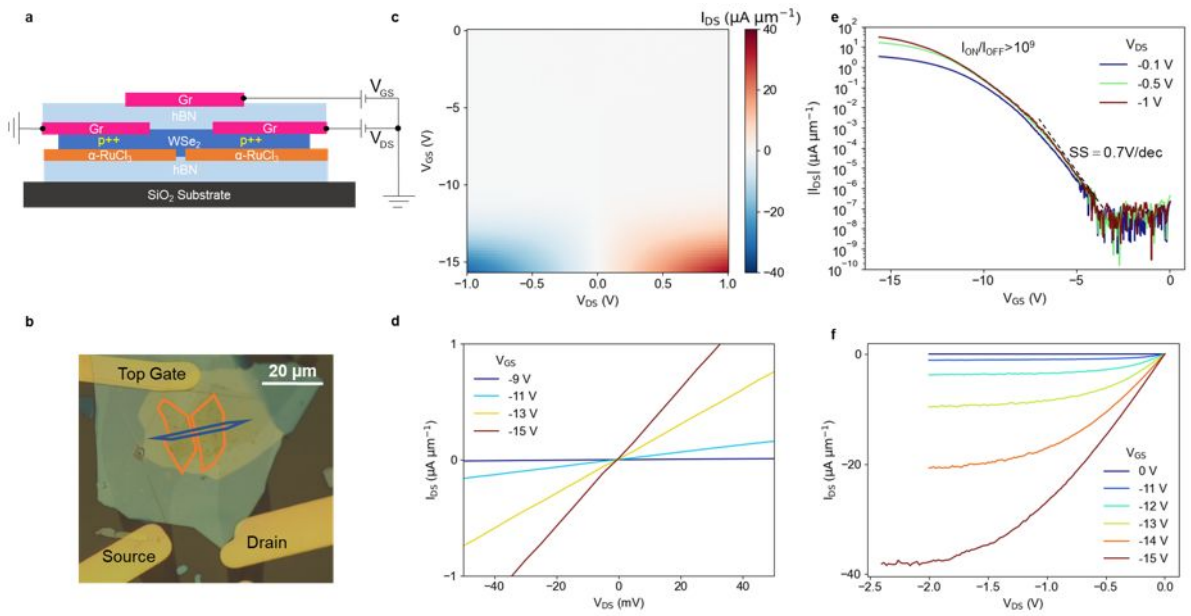


Figure 4: Characterization of monolayer WSe_2 FET. (**a**) Schematic cross-sectional view of FET device structure. The contact regions are sandwiched by a few-layer graphite and a few-layer α-$RuCl_3$. The monolayer WSe_2 channel is separated from the few-layer graphene top gate by a 30-nm-thick hBN (**b**) Optical image of the monolayer WSe_2 FET device. Blue and orange boxes mark the monolayer WSe_2 region and α-$RuCl_3$ contact region, respectively. The channel length and width are 0.5 μm and 2 μm. (**c**) 2D color plot of drain-source current I_{DS} as a function of drain-source voltage V_{DS} and top gate voltage V_{GS} at room temperature. The on-state drain-source current can be as high as 31 μA μm^{-1} when the FET operates at V_{DS}=-1V. (**d**) $I_{DS} - V_{DS}$ characteristics at room temperature. The source-drain current I_{DS} varies linearly with V_{DS} at sufficiently high gate voltages, indicating an Ohmic contact in the on states. (**e**) Drain-source current (on a logarithmic scale) as a function of top gate voltage with drain-source voltage of -0.1V, -0.5V and -1V. For a drain-source bias voltage V_{DS} = -100 mV, an on-current of 4 μA μm^{-1} is observed. At drain-source bias voltage V_{DS} = -1V, the maximum on-current is 31 μA μm^{-1}. The on/off current ratio I_{ON}/I_{OFF} can exceed 10^9 with an off-state current of about 10^{-8}

μA μm^{-1}. The subthreshold swing is around 0.7 V per decade. (**f**) Drain–source current I_{DS} as a function of drain source bias voltage V_{DS} at different top gate voltages. A saturation region is observed for all applied gate voltages.

References

1. Chhowalla M, Jena D, Zhang H. Two-dimensional semiconductors for transistors. Nature Reviews Materials. 2016;1(11):1-15.

2. Novoselov KS, Mishchenko A, Carvalho oA, Castro Neto A. 2D materials and van der Waals heterostructures. Science. 2016;353(6298):aac9439.

3. Allain A, Kang J, Banerjee K, Kis A. Electrical contacts to two-dimensional semiconductors. Nat Mater. 2015;14(12):1195-1205.

4. Kang S, Lee D, Kim J, Capasso A, Kang HS, Park J-W, et al. 2D semiconducting materials for electronic and optoelectronic applications: potential and challenge. 2D Materials. 2020;7(2):022003.

5. Lin Z, Liu Y, Halim U, Ding M, Liu Y, Wang Y, et al. Solution-processable 2D semiconductors for high-performance large-area electronics. Nature. 2018;562(7726):254-258.

6. Li M-Y, Su S-K, Wong H-SP, Li L-J. How 2D semiconductors could extend Moore's law. Nature. 2019;567(7747):169-170.

7. Cao W, Kang J, Sarkar D, Liu W, Banerjee K. 2D Semiconductor FETs—Projections and Design for Sub-10 nm VLSI. IEEE Transactions on Electron Devices. 2015;62(11):3459-3469.

8. Liu C, Chen H, Wang S, Liu Q, Jiang Y-G, Zhang DW, et al. Two-dimensional materials for next-generation computing technologies. Nature Nanotechnology. 2020;15(7):545-557.

9. Ma L, Nguyen PX, Wang Z, Zeng Y, Watanabe K, Taniguchi T, et al. Strongly correlated excitonic insulator in atomic double layers. Nature. 2021;598(7882):585-589.

10. Nguyen PX, Ma L, Chaturvedi R, et al. Perfect Coulomb drag in a dipolar excitonic insulator. arXiv preprint. 2023. https://arxiv.org/abs/2309.14940. (accessed 2024-04-29).

11. Qi R, Joe AY, Zhang Z, et al. Perfect Coulomb drag and exciton transport in an excitonic insulator.

arXiv preprint. 2023. https://arxiv.org/abs/2309.15357. (accessed 2024-04-29).

12. Qi R, Joe AY, Zhang Z, et al. Thermodynamic behavior of correlated electron-hole fluids in van der Waals heterostructures. arXiv preprint. 2023. https://arxiv.org/abs/2312.03251. (accessed 2024-04-29).

13. Razavieh A, Zeitzoff P, Nowak EJ. Challenges and limitations of CMOS scaling for FinFET and beyond architectures. IEEE Transactions on Nanotechnology. 2019;18:999-1004.

14. Tung RT. The physics and chemistry of the Schottky barrier height. Applied Physics Reviews. 2014;1(1):011304.

15. Louie SG, Cohen ML. Electronic structure of a metal-semiconductor interface. Physical Review B. 1976;13(6):2461.

16. Kim C, Moon I, Lee D, Choi MS, Ahmed F, Nam S, et al. Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides. ACS nano. 2017;11(2):1588-1596.

17. Sotthewes K, Van Bremen R, Dollekamp E, Boulogne T, Nowakowski K, Kas D, et al. Universal Fermi-level pinning in transition-metal dichalcogenides. The Journal of Physical Chemistry C. 2019;123(9):5411-5420.

18. Wang Y, Kim JC, Li Y, Ma KY, Hong S, Kim M, et al. P-type electrical contacts for 2D transition-metal dichalcogenides. Nature. 2022;610(7930):61-66.

19. Wang Y, Kim JC, Wu RJ, Martinez J, Song X, Yang J, et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. Nature. 2019;568(7750):70-74.

20. Shen PC, Su C, Lin Y, Chou AS, Cheng CC, Park JH, et al. Ultralow contact resistance between semimetal and monolayer semiconductors. Nature. 2021;593(7858):211-217.

21. Patoary NH, Xie J, Zhou G, Al Mamun F, Sayyad M, Tongay S, et al. Improvements in 2D p-type WSe(2) transistors towards ultimate CMOS scaling. Sci Rep. 2023;13(1):3304.

22. Liu Y, Liu S, Wang Z, Li B, Watanabe K, Taniguchi T, et al. Low-resistance metal contacts to encapsulated semiconductor monolayers with long transfer length. Nature Electronics. 2022;5(9):579-585.

23. Maxey K, Naylor C, O'Brien K, Penumatcha A, Oni A, Mokhtarzadeh C, et al., editors. 300 mm MOCVD 2D CMOS Materials for More (Than) Moore Scaling. 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits); 2022: IEEE.

24. Chiang C-C, Lan H-Y, Pang C-S, Appenzeller J, Chen Z. Air-stable P-doping in record high-performance monolayer WSe 2 devices. IEEE Electron Device Letters. 2021;43(2):319-322.

25. Wang Y, Balgley J, Gerber E, Gray M, Kumar N, Lu X, et al. Modulation Doping via a Two-Dimensional Atomic Crystalline Acceptor. Nano Lett. 2020;20(12):8446-8452.

26. Parker G. Encyclopedia of materials: science and technology. 2001:1581-1587.

27. Rhoderick EH, Williams RH. Metal-semiconductor contacts: Clarendon press Oxford; 1988.

28. Lousberg G, Yu H, Froment B, Augendre E, De Keersgieter A, Lauwers A, et al. Schottky-barrier height lowering by an increase of the substrate doping in PtSi Schottky barrier source/drain FETs. IEEE electron device letters. 2007;28(2):123-125.

29. Rizzo DJ, Jessen BS, Sun Z, Ruta FL, Zhang J, Yan JQ, et al. Charge-Transfer Plasmon Polaritons at Graphene/alpha-RuCl(3) Interfaces. Nano Lett. 2020;20(12):8438-8445.

30. Biswas S, Li Y, Winter SM, Knolle J, Valentí R. Electronic Properties of α− RuCl 3 in proximity to graphene. Physical Review Letters. 2019;123(23):237201.

31. Rizzo DJ, Shabani S, Jessen BS, Zhang J, McLeod AS, Rubio-Verdu C, et al. Nanometer-Scale Lateral p-n Junctions in Graphene/alpha-RuCl(3) Heterostructures. Nano Lett. 2022;22(5):1946-1953.

32. Sternbach AJ, Vitalone RA, Shabani S, Zhang J, Darlington TP, Moore SL, et al. Quenched

Excitons in WSe(2)/alpha-RuCl(3) Heterostructures Revealed by Multimessenger Nanoscopy. Nano Lett. 2023;23(11):5070-5075.

33. Pack J, Guo Y, Liu Z, Jessen B, Liu S, Holtzman L, et al. Improved p-type Contact to WSe 2 Using a α-RuCl3 Charge-Transfer Interface. Bulletin of the American Physical Society. 2023;68(3).

34. Liu Y, Duan X, Shin HJ, Park S, Huang Y, Duan X. Promises and prospects of two-dimensional transistors. Nature. 2021;591(7848):43-53.

35. Fallahazad B, Movva HC, Kim K, Larentis S, Taniguchi T, Watanabe K, et al. Shubnikov-de Haas Oscillations of High-Mobility Holes in Monolayer and Bilayer WSe_2: Landau Level Degeneracy, Effective Mass, and Negative Compressibility. Phys Rev Lett. 2016;116(8):086601.

36. Movva HCP, Fallahazad B, Kim K, Larentis S, Taniguchi T, Watanabe K, et al. Density-Dependent Quantum Hall States and Zeeman Splitting in Monolayer and Bilayer WSe_2. Phys Rev Lett. 2017;118(24):247701.

37. Movva HC, Rai A, Kang S, Kim K, Fallahazad B, Taniguchi T, et al. High-mobility holes in dual-gated WSe2 field-effect transistors. ACS nano. 2015;9(10):10402-10410.

38. Mashhadi S, Weber D, Schoop LM, Schulz A, Lotsch BV, Burghard M, et al. Electrical Transport Signature of the Magnetic Fluctuation-Structure Relation in alpha-RuCl(3) Nanoflakes. Nano Lett. 2018;18(5):3203-3208.

39. Fang H, Chuang S, Chang TC, Takei K, Takahashi T, Javey A. High-performance single layered WSe2 p-FETs with chemically doped contacts. Nano letters. 2012;12(7):3788-3792.

40. Yamamoto M, Nakaharai S, Ueno K, Tsukagoshi K. Self-Limiting Oxides on WSe2 as Controlled Surface Acceptors and Low-Resistance Hole Contacts. Nano Lett. 2016;16(4):2720-2727.

41. Hattori Y, Taniguchi T, Watanabe K, Nagashio K. Anisotropic dielectric breakdown strength of

single crystal hexagonal boron nitride. ACS Applied Materials & Interfaces. 2016;8(41):27877-27884.

42. Li H, Ying Z, Lyu B, Deng A, Wang L, Taniguchi T, et al. Electrode-Free Anodic Oxidation Nanolithography of Low-Dimensional Materials. Nano Lett. 2018;18(12):8011-8015.

43. Liu Y, Guo J, Zhu E, Liao L, Lee S-J, Ding M, et al. Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. Nature. 2018;557(7707):696-700.

44. Zhang S, Chuang H-J, Le ST, Richter CA, McCreary KM, Jonker BT, et al. Control of the Schottky barrier height in monolayer WS2 FETs using molecular doping. AIP Advances. 2022;12(8).

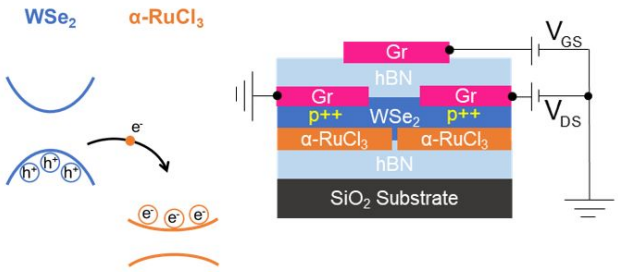
45. Salahuddin S, Datta S, editors. Can the subthreshold swing in a classical FET be lowered below 60 mV/decade? 2008 IEEE International Electron Devices Meeting; 2008: IEEE.

46. Robertson J. High dielectric constant oxides. The European Physical Journal Applied Physics. 2004;28(3):265-291.

47. Zhang C, Tu T, Wang J, Zhu Y, Tan C, Chen L, et al. Single-crystalline van der Waals layered dielectric with high dielectric constant. Nat Mater. 2023;22:832-837.

48. Schwierz F. Graphene transistors. Nat Nanotechnol. 2010;5(7):487-496.

For Table of Contents Only



TOC Graphics