Reliability Challenges in Advance Packaging

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***Abstract*—This paper highlights the packaging related reliability issues in various advanced packaging schemes such as 3-D stacking, interposers, fan-out packaging, and the more recently developed silicon interconnect fabric integration. The need for heterogeneous integration, superior electrical and thermal performance, reduction of form factor and overall system-footprint, and integration of high-density interconnects are the main driving forces behind the development of these advanced packaging techniques. As the packaging and system integration is becoming more complex, the emphasis is mainly on improving the reliability of system-level packaging rather than the individually packaged devices.**

***Index Terms*—3D Stacking, Interposers, Fan-out packaging, Silicon Interconnect Fabric (Si-IF), Reliability**

I. INTRODUCTION

The advanced packaging and system level integration schemes such as system-in-package (SiP), interposers, 3-D stacking are mainly focusing on improving the form factor, reducing the overall foot print, and improving the electrical and thermal performance of the system. A package consists of several hierarchal packaging levels and on the first level, single or a stack of multiple dies (e.g. Hybrid memory cube, HMC) are directly attached to a packaging laminate using micro-bumps. An "Interposer" is often integrated between the chips and package laminate, which provides high density interconnects between various chips (or stacked chips) at very tight pitches (e.g. High bandwidth memory HBM) using C4-bumps or micro-bumps. The package laminated is subsequently mounted on a printed circuit board (PCB) using ball grid arrays (BGAs) or land grid arrays (LGAs) connections. A complex system consists of several such PCBs, which are connected through a mother board or a backplane using mechanical connectors.

A typical package consists of a fairly large number of disparate materials with significantly different material properties such as coefficients of thermal expansions (CTEs), thermal and electrical conductivities, elastic moduli etc. This causes enormous thermo-mechanical stresses on the chips and leads to the so-called chip-package interactions (CPI) which cause cracking of the low-k dielectrics, pulling out of the metal structures and so on [1]. In addition, the package itself can severely warp, and this, in turn, adds additional stresses especially for large area dies. Major reliability issues in an advanced package are highlighted in figure 1.

Fan-out (wafer-level or panel-level) packaging, and the more recently developed "Silicon Interconnect Fabric (Si-IF) integration technology [2] eliminate the use of the packaging laminate in package hierarchy and allow high density integration with improved system performance. The Si-IF integration has an additional advantage compared to the fan-out (FO) package integration by eliminating the use of organic for most part, and using a single packaging hierarchical level and thus completely avoids the use of PCB. The FO package still needs to be mounted on a PCB during system level integration. The commercially FO processes suffer from severe die-shift problems and, therefore, the wiring and interconnect pitch are limited due to overlay accuracy to a few microns. The assembly related failures in Si-IF integration scheme i.e. metal-metal interconnections, passivation and etc. are still under investigation. In the following sections we will highlight main reliability issues in each of the aforementioned advanced packaging and integration schemes.

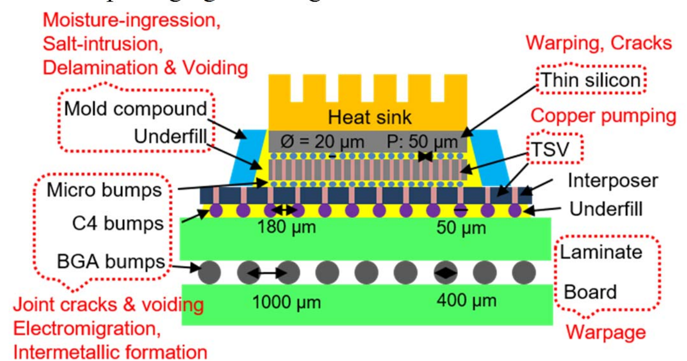

Figure1: Reliability issues in advanced package

II. RELIABLITY ISSUES IN 3D INTEGRATION

1. Micro-bump technology

The interconnections between the stacked dies are realized through micro-bumps, which are the copper pillars capped with a thin solder layer. The large area thinned dies suffer from pre-warpage problems prior to the bonding process. A localized thermal compression bonding (TCB) process is often used to mount the chips in a flip-chip fashion. The pressure helps to keep the die flat against the mounting substrate. This process is subjected to various reliability issues. For instance, excess pressure can cause the solder squish at the joining interfaces, which results in solder bridging, and a very thin solder line consisting of brittle intermetallic compounds. During thermal loading, these interconnects are susceptible to fatigue cracks. .

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2. TSV related stresses

Although the "Through Silicon Vias (TSVs)" are a required feature in 3D-integration, their presence has the potential to have detrimental effects on device performance. A significant CTE mismatch occurs between copper (17 ppm/K) and silicon (2.6 ppm/K), which leads to the creation of localized stresses in the surrounding silicon matrix during thermal excursions. For this reason, researchers have proposed partial filling of TSV with Cu, followed by a complete filling with a polymer of appropriate physical properties [3]. Volant et al. [4] have proposed an annular co-axial TSV that contains a suitable polyimide to overcome the thermomechanical reliability problem. However, the industrial use of bottom-up plating, homogenizing post plating/CMP anneals, and microstructure optimization have reduced the effect of Cu pumping to negligible levels in most cases.

3. Thin silicon issues

The semiconductor chips are very often thinned down in the range of 50-to-100 μm. The main reasons to do so are (1) lower thermal resistance to the heat sink, (2) greater compliance to combat warpage during assembly, and (3) in 3D integration, to accommodate a reasonable aspect ratio (>1:10) for TSV processing. However, the unsupported thin silicon warps considerably, after assembly. This leads to considerable built-in stress, causing reliability problems for the device structures and large residual stress on die-to substrate interconnections (micro-bumps) post assembly. Furthermore, thinned silicon is very fragile and is subjected to cracking during handling. This problem also pervades assembly on organic laminates and PCBs, which are themselves warped significantly.

4. Solder-based joints

In conventional packaging, solder balls are used to join the dies to each other and to the laminate or PCB. In the former case they are called C4 or solder-capped pillars (depending on size) and in the latter case they are called BGAs. The primary function of these joints is to provide electrical connections. There are three principal modes of failure for these connections: 1. embrittlement and voiding leading to fatigue induced failures. The failure may be caused by thermal cycling during the course of chip operation or even during various reflows that it is subjected to during processing; 2. Internal stress caused by the built-in warpage of both the dies and the laminate/PCB; and 3. Electromigration caused by the current flow, especially current crowding near the edge of the bump. The first two concerns are alleviated by not relying on the solder joints to hold the assembly together but through the use of an additional bonding filler called the underfill.

5. Underfill

The application of "Underfill" is a common practice during assembly of chip-to-substrate (using C4s) or package-to-board (using BGA) contacts. Underfill is usually applied after reflowing or localized solder TCB process. The main challenge is complete removal of the flux material under the chip after bonding process. The flux residuals are trapped inside underfill material during capillary filling and cause formation of voids due to outgassing and flux activation at elevated temperatures. Consequently, mechanical strength of the die-attachment is decreased over time as underfill ages. Another concern is the ingress of corrosives from the ambient gases over time, including moisture.

6. Passivation and moisture ingress

Considering the above, package is usually passivated with organic passivation, which typically is a silicone-based material. All organic materials are non-hermetic and, therefore, cannot completely prevent the moisture ingression. If the passivation does not stick well to the underlying surface due to the presence of an impurity (e.g. salts), an osmotic pressure is build up which causes water vapor to condense at the interface. Over time, moisture ingression can corrode the underlying metal structures and cause severe reliability problems.

7. Electomigration

Electro-migration in the soldered contacts is a known reliability problem. Electrical current densities at the edge of the bumps are very high, causing the movement of solder material over time. Consequently, the soldered contacts suffer from the formation of voids. The voiding effects become severe at elevated temperatures as electromigration is further superimposed by thermo-migration [5]. While full conversion to intermetallics reduces failure by electromigration (because the intermetallics are bound and diffuse less), the intermetallics are brittle, subject to voids and enhance other failure modes including cracking.

III. Reliablity Issues In Fan-Out Packaing

Fan-out wafer level packaging is an emerging scheme to address high-density interconnects. This technique completely avoids the use of package laminate. A detailed description of fan-out process is given in [6]. Here, we will describe few main issues with this technique.

1. Molding compound CTE mismatch and curing stress

Currently, rigid molding compounds (MCs) are used as the base material for fan-out processes. High thermo-mechanical stresses are incurred during curing process as well as in the molded-form, due to the large CTE mismatch between semiconductor chip (2-3 ppm/K) and MC (30-50 ppm/K). Various filler particles and stress relieve agents are incorporated in the MCs to improve performance of the material. Increasing ratio of filler particles to MC increases Young's modulus of the material while coefficient of thermal expansions decreases. Fracture strength of these materials decrease with increasing temperatures. The molding compounds are non-hermetic and over time they absorb water vapor and can ultimately lead to corrosion problems.

2. Die shift

Die-shift has become a very critical problem as rigid molding compound shrinks during curing process. Die-shifts are reported to be as high as up to 50-80 microns, which causes severe alignment issues during fan-out processes. A lot of emphasis is being put towards finding a suitable curing material with less shrinking properties. Misalignment can also

be reduced by using an adaptive lithographic process which accounts for them.

3. Bendability in flexible fan-out process

Fukushima *et al.* have introduced a fan-out wafer-level process, called Flextrate^{TM}, for flexible biocompatible substrates [7]. The molding compound in this case is a medically graded silicone (PDMS) material. This flexible platform is superior in terms of cure-induced thermo-mechanical stresses and exhibits minimum die-shift i.e. in the range of few microns. The main reliability concern is the integrity of fan-out metal structures. During the bending of PDMS, metal wires undergo plastic deformation causing increase of electrical resistance and a mechanical reliability problem. Furthermore, they can possibly delaminated from the PDMS. Fukushima *et al,* have introduced special stress buffer layers to minimize stresses in metal structures [7]. Corrugated structures for Cu wires have been introduced by Hanna *et al.* to improve the reliability of metal wires during bending [8].

4. Moisture ingression and salt intrusion

Flextrate^{TM}, technology is mainly targeted for biomedical applications i.e. implantable biomedical microsystems as well as wearable devices. PDMS is a non-hermetic epoxy based material. Moisture ingression and salt intrusion can be minimized but cannot be completely eliminated, which is a main reliability concern for implantable electronics. The adhesion between chips & PDMS, metal-structures & PDMS is vital for reliability. If delamination occurs, both moisture and salt scan inflict significant corrosion in metal structures, which are typically copper. For biomedical applications, saline immersion tests are used for short or long-term qualification.

IV. IV. SILICON INTERCONNECT FABRIC:

Bajwa et al [2], have developed a system-level integration scheme for mounting of various heterogeneous components on a common platform, called "Silicon Interconnect Fabric (Si-IF)". This scheme simplifies packaging hierarchy by implementing only one packaging level, where heterogeneous components (chips, passives, etc.) are mounted on Si-IF at extreme tight (2-10 microns) interconnect pitches and small inter-dielet distances (50-100 microns). This integration scheme relies on a solderless direct metal-metal bonding of components. Here, main packaging-related reliability issues will be addressed.

1. Metal-metal interconnects

Chip-to-wafer (or substrate) metal-metal (Cu or Au) direct thermal compression bonding has been chosen as the main die-attach technology to achieve high-interconnect densities and to achieve small inter-dielet distances. This technology uses similar metals at the joining interface and eliminates use of solder material, therefore; inhibits the formation of intermetallic compounds which are the main cause of joint failures during cycling thermal loading. Cu-Cu bonding is extremely challenging as Cu is prone to oxidation and forms various oxides (CuO and Cu_2O) at elevated temperatures [9]. A pre-bonding oxide cleaning process is absolutely essential for a reliable metal-metal bond. There is no long-term reliability data for these types of interconnects. Power cycling, thermal shock cycling and drop tests have to be performed to investigate the integrity of these interconnects.

2. Passivation

Si-IF integration approach relies on extreme tight pitches and small inter-dielet distance. Hence, conventional underfill materials cannot be used. The Cu-pillars in this scheme are approximately 1-2 microns higher than the Si-IF surface. The auto filling of epoxy-based material due to capillary forces is highly unlikely. For passivation, parylene-based conformal coating has been employed as it can possibly penetrate through micro-voids. Parylene, is a very good moisture barrier, but it cannot prevent salt intrusion which can lead to corrosion problems over time. Parylene is notorious for its adhesion properties to metals. Silane-based adhesion promotors can sufficiently anchor parylene to silicon oxide passivation layer, but its adherence to copper is still very poor. Thermal cycling and high-temperature storage tests are needed to be performed to evaluate long-term stability of parylene coating for Si-IF based assemblies.

V. SUMMARY

With emergence of advanced packaging technologies, the understanding of underlying reliability issues is very critical. CTE mismatch induced thermomechanical stresses, moisture ingression, salt intrusion, delamination of passivation layers, metal (Cu) oxidation, formation of intermetallic compounds, electromigration, etc. are highlighted as main reliability concerns. Conventional reliability tests such as thermal shock, thermal cycling, power cycling, high temperature storage, humidity test, drop tests, saline immersion tests and etc. can be adopted for these novel technologies.

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