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Electrodeposition of Electroluminescent CdSe Nanowire Devices

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Electrodeposition of Electroluminescent CdSe Nanowire Devices

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Physics

by

Shaopeng Qiao

Dissertation Committee:
Professor Reginald M. Penner , Chair
Professor Ilya N. Krivorotov
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2018

DEDICATION

To my parents and friends.

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8. Won-Tae Koo, Ji-Soo Jang, **Shaopeng Qiao**, Wontae Hwang, Gaurav Jha, Reginald M. Penner and Il-Doo Kim, "Hierarchical Metal-Organic Framework Assembled Membrane Filter for Efficient Removal of Particulate Matter", ACS Applied Materials and Interfaces 10 (2018) 19957.

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PRESENTATIONS and TALKs

1. Electrodeposited, Transverse Nanowire Electroluminescent Junctions, *MRS Spring Meeting,* ***Apr.2017****, Phoenix, Arizona.*

2. Electrodeposited, Transverse Nanowire Electroluminescent Junctions, *NKIS*, ***Oct. 2017***, *San Jose, California*

ABSTRACT OF THE DISSERTATION

Electrodeposition of Electroluminescent CdSe Nanowire Devices

By

Shaopeng Qiao

Doctor of Philosophy in Physics

University of California, Irvine, 2018

Professor Reginald M. Penner , Chair

Electrodeposited nano-materials have huge potential to reduce the cost of nano and micro fabrications dramatically especially in light emitting diodes field. It is difficult to fabricate high performance devices and understand the working mechanisms due to the polycrystalline nature of most electrodeposited materials. In this dissertation, electrodeposited cadmium selenide was used to fabricated two different structures of light emitting devices. In the second chapter, the preparation by electrodeposition of transverse nanowire electroluminescent junctions (*tn-ELJs*) is described and the electroluminescence (EL) properties of these devices are characterized.The resulting linear array of nickel-CdSe-gold junctions produce electroluminescence (EL) with an external quantum efficiency, EQE, and threshold voltage, V_{th}, that depends sensitively on w_{CdSe}. EQE increases with increasing electric field and also with increasing w_{CdSe}, and V_{th} also increases with w_{CdSe}, and therefore the electrical resistance, of the *tn-ELJs*. V_{th} down to 1.8($\pm$0.2)V (for w_{CdSe} $\approx$100 nm) and η_{EL} of 5.5($\pm$0.5) $\times$ 10^{-5} (for w_{CdSe} $\approx$450 nm) are obtained. *tn-ELJs* produce a broad EL emission envelope, spanning the wavelength range from 600 - 960 nm. In the third chapter, A wet chemical process involving two electrodeposition steps followed by a solution casting step, the $EESC$ process, is described for the fabrication of electroluminescent, radial junction wires. $EESC$ is demonstrated by assembling three well-studied nanocrystalline (or amorphous) materials: Au,CdSe, and PEDOT:PSS. The tri-layered device architecture produced by $EESC$

minimizes the influence of an electrically resistive CdSe emitter layer by using a highly conductive gold nanowire that serves both as a current collector and a negative electrode. Hole injection, at a high barrier CdSe-PEDOT:PSS interface ($\phi_h \approx 1.1$ V), is facilitated by a contact area that is 1.9 - 4.7 fold larger than the complimentary gold-CdSe electron-injecting contact ($\phi_e \approx 0.6$ V) contributing to low voltage thresholds (1.4 - 1.7 V) for EL emission. Au@CdSe@PEDOT:PSS wire EL emitters are 25 μm in length, but the *EESC* process is scalable to nanowires of any length, limited only by the length of the central gold nanowire that serves as a template for the fabrication process. Radial carrier transport within these multishell wires conforms to the back-to-back diode model.

Chapter 1

Introduction

1.1 Electroluminescence from Electrodeposited Semiconductor Nanostructures

Methods for patterning nanometer-scale electroluminescent (EL) structures on surfaces will be required for a variety of anticipated device applications ranging from chemical sensors, to information transfer and processing, and interfaces to biological systems.[104, 57, 105] Single semiconductor nanostructures were first electrically stimulated to emit light in 2001 when Lieber and coworkers reported light emission at the forward-biased junctions between crossed n-doped and p-doped InP nanowire junctions.[27] Many creative device architectures for nanostructure EL devices have subsequently been demonstrated based upon single nanowires,[6, 116, 117, 24, 33] nanowire arrays interfaced to films,[107, 34, 12] crossed nanowire p-n junctions,[38, 42, 115] and core-shell hetrostructures,[77, 94, 37, 54, 8] In the

specific case of devices based upon cadmium selenide (CdSe) - the semiconductor of interest here - external quantum efficiencies (EQEs) are generally in the 10^{-7} to 10^{-5} range (Table 1.1).

Work on *films* of thousands or millions of semiconductor nanocrystals preceded experiments on single nanostructures. These films are macroscopic in two dimensions, and nanoscopic in the third, or thickness dimension. Bulovic and coworkers first demonstrated that layers of CdSe nanocrystals could produce EL in 1992.[17] Although EQE for these devices were initially as low as those seen for emissive devices based upon single semiconductor nanostructures,[19, 18] it was soon discovered that the insertion of hole-transporting layers (e.g. PEDOT) and electron-injecting layers (e.g. ZnO) sandwiching the emitting layer elevated the EQE to 1% or higher,[51, 114, 41, 71, 106] (for recent reviews, see: [84, 90]). Multi-layer, multi-junction wires that are optimized for efficient EL can be obtained using epitaxial growth processes, starting with vapor-liquid-solid (VLS) growth of III-V vertical nanowire forests.[80, 23, 94, 77, 48, 39, 43, 9, 40] These processes yield very low defect materials, with excellent control of layer thicknesses, composition and lattice match, resulting in efficient, bright EL light emitters. But these exquisite architectures are obtained at the high cost of the required vacuum and thermal processing and the requirement for significant and nontrivial post-synthesis processing to position wire emitters within circuits, attach electrical contacts, etc. A second issue is the fact that long wires, beyond 5 μm in length, are not generally accessible using this approach.[80, 23, 94, 77, 48, 39, 43, 9, 40]

At the other end of the spectrum are solution processing methods that facilitate the high-throughput assembly of materials that can be nanocrystalline or even amorphous into devices consisting of layers that are stacked along the direction of charge transport. A layer of semiconductor nanocrystals is usually the EL emissive element in these devices.[109, 50, 97, 111, 1, 20, 56, 44, 65] Again, a diversity of efficient and bright EL light emitting systems have been demonstrated for a range of semiconductor emitters. The catch is that solution processing

Table 1.1: Performance of CdSe Nanostructure-Based Electroluminescent Junctions.

Junction Description[a]	Electrode Spacing (nm)	V_{th}[b] (V)	Spectral Range (nm)	EQE_{max}[c]	Ref
nc films					
CdSe QD	1000	4	480-650	1-10$\times10^{-5}$	[18]
CdSe QD-PVK	70-120	5-7	615-650	5$\times10^{-6}$	[19]
CdSe QD-TPD	40	3	540-590	5.2$\times10^{-3}$	[17]
CdSe-CdS core-shell QD	- -	4	600-630	4-8$\times10^{-3}$	[114]
CdSe-CdS core-shell QD	- -	1.5	600-635	0.12-0.18	[55]
CdSe QD TPD	- -	15.5	400-750	1.4$\times10^{-6}$	[82]
CdSe-CdS nanoplates	122-144	2.25	530-600	0.05	[110]
CdSe-CdS dot-in-rod QD	175	3	600-700	0.061	[11]
CdSe-CdZnS QDs core-shell QD	150	1.7	580-670	0.182	[113]
CdSe-CdZnS QDs core-shell QD	130-135	2.5	470-550	0.06	[52]
single nanostructures					
CdSe NR	30	1.7($\pm$0.1)	650-820	10^{-5}	[33]
CdSe NW	2000-6000	4	620-850	(1-5)$\times10^{-6}$	[24]
***nc*-CdSe in a nanogap**	200	1.5($\pm$0.2)	650-890	1.8($\pm$0.7)$\times10^{-6}$	[100]
***nc*-CdSe NW arrays**	600	6.2($\pm$0.5)	610-890	4($\pm$1)$\times10^{-6}$	[3]
CdSe *tn-ELJ*	448	6.9($\pm$0.3)	560-960+	4.9($\pm$0.2)$\times10^{-5}$	[78]
***EESC* Au@CdSe@PEDOT:PSS**	302	1.44($\pm$0.02)	650-800	3.8($\pm$0.6)$\times10^{-4}$	**this work**
	595	1.50($\pm$0.00)	650-800	9($\pm$2)$\times10^{-5}$	“
	788	1.53($\pm$0.03)	650-800	1.9($\pm$0.6)$\times10^{-4}$	“
	953	1.60($\pm$0.04)	650-800	1.5($\pm$0.6)$\times10^{-4}$	“
	1164	1.70($\pm$0.04)	650-800	7.1($\pm$0.2)$\times10^{-5}$	“

[a]Abbreviations: NR = nanorod, NW = nanowire, *nc* = nanocrystals or nanocrystalline, PVK = poly(vinylcarbazole), TPD = N,N' - diphenyl-N,N' - bis(3-methylphenyl) - (1,1'-biphenyl) - 4,4'-diamine. [b]$V_{th} = E_{app}$ at the EL emission threshold. [c]EQE_{max} = The maximum EQE.

methods have been limited to the preparation of two-dimensional films with millimeter-scale, or larger, lateral dimensions.[109, 50, 97, 111, 1, 20, 56, 44, 65] Adapting these methods to nonplanar geometries such as cylinders or wires is not easily accomplished and radial junction EL-emitting devices, analogous to those obtained by epitaxial deposition, have not be achieved using solution processing to our knowledge.

Here, we describe two different electroluminescent metal-semiconductor-metal (M-S-M) nanostructures fabricated using solution processing methods. The first type of device is structured by locating nickel and gold contact on the opposite sides of *nc*-CdSe nanowires along the transverse direction. Light is emitted from the CdSe nanowire to air directly. The second type of device is structured by stacking each layer coaxially and the gold nanowire works as the core and CdSe, PEDOT:PSS works as the shell subsequently. Light is emitted from the CdSe nanowire and then travel through the transparent PEDOT:PSS layer into air.

1.2 Carrier Generation and Transport in M-S-M Structures

Electroluminescence is generated through the radiative recombination of free electrons and holes either within the material or at the interface between the material and the contact. So the density and distribution of these free electrons and holes would be the key factors for electroluminescence.

For a M-S-M structure, there are three important parts : a) the first metal-semiconductor (M-S) contact; b) the bulk part of the semiconductor material; c) the second M-S contact. These two M-S contacts would form two Schottky barriers on two sides. Upon a potential applied on the two metal contacts, electrons and holes will start to flow within the structure due to the electric force. The band energy diagram for a n-type M-S-M structure is showed

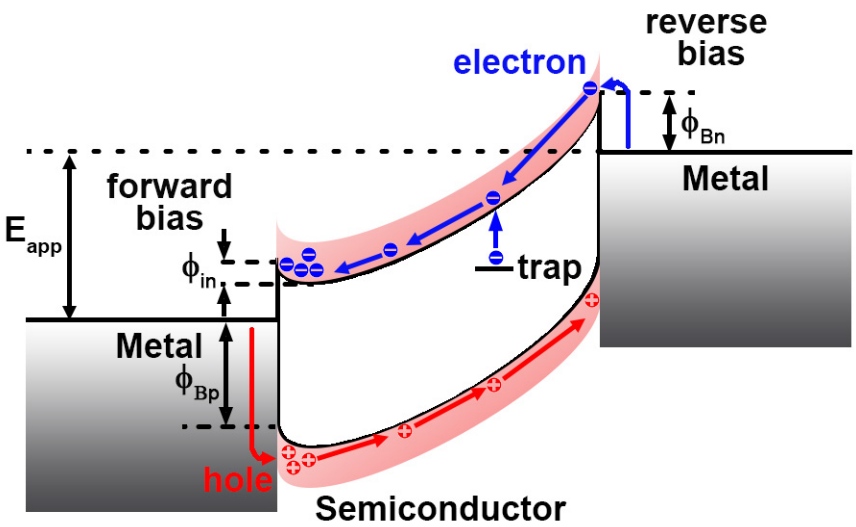

Figure 1.1: Band energy diagram for a M-S-M structure under an applied potential. E_{app} is the applied potential, Φ_{Bn} is the Schottky barrier height for electrons, Φ_{Bp} is the Schottky barrier height for holes, Φ_{in} is barrier height caused by the build in potential for electrons which is equal to $V_{bi} - V_1$ where V_{bi} is the build in potential and V_1 is the potential distributed on this M-S interface

in Figure 1.1. [92, 91, 15] (We are only interested in n-type semiconductor here since the material CdSe we study is a n-type semiconductor.)

Schottky Emission. For these two M-S contacts, free electrons are injected from the right contact which forms a reverse biased Schottky barrier with the middle semiconductor and holes are injected from left contact which forms a forward biased Schottky barrier with the middle semiconductor. As Figure 1.1 shows, there are two barriers for electron flow at these two contacts: ϕ_{Bn} and ϕ_{in}. ϕ_{in} is much smaller than ϕ_{Bn} and would become 0 when E_{app} is big enough. So the limiting factor for electron flow is ϕ_{Bn} at the right Schottky barrier. For a n-type semiconductor, the carrier concentration of holes is much lower than the carrier concentration of electrons, so the contribution of holes to the current can be ignored. However, hole injection still plays an very important role here. When holes are injected from the left contact into the middle semiconductor, hole concentration would increase. This

increase could amplify the probability of radiative recombination of free electrons and holes within a n-type semiconductor where hole concentration is very small compared to electron concentration. In summary, the limiting factor for total current or carrier injection at the two M-S contacts is the barrier height at the reverse biased Schottky barrier.

For a Schottky barrier, current transport is explained by thermionic emission theory, which can be expressed as[70, 68, 92]

$$J = J_0 \left[exp\left(\frac{qV}{kT}\right) - 1 \right] \tag{1.1}$$

and

$$J_0 = A^{**}T^2 exp\left(-\frac{\phi_b}{kT}\right) \tag{1.2}$$

where J_0 is saturation current density, q is the unit electronic charge, k is the Boltzmann constant, T is the absolute temperature, A^{**} is the effective Richardson constant, and phi_b is the Schottky barrier height in eV. With real experimental data, I-V curves usually deviate from this ideal situation due to the interface states or the image forces. Ideality factor n was introduced to compensate this difference with n = 1 corresponding to the ideal thermionic emission. And a bigger n value usually means the electric contact at the interface is not so ideal and could have a lot of defects. With n, the expression becomes

$$J = J_0 \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \tag{1.3}$$

If we consider two sides of an identical M-S-M structure: one is reverse bias (diode 1) and one is forward bias (diode 2), we have

$$J = J_{01}\left[1 - exp\left(-\frac{qV_1}{nkT}\right)\right] \tag{1.4}$$

$$J = J_{02}\left[exp\left(\frac{qV_2}{nkT}\right) - 1\right] \tag{1.5}$$

voltage drops on two contacts would be

$$V_1 = -\frac{nkt}{q}ln\left(1 - \frac{J}{J_{01}}\right) \tag{1.6}$$

$$V_2 = \frac{nkt}{q}ln\left(1 + \frac{J}{J_{02}}\right) \tag{1.7}$$

Assume there is no voltage drop across the middle materials part, then we $V = V_1 + V_2$ and solve for J

$$J = \frac{2J_{01}J_{02}sinh(\frac{qV}{2nkT})}{J_{01}exp(-\frac{qV}{2nkT}) + J_2exp(\frac{qV}{2nkT})} \tag{1.8}$$

For an asymmetric M-S-M structure, n_1 and n_2 might be different but there is no analytical

solution for J anymore. Sinha *et al.*[88, 87] introduced an approximated equation for J

$$J = \frac{J_{01} J_{02} sinh(\frac{qV}{2kT})}{J_{01} exp(-\frac{qV}{2n_1 kT}) + J_2 exp(\frac{qV}{2n_2 kT})} \tag{1.9}$$

Poole Frenkel Emission. For the bulk part, free electrons could be generated from traps. Since the energy level of traps is lower than the conduction band, extra energy would need to be provided for electrons to jump from this barrier. Similar as Schottky emission, this process can be realized through thermal activation. Under electric field, the barrier height could be lowered and this thermal activation process could be enhanced. This is called Poole-Frenkel (P-F) emission, and it can be expressed as [85, 15]

$$J = J_0 \; exp\left(\frac{\beta_{pf} \mathcal{E}^{1/2}}{kT}\right) \tag{1.10}$$

and

$$J_0 = q\mu N_C \mathcal{E} exp\left(\frac{-\phi_T}{kT}\right) \tag{1.11}$$

where β_{pf} is the P-F field-lowering coefficient, $\mathcal{E}$ is the magnitude of the electric field (E_{app}/d), μ is the electronic drift mobility, N_C is the density of states in conduction band, ϕ_T is the trap energy level in eV.[86, 91] P-F emission could increase the carrier concentration within the material, and thus enhance the electron and hole recombination. Although the majority of the recombination would be non-radiatively, but the total radiatively recombination could

be increased overall. P-F emission usually occurs at relatively high electric field.

Besides electron emission, electron transport also happens within the bulk part and there could be several different situations.

Hopping Conduction. With outside potential or electric field, electrons could hop from one trap site to another trap site due to the tunneling effect. It depends on the trap depth or the distance between the trap states and the bottom of conduction band, the distance between two traps, and also the field strength. This hopping process can be expressed as[62, 15]

$$J = qan\nu exp\left(\frac{qa\mathcal{E} - \phi_T}{kt}\right) \tag{1.12}$$

where a is the mean hopping distance, n is the electron concentration in the conduction band of the material, ν is the frequency of thermal vibration of electrons at trap sites, and ϕ_T is the trap energy level in eV. Unlike P-F emission which is a thermionic process, hopping conduction is a tunneling process. This means this process could only happen when the average distance between the trap states is relatively small.

Space Charge Limited Conduction. When free electrons are injected into intrinsic and low doped semiconductor, the electron flow could be affected a lot by space charges which make the electric field ununiform in the material. Space charge limited conduction (SCLC) is characterized by Child's law[13] or Mott-Gurney's law[63] which has the following expression

$$J = \frac{9\epsilon_s \mu V^2}{8d^3} \tag{1.13}$$

where μ is the carrier mobility, ϵ_s is the dielectric constant, and d is the distance between two electrodes. While keep increasing the voltage applied, all the traps will be filled at a "threshold" voltage and the current would increase dramatically. A good approximated equation was found by Murgatroyd to express this situation[7]

$$J = \frac{9\epsilon_s \mu V^2}{8d^3} exp\left[\frac{0.891}{kT}\left(\frac{e^3 V}{\pi \epsilon_s d}\right)\right] \tag{1.14}$$

Since there is this steep increasing in the current at higher electric field, this process might get mixed with P-F emission due to similar mathematical relationship. In summary, $I - V$ curve for a M-S-M structure with SCLC usually has three regions: 1) Ohmic like conduction region where $I - V$ curve is linear or $I \propto V$; 2) Child's law region which has $I \propto V^2$; 3) traps-filled-limit (TFL) region which has a enormously steep current rise. With $lnI - lnV$ curve, the slope would correspond to 1, 2, > 2 regions. [32, 47, 79, 66, 15]

Grain-Boundary-Limited Conduction. For a polycrystalline material, there are a lot of grain boundaries. When electrons flow to a grain boundary, it would experience a much higher resistivity than that in the grain. In terms of energy, the grain boundary function like an energy barrier and it would limit the electron flow. [76, 89] Under extra electric field, the barrier height could also be lowered like Poole Frenkel emission. So experimentally this process might not be able to be indentified out separately.

In summary, carrier injection and transportation in a n-type M-S-M structure is dominated by the electron injection and transportantion. This process could be limited by the contact and Schottky emission would be the main contributing mechanism. It could also be limited by the bulk part where multiple mechanisms including P-F emission, SCLC, etc. could be responsible depending on the material properties and also applied voltage. It would be

important to understand the working mechanism for the system studied since it would be related to the electron and hole recombination directly. Through the shape of $I - V$ curve, we could tell the limiting factors for the system studied and might also see the transitions between each mechanism.

Chapter 2

Electrodeposited, Transverse Nanowire Electroluminescent Junctions

2.1 Introduction

In this chapter, we describe a discovery platform that provides a means for electrodepositing and characterizing the *EL* properties of linear arrays of many nearly identical metal-semiconductor-metal (M-S-M) junctions. We use this platform to characterize arrays of nickel-(*nc*-CdSe)-gold M-S-M junctions. These junctions are prepared by first electrodepositing an ensemble of 60 nearly identical *nc*-CdSe nanowires, and then locating nickel and

gold contacts on opposite sides of each nanowire along their axes also using electrodeposition. These devices are termed "transverse nanowire electroluminescent junctions" or *tn-ELJs*.

2.2 Process Flow

tn-ELJs are prepared using a process (Figure 2.1) that provides for precise control of the width (± 5 nm) of the CdSe nanowire - which coincides with the electrical axis of the device - and the height (± 2 nm) the CdSe nanowire - which corresponds to the optical axis of the device. A second attribute of *tn-ELJs* is that the two metal-semiconductor junctions are both prepared by electrodeposition, thereby insuring electrically intimate contact between nickel and CdSe (Figure 2.1, step 2), and subsequently, CdSe and gold (Figure 2.1, step 3). Finally, in contrast to stacks of 2D films where the electrical and optical axes are coincident, the optical axis of the *tn-ELJ* is orthogonal to the electrical axis, allowing independent optimization of these dimensions for these two functions. The precision of *tn-ELJ* fabrication exposes the dominant influence of the *nc*-CdSe nanowire width, w_{CdSe}, on the two major metrics characterizing EL performance - the threshold for light emission, V_{th}, and the EQE.

2.3 Results and Discussion

2.3.1 Electrodeposition

tn-ELJs were prepared using a version of the lithographically patterned nanowire electrodeposition (LPNE) process (Figure 2.1) that we have previously described.[99, 58] The lithographically patterned nickel electrode that is employed for CdSe electrodeposition serves as one electrical contact to a CdSe nanowire, and the second gold electrode is electroplated at

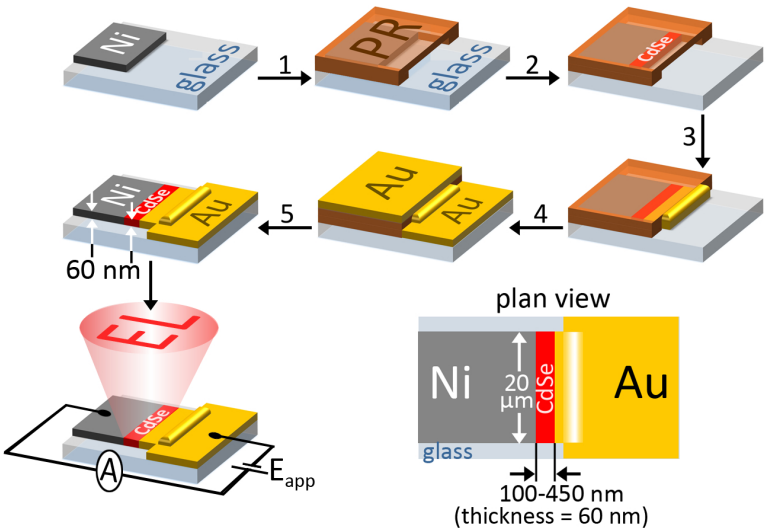

Figure 2.1: Simplified process flow for the fabrication of a single transverse nanowire electroluminescent junction (*tn-ELJ* - for a complete process flow, see Figure S1). In Step 1, an evaporated nickel film on glass is patterned using photolithography. After spincoat of a photoresist (PR) layer and some additional processing, a horizontal trench is produced adjacent to the edge of the nickel film. This trench has dimensions of 60 nm (height), 20 μm (length) and 300 nm $\sim$ 1μm (depth). In Step 2, this patterned nickel edge is immersed in a plating solution and CdSe nanowires are electrodeposited within the trench using the nickel edges as working electrodes. The width of the CdSe nanowires is controlled by the electrodeposition conditions, which are identical for every nanowire. A gold electrical contact is then electrodeposited onto each CdSe nanowire. After the trench is filled with gold, the excess gold emerges from the trench forming a bump, as depicted in Step 3. In Step 4, a gold film is evaporated onto the entire surface of the device and then, in Step 5, the gold-coated photoresist layer is removed by lift-off. *tn-ELJ* devices produce *EL* light emission upon the application of a voltage bias to the nickel and gold contacts.

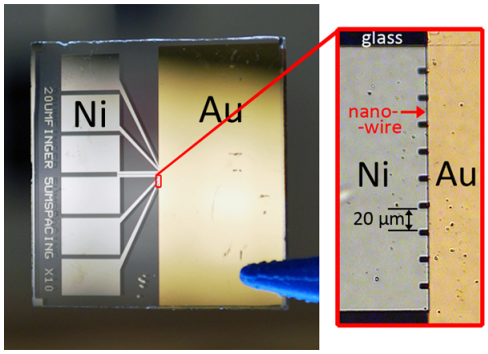

Figure 2.2: *tn-ELJ* device pictures. a) Photograph of 6 individual Ni-CdSe-Au *tn-ELJ* array devices on glass. The CdSe nanowires are vertically oriented along the left edge of the gold film. b) Photomicrograph of one of the six devices. Each device has ten individual nickel contacts to CdSe nanowires, and each is 20 μm in width.

the CdSe surface (Figure 2.1). This process, carried out in parallel, provides a means for preparing a total of sixty pairs of nickel-gold electrodes in groups of ten, coupled with sixty nearly identical CdSe nanowires (Figure 2.2).

Uniformity of the CdSe nanowire width is achieved by electrodepositing the CdSe nanowire according to the reaction: $Cd^{2+} + H_2SeO_3 + 4H^+ + 6e^- \rightarrow CdSe(s) + 3H_2O$ under conditions of activation control. Here, this was accomplished using potentiostatic deposition at -0.60 V vs. SCE (Figure 2.3a). Electrodeposition current *versus* time transients (Figure 2.3b) show increasing current indicative of an increase in the wetted surface area of the nascent nanowire during electrodeposition. This increase in wetted surface area is likely the result of the deposition of a porous CdSe deposit, since voids are visible in some of the SEM images presented below (Figure 2.4).

In each *tn-ELJ*, the lithographically patterned nickel electrode used to grow the CdSe nanowires serves as one electrical contact. The second contact, composed of gold, is prepared by electrodeposition directly onto the edge of the freshly-deposited CdSe nanowire. Again, this process is accomplished by the slow, activation-controlled deposition of gold (potentiostatic deposition at -0.90 V vs. SCE (Figure 2.3c)). A quasi-constant deposition current is

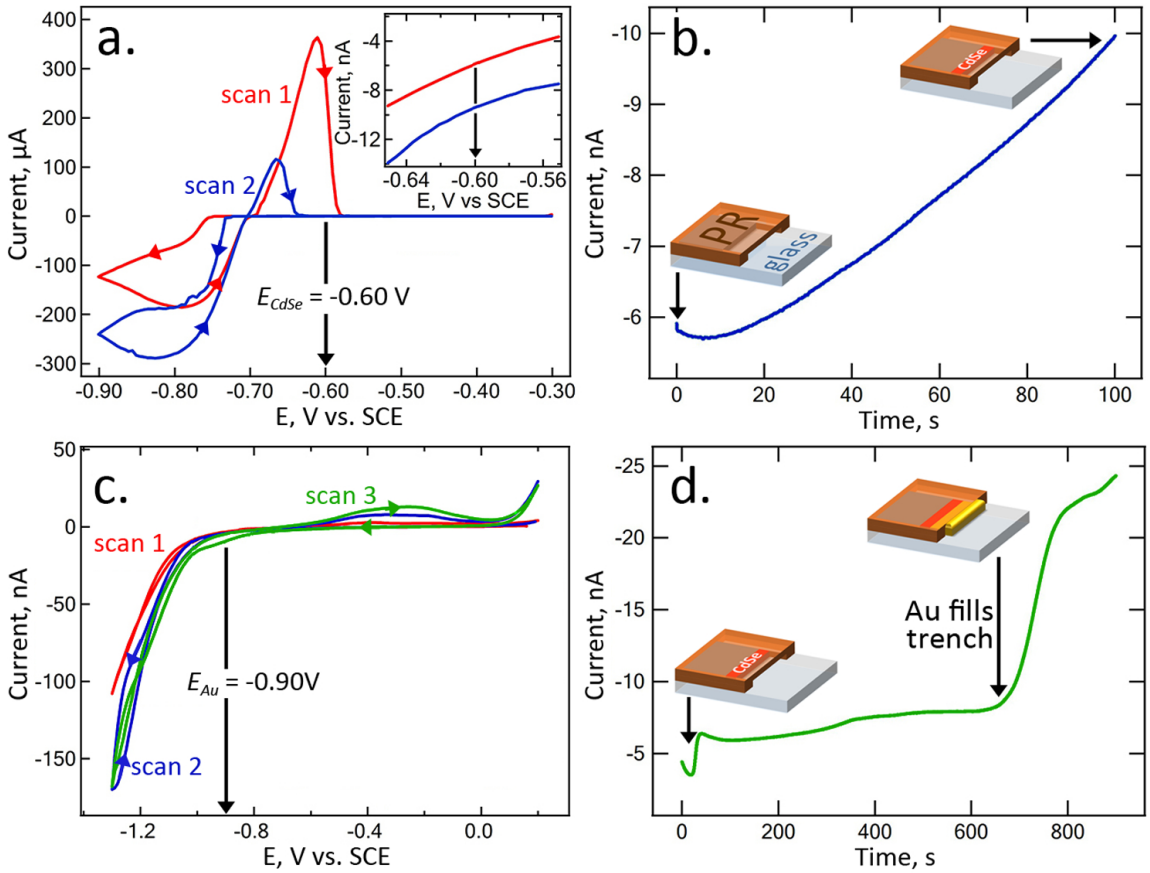

Figure 2.3: Electrodeposition of CdSe nanowires (a,b) and a gold contact (c,d). a) Cyclic voltammetry (50 mV/s) in the plating solution used for CdSe electrodeposition, containing 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1-2. b) Current *versus* time transient for the potentiostatic growth at -0.60V of CdSe nanowires. CdSe nanowires with widths, w_{CdSe}, ranging from 102 nm to 448 nm were prepared by increasing the electrodeposition time from 20s to 100s. c) Cyclic voltammogram (50 mV/s) for a commercial gold plating solution acquired using the edges of CdSe nanowires. d) Current *versus* time transient for the potentiostatic growth at -0.90V of gold contacts at the CdSe nanowires. A rapid increase in current, starting at 650s, signals the filling of the photoresist trench.

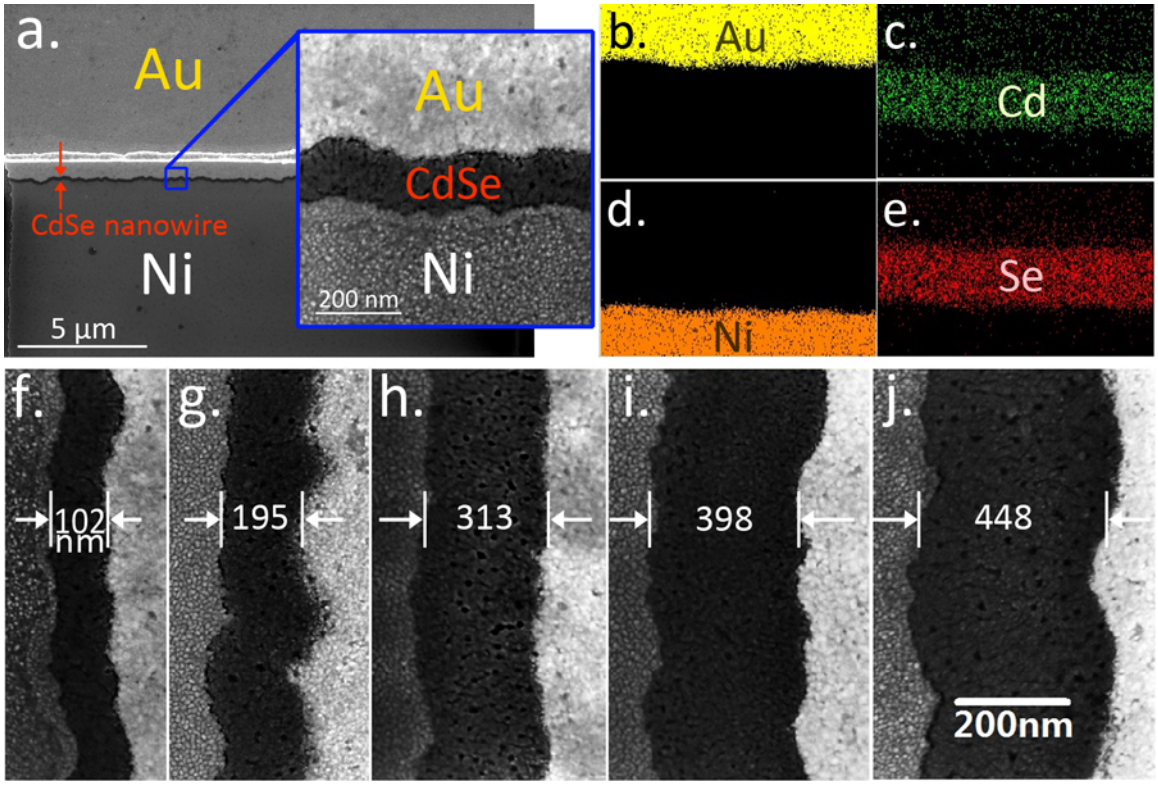

Figure 2.4: Scanning electron micrographs of *tn-ELJ* Ni-CdSe-Au junctions, all 60 nm in thickness. a) Low magnification image showing the horizontal CdSe nanowire, with top gold and bottom nickel electrodes. INSET: Higher magnification SEM image of the indicated region. b-e) EDX elemental maps of the junction region shown in the inset of (a) showing regions of Au (b), Cd (c), Ni (d), and Se (e). f-j) SEM images of five Ni-CdSe-Au *tn-ELJ* having w_{CdSe} varying from 102 nm (f) to 448 nm (j).

observed during this process (Figure 2.3d) until the trench fills with gold (Figure 2.3d, 650s). At longer times, a rapid increase in the gold deposition current is observed resulting in the formation of a linear gold bump at the mouth of the trench, parallel to the CdSe nanowire (Figure 2.4a.) *tn-ELJ* device fabrication is completed by vapor depositing additional gold to facilitate the attachment of electrical leads.

Table 2.1: Fitting Parameters For Calculations of I-V Curves According to the Back-to-Back Schottky Barrier Model (Eq. 2.1)

w_{CdSe} (nm)	A^{**a} (A cm^{-2} K^{-1})	$\phi_{B1}{}^{b}$ (eV)	$\phi_{B2}{}^{c}$ (eV)	$n_1{}^{d}$	$n_2{}^{e}$
102	15.6	0.52	0.57	1.295	1.196
195	15.6	0.52	0.55	1.185	1.127
313	15.6	0.55	0.56	1.125	1.130
399	15.6	0.58	0.59	1.147	1.086
448	15.6	0.62	0.64	1.239	1.209

[a] A^{**} = effective Richardson constant.[75]
[b] ϕ_{B1} = Schottky barrier height for Ni-CdSe contact.
[c] ϕ_{B2} = Schottky barrier height for Au-CdSe contact.
[d] n_1 = ideality factor for Ni-CdSe contact
[e] n_2 = ideality factor for Au-CdSe contact

2.3.2 SEM Characterization

SEM images of *tn-ELJ* Ni-CdSe-Au junctions (Figure 2.4) show that the width of the CdSe nanowire is conformal with respect to the nickel electrode (Figure 2.4a and inset) and directly proportional to the electrodeposition time. EDX elemental analysis (Figure 2.4c,e) shows the CdSe layer to be stoichiometric (Cd:Se=1.02±0.01) within the precision of this measurement. Five *tn-ELJ* with different w_{CdSe} values, shown in Figure 2.4f-j, were investigated in this study. In recent prior work,[4, 100, 3, 46, 45] the properties of the *nc*-CdSe produced by an identical procedure have also been characterized by x-ray diffraction, Raman spectroscopy, and transmission electron microscopy. Electrodeposited *nc*-CdSe is crystalline, possesses a cubic crystal structure, and has a mean grain diameter of ≈5 nm.[4, 100, 3, 46, 45]

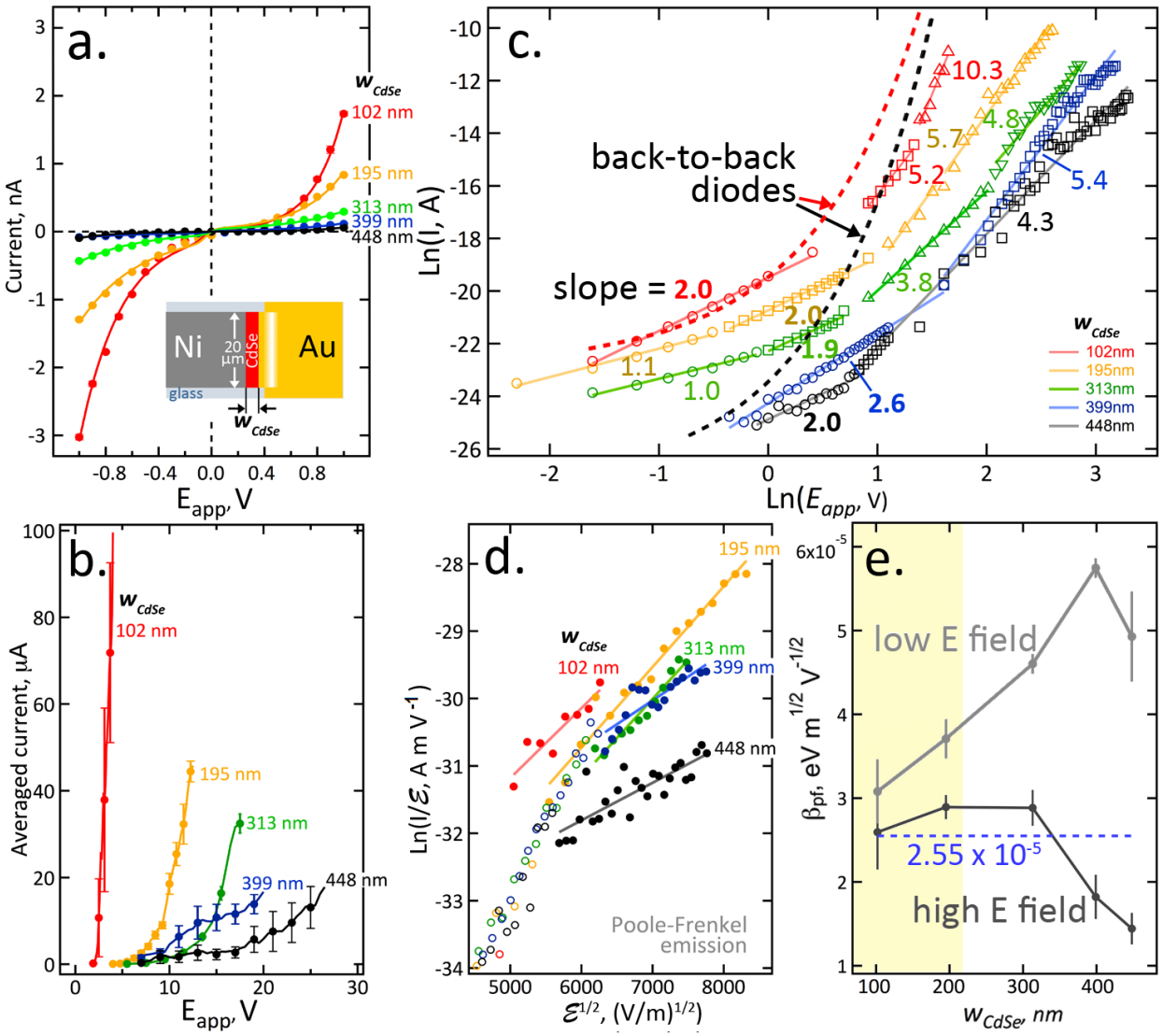

Figure 2.5: Electrical characterization of Ni-CdSe-Au *tn-ELJs*. a,b) Current *versus* voltage plots showing: a) low voltage ($E_{app} < 1.0$ V) and, b) high voltage region ($E_{app} > 1$ V in positive polarity only. c) Plot of Ln(I) *versus* Ln(E_{app}) showing the slopes of linear regions of the $I - V$ data. The dashed red line and dashed black lines are the predictions of Eq. 2.1 for back-to-back Schottky barriers, using the parameters of Table 2.1 for $w_{CdSe} = 102$ nm and 448 nm, respectively. d) Plot of Ln(I/$\mathcal{E}$) *versus* $\mathcal{E}^{1/2}$ highlighting linear regions, consistent with possible Poole-Frenkel emission at high $\mathcal{E}$. e) Plot of Poole-Frenkel field lowering coefficient, β_{pf}, as a function of w_{CdSe} for both high $\mathcal{E}$ (>3 × 10^7 V/m) and low $\mathcal{E}$ regions.

2.3.3 Current Transport

Transport in metal-semiconductor-metal (M-S-M) junctions where both junctions are Schottky barriers was studied by Sze *et al.* in 1971[92] and subsequently by others.[70, 68, 14] With the application of a potential, E_{app}, the M-S-M has one forward biased Schottky barrier (with (+) polarity) and one reverse biased Schottky barrier ((−) polarity) and transport, predominantly by majority electrons, is controlled by the reverse-biased junction. Current *versus* E_{app} (or *I-V*) curves are characterized by exponentially increasing current and, for identical metal contacts, are symmetrical about $E_{app} = 0$, conforming to the equation:[88, 14, 87]

$$J(V) = \frac{J_1 J_2 sinh(\frac{qV}{2kT})}{J_1 exp(\frac{qV}{2n_1 kT}) + J_2 exp(-\frac{qV}{2n_2 kT})} \tag{2.1}$$

Where J_1, for example, is given by:[91]

$$J_1 = A^{**} T^2 exp(-\frac{\phi_{B1}}{kT}) \tag{2.2}$$

and the equation for J_2 is analogous. Here A^{**} is the effective Richardson constant. For CdSe, $A^{**} = 15.6$ A cm^{-2} K^{-1}).[75] ϕ_{B1} and ϕ_{B2} are the Schottky barrier heights of the Au-CdSe and Ni-CdSe contacts, respectively, and n_1 and n_2 are the two ideality factors for these junctions. Eq. 2.1 does an excellent job of fitting our experimental *I-V* curves for all five *tn-ELJs* and w_{CdSe} values (Figure 5a). The fitting parameters required to produce these curves (Table 2.1) are also physically reasonable, involving the known Richardson constant and barrier heights in the range from 0.52 - 0.64 eV - close to those reported for macroscopic CdSe-Au Schottky barriers.[95] We conclude that for $|E_{app}| < 1.0$ V, *I-V* curves for *tn-ELJs*

are well described by the back-to-back Schottky barrier model.[70, 68, 14]

For $|E_{app}| > 1.0$ V, however, the currents predicted by Eq. 2.1 are significantly higher than those observed experimentally for *tn-ELJs*. For example, using the parameters of Table 2.1, dashed lines in Figure 2.5c show the predicted *I-V* behavior for the 102 nm (red dashed line) and the 448 nm (black dashed line) *tn-ELJ*s. A comparison of the dashed curves with the experimental data points of the same color shows that the disparity between them increases with increasing E_{app}. This disparity is explained by the presence of a highly resistive CdSe layer in the *tn-ELJs*, sandwiched between the two Schottky barriers. Based upon the analysis of these currents described below, we conclude that transport through a *tn-ELJ* is not limited by transport at one or both of the Schottky barriers, but by processes occurring in the bulk of the CdSe, even though this "bulk" is nanoscopic in both length (≈100-450 nm) and thickness (60 nm).

Information on the transport mechanisms operating within the CdSe can be obtained by analyzing the E_{app} dependance of the current. Space charge limited conduction (SCLC) has previously been proposed to model the *I-V* behavior of Au-CdSe-Au junctions.[69] SCLC conforms to the Mott-Gurney Eq.:[63]

$$J = \frac{9\epsilon_s \mu (E_{app})^2}{8d^3} \tag{2.3}$$

where J is the current density (A/m^2), μ is the carrier mobility (m^2/(V·s)), $\epsilon_s = = 7.82$ x 10^{-11} F/m for CdSe, and $d = w_{CdSe}$[63] Eq. 2.3 predicts that Ln(I) *versus* Ln(E_{app}) will have a slope of 2.0, and this behavior is observed for four of the five of the CdSe thicknesses (Figure 2.5c); $w_{CdSe} = 399$ nm instead shows a slope of 2.6. In this potential regime, SCLC is likely the dominant mechanism of charge transport. At lower E_{app}, a slope of 1.0, indicative

of ohmic conduction, is seen for several w_{CdSe} (w_{CdSe} = 195 and 313 nm) . Slopes larger than 2.0 are observed for all devices at $E_{app} > 10$ V. As previously described,[66, 7, 83] slopes exceeding 2.0 signal that the SCLC current is augmented by other transport mechanisms such as P-F emission or Schottky emission.

P-F emission conforms to Eq. 2.4 while, as already indicated, Schottky emission is modeled by Eq. 2.1:[85, 86, 91]

$$J = J_0 \, exp\left(\frac{\beta_{pf}\mathcal{E}^{1/2}}{kT}\right) \tag{2.4}$$

where β_{pf} is the P-F field-lowering coefficient and $\mathcal{E}$ is the magnitude of the electric field (E_{app}/d).[86, 91] These two mechanisms both predict linear $Ln(I/\mathcal{E})$ *versus* $\mathcal{E}^{1/2}$, which we observe at high values of $\mathcal{E} > 3 \times 10^7$ V/m for all five devices (Figure 2.5d).

From the slope of these plots, an experimental value of β_{PF} can be calculated and compared with the theoretically expected value for CdSe of 2.55×10^{-5} $eVm^{-1/2}$ $V^{1/2}$, indicated by the horizontal blue dashed line in Figure 2.5d. In the high $\mathcal{E}$ region $> 3 \times 10^7$ V/m, we measure β_{pf} values in the range from 1.5 - 2.9 $\times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$ - close to that expected for Poole-Frenkel emission in CdSe (Figure 2.5e). The best agreement is seen for the thinnest *tn-ELJs* (w_{CdSe} = 102 and 195 nm) where β_{pf} values are in the range from 2.6-2.9 $\times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$. Much larger values of β_{pf} are seen in the low $\mathcal{E}$ region $< 2 \times 10^7$ V/m where we believe that SCLC, not Poole-Frenkel or Schottky emission, is the dominant mechanism of charge transport. We interpret a high level of agreement of the experimental β_{pf} value with the theoretical value to suggest the likely prevalence of P-F emission, as opposed to Schottky emission, in *tn-ELJs* at high $\mathcal{E}$.

To summarize these observations, our analysis of *tn-ELJs* reveals the operation of up to three

Table 2.2: Discrete Slopes of Ln(I) *versus* Ln(E_{app}) Plots Observed at Progressively Higher E_{app}

w_{CdSe} (nm)	Slope 1	Slope 2	Slope 3	Slope 4
102	–	2.03 (±0.05)	5.2 (±0.2)	10 (±1)
195	1.1 (±0.1)	2.00(±0.05)	5.7 (±0.1)	–
313	1.03 (±0.06)	1.9 (±0.1)	3.77 (±0.07)	4.8 (±0.2)
399	–	2.63 (±0.05)	5.5 (±0.1)	–
448	–	2.0 (±0.2)	4.33 (±0.07)	–

discrete charge transport mechanisms in parallel - ohmic conduction, SCLC, and (likely) P-F emission - with increasing importance of SCLC and P-F emission as E_{app} increases. The values of these discrete slopes (see in the plot of Figure 2.5c), which delineate voltage intervals in which particular mechanisms are operating, are tabulated in Table 2.2.

2.3.4 Electroluminescence Intensity and External Quantum Efficiency

EL emission from ten-element arrays of Ni-CdSe-Au *tn-ELJs* (Figure 2.6) was imaged as a function of E_{app} using an inverted optical microscope (Figure 2.9). For the w_{CdSe} = 102 nm device, all ten channels produce EL at E_{app} = 3-4 V, but EL emission intensity increases with E_{app} and is non-uniformly distributed within each channel and between different channels (Figure 2.6) - a characteristic feature of EL in these systems that we discuss below. The properties this EL emission depended sensitively on the width of the CdSe emitter layer, w_{CdSe} (for a constant 60 nm height of this emitter layer, Figure 2.7a). For example, the voltage threshold for EL emission, V_{th}, increases from 2 V to 7 V in direct proportion to w_{CdSe} (Figure 2.7a,b). This trend is also evident in prior work involving CdSe EL emitting

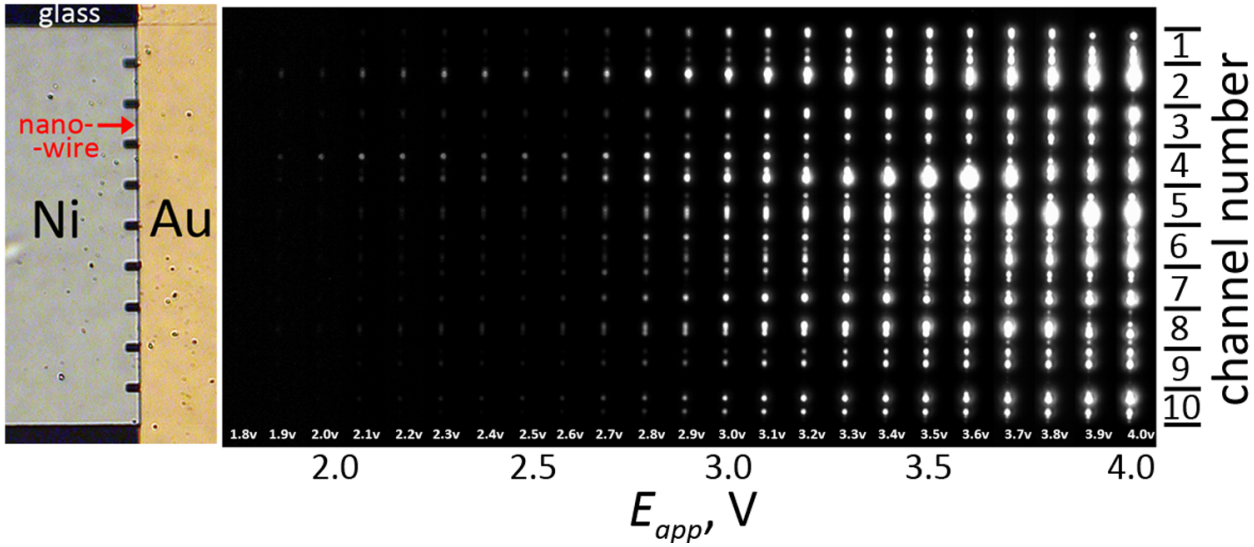

Figure 2.6: Optical micrograph of EL emission as a function of E_{app} for a ten-element *tn-ELJs* with w_{CdSe} = 102 nm. At left is shown an optical micrograph of the ten electrode array, showing the vertical orientation of the CdSe nanowire and the position of the nickel contacts.

device structures where the spacing of electrodes has been varied (Table 1.1), and it derives in part from the ohmic resistance imposed by the emitter layer. The lowest values for V_{th} are those where the narrowest electrode spacings were used. For example, Gudiksen *et al.*[33] reported a V_{th} of 1.7 V for EL emission from transistors with electrode spacings of 30 nm. EL from gold nanogaps that are 100-200 nm in width and filled with electrodeposited CdSe[100] are characterized by V_{th} = 1.5 - 1.9 V. It should be noted that even lower values of V_{th} have been demonstrated in cases where hole and electron transporting layers have been added on either side of the CdSe emitted layer, irrespective of the electrode spacing.[55, 51, 90, 112, 82]

tn-ELJs with narrow CdSe emitters are also capable of brighter EL emission. For example, the maximum EL intensity produced at w_{CdSe} = 102 nm using 3 V is twice as high as the maximum EL intensity measured for the 448 nm *tn-ELJs* at 26 V (Figure 2.7a). But the quantum efficiency of EL emission is actually inversely correlated with w_{CdSe}. In the plot of external quantum yield (EQE) *versus* the electric field, $\mathcal{E}$ (Figure 2.7c), devices with all five values of w_{CdSe} show similar EQE values at low $\mathcal{E}$ of $\approx 2 \times 10^7$ V/m. But for higher

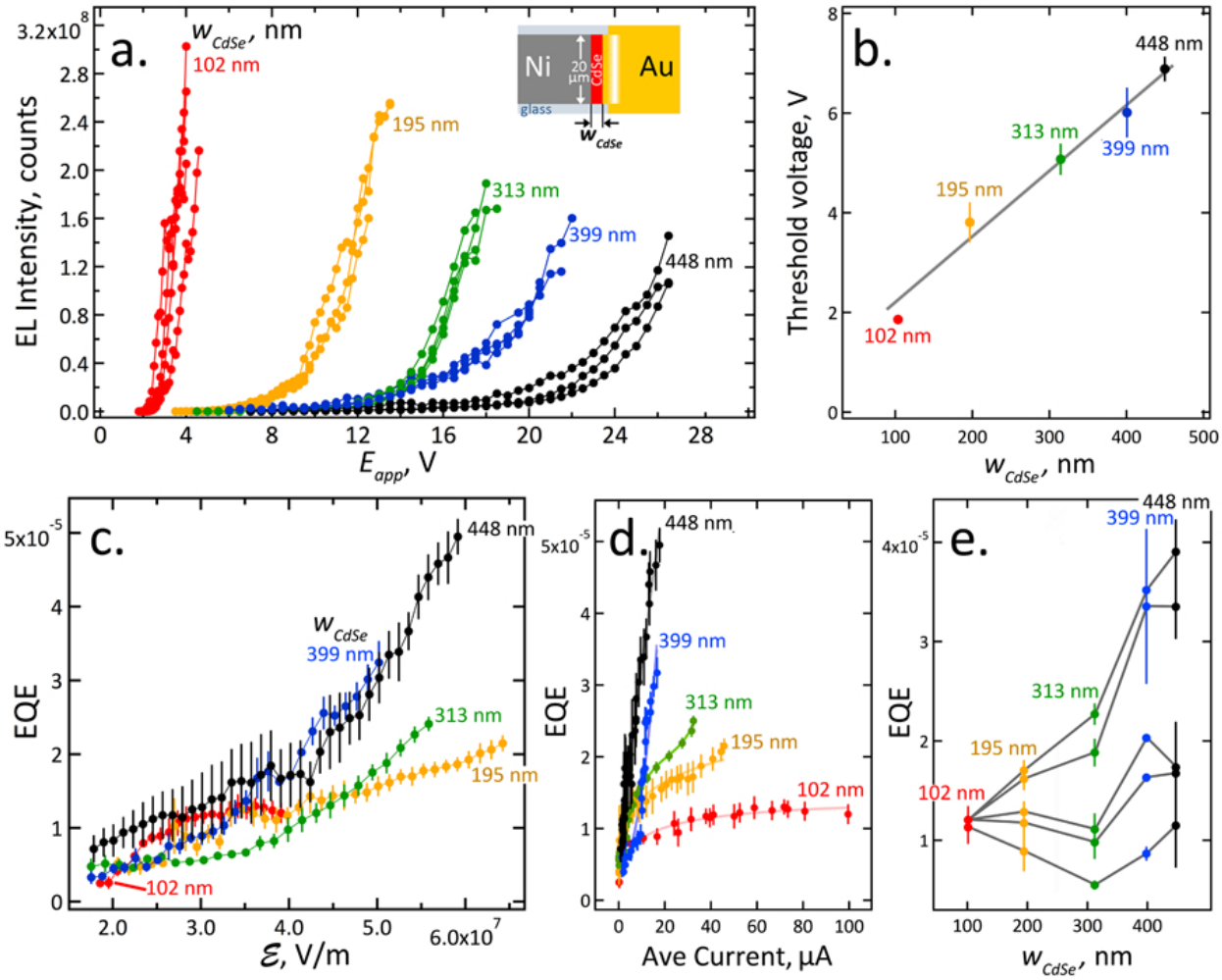

Figure 2.7: Optical characterization of Ni-CdSe-Au *tn-ELJs*. a) *EL* intensity *versus* E_{app} for five widths of devices described in Figure 2.5. Error bars represent $\pm 1\sigma$ for n devices as follows: $n = 3$ ($w_{CdSe} = 102$ nm), $n = 3$ (195 nm), $n = 4$ (313 nm), $n = 4$ (399 nm), and $n = 3$ (448 nm). b) Threshold voltage, V_{th}, *versus* w_{CdSe}. Here, V_{th} is estimated as the lowest voltage at which *EL* emission is observed above background. c) External quantum efficiency (EQE) *versus* electric field, $\mathcal{E}$ for the five devices described in Figure 2.5. d) *EQE* *versus* average device current. e) *EQE* for the five devices described in Figure 2.5, each corresponding to five discrete $\mathcal{E}$ values: 2.85, 3.90, 4.15, 5.15, 5.50 ($\times 10^7$ V/m).

fields of up to 6×10^7 V/m, EQE is preferentially increased for the widest emitter layers (w_{CdSe} = 313, 399, and 448 nm). At high fields, for example, the 448 nm *tn-ELJs* produces an EQE ($\approx 5 \times 10^{-5}$) that is five times as high as the maximum EQE measured for the 102 nm *tn-ELJs*. This EQE is amongst the largest measured for CdSe EL devices that do not have dedicated hole and/or electron injection layers (Table 1.1).

A plot of EQE *versus* current (Figure 2.7d) shows that, in general, EQE increases monotonically with increasing current. The slope of this increase is correlated with w_{CdSe}. The exception to this rule involves the narrowest emitter layer, w_{CdSe} = 102 nm, where the EQE first increases, and then reaches a plateau at a maximum EQE of $\approx 1.2 \times 10^{-5}$. Wider CdSe layers show more steeply sloping EQE *versus* current behavior, and larger EQE_{max} as current is increased, but the maximum attainable current and therefore EQE in wide CdSe emitter layers are both limited (Figure 2.7d).

In Figure 2.7e, the EQE is plotted for *tn-ELJs* as a function of w_{CdSe} for five discrete $\mathcal{E}$ values. This plot highlights the fact that wide CdSe emitter layers produce elevated EQE only at high fields, $\mathcal{E} > 5 \times 10^7$ V/m. At lower $\mathcal{E}$ values, EQE for *tn-ELJs* with five w_{CdSe} are within a factor of two of each other (Figure 2.7e).

2.3.5 Electroluminescence Spectra and Mechanisms

A typical EL spectrum for a *tn-ELJs* (Figure 2.8a) shows a broad emission envelope spanning the wavelength range from 500 nm to 1000 nm. A photoluminescence (PL, λ_{ex} = 532 nm) spectrum for electrodeposited *nc*-CdSe is much narrower, and centered at the 725 nm bandgap, E_{bg}, of CdSe (Figure 2.8). This dramatic broadening of the spectral output in EL as compared with PL has been observed in many previous studies involving a range of materials.[6, 25, 53, 24, 33, 82] A second characteristic feature of EL emission in *tn-ELJs*, already seen in Figure 2.6, is that the EL produced within a 20 μm wide element consists of

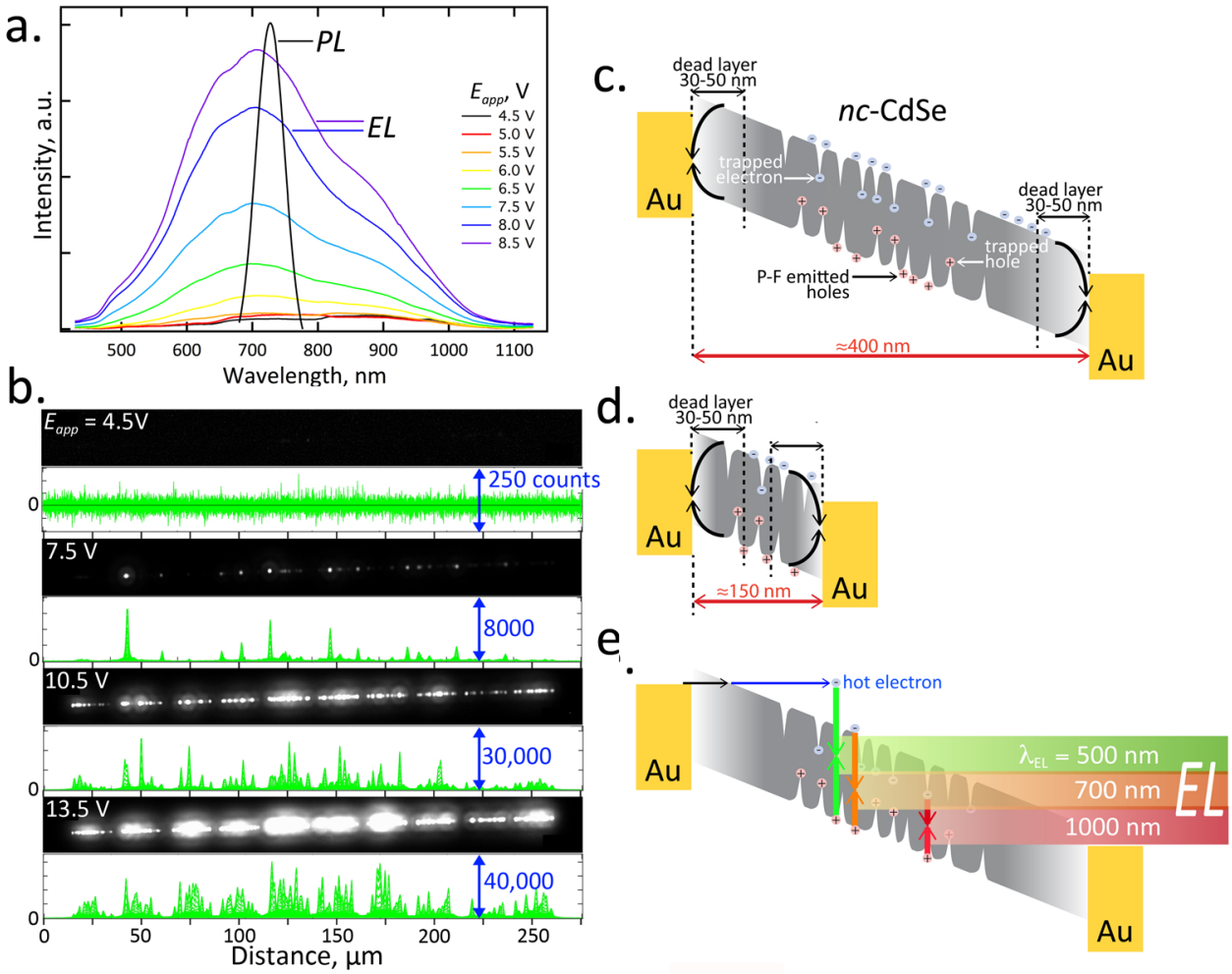

Figure 2.8: Spectra and proposed mechanism for EL emission. a) EL spectra as a function of E_{app} for a ten-element *tn-ELJs* with $w_{CdSe} = 102$ nm. PL spectrum acquired with excitation at $\lambda_{ex} = 532$ nm. b) Micrographs and intensity plots for a $w_{CdSe} = 195$ nm *tn-ELJs* at four $E_{app} = 4.5$ V - 13.5 V. EL emission consists of a series of sub-micron point emitters that coalesce at high E_{app}. c) Schematic energy level diagram for a wide ($w_{CdSe} = 400$ nm) *nc*-CdSe emitter layer illustrating the presence of deep trap states for electrons and holes, and the presence of a dead layer in which e^-/h^+ recombination is nonradiative. d) Same diagram as in (c) except illustrating a narrow ($w_{CdSe} = 150$ nm) *nc*-CdSe emitter layer, e) Processes contributing to broad-band EL emission including hot electron-hole recombination ($h\nu > E_{bg}$, green), band-edge emission ($h\nu \approx E_{bg}$, orange), and free hole-trapped electron recombination ($h\nu < E_{bg}$, red).

a series of sub-micron point emitters - even at high E_{app}. This is apparent in the images and plots of Figure 2.8b that show emission from a w_{CdSe} = 195 nm *tn-ELJ* at E_{app} from 4.5 V to 13.5 V. One possible reason for localized light emission is modulation of the electric field along the axis of each CdSe nanowire, caused by its width nonuniformity. In this case, local constrictions in width would correlate with a locally higher $\mathcal{E}$ and enhanced EL emission. The number and total area of the light emitting regions increases with E_{app}. The spectrum of Figure 2.8a was acquired for a device consisting of ten *tn-ELJs*, and therefore contains many point emitters. Spectra for single point emitters could not be acquired in this study, but there is evidence that the broad emission seen in Figure 2.8a is produced by each point emitter and is not the sum of many narrower emission spectrs produced by an ensemble of point emitters. The evidence takes the form of the potential dependence (Figure 2.8a). At low E_{app} values (≈4 V), just a handful of point emitters are observed and the total EL intensity is very low, but the spectral width of the EL emission is similar to that seen at higher E_{app} values, although emission is somewhat red-shifted. This observation suggests that each micron-scale emitter produces a broad spectrum and that the spectral width seen for many emitters (e.g., Figure 2.8a) is not a function of the number of emitters, with each producing a much narrower emission envelope.

A schematic band diagram (Figure 2.8c-e) illustrates the salient features of EL emission in these nickel-(*nc*-CdSe)-gold *tn-ELJs*. The observed reduction in EQE with decreasing w_{CdSe} (Figure 2.7d,e) suggests the presence of "dead layers" adjacent to the metal contacts within which EL is quenched. This phenomenon has been described previously in connection with EL in thin-film M-S-M devices,[21, 64] but the mechanism responsible for dead layers remains unresolved. One possible mechanism accounting for a dead layer adjacent to metal contacts is the physical diffusion/migration of electrons and/or holes to these metal contacts and their subsequent radiationless recombination. In this case, the thickness of the dead layers should approximate the minority carrier diffusion length, estimated to be 30-50 nm based upon our prior measurements of carrier mobilities [4] and minority carrier lifetimes[46]

in electrodeposited *nc*-CdSe. A second possibility, also suggested by others,[67] is that radiationless recombination near a contact is a symptom of poorer CdSe quality, in terms of impurities and crystallinity. Further work will be required to elucidate this mechanism.

Also as depicted in Figure 2.8c-e, the *nc*-CdSe emitter contains deep traps for both electrons and holes, associated mainly with disorder and inpurities at grain boundaries. As E_{app} is increased, $\mathcal{E}$ exceeds the threshold for P-F emission ($> 5 \times 10^7$ V/m) which triggers the release by field-ionization of trapped holes. Field-emitted, mobile holes rapidly and radiatively recombine with electrons to produce EL. The broad spectral envelope for EL emission seen in Figure 2.8a is accounted for by the operation of three processes in parallel (Figure 2.8e): i) hot electron-hole recombination ($h\nu > E_{bg}$, green), ii) band-edge emission ($h\nu \approx E_{bg}$, orange), and, iii) free hole-trapped electron recombination ($h\nu < E_{bg}$, red). But although EL emission that is red-shifted from E_{bg} is likely caused by trapped carriers, it remains unclear (also in other studies) why the electron and hole traps leading to red-shifted emission in EL are preferentially populated in EL relative to PL.

2.3.6 Conclusion

In conclusion, we describe a discovery platform that consists of arrays of transverse nanowire light emitting nanojunctions or *tn-ELJs*. These device arrays have the potential to advance our understanding of EL in electrodeposited materials - in this case, arrays of nickel-(*nc*-CdSe)-gold *tn-ELJs*. These *tn-ELJs* exhibit highly reproducible, and tunable, properties for EL light emission that are strongly influenced by the width of the CdSe emitter layer along the electrical axis, w_{CdSe}. Transport in *tn-ELJs* involves a progression of three mechanisms as E_{app} is increased - ohmic conduction, space-charge limited conduction, and Poole-Frenkel (P-F) emission. The voltage threshold for light emission, ranging from 2 V to 7 V, is directly proportional to w_{CdSe} from 100 nm to 450 nm. The external quantum efficiency (EQE) of

the observed EL increases for all *tn-ELJs* with the applied electric field, suggesting that P-F emission of mobile holes into the valance band is rate-limiting. Finally, the maximum external quantum efficiency (EQE_{max}) also increases monotonically with w_{CdSe}, up to 5×10^{-5} for $w_{CdSe} = 450$ nm. These observations are consistent with a mechanism of EL light emission involving the P-F emission of holes in the valence band of the electrodeposited *nc*-CdSe nanowire, with subsequent radiative recombination with electrons that are both injected above the conduction band-edge (hot electrons), and others that are trapped, leading to a broad spectral bandwidth for the emission process. Working in opposition to this process is nonradiative electron-hole recombination near (within 30-50 nm) the metal electrical contacts, leading to higher EQE in wide CdSe emitters.

The maximum EQE obtained here of 5×10^{-5} is low, but comparable or better than in previous studies where the same M-S-M architecture has been studied (Table 1.1). In future work, the influence of dedicated hole and electron injecting and transporting layers adjacent to the CdSe emitter layer will be evaluated as a means for obtaining higher EL quantum efficiencies.[84, 90]

2.4 Methods

2.4.1 Device Fabrication

CdSe light emitting devices were fabricated using the LPNE method in combination with several additional photolithography steps (Figure 2.1). First, a 60 nm thick layer of nickel was thermally evaporated on a precleaned soda lime glass slide (2.5 cm × 2.5 cm × 1 mm). Then a layer of photoresist (PR, Shipley, S1808) was spin-coated (2500 rpm, 80 s) onto the nickel surface, followed by a soft-bake at (90°C) for 30 min. The PR-coated nickel was then

covered with a contact mask, exposed to UV light, and the exposed PR was developed for 20 s (Microposit, MF-319), rinsed with water (Millipore MilliQ, $\rho > 18$ M$\Omega\cdot$ cm), and air dried. The freshly exposed nickel layer was then removed using nickel etchant (Alfa Aesar) for 2 min, resulting in six parallel 10-finger patterns consisting of 20 μm wide Ni-CdSe-Au *tn-ELJs* spaced by 5 μm (Figure 2.2). The photoresist layer was then removed with acetone and a second layer of photoresist (Shipley, S1808) was spin-coated and photolithographically patterned. Exposed nickel was over-etched in 0.80 M nitric acid for 6 8 min to create a horizontal trench with a width of 300 nm $\sim$ 1 μm at the end of each nickel finger.

CdSe nanowires were electrodeposited into these trenches potentiostatically at -0.60 V *versus* saturated calomel electrode (SCE) in an unstirred, room temperature, aqueous plating solution consisting of 0.30M $CdSO_4$, 0.70mM SeO_2, and 0.25 M H_2SO_4 at pH 1-2. (Caution: both $CdSO_4$ and SeO_2 are highly toxic). Gold contacts were then electrodeposited onto the solution-exposed edge of the CdSe nanowire potentiostatically at -0.90 V *versus* SCE using a Clean Earth Inc. gold plating solution. Gold deposition was continued until the gold emerged from the trench, as signaled by an increase in the electrodeposition current (Figure 2.3d). All electrodeposition operations were carried out using a Gamry Series G 300 potentiostat in conjunction with a one compartment three-electrode electrochemical cell with SCE as the reference electrode and platinum foil as the counter electrode. After gold electrodeposition, a layer of gold was thermally evaporated to form a connection with the electrodeposited gold contact, facilitating the attachment of wire contacts. The PVD-deposited gold on the photoresist coated portion of the device was removed by lift-off.

2.4.2 Structural Characterization

Scanning electron microscopy (SEM) images were acquired using a FEI Magellan 400 XHR system at an accelerating voltage of 1 or 8 keV without metal or carbon coating. Energy-

dispersive X-ray spectroscopy (EDS) images were also acquired using this instrument which is equipped with a 80 mm^2 silicon drift X-ray detector (Oxford Instruments, with Aztec software).

2.4.3 Electroluminescence and Photoluminescence

EL images as a function of bias were acquired using an inverted microscope (Olympus, IX71) equipped with a 40× objective lens (Olympus, LUCPlanFLN 40×0.60) and a CMOS camera (Andor, Neo) as Figure 2.9 shows. Electrical measurements during EL emission were accomplished using a sourcemeter (Keithley 2400) controlled by LabVIEW software. EQE was calculated using the number of photons out of *tn-ELJs* devices devided by the number of electrons flowing through the material per second. Cmos sensitivity and geomtry loss was factored into calculation. EL spectra were obtained using a spectrometer (Andor, Shamrock SR-500i-D2) equiped with a 300 l/mm grating blazed at 760nm and a CCD camera (Andor, Newton). All the EL measurements were carried out under cooling condition using a Peltier cooling device (Custom Thermoelectric, 19012-5L31-06CQQ-X) in nitrogen environment(to avoid water condensation or frost). PL spectra were acquired using a SpectraPro 2300i spectrometer (Princeton Instruments, Acton) excited by a 532nm laser.

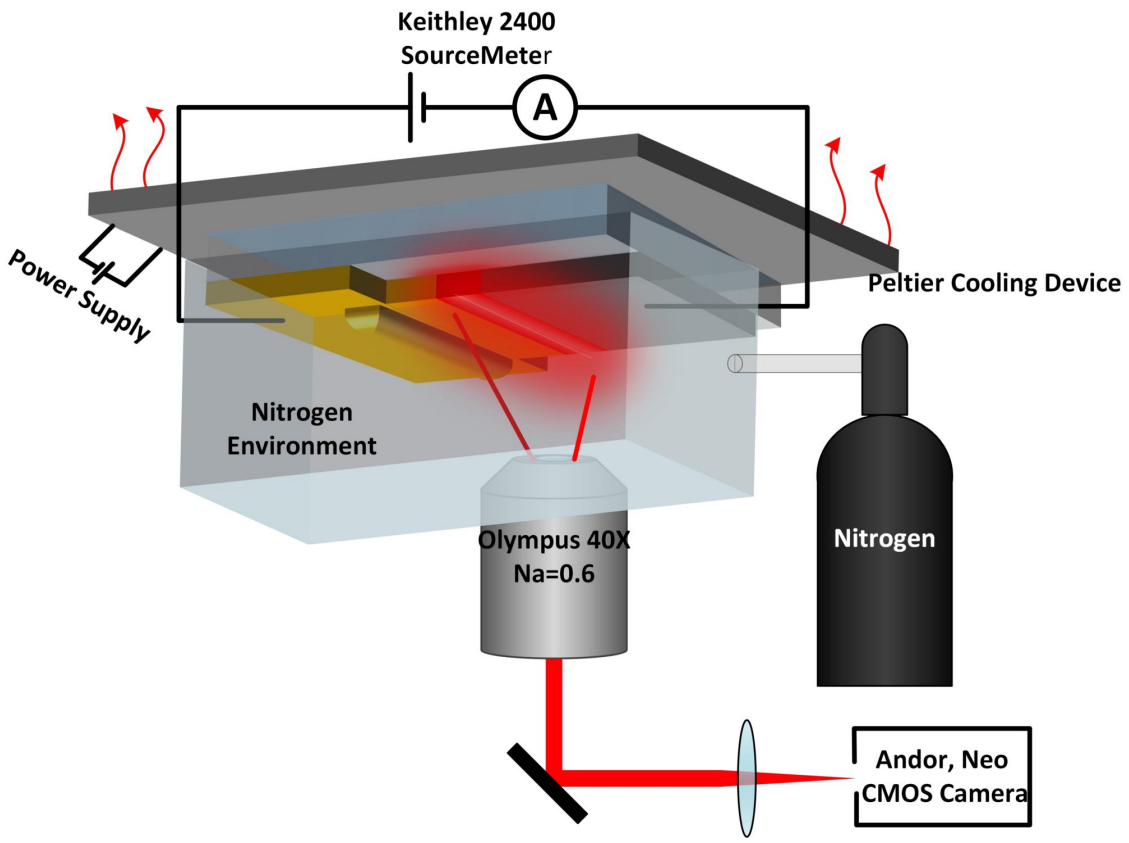

Figure 2.9: EL measurement set-up. The *tn-LEJs* was glued on a $1inch \times 3inches$ glass slide then glued on a peltier cooling device using the copper tape. The peltier was used to remove the heat generated during EL measurement. The *tn-LEJs* was connected to a Keithley 2400 sourcemeter, and then the whole device was placed on an inverted microscope stage. The device along with the objective lens were wrapped with regular food wrap to create a sealed environment. The food wrap was then pierced through by a small glass pipe connected with a nitrogen tank. A nitrogen environment was created during EL measurenment to avoid water condensation or frost.

Chapter 3

It's *EESC*: Rapid, Wet Chemical Fabrication of Radial Junction Electroluminescent Wires

To be submitted.

3.1 Introduction

Can a wet chemical fabrication route to electroluminescent *wires* be realized, and what level of performance can be achieved for EL emitters prepared by such a process? The *EESC* process described here is a high throughput, wet-chemical process for assembling a radial junction EL wire emitter consisting of concentric layers of three well-studied nanocrystalline (or amorphous) materials: Au, CdSe, and the polystyrene sulfonate (PSS) salt of poly(3,4-ethylenedioxythiophene (PEDOT:PSS).

In the first step of the *EESC* process, ultra-long (mm scale) gold nanowires are fabricated us-

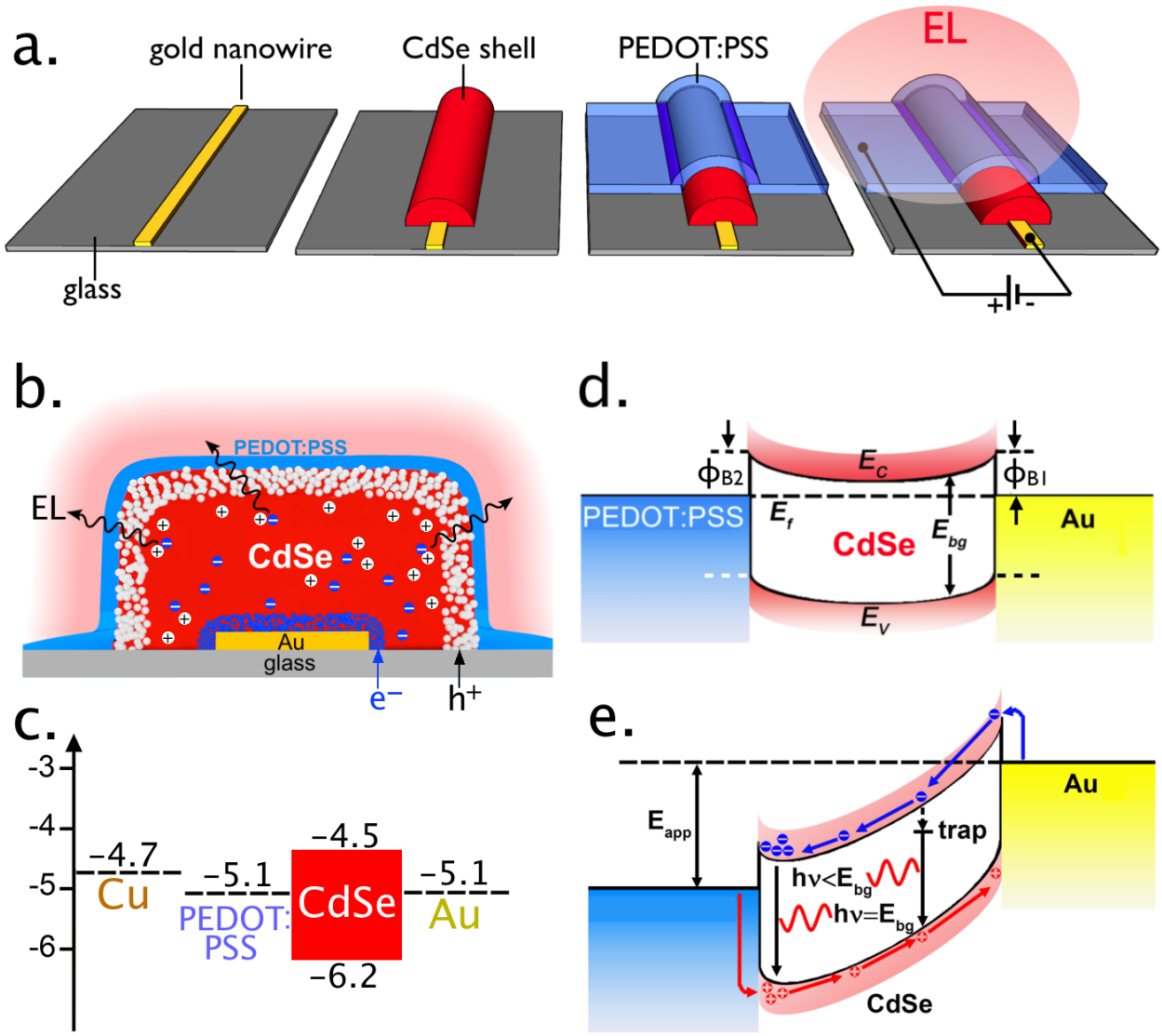

Figure 3.1: *EESC* fabrication of a Au@CdSe@PEDOT:PSS EL-emitting wire. a) Schematic three-step *EESC* process flow for fabrication of Au@CdSe@PEDOT:PSS wires. b) Cross-sectional view of this wire showing gold center electrode, red CdSe emitter layer, and blue PEDOT:PSS hole injecting layer. Electrons (dark blue), injected at the gold-CdSe interface radiatively recombine with holes (white) injected at the CdSe-PEDOT:PSS interface to produce EL emission at the CdSe bandgap. Hole injection is facilitated by a PEDOT:PSS/CdSe interface that is 2 - 5 fold larger than the complimentary gold-CdSe interface, depending upon the diameter of the CdSe shell. c) Energy diagram showing the relative energies of band edges for filled states (Au, PEDOT:PSS and Au) as well as the conduction band edge of CdSe. d,e) Band diagrams illustrating energetic relationships for the three layers at equilibrium (d) and in "forward bias" corresponding to Au (-) with E_{app}≈1.6 V (e). $\phi_{B1} \approx \phi_{B2} =$ 0.64 eV. $E_{BG} = 1.70$ eV.

ing the lithographically patterned nanowire electrodeposition (LPNE) process.[99, 58] Then, 25 μm sections of this gold nanowire are used as electrodes to electrochemically synthesize a conformal and hemicylindrical CdSe shell with a controlled thickness that can be varied from 300 - 1200 nm. Finally, a PEDOT:PSS over-coating is applied by spin-coating to complete the device structure (Figure 3.1a). Since the first electrodeposition step that patterns a gold nanowire is accomplished using LPNE which involves photolithography, *EESC* is not a "solution processing" scheme in the strictest sense of that phrase, because photolithography is intrinsic to LPNE, but no clean room is required by the LPNE process[99, 58] and the subsequent two steps are wet chemical in nature. In this proof-of-concept demonstration, the EL wires produced by *EESC* are 25 μm in length, amongst the longest so far demonstrated to our knowledge, but the *EESC* process is scalable to nanowires of any length, limited only by the length of the central metal nanowire which can readily be 1.0 cm using LPNE.$^{e.g.}$[**?**] These 25 μm wires provide the opportunity to assess the *uniformity* of light emission along the axis of these structures, as well as other metrics.

EL light emission is produced by the recombination of injected electrons and holes within the CdSe shell (Figure 3.1b), along the entire length of the wire. In spite of the energetic symmetry of this device (Figure 3.1c), hole injection, at a high barrier CdSe-PEDOT:PSS interface ($\phi_h \approx 1.1$ V), is facilitated by a contact area that is 1.9 - 4.7 fold larger than the complimentary gold-CdSe electron-injecting contact ($\phi_e \approx 0.6$ V) contributing to low voltage thresholds (1.4 - 1.7 V) for EL emission.

3.2 Fabrication Process

The *EESC* process. Electroluminescent Au@CdSe@PEDOT:PSS wires were fabricated using the *EESC* process flow (Figure 3.2a). In summary, steps 1 - 5 are standard LPNE[99, 58] process flow for the fabrication by electrodeposition of a gold nanowire. Steps 6 and 7

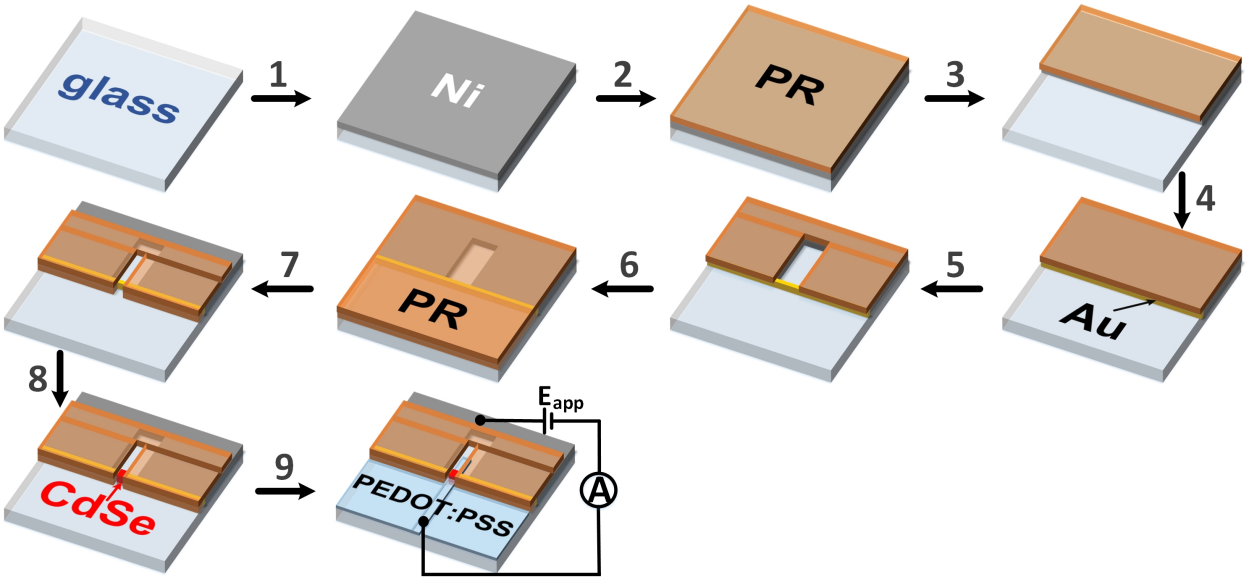

Figure 3.2: Fabrication of Au@CdSe@PEDOT:PSS wires by *EESC*. Process flow: Step 1 - a 60 nm thick layer of nickel is thermally evaporated on a glass slide. Step 2 - photoresist (PR, Shipley S1808) is spin-coated onto the nickel surface. Step 3 - a horizontal trench 60 nm (h) $\times$ 2.5 cm (l) $\times$ 1 μm (d) is produced in the PR layer adjacent to the edge of the nickel film. Step 4 - nickel edge is immersed in a Au plating solution and a Au nanowire is electrodeposited using the nickel edge as the working electrode. Step 5 - a 2 mm width trench exposes the gold nanowire. Step 6 - PR layer is removed and a thicker PR layer (Shipley, S1827) is spin-coated. Step 7 - a window of 25 μm width is created. Step 8 - a CdSe shell is electrodeposited on exposed gold nanowire; the thickness of the CdSe shell is controlled by the electrodeposition time. Step 9 - a layer of PEDOT:PSS is applied as a transparent top positive electrode.

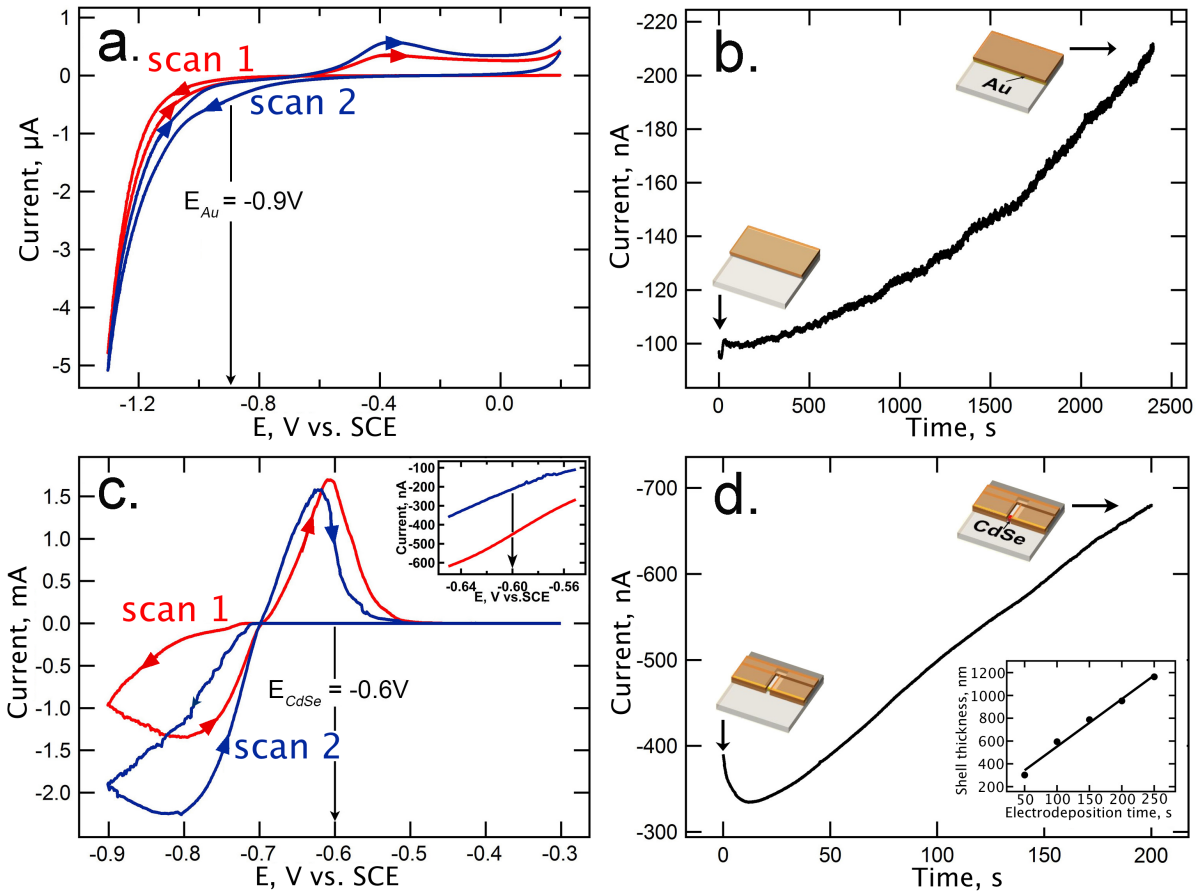

Figure 3.3: a,b). Gold electrodeposition cyclic voltammograms (CVs) at 50 mV/s in Clean Earth Inc. gold plating solution, (a) and current *vs.* time transients (b). c,d). CdSe electrodeposition CVs at 50 mV/s (c) and current vs. time transients and the inset shows CdSe shell thickness vs. electrodeposition time(d).

are optional, as they provide for masking of the gold nanowire prior to electrodepositing the CdSe shell, in step 8. Electrical contacts are attached in step 9 (Figure 3.2a).

The two most critical steps of the *EESC* process are the two electrodeposition steps: gold in Step 5 and CdSe in Step 8. Gold electrodeposition occurs under conditions of activation control at -0.90 V vs. SCE, located at the foot of the gold plating wave (Figure 3.3a), in a commercial gold plating solution (Clean Earth Inc.).[78, 101] Approximately 40 minutes is required to produce a gold nanowire that is ≈850 nm in width within a 60 nm horizontal

trench that defines its height. During this 40 minutes, the gold plating current increases by a factor of approximately two (Figure 3.3b) as the solution-wetted gold surface roughens, as clearly seen in the SEM image of Figure 3.4e, for the gold nanowire (left edge).

The CdSe shell, 350 - 1150 nm in radius, is electrodeposited from an aqueous plating solution according to the reaction: $Cd^{2+} + H_2SeO_3 + 4H^+ + 6e^- \rightarrow CdSe(s) + 3H_2O$ from a solution containing 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1-2 (**caution: both $CdSO_4$ and SeO_2 are highly toxic**).[78, 101] As previously demonstrated,[78, 101] a stoichiometric CdSe layer is obtained by activation-controlled electrodeposition at a constant potential of -0.60 V vs. SCE (Figure 3.3c). Using an unstirred, room temperature plating solution, the duration of the CdSe growth is 50 to 250 seconds, depending upon the shell thickness that is desired.[78, 101] The deposition current increases during this deposition process in approximate proportion to the increasing area of the hemicylindrical CdSe-surface (Figure 3.3d). Finally, the PEDOT:PSS layer is deposited by spin-coating (2500 rpm, 80 s) onto the glass slide twice, with air drying of the layer between these two depositions.

3.3 Results and Discussion

3.3.1 SEM and AFM Characterization

SEM and AFM characterization. If the PEDOT:PSS layer is omitted, the uniformity of the electrodeposited CdSe layer can be evaluated using SEM. Images for Au@CdSe wires (Figure 3.4a) shows a smooth CdSe layer with a uniform thickness along the axis of the wire. This uniformity is a direct consequence of kinetically-controlled CdSe electrodeposition that produces a constant current density (A/cm^2), unaffected by more rapid diffusional transport of Cd^{2+} and SeO_3^{2-} expected at the left and right edges of the CdSe layer. EDX elemental maps also show spatially uniform Cd and Se concentrations along the wire axis (Figure 3.4b)

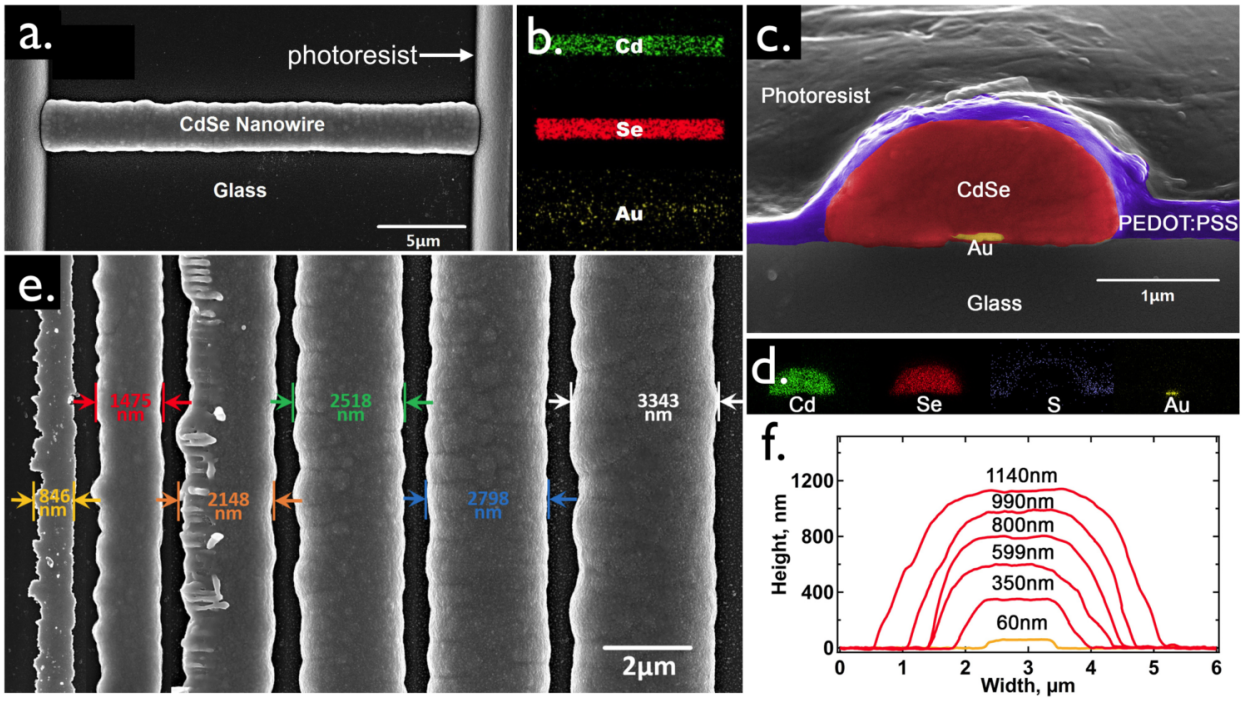

Figure 3.4: Scanning electron microscopy (SEM) and atomic force microscopy (AFM). a) Low magnification SEM image of a 25 μm length Au@CdSe@PEDOT:PSS wire, b) Electron dispersive x-ray (EDX) elemental map showing Cd (green), Se (red) and Au (yellow), c). Cross-sectional SEM image showing (in false color) central gold nanowire (yellow), CdSe shell (red), and PEDOT:PSS top layer (blue). d) EDX elemental map showing Cd (green), Se (red), S (blue) and gold (yellow), e) Bare Au and five Au@CdSe@PEDOT:PSS wires ranging in diameter from 846 nm (left) to 3343 nm (right), f) AFM height traces for the same six GCP wires shown in (e). The excess apparent width seen in these data, relative to (e) is the result of convolution of the AFM tip with the wire. The total vertical height is accurate.

as well as within the CdSe shell (Figure 3.4d). A Au EDX map (Figure 3.4b) shows low signal caused by the attenuation of electrons by the intervening CdSe shell, but the EDX signal for this nanowire is seen in the EDX map of the cross-section (Figure 3.4d). Cross-sectional SEM images of wires (Figure 3.4c) reveal the gold nanowire at the glass surface, surrounded by the CdSe shell (≈ 1.0 μm in radius), and the PEDOT:PSS overlayer with a thickness varying from 150 nm to 300 nm in this case. The CdSe shell can be grown conformally over a wide range of radii from 300 nm to 1200 nm, as seen in the SEM image and AFM height-distance traces of Figure 3.4e and 3.4f, respectively.

3.3.2 Current Transport

Transport in Au@CdSe@PEDOT:PSS wires. Au@CdSe@PEDOT:PSS wires are metal-semiconductor-metal (M-S-M) junctions in which both the gold and PEDOT:PSS layers are metallic with approximately the same work function, ϕ: 5.1 eV (Figure 3.1c). When contacted by CdSe, both Au and PEDOT:PSS produce a rectifying Schottky barrier (Figure 3.1d,e).[92, 70, 68, 14] For the Au@CdSe@PEDOT:PSS device, the two Schottky barriers are oriented back-to-back: one forward biased (with metal-(+) polarity) and one reverse biased (metal-(−)). For a uniformly n-doped semiconductor (the present case), current is limited by the reverse biased junction and majority electrons dominate charge transport relative to holes. This is because of the disparity between the barrier height for electrons, $\phi_n \approx 0.64$ eV and holes, $\phi_p \approx 1.06$ eV.

If the metal-semiconductor junctions are identical, current *versus* E_{app} (or I-V) curves show an exponentially increasing current in both directions and are symmetrical about $E_{app} = 0$,

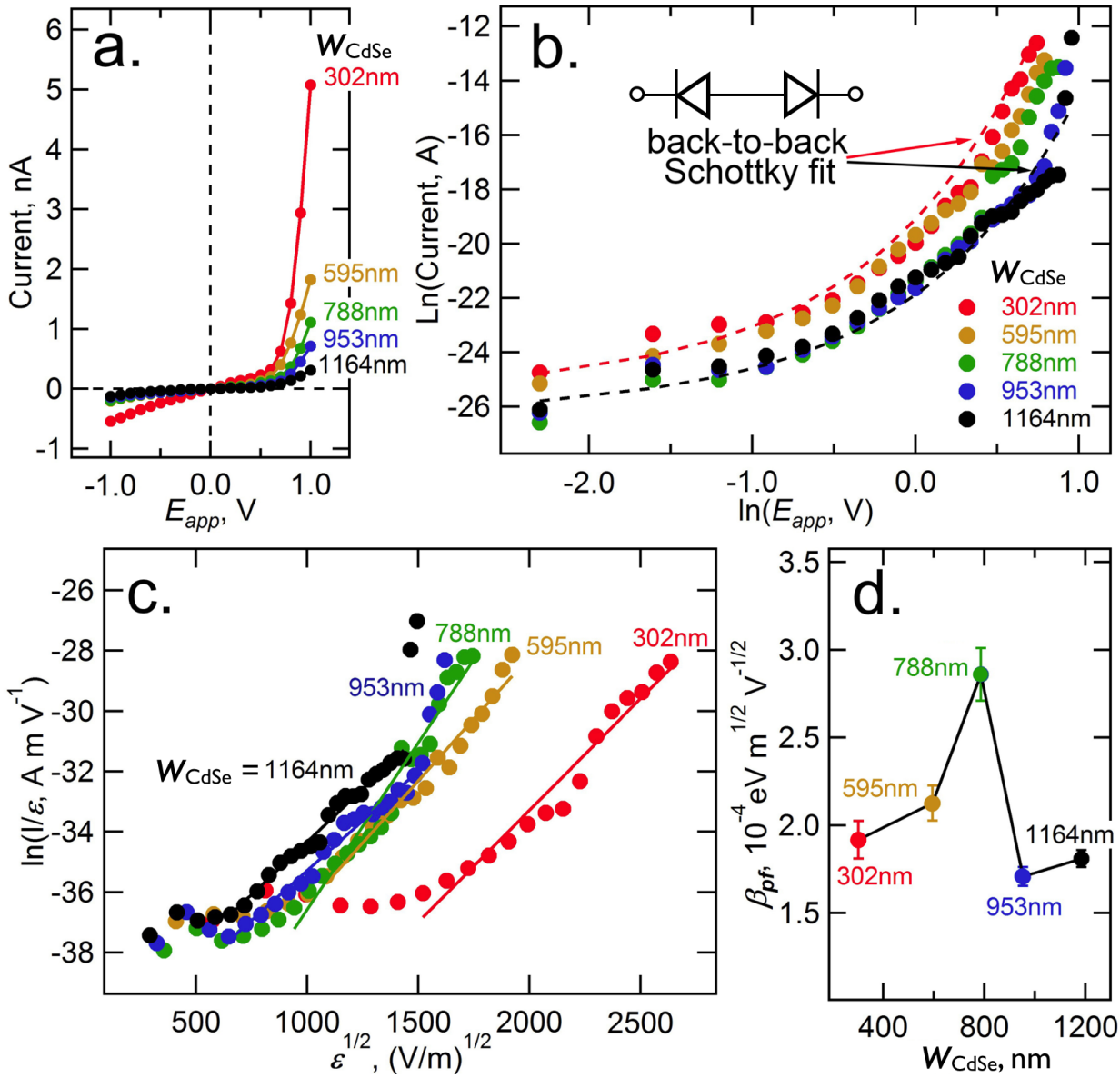

Figure 3.5: Transport properties of Au@CdSe@PEDOT:PSS wires (In this figure, (+) bias polarity indicates PEDOT:PSS (+) and Au (-) polarity.) a) Current-voltage (I-V) plots showing the low voltage region ($E_{app} < 1.0$ V) for five CdSe shell thicknesses as indicated. b) Ln(I) *versus* Ln(E_{app}) from 0 to + 2.5 V for the same five CdSe shell thicknesses showing agreement of these data with the back-to-back Schottky diode model of Eq. 3.1. The two dashed lines are the predictions of Eq. 3.1 for back-to-back Schottky barriers, using the parameters of Table 3.1 for $w_{CdSe} = 302$ nm (red) and 1164 nm (black). c) Plot of Ln(I/$\mathcal{E}$) *versus* $\mathcal{E}^{1/2}$, and the linear region fitted Poole-Frenkel emission Eq. 3.3. d) Poole-Frenkel field lowering coefficient, β_{pf}, *versus* w_{CdSe} showing values an order of magnitude higher than the theoretically predicted value of $\beta_{pf} \approx 2.5$ x 10^{-5} eV m$^{1/2}$ V$^{-1/2}$.

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conforming to the equation:[88, 14, 87, 93, 70, 68]

$$I(V) = \frac{2I_1 I_2 sinh\left(\frac{qV}{2KT}\right)}{I_1 exp\left(-\frac{qV}{2n_1 KT}\right) + I_2 exp\left(\frac{qV}{2n_2 KT}\right)} \tag{3.1}$$

Where I_1 is given by:[92, 88, 14, 87]

$$I_1 = A^{**} A_1 T^2 exp\left(\frac{-q\phi_{B1}}{KT}\right) \tag{3.2}$$

The equation for I_2 is analogous. Here A^{**} is the effective Richardson constant that is assumed to be 15.6 A cm^{-2} K^{-1} [75] for both Au-CdSe and PEDOT:PSS-CdSe Schottky barriers (Table 3.1). ϕ_{B1} is the barrier height for electrons at the Au-CdSe whereas ϕ_{B2}, used in the analogous expression for I_2, applies to the PEDOT:PSS-CdSe contact (Figure 1d). n_1 and n_2 are the ideality factors for these two junctions while A_1 and A_2 are their respective interface areas.[91]

But in spite of the symmetry implied by the energy level diagram (Figure 3.1c), symmetrical *I-V* curves are not observed (Figure 3.5a). Instead, significantly more current is seen for E_{app}-(+) bias, corresponding to Au (-); PEDOT:PSS (+) polarity. Henceforth, we refer to this as "forward bias". This asymmetry in the *I-V* curve is attributed to three factors: First, the interfacial area of the CdSe-PEDOT:PSS junction is larger relative to the Au-CdSe junction, a factor that should facilitate hole injection from a (+) PEDOT:PSS contact into CdSe. The ratio of these areas depends upon the radius of the CdSe shell (w_{CdSe}), and increases from 1.9 (w_{CdSe} = 350 nm) to 4.7 (1140 nm)(Table 3.1). Second, while both Au and PEDOT:PSS are metallic with similar work functions, they are otherwise very different

Table 3.1: Fitting Parameters For The Calculation of I-V Curves Using the Back-to-Back Diode Model (Eq. (3.1))

W_{CdSe} (nm)	A^{**a} (A cm^{-2} K^{-1})	${\phi_{B1}}^b$ (eV)	${\phi_{B2}}^c$ (eV)	${n_1}^d$	${n_2}^e$	A_2/A_1
302	15.6	0.628	0.586	1.11	1.48	1.9
595	15.6	0.615	0.638	1.15	1.33	2.8
788	15.6	0.643	0.643	1.14	1.38	3.4
953	15.6	0.653	0.642	1.11	1.38	4.0
1164	15.6	0.649	0.672	1.16	1.29	4.7

[a] A^{**} = effective Richardson constant for CdSe.[75]
[b] ϕ_{B1} = Schottky barrier height for Au-CdSe contact.
[c] ϕ_{B2} = Schottky barrier height for PEDOT:PSS-CdSe contact.
[d] n_1 = ideality factor for Au-CdSe contact
[e] n_2 = ideality factor for PEDOT:PSS-CdSe contact
A_1 = interface area for Au-CdSe contact
A_2 = interface area for PEDOT:PSS-CdSe contact

materials, having radically different electronic structures and densities of states. Just as PEDOT:PSS is superior in terms of hole injection, Au is expected to provide for more efficient electron injection than PEDOT:PSS. Third, the Au-CdSe and PEDOT:PSS-CdSe interfaces are formed using fundamentally different processes - electrodeposition and solution casting, respectively. It is unclear, however, how the fabrication method influences the device properties.

Ideality factors at both junctions, n_1 and n_2, are obtained in the process of fitting experimental I-V curves using Eq. (3.1) (Table 3.1). These provide an indication of the degree to which these interfaces are operating in accordance with ideal thermionic emission, characterized by $n = 1$.[91] Deviations - usually in the positive direction - from $n = 1.0$ can be caused by image forces acting to reduce the barrier height, to interface states or traps at the interface, and simply by high dopant concentrations in the semiconductor.[91, 59] Ideality factor values for the Au-CdSe interface, n_1, are close to unity, ranging from 1.11 to

1.16 (Table 3.1) suggesting $EESC$ produces a low defect density contact between Au and CdSe, and that the CdSe dopant concentration is not too high to degrade n_1.[26, 72] Ideality factors for PEDOT:PSS (n_2) are higher, ranging from 1.29 to 1.48 (Table 3.1); larger than measured for Au-CdSe but comparable to, or lower than, n values reported for PEDOT:PSS interfaces with semiconductors, demonstrating that the quality of the PEDOT:PSS-CdSe interace produced by the $EECS$ process is not atypical.[29, 22]

"Forward bias" (Au (-)) is associated both with higher current (Figure 3.5a) and stronger EL light emission (*vide infra*) and within this regime, Eq (3.1) predicts experimental I-V curves for devices with all five CdSe shell thicknesses and across the entire E_{app} range measured here (Figure 3.5b). The fits to our data using Eq. (3.1) produce parameters summarized in Table 3.1 that are physically reasonable including barrier heights in the range from 0.59 to 0.67 eV that are in the range of barriers reported for macroscopic CdSe-Au Schottky barriers[95] and CdSe-PEDOT:PSS Schottky barriers[49]. The tentative conclusion is that in the Au-CdSe-PEDOT:PSS device, the two Schottky junctions are in full control of carrier transport.

Control of transport by other processes, operating in the bulk of the CdSe instead of at the junctions, would be revealed by negative deviations of the current from the predictions of Eq. (3.1). Two common processes invoked to account for such deviations are space charge limited conduction (SCLC) and Poole-Frenkel (P-F) emission. The absence of these two processes is significant because in planar Au-CdSe-Ni EL emitting junctions[78] both SCLC and PF emission have been detected at intermediate ($0.5 < E_{app} < 2$ V) and high (E_{app} ¿ 3 V) bias conditions, respectively, whereas Schottky control of transport was seen only at low E_{app} below 1.0 V.[78]

In particular, we looked carefully for evidence of PF emission at high biases because this process releases trapped minority carriers in the CdSe, accentuating EL emission in the bulk of the CdSe, in principle. PF emission is predicted by Eq. 3.3 which predicts a linear

$Ln(I/\mathcal{E})$ *versus* $\mathcal{E}^{1/2}$ in the regime of E_{app} where PF emission is occurring:[85, 86, 91]

$$J = J_0\ exp\left(\frac{\beta_{pf}\mathcal{E}^{1/2}}{kT}\right) \tag{3.3}$$

where β_{pf} is the PF field-lowering coefficient and $\mathcal{E}$ is the magnitude of the electric field (E_{app}/w_{CdSe}).[86, 91] Because linear $Ln(I/\mathcal{E})$ *versus* $\mathcal{E}^{1/2}$ is also predicted for Schottky emission (Eq. (3.1)),[91] it is also important to calculate the Poole-Frenkel field lowering coefficient, β_{PF} from the slope of this plot for comparison with the theoretically expected β_{pf} value of 2.55 $\times$ $10^{-5} eVm^{1/2}V^{-1/2}$[69] in order to validate PF emission as a possible contributor to transport. Plots of $Ln(I/\mathcal{E})$ *versus* $\mathcal{E}^{1/2}$ (Figure 3.5c) show linearity over a wide E_{app} range consistent with either PF or Schottky emission, but the calculated β_{PF} (Figure 3.5d) is too high, in the range from 1.5 - 2.8 $\times$ 10^{-4} eV $m^{-1/2}$ $V^{1/2}$ which is approximately an order of magnitude higher than the theoretical β_{pf} value.[69]. Beyond this, the electric fields generated in the region of linearity (1 $\times$ 10^6 V/m $< \mathcal{E} <$ 8 $\times$ 10^6 V/m) are significantly lower than have been required to generate PF emission in similar systems ($\mathcal{E} \approx$ 1 - 7 $\times$ 10^7 V/m).[78]. Collectively, the data suggests that the linear $Ln(I/\mathcal{E})$ *versus* $\mathcal{E}^{1/2}$ (Figure 3.5c) is a consequence of Schottky emission, rather than PF emission in these systems. In summary, transport through Au@CdSe@PEDOT:PSS devices, across a wide range of w_{CdSe} and E_{app}, conforms to the predictions of Schottky emission at back-to-back Schottky junctions.[91, 88, 14, 87]

3.3.3 EL Emission Intensity and EQE

EL emission from Au@CdSe@PEDOT:PSS wires. A false color photomicrograph of a Au@CdSe@PEDOT:PSS wire (Figure 3.6a) shows the CdSe and PEDOT:PSS-coated gold

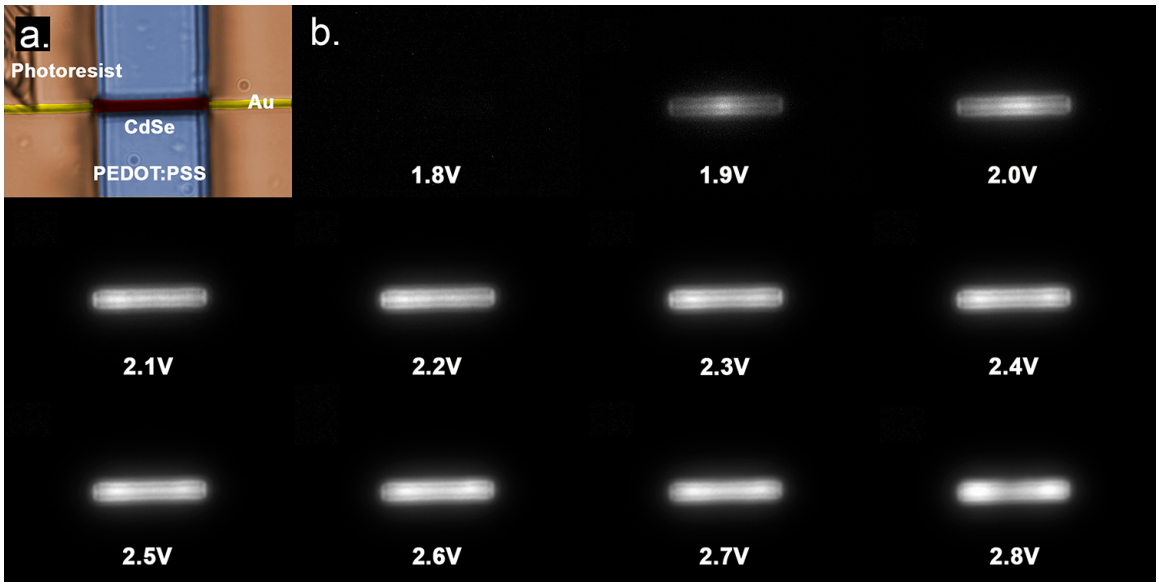

Figure 3.6: EL emission for Au@CdSe@PEDOT:PSS wires: a) False color photomicrograph of a Au@CdSe@PEDOT:PSS wire showing PR-covered gold nanowire on each side (yellow), and a 25 μm emitter region covered with CdSe (magenta) and PEDOT:PSS (blue). b) EL emission maps for a w_{CdSe} = 1064 nm as a function of E_{app} from 1.8 V to 2.8 V. The uniformity of the EL emission intensity along the wire is notable.

nanowire as a 25 μm wide dark band against the light blue PEDOT-PSS layer, with uncoated gold nanowire on both sides, protected by photoresist. A copper electrode (not shown), is used to make contact to the PEDOT-PSS layer. The device shown here has the thickest CdSe shell, w_{CdSe} = 1064 nm. The application of a forward bias at the PEDOT:PSS - Au contacts induces EL emission from regions of the wire having all three layers: Au, CdSe, and PEDOT:PSS. Photomicrographs of the device acquired in the dark (Figure 3.6b) show a voltage threshold for EL, E_{th} = +1.8 V and an increase in EL intensity with E_{app} up to +2.8 V. Light at 1.8 V can not be seen here due to the low light intensity and the contrast settings. Although it is not visible in this figure, for devices with w_{CdSe} = 1064 nm, an onset for EL is actually detected at E_{th} = +1.7 eV, averaged over several devices. E_{th} is also inversely correlated with w_{CdSe} (Figure 3.7a, inset) so thinner shells produce even lower E_{th} values, down to +1.45 V for w_{CdSe} = 350 nm. Relative to other CdSe-based EL emission systems (Table 1.1), this E_{th} value is amongst the lowest.

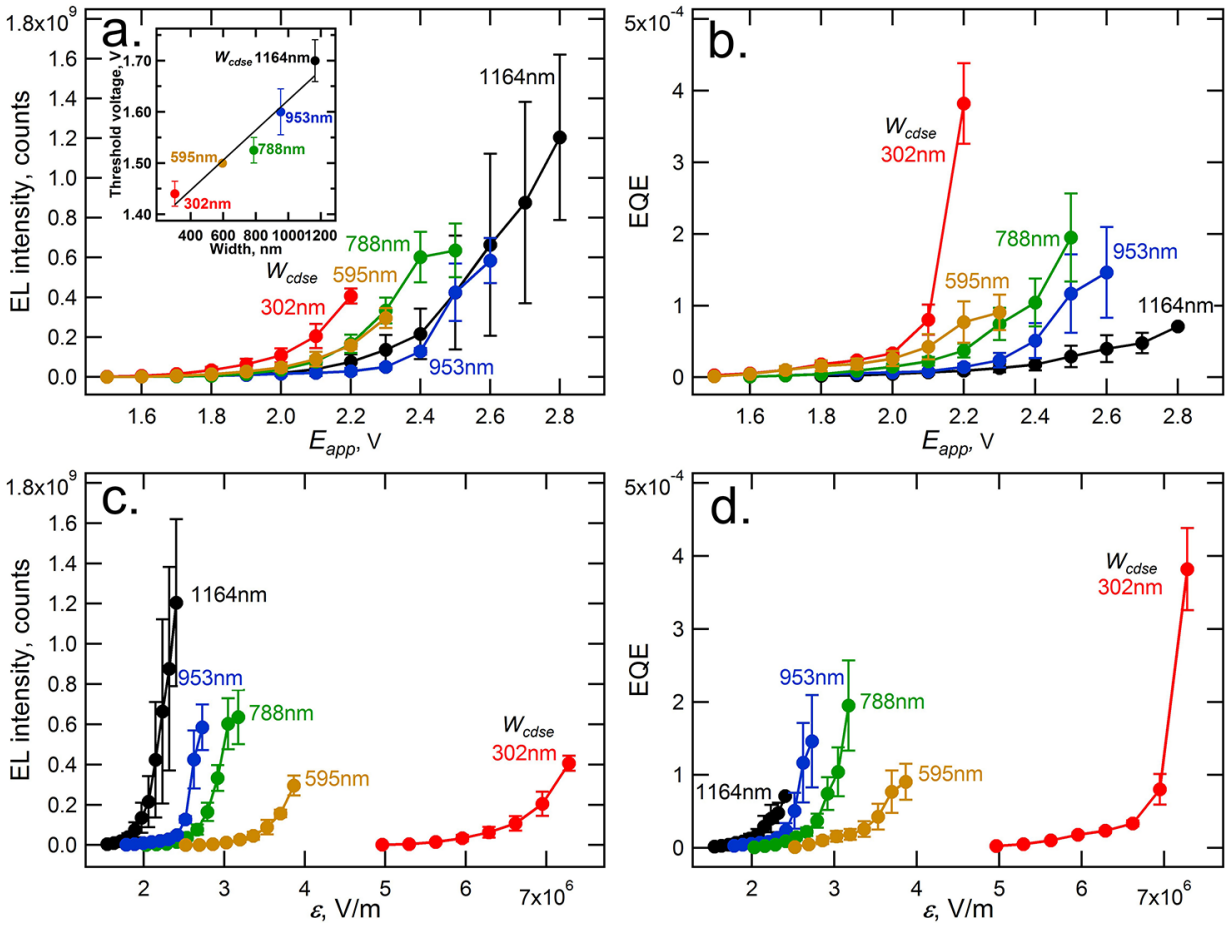

Figure 3.7: a,b). *EL* intensity (a) and external quantum efficiency (EQE) (b) *versus* E_{app} for devices with w_{CdSe} varying from 302 nm to 1064 nm.*versus* E_{app} for GCPs with w_{CdSe} varying from 302 nm to 1064 nm. The inset in (a) is a plot of the threshold voltage, V_{th}, *versus* w_{CdSe}. Here, V_{th} is estimated as the lowest voltage at which *EL* emission is observed above background. c,d). *EL* intensity (c) and EQE (d) *versus* electrical field strength, ϵ, for Au@CdSe@PEDOT:PSS wires with w_{CdSe} varying from 302 nm to 1064 nm.

For CdSe-based EL emission systems, E_{th} values below 2.0 V are unusual, and in all prior cases of which we are aware such low E_{th} values require channel lengths below 200 nm (Table 1.1). For example, gold nanogaps that are 100-200 nm in width and filled with electrodeposited CdSe are characterized by V_{th} = 1.5 - 1.9 V.[100] Planar M-S-M junctions containing electrodeposited CdSe show V_{th} = 2.0 V for a CdSe thickness of just 100 nm, but larger values up to 7.0 V for thicker CdSe layers of 450 nm.[78] Electrode spacings of just 30 nm were associated with a V_{th} = 1.7 V.[33] Relative to the other CdSe-based EL device architectures we have studied,[100, 78, 74, 3] two unique characteristics of the current device is the use of a conformal PEDOT:PSS hole injecting layer and the expansion of the interface area of the PEDOT:PSS with the CdSe emitter layer. Either or both of these factors would be contributing to lower E_{th}.

As already noted above, transport in Au@CdSe@PEDOT:PSS wires can be accounted for by majority electrons alone, but EL requires holes. These holes are commonly injected at the positive contact - PEDOT-PSS in this case - and radiative recombination with electrons produces EL which is localized within one hole diffusion length, L_p, from this contact. In polycrystalline II-VI films, typical value for L_p are in the 400-600 nm range.[73, 60] The EL intensity is typically minority carrier limited, and this provides an explanation for increasing EL intensity with both E_{app} and current (Figures 3.7a and 3.7b).

Although we are not able to resolve the location of light emission within the CdSe layer in our optical images, the positive correlation with w_{CdSe} (Figure 3.7a) is evidence that it originates from a layer of thickness L_p from the PEDOT:PSS contact. This is because the volume of EL-producing CdSe and the emitting area of the device both increase with the radius of the CdSe shell in this case. If, on the other hand, EL originates in a layer localized at the Au-CdSe contact, the volume and area of emission will be constant and the *opposite* dependance on w_{CdSe} should be observed as a thicker CdSe shell self-absorbs the emitted EL. However, this case would not be expected based upon the (-) bias applied to the gold

contact in our experiments.

The maximum external quantum efficiency (EQE) of Au@CdSe@PEDOT:PSS wires increases with E_{app} and is in the range from (0.70 - 3.8) $\times$ 10^{-4} (Figure 5d). The correlation of EQE with E_{app} has been frequently observed and is attributed to the filling of trap states which mediate nonradiative recombination under high injection conditions.[5, 102, 35] Less obvious is the reason for EQE to be *inversely* correlated with w_{CdSe} (Figure 5d), on average, when EL intensity is directly correlated with w_{CdSe} (Figure 5c). Enhanced EL could be related to $\mathcal{E}$ if PF emission were operating (we have already concluded above that it is not) - and thin CdSe shells would exhibit higher efficiency in this case - but neither EQE nor EL intensity are well correlated with $\mathcal{E}$ across all five w_{CdSe} values (Figure 5e,f). Self-absorption of emitted EL by the CdSe shell provides one rational higher EQE with decreasing w_{CdSe}.[91]

Time dependent EL emission from Au@CdSe@PEDOT:PSS wires. One interesting phenomenon we observed is the time dependent behavivor of EL at high E_{app}. As Figure 3.8g shows, current increases from an initial value and stabilize over a rather long time in the range of tens of seconds when a relative high potential is applied. This behavior leads the EL intensity as well as EQE to increase over time (Figure 3.8a - f), and the EL intensity increases faster than the current (Figure 3.8g, h). For the current increase, one possible explanation is the Joule heating. You *et al.*[108, 28, 36, 61] studied the current-induced joule heating on nanowires and the temperature shows similar behavior. Heat generated from Joule heating will increase the temperature of the nanowire, and the heat dissipated though the substrate and air reaches an equilibrium with the generated heat. Then the temperature of the nanowire will stabilize. As temperature increases, the current will increase as well, so as the EL intensity and EQE.[102, 35, 5] This behavior is consistent with the previous voltage dependent EL: both EL and EQE behaviors could be attributed to the temperature effect. However, we do see "efficiency droop" with longer turn-on time or higher temperature here. One possible reason is the device was operating at relative high voltage and high current

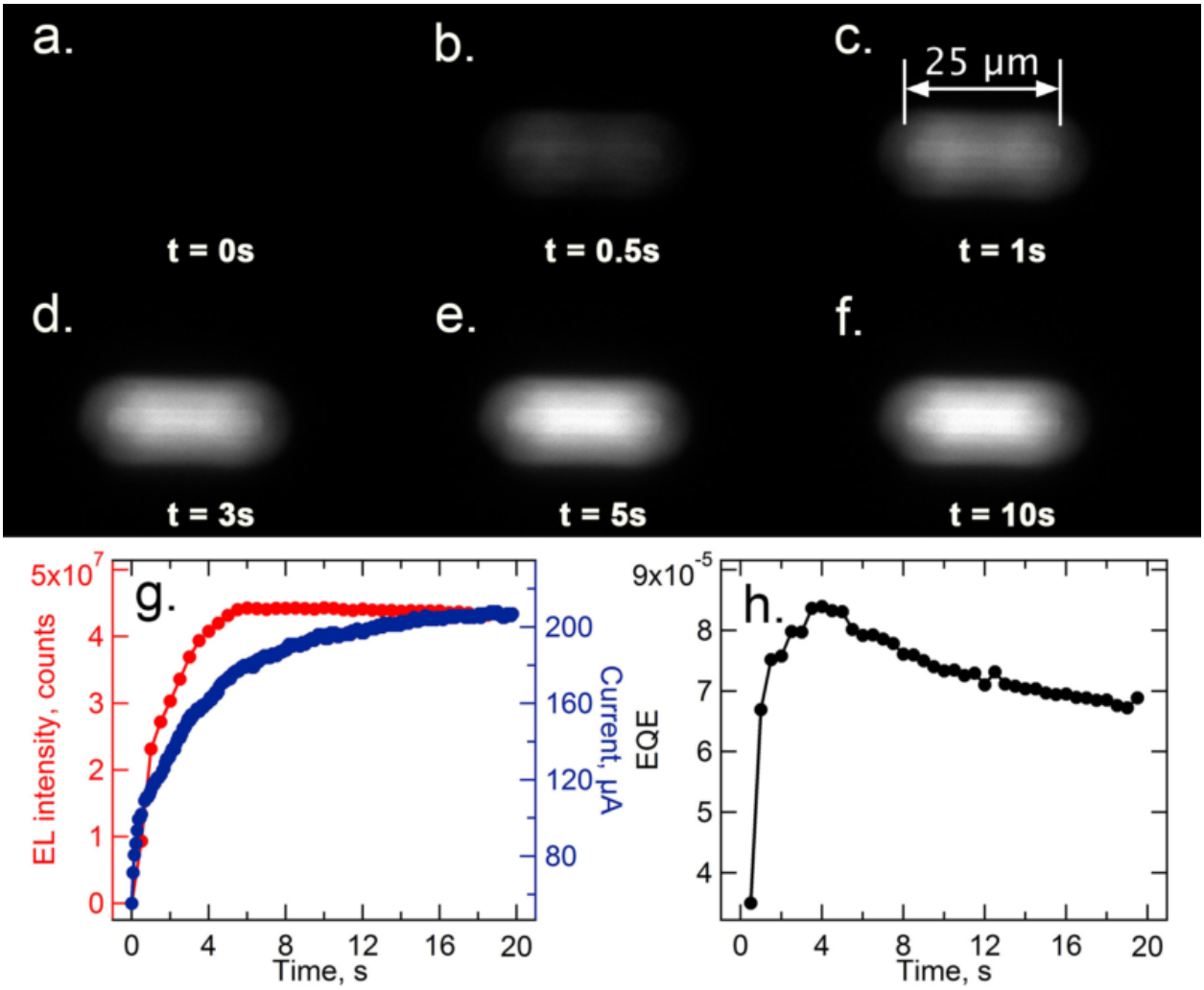

Figure 3.8: "Turn-on" of a Au@CdSe@PEDOT:PSS wire. a-f) Photomicrographs of EL emission from a device with w_{CdSe} = 1164 nm at E_{app} = 3.1V. g) Plot of EL emission intensity (red) and current (blue) *versus* time. The EL intensity increases for 5 - 10 s prior to stabilizing. h) Plot of EQE *versus* time for the same data plotted in (g).

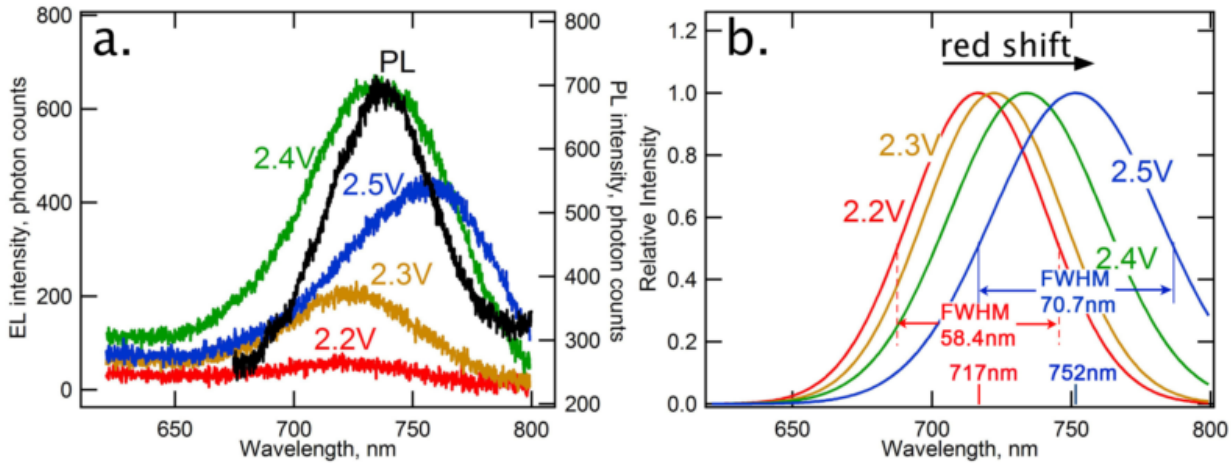

Figure 3.9: EL spectra for a Au@CdSe@PEDOT:PSS wire. a) Raw EL spectra as a function of E_{app} for a Au@CdSe@PEDOT:PSS wire having $w_{CdSe} = 788$ nm. The PL spectrum was acquired for this device with excitation at $\lambda_{ex} = 532$ nm. b). Normalized and Gaussian-fitted EL spectra showing red-shifted emission maxima as well as spectral broadening with increased E_{app}.

region and heat generated from Joule heating could damage the device and also lead to high leakage current. [16]

3.3.4 EL and PL Spectra

***EL* spectra**. A comparison of photoluminescence (PL) and EL spectra as a function of E_{app} (Figure 3.9a) shows that EL spectra are somewhat broader spectrally for all E_{app}, and a slight increase in spectral width is seen with increasing E_{app}, visible most clearly in the Gaussian fits of Figure 3.9b. These EL spectra are far narrowed than those for planar Au-CdSe-Au junctions prepared by electrodeposition,[78] where Poole-Frenkel emission was implicated in the transport process. For those devices, EL spectra showed a FWHM approaching 500 nm at E_{app} of 8.5 V and 300 nm at 4.5 V[78] whereas in the Au@CdSe@PEDOT:PSS device FWHM are in the 58 - 70 nm range for 2.2 V $< E_{app} <$ 2.5 V (Figure 3.9b). In our prior work, these broad emission envelopes were attributed, in part, to recombination of trapped holes (electrons) with electrons (holes) within the bandgap.[78] With PF emission

acting as a major contributor to current transportation, higher electric fields will activate more recombination centers at different energy levels. In the present case, current transport is dominated instead by back-to-back Schottky emission leading to the expectation that band edge emission produced by injected holes and at the (+) contact would be the main radiative recombination mechanism, providing for narrower spectra centered at the CdSe bandgap.[31, 30]

In addition to broadening, peak EL intensities also red-shift with increasing E_{app} (Figure 3.9b). The current also increases with E_{app} and can be expected to drive Joule heating of the device to some extent, thereby decrease in the bandgap in accordance with Varshini's law. [96, 2, 5, 81, 102, 98, 35]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T} \tag{3.4}$$

where $E_g(0)$ is the band gap at 0K, α is the $T \to \infty$ limiting value of the band gap shrinkage coefficient $dE_g(T)/dT$ and β is a material specific parameter. This heating-induced contraction of the bandgap, caused by a thermally induced increase in the interatomic spacing, has been previously documented for CdSe.[33, 103, 10]

EL images as a function of applied bias were acquired using an inverted microscope (Olympus, IX71) equipped with a 40× objective lens (Olympus, LUCPlanFLN 40 × 0.60) and a CMOS camera (Andor, Neo). Electrical measurements during EL emission were accomplished using a source-meter (Keithley 2400) controlled by LabVIEW software. EQE was calculated using the number of photons out of the single nanowire light emitter devided by the number of electrons flowing through the material per second. CMOS sensitivity and geometry loss was factored into calculation. EL spectra were obtained using a spectrometer

(Andor, Shamrock SR-500i-D2) equipped with a 300 l/mm grating blazed at 760nm and a CCD camera (Andor, Newton). All the EL measurements were carried out under room temperature. PLspectra were acquired using a SpectraPro 2300i spectrometer (Princeton Instruments, Acton) with excitation from a 532 nm laser.

3.4 Conclusion

In summary, we have described a new, high throughput process for preparing three-layer - M_1-S-M_2 - electroluminescent wires. This process involves two electrodeposition steps and a solution casting step ($EECS$). A distinguishing feature of $EECS$ is its ability to produce long EL-emitting wires, limited only by the length of the gold nanowire core which is prepared using the LPNE process. We demonstrate $EECS$ here by fabricating Au@CdSe@PEDOT:PSS wires 25 μm in length - a record for wire-based EL-emitting devices. Using the $EECS$ process, millimeter-scale EL emitting Au@CdSe@PEDOT:PSS wires should be accessible using exactly the same processing conditions described here. In Au@CdSe@PEDOT:PSS wires, the efficiency of EL emission is signnificantly improved, by an order of magnitude in EQE, relative to planar Au-CdSe-Au emitters described just two years ago.[78] But further improvements are needed to bring EQE to 1.0 % enabling brightness that competes with state-of-the-art quantum dot-based EL devices.

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