Lawrence Berkeley National Laboratory
Recent Work

Title
SIGNAL PROCESSING FOR AN OPTICAL WIDE BAND DATA TRANSMISSION SYSTEM

Permalink
https://escholarship.org/uc/item/7284k6p1

Authors
Nakamura, M.
Leskovar, B.
Turko, B.T.

Publication Date
1987-07-01

eScholarship.org Powered by the California Digital Library
University of California

LBL-23817

Lawrence Berkeley Laboratory
UNIVERSITY OF CALIFORNIA

Engineering Division

RECEIVED
LAWRENCE
BERKELEY LABORATORY
JAN 8 1988
LIBRARY AND
DOCUMENTS SECTION

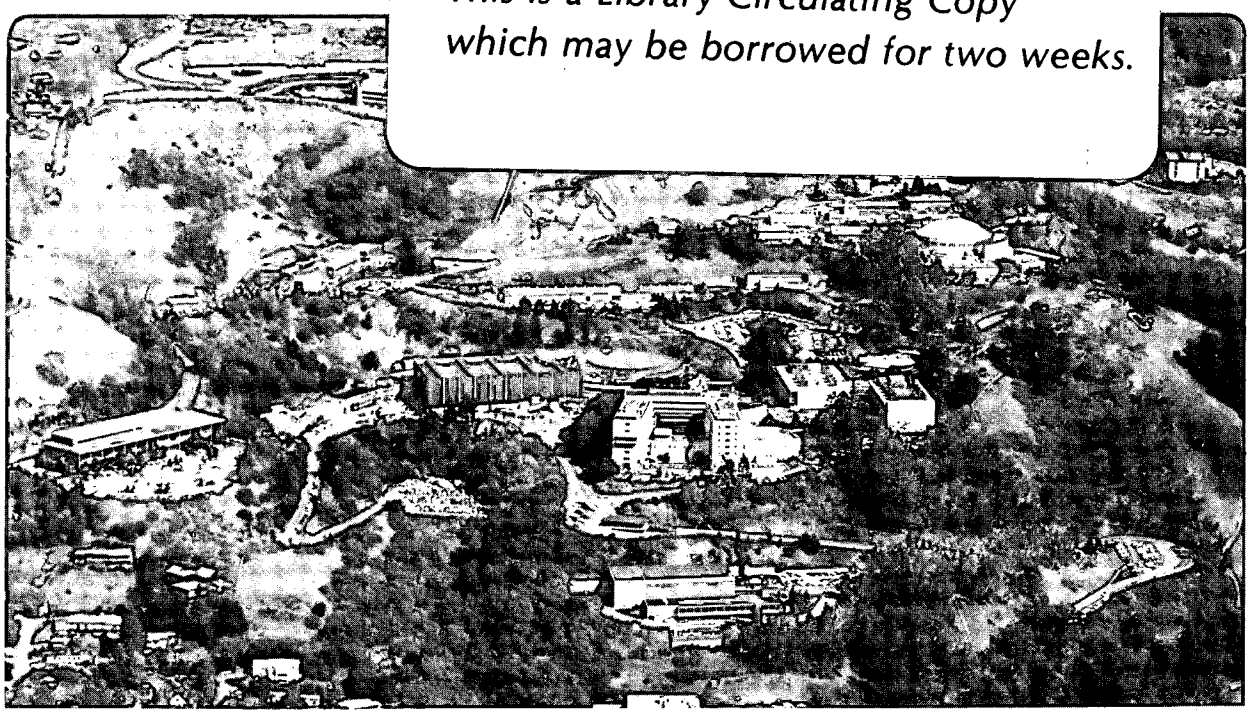
Presented at the 1987 Nuclear Science Symposium, San Francisco, CA, October 21–23, 1987, and to be published in the Proceedings

Signal Processing for an Optical Wide Band Data Transmission System

M. Nakamura, B. Leskovar, and B.T. Turko

July 1987

TWO-WEEK LOAN COPY
This is a Library Circulating Copy
which may be borrowed for two weeks.



Prepared for the U.S. Department of Energy under Contract DE-AC03-76SF00098

LBL-23817

DISCLAIMER

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.

SIGNAL PROCESSING FOR AN OPTICAL WIDE BAND DATA TRANSMISSION SYSTEM

M. Nakamura, B. Leskovar and B.T. Turko
Lawrence Berkeley Laboratory
University of California
Berkeley, California 94720 U.S.A.

ABSTRACT

The signal processing for an optical wide band transmission system using gallium arsenide (GaAs) digital integrated circuits and optical fibers has been investigated. Multiplexing, coding, synchronization, demultiplexing, and error checking at 780 Mbit/s data rates are described. Data storage in memory for linking to a computer is also considered. The design uses available GaAs and silicon components. The reliability of GaAs components is discussed as well as the layout and thermal considerations required for a high speed system.

INTRODUCTION

Systems for local communication such as computer interconnections, rf distributions in phased array radars and instrumentation for basic and applied research require a high data rate processing capability. In particular, high spatial resolution charge-coupled device (CCD) image sensors and image intensifiers, with frame rates of 500 frames/s or higher require extremely high data rate transfer and processing capability.

The use of fiber optic cables and gallium arsenide (GaAs) digital integrated circuits (IC's) presents a solution to achieving these high data rates. Such a system for ultra high data rate capability has recently been investigated [1,2]. The system discussed here will have the capability of taking information from a high frame rate, high resolution image sensor based on a charge coupled device (CCD) and transmitting data from each frame over tens-of-kilometer long fiber optic cables within a few milliseconds. The image sensor will be comprised of a CCD array of 12 blocks, each block size being 86 x 256 pixels. This is equivalent to having 12 individual cameras with a CCD array of 86 x 256 and recombining them into one to obtain a nominal 512 x 512 array. Each block will be handled individually, although the blocks will have common clock drivers.

SYSTEM DESCRIPTION

A simplified diagram of the system is shown in Fig. 1. After an image is temporarily stored in the CCD image sensor, the analog information in the image sensor is read out at a 15 MHz rate and digitized by flash analog-to-digital converters (ADC's) with 12 bit resolution. Pixel by pixel information from all 12 blocks of the CCD image sensor are read out simultaneously and digitized by twelve ADC's after which an odd parity bit is added to each digitized word. By time division multiplexing four blocks of the CCD image sensor onto one fiber optic data transmission cable and using a total of three fiber optic lines, the multiplexed data of all twelve blocks can be transmitted at a data rate of 780 Mbit/s (15 MHz x 13 bits x 4). This is a data rate within present day fiber optics technological capability and GaAs digital IC speeds. The data transfer time for each frame is a few milliseconds.

Laser diode transmitters will send the data over fiber optic cables to receivers designed for low noise performance. Clock recovery and phase-locked loop circuits will synchronize the receiver clock with the incoming data. Demultiplexing of the data is done by converting the bits in the serial stream of data into parallel form, in order to reduce the rates of handling the data from 780 MHz to 15 MHz. At 15 MHz, complementary metal oxide semiconductor (CMOS) memory chips can easily handle the data storage rate. Their low current requirements provide the added advantage that a backup battery could be used for retention of data in the data storage system. The information in the data storage will subsequently be transferred to a computer. Row synchronization, parity checks and other error checking schemes will be employed to achieve the best possible data recovery at the receiver.

Figure 2 shows the serial data format used to transmit data over the fiber optic cables. Row synchronization word (RSW) along with two Dummy Words, all with even parity, are sent at the beginning of each row (or line) of the image sensor block. RSW is made up of two redundant words with a selected bit pattern designed to be uniquely identifiable as the beginning of a row. Since real data will be sent using odd parity and RSW using even parity, the probability of two consecutive real data words matching RSW should be next to nil when receiving and synchronizing data for data storage. RSW and Dummy Words occupy the space of four data words to be compatible with the 4 blocks-to-one fiber cable format chosen for this system. This makes the demultiplexing of data simpler because all data and RSW formats will be comprised of 4 data-word groups.

Transmission of data using a non-return to zero (NRZ) digital coding format is proposed because bandwidth requirements are effectively one-half that of a return to zero (RZ) pulse code format. This is helpful in maintaining the best possible bit error rate (BER). Other pulse code formats such as bi-phase, amplitude modulation, frequency modulation and phase modulation have been rejected as being more complex or requiring more bandwidth than NRZ. At present, most performance characterizations for high speed optical communication components and systems are normalized to NRZ code standards. Descriptions of transmission and reception of data will be made on the basis of NRZ techniques.

DIGITIZATION, MULTIPLEXING AND CODING OF DATA

Figure 3 shows in more detail how it is proposed to digitize the analog signals from the CCD's, add parity, temporarily store data in a buffer register, transfer data into a shift register, read out in bit serial fashion and send the data to the laser transmitter. Since gallium arsenide (GaAs) devices are capable of handling data at greater than 1 Gbit/s speeds, GaAs technology will be used in the gates along with the other devices within the blocks identified as GaAs. All other devices in the figure will use silicon bipolar technology, namely emitter

coupled logic (ECL). Row sync word (RSW) and Dummy Words are introduced separately at the appropriate time. Details in the figure are shown for four blocks multiplexed onto one fiber optic cable, and the transmission of all twelve blocks would be accomplished by triplicating the described system.

CAV 1220, a flash ADC produced by Analog Devices, is a 12 bit, 20 MHz ADC which meets our requirements for an analog to digital converter. The system timing requirements are fitted to the ADC's timing functions required by the multiplexing scheme. Timing waveforms for controlling the ADC's and shift registers are shown in Fig. 4. The first line of the figure is the encode command which is applied to the CAV 1220 at a 15 MHz rate. Due to pipelining within the ADC, DATA READY and ADC OUTPUT signals from the CAV 1220 do not occur until several encode commands have been issued. Although the DATA READY signal is available from the ADC, this function is ignored in our system. During the pipelining operation, a shift register is parallel loaded with the RSW and Dummy Words for bit serial transmission, and thus with the appropriate delay, the timing can be made to mesh with ADC OUTPUT. Clock A (CLK A) shifts the RSW and dummy words to the RE-SYNC flip flop (FF) which re-synchronizes all data via reclock (RECLK) in NRZ format before the digital information is presented to the laser transmitter.

The fourth line in Fig. 4 shows the time at which the data from the ADC's are transferred to the Buffer Registers I, II, III and IV. In a manner similar to that described for RSW and Dummy Words, clock B (CLK B) and clock C (CLK C) load and shift data to the RE-SYNC FF for re-synchronization. Details for a single encode cycle of this operation are shown in Fig. 5. Gates I, II, III and IV are generated at the times shown and the PAR/SER controls for B and C are also indicated. The PAR/SER controls invoke a parallel (PAR) command when the shift registers are loaded and a serial (SER) command when data are being shifted out in a bit serial fashion.

IDLE DATA are transmitted before useful data are sent to allow the receiver circuits to obtain bit patterns with sufficient transitions so that the clock recovery circuit and phase-locked loop can synchronize. The receiver clock will therefore already be re-synchronized to the transmission clock rate when the CCD image sensor data arrive. The IDLE DATA signal will be a simple one-zero-one-zero pattern generated by the Binary FF located at the right center of the diagram. The IDLE DATA are sent any time there is a known gap in the bit serial stream, such as during horizontal or vertical blanking. The 780 MHz reclock (RECLK) is phase-delayed to obtain synchronization with data at the RE-SYNC FF shown in Fig. 3.

In Figure 6 details of the controls and timing are shown. The Master Clock operates at 780 MHz from which all other timing is derived. The IDLE control and the Q-not output from the flip flop near the center of the diagram combine to generate the "D" signal which gates the IDLE DATA to the RE-SYNC FF (see Fig. 3). The Enable Readout and Start Readout combine and are inserted onto the D inputs of the first of the two Synchronizing FF's which changes the state of the first flip flop at the next clock input, which in turn will cause the second flip flop to change 180 degrees later in the Master Clock phase. The Q signal from the second Synchronizing FF is inserted at several gates which produce the following results: 1) the "A" signal is activated and 2) the Master Clock signal is allowed through its gate (see left center of the diagram).

A Divide-by-52 counter produces a 15 MHz clock from the 780 MHz Master Clock. The CCD camera and the ADC's receive these 15 MHz clock pulses needed for their operation, but this signal must be gated so that the CCD camera and ADC's do not operate during the time that the RSW and Dummy Words are being transmitted. Meanwhile, a Divide-By-N counter produces a delay that matches the end of the transmission of the RSW and Dummy Words to the delay caused by the pipelining in the ADC's as is shown in Fig. 4. The end of this delay period simultaneously turns off the "D" signal and turns on the Gated 780 MHz CLK which is the source for CLK A, CLK B and CLK C.

All of the flip flop controls in the upper right corner of the diagram are in the state which allows the CLK A signal to be generated first. Another Divide-By-52 counter measures out exactly 52 CLK A pulses after which time the flip flop switches from A-CLK to B/C-CLK pulses. At this same time the gates at the upper left corner of the diagram switch from "A" to "B" or "C". "B" or "C" is determined by another flip flop which controls the B1 and C1 outputs. This flip flop is first set to allow the CLK B signal to be generated, and after 13 pulses the flip flop changes to allow the CLK C signal to be generated, and etc.

To backtrack a bit at this time, ADC OUTPUT from the ADC's has in the meantime become available. After an appropriate delay, a pulse shaping network (PSN) produces a pulse that is delayed by four additional delay circuits (DELAY1, DELAY2, DELAY3 and DELAY4) which in turn generate the Gate and Load signals as shown on the diagram and at the times shown in Fig. 5.

Meanwhile, at the upper center of the diagram, a Divide-by-256 counter is counting the 15 MHz clock pulses to keep track of 256 pixels that constitute a row of the CCD image sensor array. After a row has been read out, the RSW and Dummy Words are again sent via CLK A. The whole procedure described above is repeated again and again until the Divide-by-86 counter at the center of the diagram has counted the 86 rows of the 86 x 256 array and halts the readout process.

The reclock (RECLK) signal serves to transmit the data with a constant phase relationship with the highly stable transmitter clock for all data. Variations in transit times on the printed circuit board can easily cause phase shifts for the different data, which, if transmitted without reclocking, would be detrimental to the operation of the receiver clock synchronization. A constant phase of the data to the transmitter clock is essential in maintaining the receiver clock synchronization because the phase information of the data is used by the phase-locked loop for synchronizing the receiver clock to the data. By reclocking the D-flip flop with the data as shown, the data are formatted into the NRZ data format code as they are sent to the laser diode for transmission over the fiber optic cables.

Gallium arsenide (GaAs) devices are used where their high speeds are essential and emitter coupled logic (ECL) devices are employed where speeds are non-critical. The choice of technology for the various devices in Figure 3 are indicated in the diagram. Input and output levels for GaAs devices are compatible with ECL so there is no problem in

mixing the two technologies within a system. In Fig. 6 all devices are GaAs IC's.

DATA PROCESSING AND STORAGE

A diagram showing the data processing steps for four blocks is given in Figure 7 and its accompanying timing diagram is shown in Figure 8. The functions shown in Fig. 7 must also be performed in triplicate to accomodate all 12 blocks of the image sensor. Since the diagram is rather detailed even for a simplified diagram, only the highlights of the receiver operation will be discussed.

The clock recovery circuit synchronizes the voltage controlled crystal oscillator (VCXO) to the incoming data with the help of a phase-locked loop which is not shown. Data are continuously clocked into the 52-Bit Shift Register at a 780 Mbit/s rate. The row sync word detector (RSW Detect) signal is activated whenever RSW arrives and alerts the receiving system that the following string of words will contain real data (see Fig. 2). A divide-by-52 counter determines that after 52 bits (13 bits x 4) have been shifted into the shift register, a Load command is issued to the 52-Bit Data Register. This action serves to demultiplex the incoming data stream because the information from the 52-Bit Data Register hereafter can be handled as parallel bits. This reduces the data handling rates from 780 Mbit/s back down to a 15 MHz rate. This also allows the use of CMOS devices for storage which need operate at only 15 MHz and have the added advantage of requiring very little current in the standby condition. This presents the possibility of using a backup battery system for the memory if requirements for a backup should exist.

Parity checks are made on the contents of the 52-Bit Data Register, and the Parity Fail flag is set if parity errors are detected. RSW Fail is flagged if the RSW signal fails to occur within a predetermined time interval. In addition, Row Sync Error is flagged if the 8-Bit counter shows a non-zero count when a new RSW signal is issued because the 8-bit counter must indicate a zero count to correspond to 256 words having been received per row.

The combination of the 8- and 7-Bit Counters provide the Memory address information for data storage synchronization. RSW, Dummy Words and parity bits will not be loaded into memory. Figure 8 shows a skip in the Write Strobe to memory whenever RSW and Dummy Words are to be suppressed from being loaded into memory. A 22016 (86 x 256) Detect signal indicates that all words from the image sensor have arrived.

All devices shown within dashed lines in Fig. 7 are GaAs while those digital circuits outside the dashed lines can be of CMOS or transistor transistor logic (TTL). Because the output device of the GaAs IC is a field effect transistor (FET), it can be wired either as a source follower for ECL logic levels or in a common source mode for TTL logic levels at the discretion of the user. There is, however, an inversion of the digital signal when operating with TTL output levels which might create a minor inconvenience, but the direct compatibility of the GaAs devices to TTL levels eliminates the logic level translator problem.

The memory for data storage will be made of memory chips using CMOS static random access memory (SRAM) technology. The memory will be addressable by our subsystem so that we control the location in which the data is written. A computer will interface with the memory storage which will allow flexibility in reading and writing data.

The memory architecture will be very simple with each memory bank dedicated to a corresponding block of the CCD image sensor. Each bank will have at least 32,768 addressable locations and at least 12 bits per location. With memory mapping techniques the 12 banks of memory can be readily addressed and controlled. Direct memory access (DMA) operation will allow rapid transfer of data from memory to the computer.

AVAILABLE COMPONENTS

The design of the system is based on available components and does not require extraordinary component selection or design. The selection of available GaAs digital IC's and components especially suited to fiber optic data transmission and reception is adequate today, but newer and expanded lines of GaAs IC's are continually being offered. New designs and applications of integrated circuits are offered by more and more companies which will make the design engineer's task much simpler in working with ultra high speed systems. The introduction of newer ready-made transmitters, receivers, transimpedance amplifiers, clock recovery circuits, etc. will also help the design engineer in the design of fiber optic systems.

While gallium arsenide (GaAs) devices are available from a number of sources at the moment, GigaBit Logic [3] has the widest selection of products and can supply all of the necessary components for the signal processing subsystems. Other companies offer a limited selection of components, and still other companies have products for military applications or in-house use only. Unfortunately, not all of the GaAs devices from the various companies are completely compatible with one another as they may use different voltages from power supplies and for thresholds.

LAYOUT AND THERMAL CONSIDERATIONS

Layout considerations are critical for devices and components at these ultra high speeds. Since the rise times and propagation delays of the signals for GaAs devices are in the picosecond region, extreme care must be taken in the layout to minimize poor terminations and non-constant impedances which can cause signal reflections and distortions. Microstrip or stripline techniques must be used. Differential propagation delays on the printed circuit board must be carefully evaluated and dealt with since, for example, the setup and hold times for a parallel load into a shift register depend on the data and clock maintaining critical timing relationships with one another.

It is generally agreed that packaging and board layout are of utmost importance in the development of high speed digital systems. A general rule of thumb is that the more circuitry you can get into a package, the more reliable the system becomes. This is true for a number of reasons of which the following are applicable to high speed work: 1) lead lengths are kept to their bare minimum. 2) transit times are due mostly to chip devices and not lead lengths. 3) reflections due to non-constant impedance are minimized when transit times in leads are short in comparison to rise times of signals. 4)

transit times of signals getting out of and back into separate components are minimized which is important since they contribute to a large percentage of the total delay.

One nanosecond per 6 inches is a typical transit time for a signal in a trace on a glass epoxy (FR-4) printed circuit (PC) board, so one can see that lead lengths of an inch or so can easily match the propagation delays for GaAs circuits which is typically around 100 ps. Since the dielectric constant of FR-4 is 4.6, other materials might be considered for use in PC boards. Teflon and Duroid with dielectric constants of 2.2 to 2.5, and polymide, with a dielectric constant of 3.8 are far better suited for very high speed logic. A multi-layer board construction might be considered for transmission of signals as well as for heat dissipation considerations.

Key strategies for keeping line lengths short include the use of very thin lines and multiple routing layers, avoiding vias (through board conductors) and using components that do not require through-hole mounting. This suggests the use of surface mount technology (SMT) and the use of improved packages such as leadless chip carriers (LCC's) and surface mount devices (SMD). Even hybridization of circuits cannot be completely eliminated from consideration. Inter-board connections present an altogether separate problem which will not be discussed here.

Terminations at packages will have to be made with chip resistors, and even then, good terminations without reflections cannot be guaranteed due to the fact that the additional lead lengths within the package may be unterminated. Some device manufacturers are considering putting termination resistors directly into the chips themselves, but this leads to higher heat dissipation within the package. Likewise, chip capacitors must be used for bypassing power supplies, threshold levels, etc., but in some instances, the chip manufacturers have low valued capacitors placed within the package to minimize lead lengths.

Thermal problems arise when using GaAs devices because the board level packing density of GaAs IC's is typically higher than for its silicon counterparts to preserve shortest propagation delays. Thermal characteristics of GaAs integrated IC's are like that of silicon bipolar ECL IC's although the thermal conductivity of GaAs is low (approximately 1/3 to 1/5 that of silicon). Despite these differences, the thermal management techniques for GaAs IC's are very similar to those required for surface mount silicon bipolar devices.

The use of heat sinking is strongly recommended for GaAs devices that dissipate more than 1 watt. In general, most GaAs IC's will require heat sinking and forced air in high density system environments. In many cases, a small heat sink and 600 linear feet per min (lfpm) air flow will be sufficient. In low density prototyping environments, a heat sink alone may be adequate. It is recommended that junction temperatures of commercial products be maintained at or below 120 degrees C so that mean time to failures (MTTF) of several million hours can be realized. Although gas or liquid cooling techniques can be applied, the printed circuit (PC) board itself could be designed to carry away the heat using multilayer boards. Packages designed to allow heat transfer from the bottom of the package could transfer the heat using vias (through board conductors) onto a solid metal core in the PC board.

RELIABILITY CONSIDERATIONS

The reliability of GaAs devices is briefly reviewed here. Table 1 has been taken from another report [4] and reproduced with permission [5]. The properties of silicon and GaAs are compared, and the advantages of GaAs over silicon are indicated. As the table indicates, the electron mobility of GaAs transistor channels is much higher than in correspondingly doped silicon device channels, and these mobilities are realized at lower applied electric fields. Because GaAs is a semi-insulating material (not semi-conducting) the parasitic capacitances (which force silicon IC manufacturers to junction or oxide isolate their transistors to avoid a loss of speed) are greatly reduced.

The lower electric field of GaAs at peak electron velocity results in lower power dissipation for the same or greater speed compared to silicon. From a reliability viewpoint, this results in fewer thermally caused failures and field-induced electromigration. Dielectric failures due to high electric fields are also greatly minimized. Another significant reliability advantage of GaAs over silicon comes from its higher energy bandgap (1.4eV). This permits higher temperature operation and ensures greater radiation tolerance. The semi-insulating substrate also contributes to reliability, due to its freedom from parasitic leakage paths and consequent circuit failures.

Depletion mode-metal-semiconductor field-effect transistor (D-MESFET) technology has certain characteristics which enhance reliability. The MESFET is a bulk current conduction, majority carrier device. The semi-insulating substrate prohibits charge collection and thus provides excellent radiation tolerance. In addition, the absence of gate oxide (non-MOS) prevents the occurrence of threshold shift effects. Also majority carrier devices are more reliable since life time degradation is not a problem. This results in a device structure that is generally free from surface charge effects and failures due to ionic contamination. A gold based metal system with titanium and platinum diffusion barriers provides a high degree of freedom from current and field-induced electromigration [6]. Gold germanium ohmic contacts have been used in GaAs microwave devices for years with proven reliability.

Semiconductor devices are sensitive to radiation, mainly neutrons and gamma rays. Radiation damage mechanisms [7] are displacement, ionization and single event upset (SEU). The gamma ray rate and neutron fluence the device can withstand during and after exposure is also a measure of its radiation resistance. Gamma ray rate is ionizing dose rate in rads/sec and neutron fluence is total number of neutrons incident per square centimeter with 1 MeV equivalent energy. Single event upset is the change in logic state of a digital circuit caused by ionization and critical charge buildup in the path of a single high energy particle.

GaAs IC's are inherently one to two orders of magnitude more resistant to radiation than even the most gamma resistant silicon devices. This is mainly because 'surface inversion' is very difficult, if not impossible, in GaAs. Resistance to gamma rays is a property of GaAs because of short minority carrier lifetime, large activation energy for creating electron-hole pairs, and the fact that GaAs MESFET devices are fabricated on semi-insulating substrates. GaAs is also intrinsically more radi-

ation resistant than silicon due to GaAs's higher band gap (1.4 eV) compared to that of silicon (1.1 eV).

The yield of good GaAs IC die per wafer follows the defect limited pattern seen earlier in silicon IC manufacturing. The yield observed in early GaAs IC manufacturing is noted to be within a factor of 2 to 4 of the yield seen in many present day leading edge silicon ECL manufacturing lines. GaAs yields should improve significantly during the next several years as manufacturing volumes build.

CONCLUSIONS

Signal processing for a 780 Mbit/s optical data transmission system can be successfully accomplished using available GaAs digital IC's. The speeds of GaAs devices are such that the multiplexing, demultiplexing, error checking, clock synchronization, etc. can be done with relative ease at the high data rates chosen. Low power CMOS devices can handle the data storage chores at 15 MHz rates and use backup battery power if the the requirement should arise.

The reliability of GaAs components is very high for thermal, radiation, leakage and electromigration effects. System reliability will be determined by the use of error checking schemes such as parity and row synchronization checks. Good thermal management techniques and layout with constant impedance lines and low differential delay will ensure excellent high speed operation with reliability.

ACKNOWLEDGEMENTS

This work was performed as part of the program of the Electronics Research and Development Group of the Lawrence Berkeley Laboratory and the Diagnostics Development Group of the Lawrence Livermore National Laboratory. The work was supported by the U.S. Department of Energy under Contract Numbers DE-AC03-76SF00098 and W-7405-ENG-48. Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

REFERENCES

1. B. Leskovar, M. Nakamura and B.T. Turko, "Optical Wide Band Data Transmission System," Lawrence Berkeley Laboratory Report, LBL-23113, March 15, 1987.

2. B. Leskovar, M. Nakamura and B.T. Turko, "Wide band Data Transmission System Using Optical Fibers," Lawrence Berkeley Laboratory Report, LBL-23304, April 23, 1987.

3. GigaBit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320-5524.

4. Venkataraman, R. and Schaefer, J., "GaAs IC Reliability and Quality Assurance Handbook," GigaBit Logic Inc., Reliability Report - 1, August 1986.

5. Venkataraman, R., GigaBit Logic Inc., private communication, March 17, 1987.

6. LaCombe, D.J. and Parks, E.L., The Distribution of Electromigration Failures, 24th Annual Proceedings, Reliability Physics, Anaheim, CA, April 1986.

7. Einspruch, N.G., (Editor), VLSI Handbook, Academic Press Inc., Orlando, FL, 1985 (chapter 32).

Table 1. Comparison of GaAs and Silicon ICs

Material	GaAs	Silicon	GaAs Advantage
N-Channel Electron Mobility	4000-5000 cm^2/V-s	800-1,000 cm^2/V-s	5 to 6 X Greater Mobility
Electric Field at Peak Electron Velocity	7 KV/cm	30 KV/cm	Lower Power Dissipation
Saturated Electron Velocity	$2.2X10^7$ cm/s (Peak)	$6.5X10^6$ cm/s	Faster Switching
Wafer Resistivity (Max)	10^9 Ω-cm	10^5-10^6 Ω-cm	Semi-Insulating Substrate
Energy Bandgap	1.4 eV	1.1 eV	Higher Temp. Operation, Reliability and Radiation Tolerance

Performance	GaAs	Bipolar (100K ECL)	GaAs Advantage
Speed-Power Product	0.9 pJ	5 pJ	High Speed - Low Power
Gain-Bandwidth Product	10-15 GHz	5 GHz	Higher Clock Rates
Clock or Data Rates	1-3 GHz (Max.)	150-600 MHz (Max.)	Improved Performance
Output Rise & Fall Times	150-250 ps (Max.)	1 ns (Max.)	Improved Performance
Gate Propagation Delay	75-150 ps (Max.)	300-500 ps (Max.)	Improved Performance

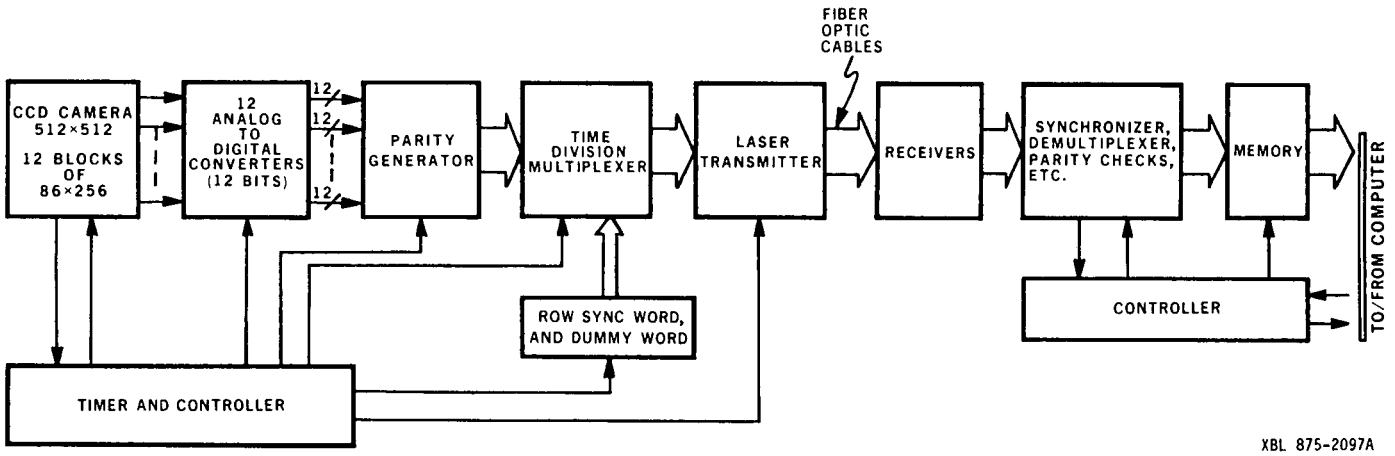
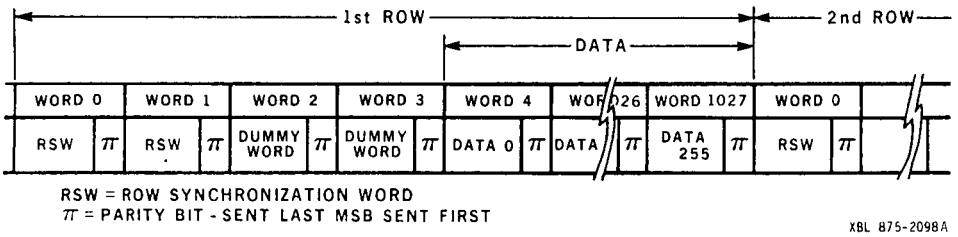


Figure 1. Simplified block diagram for optical wide band data transmission system.

Figure 2. Serial data format.



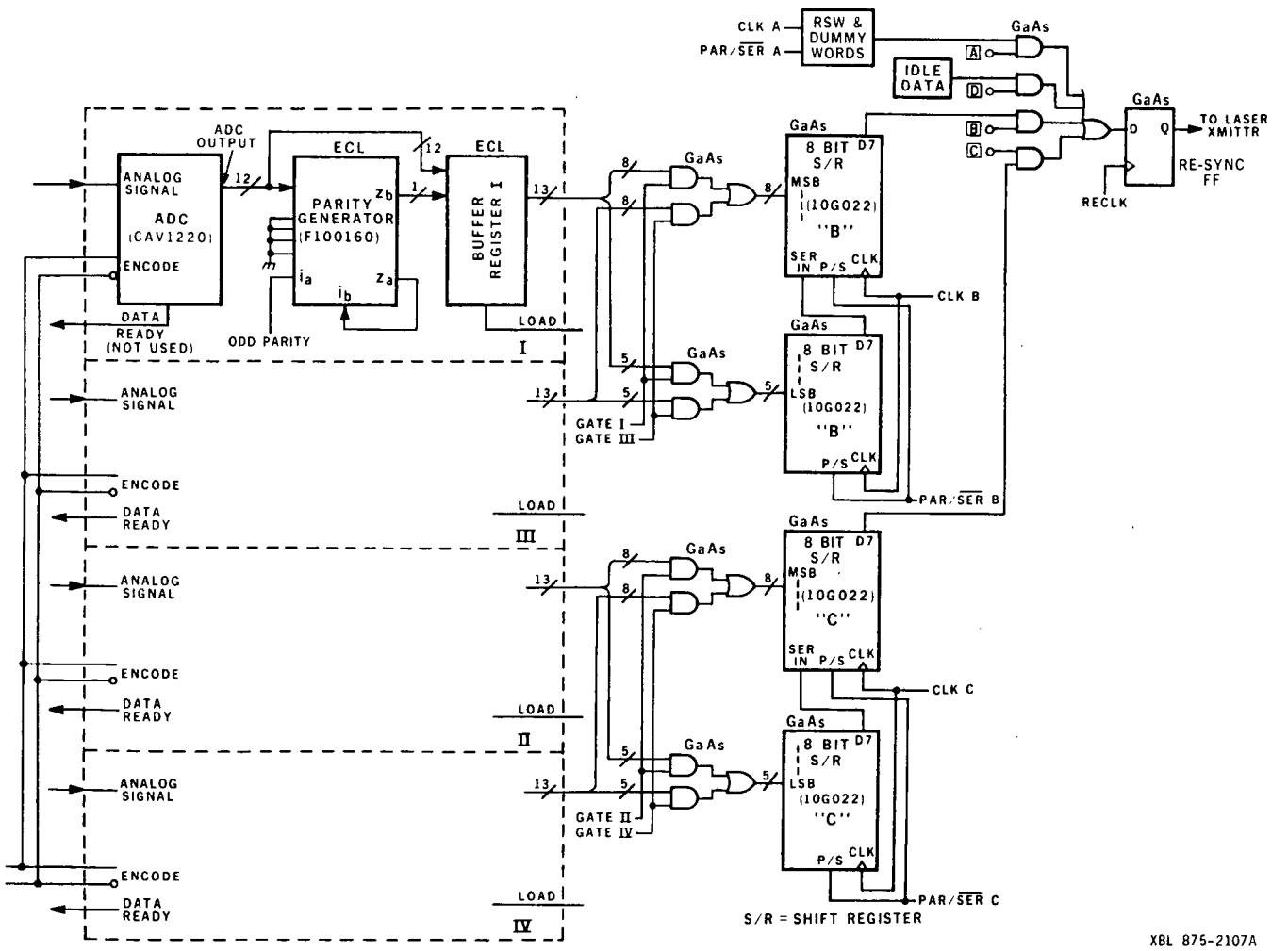


Figure 3. Time division multiplexing scheme - parallel to bit serial conversion.

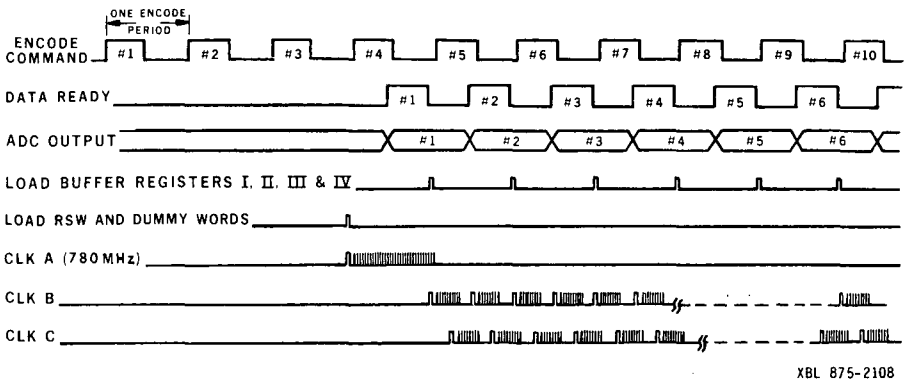


Figure 4. Detailed multiplexing timing diagram.

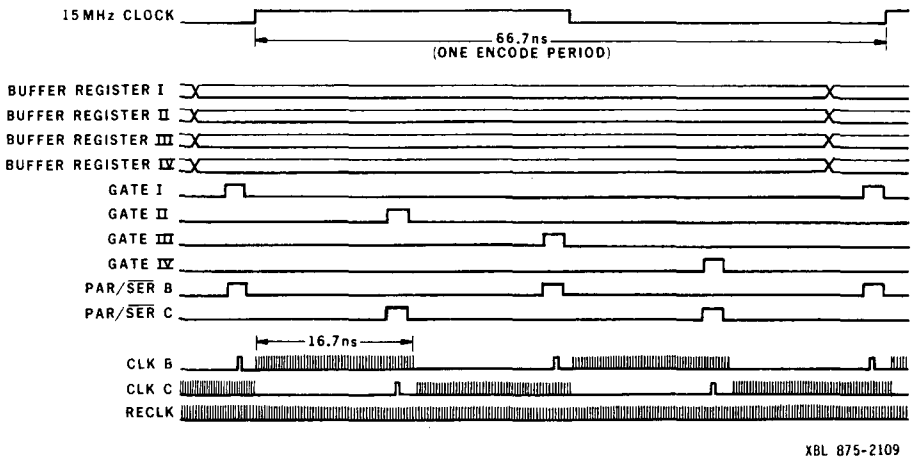


Figure 5. Control and timing diagram for multiplexing and transmitting data.

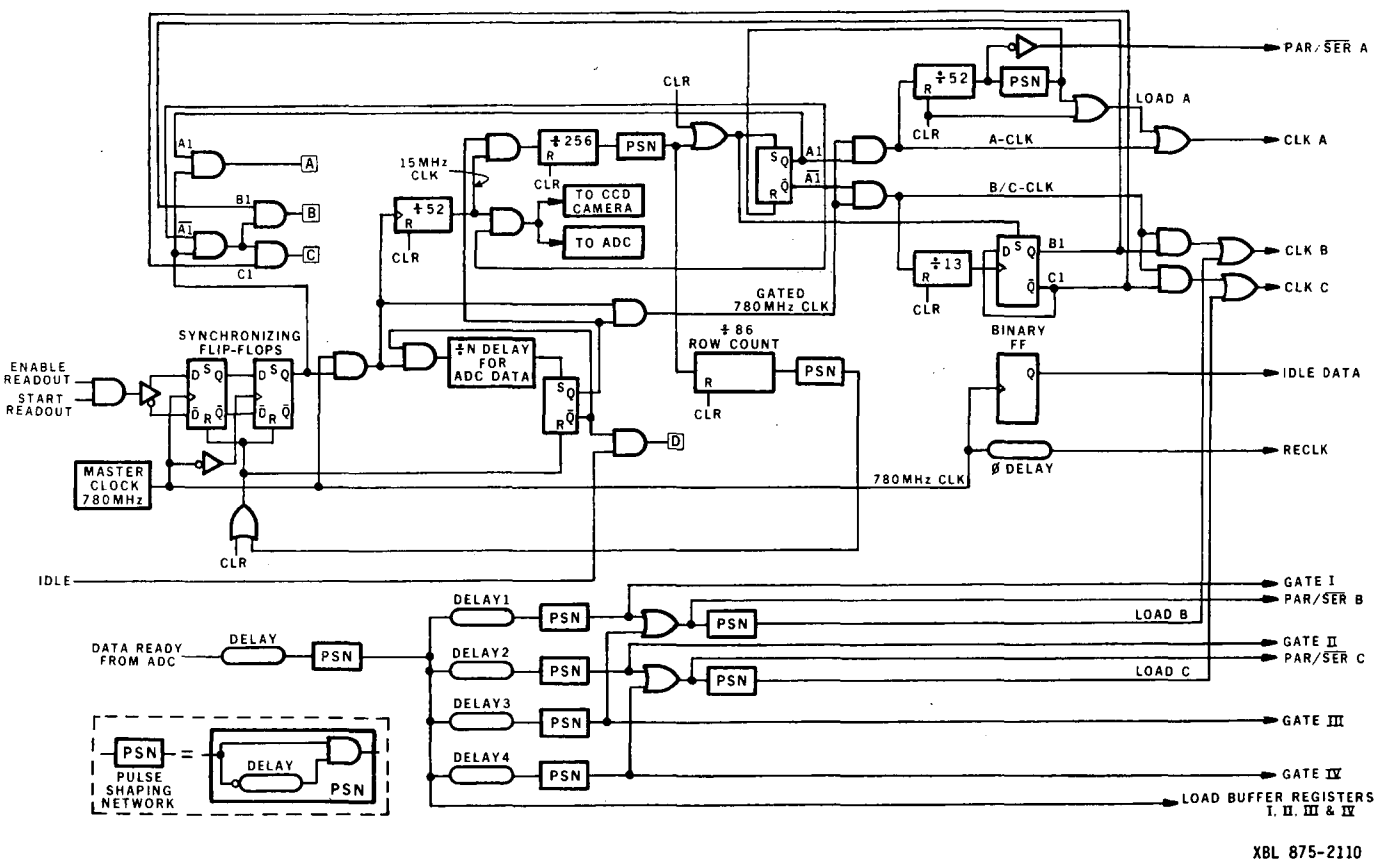


Figure 6. Multiplexing timing diagram.

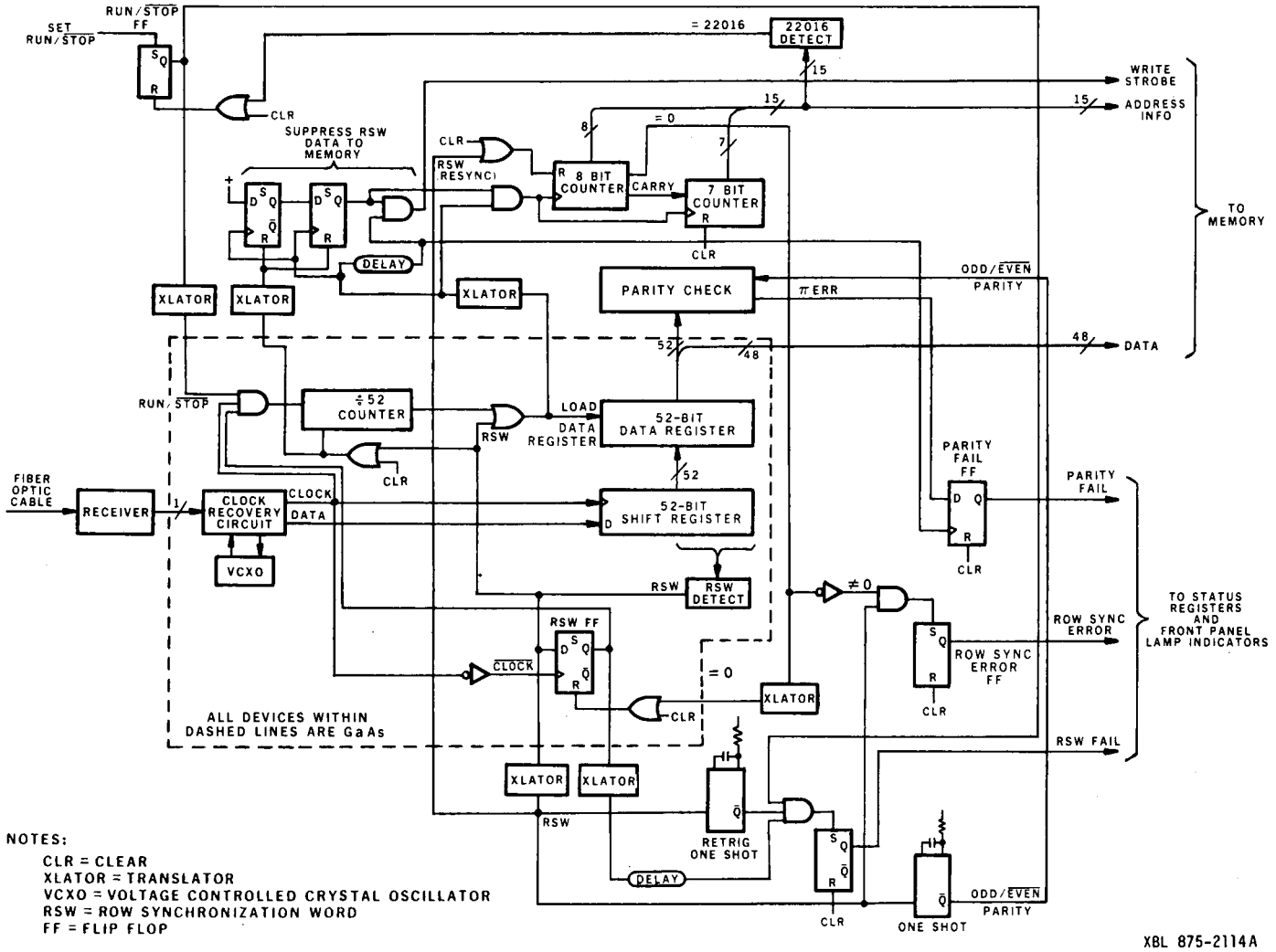


Figure 7. Diagram showing synchronization, demultiplexing, error checking and data preparation for memory.

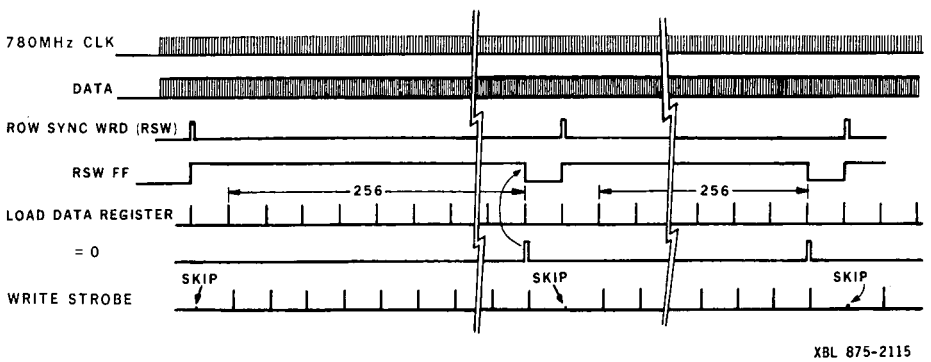


Figure 8. Timing diagram for synchronizing, demultiplexing and data preparation for memory.

LAWRENCE BERKELEY LABORATORY
TECHNICAL INFORMATION DEPARTMENT
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720