Integrated Millimeter-Wave Frequency Synthesizer And Radar Front End Based On Low-Power And Low-Noise Sub-Sampling Phase-Locked Loop

By

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DISSERTATION

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至人無己
神人無功
聖人無名

《莊子》

SE PERFECTI ABSTINENT.
LAVDE IMMORTALES ABSTINENT.
FAMA SANCTI ABSTINENT.

— *CHVANGCIVS*

From ego the perfect abstain;
From credit the immortal abstain;
From fame the holy abstain.

— *Zhuang Zi*

Contents

Abstract

Millimeter-Wave (mmWave) Integrated Circuit (IC) design has become a promising research topic since last decade. Millimeter-Wave signals (30GHz to 300GHz) benefit from ultra-high bandwidth and unique physical attributes. With the portability brought by IC techniques, mm-wave chips have enabled applications such as ultra-high-speed (5G/6G) communications, mobile satellite communications, Internet-of-Things (IoT) sensors, ultra-high-resolution radar and various kinds of dieletric, biomedical and chemical sensors. However, with stringent power budget of portable devices and the power-hungry attribute of mmWave circuits, low-power and low-noise on-chip mmWave signal generation and radar design are faced with great challenges.

In the first part of this dissertation, a new mmWave frequency synthesizer structure is proposed. Based on Sub-Sampling Phase-Locked Loop (SSPLL) technique, the generated signal achieves low in-band phase-noise. With the proposed dividerless frequency acquisition technique based on a Sub-Sampling Lock Detector (SSLD) and on-chip intermediate-frequency PLL (IF-PLL), the SSPLL can automatically detect its lock status and lock to the correct target frequency without using power-hungry mmWave Injection-Locking Frequency Dividers (ILFD). To verify the proposed system, a prototype 40.5GHz SSPLL chip has been taped out in 65nm CMOS. Due to the relatively low-frequency operation and moderate noise requirement of IF-PLL, as well as the low-power SSLD, the proposed system achieves low power consumption and jitter simultaneously. The measured results show an 8.8mW power consumption and 228fs RMS jitter with in-band and out-band phase noise of -96.6dBc/Hz at 1MHz offset and -106.9dBc/Hz at 10MHz offset, respectively.

Another critical issue of charge pump (CP) current mismatch and its exclusive effects on SSPLL are presented in this dissertation. Transistor's channel-length-modulation (CLM) effect induces SSPLL loop gain distortion and decreases VCO control voltage (V_{ctrl}) locking range (LR). A feedback based compensation method, which is the first-published solution to SSPLL CP mismatch, is then proposed. In a prototype mmWave SSPLL with the proposed compensated CP, the CLM effect is cancelled and V_{ctrl} LR is extended from 0.50V to 0.75V under a 1V supply, without degrading SSPLL noise performance much. As a result of the more efficient use of V_{ctrl} range, VCO capacitor bank setup number is reduced from 10 to 7 to cover the same 10% total tuning

range. The compensation circuitry consumes only 0.36mW power. The prototype 40.5GHz SSPLL consumes only 9.5mW power with 192fs RMS jitter.

Radar sensors with ultra-high range resolutions have great potential in non-contact sensing of human vital signs, biomedical signals, material thickness and mechanical vibration, and in imaging. With short wavelengths for high resolution and relatively simple structure, mmWave Doppler radar has become a competitive candidate in various displacement-sensing applications. However, issues like detection nulls, nonlinear gain and quadrature signal paths mismatch limit the performance of mmWave Doppler radar. In the last part of this dissertation, a novel system structure of Doppler radar front end is proposed utilizing the intrinsic low added in-band noise feature of SSPLL and a proposed quadrature-less demodulation method. A prototype 110mW 39GHz Doppler radar front end in 65nm CMOS for displacement and vibration sensing is presented. Sub-sampling PLLs (SSPLL) generate single-tone radiated signal. A proposed phase demodulator (PDM) uses coherent IF demodulation to convert displacement to a DC/baseband signal with constant gain. Detection nulls in conventional Doppler radars are eliminated without using quadrature demodulation. The prototype radar achieves $4\mu m$ static and $77nm$ vibrational (at 10KHz) range resolutions.

Acknowledgments

I invite you to think. What is the purpose of life? What would you like to do if you have all the resources you crave? What are truly meaningful?

From mundane point of view, one of the most meaningful endeavours of a human being is to advance our civilization. Art works, creative ideas, scientific research, innovations and inventions ... Civilization is the unique collection of things we human beings develop. Now, I dare to say without regret, that I have spent part of the most precious years in my life on contributing to the advancement of scientific research.

However, as my life is not coming to an end yet, the endeavour is far from over. I invite you, my dear readers, to join me and perpetually to lead instead of to follow, to pioneer instead of to settle, to innovate instead of to chase the ambulance.

Throughout the PhD study at UC Davis, I couldn't have expressed my acknowledgment enough to so many people.

It is my greatest honor to have known and be advised by Prof. Omeed Momeni, who has given me so much freedom in coming up with new ideas and trying them out. His insights, wisdom, optimism and passion on both academic topics and life have deeply influenced me directly and by osmosis. From my humble perspective, Prof. Momeni has exemplified as a paragon of advisors, far beyond merely a teacher or a researcher. All my research accomplishments would not possibly have been achieved, or even initiated, without the brainstorming with and the continuous guidance and support from Prof. Momeni. I'm sincerely obliged to him.

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Top-notch research is always accompanied by obstacles and grueling days. Thanks to many artistic works, I could refresh myself with laugh, pleasure and optimism, and go back to the battle field recharged.

I thank all the persons, acquainted and strange, who helped me, inspired me and trusted me.

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CHAPTER 1

Introduction

As scientist Xuesen Qian introduced in his classic "Engineering Cybernetics", using feedback control, very accurate systems can be achieved with not-so-accurate components [**1**]. Nowadays, feedback based systems are pervasive in almost every aspect of engineering design, with famous examples of phase-locked loop (PLL) based frequency synthesizers and various categories of radar systems. Through combinational innovations, individual new techniques can be organically intertwined into exponentially powerful networks, leading to sustaining breakthroughs, advancing human civilizations, and benefiting the whole world [**2**,**3**]. Guided by the philosophy of innovation, several research projects have been conducted during my PhD study on developing novel integrated circuits and systems with low power consumption, low noise and high accuracy. The results are hereby presented in this dissertation.

The structure of this dissertation is as follow: Chapter 2 introduces on-chip mmWave frequency synthesizer design and the proposed low-power and low-noise sub-sampling phase-locked loop (SSPLL) with dividerless frequency acquisition technique. A 8.8mW 40.5GHz prototype frequency synthesizer is presented. The synthesizer system consists of an SSPLL with 100MHz crystal reference, a 900MHz high-frequency-reference (HFR) PLL and a novel sub-sampling lock detector (SSLD). The SSLD keeps monitoring the locking status of the SSPLL by sampling the SSPLL output with the HFR 900MHz reference, and automatically controls the SSPLL for frequency acquisition if it loses lock or locks to a wrong 100MHz harmonic. This is done without using power-consuming divider-based frequency-locked loop in conventional SSPLL. Due to the relatively low-frequency operation and moderate noise requirement of HFR, as well as the low-power SSLD, the proposed system achieves low power consumption and jitter simultaneously. The measured results show 8.8mW power consumption and 228fs RMS jitter with in-band and out-band phase noise of -96.6dBc/Hz at 1MHz offset and -106.9dBc/Hz at 10MHz offset, respectively.

Chapter 3 raises the issue of charge pump (CP) current mismatch and its exclusive effects in SSPLL, and proposes a compensation method which is the first-published solution to this issue. Transistor's channel-length-modulation (CLM) effect induces SSPLL loop gain distortion and decreases VCO control voltage (V_{ctrl}) locking range (LR). In a prototype design of a 40.5GHz SSPLL with the proposed compensated CP, feedback loops cancels the CLM effect and hence extends V_{ctrl} LR from 0.50V to 0.75V under a 1V supply, without degrading SSPLL noise performance. As a result of the more efficient use of V_{ctrl} range, VCO capacitor bank setup number is reduced from 10 to 7 to cover the same 10% total tuning range. Due to the low-power dividerless structure with sub-sampling lock detector SSLD for frequency acquisition, the SSPLL with the proposed compensated CP consumes only 9.5mW power with 192fs RMS jitter.

Finally in Chapter 4, a novel system structure of Doppler radar front end is proposed utilizing the intrinsic low in-band added noise feature as well as the developed techniques introduced in the previous chapters. A 110mW 39GHz continuous-wave (CW) Doppler radar front end in 65nm CMOS for displacement/vibration sensing is presented. Sub-sampling PLLs (SSPLL) generate single-tone radiated signal. A proposed phase demodulator (PDM) converts displacement to a DC/baseband signal with constant gain. Detection nulls in conventional CW radars are eliminated without using quadrature demodulation. Coherent demodulation allows the radar to achieve $4\mu m$ static and $77nm$ vibrational (at 10KHz) range resolutions.

This dissertation is composed mainly based on the published works during my PhD study. Hence, significant overlap exists between the published conference and journal papers and the content in Chapter 2 through Chapter 4. The readers are invited to follow the extended and future works related with the techniques presented in this dissertation, especially on the high-resolution Doppler radar sensor in Chapter 4 briefly introduced due to the limited time left after the measurement results were obtained and before the completion of this dissertation.

CHAPTER 2

Dividerless Frequency Acquisition for Millimeter-Wave SSPLL

2.1. Introduction

Millimeter-Wave (mmWave) signals play an increasingly important role in many emerging applications including $5^{th}/6^{th}$-generation (5G/6G) wireless communications [**4**, **5**], biomedical and dielectric sensing [**6**] and specialty applications such as atomic clock excitation [**7**] as shown in Fig. 2.1. With integrated circuit (IC) technology advancing towards faster and higher-performance processes, on-chip mmWave signal generation and frequency synthesis have become a reality [**8**]. A critical specification of mmWave frequency synthesis is the signal's phase noise and jitter. Given that individual circuit blocks such as voltage-controlled oscillators (VCO) have poor free-running phase noise, complex structures such as feedback based phased-locked loop (PLL) must be adopted to generate low-noise mmWave signals. However, systems with more components usually call for higher power consumption. This is even worse for circuits running at mmWave frequencies due to the higher loss. With the trend of designing energy-efficient electronic devices with low power budget, especially for wireless mobile user ends and ubiquitous Internet-of-Things (IoT) networks [**9**], researchers have been investigating novel low-power system structures for mmWave frequency synthesis while maintaining low noise performance.

Over the past decade, sub-sampling phase-locked loop (SSPLL) has become a popular candidate in frequency synthesis for its lower in-band phase noise (PN) than the frequency-divider based PLL counterparts [**10**]. However, one of the drawbacks of SSPLL is the possible locking to wrong harmonics of input reference. A frequency-locked-loop (FLL) based on divider-chain must be adopted to produce a correct output frequency [**10**]. Such frequency dividers, which are typically based on injection-locked structures, suffer from limited locking range and high power consumption, and requires high injecting power from VCO [**11**, **12**, **13**]. To save power, prior-arts on SSPLL

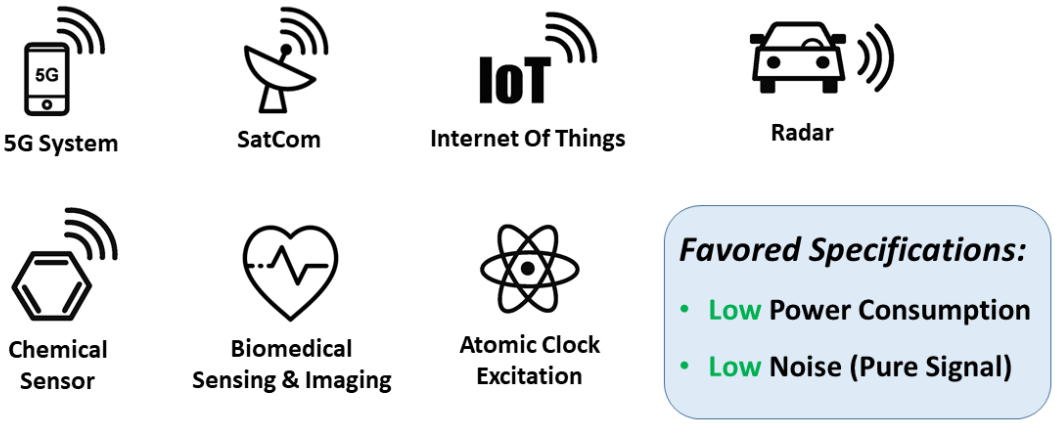


FIGURE 2.1. Applications needing mmWave signal generation.

claim to turn off FLL after sub-sampling loop is locked to the correct reference harmonic [**10**, **14**]. However, this procedure is manual, and lacks a reliable mechanism to automatically detect unlock/locked-to-wrong-harmonic states and re-enable the FLL. As a result, FLL must be always on and induces high power consumption.

In this chapter, we propose a low-power mmWave frequency synthesizer structure, achieving frequency acquisition at 40.5GHz through a novel sub-sampling lock detector (SSLD) without frequency dividers [**15**]. As a result, the proposed system consumes only 8.8mW with 228fs RMS jitter.

This chapter is organized as follows: We first analyze different on-chip mmWave frequency synthesizer structures in Section 2.2, and then lead to our proposed SSPLL system structure in Section 2.3. Then a prototype SSPLL based on the proposed structure is presented in Section 2.4. In Section 2.5, we introduce the proposed sub-sampling lock detector (SSLD), which is the essential block achieving automatic low-power frequency acquisition. Section 2.6 presents the detail design and considerations of the SSPLL main loop. Section 2.7 and Section 2.8 present the design of the mmWave blocks and the high-frequency reference generation PLL, respectively. Measurement results follow in Section 2.9. After comparison with the state-of-the-art, we conclude our paper in Section 2.10.

2.2. On-Chip Millimeter-Wave Frequency Synthesizers

Several mainstream circuit structures have been developed to achieve on-chip mmWave frequency synthesis. The most straightforward method, shown in Fig. 2.2, uses a conventional PLL to multiply a reference frequency f_{ref} by M and generate $f_{out} = M * f_{ref}$ [**8**, **16**]. Here, the noises from reference PN, together with phase frequency detector (PFD), charge pump (CP) and loop filter (LF) are amplified to the output by M^2. The in-band output PN of conventional PLL is derived as:

$$\mathcal{L}_{\text{in-band,PLL}} = (\mathcal{L}_{\text{ref}} + \mathcal{L}_{\text{PFD,CP}}) \cdot \mathrm{M}^2 \ , \tag{2.1}$$

where $\mathcal{L}_{\text{ref}}$ is the input reference PN, $\mathcal{L}_{\text{PFD,CP}}$ is the PLL input-referred PN of PFD and CP.

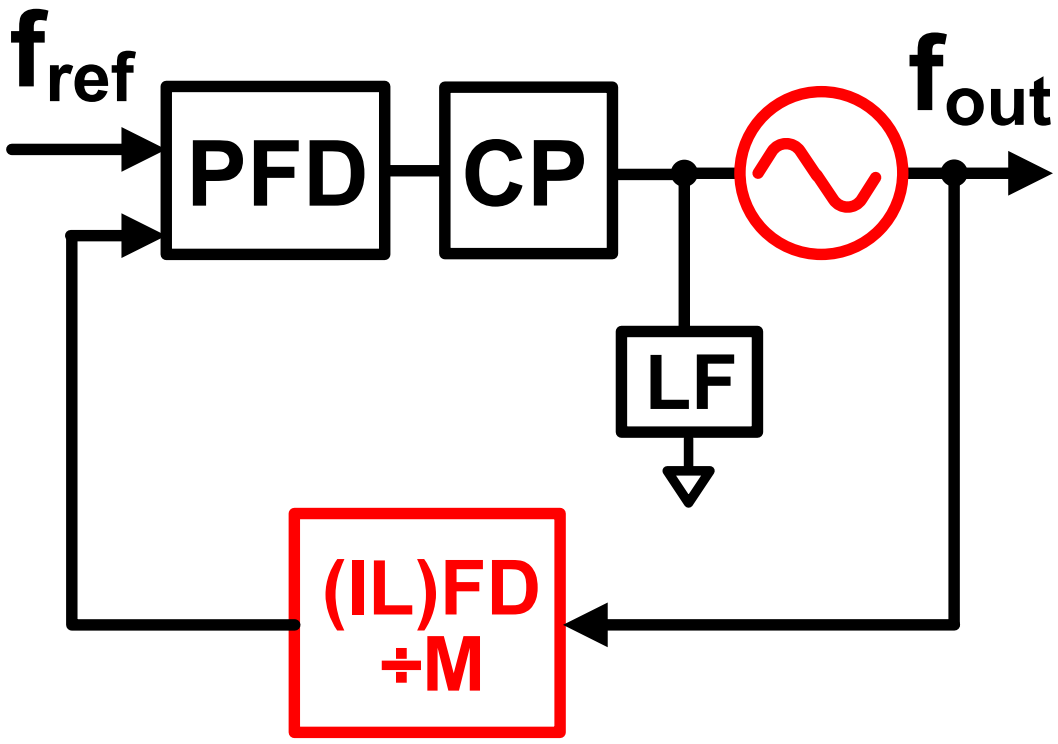


FIGURE 2.2. Conventional divider-based PLL.

Comparably, sub-sampling PLL (SSPLL) shown in Fig. 2.3 can significantly reduce in-band PN contributed by the sub-sampling phase detector (SSPD) and the CP [**10**]:

$$\mathcal{L}_{\text{in-band,SSPLL}} = \mathcal{L}_{\text{ref}} \cdot \text{M}^2 + \mathcal{L}_{\text{SSPD,CP}} \ , \tag{2.2}$$

where $\mathcal{L}_{\text{SSPD,CP}}$ is the SSPLL input-referred PN of SSPD and CP. However, SSPLL can lock to any integer harmonic of f_{ref}. Hence, a frequency-locked loop (FLL) is necessary to ensure certain output frequency. Both conventional PLL and SSPLL involve frequency dividers (FD) in their structures. Constrained by the limited transistor speed with CMOS processes, frequency dividers typically adopt injection-locked structures (ILFD) when operating at mmWave [**12**]. Nevertheless, ILFD suffers high power consumption when operating at mmWave frequencies, requires high injecting power from the mmWave VCO to ensure reliable injection [**17**], and suffers from limited locking range if injected with low-power signals [**11**, **13**]. Another sampling PLL structure, reference-sampling PLL (RSPLL), emerges in recent years [**18**]. However, RSPLL needs to rectify its output to be square-wave with high-slope edges to sample the reference. With the limited transistor speed (f_T) of CMOS processes, rectifying mmWave signals into sharp-edge square-waves is not feasible. Hence, RSPLL is usually not used for synthesizers beyond 10GHz.

To avoid using ILFDs for mmWave frequency synthesis, two candidates are available as shown in Fig. 2.4 and Fig. 2.5. Cascaded PLL in Fig. 2.4 generates an intermediate frequency, IF, with a first-stage conventional PLL, and then scale it up with an SSPLL [**19**, **20**, **21**]. Because frequency dividers only exist in the low-frequency first-stage PLL, their structure is of digital circuitry with low power consumption. Frequency acquisition is achieved by setting IF larger than the VCO's tuning range in the second stage. Hence, the SSPLL can only lock to one frequency, which is a certain harmonic of IF. However, cascaded PLL partially sacrifices the SSPLL low-noise performance to achieve frequency acquisition. Its in-band output PN is:

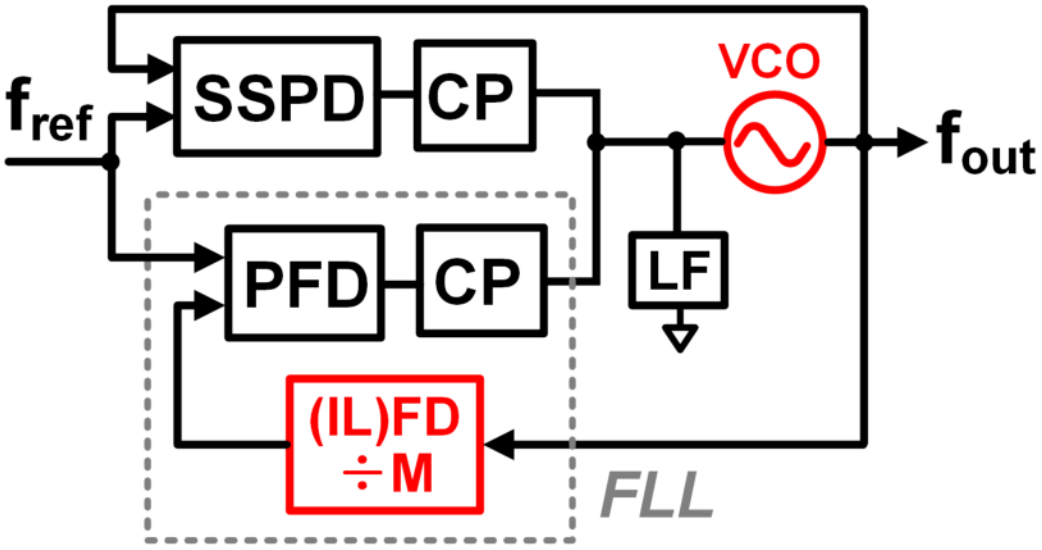


FIGURE 2.3. SSPLL with conventional divider-based FLL.

$$\begin{aligned}\mathcal{L}_{\text{in-band,CasPLL}} = &(\mathcal{L}_{\text{ref}} + \mathcal{L}_{\text{PFD,CP1}}) \cdot H_{\text{LP}}^2 \cdot \text{M}^2 \\ &+ \mathcal{L}_{\text{VCO1}} \cdot H_{\text{HP}}^2 \cdot {\text{M}_2}^2 + \mathcal{L}_{\text{SSPD,CP2}} \ ,\end{aligned} \tag{2.3}$$

where $M = M_1 * M_2$, $\mathcal{L}_{\text{PFD,CP1}}$ is the first-stage PLL input-referred PN of PFD and CP1, H_{LP} is the phase-domain closed-loop transfer function (low-pass behavior) from the first-stage PLL input to IF, $\mathcal{L}_{\text{VCO1}}$ is the open-loop output PN of VCO1, H_{HP} is the phase-domain closed-loop transfer function (high-pass behavior) from the VCO1's output to IF, $\mathcal{L}_{\text{SSPD,CP2}}$ is the second-stage SSPLL input-referred PN of SSPD and CP2. Although SSPD and CP2 noise contributions are low, the first-stage conventional PLL adds residual noise from its PFD, CP1, FD and VCO1. Prior works have shown that low noise can be achieved by carefully optimizing the first-stage conventional PLL bandwidth and the IF value [**19**]. However, such optimization results in a relatively high IF around several GHz, and thus increases the design complexity of the SSPD as well as the total system power consumption.

Fig. 2.5 shows another mmWave synthesis structure based on injection-locked frequency multipliers (ILFM) [**22**, **23**, **24**, **25**]. Like the case for cascaded PLL, a first-stage PLL is used to

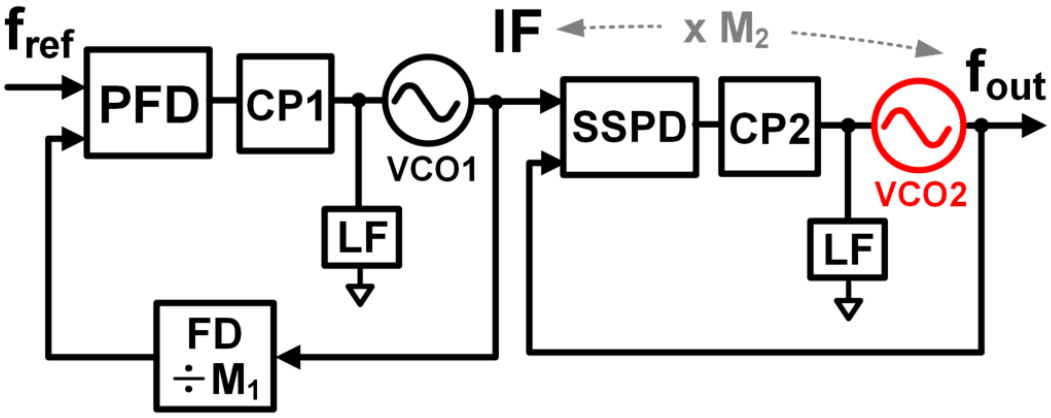


FIGURE 2.4. Cascaded PLL.

generate an IF. The first-stage PLL then drives an ILFM, or a chain of ILFM, to produce the final mmWave output as an integer multiple of IF. When properly locked, ILFM does not add much noise, but simply upscales the input signal's PN by square of the frequency multiplication number. Its in-band output PN is:

$$\begin{aligned}\mathcal{L}_{\text{in-band,ILFM}} = &(\mathcal{L}_{\text{ref}} + \mathcal{L}_{\text{PFD,CP}}) \cdot H_{\text{LP}}^2 \cdot \text{M}^2 \\ &+ \mathcal{L}_{\text{VCO}} \cdot H_{\text{HP}}^2 \cdot {\text{M}_2}^2 \ .\end{aligned} \tag{2.4}$$

Hence, ILFM is favored because of its low-noise performance. Similar to ILFD, ILFM is naturally an oscillator with resonant tank, and also suffers from limited locking range due to high quality-factor tank. To ensure locking, a frequency-tracking loop (FTL) is thus needed. While FD-based FTL could be very power hungry, low-power FTLs based on envelope/phase detection have been developed [**26**, **27**]. Nonetheless, to ensure proper locking and low PN, ILFM's input injecting signal must be strong enough [**28**, **29**, **30**]. While typical ILFM multiplication numbers are 2 to 4, such requirement means high injecting frequency with high power and that results in high power consumption for the synthesizer system.

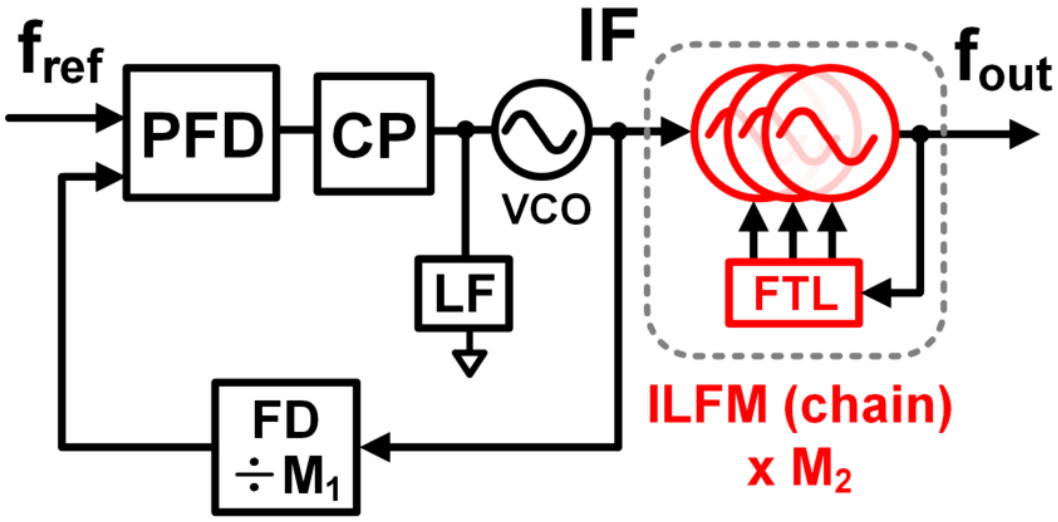


FIGURE 2.5. Injection-Locked Frequency Multipliers (ILFM).

TABLE 2.1. Comparison between existing and the proposed mmWave frequency synthesis structures.

Topology	**In-band PN**	**Power Consumption**
Traditional PLL	High	High
SSPLL+Divider-based FLL	Low	High
Cascaded PLL	Moderate	Moderate
ILFM	Low	High
Proposed SSPLL+SSLD	Low	Low

With the pros and cons of existing mmWave synthesizers, we are proposing a new structure based on SSPLL and a sub-sampling lock-detector (SSLD). As explained in the next section, our proposed synthesizer achieves low noise and low power consumption simultaneously without using ILFDs, and can operate over a wide temperature range. The automatic lock detection and re-lock procedure implemented by the novel SSLD greatly help with the robustness of the proposed synthesizer. Table 2.1 qualitatively compares the performance of existing mmWave synthesizer structures with the proposed system.

2.3. System Structure of Proposed Dividerless SSPLL

The conceptual diagram of our proposed mmWave frequency synthesizer is shown in Fig. 2.6 [**15**, **31**, **32**, **33**],. First, a low-frequency ring-oscillator based traditional PLL, IF-PLL, generates

an intermediate frequency, $IF = N \cdot f_{ref}$, from the input crystal reference with frequency of f_{ref}. The IF signal will be used to frequency-lock the mmWave SSPLL, as well as to detect the locking status of the SSPLL. The SSPLL output frequency, $f_{out} = M \cdot IF$, is a multiple integer of IF. When the SSPLL takes the IF as reference, the synthesizer becomes a cascaded PLL for frequency acquisition. Frequency tuning range for each capacitor bank setup of the SSPLL's VCO is designed to be smaller than IF. During the initial SSPLL calibration, it can be determined that which VCO bank setup generates the target f_{out}. Under this acquired bank setup and with IF as reference, the SSPLL can only possibly lock to the target frequency of $M \cdot IF$. Hence, the SSPLL achieves frequency locking without using mmWave frequency dividers.

After frequency acquisition is achieved, the SSPLL will directly take f_{ref} as reference and switch to the corresponding loop configuration to benefit from crystal's low PN. Hence, the IF signal only connects to the SSPLL during frequency acquisition and doesn't affect SSPLL steady-state output PN. This reference switching procedure is automatic and implemented by the sub-sampling lock detector (SSLD). The SSLD uses the IF to sample the SSPLL output, f_{out}, and detects whether the SSPLL is locked to the target frequency through internal signal processing. If the SSPLL loses lock, or locks to a wrong harmonic of f_{ref} (e.g. at $(N \cdot M + 1)\, f_{ref}$), the SSLD will automatically switch SSPLL's reference to IF, as well as the corresponding loop configuration accommodating IF, for frequency acquisition. As soon as SSPLL locks to $N \cdot M \cdot f_{ref}$, SSLD will switch SSPLL's reference back to f_{ref} and keep monitoring the locking status. Hence, with the help of the SSLD, the proposed system achieves automatic lock detection and re-lock for SSPLL.

Low power consumption of the proposed system in Fig. 2.6 is achieved with the design of the IF-PLL and SSLD. Since the IF reference connects to the SSPLL only during frequency acquisition, its PN doesn't affect the SSPLL steady-state output PN. Hence, the value of IF is not constrained by any noise-based optimization as that in a cascaded PLL [**19**], and it can be selected solely based on the mmWave VCO TR. As explained later, IF is typically chosen to be around 1GHz to make IF-PLL operate at a relatively low frequency and consume low power. Furthermore, noise of IF is only required to be low enough to perform the SSLD sampling operation. This requirement is much more relaxed than the one needed to achieve the best SSPLL output PN. Therefore, the IF-PLL

can be designed with more flexibility to trade off noise performance for lower power consumption. The SSLD also consumes very low power since it contains only one block operating at mmWave frequency: an output buffer for SSPLL VCO. The buffer is required to moderately amplify the voltage amplitude, instead of power, of the SSPLL output and therefore can be designed with low power consumption. As shown in the next sections, other blocks in SSLD consume little power when the SSPLL is locked. Moreover, unlike the traditional ILFD-based SSPLL, the proposed dividerless SSPLL doesn't require the mmWave VCO and buffers to deliver high injection power to subsequent blocks. Consequently, VCO and buffers can be biased in Class-AB operation for low power consumption.

2.4. Prototype 40.5GHz Low-Power & Low-Noise SSPLL

Based on the system structure in Fig. 2.6, a prototype 40.5GHz SSPLL with the proposed dividerless frequency acquisition mechanism is designed. System diagram of the prototype mmWave frequency synthesizer is shown in Fig. 2.7. In our design, IF is chosen to be 900MHz so that $f_{out} = 40.5GHz = 45 \times 900MHz$. Choosing IF value also affects power consumption: a very high IF (e.g. 2.7GHz) means more power budget for the IF generation PLL, while a very low IF (e.g. 300MHz) demands the SSPLL VCO to have more capacitor banks and hence more high-frequency

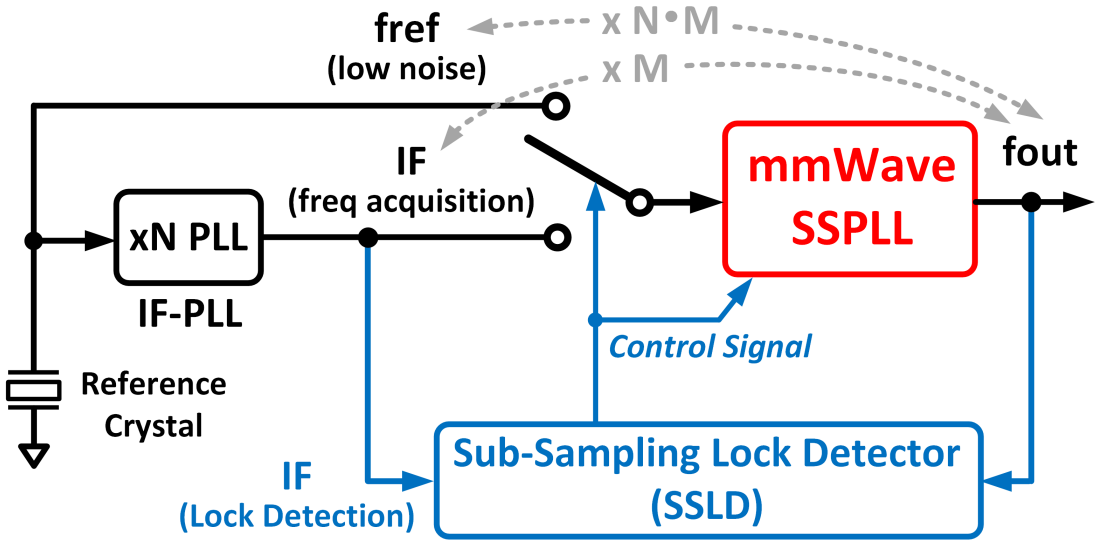


FIGURE 2.6. Concept of the proposed mmWave SSPLL without ILFDs.

loss to cover the same total tuning range. During the initial SSPLL calibration, it can be determined which VCO capacitor bank setup generates the target f_{out}. Using this acquired bank setup, the SSPLL can only possibly lock to one harmonic of 900MHz to generate 40.5GHz.

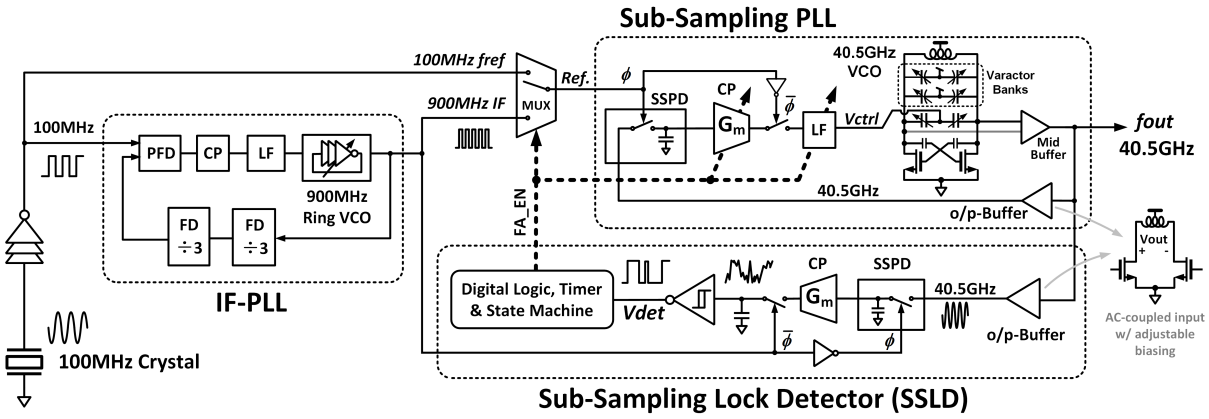


FIGURE 2.7. Detail system diagram of the prototype 40.5GHz dividerless SSPLL.

The SSPLL loop will directly take the 100MHz crystal signal as reference to benefit from crystal's low PN, after frequency acquisition is achieved. Hence, the 900MHz signal doesn't affect SSPLL output PN in steady state. The reference switching procedure is automatic and implemented by the sub-sampling lock detector (SSLD). The SSLD uses the 900MHz IF to sample the SSPLL output and uses internal signal processing to detect whether the SSPLL is locked to 40.5GHz. If the SSPLL loses lock, or locks to a wrong 100MHz harmonic, e.g. at 40.7GHz, the SSLD will automatically switch SSPLL's reference to 900MHz for frequency acquisition. As soon as SSPLL locks to 40.5GHz, SSLD will switch SSPLL's reference back to 100MHz and keep monitoring the locking status. Hence, with the help of the SSLD, our proposed system achieves automatic lock detection and re-lock for the SSPLL.

The system achieves low-power mmWave frequency synthesis due to the following reasons:

- The high-frequency reference PLL (HFR), producing the 900MHz IF, operates at relatively low frequency and hence consumes low power. This is because the HFR's frequency is not constrained by any noise-based optimization as that in [**19**], and it can be selected solely based on mmWave VCO tuning range;

- The 900MHz reference's PN doesn't affect the SSPLL output, because it is connected to the SSPLL only during frequency acquisition. Hence, the HFR noise is only required to be low enough to perform the SSLD sampling operation. This requirement is much more relaxed than the one needed to achieve the best mmWave phase noise at the output. Therefore, the 900MHz PLL can be designed with low power consumption;
- As shown in Fig. 2.7, the SSLD contains only one block operating at mmWave frequency: a VCO output buffer. The buffer is required to moderately amplify the voltage amplitude of the 40.5GHz signal and therefore can be designed with low power consumption. Following the output buffer, SSLD's analog interface, consisting of SSPD and CP operating at 900MHz, consumes little power.

At the same time, the proposed synthesizer benefits from the low in-band PN by using a 100MHz crystal reference in steady-state, and thus achieves low noise and low power consumption simultaneously.

In the following sections, individual blocks' working principles, designs and considerations are presented and discussed in details.

2.5. Sub-Sampling Lock Detector (SSLD)

Lock detection blocks have been developed to monitor the PLL locking status. Prior arts use structures based on comparing input reference with quadrature PLL output [**34**] or with frequency-divided output [**35**]. These structures are not suitable for mmWave low-power design due to the power-hungry divider chain. In this section, we propose a low-power sub-sampling lock-detector (SSLD), which detects whether the SSPLL is locked to the target frequency and can automatically control the loop to go through frequency acquisition if the SSPLL loses lock or locks to wrong 100MHz harmonics.

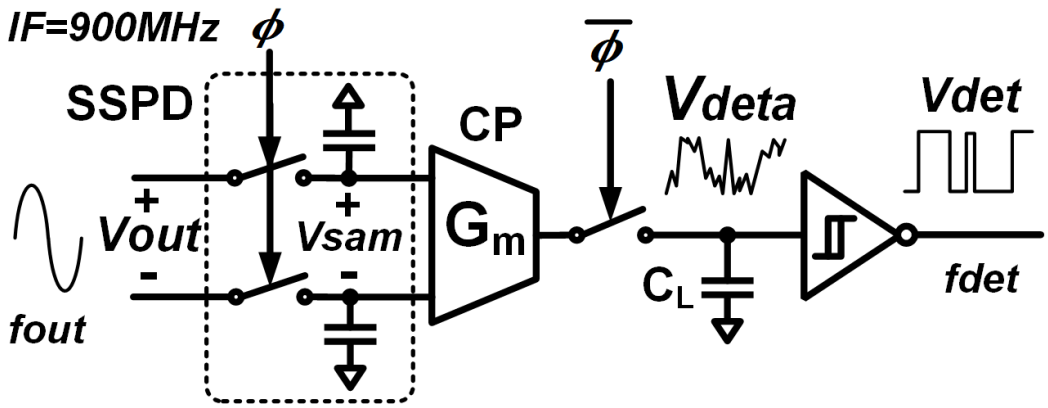


FIGURE 2.8. Analog interface of the proposed SSLD.

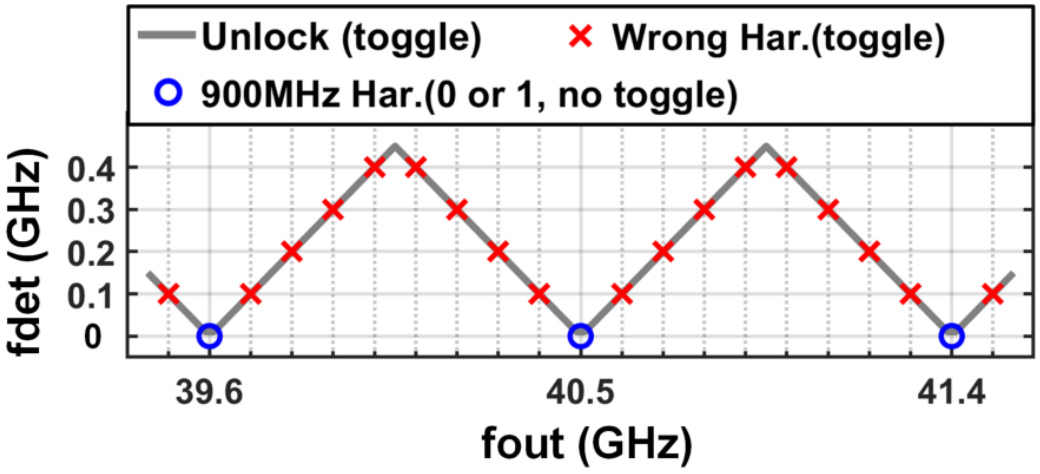


FIGURE 2.9. Princple of sub-sampling lock detection: relationship between sampled waveform toggling frequency f_{det} and SSLD input frequency f_{out}.

2.5.1. Analog Interface. To examine whether an SSPLL output frequency f_{out} is an integer multiple of 900MHz, we can use the 900MHz signal to sub-sample the SSPLL output signal V_{out}. Fig. 2.8 shows the input analog interface of the SSLD. The sampling switches output signal V_{sam} is a semi-discrete signal and its sampled value can be calculated as:

$$V_{sam}(n) = A_{sam} \sin\left(2\pi \frac{f_{out}}{900MHz} n + \phi_{sam}\right) , \tag{2.5}$$

where n is an integer standing for the n^{th} sample, A_{sam} is the amplitude, ϕ_{sam} is the random default phase of V_{sam} and f_{out} is the SSPLL output frequency. We then amplify V_{sam} with a charge pump and a small capacitive loading, and then rectify it to be a square-wave signal V_{det} with a Schmitt trigger. V_{det} can be calculated as:

$$V_{det}(n) = \frac{1}{2} sign\left\{\sin\left(2\pi \frac{f_{out}}{900MHz} n + \phi_{sam}\right)\right\} + \frac{1}{2} \ . \tag{2.6}$$

To better understand the locking status of the SSPLL, V_{det}'s toggling frequency, f_{det}, needs to be explored. Since V_{det} is a discrete-time signal with a sampling rate of 900MHz, its frequency shown in time-domain is restrained by the Nyquist sampling criteria of $f_{det} < 900MHz/2$. For example: f_{det} is 100MHz for all values of $f_{out} = N * 900MHz + 100MHz$; f_{det} is also 100MHz, instead of 800MHz, for $f_{out} = N * 900MHz - 100MHz$, because of the Nyquist sampling criteria [**36**]. Hence, we can summarize the expression of f_{det} as:

$$\begin{aligned} f_{det} = \min\{ & f_{out} \bmod 900MHz, \\ & 900MHz - (f_{out} \bmod 900MHz)\} \ , \end{aligned} \tag{2.7}$$

where "$a \bmod b$" is the remainder of a divided by b. Values of f_{det} is examined for three SSPLL lock states:

2.5.1.1. *SSPLL locks to 900MHz Harmonics.* When the SSPLL locks to 900MHz harmonics, $f_{out} = N * 900MHz$, where N is an integer. Hence we have:

$$V_{det}(n) = \frac{1}{2} sign\{\sin(\phi_{sam})\} + \frac{1}{2} \ . \tag{2.8}$$

In this case, sampled phase of SSPLL output does not change with time, $V_{det}(n)$ becomes a stable value of either 0 or 1, and therefore $f_{det} = 0$ (shown as blue circles in Fig. 2.9).

2.5.1.2. *SSPLL locks to wrong 100MHz harmonics.* When the SSPLL takes 100MHz as reference, it may lock to a 100MHz harmonic which is not a 900MHz harmonic. Then we have $f_{out} = N * 900MHz + M * 100MHz$, where N and M are integers and $-4 \leq M \leq 4$. In this case, toggling frequency $f_{det} = M * 100MHz$ according to (2.7) (shown as red crosses in Fig. 2.9).

2.5.1.3. *SSPLL loses lock.* When the SSPLL loses lock, initially f_{out} is a straying random value, and V_{det} will toggle at random frequencies in the 0 to 450MHz range (shown as gray lines in Fig. 2.9). Finally, because the 100MHz reference keeps sampling the loop, the SSPLL will settle and lock to an 100MHz harmonic (red crosses in Fig. 2.9). Thus, this case reduces to either case 1) or case 2).

Fig. 2.9 illustrates (2.7) and summarizes the abovementioned cases with f_{out} centered at 40.5GHz, which is used and implemented in this work. The goal of the SSLD is to make sure the SSPLL operates at the blue circle, where $f_{out} = 40.5GHz$ and V_{det} does not toggle. During the SSPLL initial calibration, free-running VCO's frequency tuning range across capacitor banks will be measured, and the banks are then set to contain the 40.5GHz target frequency. The VCO is designed to have less than 900MHz tuning range for each bank setup, so that after initial calibration, 40.5GHz will be the only 900MHz harmonic to lock to. A waveform illustration example of SSLD analog interface signals corresponding to case 2 is shown in Fig. 2.10. For simplicity in plotting, f_{out} is chosen to be 9.3GHz, which is 300MHz away from the closest 900MHz harmonic. As can be deduced from Fig. 2.9, we can verify that V_{det} has a toggling frequency of 300MHz.

Due to circuit noise, the theoretical calculation of f_{det} will change randomly in real application. Jitter of the 900MHz signal, σ_{IF}, together with the SSPLL output phase error ϕ_{err} will induce a random phase error $\Delta\phi(n) = 2\pi f_{out}\sigma_{IF}(n) + \phi_{err}(n)$ at each sampling moment. When the SSPLL locks to a 900MHz harmonic and in the presence of noise, V_{det} in (2.8) becomes:

$$V_{det}(n) = \frac{1}{2} sign\left\{\sin\left[\phi_{sam} + \Delta\phi(n)\right]\right\} + \frac{1}{2}\ . \tag{2.9}$$

Here we reasonably assume that the 900MHz jitter induced phase error is significantly larger than ϕ_{err}, so $\Delta\phi(n) \approx 2\pi f_{out}\sigma_{IF}(n)$. From (2.9) we observe that, if σ_{IF} is too large, V_{det} may toggle

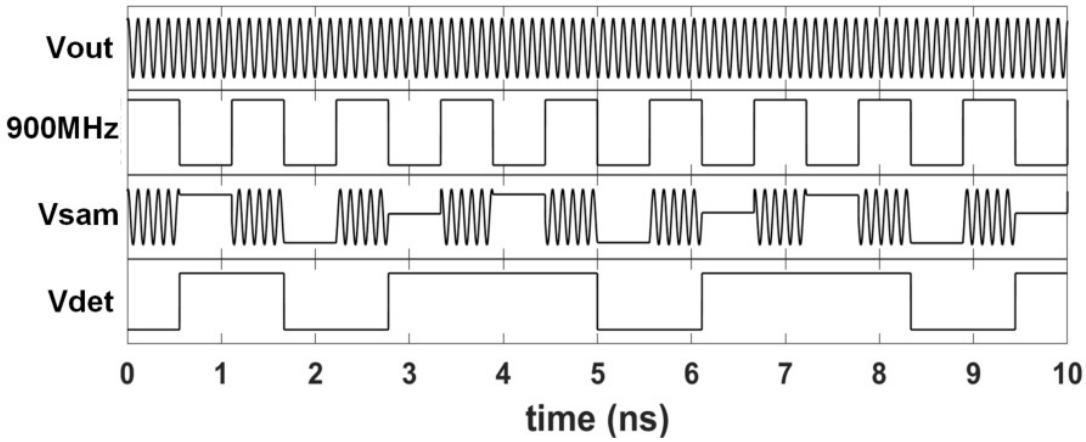


FIGURE 2.10. An example of SSLD Analog Interface output, in case of f_{out} = 9.3GHz, deviating 0.3GHz from the closest 900MHz harmonic, producing f_{det} = 300MHz.

stochastically even if the SSPLL has locked to a 900MHz harmonic. As will be discussed in the next subsection, the toggling number of $V_{det}(n)$ is only counted within a small time window. Thus, given the short time span of the window, the phase error is mainly induced by the short-term period jitter which are contributed by high-frequency part of 900MHz PN [**37**]. Since VCO noise dominates the high-frequency PN in a PLL, the 900MHz PLL is designed with high loop bandwidth to suppress its ring-VCO's PN and to achieve a low short-term jitter.

To prevent the jitter-induced random toggling of V_{det}, parameters of the SSLD analog interface and the 900MHz reference jitter must be carefully designed. From (2.9) it is observed that, $\Delta\phi(n)$ is most likely to toggle V_{det} when $\phi_{sam} \approx 0$. The output of the Schmitt trigger in our design is inverted by a rising input above 0.75V or a falling input below 0.25V, i.e. a hysteresis of V_{hys}=0.5V, under a 1V supply voltage. Suppose that the SSPLL is locked to f_{out}=40.5GHz, and Schmitt trigger input, V_{deta}, is at 0V (or 1V) with $\phi_{sam} \approx 0$ when SSPLL is locked, and V_{det} is settled to 1V (or 0V). In order to avoid jitter-induced Schmitt trigger inverting, maximum jitter-induced voltage change on V_{deta} during one sampling cycle should satisfy:

$$\Delta V_{deta,j} = A_{sam} \sin\left(2\pi f_{out} \sigma_{IF,max}\right) G_m \frac{T_{IF}}{2C_L} \ll 0.25V + V_{hys}, \tag{2.10}$$

where $\sigma_{IF,max}$ is the maximum period jitter of the 900MHz reference, G_m is the charge pump transconductance, $T_{IF} = 1.1ns$ is the period of the 900MHz IF, and C_L is the voltage holding capacitor in Fig. 2.8. On the other hand, when SSPLL is not locked to 40.5GHz, V_{det} must be able to toggle. In such cases, $V_{sam}(n)$ is approximately a discrete sine-wave according to (2.5). Let's define a parameter $0 < k < 100\%$, and require that any $|V_{sam}(n)|$ larger than kA_{sam} can charge/discharge V_{deta} to toggle V_{det} within one sampling cycle. Hence, the following should be satisfied:

$$\Delta V_{deta,tog} = kA_{sam}G_m\frac{T_{IF}}{2C_L} > 0.25V + V_{hys}. \tag{2.11}$$

We must design the SSLD parameters and the 900MHz jitter to satisfy (2.10) and (2.11) simultaneously. In our design, we first choose $k = 60\%$ so that V_{det} can toggle for any $|V_{sam}(n)| > 60\%A_{sam}$, and we have $A_{sam} = 0.15V$ for low-power mmWave buffer, $G_m = 1mS$ and $C_L = 50fF$, so that $\Delta V_{deta,tog} = 1V$ to satisfy (2.11). Then, with $f_{out} \approx 40.5$GHz, condition (2.10) translates into: $\sigma_{IF,max} \ll 1.83$ps, which means a RMS period jitter smaller than 1.3ps for the 900MHz reference. Such a moderate jitter requirement provides us great leeway to design a low power 900MHz PLL. Simulated SSLD-induced RMS output noise at V_{deta} is below 9mV (integrated from 1kHz to 1GHz), which is negligible compared to V_{hys}.

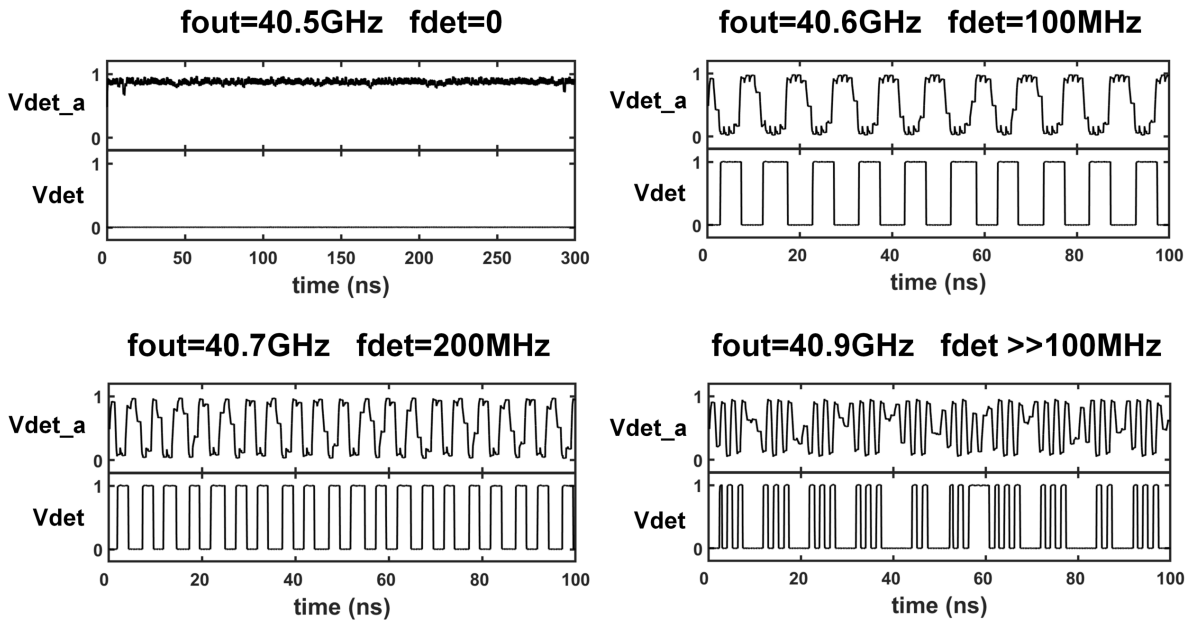


FIGURE 2.11. Simulated SSLD analog interface waveforms for various f_{out} values with transient circuit noise and reference jitter.

Fig. 2.11 shows the circuit simulation result of the SSLD analog interface corresponding to various f_{out} values. Transient 900MHz reference jitter and circuit noise are added in the simulation. Toggling frequency f_{det} is observed to be consistent with theoretical calculation in Fig. 2.9 when f_{out} is close to 900MHz harmonics. When f_{out} deviates too much from 900MHz harmonics, f_{det} doesn't strictly follow the theoretical value. This is because f_{det} is approaching to the limit of the Nyquist sampling criteria of $f_{det} < 900MHz/2$, and sampled phase of V_{out} periodically reaches very small values. These small sampled phases induce small $V_{sam}(n)$ that can not be amplified enough to toggle the Schmitt trigger. However, since we choose $k = 60\%$ for condition (2.11), there are periodical samples with high/low enough values to toggle V_{det} even if f_{det} approaches Nyquist limit.

From the above analysis, it is inferred that V_{det} is not a very accurate indicator of the exact frequency difference between f_{out} and 900MHz harmonic. However, as mentioned before, SSLD's objective is only to distinguish two states of the SSPLL: a) Locked to the 900MHz harmonic; b) Unlocked to the 900MHz harmonic, including unlock state and locked to wrong 100MHz harmonics.

Hence, in practice, if V_{det} toggling frequency is above a certain number, SSPLL is not locked to the correct frequency. This property can be used to generate the control signal for re-lock procedure. Next, we will explain the methodology to achieve this goal.

2.5.2. Digital Logic & State Machine. After producing V_{det} signal from the analog interface, it is fed into the digital logic circuit for further signal processing and control signal generation. Fig. 2.12 shows the pseudo-digital circuitry, which contains analog delay cells. First, the digital logic needs to detect whether the SSPLL locks to the 900MHz harmonic. As discussed previously, this is indicated by the f_{det} value in three cases: a) When the SSPLL is locked to the 900MHz harmonic, $f_{det} \approx 0$; b) When the SSPLL is locked to wrong 100MHz harmonics, $f_{det} \geq$100MHz; c) When the SSPLL loses lock, f_{out} initially strays as a random value and induces temporary $f_{det} \gg 0$, and finally locks to a 100MHz harmonic after the SSPLL is settled. And this case reduces to either a) or b). Hence, to detect whether the SSPLL locks to the target 900MHz harmonic, we only need to distinguish between the two cases of $f_{det} \approx 0$ and $f_{det} \geq$100MHz. We can thus set a threshold frequency value of $0 < f_{th} <$ 100MHz to distinguish these two cases. As discussed previously, jitter and circuit noise induce random toggling on V_{det}. In our design, f_{th} is chosen around the middle between 0 and 100MHz for a good tolerance on the random toggling.

f_{det} is measured in a statistical way by counting V_{det} rising edge number within a preset time window of T_{win}. This is implemented by feeding V_{det} through a chain of N_{FD}-stage resettable D flip-flop dividers and checking the output signal CNT at the end of the time window. Within T_{win}, the minimum V_{det} rising edge number required to flip CNT from 0 to 1 is $1 + 2^{N_{FD}-1}$. This translates to a threshold toggling frequency of:

$$f_{th} = \frac{2^{N_{FD}-1}}{T_{win}}. \tag{2.12}$$

Next, a digital logic is designed to generate an indicating signal $TRIG$: a) If $f_{det} < f_{th}$, the SSPLL is locked to the 900MHz harmonic and $TRIG$ is always 0; b) If $f_{det} > f_{th}$, the SSPLL is not locked to the 900MHz harmonic and $TRIG$ is changed to 1. Note that for a determined f_{th}, T_{win} doubles for every one more stage divider, and it will significantly increase detection time. Thus,

N_{FD} should not be too high. Meanwhile, N_{FD} should also be significant enough for the detection to tolerate V_{det}'s jitter-induced random togglings within T_{win}. In this work, we choose T_{win}=400ns and $N_{FD} = 5$ to have $f_{th} = 40$MHz according to (2.12). This means that when the SSPLL is locked to target frequency and $f_{det} = 0$, the lock detection can tolerate up to 16 random togglings within 400ns without triggering the re-lock procedure.

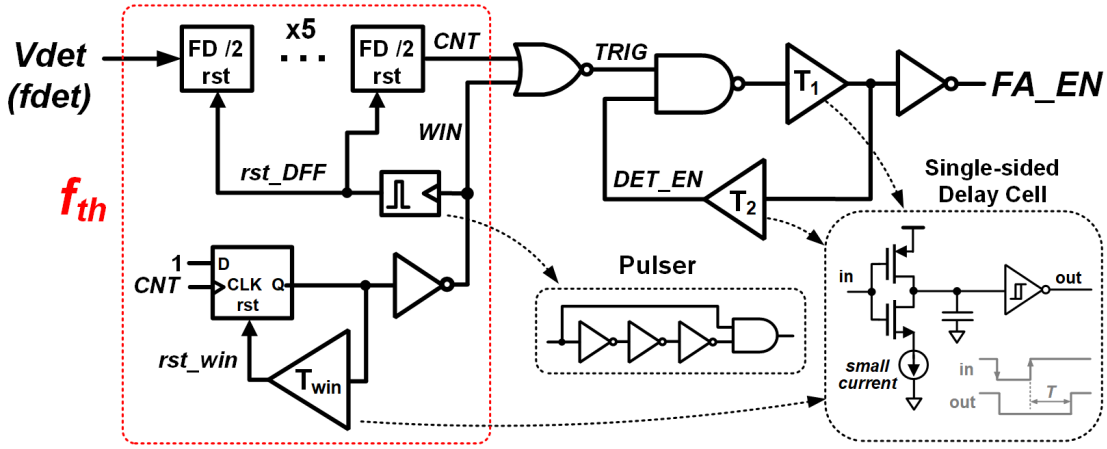


FIGURE 2.12. Digital circuitry following the SSLD analog interface, for signal processing and SSPLL reference control signal generation.

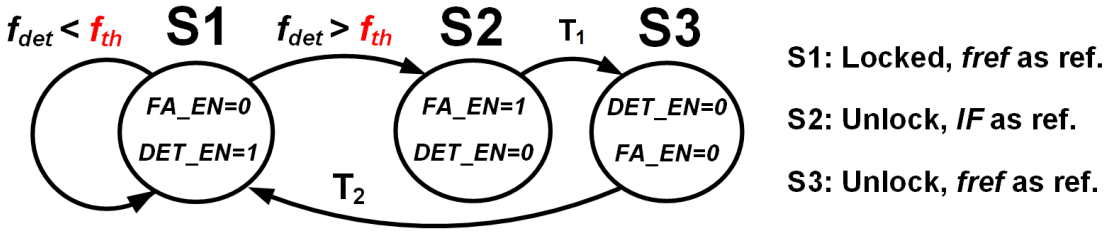


FIGURE 2.13. State machine diagram of the SSLD digital logic illustrating unlock detection and automatic frequency acquisition.

A pseudo-digital finite-state machine (FSM) shown in Fig. 2.13 is designed to generate a control signal FA_EN for enabling SSPLL frequency acquisition and re-lock procedure. As shown

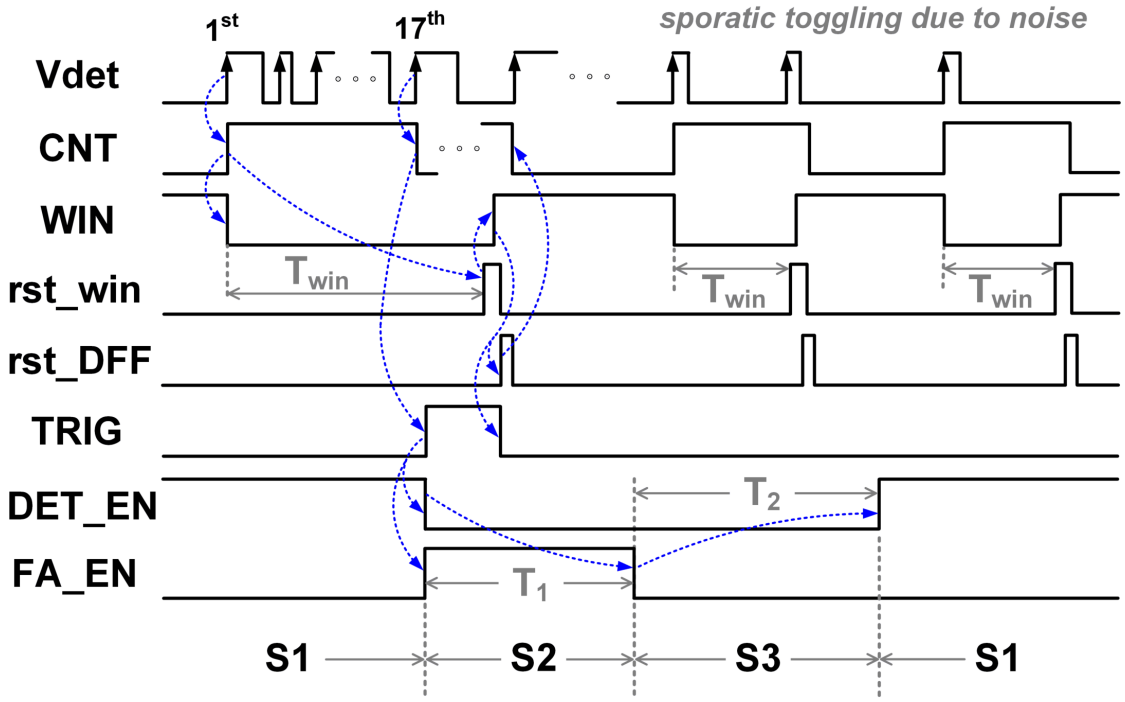


FIGURE 2.14. Illustration of the SSLD digital logic signals in different states.

in Fig. **??**, FA_EN selects different references and loop configurations for the SSPLL: when FA_EN=0, the SSPLL takes 100MHz as reference with corresponding configurations in CP and LF for low-noise phase-lock; when FA_EN=1, the SSPLL takes 900MHz as reference and switches to different CP and LF configurations for frequency acquisition. Signal DET_EN is designed to enable or disable the lock detection. When $DET\_EN = 0$, output of the D flip-flop chain is disconnected from the following digital logic, and the lock detection is disabled. The SSLD state machine works as follows. State S1 corresponds to the desired case in which the SSPLL is locked to the 900MHz harmonic. In this state, the SSPLL takes 100MHz as reference and the SSLD keeps detecting the lock status. After SSPLL unlock/wrong-frequency-locking status is detected, the FSM will enter state S2, setting FA_EN to 1 to enable SSPLL frequency acquisition. S2 also sets DET_EN to 0 to temporarily disable lock detection, preventing the temporary random togglings of V_{det} from disturbing the FSM logic. After a sufficient time T_1, SSPLL locks to 900MHz and the FSM transits to state S3. In S3, FA_EN is set to 0 and the SSPLL reference is switched from 900MHz to 100MHz. The SSPLL needs to rectify the initial phase difference between its output and the

100MHz reference, and finally re-lock to 100MHz with f_{out} being the 900MHz harmonic. As will be discussed in the next section, the SSPLL loop must be designed to ensure that f_{out} won't deviate too much after the references are switched, otherwise f_{out} will be locked to a wrong 100MHz harmonic during S3. After a sufficient time T_2, SSPLL locks to 100MHz with our target f_{out}. Consequently, the FSM sets DET_EN to 1, enabling lock detection, and transits to state S1. This automatic and continuous lock detection and re-lock procedure ensures a reliable locking at all times. A detailed time-sequence signal illustration of the SSLD pseudo-digital circuitry is provided in Fig. 2.14. T_{win}, T_1 and T_2 are set by the edge-sensitive single-sided delay cells consisting of current-starved inverter, capacitive loading and Schmitt trigger. The delay cell delays the rising-edge input, while acts as a no-delay buffer for falling-edge input.

2.6. SSPLL Loop Design

2.6.1. Loop Gain & Bandwidth Switching. In a conventional SSPLL, besides the loop stability, the main concern in the design of the loop parameters is to achieve low output PN [**38**,**39**]. This is done by trading off low-frequency and high-frequency PN proportions, and optimizing the loop bandwidth ω_{BW} after individual block noise optimization for VCO, CP and SSPD etc. In our proposed structure, since the reference of the SSPLL is switched after frequency acquisition, another important loop design concern is to make sure the switching is smooth and f_{out} keeps the same value after switching.

The phase-domain model of the SSPLL is shown in Fig. 2.15. The closed-loop transfer function from SSPLL input phase to the VCO control voltage V_{ctrl} is derived as:

$$H_{Vctrl}(s) = \frac{V_{ctrl}(s)}{\phi_{in}(s)} = \frac{G \cdot H_{LF}(s)/K_{VCO}}{1 + G \cdot H_{LF}(s)/s} \ , \tag{2.13}$$

where $G = K_{SSPD} \cdot K_{CP} \cdot K_{VCO}$, $K_{SSPD} = A_{out}$ is the gain of SSPD, A_{out} is the 40.5GHz signal amplitude at SSPD output, $K_{CP} = G_m \tau_{pul}/Tref$ is the gain of CP, G_m is the CP transconductance, T_{ref} is the reference period (in this case 10ns), τ_{pul} is the SSPD sampling pulse width (in our design $\tau_{pul} = 0.5Tref$), $H_{LF}(s)$ is the loop filter transfer function and K_{VCO} is the VCO voltage-to-frequency gain.

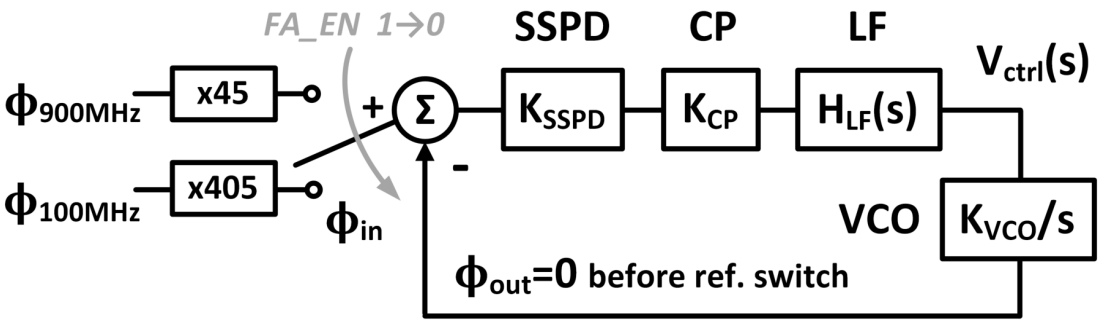


FIGURE 2.15. SSPLL loop design consideration for maintaining correct f_{out} after reference switching: SSPLL phase-domain model.

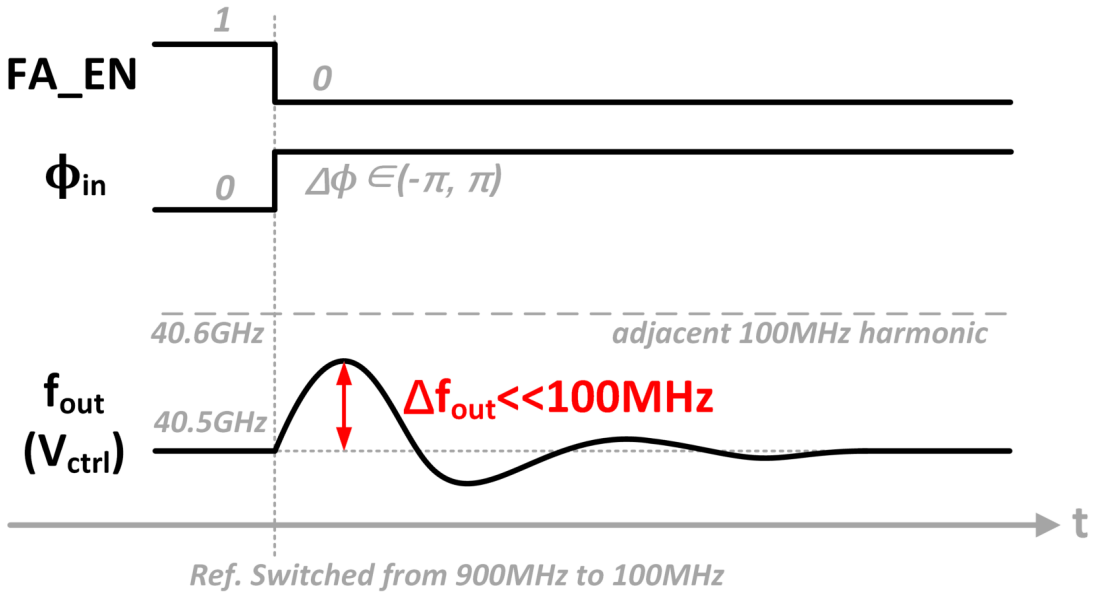


FIGURE 2.16. Illustration of transient signal waveforms during reference switching procedure.

Before reference is switched from 900MHz to 100MHz, the SSPLL output and the 900MHz reference have already locked with no phase difference. Immediately after switching 100MHz to the SSPLL input, the initial phase input from the 100MHz is ϕ_{in}, and has a radian range of $-\pi$ to $+\pi$. In a quick switching operation, ϕ_{in} acts as a step change at the SSPLL input and induces a

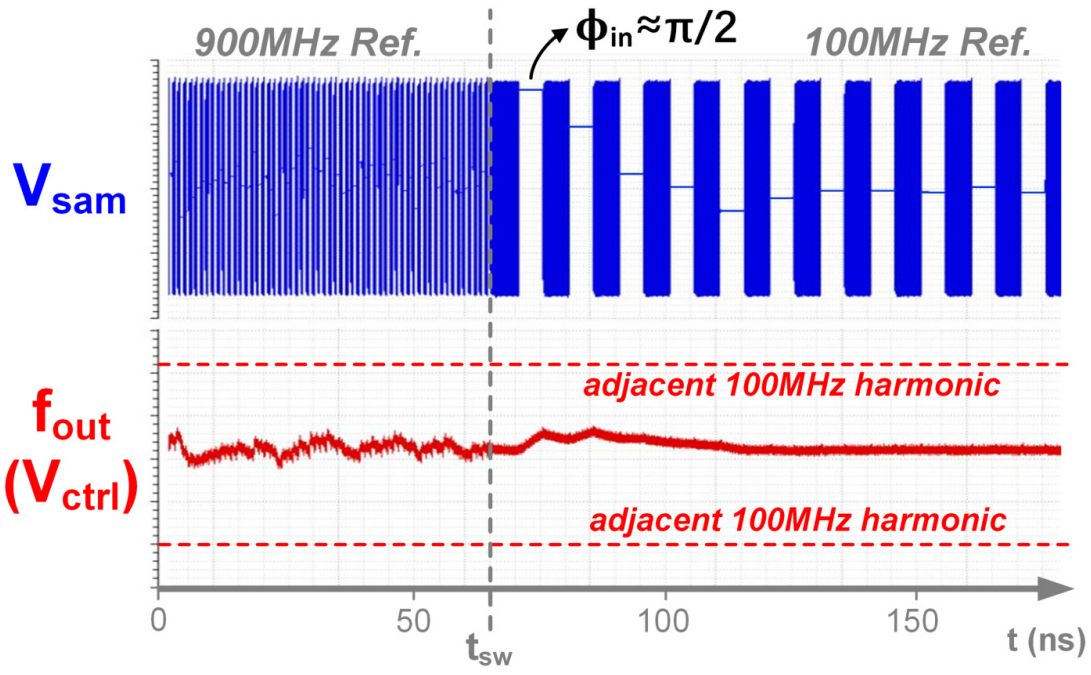


FIGURE 2.17. Simulated result of the proposed SSPLL with circuit noise and reference jitters, showing f_{out} locks to its expected value after reference switching.

step response at V_{ctrl} and hence f_{out}. This procedure is illustrated in Fig. 2.16 with transient signal waveforms. The maximum f_{out} deviation $\Delta f_{out,max}$ can be theoretically calculated by analyzing the time-domain expression of $V_{ctrl}(t)$. The loop should be designed to have $|\Delta f_{out,max}| \ll 100\text{MHz}$ for all $|\phi_{in}|$, ensuring that the SSPLL won't lock to adjacent wrong 100MHz harmonics after switching. Step response of the loop and its maximum frequency deviation is derived in Appendix A. Because SSPLL is configured to accommodate the 100MHz reference after switching, K_{CP} and $H_{LF}(s)$ used in our calculations are of the values for the 100MHz reference configuration. It can be observed from (A.5) that the maximum possible frequency deviation happens when $|\phi_{in}| = \pi$. Hence, with (A.5), the loop parameters should satisfy the following condition:

$$|\Delta f_{out,max}(\pi)| = \frac{2\pi GR \cdot exp\left(\frac{-\pi}{2\sqrt{4GC_pR^2-1}}\right)}{\sqrt{4GC_pR^2-1}} \ll 100\text{MHz} \ . \tag{2.14}$$

In the proposed SSPLL, the loop parameters are designed to satisfy (2.14) with a calculated $|\Delta f_{out,max}(\pi)| = 36MHz$. It must be noted that (2.13) is not strictly accurate for large ϕ_{in}, since $K_{SSPD} = A_{out}$ is only valid for small ϕ_{in} [**40**, **41**]. Hence, loop operation should be verified through circuit simulation. A simulated example of the proposed SSPLL during reference switching is shown in Fig. 2.17. This simulation includes transient noise and reference jitters. In this simulation, the maximum frequency deviation for $\phi_{in} \approx \pi/2$ is $|\Delta f_{out,max}(\phi_{in} \approx \pi/2)| \approx 20MHz$. Due to the linear behavior of the SSPLL loop, it can be inferred from (A.5) that, for the maximum phase input of $|\phi_{in}| = \pi$, the maximum frequency deviation $|\Delta f_{out,max}(\phi_{in} = \pi)| \approx 40MHz$. Hence, the simulated maximum frequency deviation is very close to the theoretical calculation in (2.14), and is small enough to avoid locking to the adjacent wrong 100MHz harmonics.

2.6.2. Circuit Implementation of SSPD, CP & LF. Fig. 2.18 shows the SSPD, CP and LF of the SSPLL. To satisfy both loop stability and smooth switching requirements, two sets of CP and LF configurations are designed for the two references. When taking the 900MHz reference, the loop gain and bandwidth are both high to enhance acquisition range, ensure fast locking and achieve good stability. With the 100MHz reference, the loop gain and bandwidth are both relatively small to design for low PN, good stability and smooth switching according to (2.14). K_{CP} and hence the loop gain is lowered by turning off the cascode transistors of CP output branches and hence reducing CP output current to $I_{cp,100\text{MHz}}$. LF and the loop bandwidths are reduced by enabling a new resistor segment, R_1, in the LF. C_p is deliberately not altered to avoid sudden change of V_{ctrl} and to achieve smooth switching. Manipulating C_p with sharp switching signal will induce significant instantaneous ΔV_{ctrl}, while adding R_1 merely induces a switch charge-injection which is filtered and dampened at V_{ctrl}. The time sequence shown in Fig. 2.19 is also important for a smooth switching: a) After FA_EN changes to 0, the reference signal, V_{ref}, is first switched from 900MHz to 100MHz. This switching is triggered by the falling edge of 100MHz reference. Hence, after reference switching, V_{ctrl} is disconnected from the CP and hold its value; b) The CP and LF configuration signals, circled 1 and 2 in Fig. 2.18, are changed after the reference switching. As a result, switching-induced instantaneous CP output current won't disturb V_{ctrl} and SSPLL f_{out} during reference switching. A V_{ctrl} buffer is added to eliminate any possible V_{ctrl} back charge from the VCO.

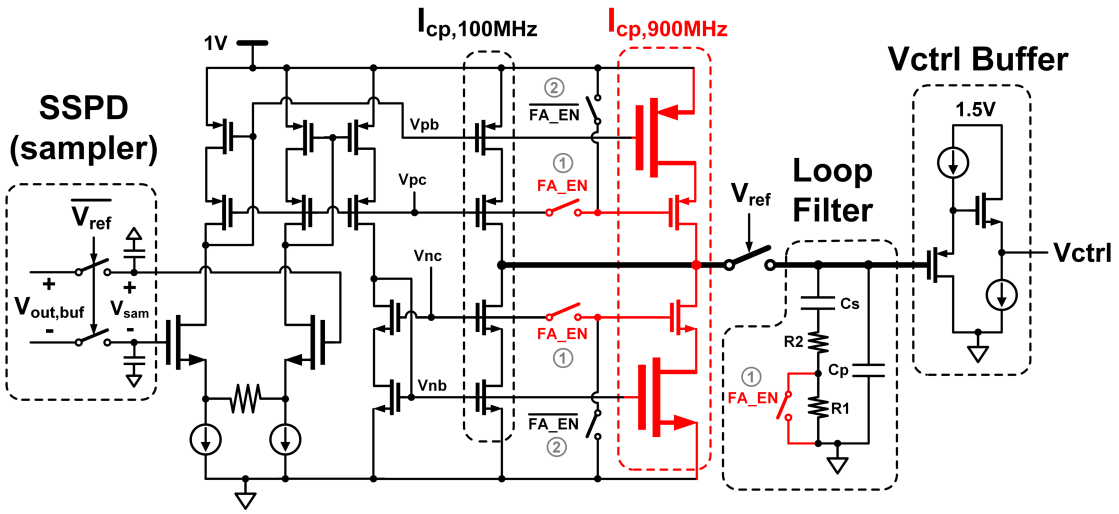


FIGURE 2.18. SSPD, charge-pump and Loop filter of the proposed SSPLL. Parts in red are enabled during frequency acquisition.

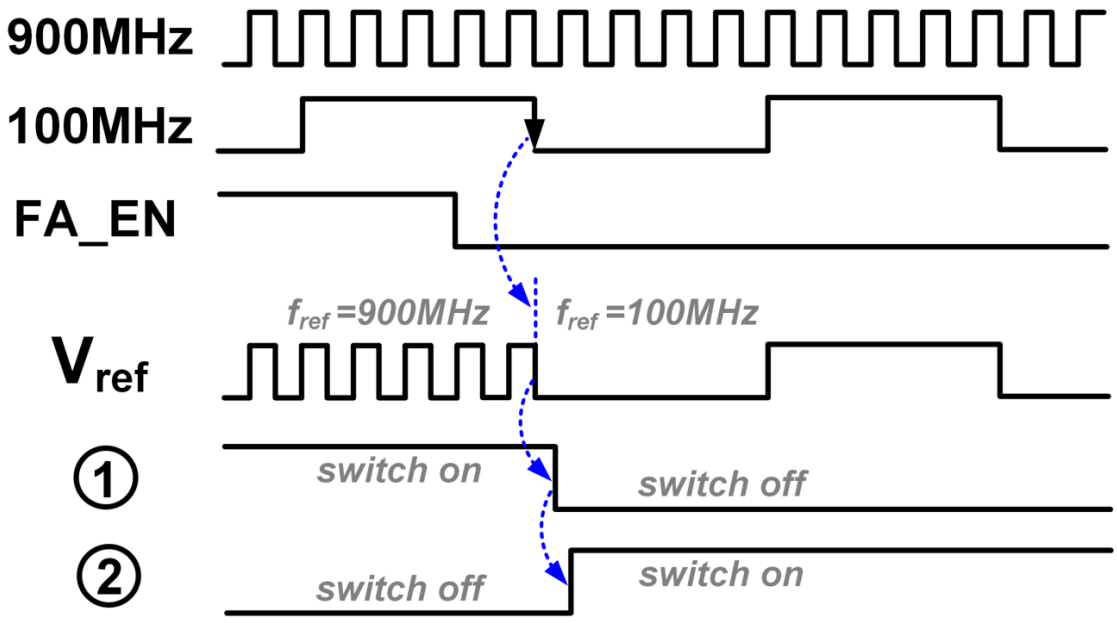


FIGURE 2.19. Time sequence consideration in switching signals on CP & LF.

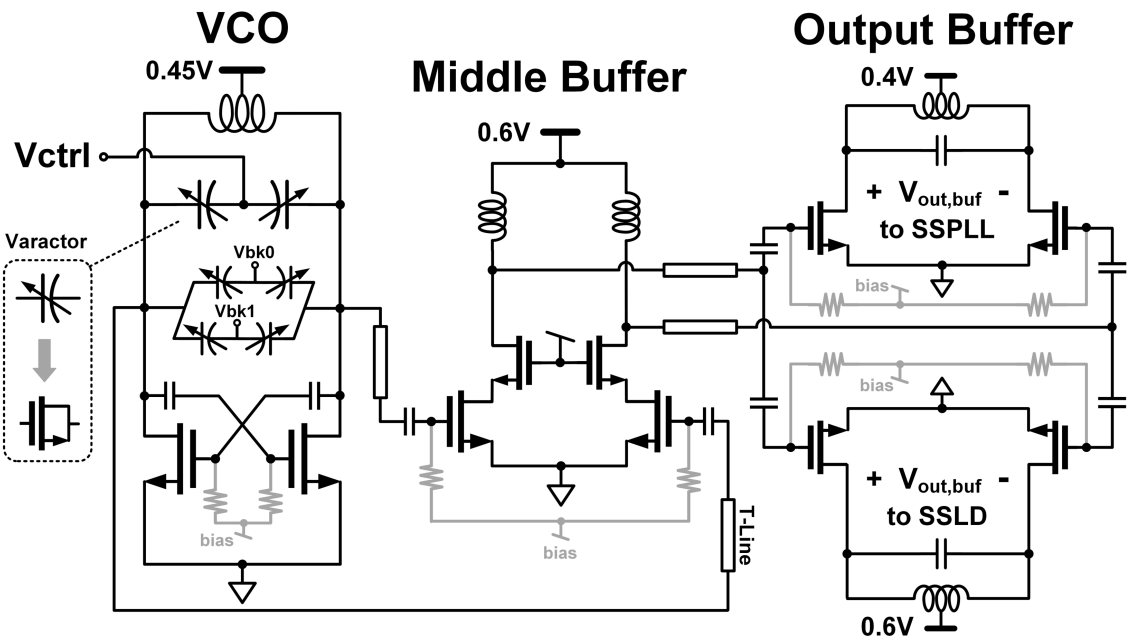


FIGURE 2.20. VCO and buffers of the proposed SSPLL.

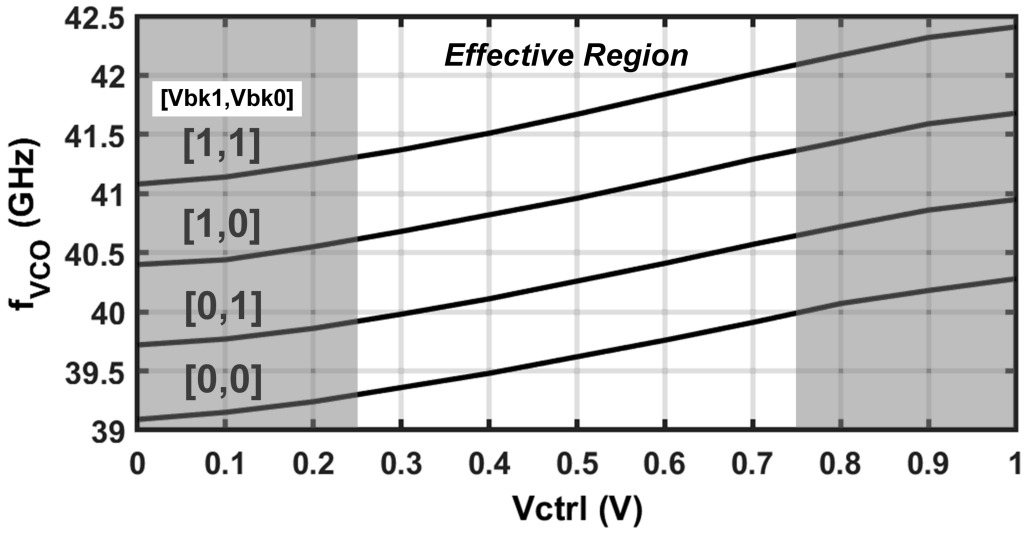


FIGURE 2.21. Simulated 40.5GHz VCO tuning range at room temperature.

2.7. VCO & Buffers

Fig. 2.20 shows the VCO and buffers of the SSPLL. The 40.5GHz LC-VCO is of cross-coupled structure with two varactor banks for frequency calibration. Fig. 2.21 shows the simulated VCO tuning range under various varactor bank setups. Considering that the CP transistors need to work in saturation region for good output current accuracy, V_{ctrl} thus has a corresponding effective region which is narrower than supply voltage as shown in Fig. 2.21. Under each bank setup, the effective VCO tuning range within the effective V_{ctrl} region is designed to be smaller than 900 MHz to satisfy frequency acquisition.

Two separate output buffers are connected to SSPLL and SSLD. A middle buffer with cascode amplifying stage is inserted between VCO and output buffers for better isolation. High amplitude V_{sam} is desired to achieve lower SSPLL output PN [**41**]. As shown in Fig. 2.18, SSPD switches have small on-resistance, and CP input has high impedance. Thus, when SSPD switches are on to generate V_{sam}, output buffer only needs to provide high voltage swing at the CP input, reducing the output power requirement for the buffers. Compared to the conventional ILFD-based SSPLL, our proposed dividerless SSPLL doesn't require VCO and buffers to deliver high injection power to subsequent blocks. Consequently, VCO and buffers are biased in class AB operation to have low power consumption.

2.8. High-Frequency Reference PLL

Sub-GHz PLL structures with low-power and low-noise performances are very mature nowadays [**42**], partly due to the advancement in low-noise inverter-based compact ring-VCO design [**43**, **44**]. Fig. 2.22 shows the HFR structure in our proposed synthesizer system. The HFR is a conventional x9 type-II PLL with a pseudo-differential ring-VCO. Load-controlled delay cells [**44**] are adopted for lower thermal noise than current-biasing counterparts. As mentioned previously, jitter requirement on HFR is not very demanding. Hence, there is more flexibility to trade off noise performance for lower power consumption in the HFR design.

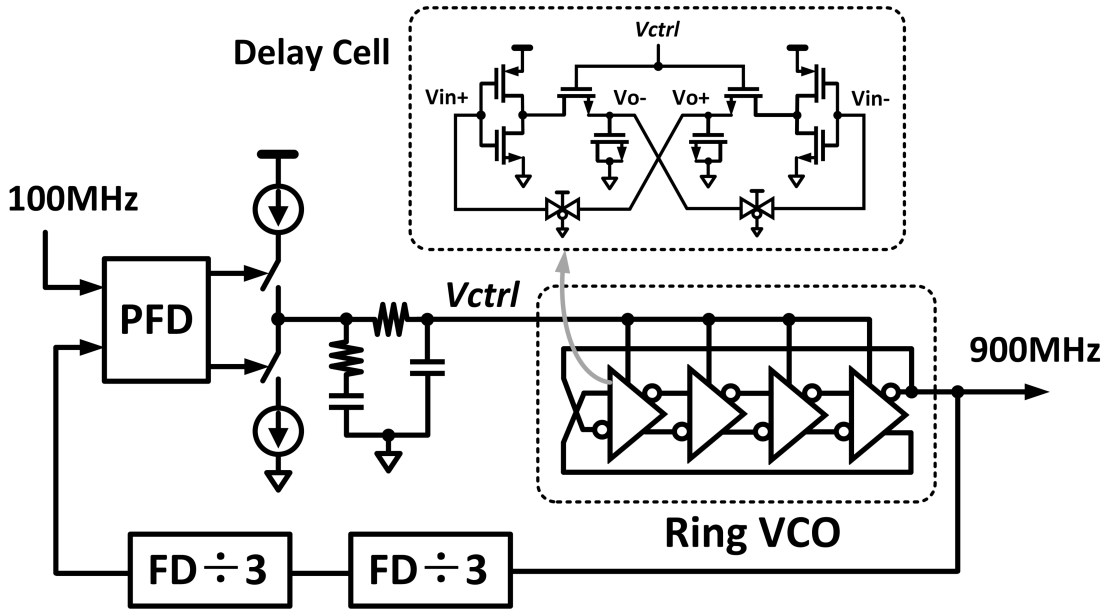


FIGURE 2.22. Block diagram of HFR, the 900MHz reference generation PLL.

2.9. Experimental Results

The proposed mmWave frequency synthesizer is designed and fabricated in a 65nm CMOS process. Die photo is shown in Fig. 2.23, with core area of $0.6mm^2$. Measurement setup is shown in Fig. 2.24. Measured VCO tuning range under 25 °C, −40 °C and 85 °C ambient temperatures is shown in Fig. 2.25. Within the effective region, VCO has a tuning range around 800MHz for each varactor bank setup. The −40 °C to 85 °C temperature range induces a VCO frequency variation of ±1%, which is small enough for the VCO to lock to 40.5GHz across temperature.

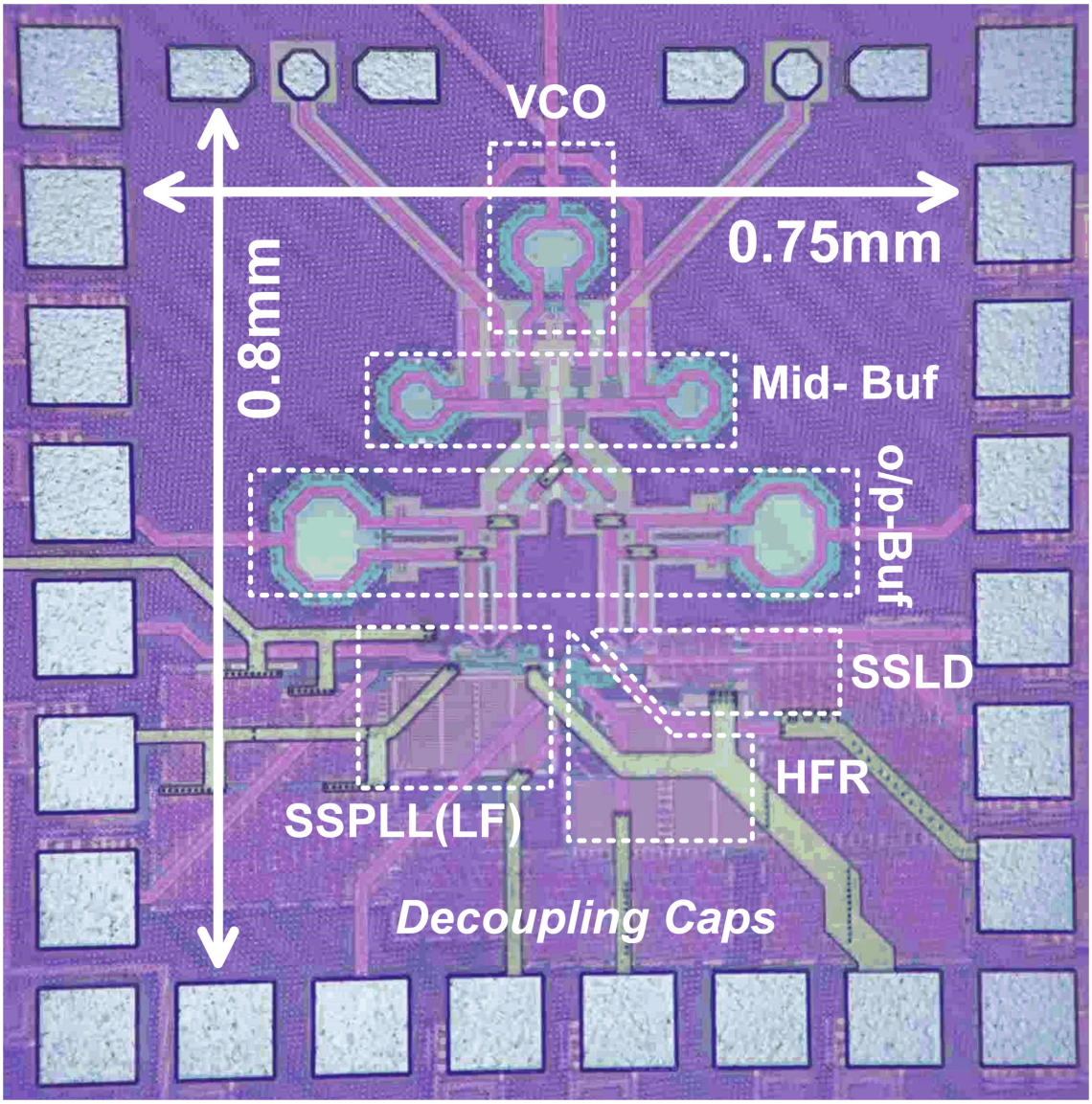


FIGURE 2.23. Chip die photo of the proposed mmWave frequency synthesize. Core area is $0.6mm^2$.

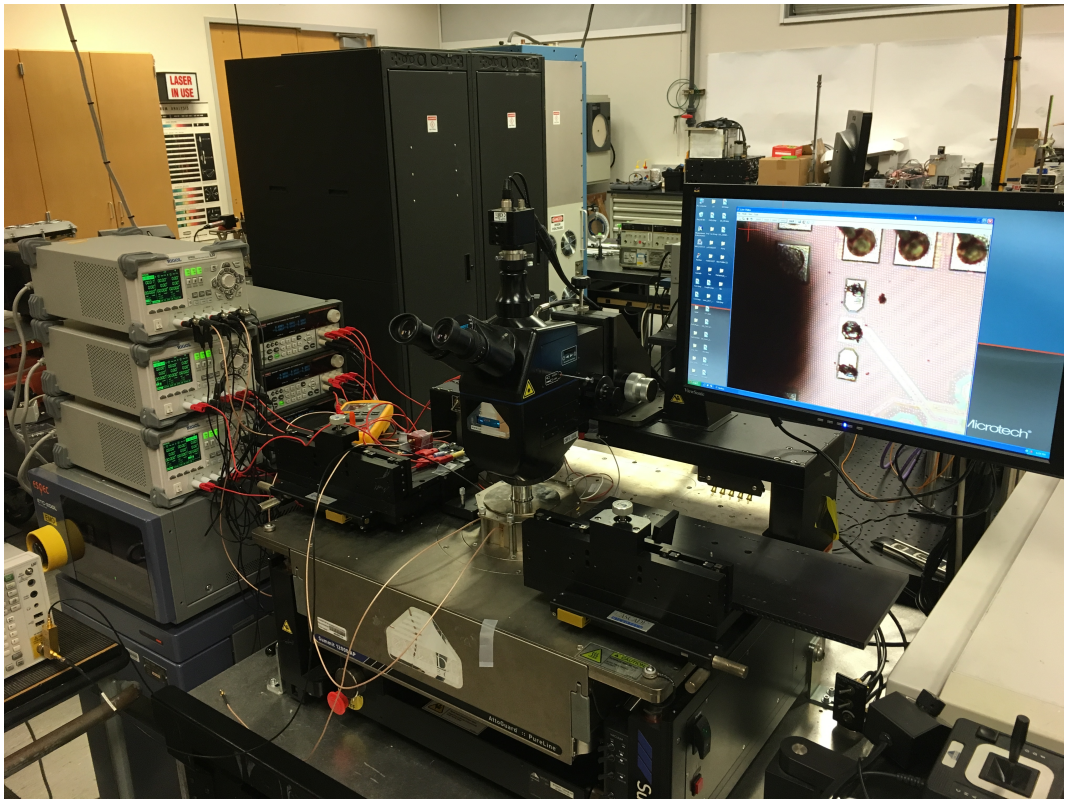


FIGURE 2.24. Measurement setup for the SSPLL chip.

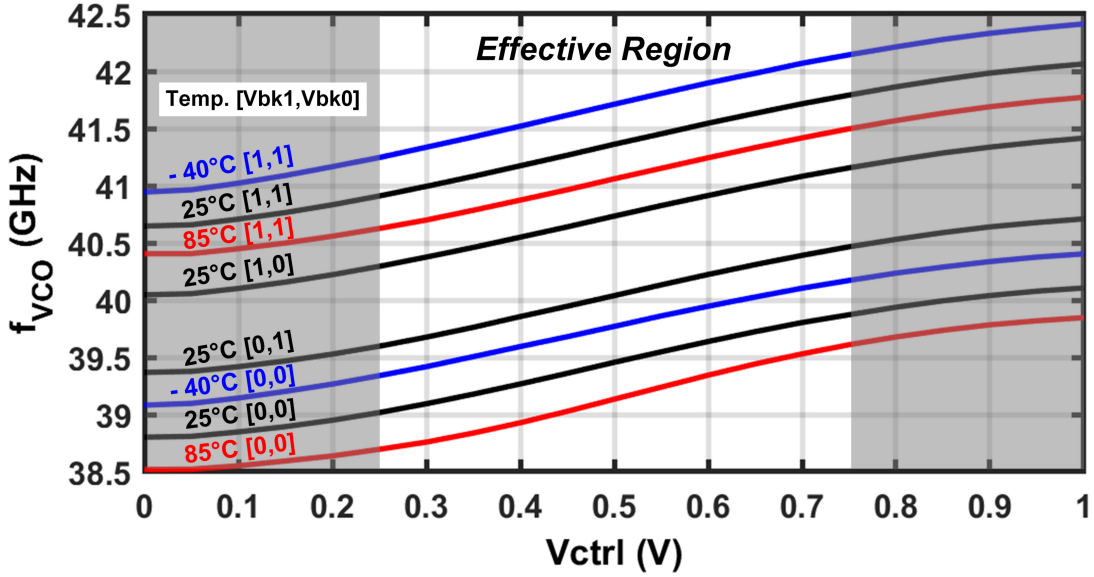


FIGURE 2.25. Measured 40.5GHz VCO tuning range under ambient temperatures of 25 °C, −40 °C and 85 °C with various varactor bank setups.

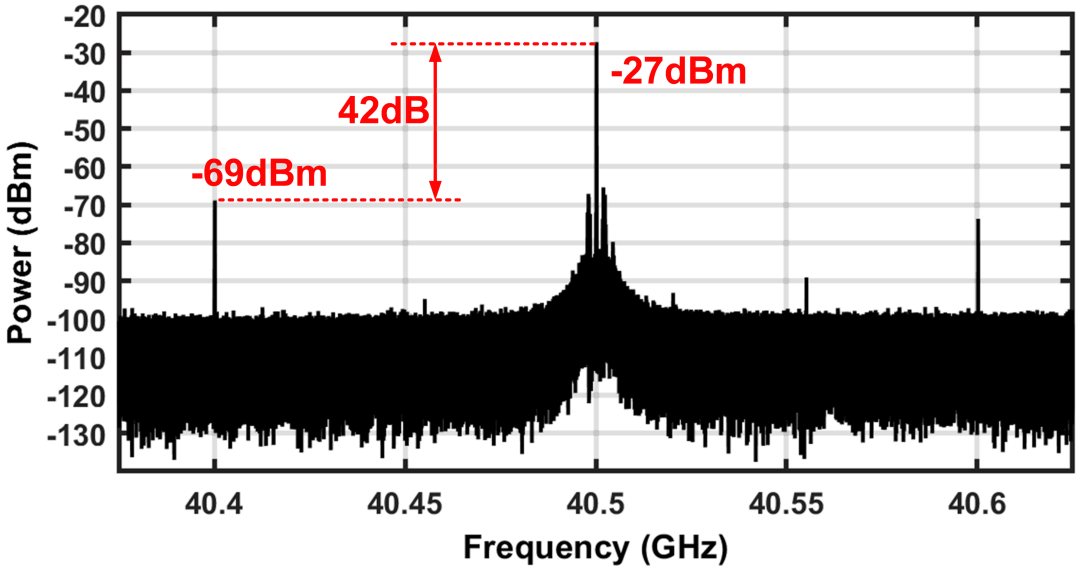


FIGURE 2.26. Measured SSPLL 40.5GHz output frequency spectrum with 100MHz reference.

The SSPLL's output signal is measured with a GSG probe, with a total cable and connector path loss of 10dB. A 100MHz crystal oscillator is used as input reference. Fig. 2.26 shows the measured frequency spectrum of the 40.5GHz SSPLL output when locked to the 100MHz reference, with a reference spur below -42dBc. The output power is high enough for our application of atomic clock excitation. An additional amplifier or stronger buffers can be adopted for higher power. The strong reference spur, which is not optimized for this design, is suspected to be caused by charge sharing from the V_{ctrl} holding switch between the CP output and the LF. Future works can adopt spur reduction techniques such as integrating the switch into CP output current branch [**40**] or using the cascode device as current mirror and using the mirroring device in Fig. 2.18 as switch [**45**].

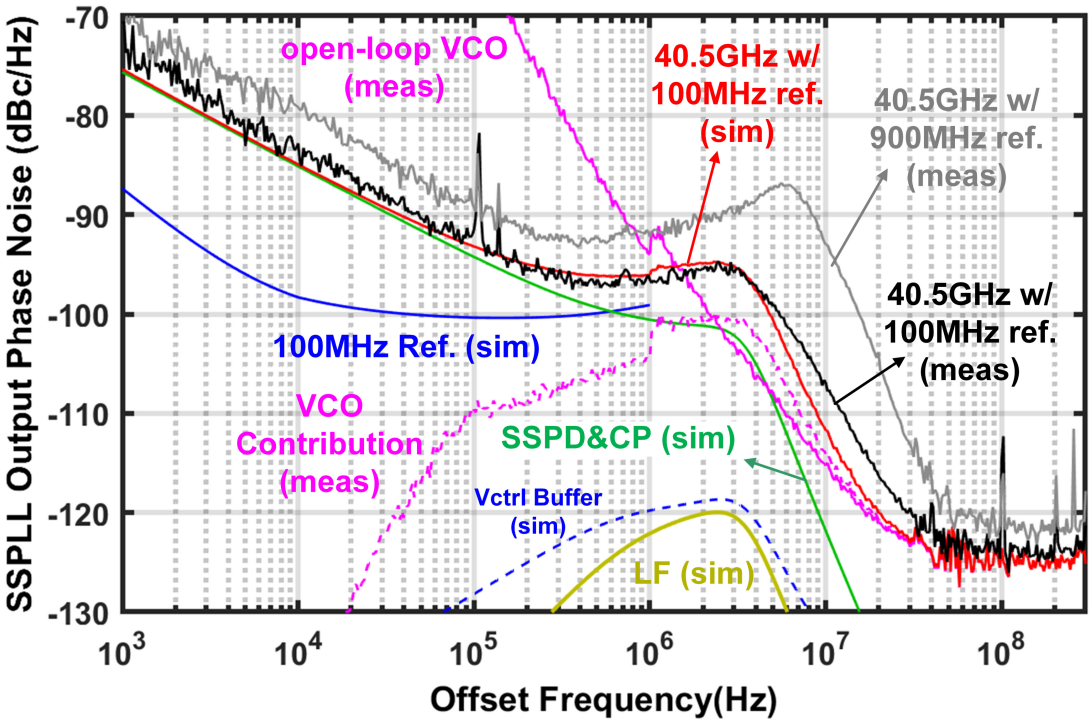


FIGURE 2.27. Simulated and measured SSPLL 40.5GHz output phase noise with each block's contributions at room temperature. Simulated 40.5GHz noise (red) with 100MHz reference is calculated with measured open-loop VCO noise (magenta). In comparison, noise with 900MHz reference (grey) in frequency acquisition is significantly higher than that with 100MHz reference (black).

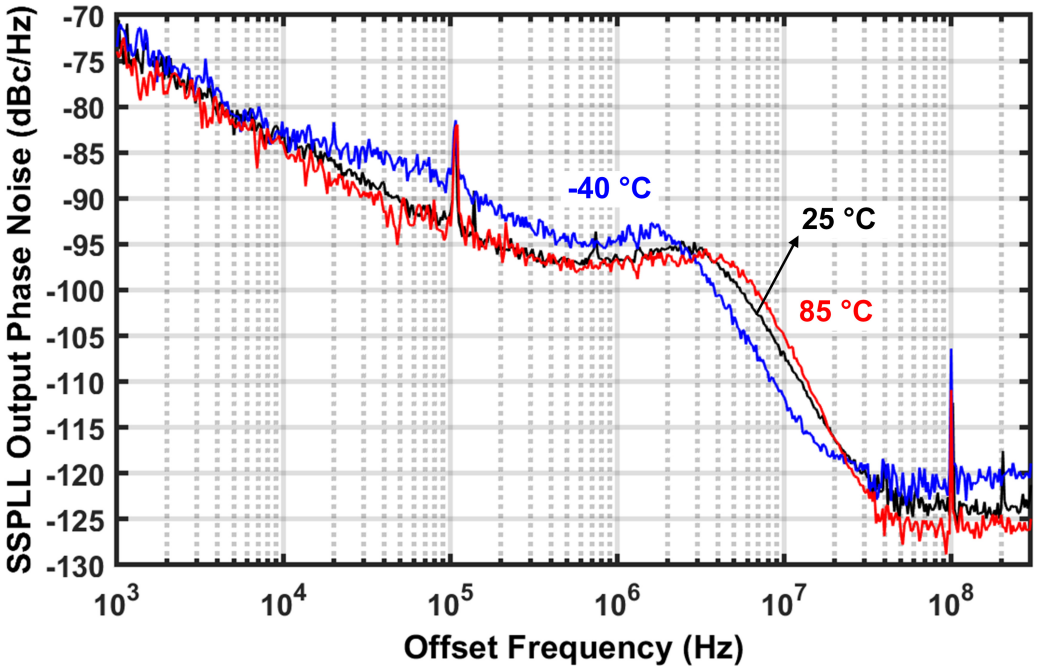


FIGURE 2.28. Measured SSPLL 40.5GHz output phase noise when locked to 100MHz reference under ambient temperatures of 25 °C, −40 °C and 85 °C.

Simulated and measured SSPLL output phase noise at room temperature is shown and compared in Fig. 2.27. The simulated 100MHz reference noise (blue) is achieved from crystal PN and inverter buffer chain added noise, and then scale up by $20log(405)$. Phase noise at 1MHz (in-band) and 10MHz (out-band) offsets are -96.6dBc/Hz and -106.9dBc/Hz, respectively. The integrated RMS jitter (10kHz to 100MHz) is 228fs. Measured HFR 900MHz RMS period jitter is 0.5ps and RMS cycle-to-cycle jitter is 0.8ps, which satisfy (2.10) and are low enough for accurate SSLD operation. Fig. 2.27 shows that, the PN with 100MHz reference (black) is 5dB (in-band) to 10dB (out-band) lower than the one with 900MHz reference (grey). This is expected because the cascaded PLL structure has added noise that is heavily contributed by the CP and the ring-VCO of the HFR. Moreover, the SSPLL's higher loop gain and bandwidth for the 900MHz reference configuration results in higher CP noise floor and total noise. The loop bandwidth with 100MHz reference configuration is around 3MHz, and is designed and optimized for noise performance as well as satisfying the requirement in (2.14). The loop bandwidth with 900MHz reference

configuration is around 6MHz to accommodate the high gain for fast frequency acquisition. The proposed SSPLL system can work across ambient temperature of $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. Phase noise with temperature variation is measured and provided in Fig. 2.28 by keeping the same biasing configurations as in room-temperature and varying the ambient temperature. It is observed that the loop gain and bandwidth change with respect to temperature. This is due to the variations of transistor's threshold voltage which affects the resistance/gain of the SSPD switch, the resistance of LF's poly resistor with negative temperature-coefficient, and the gain of the VCO buffers. The spurs at 107kHz and 138kHz are originated from the SSPLL input inverter DC biasing directly from the noisy power supply.

TABLE 2.2. Proposed SSPLL Performance Summary in Comparison with the State-of-the-art.

Ref.	**Topology**	**Tech. (nm)**	f_{ref} **(MHz)**	f_{out} **(GHz)**	**PN[a](dBc/Hz)**		σ_{rms} **(fs)**	**Ref.Spur (dBc)**	P_{DC} **(mW)**	**Area (mm^2)**	**FOM_1[b]**	**FOM_2[c]**
					1MHz	**10MHz**						
[**14**] JSSC'15	SSPLL	40	40	60	-95.4	-104.4	200	<-40	42	0.16	-234	-265.9
[**12**] JSSC'16	SSPLL	65	36/40	60	-95.4	-125.4	290	-73	32	0.7	-235.7	-267.5
[**16**] RFIC'17	PLL	250[d]	50	40	-100.6	-124.9	149	-73	323	0.45	-231.5	-260.5
[**19**] TMTT'17	PLL+SSPLL	65	230	28	-112.8	-121.8	79	-63	27	0.28	-247.7	-268.6
[**24**] ISSCC'18	PLL+ILFM	65	120	29	-99.1	-115.8	206	-83	36.4	0.95	-238.1	-262
[**46**] ISSCC'19	SS-DPLL	65	100	30	-97.1	-115.4	197.6	N/A	35	0.55	-238.6	-263.5
[**21**] TMTT'19	PLL+SSPLL	65	100	100	-93.6	-114.5	607	-43	57	0.88	-227	-257
[**47**] JSSC'19	SS-DPLL +ILFM	65	100	30	-102	-122	77	-58	41.8	0.32	-246	-270.6
[**48**] ISSCC'19	SSPLL	65	103	30	-109	-120	71	-63	15.3	0.24	-251	-275.2
[**49**] JSSC '20	Ref.SPLL +ILFM	45	80	36	-93.9	-108	251	-60	20.6	0.41	-238.9	-265.4
This Work	**SSPLL +SSLD**	**65**	**100**	**40.5**	**-96.6**	**-106.9**	**228**	**<-42**	**8.8[e]**	**0.6**	**-243.4**	**-269.5**

[a] Normalized to 40.5GHz
[b] FOM_1=20 log (jitter/1s) + 10 log (P_{DC}/1mW)
[c] FOM_2=20 log (jitter/1s) + 10 log (P_{DC}/1mW) + 10 log (f_{ref}/f_{out})
[d] 0.25 um BiCMOS
[e] Excluding the 0.75mW power of the V_{ctrl} buffer.

To verify the SSLD analog interface functionality, V_{det} is measured with different f_{out} values and shown in Fig. 2.29. f_{out} is manipulated by tuning V_{ctrl} on an open-loop VCO. As shown in Fig. 2.29: a) For f_{out} ≈40.5GHz, due to the open-loop VCO frequency instability and circuit noise, V_{det} is not exactly DC, but toggles at a sufficiently low frequency; b) When f_{out} is approximately 40.6GHz, 40.7GHz or 40.9GHz, although f_{det} is not exactly as calculated in Fig. 2.9, it is around or above 100MHz. This is sufficiently high to detect locking status and to enable the frequency acquisition process.

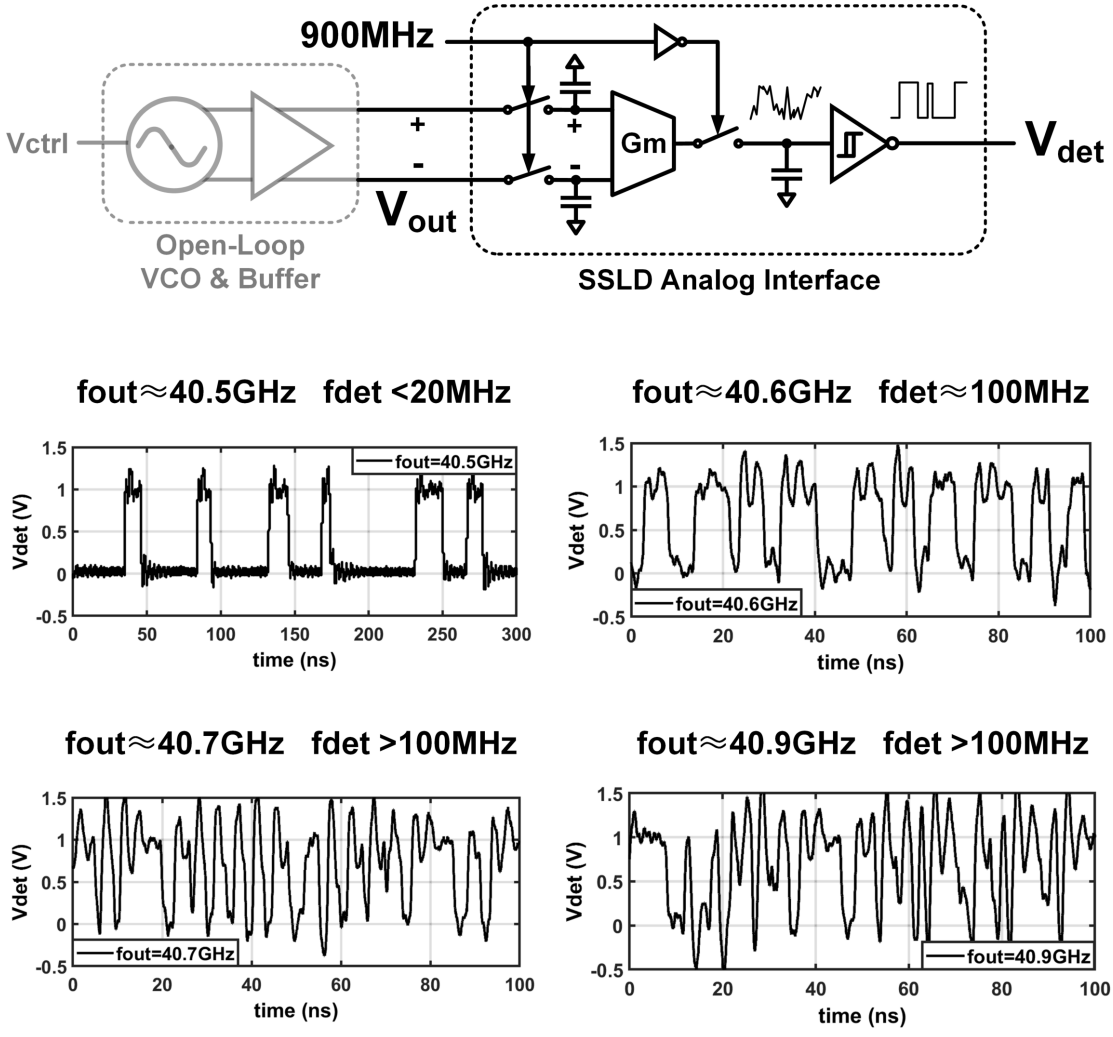


FIGURE 2.29. Measured SSLD analog interface output signal with different open-loop VCO frequencies.

The SSPLL's automatic lock detection and re-lock procedure is measured and shown in Fig. 2.30. First, the SSPLL loop is opened and V_{ctrl} is forced to be 300mV lower than the locked value to mimic an unlocked SSPLL. The gap of 300mV is chosen because it contains several V_{ctrl} values corresponding to wrong 100MHz harmonics. Next, we close the loop and examine the re-lock procedure by observing V_{ctrl} and reference switching signal FA_EN with oscilloscope. SSLD digital logic states are labeled according to Fig. 2.13. After the SSPLL loop is closed, the SSLD detects the unlock state. After a while, the SSLD is triggered to S2, setting FA_EN to 1 and switching 900MHz to the SSPLL for frequency acquisition. After the preset time T_1, SSLD enters state S3, setting FA_EN to 0 and switching 100MHz to the SSPLL for phase locking. After another preset time T_2, phase lock is achieved and SSLD enters S1. FA_EN remains at 0, meaning the SSPLL is locked to the 100MHz reference. Meanwhile, V_{ctrl} also settles at the value corresponding the correct 100MHz harmonic. From the zoomed-in figure in Fig. 2.30, it is observed that the maximum frequency deviation after reference switching is $|\Delta f_{out,max}| \approx 20MHz$. This deviation satisfies the design target in (2.14) and is small enough to avoid locking to wrong 100MHz harmonics.

Total power consumption of the chip is 8.83mW, out of which 4.24mW, 2.76mW and 1.83mW are consumed by SSPLL, HFR and SSLD, respectively. Power consumptions of blocks operating at mmWave are: 1.75mW for the VCO, 1.36mW for the middle buffer and 1.85mW for the two output buffers. The V_{ctrl} buffer in Fig. 2.18 consumes 0.75mW, which is excluded from the total power consumption since measurement shows it can be abandoned given the suspected VCO back-charging is not present in taped-out chips. Table 2.2 shows the measured performance summary of the proposed frequency synthesizer in comparison with the state-of-the-art. To the best of our knowledge, the proposed SSPLL with the novel SSLD has the lowest power consumption among 30GHz and above frequency synthesizers and the best figure of merit (FOM) among 40GHz to 60GHz frequency synthesizers with crystal references.

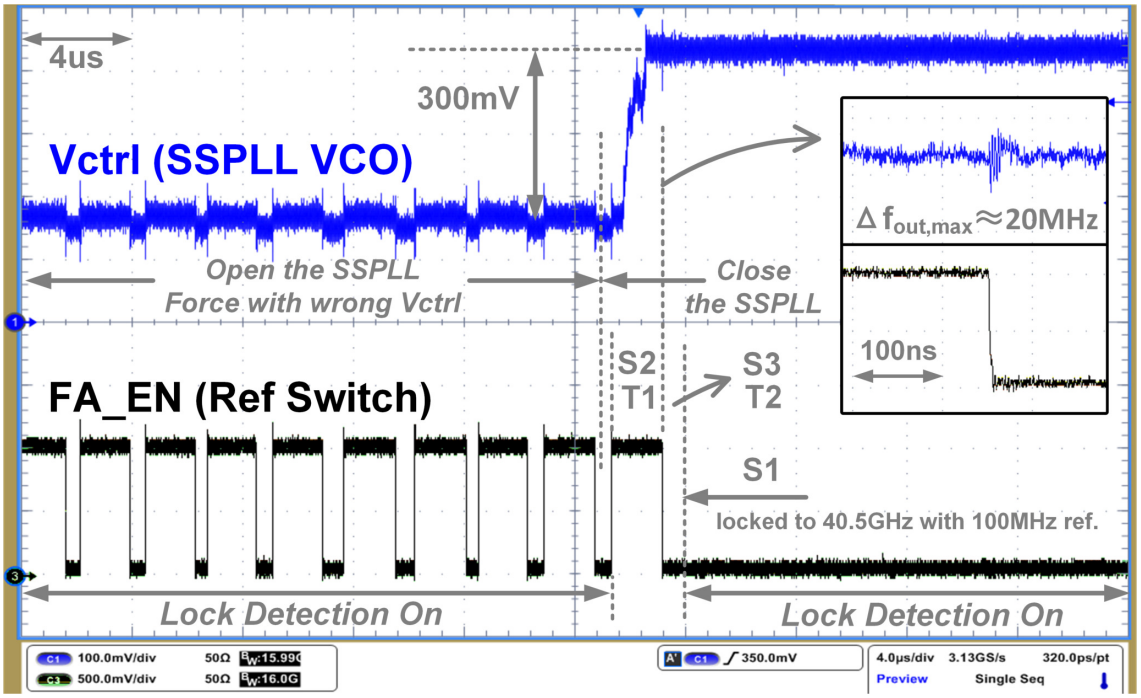


FIGURE 2.30. Measured automatic lock-detection and re-lock procedure of the proposed frequency synthesizer.

2.10. Conclusion & Outlook On Future Work

In this chapter, we propose a low-power and low-noise mmWave frequency synthesizer based on SSPLL and a novel SSLD. The 40.5GHz SSPLL system consumes 8.8mW, with 228fs RMS jitter, and can work reliably across a wide ambient temperature range from $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. Such a low system power consumption is contributed by the proposed low-power SSLD and the relatively low-frequency 900MHz generation PLL. The SSLD keeps monitoring the locking status of the SSPLL. When the SSPLL loses lock or locks to a wrong harmonic, the SSLD can automatically switch its reference to the 900MHz reference for frequency acquisition without using frequency dividers. Measured results verify that the proposed SSPLL achieves the lowest reported power consumption among 30GHz and above frequency synthesizers as well as low noise performance simultaneously. The proposed mmWave frequency synthesizer is a good candidate for low-power applications such as 5G/6G wireless communication user ends, IoT sensors and atomic clock excitation.

As communication systems urged by higher data rates from various emerging applications such as high-resolution virtual reality (VR) and augmented reality (AR), frequency synthesizers are stepping into high-mmWave and sub-THz bands above 100GHz. Although featured with intrinsic low in-band noise, SSPLL is faced with an obvious conundrum of how to realize the SSPD able to directly sample >100GHz signals. As discussed previously, using ILFMs to multiply the SSPLL frequency inevitably boosts in-band added noise. Hence, ILFM is not a good solution. Even with the more advanced semiconductor process nodes, shorter channel lengths, lower parasitic capacitance of transistors and higher transistor speed (f_T), directly sampling >100GHz signal induces significant loss and calls for power-hungry VCO buffers. Smart ways of mmWave and sub-THz signal sampling are becoming the grail in RF frequency synthesizer field.

CHAPTER 3

Charge-Pump Current Mismatch Compensation for SSPLL

3.1. Introduction

Phase-locked loops (PLL) that can lock with wide control voltage (V_{ctrl}) range of voltage-controlled oscillators (VCO) have various benefits. With integrated circuit advancing into short-channel low supply-voltage processes, analog blocks such as PLL charge pumps (CP) and VCO's designed for low-voltage and low-power operation face limited voltage headroom [**50**, **51**]. A wide V_{ctrl} locking range (LR) reduces design complexity within the limited headroom, and helps a PLL utilize more of its VCO's tuning range (TR) [**52**, **53**]. Moreover, individual calibration capacitor bank in VCO's resonant tank can cover more frequency with wider V_{ctrl} LR. Therefore, frequency overlap between adjacent banks and hence the total bank number can be reduced. Fewer banks and switches reduce loss in the VCO and increase power efficiency especially at millimeter-wave (mmWave) frequencies. In specialty applications such as PLL-based mmWave and Terahertz (THz) dielectric sensing, V_{ctrl} is a direct gauge of a material's complex permittivity [**6**]. Wider V_{ctrl} LR means wider sensing range and finer resolution.

In the past decade, sub-sampling PLL (SSPLL) becomes popular due to its intrinsic lower in-band phase noise (PN) than the frequency-divider based PLL counterparts [**10**]. However, in a practical PLL, V_{ctrl} LR is limited by charge pump output current mismatch mainly caused by channel-length modulation (CLM) on transistors. In traditional PLL's, this mismatch causes higher reference spur and CP gain distortion. In SSPLL's, this current mismatch not only induces CP input voltage offset, limiting the effective CP input range, but also significantly decreases the gain of sub-sampling phase detector (SSPD). Compensation techniques for traditional PLL's CP current mismatch have been developed in multiple structures [**54**, **55**, **56**, **57**, **58**, **59**], which use feedback loops to adjust the current biasing. However, unlike the CP's with static biasing in traditional PLL,

SSPLL CP output currents are controlled by the sampled signal that is changing widely especially during acquisition [**41**]. Therefore, existing CP compensations cannot be used in SSPLL.

In this chapter, a CP current mismatch compensation method for SSPLL is proposed. The compensated CP cancels the input offset and eliminates the SSPD gain degeneration without sacrificing SSPLL's low in-band PN performance. A 40.5GHz SSPLL with dividerless automatic frequency acquisition, 9.5mW power consumption, and minimum RMS jitter of 192fs is designed with the proposed compensated CP. Under 1V supply voltage, the compensated V_{ctrl} LR reaches 0.75V, extended by 50% from the uncompensated 0.5V range.

This chapter is organized as follows: The CLM effect on SSPLL CP and SSPLL performance is analyzed in Section 3.2. Next, we review the existing CP mismatch compensations for traditional PLL and their limitations in Section 3.3. Then, our proposed mismatch compensated CP for SSPLL is introduced in Section 3.4. In Section 3.5, the design of a low-power mmWave SSPLL with the proposed compensated CP is presented. The measurement results of the improved V_{ctrl} locking range with CP compensation, together with the whole SSPLL performance are provided in Section 3.6. After comparison with the state-of-the-art, we conclude our paper in Section 3.7.

3.2. Effects of CP Current Mismatch on SSPLL

Fig. 3.1 shows an SSPLL and its CP structure. At the input of the CP is a common-mode DC biasing with sampled differential voltage, V_{sam}, from the VCO output buffer. CP converts V_{sam} into output currents I_{up} and I_{dn}. Depending on the V_{ctrl} value, drain-source voltages, $V_{SD,up}$ and $V_{DS,dn}$ of transistors M_{up} and M_{dn} are different. With CLM [**60**], the CP currents are:

$$\begin{cases} I_{up} = N \cdot \left(I_0' + \frac{1}{2} V_{sam} g_{m,CP}\right) \cdot (1 + \lambda \cdot \Delta V_{SD,up}) \ , \\ I_{dn} = N \cdot \left(I_0' - \frac{1}{2} V_{sam} g_{m,CP}\right) \cdot (1 + \lambda \cdot \Delta V_{DS,dn}) \ , \end{cases} \tag{3.1}$$

where N is the current mirroring ratio from the CP input stage to the output branch, I_0' is the static biasing current of the CP input differential stage, $g_{m,CP}$ is the CP input stage transconductance, λ is the CLM parameter assumed the same for NMOS and PMOS for simplicity. $\Delta V_{SD,up} = V_{SD,up} - 0.5V_{DD}$ and $\Delta V_{DS,dn} = V_{DS,dn} - 0.5V_{DD}$ are the CP output branch transistors' drain-source

voltage deviation from the standard value of $0.5V_{DD}$, assuming CP supply voltage is V_{DD} and CP output voltage is V_{ctrl} when output switches are on. Defining $\Delta V_{ctrl} = V_{ctrl} - 0.5V_{DD}$, CP output branch biasing current $I_0 = N \cdot I_0'$ and CP total transconductance $G_{m,CP} = N \cdot g_{m,CP}$, the CP net output current $I_{out} = I_{up} - I_{dn}$ can be calculated as:

$$I_{out} = V_{sam} G_{m,CP} - 2I_0 \lambda \Delta V_{ctrl} \ . \tag{3.2}$$

From (3.2) it is observed that, CLM induces a current mismatch between I_{up} and I_{dn} equal to the second term, $\Delta I = -2I_0 \lambda \Delta V_{ctrl}$. As can be seen in the following analysis, this mismatch induces CP input offset voltage, causes significant gain degeneration in SSPD and limits the V_{ctrl} LR. Therefore,the mismatch needs to be compensated, especially in platforms that CLM is substantial.

In an ideal locked SSPLL, in order to make V_{ctrl} stable (i.e. $I_{out} = 0$), V_{sam} value at each sampling moment has to be 0. However, (3.2) shows that CLM induces a current mismatch between I_{up} and I_{dn}. Hence, even when V_{sam} is 0, $I_{out} = \Delta I$ is a function of V_{ctrl} and might not be 0. This means the current mismatch creates an effective CP input offset voltage, $V_{os} = \Delta I / G_{m,CP}$. For a stable V_{ctrl} and a locked frequency, the effective CP input $V_{sam,eff} = V_{sam} + V_{os}$ must be zero, so that $I_{out} = 0$. As a result, V_{sam} becomes $-V_{os}$, to compensate V_{os} at any sub-sampling moment.

Fig. 3.2 illustrates the different cases of SSPD and CP operation in a locked SSPLL. $V_{sam} = A_{sam} sin(\phi)$, where A_{sam} is the amplitude and ϕ is the phase of V_{sam} with respect to the sampling edge. Case 1 corresponds to an ideal CP without CLM and thus $V_{os} = 0$. The SSPD gain is $K_{SSPD} = \partial V_{sam} / \partial \phi = A_{sam} \cos \phi$. Sub-sampling at $V_{sam} = 0$ (i.e. $\phi = 0$), allows the SSPD to have a maximum gain of $K_{SSPD,max} = A_{sam}$. Given that A_{sam} is typically small due to high-frequency circuit loss and low-power buffer design, especially at mmWave frequencies, sampling with highest possible gain is always desired to achieve enough SSPLL loop gain. In Case 2, for a CP with CLM effect, a high V_{ctrl} induces a negative V_{os}, leaving hardly any positive input range ($V_{up,max}$) for the CP to further increase V_{ctrl}. Similarly, in Case 3, a low V_{ctrl} prevents CP from locking V_{ctrl} to lower values with the limited negative input range of $V_{dn,max}$. Hence, CLM will significantly

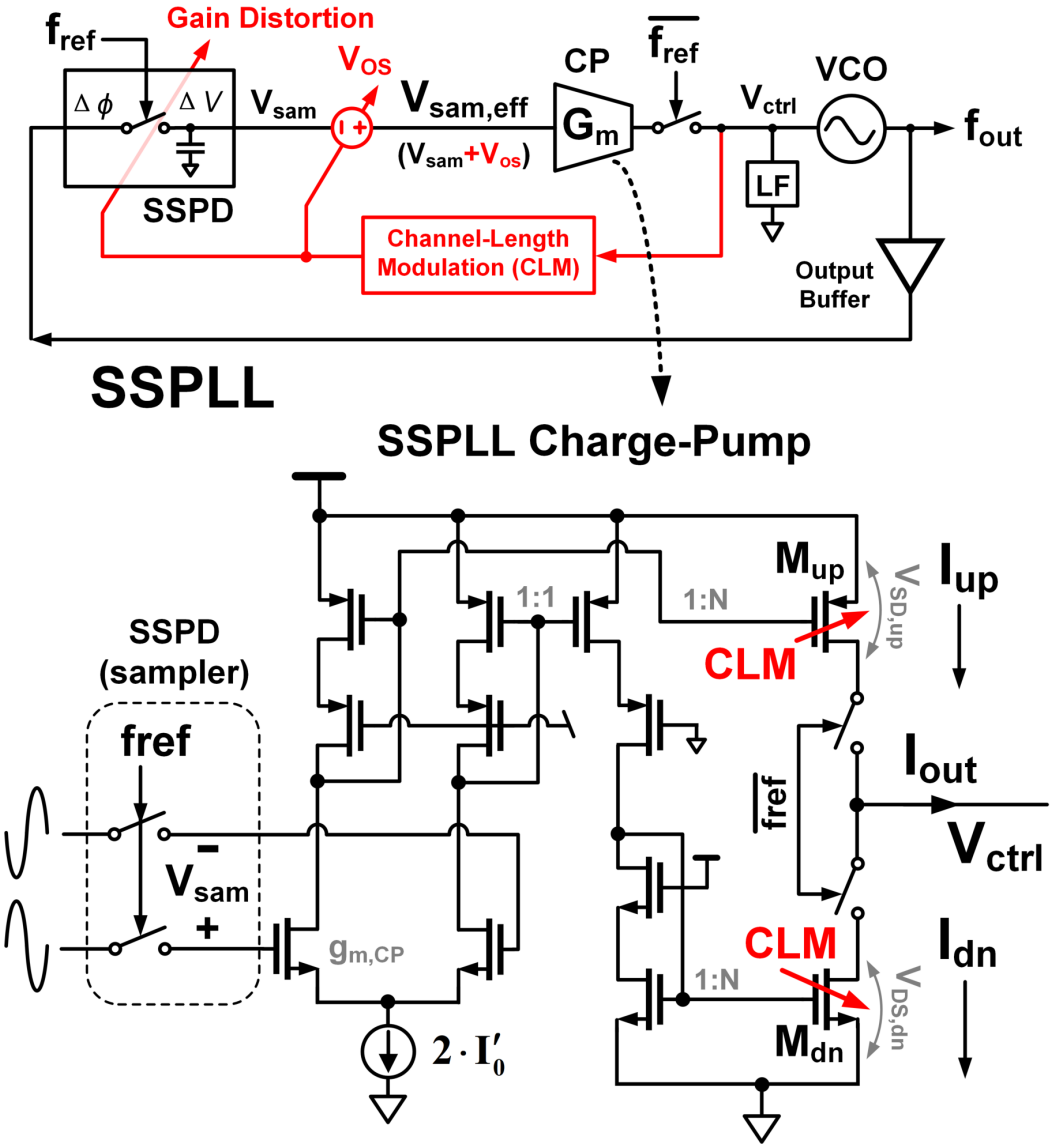


FIGURE 3.1. SSPLL structure with CP suffering CLM effect.

decrease the LR of SSPLL's V_{ctrl}. Moreover, for both Case 2 & 3, SSPD gain decreases because the non-zero V_{sam} and ϕ generate lower K_{SSPD} compared to that in Case 1. This SSPD gain distortion decreases SSPLL loop gain and bandwidth, and thus degrades SSPLL PN, jitter and loop stability.

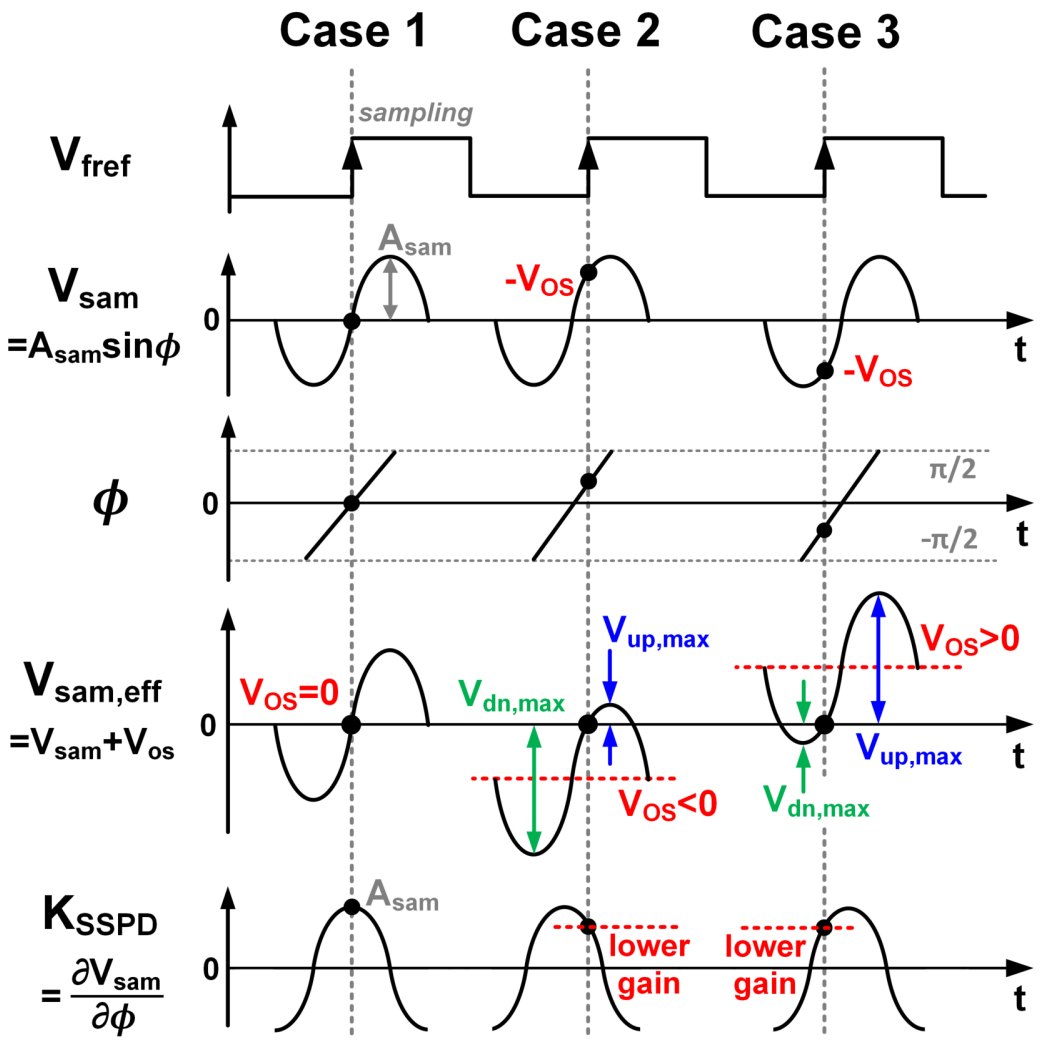


FIGURE 3.2. CLM effect decreases SSPD gain and creates an offset voltage at CP input, limiting V_{ctrl} locking range. Case 1: ideal CP without CLM; Case 2 & 3: CP with CLM.

Other factors can exacerbate the CLM effect. In a cascaded SSPLL such as [**19**] with high-frequency intermediate reference, or in an SSPLL with very narrow sampling pulses, CP needs to have faster response and higher bandwidth. In these designs, shorter-channel devices with worse CLM effect (larger λ) are adopted, resulting in even lower V_{ctrl} LR and SSPD gain. Furthermore, in low-power SSPLL's [**15**], VCO output buffers produce small A_{sam}, making V_{os} comparable to A_{sam} when CLM effect is significant, further limiting V_{ctrl} LR.

3.3. Limitation of Existing PLL CP Mismatch Compensation Techniques

Various CP current mismatch compensation structures have been proposed for traditional phase-frequency detector (PFD) based PLL's [**54**, **55**, **56**, **57**, **58**]. The compensation structures are all based on feedback loops as shown in Fig. 3.3. CP output current I_{up} and I_{dn} are generated from a constant biasing current I_{bias}. With different V_{ctrl} values, I_{up} may not be equal to I_{dn} due to CLM. A compensation feedback consisting of an amplifier (green) and a dummy current branch, with transistor sizing and biasings identical to the output branch, is built to ensure $I_{up} = I_{dn}$ for any V_{ctrl} value. In a traditional PLL, CP gain is implemented by controlling the switching signals V_{up} and V_{dn}, and the ON time of CP currents, I_{up} and I_{dn}. The net CP output current, I_{cp}, equals to I_{up} or I_{dn} depending on the values of V_{up} and V_{dn}. Moreover, I_{up} and I_{dn} can only be either zero or a constant value generated by I_{bias}. These features of traditional CP make the compensation feedback easy to implement. However, as shown in Fig. 3.1, SSPLL CP currents are differentially produced by a varying voltage V_{sam}. For example, when $V_{sam} > 0$, I_{up} increases while I_{dn} decreases. Thus, existing CP current mismatch compensation methods cannot be applied to SSPLL CP, and a new method is needed. Furthermore, traditional PLL's CP current mismatch only induces higher reference spur, without affecting the PFD gain [**38**]. This is because PFD converts phase difference into time with a constant gain [**38**, **39**], while SSPLL's SSPD converts phase difference into voltage with a gain that is a function of the mismatch as mentioned in Fig 3.2. Hence, CP mismatch compensation is more critical for SSPLL compared with traditional PLL.

3.4. Proposed Mismatch Compensation for SSPLL CP

3.4.1. Circuit Implementation. Fig. 3.4 shows the proposed compensation method for SSPLL CP mismatch. This compensation is to make sure when $V_{sam} = 0$, I_{out} is also 0 for any V_{ctrl} value. In other words, the compensation ensures $V_{os} = 0$ so that $V_{sam} = V_{sam,eff}$. A dummy charge pump (CP_{dum}) is designed with the same transistor sizes and layouts of the CP, to accurately mimic the CLM effect on output currents, except that CP_{dum} output branch current is mirrored by a factor of 1, instead of N, to save power. CP_{dum} input has the same DC biasing of the CP input, so that the CP and the CP_{dum} output biasing currents are $I_0 = N \cdot I_{0,dum}$ and $I_{0,dum}$,

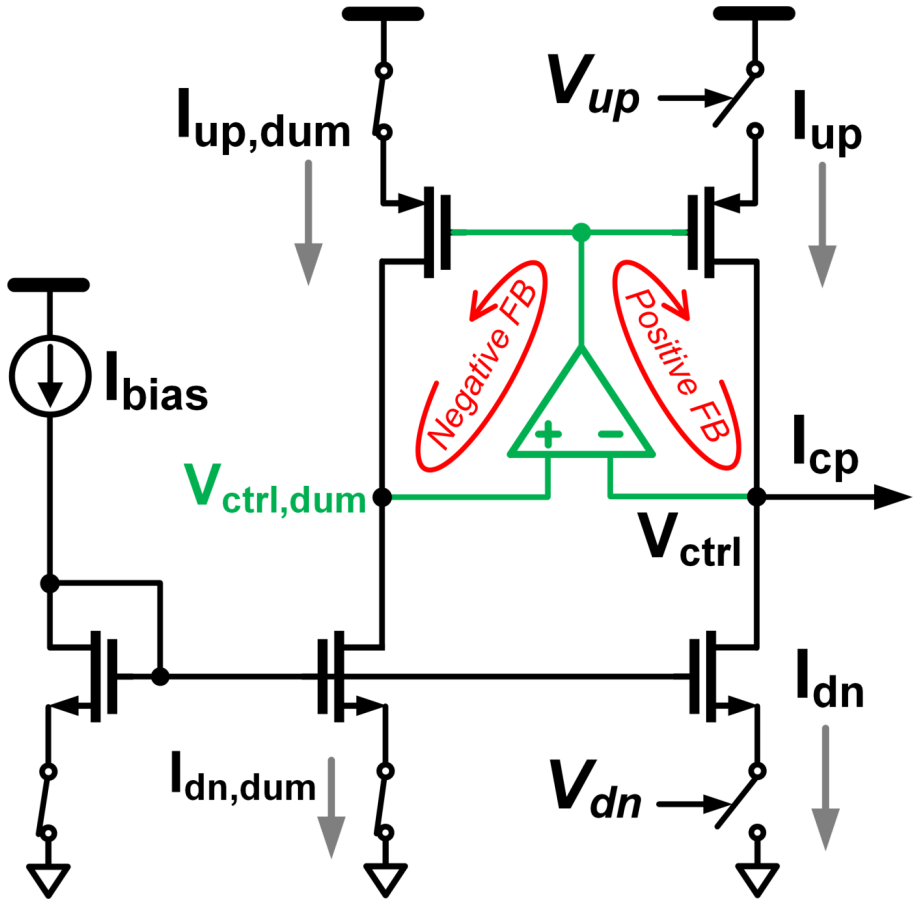


FIGURE 3.3. Current mismatch compensation structure for traditional PLL charge pump.

respectively. This input biasing is the output DC voltage of the VCO buffer, $V_{out,DC}$. CP_{dum} output voltage, $V_{ctrl,dum}$, is forced to follow V_{ctrl} by a negative feedback shown in green. The feedback contains an amplifier driving a pair of identical transconductive current sources $G_{m,C1}$ and $G_{m,C2}$. The amplifier is designed with rail-to-rail input range to accommodate wide V_{ctrl} value. $G_{m,C2}$ drains or sinks a compensation current $I_{comp,dum}$ to control $I_{dn,dum}$ and ensures $I_{up,dum}$=$I_{dn,dum}$. Meanwhile, $G_{m,C1}$ produces a current I_{comp}, equal to $I_{comp,dum}$, to adjust the CP biasing. When $V_{sam} = 0$, CP and CP_{dum} have the same unit biasing condition and are compensated in a same way. Since the compensation makes $I_{up,dum}$=$I_{dn,dum}$ and $V_{ctrl,dum}$=V_{ctrl}, it also ensures I_{up}=I_{dn} for any V_{ctrl} as long as $V_{sam} = 0$. Consequently, current mismatch and the effective V_{os} in CP, together with SSPD gain distortion, are cancelled.

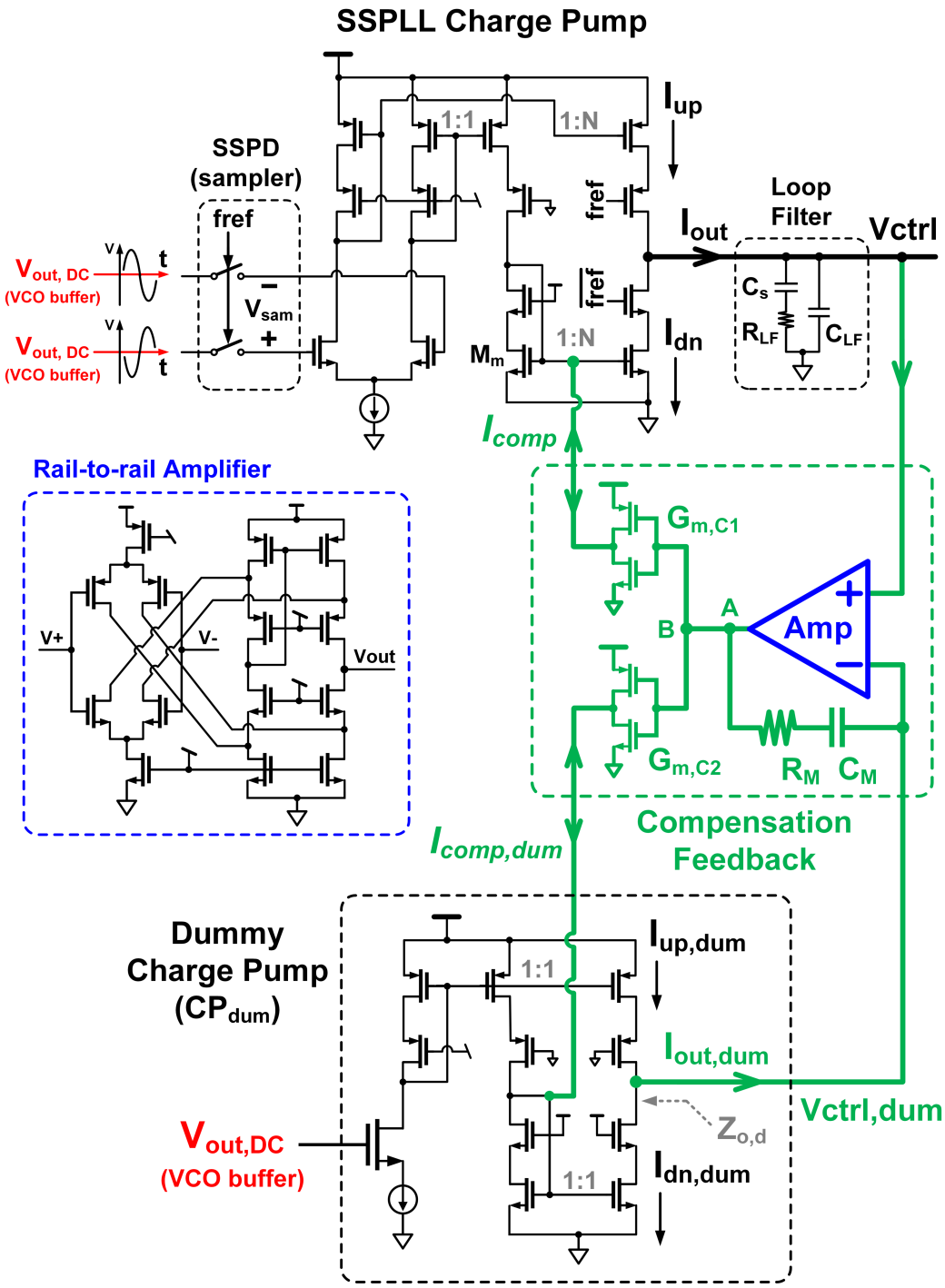
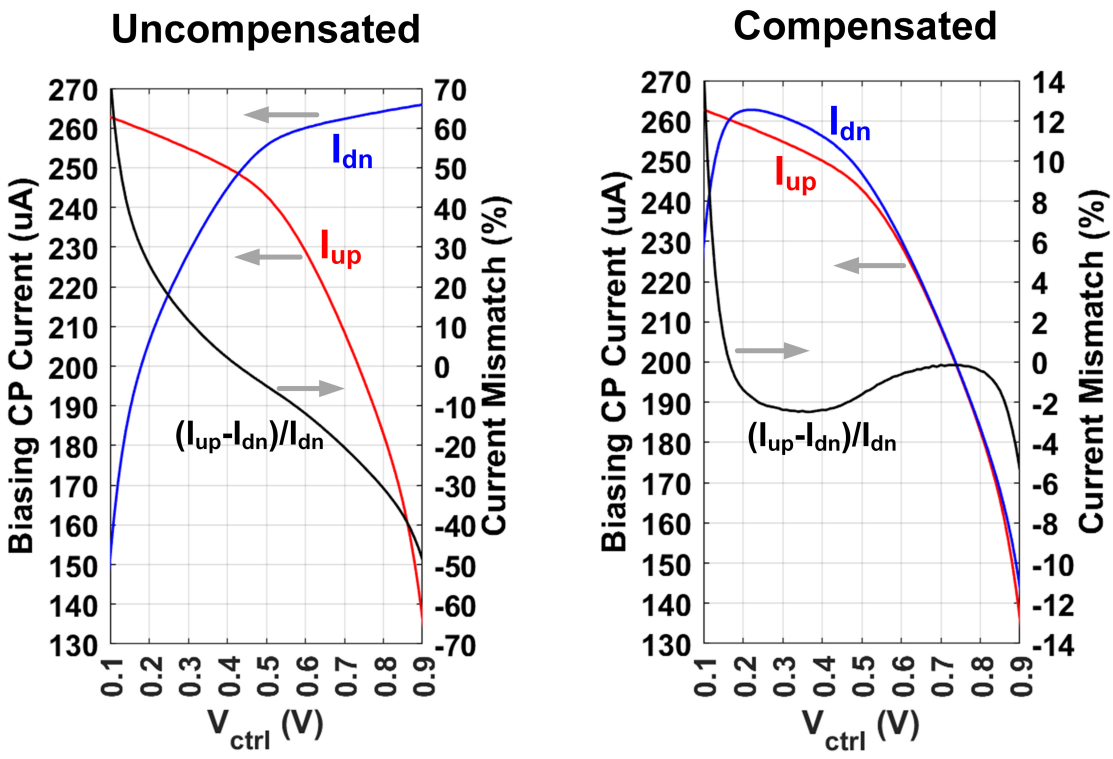


FIGURE 3.4. Proposed mismatch-compensated CP for SSPLL.



(a) (b)

FIGURE 3.5. Simulated SSPLL CP static biasing currents and CLM-induced mismatch, with CP input $V_{sam} = 0V$: (a) Without compensation, significant current mismatch will induce large V_{os} at CP input, decreasing SSPD gain and limiting CP operation range; (b) With the proposed compensation network, biasing current mismatch and hence V_{os} are ensured to be small across a wide range of CP output voltage V_{ctrl}.

With the mismatch compensation feedback, the CP net output current can be calculated based on (3.2) as:

$$I_{out} = V_{sam} \cdot G_{m,CP} + \Delta I - I_{comp} \cdot N(1 + \lambda \Delta V_{ctrl}) \ , \tag{3.3}$$

where $\Delta I = -2I_0 \lambda \Delta V_{ctrl}$. Because transistors in CP_{dum} are identical to those in CP, $I_{out,dum}$ can be evaluated from (3.3) with $V_{sam} = 0$ and $N = 1$. In steady state, $I_{out,dum} = \Delta I_{dum} - I_{comp,dum} \cdot (1 + \lambda \Delta V_{ctrl,dum}) = 0$. Due to the feedback loop, identical sizing and identical $G_{m,C1}$

and $G_{m,C2}$, it is ensured that $\Delta I_{dum} = \Delta I/N$, $I_{comp,dum} = I_{comp}$ and $V_{ctrl,dum} = V_{ctrl}$. Hence, $\Delta I - I_{comp} \cdot N(1 + \lambda \Delta V_{ctrl}) = 0$ and the compensated CP output current becomes: $I_{out} = V_{sam} \cdot G_{m,CP}$. This means the compensation current, I_{comp}, cancels the mismatch current ΔI in CP, and as a result the CP input offset voltage and SSPD gain degeneration, are eliminated.

Fig. 3.5 compares the simulated SSPLL CP current mismatch with and without the proposed compensation network. Within the V_{ctrl} range of 0.1 to 0.9V, which is reasonable for CP output transistor to operate, the uncompensated current mismatch spans from -50% to 70% as shown in Fig. 3.5(a), while the compensated mismatch is reduced to -4% to 14% as shown in Fig. 3.5(b).

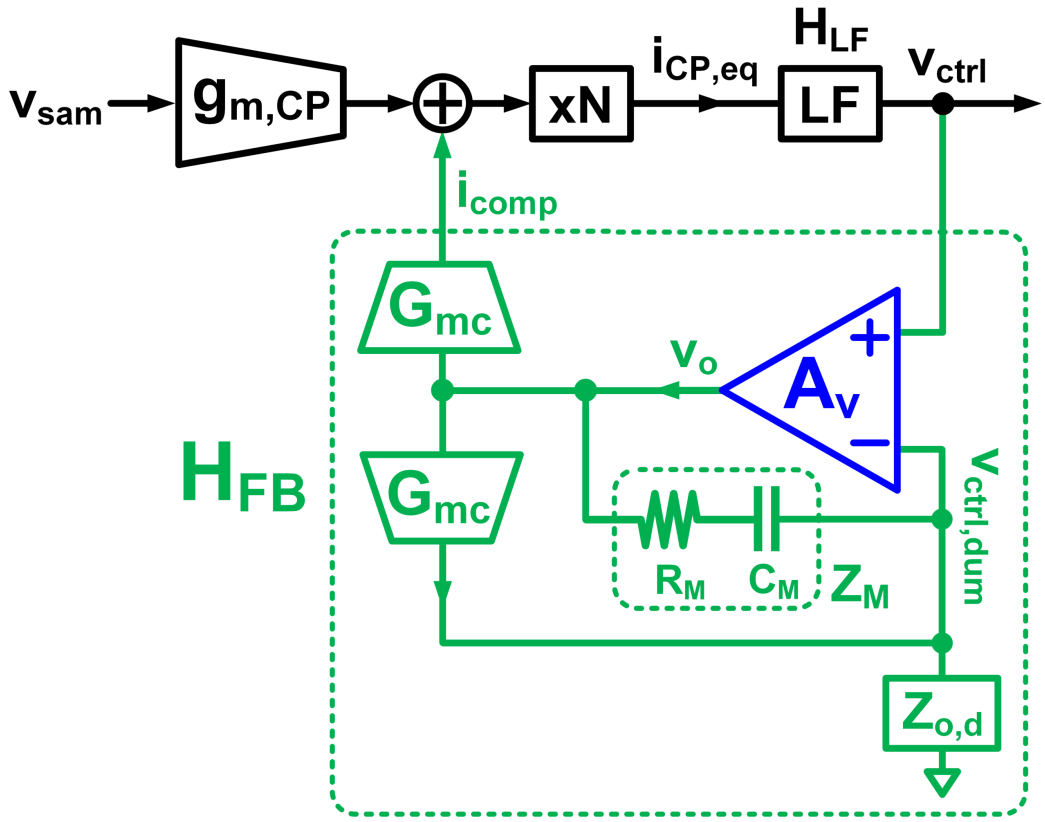


FIGURE 3.6. Block diagram of the proposed CP with mismatch compensation and the ensuing LF.

3.4.2. Transfer Function of the Proposed CP. To derive the transfer function of the proposed compensated CP, LF must be included since its filtered output, V_{ctrl}, is the input of the

compensation network. The block diagram of the proposed CP with compensation and the LF is shown in Fig. 3.6. In this model, the rail-to-rail amplifier (blue) voltage gain is A_V, and the signal path from amplifier output, V_o, to CP output current has an equivalent transconductance of $N \cdot G_{mc}$, where $G_{mc} = G_{m,C1} = G_{m,C2}$. The signal path from amplifier output to dummy CP output is a transconductor with gain of G_{mc} loaded with the CP_{dum} output impedance, $Z_{o,d}$.

With the compensation feedback transfer function, $H_{FB}(s)$, derived in Appendix B, we can achieve the total equivalent transfer function of the proposed CP together with the LF from Fig. 3.6 as:

$$H_{eq}(s) = \frac{v_{ctrl}}{v_{sam}} = \frac{N \cdot g_{m,CP} \cdot H_{LF}}{1 - N \cdot H_{LF} H_{FB}} \ . \tag{3.4}$$

Given that the CP transconductance is $G_{m,CP} = N \cdot g_{m,CP}$, (3.4) can be rearranged into a more straightforward model as shown in Fig. 3.7 for easier analysis, especially for analyzing noise behavior in Section 3.4.4. It consists of a CP without CLM effect, a shaping block induced by compensation, and an LF. The shaping block transfer function, $H_{SP}(s)$, can be derived as:

$$H_{SP}(s) = \frac{H_{eq}}{G_{m,CP} H_{LF}} = \frac{1}{1 - N \cdot H_{LF} H_{FB}} \ . \tag{3.5}$$

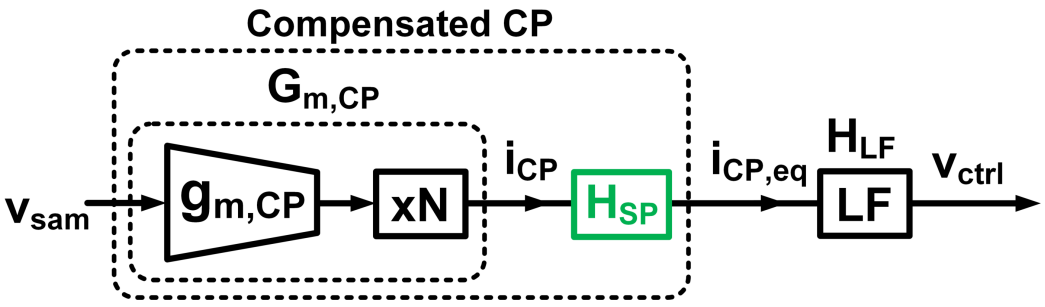


FIGURE 3.7. Rearranged block diagram of the proposed CP with compensation and LF.

3.4.3. Stability Analysis. Unlike the traditional PLL CP, I_{out} of SSPLL CP is controlled by input voltage V_{sam} in time-domain as illustrated in Fig. 3.8. V_{sam} is periodically sampled and held by reference V_{fref}. During "sample", CP output switches are turned off, I_{out} is disconnected from LF and V_{ctrl} keeps its prior value as shown in Fig. 3.8. During "hold", V_{sam} keeps its sampled value, I_{out} is generated as shown in (3.2) and fed into LF to change V_{ctrl}. For designing the CP compensation, we must make sure that: 1) $V_{ctrl,dum}$ follows V_{ctrl} fast enough for timely compensation. This is done by designing the compensation loop with high enough gain and bandwidth, and 2) The compensation must be stable during operation. This is ensured by adding Miller compensation resistor R_M and capacitor C_M for good phase margin. The bandwidth of the compensation loop doesn't have to be as wide as the frequency of the SSPLL reference. During frequency acquisition, V_{ctrl} changes abruptly at each sampling edge as shown in Fig. 3.11, if $V_{ctrl,dum}$ follows the average value of V_{ctrl}, instead of the instantaneous value, the current mismatch will be compensated.

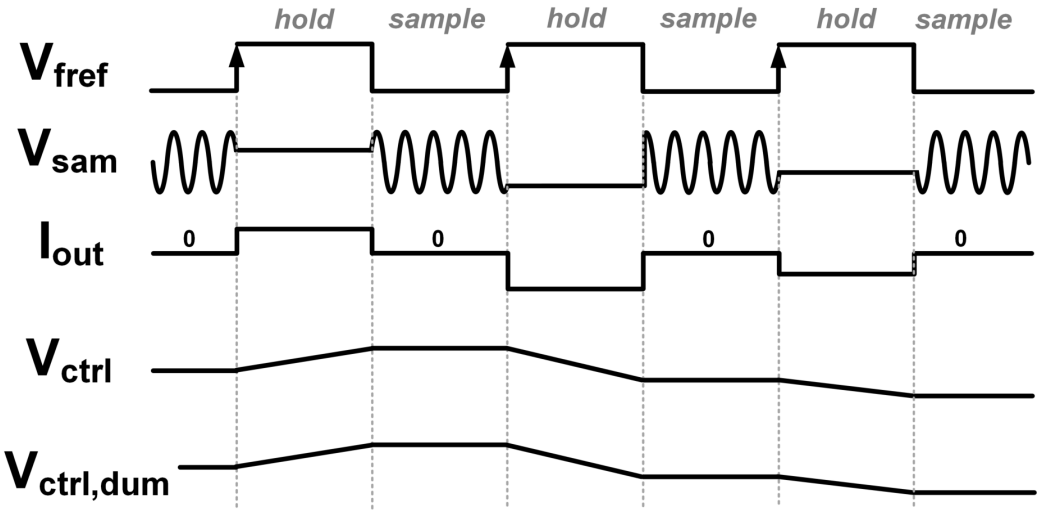


FIGURE 3.8. Transient illustration of SSPLL CP signals.

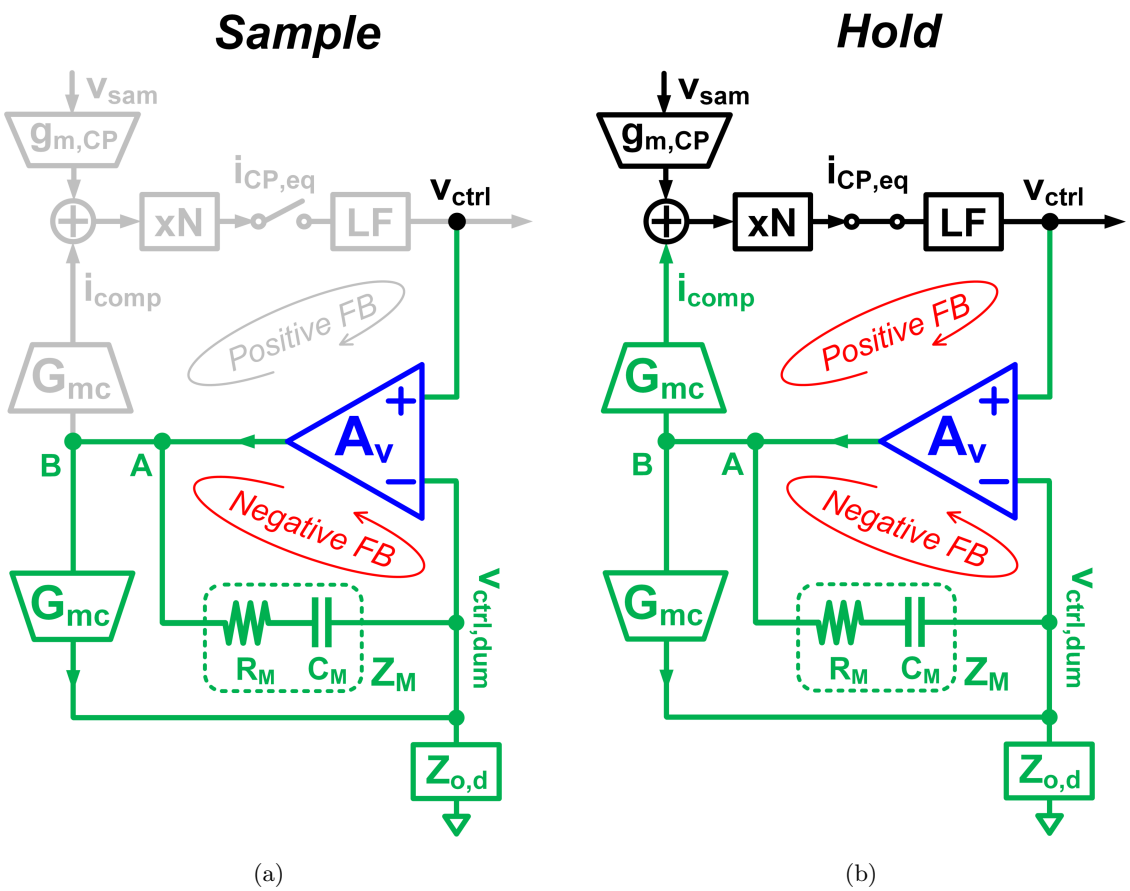
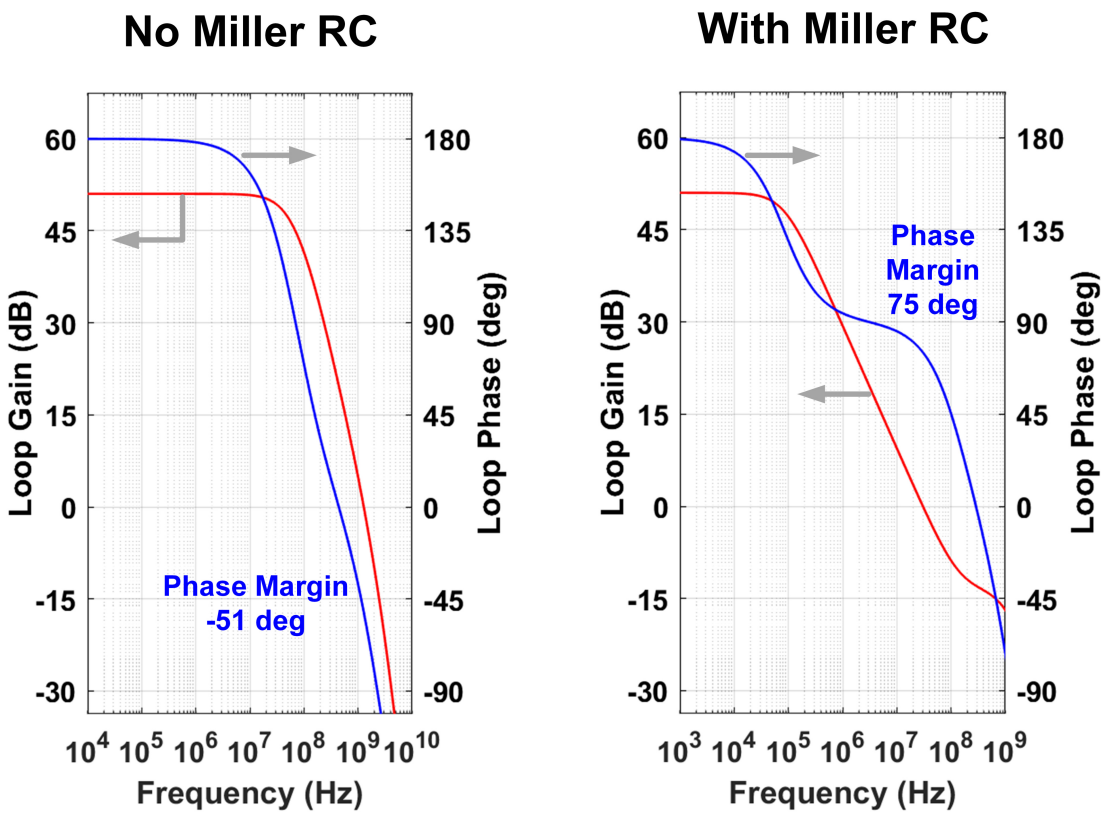


FIGURE 3.9. CP compensation circuit model for stability analysis: (a) During "sample" period in Fig. 3.8, when CP and LF are disconnected and V_{ctrl} keeps its value; (b) During "hold" period in Fig. 3.8, when CP and LF are connected and V_{ctrl} changes its value.

Fig. 3.9 shows the equivalent block diagram of the proposed CP compensation network for "sample" and "hold" periods. It is observed from Fig. 3.9 that, similar to the traditional CP compensation in Fig. 3.3, the proposed compensation establishes a negative and a positive feedback loops. During "sample" period shown in Fig. 3.9(a), the positive feedback is disabled since CP and LF are disconnected, and stability can be simply achieved with Miller compensation. However, during "hold" period shown in Fig. 3.9(b), both the positive and negative feedback loops operate simultaneously. To ensure stable operation, overall loop gain and phase change of the dual-loop network should satisfy the Barkhausen stability criterion [**61**]. Since the positive and negative

feedback loops share the same signal path from node A to node B labeled in Fig. 3.9, a probe can be inserted between A and B to simulate the network's loop gain, phase and stability [**62**, **63**].



(a) (b)

FIGURE 3.10. Simulated CP compensation network loop stability and phase margin during "hold" period: (a) Without Miller compensation, the CP compensation network is not stable; (b) With Miller compensation, the CP compensation network is stabilized with good phase margin.

Fig. 3.10 shows the simulated CP network stability and phase margin during "hold" period, with and without Miller compensation. It is observed that the Miller compensation stabilizes the network and delivers a high phase margin of 75 degree. To verify the loop stability, transient simulation of the SSPLL with the proposed CP compensation is performed. Fig. 3.11 shows the simulated results during the SSPLL's frequency acquisition period, in which V_{ctrl} moves up to lock to the correct value. It can be observed that, $V_{ctrl,dum}$ closely follows V_{ctrl} in a stable fashion.

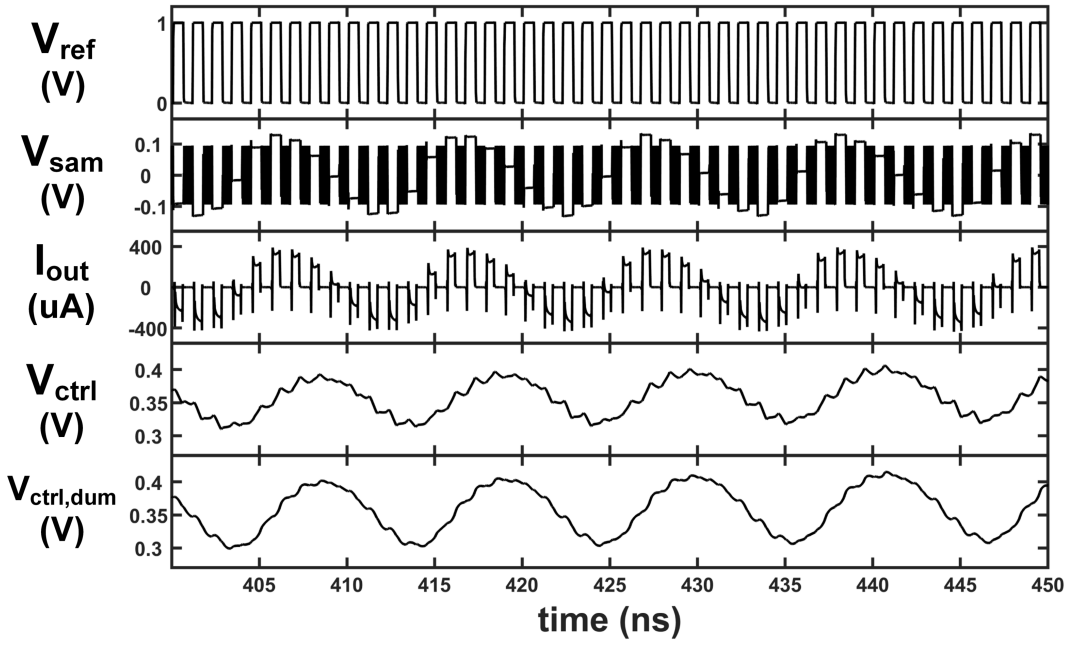


FIGURE 3.11. Simulated transient waveforms of the SSPLL with CP compensation during frequency acquisition.

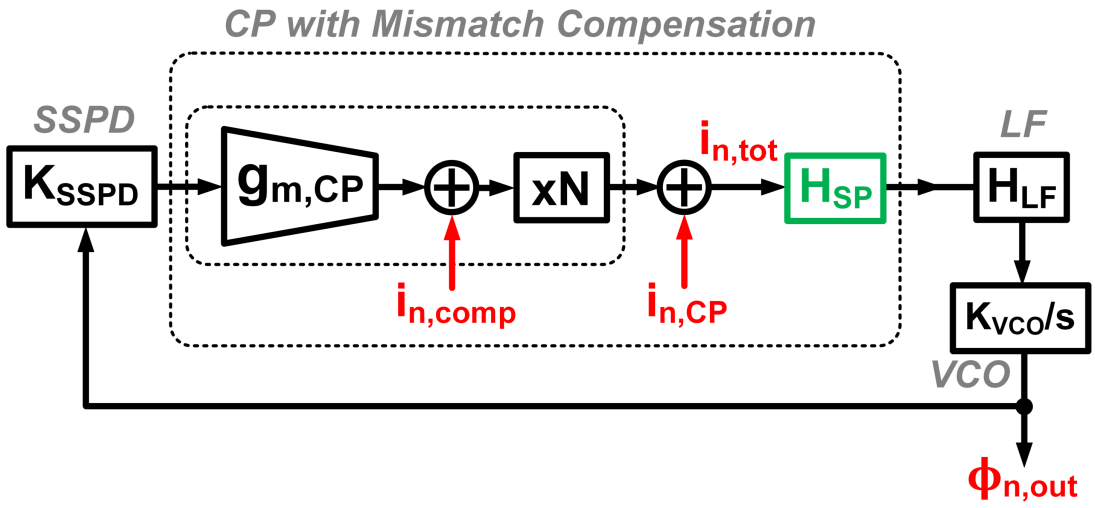


FIGURE 3.12. Noise sources and circuit model for the CP compensation.

3.4.4. Noise Analysis. The proposed compensation structure contains feedback loops and adds new noise into the SSPLL. To ensure the compensation cancels CP current mismatch without sacrificing SSPLL's low in-band noise feature, we need to evaluate the noise contribution of the compensated CP. Fig. 3.12 shows the SSPLL block diagram with the proposed compensated CP for noise analysis.

The compensation structure affects noise in two ways: 1) The compensation network shapes the CP output noise current $i_{n,CP}$, and 2) The compensation circuit adds output-referred current noise, $i_{n,comp}$, to the SSPLL. Since these two noise sources are uncorrelated, the total CP output noise current power before shaping, $i^2_{n,tot}$, is:

$$i^2_{n,tot} = i^2_{n,CP} + N^2 i^2_{n,comp} \ . \tag{3.6}$$

At low frequencies, $i_{n,comp}$ is mainly contributed by the CP_{dum} devices' flicker noise, which is comparable to its counterpart in CP due to the identical transistor sizes. At high frequencies, $i_{n,comp}$ is filtered by the SSPLL loop as will be analyzed later.

The noise transfer function from $i_{n,tot}$ to SSPLL output phase noise $\phi_{n,out}$ can be derived from Fig. 3.12 as:

$$H_{n,CP} = \frac{\phi_{n,out}}{i_{n,tot}} = \frac{H_{SP}H_{LF}K_{VCO}/s}{1 + K_{SSPD}G'_{m,CP}H_{SP}H_{LF}K_{VCO}/s} \ , \tag{3.7}$$

where $G'_{m,CP} = (\tau_{pul}/T_{ref})G_{m,CP}$, τ_{pul} is the SSPD switch-on pulse width ($\tau_{pul} = 0.5T_{ref}$ in our design) and T_{ref} is the SSPLL reference signal period. Assuming the SSPLL loop bandwidth is $\omega_{BW} \approx \omega_{LF} = 1/(R_{LF}C_{LF})$, we can evaluate the CP-induced phase noise as:

$$\phi^2_{n,out}(s) \approx \begin{cases} i^2_{n,tot}/(K_{SSPD}G'_{m,CP})^2 \ , & \omega < \omega_{BW} \\ i^2_{n,tot}(H_{SP}H_{LF}K_{VCO}/s)^2 \ . & \omega > \omega_{BW} \end{cases} \tag{3.8}$$

Comparing (3.8) with its counterpart without CP compensation (i.e. $H_{SP} = 1$), we can conclude that CP-induced in-band noise is processed in the same way as in a normal SSPLL and won't be boosted by the compensation network. Moreover, with (3.5) and (B.3) we can determine that $|H_{SP}| \approx 1$ for $\omega > \omega_{BW}$. Hence, the out-band CP noise is low-pass filtered as in an SSPLL without CP compensation. This is verified by the measurement results and shown with the simulated results (solid and dashed blue lines) in Fig. 3.18 provided in Section 3.6.

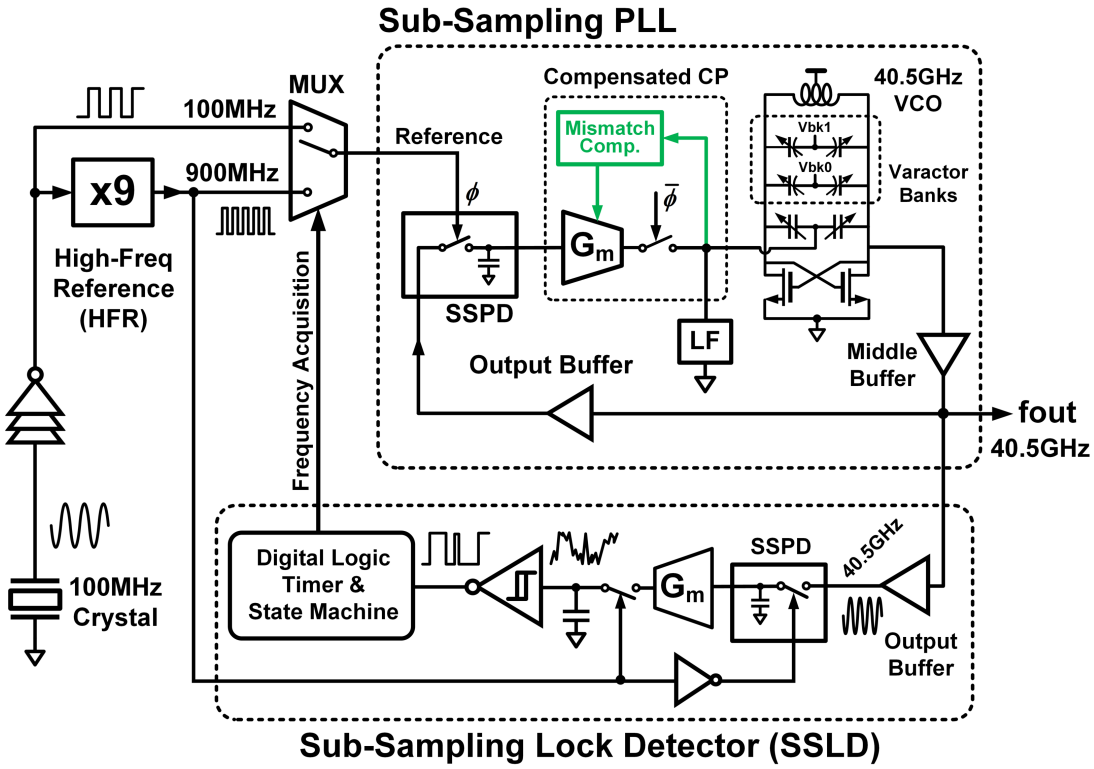


FIGURE 3.13. Prototype low-power SSPLL with proposed compensated CP.

3.5. Prototype 40.5GHz SSPLL with Proposed CP Compensation

A low-power 40.5GHz SSPLL is designed with the proposed CP compensation structure as shown in Fig. 3.13. Instead of using traditional frequency-locking loop (FLL), dividerless sub-sampling lock detector (SSLD) along with a high-frequency reference (HFR) are employed for frequency-acquisition to achieve low power consumption [**15**]. The HFR is a 900MHz type-II PLL

for frequency-locking the SSPLL to integer harmonics of 900MHz. The SSLD detects whether the SSPLL is locked to 900MHz harmonics by sub-sampling its output with 900MHz reference. SSLD automatically switches SSPLL's reference to 900MHz for frequency-acquisition, if SSPLL loses lock or locks to a wrong 100MHz (crystal reference) harmonic. When locked, it switches the reference back to 100MHz to benefit from low PN of the crystal. In this way, power-hungry and sensitive mmWave injection-locking frequency dividers (ILFD) in traditional FLL's [**12**] are avoided. Therefore, the whole SSPLL achieves low in-band PN and low power consumption simultaneously. The CP compensation can be turned off for performance comparison.

3.6. Experimental Results

The proposed SSPLL is designed and fabricated in 65nm CMOS. The chip die photo is shown in Fig. 3.14. Core area is $0.6mm^2$. The measurement setup is shown in Fig. 3.15. Due to the low-power structure, the proposed SSPLL achieves 9.52mW power consumption (6.37mW, 1.85mW and 1.30mW for SSPLL, HFR and SSLD, respectively). The compensation structure consumes 0.36mW.

V_{ctrl} locking range is measured with two methods for compensated and uncompensated CP: 1) Lock SSPLL to HFR, tune the 100MHz reference frequency (from signal generator) and read the locked V_{ctrl} range; 2) Lock SSPLL directly to the 100MHz crystal, tune varactor banks to change V_{ctrl}, and read the locked V_{ctrl} range. The results from the two methods are consistent and shown in Fig. 3.16. Under 1V supply, V_{ctrl} LR with compensated CP reaches 0.75V, as shown in Fig. 3.16(b), extended by 50% from the uncompensated range of 0.5V in Fig. 3.16(a). VCO's varactor banks are tuned to mimic various discrete capacitor bank setups. With compensation, the minimum VCO varactor bank number to cover the measured 10% TR is reduced to 7, compared to 10 for the uncompensated SSPLL. This is due to less bank overlap in the compensated version as expected. We define a figure-of-merit (FOM) of "V_{ctrl} LR Efficiency (%)" as:

$$\eta_{V_{ctrl}} = \frac{\text{Total TR (Hz) / } K_{VCO} \text{ (Hz/V)}}{\text{Total VCO bank number * } V_{DD,CP} \text{ (V)}} \ , \tag{3.9}$$

where $V_{DD,CP}$ is the CP supply voltage and K_{VCO} is the VCO gain (1V and 0.8GHz/V, respectively, in our design). This FOM evaluates how efficiently the V_{ctrl} LR utilizes the available range of $V_{DD,CP}$. For our SSPLL, compensated $\eta_{V_{ctrl}}$ is improved to 72% from the uncompensated 50%.

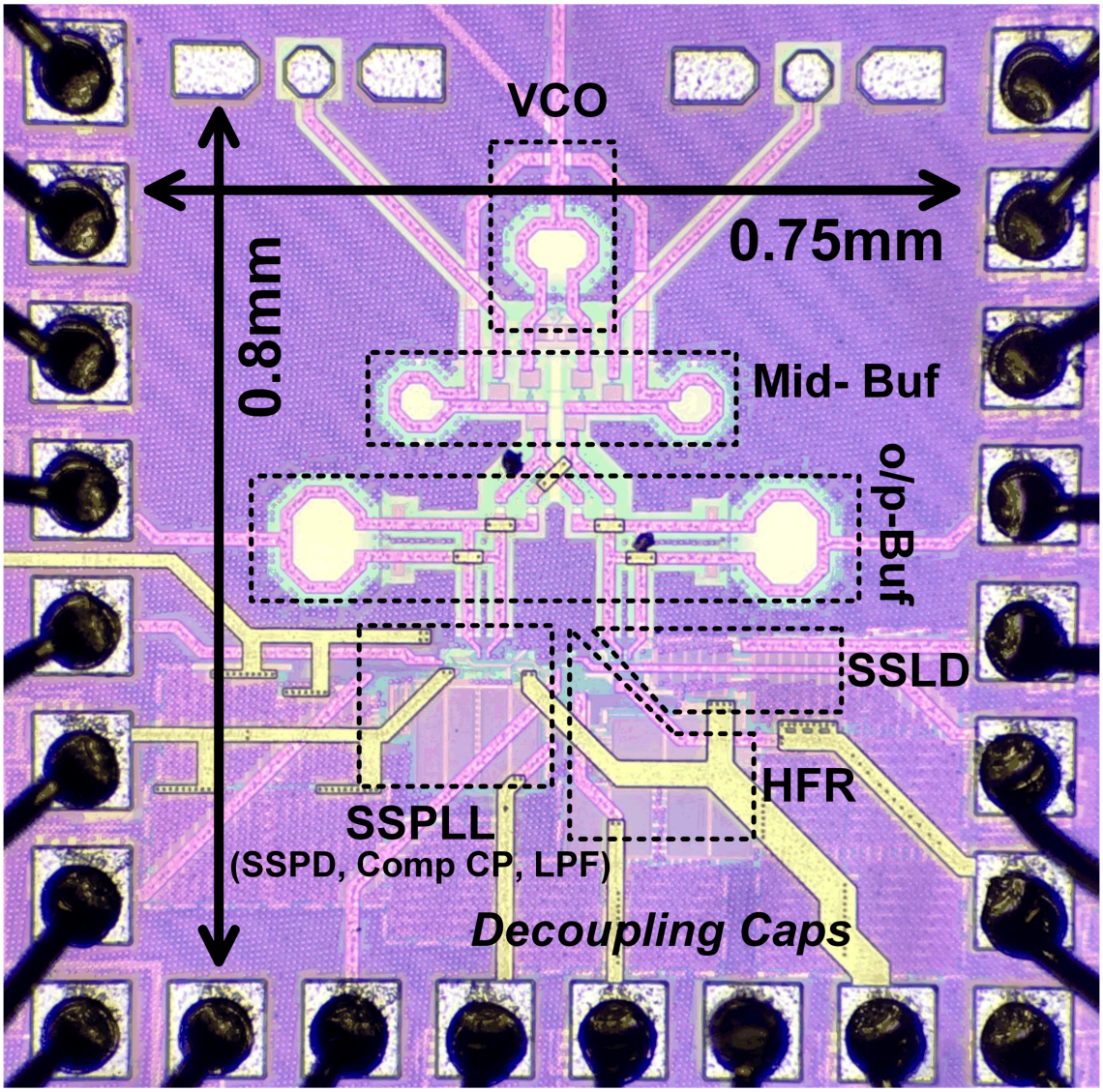


FIGURE 3.14. Chip die photo of the low-power 40.5GHz SSPLL with proposed mismatch compensated CP. Core area is $0.6mm^2$.

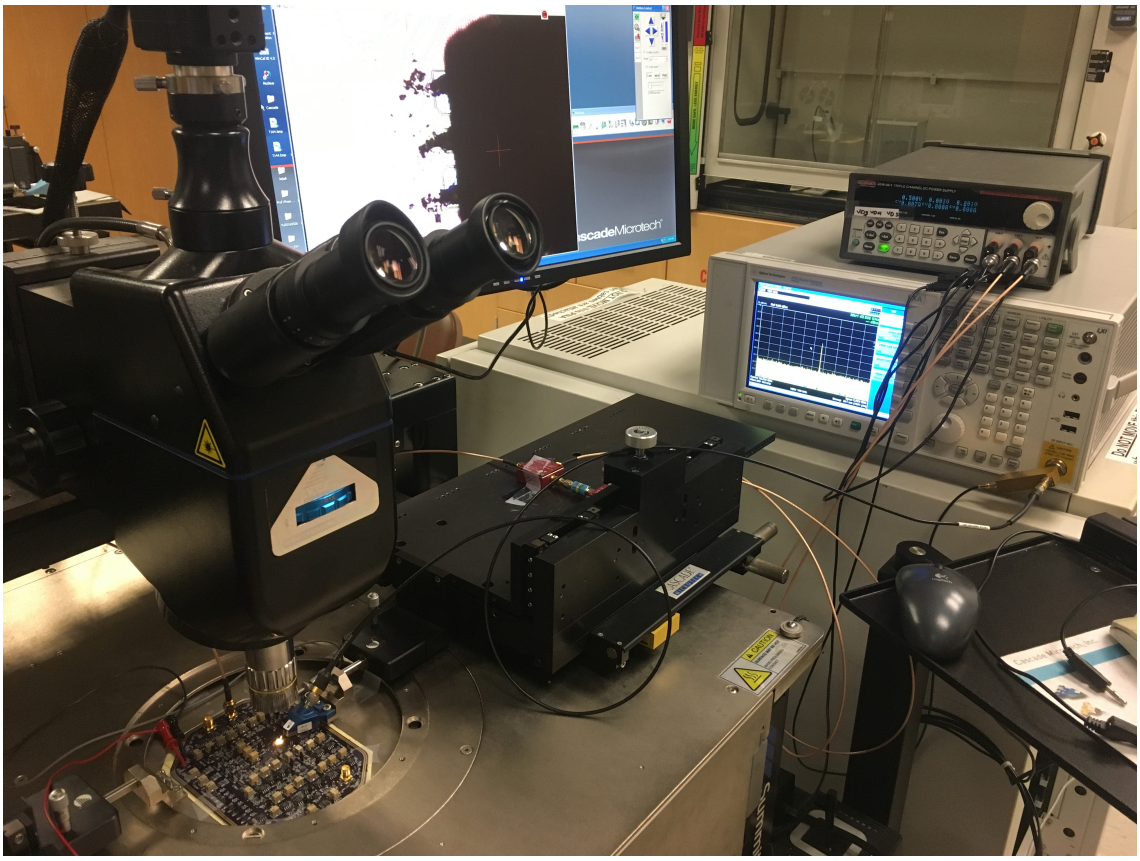
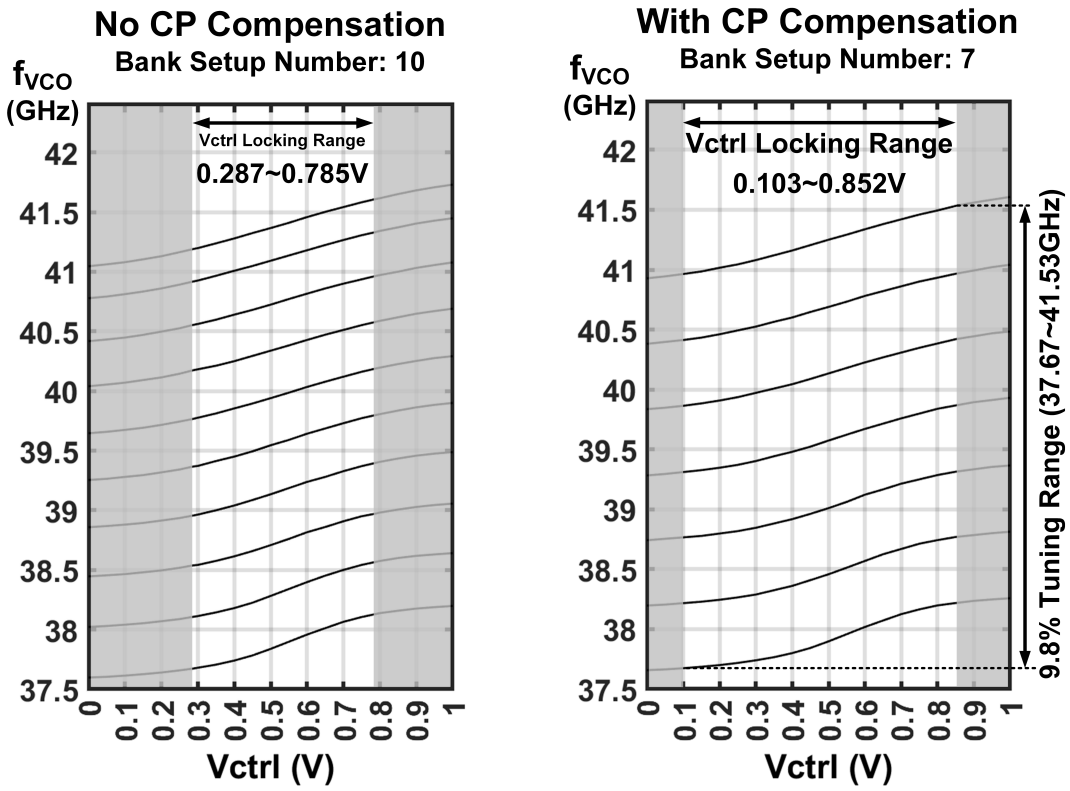


FIGURE 3.15. Measurement setup for the chip.



(a) (b)

FIGURE 3.16. Measured V_{ctrl} locking range of the prototype SSPLL: (a) Without CP compensation, it needs 10 sets of VCO capacitor bank setup to cover the total tuning range; (b) With CP compensation, it needs 7 sets of VCO capacitor bank setup to cover the total tuning range.

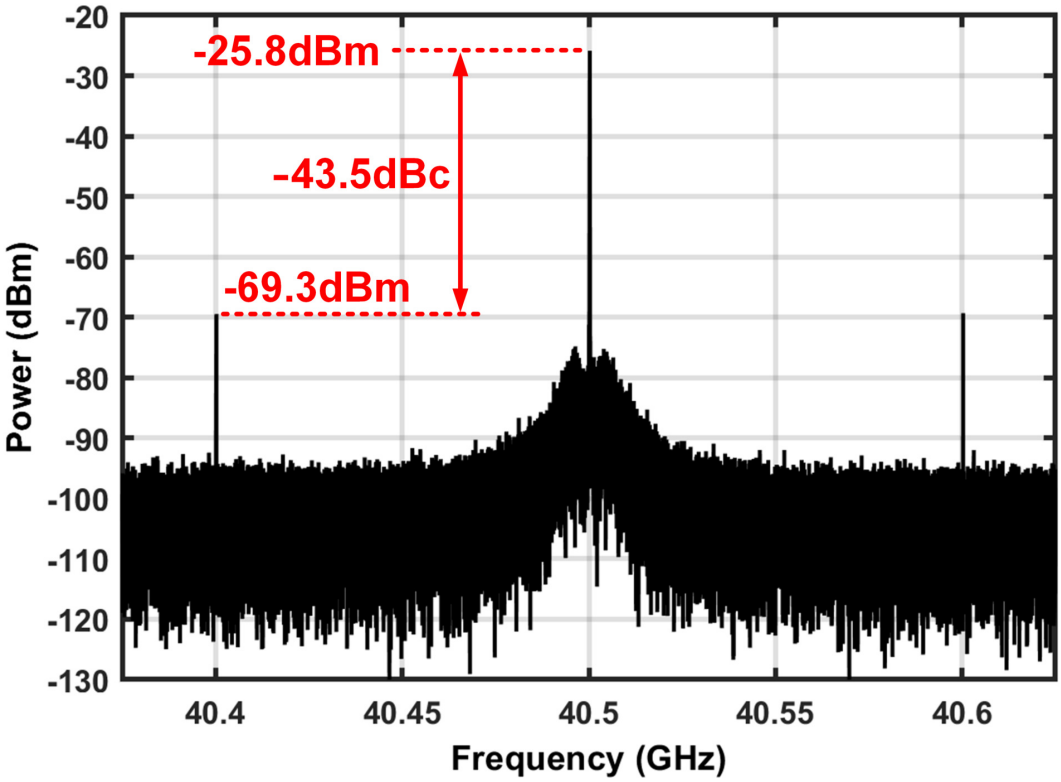


FIGURE 3.17. Measured SSPLL 40.5GHz output frequency spectrum.

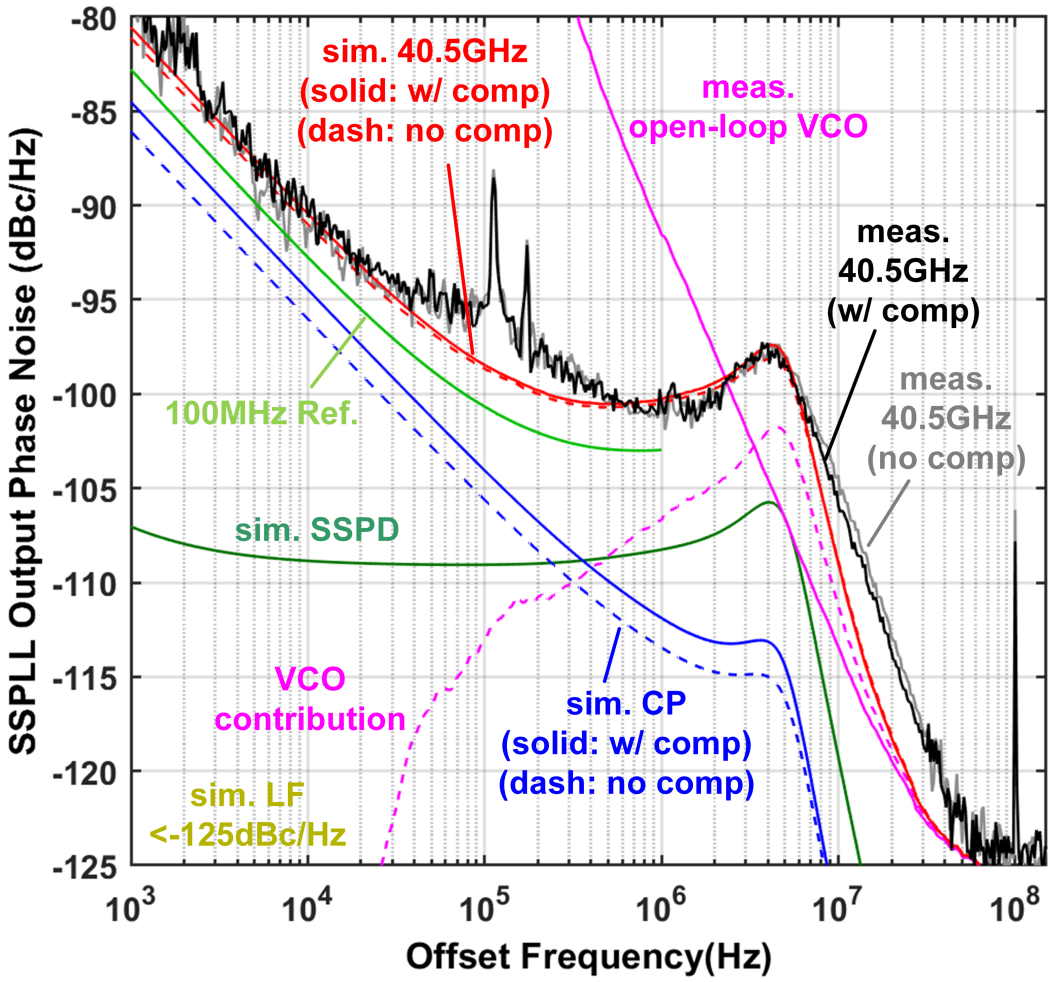


FIGURE 3.18. Measured (black) and simulated (solid red) CP-compensated SSPLL 40.5GHz output phase noises compared with uncompensated PN (grey and dashed red), with each block's noise contribution.

TABLE 3.1. Performance Summary in Comparison with the State-of-the-art.

Ref.		Top.	Tech. (nm)	f_{ref} (MHz)	f_{out} (GHz)	TR (%)	$\eta_{V_{ctrl}}$ (%)	PN[a](dBc/Hz) 1MHz	PN[a](dBc/Hz) 10MHz	Ref.Spur (dBc)	σ_{rms} (fs)	P_{DC} (mW)	Area (mm^2)	FOM_1[b] FOM_2[c]
[14] JSSC'15		SSPLL	40	40	60	16.2	33	-95.4	-104.4	-40	200	42	0.16	-234/-265.9
[12] JSSC'16		SSPLL	65	36/40	60	15.9	30	-95.4	-125.4	-73	290	32	0.7	-235.7/-267.5
[64] TCAS-II'17		PLL	28	125	32	33	12	-89.0	-86.0	N/A	1260	30	0.02	-223.2/-247.3
[19] TMTT'17		PLL+ SSPLL	65	230	28	24.5	19	-112.8	-121.8	-63	79	27	0.28	-247.7/-268.6
[48] ISSCC'19		SSPLL	65	103	30	14.9	26	-109	-120	-63	71	15.3	0.24	-251/-275.2
This Work	**No comp**	**SSPLL +SSLD**	**65**	**100**	**40.5**	**9.8**	**50**	**-100.0**	**-105.9**	**-41.7**	**204**	**9.1**	**0.6**	**-244.2/-270.3**
	CP comp						**72**	**-100.5**	**-105.9**	**-43.5**	**192**	**9.5**		**-244.6/-270.6**

[a] Normalized to 40.5GHz

[b] FOM_1=20 log (jitter/1s) + 10 log (P_{DC}/1mW)

[c] FOM_2=20 log (jitter/1s) + 10 log (P_{DC}/1mW) + 10 log (f_{ref}/f_{out})

The SSPLL 40.5GHz output frequency spectrum is measured in Fig. 3.17, with reference spur of -43.5dBc. The measured (black) and simulated (red) 40.5GHz SSPLL output phase noises with CP compensation, and measured PN without compensation (grey), together with each block's noise contribution (color), are shown in Fig. 3.18. The simulated 100MHz reference noise (light green) is achieved from crystal PN and inverter buffer chain added noise, and the scale up by $20log(405)$. Simulated CP noise with (solid blue) and without (dash blue) mismatch compensation verifies the prior analysis: compensation network adds noise especially at low frequency from the CP_{dum} flicker noise, while high-frequency and out-band noise is filtered by the SSPLL loop. Although the simulated CP noise has increased by CP_{dum}, the overall increase in 40.5GHz phase noise due to compensation network is minute in both simulation and measurement. SSPD noise (dark green) surpasses CP noise to dominate the in-band noise floor. In these measurements N is 1 when the loop is locked to the 100MHz reference. The spurs and bump around 100KHz are caused by the reference input DC-biasing from the noisy power supply. To further examine the effect of the proposed compensation, PN and jitter versus V_{ctrl} are measured and shown in Fig. 3.19 & 3.20 by keeping SSPLL locked to 40.5GHz and tuning the banks to change locked V_{ctrl}. The minimum RMS jitter is 192fs (10kHz to 100MHz) as shown in Fig. 3.20. It's observed from Fig. 3.19 that CP compensation doesn't deteriorate SSPLL's PN. This measured result is consistent with and verifies the noise analysis provided in Section 3.4. With compensation, jitter increases with V_{ctrl} as shown in Fig. 3.20. This is because the CP gain is distorted monotonically with V_{ctrl} value as shown in (3.3).

Table. 3.1 shows the performance comparison with the state-of-the-art. To our knowledge, the proposed current mismatch compensation structure is the first of its kind for SSPLL CP. Moreover, both the SSPLL's power consumption and normalized bank number are among the lowest in published 30GHz to 60GHz SSPLL's.

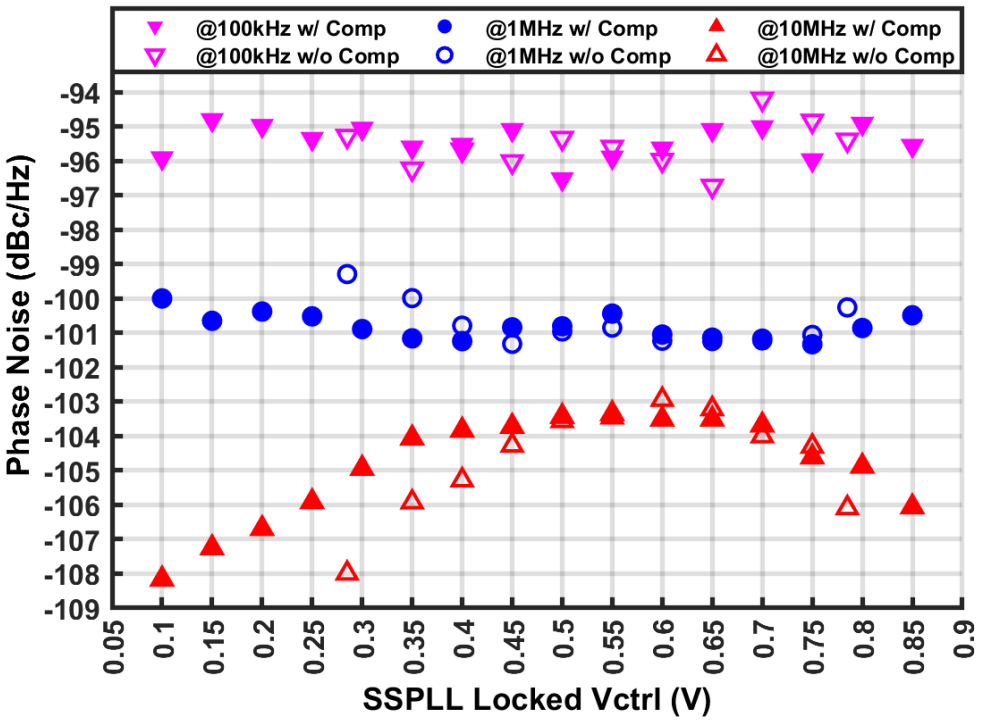


FIGURE 3.19. Measured SSPLL 40.5GHz output phase noise at various locked V_{ctrl}, with and without CP mismatch compensation.

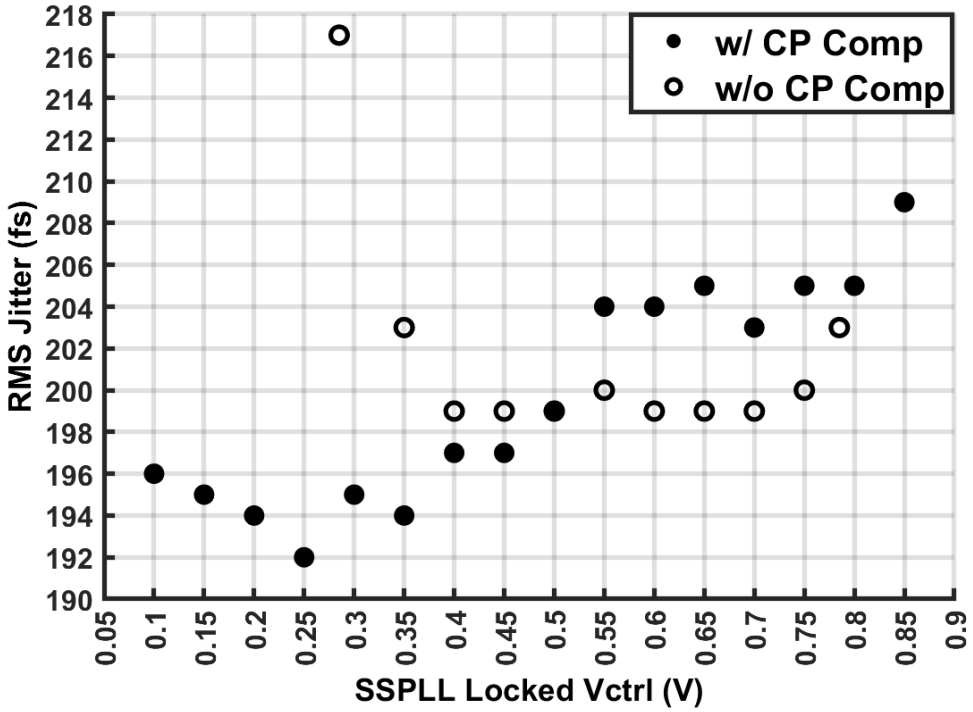


FIGURE 3.20. Measured SSPLL 40.5GHz output RMS jitter at various locked V_{ctrl}, with and without CP mismatch compensation.

3.7. Conclusion & Outlook On Future Work

In this chapter, we propose a current mismatch compensation structure for SSPLL CP to alleviate transistors' CLM effect. With a dummy CP identical to SSPLL CP and a rail-to-rail amplifier based compensation feedback, the proposed structure generates compensation current and cancels CLM-induced CP output current mismatch. As a result, both SSPD gain degeneration and CP input voltage offset are cancelled, and hence SSPLL can lock with a much wider range of V_{ctrl}. With the compensation, fewer VCO capacitor banks are needed to cover the same frequency tuning range. A 40.5GHz SSPLL is designed in 65nm CMOS with the proposed compensated CP. Measured results show that the compensation extends V_{ctrl} LR from 0.50V to 0.75V under 1V supply, without much noise contribution. Capacitor bank setup number is hence reduced from 10 to 7 for the 10% tuning range. Due to the SSLD-based structure, the SSPLL only consumes

9.5mW power with 192fs RMS jitter. The proposed mmWave SSPLL is a promising candidate for low-power applications such as high-resolution on-chip dielectric sensing.

The limitation of the proposed design of CP mismatch compensation is that only down-current is compensated. Future works can focus on simultaneous compensation on up- and down- currents, so that the equivalent CP gain doesn't vary monotonically.

CHAPTER 4

Quadrature-less Doppler Radar Front End for Displacement Sensing

4.1. Introduction

Radar sensors with ultra-high range resolutions have great potential in various non-contact sensing applications [**65**,**66**,**67**,**68**]. Human vital signs such as respiration, heart-beat and epilepsy induce mm level displacement at very low frequencies around 1Hz [**69**, **70**, **71**]. High-precision industrial manufacture could require μm level accuracy in material thickness and evenness. Detection of μm level mechanical vibration of infrastructure, machines and high-precision instruments in labs, factories and specialty environments like rockets and satellites also call for high-resolution sensors [**65**, **72**]. Utilizing beamforming and phased-array techniques, mmWave and THz radar can be designed as high-resolution imager [**73**]. Although depending on system sensor/radar topologies, generally speaking, shorter wavelengths of mmWave and THz ultra-high-frequency signals improve the detection accuracy and range-resolution.

In this chapter, we first present different existing displacement sensor/radar topologies and their pros and cons. Then, a novel Doppler radar front end for low-power and ultra-high range resolution displacement and vibration sensing is proposed. The proposed system utilize correlated-referenced SSPLLs and coherent phase demodulation to achieve low-noise, linear-gain and high-accuracy displacement and vibration detection without using quadrature demodulation and doesn't have detection null issue commonly found in conventional Doppler radars. A prototype 39GHz Doppler radar chip is designed with the proposed structure. Detailed implementation method and noise analysis are presented, followed by measurement results of both static and vibrational object displacement.

4.2. Frequency-Modulated Continous Wave (FMCW) Radar

Frequency-Modulated Continuous-Wave (FMCW) radars in Fig. 4.1 can indicate absolute object position. The transmitted signal frequency, which is the same as that of local oscillator (LO), is modulated with a predetermined waveform such as triangular sawtooth waveform. The modulated frequency range, also called "modulation bandwidth" by convention, is f_{BW}. The modulation time, also named "chirp time" for linear modulation, during which the signal frequency varies by f_{BW} for one round, is T_c. The signal is radiated on object and reflected back. Due to time delay of signal travelling to and back from the object, received signal will have a frequency difference from the LO at the received moment. With a constant frequency modulation slope, the displacement of the object can be derived as:

$$d_{obj,FMCW} = \frac{c \cdot T_c \cdot \Delta f}{2 f_{BW}} \ , \tag{4.1}$$

where Δf is the frequency difference between received signal and LO at the received moment, which can be obtained in frequency spectrum after applying fast Fourier transform (FFT) on the transient received signal during one chirp. The range resolution of FMCW radar is constrained by the minimum frequency resolution of the spectrum converted from the transient received signal during one chirp cycle of T_c. In other words, the range resolution is the smallest measurable Δf, and it can be calculated as:

$$d_{res,FMCW} = \frac{c}{2 f_{BW}} \ . \tag{4.2}$$

Hence, it can be calculated from (4.2) that, f_{BW} must reach hundreds of tera-hertz (THz) to achieve μm-level resolutions. Such a frequency range is unrealistic for the current integrated circuit technologies.

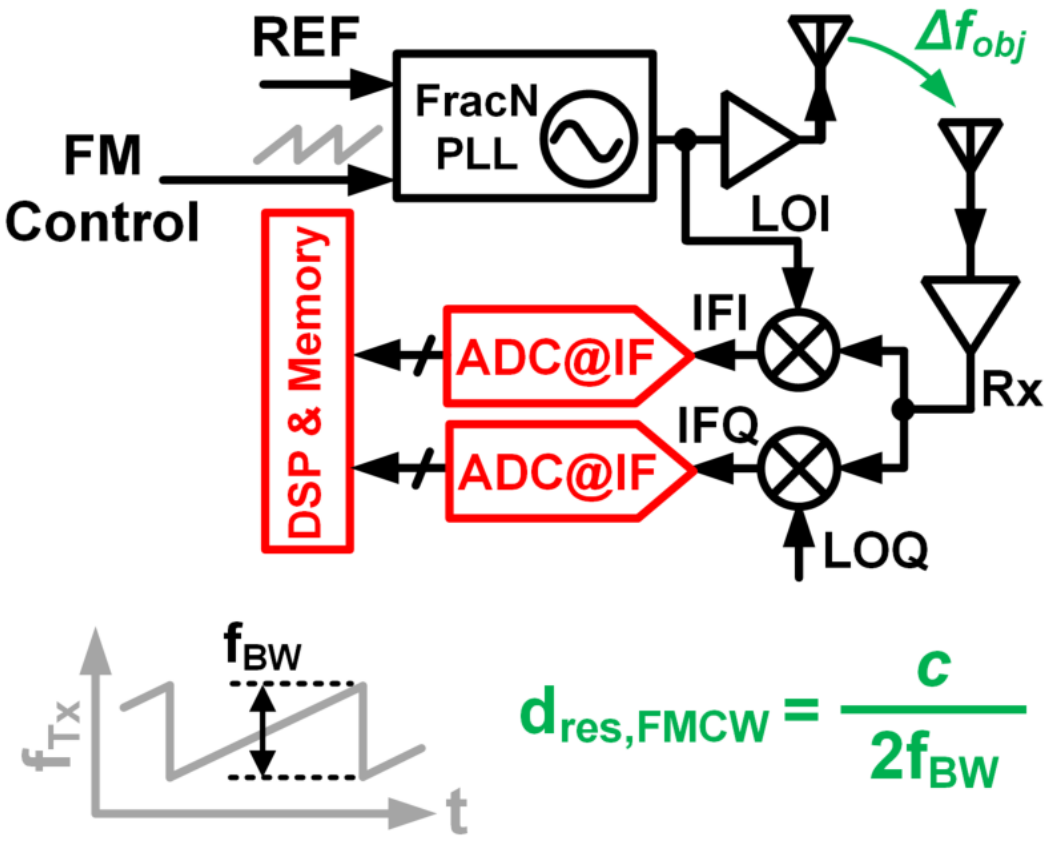


FIGURE 4.1. FMCW Radar.

Phase demodulation technique is an effective solution to the limited f_{BW} issue in the above-mentioned frequency demodulation method [**72**,**73**,**74**,**75**,**76**,**77**]. Quadrature demodulation on received signal is necessary to provide phase information of received signal. By performing complex digital signal processing (DSP) and slow-time FFT on the accumulated threads of quadrature demodulated signals, relative phase change of the received signal and hence the relative displacement of the object can be calculated. Thus, the range resolution can be significantly improved. However, this method demands large resource in memory, DSP complexity and calibration/compensation for the quadrature mismatch and chirp slope nonlinearity critical to achieving high resolutions. As a result, power consumption will increase, and detection speed is impaired due to the data accumulation.

Another factor of FMCW radar affecting system power consumption is the analog-to-digital converters (ADC). With high value of f_{BW}, the IF frequency after down-conversion could reach MHz and even GHz levels. High-resolution ADCs clocked at frequencies high enough to sample the IF consumes high power, let alone at least two such ADCs are needed for quadrature paths. Thus, FMCW radar faces intrinsic drawbacks in low-power and high-resolution displacement sensing applications.

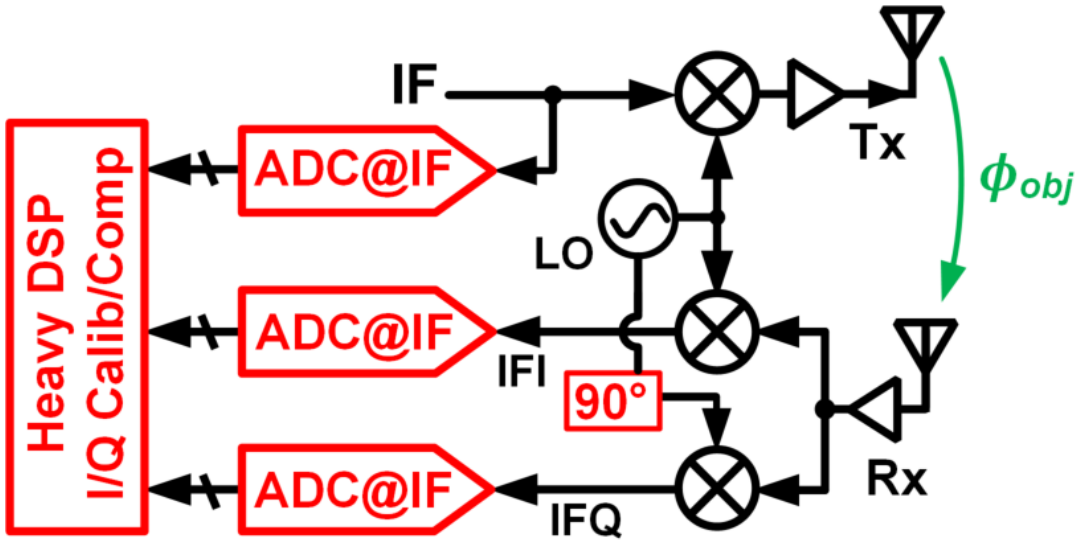


FIGURE 4.2. Continuous-Wave Doppler Radar.

4.3. Doppler Radar & Detection Nulls

Doppler radars, as shown in Fig. 4.2, can detect speed and relative displacement of an object with an unmodulated frequency through Doppler effect [**65**,**70**,**71**,**78**,**79**,**80**]. The received signal's phase carries object's displacement information. As shown in Fig. 4.3, for a static object with a distance of d_{obj} away from the radar, the object-induced phase change between transmitted signal and received signal is:

$$\phi_{obj} = \frac{4\pi d_{obj}}{\lambda_c} \ , \tag{4.3}$$

where λ_c is the wavelength of radar transmitted signal.

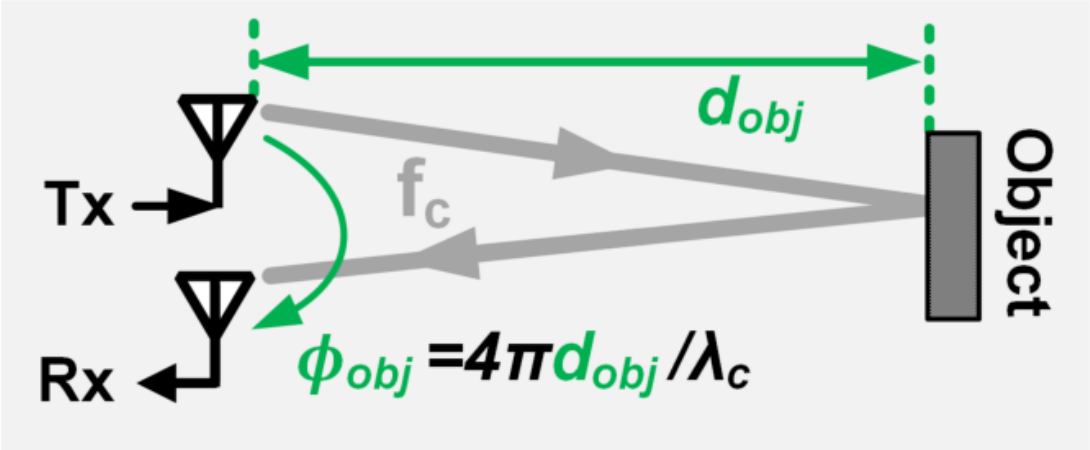


FIGURE 4.3. Object-induced phase change in Doppler Radar.

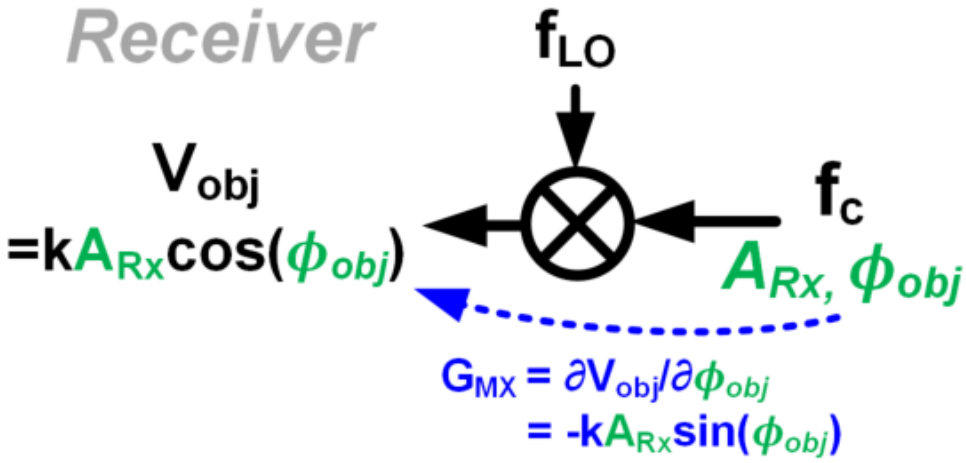


FIGURE 4.4. Non-quadrature demodulation receiver structure.

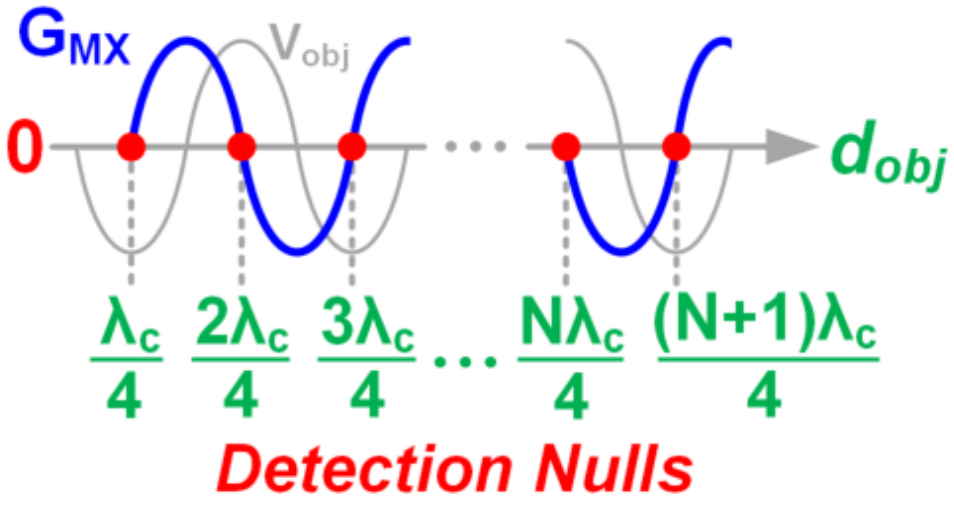


FIGURE 4.5. Detection nulls at which conversion gain reaches 0.

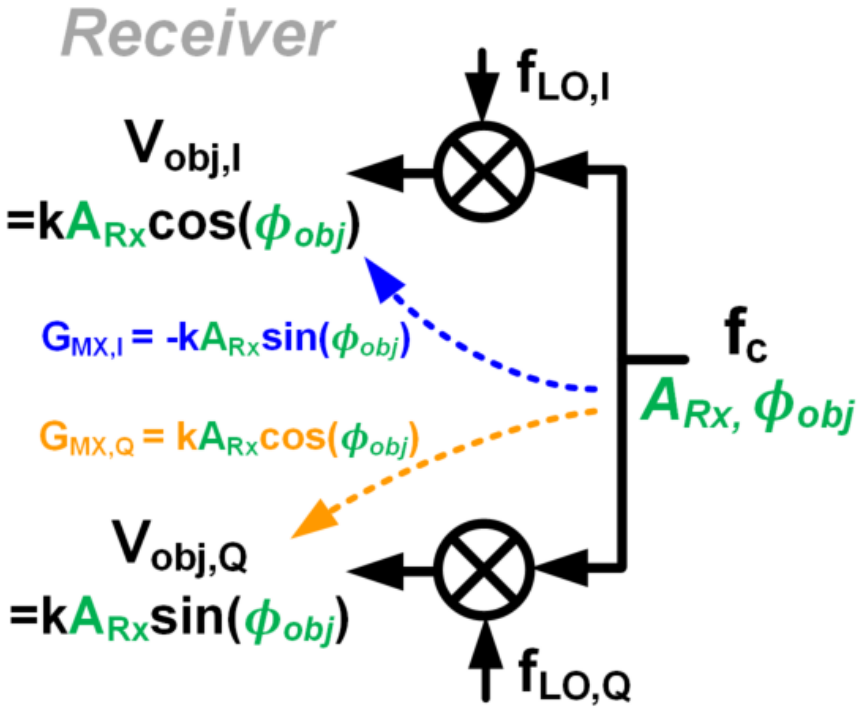


FIGURE 4.6. Quadrature demodulation receiver structure.

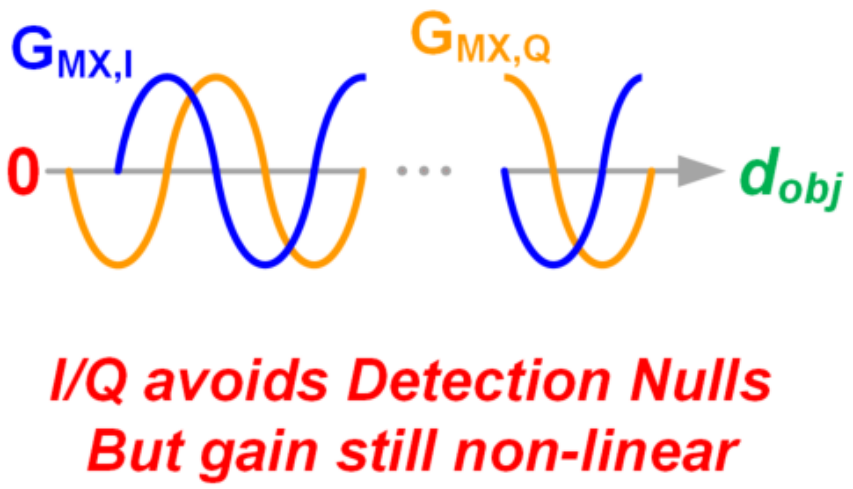


FIGURE 4.7. There is always a non-zero conversion gain in the quadrature paths.

However, conventional Doppler radars suffer from the intrinsic drawback of "Detection Nulls" [**69**]. Fig. 4.4 illustrate a simplified phase-demodulation receiver structure, and Fig. 4.5 shows the output voltage and conversion gain plots. From the figures and plots it can be observed that, the radar's detection gain, which is a function of the receiver mixer's conversion gain, reaches "null" or zero periodically when the object distance is an integer multiple of $\lambda_c/4$. This is because the phase-to-voltage gain of the receiver's down-conversion mixer is a non-linear sinusoidal function of the phase and the power of received signal.

In order to solve the Detection Nulls issue, quadrature demodulation is necessary to always provide a non-zero conversion gain signal path in Doppler radar's receiver [**80**]. As shown in Fig. 4.6 and Fig. 4.7, when either in-phase or quadrature path's gain reaches zero, the other path's gain is non-zero. However, since the gain is still a non-linear function of received signal amplitude A_{rx} and phase ϕ_{obj}, accurate demodulation of the phase to achieve high-resolution and linear displacement sensing requires comprehensive power and gain calibrations as well as post-processing mismatch compensation for quadrature paths. Furthermore, a couple of high-resolution ADCs must be used.

The direct-conversion structure shown in Fig. 4.6 suffers from the common drawbacks in direct-conversion receivers for communication including LO leakage, vulnerable to baseband flicker noise, DC offset at mixer output and so on [**39**]. To alleviate the drawbacks, low-IF heterodyne

structure with quadrature down-conversion is preferred [**71**, **78**], which is exemplified in Fig. 4.2. However, this system needs multiple power-hungry ADCs operating at IF, and they further increase power consumption in addition to all the calibrations and compensations in DSP.

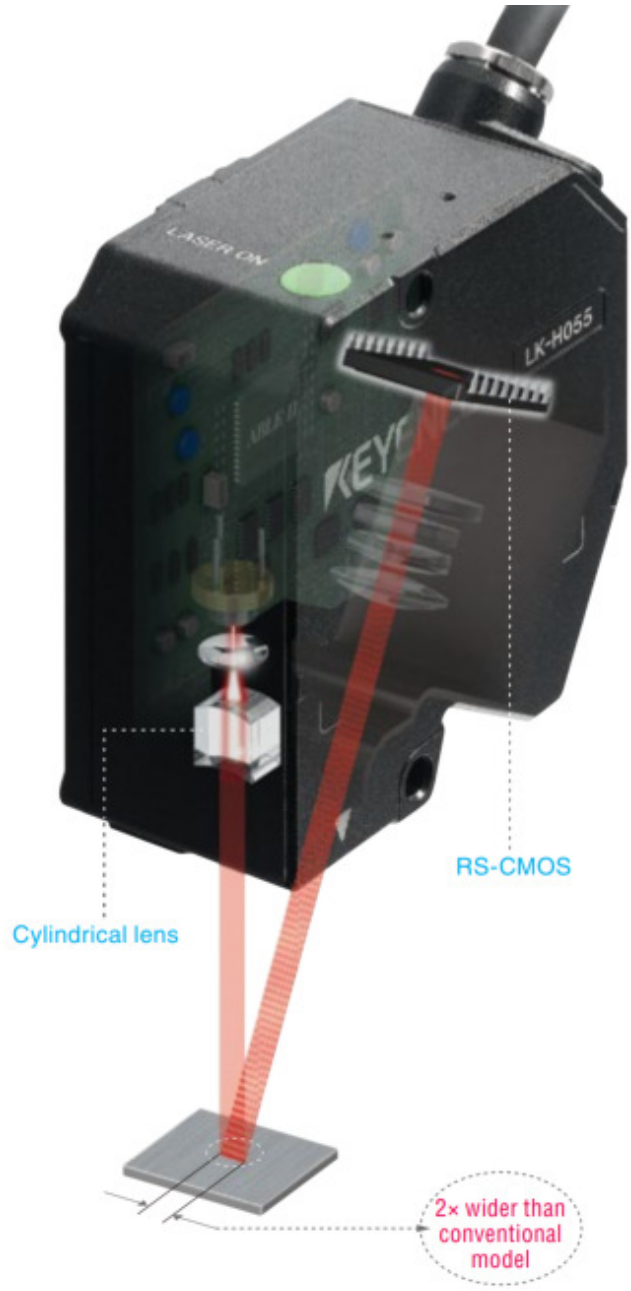


FIGURE 4.8. Keyence laser vibrometer.

4.4. Laser Vibrometer

One of the most accurate displacement sensors is laser vibrometer. A Keyence laser vibrometer module is shown in Fig. 4.8 [**81**]. Using short-wavelength laser beams, the vibrometer module can detect upto nm and even sub-nm level displacement. However, there are several drawbacks. The module is bulky due to the packaged optical link. The price of laser vibrometer is very high, with the cheapest labelled several thousand dollars. The cost is intrinsic, partly due to the expensive CMOS light sensor chip with a significant area, as well as the laser generator. The measuring distance is very limited at around $5cm$ from the object, and this prevents its application in many non-contact displacement sensing such as human vital-sign detection.

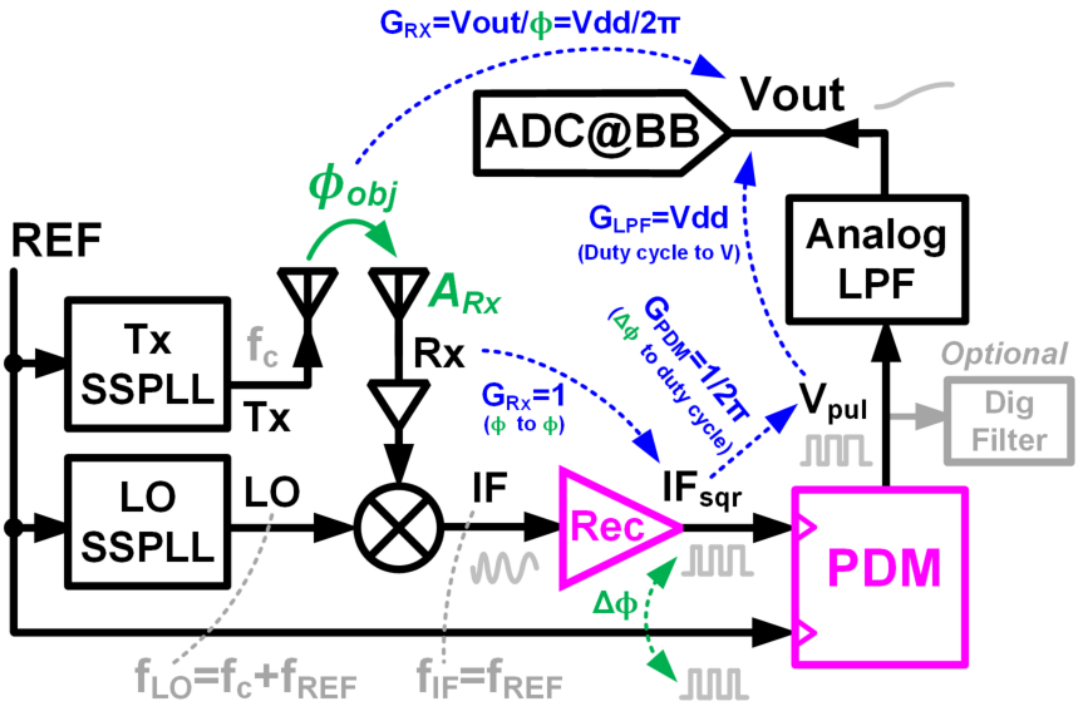


FIGURE 4.9. Proposed quadrature-less and detection-null-less Doppler radar front end.

4.5. Proposed Quadrature-less & Detection-Null-less Doppler Radar

Realizing the drawbacks of conventional Doppler radar structure, in this dissertation, a low-power displacement and vibration sensing Doppler radar front end structure is proposed,

which eliminates detection nulls without using quadrature demodulation as shown in Fig. 4.9. Two low-noise integer-N SSPLLs with the same reference (REF) at f_{REF} generate the transmitted signal (Tx) and the local-oscillator signal (LO) at f_{Tx} and $f_{LO} = f_{Tx} + f_{REF}$, respectively. Since Tx is a single tone without sidebands, quadrature demodulation is not needed. After radiation and reflection from the object, the received signal (Rx) carries phase information of ϕ_{obj} induced by the object's position. The Rx signal is first amplified by an LNA and then down-converted with LO and the mixer. After low-pass filtering, the mixer's output is an IF signal carrying ϕ_{obj} at f_{REF}. This IF is rectified to a square wave of IF_{sqr}, whose rising edges are synchronized with IF's zero-crossings. Thus, ϕ_{obj} is converted to the time of rising edges of IF_{sqr}. A phase demodulator (PDM) compares the rising edges of IF_{sqr} with REF to extract ϕ_{obj}. Since both IF_{sqr} and REF are at f_{REF}, resulted PDM output is a pulse signal also at f_{REF}, but with pulse widths proportional to ϕ_{obj}. Finally, a low-pass filter (LPF) converts the pulses into a voltage signal of V_{out} at DC or baseband depending on whether the object is static or vibrating. Because the IF rectifier's phase-to-phase gain, the PDM's phase-to-pulse-width gain, and the LPF's pulse-width-to-voltage gain are all linear, as labelled in blue in Fig. 4.9, the proposed radar is free from detection nulls. The receiver detection gain from ϕ_{obj} to V_{out} is:

$$G_{RX} = \frac{\partial V_{out}}{\partial \phi_{obj}} = \frac{Vdd}{2\pi} \ , \tag{4.4}$$

where Vdd is the supply voltage of the PDM, as well as the full-scale voltage of V_{out}. Furthermore, if the Rx power and the receiver gain are high enough to produce sharp-edge IF_{sqr}, the proposed structure demodulates ϕ_{obj} into V_{out} with a linear gain irrespective of received signal power. Thus, power detection and calibration are not needed. Finally, only one ADC is needed to convert the DC/baseband V_{out}, making power consumption intrinsically lower than FMCW or conventional Doppler radars with multiple ADCs operating at IF. Benefited from low SSPLL-added noise and coherent IF demodulation in PDM, the proposed radar can achieve ultra-high sensing resolution.

Table. 4.1 compares the pros and cons of different displacement-sensing radar front end topologies. With the linear and received-power-independent detection gain, quadrature-less

TABLE 4.1. Radar Topology Comparison

	FMCW	Conv. Doppler	Proposed
Absolute Distance	Yes	No	No
< λ Range Resolution	- High freq & BW - Memory & DSP	Yes	Yes
Vibration Freq	Yes	Yes	Yes
Displacement	Yes	w/ Power Calibration	Yes
Rx Demodulation	- I/Q needed for Phase Demod - Analog o/p @ IF	- Non-linear gain - I/Q LO needed for Det-Nulls - Analog o/p @ IF	- Linear gain - I/Q not needed: No Det-Nulls - Analog o/p @ baseband
DSP	Heavy (ADCs@IF)	Heavy (ADCs@IF, calib/comp)	Light (single ADC@BB)
Power Consumption	High	High	Low

structure, and requirement of only 1 ADC for baseband signal, the proposed Doppler radar intrinsically consumes lower power than FMCW and conventional Doppler radars. Due to low added-inband noise feature of SSPLL, correlated reference to the two SSPLLs, and coherent phase demodulation in PDM, the proposed radar can achieve very low noise and hence ultra-high range resolution in displacement-sensing.

4.6. Prototype 39GHz Displacement & Vibration Sensing Doppler Radar

Based on the proposed radar topology, Fig. 4.10 illustrates the detailed design of the implemented radar in the proposed structure. A 1GHz off-chip reference with phase noise (PN) of $\phi_{n,REF}$ is fed into the chip. A 39GHz Tx and a 40GHz LO are generated from two SSPLLs. The phase noise contributed by the VCOs ($\phi_{n,VCO1}$ and $\phi_{n,VCO2}$) is high-pass-filtered by the SSPLL loop, and therefore in-band phase noise of SSPLL output phase (ϕ_{Tx} and ϕ_{LO}) contains upscaled $\phi_{n,REF}$, non-upscaled charge pump (CP) added noise ($\phi_{n,CP1}$ and $\phi_{n,CP2}$) and phase-detector (SSPD) added noise ($\phi_{n,CP1}$ and $\phi_{n,CP2}$) [**15**,**31**]. The phase noise of Tx and LO can be expressed as:

$$\phi^2_{n,Tx} = 39^2\phi^2_{n,REF} + \phi^2_{n,SSPD1} + \phi^2_{n,CP1} + \phi^2_{n,VCO1}(HF) \ , \tag{4.5}$$

$$\phi_{n,LO}^2 = 40^2\phi_{n,REF}^2 + \phi_{n,SSPD2}^2 + \phi_{n,CP2}^2 + \phi_{n,VCO2}^2(HF) \ . \tag{4.6}$$

Because the phase differences between REF and two SSPLL output signals are constant, we can omit them for convenient calculation and derive the Tx and LO signals' phases as:

$$\phi_{Tx} = \sqrt{\phi_{n,Tx}^2} \ , \tag{4.7}$$

$$\phi_{LO} = \sqrt{\phi_{n,LO}^2} \ . \tag{4.8}$$

In the SSPLLs of the prototype radar, the input signal to SSPDs are designed with large swing so that $\phi_{n,SSPD}^2$ is negligible compared to $\phi_{n,CP}^2$. Meanwhile, $\phi_{n,CP}^2$, of which the low-frequency flicker noise is critical to radar's detection resolution, is minimized by adopting one-stage differential-to-single-ended transconductor with tail-resistor biasing and source-degenerated transistors. CP current mismatch compensation is applied for robust locking [**32**, **82**]. VCOs are designed with ¡1GHz frequency range under any capacitor bank to ensure correct locked frequencies. Hence, no frequency acquisition loop is needed.

The Tx signal is passed to a GSG pad through a transformer coupled to VCO tank. Accessing the chip with probes, two horn antennae with 19dBi gain are used to radiate Tx on and receive reflection from an object which is d_{obj} away from the antennae and has a relative displacement of Δd. An object-induced phase change of $\phi_{obj} = 4\pi(d_{obj} + \Delta_d)/\lambda_{39G}$ is added to ϕ_{Tx}, where λ_{39G} is the Tx wavelength, and results in an Rx phase of ϕ_{Rx}:

$$\phi_{Rx} = -\phi_{obj} + \sqrt{\phi_{n,Tx}^2} \ . \tag{4.9}$$

Note that the constant phase delay along probes and cables are omitted for convenient calculation.

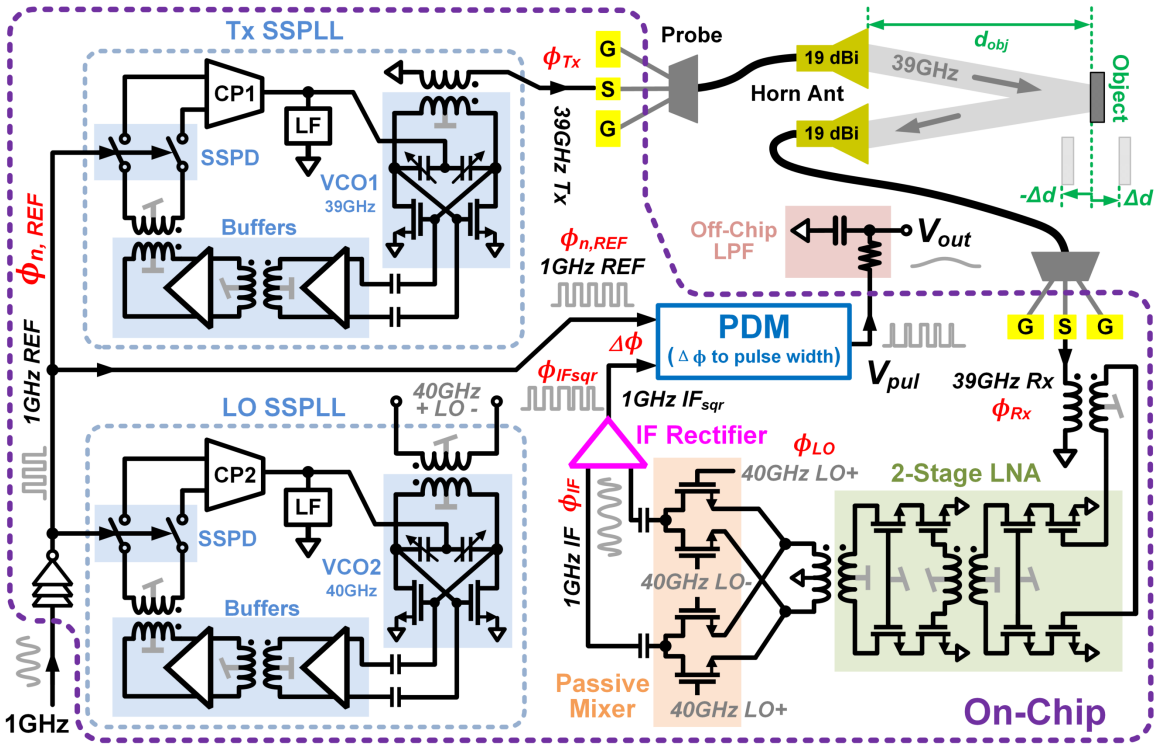


FIGURE 4.10. Prototype 39GHz displacement-sensing Doppler Radar.

The received Rx signal is converted to a differential signal by a balun, and then amplified by a two-stage LNA. To minimize added flicker noise, a passive mixer is used to down-convert Rx to IF. Since Tx and LO SSPLLs are referenced with the same REF, their upscaled REF PNs are correlated. Thus, the phase of IF can be calculated as:

(4.10)

$$\phi_{IF} = \phi_{obj} + \sqrt{\phi^2_{n,REF} + \phi^2_{n,CP1} + \phi^2_{n,CP2} + \phi^2_{n,LNA} + \phi^2_{n,Mx} + \phi^2_{n,VCO1}(HF) + \phi^2_{n,VCO2}(HF)}\ ,$$

where $\phi^2_{n,LNA}$ and $\phi^2_{n,Mx}$ are added phase noise from LNA and Mixer, respectively. As a result, (4.10) shows that only $1 \times \phi_{n,REF}$ is remained in IF phase (ϕ_{IF}), while uncorrelated CPs, VCOs, LNA and Mixer noises add up in ϕ_{IF}. Assuming high swing at rectifier input and neglecting the added noise from the rectifier, its output signal IF_{sqr} is a square-wave with a phase of:

(4.11)

$$\phi_{IF_{sqr}} = \phi_{IF}\ .$$

Now, phase information of ϕ_{obj} together with phase noise are transferred to the phase of IF_{sqr}. Being a square-wave, $\phi_{IF_{sqr}}$ is embodied by the rising/falling edges of IF_{sqr}.

After achieving IF_{sqr}, a linear-gain coherent IF phase demodulator (PDM) is design in Fig. 4.11. The PDM senses the rising edges of REF and IF_{sqr} in sequence, and produce a pulse signal with its pulse width proportional to the time delay, which the phase difference of $\Delta\phi = \phi_{IFsqr} - \phi_{REF}$, between REF and IF_{sqr}. Since REF and IF_{sqr} carry the same amount of coherent REF phase noise, the $1 \times \phi_{n,REF}$ noise included in ϕ_{IFsqr} is cancelled by REF at the input of PDM. Hence, we have:

$$\begin{aligned}\Delta\phi &= \phi_{IF_{sqr}} - \phi_{REF} = \phi_{IF} - \phi_{REF} \\ &= \phi_{obj} + \sqrt{\phi_{n,CP1}^2 + \phi_{n,CP2}^2 + \phi_{n,LNA}^2 + \phi_{n,Mx}^2 + \phi_{n,VCO1}^2(HF) + \phi_{n,VCO2}^2(HF)} \\ &= \phi_{obj} + \phi_{n,floor} \ ,\end{aligned} \tag{4.12}$$

where $\phi_{n,floor}$ is the phase noise floor of detection. After processing $\Delta\phi$ through the PDM's logic and the state machine shown in Fig. 4.12, the PDM generates an output, V_{pul}, having the frequency of IF, and a pulse width proportional to $\Delta\phi$, and a duty cycle of:

$$D_{pul} = \frac{\Delta\phi}{2\pi} \ . \tag{4.13}$$

Thus, the PDM transfers phase different of $\Delta\phi$ to the duty cycle of V_{pul} with a constant gain of

$$G_{PDM} = \frac{\partial D_{pul}}{\partial \Delta\phi} = \frac{1}{2\pi} \ . \tag{4.14}$$

An analog low-pass filter (LPF) consisting of a tunable resistor and a 10nF capacitor is loaded to the PDM output. The LPF filters V_{pul} and converts its duty cycle to a voltage signal of V_{out} with a constant gain of:

$$G_{LPF} = \frac{\partial V_{out}}{\partial D_{pul}} = V_{FS} \ . \tag{4.15}$$

where V_{FS} is the supply voltage of the PDM circuitry generating V_{pul}, as well as the full-scale voltage of V_{out}. After filtering through the LPF, signal V_{out} can be calculated to be:

$$V_{out}(f) = \begin{cases} \Delta\phi(f)V_{FS}/2\pi \ , & f \ll f_{LPF} \\ 0 \ . & f \gg f_{LPF} \end{cases} \tag{4.16}$$

where f_{LPF} is the LPF bandwidth. We design f_{LPF} around 1MHz or lower, so that 1) high-frequency phase noise of $\phi_{n,VCO}$ in (4.12) is filtered, and 2) only static and vibrational displacement with frequency much less than 1MHz can be sensed which makes the radar sensor capable of detecting most of the mechanical vibration situations. With (4.3), (4.12) and (4.16), the relation ship between object distance d_{obj} and radar's output signal V_{out} can be calculated as:

$$d_{obj}(f) = \frac{\lambda_{39G}}{2V_{FS}} \cdot [V_{out}(f) + V_{n,floor}(f)] \ , \tag{4.17}$$

where $V_{n,floor}(f)$ is the noise floor of $V_{out}(f)$, with expression of:

$$V_{n,floor}(f) \approx \frac{V_{FS}}{2\pi} \sqrt{\phi^2_{n,CP1}(f) + \phi^2_{n,CP2}(f) + \phi^2_{n,LNA}(f) + \phi^2_{n,Mx}(f)} \ . \tag{4.18}$$

The approximation in (4.18) is for neglecting the filtered VCO phase noises and the LPF thermal noise. It must be noted that, $V_{n,floor}(f)$ is a function of frequency, with its value increases at lower frequencies due to flicker noise frequency feature. It can be observed from (4.17) and (4.18) that, through coherent phase demodulation in PDM and LPF filtering, the noise floor is significantly reduced to only contain low-frequency flicker noises from CPs, LNA, and Mixer. The radar's resolution, d_{res}, which is the minimum detectable displacement and limited by $V_{n,floor}$, can be expressed as:

$$d_{res}(f) \approx \frac{\lambda_{39G}}{2V_{FS}} \cdot V_{n,floor}(f) \ , \tag{4.19}$$

The state machine of PDM is also designed to ensure a monotonic phase-to-duty-cycle gain, so that the radar can distinguish object's displacement direction (moving further or closer to the radar) without ambiguity, as shown in Fig. 4.12. From (4.17) we know, nn object displacement of Δd produces a voltage change of ΔV_{out}, with a constant gain of $\Delta V_{out}/\Delta d = 2V_{FS}/\lambda_{39G}$. Hence, detection nulls are eliminated, and displacement sensing can be done without knowing Rx power.

Signal illustration of IF_{sqr} processing and V_{out} generation through the PDM and the LPF is shown in Fig. 4.13. When the object has static displacement of Δd, a proportional amount of DC change will be produced in V_{out}. On the right of the figure, the object's mechanical vibration induces an oscillation in Δd, which proportionally produces a corresponding AC signal carried by V_{out}. Note that the radar still bear the intrinsic features of Doppler radars, which only indicate relative displacement within the range of $\lambda_c/2$. Continuously storing measured V_{out} and un-wrapping the data could be a feasible and potential solution for larger range displacement sensing.

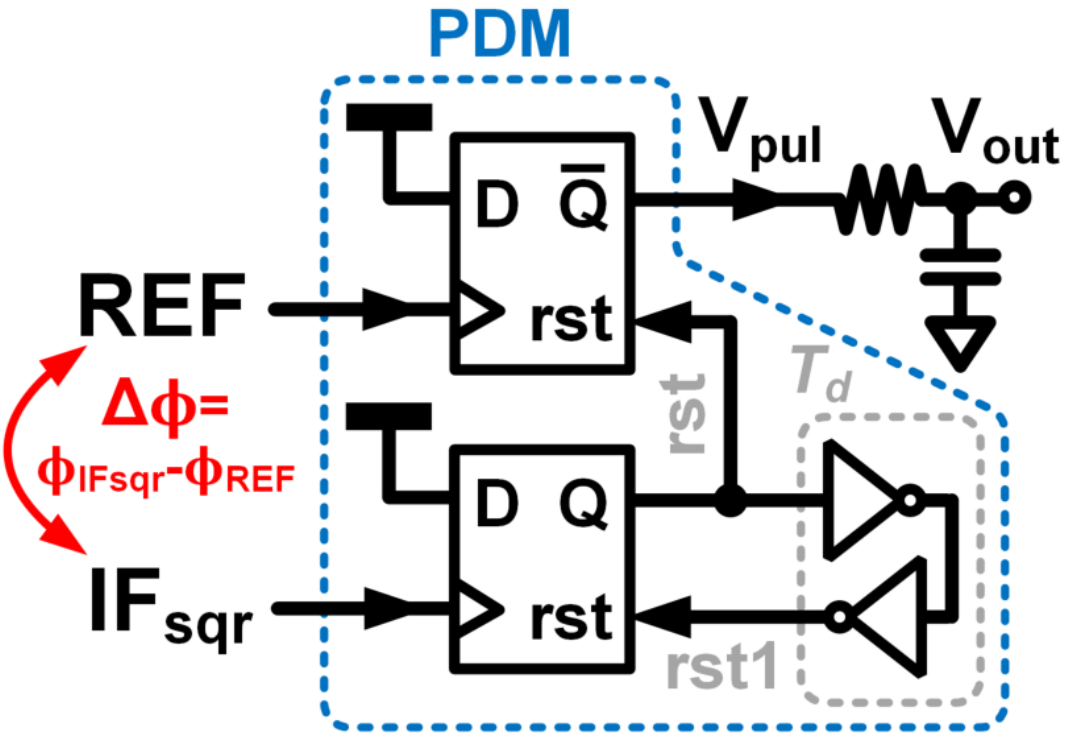


FIGURE 4.11. Proposed linear-gain IF phase demodulator (PDM).

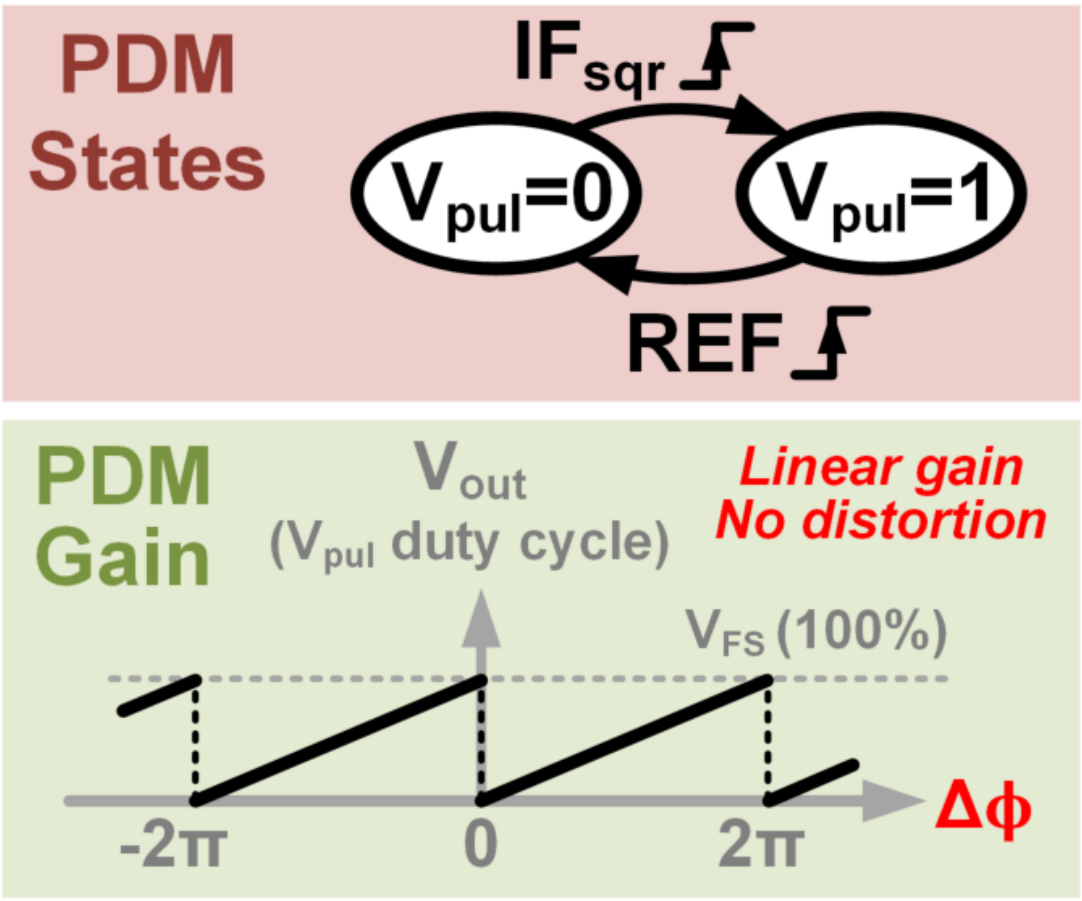


FIGURE 4.12. State machine and phase demodulation gain of the proposed PDM.

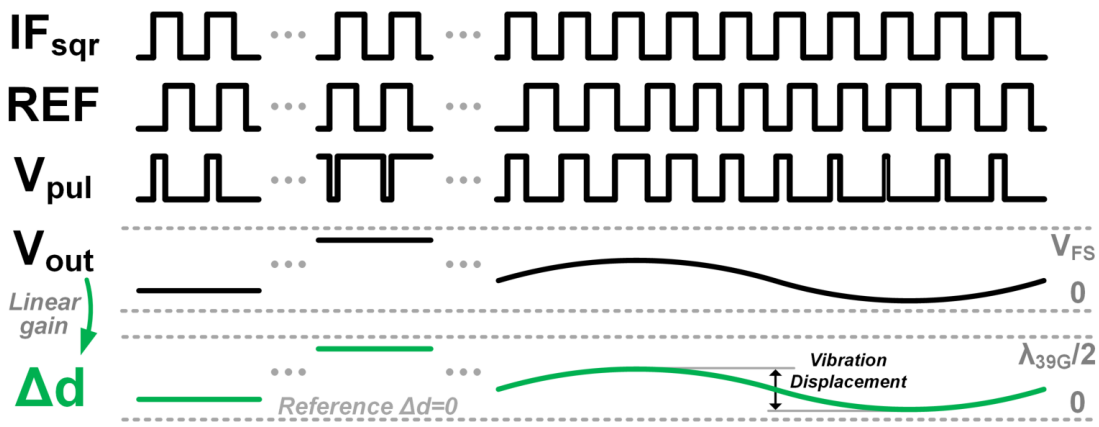
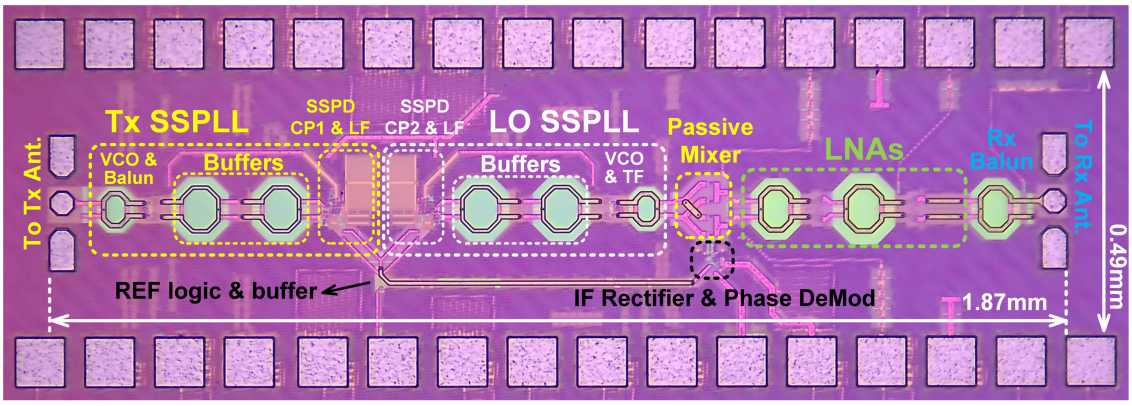


FIGURE 4.13. Signal illustration of the proposed PDM loading an LPF.



	Tx SSPLL			LO SSPLL			LNA	REF Log & Buf	IF Rec & PDM	Total
	VCO1	Buffers	CP1	VCO2	Buffers	CP2				
Power(mW)	16	15.6	1	12	12.7	1.1	46.2	4.7	0.4	109.8

FIGURE 4.14. Die micrograph and power consumption of the prototype Doppler radar front end.

4.7. Experimental Results

The proposed radar front end is fabricated in 65nm CMOS process with a core area of $0.92mm^2$ and a total power consumption of 110mW, as shown in Fig. 4.14. Measured power at Tx output pad

is 2.8dBm, and the EIRP at antenna output is 15.5dBm. A Keithley DMM6500 digital multimeter mimicking an ADC is connected to V_{out}. With V_{FS}=1V, the theoretical displacement-to-V_{out} gain is:

$$\begin{aligned} G_{d2V} &= \frac{\partial V_{out}}{\partial d_{obj}} \\ &= 2V_{FS}/\lambda_{39G} \\ &= 260V/m \ . \end{aligned} \tag{4.20}$$

4.7.1. Static Displacement. Fig. 4.15 shows the setup and measured results of static displacement sensing. A 10x10cm aluminium board is used as an object, whose position is manually adjusted through a micrometer with 0.5μm resolution. Fig. 4.16 presents the measured V_{out} for static object displacement within nearly the full range of $\lambda_{39G}/2 = 3.8$mm, corresponding to a $\Delta\phi_{obj}$ range of 2π, at different object distance (d_{obj}). For the full range measurement, V_{out} is measured with a displacement step of 0.1mm. It verifies that detection nulls are eliminated since $\partial V_{out}/\partial d_{obj}$ never reaches zero.

Fig. 4.17 shows the measured results of static range resolution. A measured static range resolution of 4μm is achieved, indicated by the $\pm 2\sigma$ error bars (95% confidence for each set of 1000 measurements at each displacement).

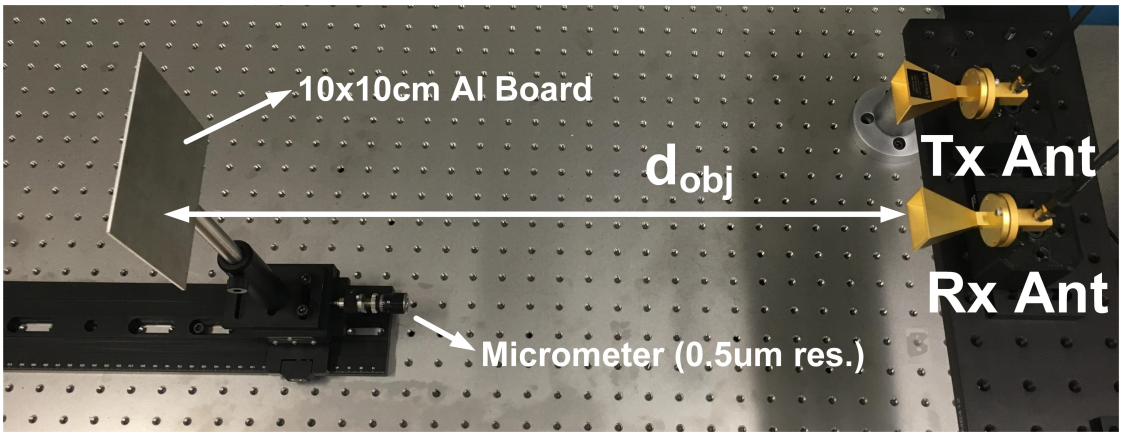


FIGURE 4.15. Measurement setup of static displacement sensing.

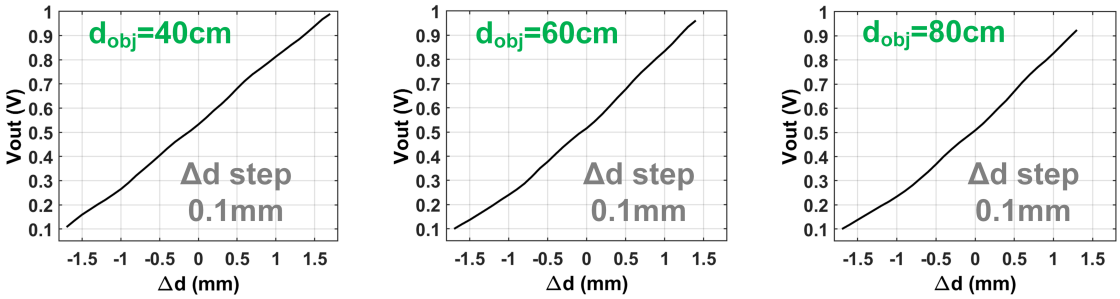


FIGURE 4.16. Measured static displacement across full range.

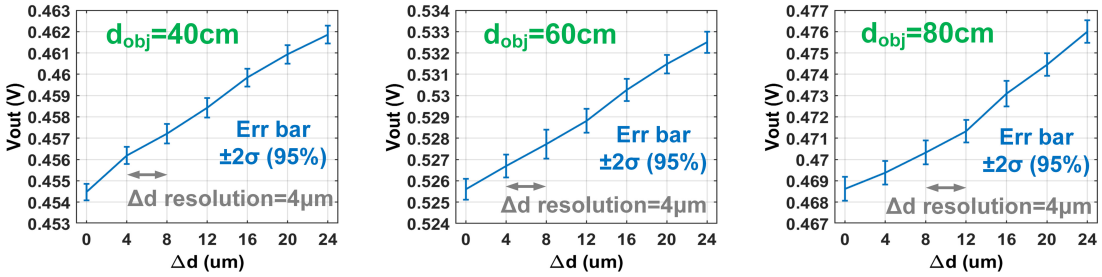


FIGURE 4.17. Measured range resolution of static displacement sensing.

4.7.2. Mechanical Vibration. Fig. 4.18 shows the measurement setup of mechanical vibration sensing. A 20cm-diameter speaker is controlled by signal source to vibrate at different frequencies with different amplitudes. The peak-to-peak vibrational displacement (D_{pp}) of the speaker is calibrated at its central position with a Keyence LK-H057 laser vibrometer, as shown in Fig. 4.19. V_{out} data is measured and collected by a digital multimeter, and frequency spectra of V_{out} are achieved by doing FFT on the sampled V_{out} data, and are shown in Fig. 4.20. Due to lower noise floor at high frequencies, measured vibrational range resolutions reach nanometer level as shown in Fig. 4.20, indicated by the minimum detectable D_{pp} corresponding to detected vibration signal at least 3dB higher than local noise floor. Note that laser vibrometer measures only at one small spot's vibrational displacement of the speaker, while the radar senses a much larger area of the speaker's cone. Thus, discrepancy exists between laser calibrated D_{pp} (shown in Fig. 4.20) and the calculated displacement amplitude through radar measured V_{out}.

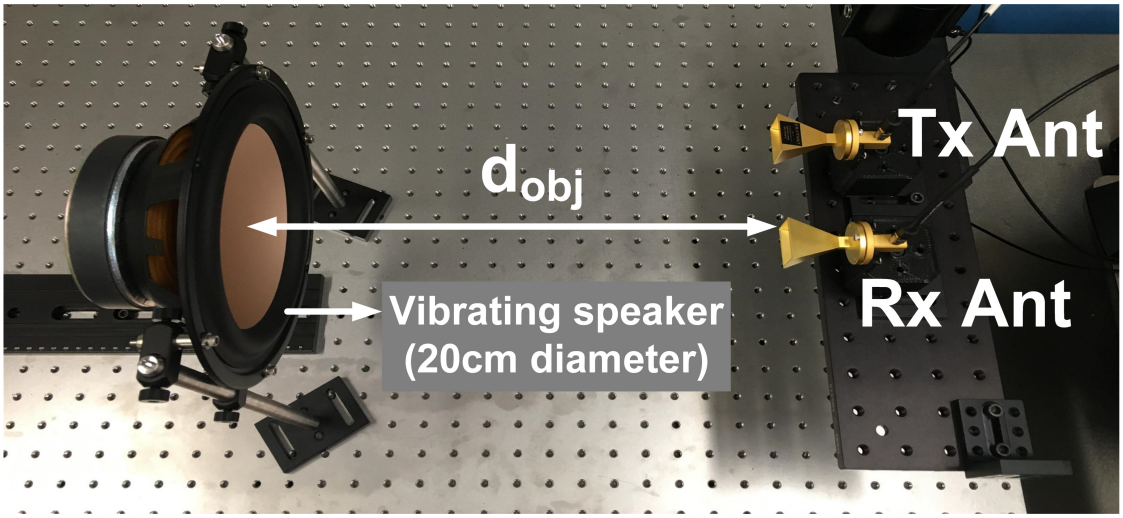


FIGURE 4.18. Measurement setup of vibration sensing.

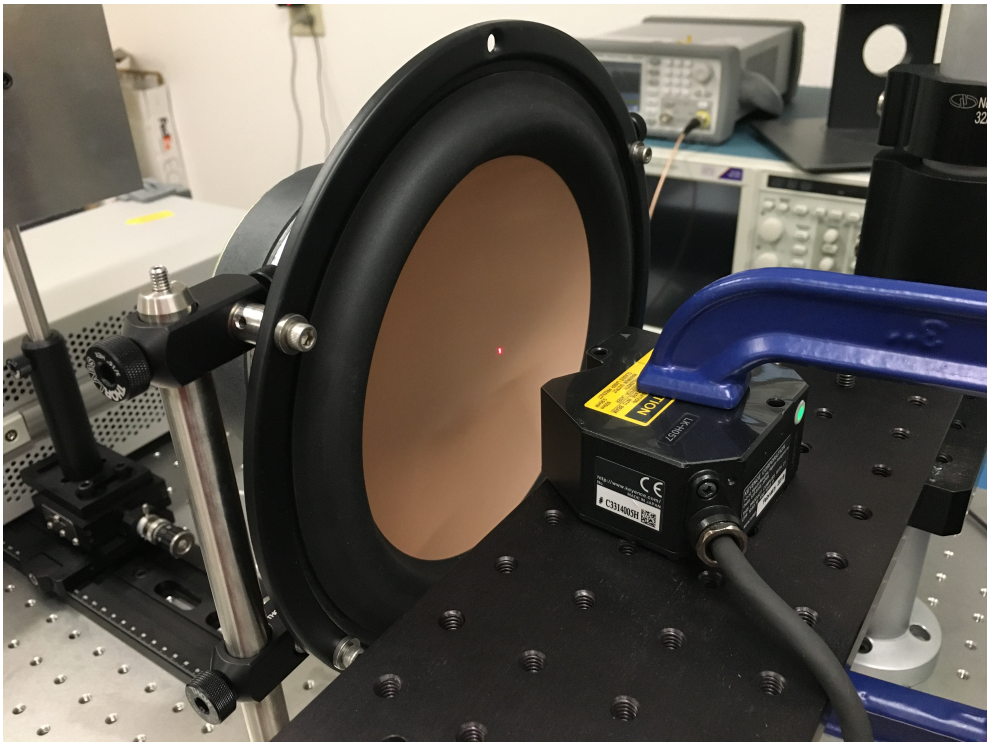


FIGURE 4.19. Measurement setup of laser vibrometer calibration.

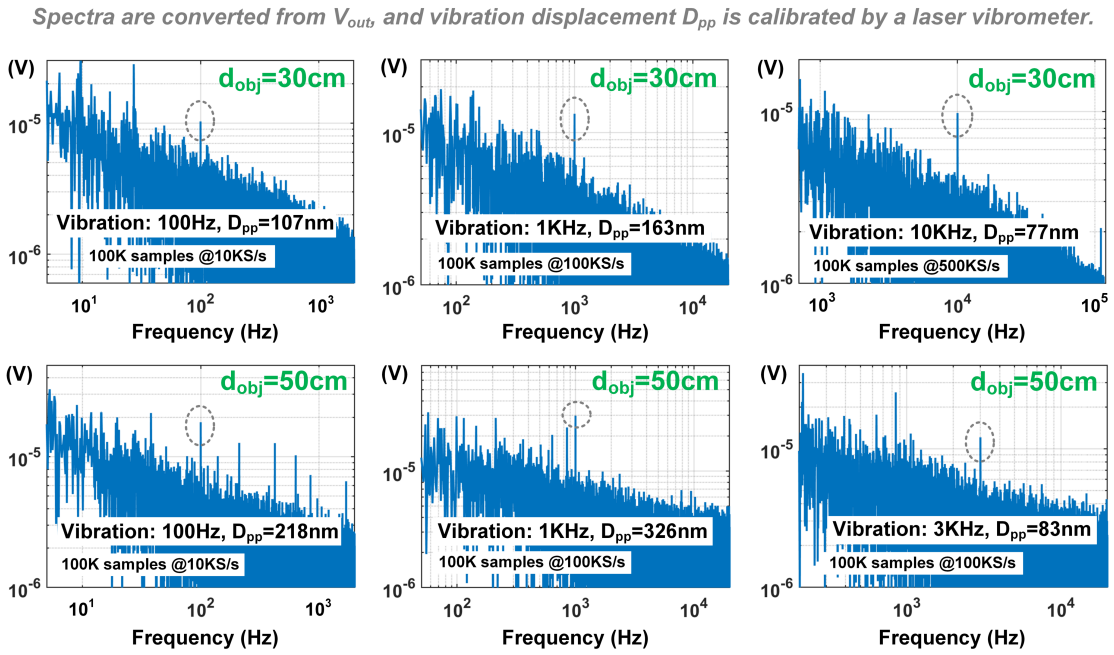


FIGURE 4.20. Measured vibrational range resolution represented by the minimum detectable vibration.

Table. 4.2 shows the performance comparison with the state-of-the-art radars. The proposed Doppler radar front end achieves ultra-high resolutions with significantly lower structure complexity, off-chip requirement, and power consumption than the state-of-the-art.

4.8. Conclusion & Outlook On Future Work

A Doppler radar front end topology eliminating detection nulls is proposed without using quadrature demodulation. Two SSPLLs sharing the same reference generate transmitted and LO signals with correlated reference noise and low added in-band phase noise. By rectifying the down-converted sine-wave IF to square-wave, phase information is converted to time domain independent on received signal power. After edge-sensing phase demodulation with coherent reference noise cancellation in the PDM, phase information is converted to duty cycle of the PDM's output pulse signal with a constant gain. A LPF processes the pulse signal and produces a voltage signal linearly proportional to the object-induced phase and hence the object distance.

TABLE 4.2. Comparison with the state-of-the-art.

	Naghavi ISSCC 21	X. Yi ISSCC 20	X. Ma TMTT 20	C. Chou TMTT 18	T. J. Kao TMTT 13	This Work
Process	55nm SiGe	65nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS
Topology	FMCW	FMCW	DSB CW	Single-Tone CW	DSB CW	Single-Tone CW
Freq (GHz)	250	270	100	60	60	39
BW (GHz/%)	67/30	100/37	-	-	-	-
Tx Power [a] (dBm)	-	-	4	3	0	2.8
Tx EIRP (dBm)	17 [b]	20 [b]	24	20	5	15.5 [c]
Obj. Distance (m)	0.25	0.31	1.5	1.2	0.3	0.5
Static Range Resolution (um)	**54**	**1500**	**-**	**500**	**20**	**4**
Vibrational Range Resolution (um)	-	-	**5** @5Hz **1** @10Hz	**500** @1.2Hz	**20** @1Hz	**0.218** @100Hz **0.326** @1KHz **0.083** @3KHz **0.077** @10KHz [d]
I/Q Rx	No	Yes	Yes	Yes	Yes	No
Required Off-Chip Processing	**@1MHz IF** - ADC **x2** - **Heavy** DSP	**@1MHz IF** - ADC **x5** - **Heavy** DSP **15GHz** REF	**@1**KHz **IF** - ADC **x3** - **Heavy** DSP **50GHz** REF	**@Baseband** - ADC x**2** - **Heavy** DSP **60**GHz **REF**	**@Baseband** - ADC **x4** - **Heavy** DSP	**@Baseband** - ADC **x1** - **Light** DSP **1GHz** REF
Power (mW)	68	840	262	243	377	110
Area (mm^2)	0.2	5	1.8	4.68	0.73	0.9

a) At chip output b) With lenses c) Including 6.3dB cable loss d) At 30cm distance

As a result, the displacement to V_{out} detection gain is theoretically constant without nulls. Due to the quadrature-less structure, relaxed calibration and compensation requirement, and that only one baseband ADC is needed, total power consumption of the proposed front end is intrinsically lower than other radar topologies. The prototype 39GHz Doppler radar front end designed in 65nm CMOS hence achieves $4\mu m$ static and up to $77nm$ vibrational range resolution with 110mW power consumption.

In this chapter, it can be observed that the versatile frequency synthesis feature of the SSPLL provides a leeway in designing radar structures. However, one of the obstacles faced with SSPLL is the maximum frequency it can directly produce without using any noise-scaling components such as frequency dividers in the feedback path or injection-locked frequency multipliers at the output. One example is how to directly generate sub-THz signals. It would be hardly possible to directly sample sub-THz signals with SSPD, let along designing the very power-consuming sub-THz

signal buffers. Harmonic-based frequency translation elements [**83**] such as ILFMs can be used. However, correlated reference noise as well as uncorrelated CP and SSPD noises are all scaled up if using ILFMs. As a result, the V_{out} noise floor and hence the radar's range resolution are impaired significantly due to the boosted added in-band phase noise from CP and SSPD, especially that these noises are mainly flcker noise which increases exponentially at low frequency. Researchers are invited to come up with new ideas of mmWave/THz frequency synthesis with low added in-band noise.

APPENDIX A

Maximum Frequency Deviation of SSPLL Due to Reference Switching

The time-domain step response of V_{ctrl} can be derived with (2.13). Let's assume the loop filter consists of a resister of value $R = R_1 + R_2$ in parallel with a capacitor of value C_p as shown in Fig. 2.18. In our design, there is another capacitor C_s in series with R. For simplicity in calculation, we can ignore C_s since $C_s \gg C_p$ (e.g. C_s=20pF and C_p=3.5pF in Fig. 2.18). Hence, the transfer function of the LF is $H_{LF}(s) = R/(1 + sRC_p)$. Let's define $G = K_{SSPD}K_{CP}K_{VCO}$ and assume reference switching happens at $t = 0$. As a result, the step excitation $\phi_{in}(t) = \phi_{in}u(t - t_{sw})$, where t_{sw} is the switching moment, becomes $\phi_{in}(t) = \phi_{in}u(t)$. Consequently, V_{ctrl} phase-domain response is calculated from (2.13) to be:

$$\begin{aligned} V_{ctrl}(s) &= \frac{\phi_{in}}{s} \cdot \frac{\frac{G}{K_{VCO}} \cdot \frac{R}{1+sRC_p}}{1 + \frac{G}{s} \cdot \frac{R}{1+sRC_p}} \\ &= \frac{-j\phi_{in}G}{2\beta K_{VCO}C_p} \left(\frac{1}{s + \alpha - j\beta} - \frac{1}{s + \alpha + j\beta} \right), \end{aligned} \tag{A.1}$$

where

$$\begin{cases} \alpha = \dfrac{1}{2RC_p} , \\ \beta = \sqrt{\dfrac{1}{C_p} \left(G - \dfrac{1}{4R^2C_p} \right)} . \end{cases} \tag{A.2}$$

This solution is valid if $G - 1/(4R^2C_p) > 0$. Given the typically large loop gain, G, and the relatively small $1/(4R^2C_p)$, this condition is valid in most cases of SSPLL design, as well as in our design.

The calculated V_{ctrl} time-domain response is:

$$V_{ctrl}(t, \phi_{in}) = \frac{\phi_{in} G \cdot e^{-\alpha t}}{\beta K_{VCO} C_p} sin\beta t + V_{ctrl,0} \ , \tag{A.3}$$

where $V_{ctrl,0}$ is the initial value as well as the final value of V_{ctrl} corresponding to f_{out}=40.5GHz. Since (A.3) has a damping behavior, we can calculate the maximum deviation of V_{ctrl} from $V_{ctrl,0}$ at $t = \pi/(2\beta)$ as:

$$\Delta V_{ctrl,max}(\phi_{in}) = \frac{2\phi_{in} GR \cdot exp\left(\frac{-\pi}{2\sqrt{4GC_pR^2-1}}\right)}{K_{VCO}\sqrt{4GC_pR^2-1}} \ . \tag{A.4}$$

Since (A.4) is an odd function of ϕ_{in}, using $f_{out} = V_{ctrl} K_{VCO}$, we can translate (A.4) to the maximum SSPLL output frequency deviation as:

$$|\Delta f_{out,max}(\phi_{in})| = \frac{2|\phi_{in}| GR \cdot exp\left(\frac{-\pi}{2\sqrt{4GC_pR^2-1}}\right)}{\sqrt{4GC_pR^2-1}} \ , \tag{A.5}$$

where $-\pi \leq \phi_{in} \leq \pi$.

APPENDIX B

Charge Pump Mismatch Compensation Feedback Transfer Function

Based on the block diagram in Fig. 3.6, the transfer function of the compensation feedback can be derived as:

$$H_{FB}(s) = \frac{i_{comp}}{v_{ctrl}} = \frac{G_{mc}A_V\left(\frac{1}{Z_M}+\frac{1}{Z_{o,d}}\right)}{A_V\left(\frac{1}{Z_M}+G_{mc}\right)+\frac{1}{Z_M}+\frac{1}{Z_{o,d}}} \ , \tag{B.1}$$

where $Z_M = R_M + 1/(sC_M)$ is the Miller compensation network impedance. Given that $A_V \gg 1$ and $A_V G_{mc} \gg 1/Z_{o,d}$ (e.g. $G_{mc} = 0.1mS$ and $Z_{o,d} = 55k\Omega$ in our design.), (B.1) can be approximated to:

$$H_{FB}(s) = \frac{i_{comp}}{v_{ctrl}} = \frac{G_{mc}\left(\frac{1}{Z_M}+\frac{1}{Z_{o,d}}\right)}{\frac{1}{Z_M}+G_{mc}} \ . \tag{B.2}$$

Defining $\omega_{M1} = 1/(R_M C_M)$, $\omega_{M2} = G_{mc}/C_M$ and $\omega_{M3} = 1/(Z_{o,d}C_M)$ with our design parameters of $R_M = 500\Omega$, $C_M = 0.5pF$, (B.2) can be further simplified into:

$$H_{FB}(j\omega) \approx \begin{cases} \frac{1}{Z_{o,d}} \ , & \omega < \omega_{M3} \\ sC_M \ , & \omega_{M3} < \omega < \omega_{M2} \\ G_{mc} \ , & \omega_{M2} < \omega < \omega_{M1} \\ \frac{G_{mc}}{1+R_M G_{mc}} \ . & \omega_{M1} < \omega \end{cases} \tag{B.3}$$

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