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Holey Silicon and Through Silicon Vias for Thermal Management of Next-Generation Electronic Systems

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Mechanical and Aerospace Engineering

by

Zongqing Ren

Dissertation Committee:
Associate Professor Jaeho Lee, Chair
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2021

DEDICATION

To

my parents, family

in recognition of their love and support

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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Micro/nanoscale thermal transport, thermal metamaterials, thermoelectric cooling, thermal management of electronics

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J1. **Zongqing Ren**, and Jaeho Lee. "Thermal conductivity anisotropy in holey silicon nanostructures and its impact on thermoelectric cooling." *Nanotechnology* 29, no. 4 (2017): 045404.

J2. Ayed Alqahtani, **Zongqing Ren**, Jaeho Lee, and Nader Bagherzadeh. "System-level analysis of 3D ICs with thermal TSVs." *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 14, no. 3 (2018): 1-16.

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C4. **Zongqing Ren**, Ziqi Yu, Jae Choon Kim, and Jaeho Lee. "Hotspot Management by Holey Silicon-Metal Composites for 1 kW/cm 2 and Beyond." In *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pp. 1253-1259. IEEE, 2019.

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ABSTRACT OF THE DISSERTATION

Holey Silicon and Through Silicon Vias for Thermal Management of Next-Generation Electronic Systems

by

Zongqing Ren

Doctor of Philosophy in Mechanical and Aerospace Engineering

University of California, Irvine, 2021

Professor Jaeho Lee, Chair

The trends of electronic systems toward nanoscale, high power, and 3D integration have made heat dissipation from local hot spots to heat sink structures ever more challenging. Meanwhile, recent advances in fabrication and manufacturing technologies have enabled the development of unique structures and brought new opportunities to address thermal management challenges. This doctoral research focuses on the use of holey silicon and through silicon vias to provide device-level and system-level cooling solutions for next-generation electronic systems.

Lateral thermoelectric coolers where Peltier cooling and heating occur in the lateral direction offer solid-state hot spot cooling capability. While most advanced thermoelectric materials with low thermal conductivities provide necessary temperature gradients for thermoelectric conversion, the heat generation in electronics is detrimental to the system where high thermal conductivity is preferred. The contrasting needs of thermal conductivity are evident in thermoelectric cooling systems which call for a fundamental breakthrough. In this dissertation, we show a silicon nanostructure with vertically etched holes, or holey silicon, uniquely combines low thermal conductivity in the in-plane direction and high thermal conductivity in the cross-plane

direction, and this anisotropy is ideal for lateral thermoelectric devices. The low in-plane thermal conductivity due to substantial phonon boundary scattering in small necks sustains temperature gradients for the Peltier effect. The high thermal conductivity in the cross-plane direction due to persistent long wavelength phonons effectively dissipates heat from a hot spot to the heat sink structure. Furthermore, cooling performance of holey silicon-based thermoelectric coolers can be significantly enhanced by integrating a metallic through silicon via that directly draws heat from a hot spot. Beyond the steady-state operation, we demonstrate a transient supercooling effect, driven by the temporal and spatial interplays between the interfacial Peltier effect and the volumetric Joule heating effect. Holey silicon with anisotropic thermal conductivity is favorable by delaying the heat diffusion in the lateral direction while allowing rapid heat dissipation in the vertical direction. The transient cooling performance can be further improved by incorporating phase change materials within holey silicon, in which their melting process delays the temperature overshoot. Apart from simulations, we fabricate holey silicon-based thermoelectric coolers through standard semiconductor processes and experimentally demonstrate their cooling performance through an infrared thermography-based measurement. The cooler temperature reduction can be improved by increasing the operating temperature. Transient supercooling is also achieved by applying a current pulse, where the cooler temperature can be temporarily lower than the minimum value in steady state.

While lateral thermoelectric devices provide extraordinary device-level cooling performance, the recent development of three-dimensional integrated circuits demanding system-level cooling solutions to advance processor design and enable continued performance scaling. Through silicon via is the main structure that enables 3D integrated circuits and provides electrical connection between dies. Thermal through silicon vias are dummy vias that facilitate heat transfer

across stacked dies. However, the insertion of thermal through silicon vias extends the distance between functional units and increases the signal delay. In this dissertation, we develop a hierarchical approach to optimize the floorplan of a 3D integrated circuit through simulated annealing to address the trade-off between the peak temperature, chip area, and performance. Compared to the floorplan with a fixed thermal via placement between cores, our algorithm optimally places thermal vias between functional units and offers the optimal floorplan.

This dissertation presents that the use of holey silicon and through silicon vias can provide effective device-level and system-level thermal management solutions for next-generation electronic systems. Holey silicon with anisotropic thermal conductivity is ideal for lateral thermoelectric devices, which enables breakthroughs in addressing local hot spots under steady-state and transient conditions. Thermal through silicon vias reduce the peak temperature of 3D integrated circuits. The hierarchical floorplanning method that includes thermal via early in the processor design process could address the trade-off between thermal and electrical performance and provide optimal floorplans for next-generation electronic systems.

Chapter 1: INTRODUCTION

1.1 Thermal Management Challenges for Advanced Electronics

The trends of semiconductor technology toward shrinking feature size, increasing transistor density, and three-dimensional (3D) integration are making the heat dissipation of electronics ever more challenging. For the past 20 years, the development of new process technologies and device structures scale the minimum feature size of transistors by approximately 0.7 times every two years as shown in Figure 1.1(a) [1].

While the size of a transistor continuously decreases, the area of a die remains relatively unchanged, and the transistor density increases dramatically, which leads to a significant increase in power density. Figure 1.1(b) shows the power densities for various processors developed over the past 40 years. When the power density exceeds 100 $W \cdot cm^{-2}$, heat dissipation becomes a major challenge and device engineers have been forced to increase the number of cores to keep increasing the overall performance [2]. Moreover, the power distribution is highly non-uniform, which creates regions with elevated heat flux that can be in the order of 1 $kW \cdot cm^{-2}$ [3]. For high-power semiconductor devices, where the energy processed and dissipated is much larger than typical logic chips, the hot spot heat flux can be even higher. In the double-diffused metal-oxide-semiconductor (DMOS), the transient power density can reach 40 $kW \cdot cm^{-2}$ [4]. In the GaN-based devices, 1 W power is dissipated in a footprint of 0.5 μm × 0.5 μm, resulting in a power density of 4 $MW \cdot cm^{-2}$ and a temperature rise of 100 °C [5]. The hot spot temperature limits the device's performance and compromises reliability. The thermal management of hot spots is the key to improve a device’s efficiency.

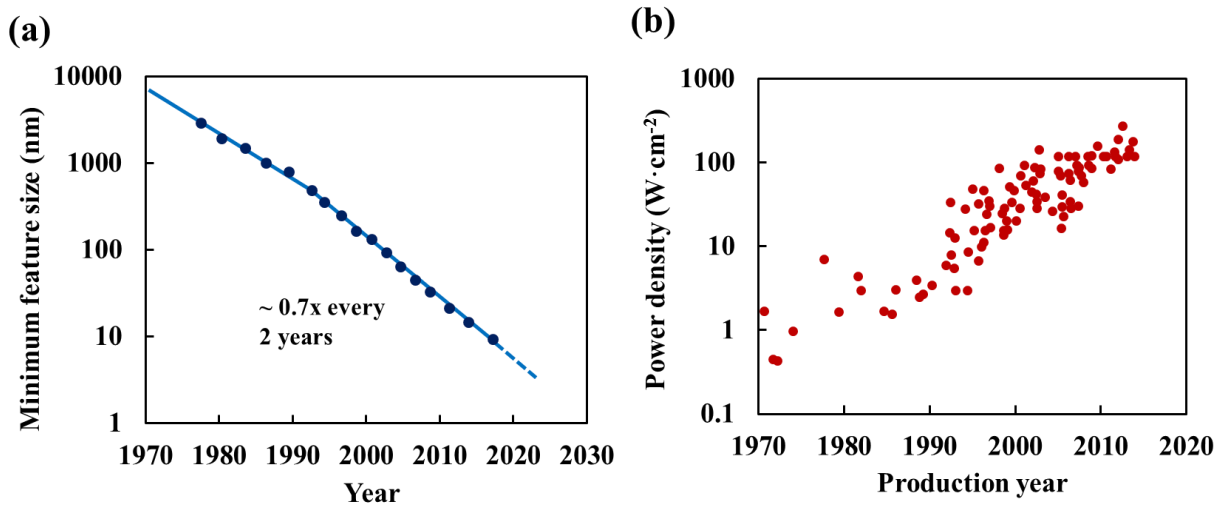

Figure 1.1 (a) The scaling trend of minimum feature size for Intel logic chips. Image adapted from [1] (b) Power densities for various commercial processors over the past 40 years. Image adapted from [2].

As the transistor size keeps shrinking, the development of new technology nodes becomes slower due to the increased process complexity. Moreover, as the minimum feature size approaches 5-7 nm range, it will be difficult to operate any transistors based on MOS due to the physical limitation [6]. To continue the success of semiconductor devices, stacking the dies on top of each other to fully utilize the vertical dimension to increase the transistor density becomes a promising solution.

In three-dimensional integrated circuits (3D ICs), through silicon vias (TSVs) run across the silicon die to provide electrical connections between active layers. Compared to 2D or 2.5D package platforms, 3D integration provides clear advantages in lowering latency, reducing power consumption, increasing interconnect bandwidth, and enabling heterogeneous integration [7]. However, thermal management has become a severe problem for 3D ICs as a direct result of the stacked structure.

As shown in Figure 1.2(a), for 2D ICs, the heat generated from the active circuits can be easily dissipated through the bulk silicon die to the heat sink. While for 3D ICs, the thermal resistance increases due to the stacked dies and interconnection layers as shown in Figure 1.2(b). The power consumption of 3D IC is expected to decrease due to the reduced wirelength, while the power density increases due to the high number of active devices per unit volume [8]. Heat removal through stacked dies is also a problem. The interconnect layers usually consist of micro-bumps and underfills, which have thermal conductivities of around 40 $W \cdot m^{-1}K^{-1}$ and 1.5 $W \cdot m^{-1}K^{-1}$, respectively, that are much lower compared to that of the bulk silicon (150 $Wm^{-1}K^{-1}$) [9]. Moreover, the die thickness in 3D ICs is also constrained by system configuration or TSV design, which affects the thermal spreading effect significantly [7]. For the thermal management of 3D ICs, it is hard to directly cool the stacked chips or dissipate heat laterally from the dies.

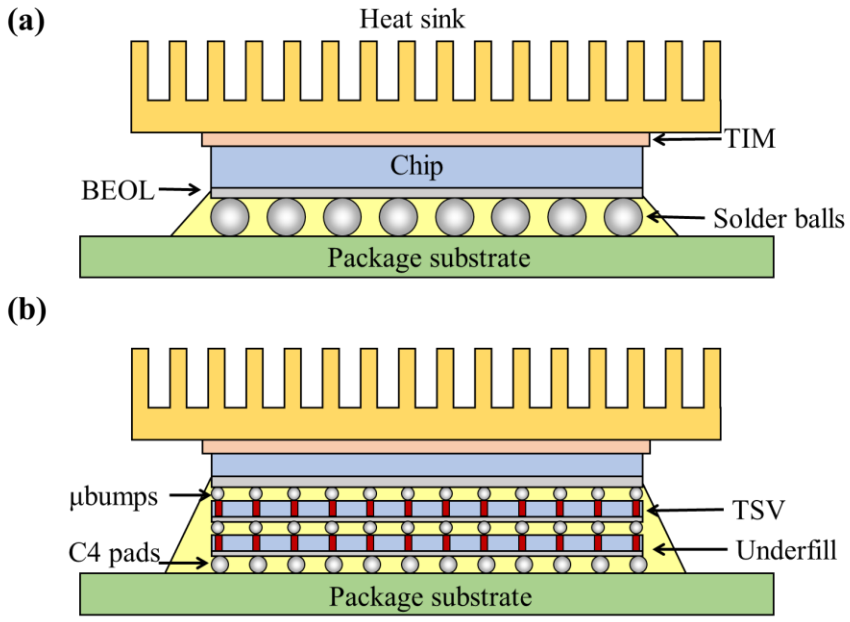

Figure 1.2 (a) The package structure of a 2D IC. BEOL and TIM represent back end of line and thermal interface material, respectively. (b) The package structure of a 3D IC. Images adapted from [8].

1.2 Thermoelectric Cooling Devices

1.2.1 Introduction to the thermoelectric effect

The thermoelectric effect describes direct conversion between thermal and electrical energy, which involves three phenomena: the Seebeck effect, the Peltier effect, and the Thomson effect [10,11]. Thermoelectric power generators produce electrical energy using a temperature gradient based on the Seebeck effect, while thermoelectric coolers (TECs) use electrical energy to provide a temperature gradient based on the Peltier effect. The Thomson effect is the heat absorption or release in a medium carrying an electrical current while sustaining a temperature gradient and is a result of the temperature dependence of the Seebeck coefficient.

The Seebeck effect is shown in Figure 1.3(a). An open-circuit voltage can be generated when two dissimilar conductors are jointed at two points with a temperature gradient. The Seebeck coefficient is defined as $S = \lim_{\Delta T \to 0} \frac{\Delta V}{\Delta T}$. With a known Seebeck coefficient, the temperature difference can be measured by measuring the voltage difference.

The Peltier effect is shown in Figure 1.3(b). When two dissimilar conductors are connected and an electrical current is flowing across them, heat will be generated or absorbed at the interface at a constant rate. The heat rate is directly proportional to the applied current I and the Peltier coefficient Π as: $q_{Peltier} = \Pi_{AB} I$, and changes sign if the current changes direction. The Peltier effect and the Seebeck effect are related as: $\Pi_{AB} = S_{AB} T$, where T is temperature.

An example of the Thomson effect is shown in Figure 1.3(c). When an electrical current is flowing through a conductor with a temperature gradient over its length, heat will be absorbed or released depending on the directions of the current and temperature gradient. The volumetric heat generation can be expressed as: $q'''_{Thomson} = -\mu_T \nabla T j$, where μ_T is the Thomson coefficient, and j

is the current density. The Thomson coefficient can be derived from the Seebeck coefficient as: $\mu_T = T\frac{dS}{dT}$.

The performance of a thermoelectric material is usually defined using the thermoelectric figure of merit $zT = \frac{S^2\sigma}{k}T$, where S, σ, and k are the Seebeck coefficient, electrical conductivity, and thermal conductivity, respectively [12].

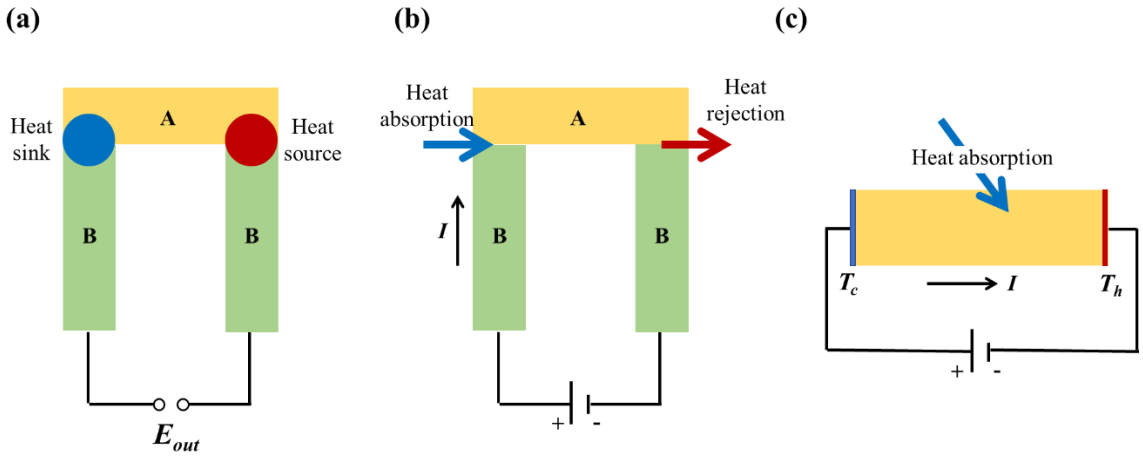

Figure 1.3 (a) Schematic of the Seebeck effect. (b) Schematic of the Peltier effect. (c) Schematic of the Thomson effect. When the current and temperature gradient is in the same direction, heat is absorbed with a positive Thomson coefficient.

1.2.2 Thermoelectric cooling devices for hot spot management

Thermoelectric cooling devices provide solid-state operation and have shown great promise for the thermal management of high heat flux hot spots with sizes in the order of tens or hundreds of micrometers.

A conventional TEC consists of an array of series connected p-type and n-type thermoelectric elements and electrical conductors. Figure 1.4 shows the basic schematic of a TEC

with one p-type and one n-type leg. A DC electrical power is used to activate the TEC. When the electrons move from the electrical conductor to the p-type thermoelectric elements or move from the n-type thermoelectric element to the electrical conductor, heat is released at the interface as electrons are dropped down to a lower energy level. When the electrons move from the p-type thermoelectric element to the conductor or move from the conductor to the n-type thermoelectric element, heat is absorbed at the interface as electrons are bumped to a higher energy level. The thermoelectric cooling performance of a TEC is related to the TEC configuration and thermoelectric properties of the materials.

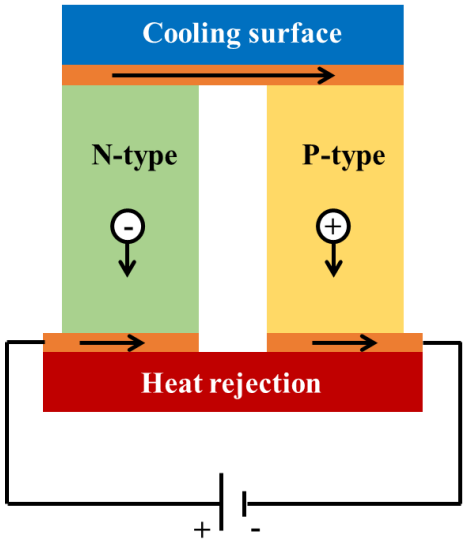

Figure 1.4 The basic schematic of a TEC with one n-type and one p-type leg.

Commercial thermoelectric coolers can only provide a cooling flux in the order of 10-100 $W \cdot cm^{-2}$, limiting its application for high heat flux hot spots [13]. To increase the cooling flux, Dr. Bar-Cohen and his group have developed mini-contact enhanced TECs to concentrate the cooling flux over a small area [14,15]. A 5 °C temperature reduction has experimentally demonstrated for a 613 $W \cdot cm^{-2}$ hot spot. Later, a micro-contact TEC with a pillar directly etched in the substrate is

developed to reduce the thermal contact resistance between the micro-contact and the substrate [16,17]. Figure 1.5(a) shows the experimental setup of the micro-contact enhanced TEC [17]. The hot side of the thermoelectric module is attached to a liquid cooled plate. The cold side of the thermoelectric module provides a cooling flux of 66 $W \cdot cm^{-2}$, which is in contact with the SiC micro-pillar (500 μm × 500 μm). An infrared (IR) camera is used to capture the temperature distribution in the SiC substrate, while the actual hot spot temperature is determined by the change in the resistivity of the Platinum heater. Figure 1.5(b) and (c) show the temperature distribution change with TEC off and on. The temperature change of a 200 × 200 μm^2 hot spot with a heat flux of 5 $kW \cdot cm^{-2}$ is measured with RTD (resistance temperature detector), which can be reduced by 12 °C when the TEC is on.

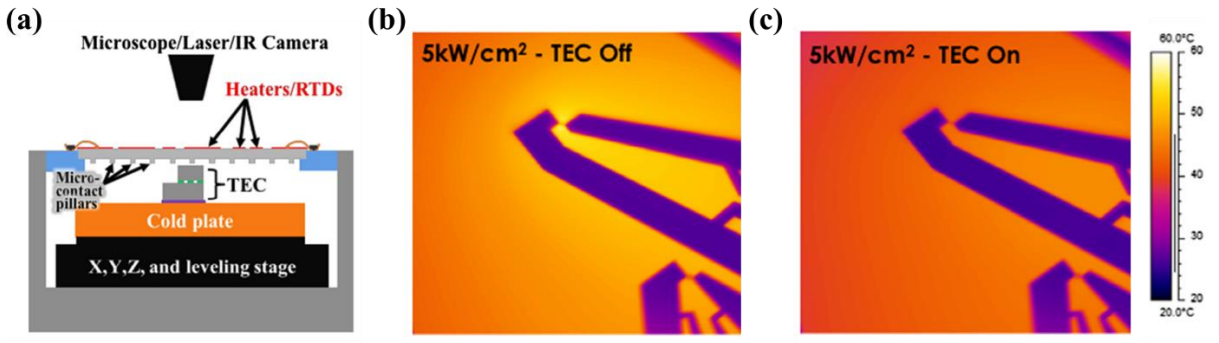

Figure 1.5 (a) Schematic of the micro-contact testing apparatus. IR images of the temperature distribution in the SiC substrate with TEC (b) on and (c) off. Images adapted from [17].

Commercial thermoelectric materials are usually based on alloys of Bi_2Te_3 with Sb_2Te_3 (p-type) and Bi_2Te_3 with Bi_2Se_3 (n-type) that have a room temperature zT around 1. Low dimensional materials such as quantum dot structures or superlattices provide new opportunities to manipulate the electrical and thermal properties of a material [18].

Dr. Shakouri and co-workers have developed thin film SiGe/Si and SiGeC/Si microrefrigerators based on superlattice structures fabricated by molecular beam epitaxy [19–23]. Figure 1.6 (a) shows the schematic of a superlattice-based microrefrigerator. A probe is used to send electrical current to the superlattice through the metal contact. A secondary metal contact is fabricated at the back side of the silicon chip to increase the thermal resistance between the heating and cooling junctions. The 3D thermal and current spreading effects provide a high cooling flux. The SiGeC/Si superlattice micro-cooler with a cooler size of 40 × 40 μm^2 can provide temperature reductions of 2.8 °C and 6.9 °C at 25 °C and 100 °C, respectively, which correspond to a cooling flux in the order of 1 $kW \cdot cm^{-2}$ [19].

Chowdhury *et al.*, have fabricated TECs based on nanostructured Bi_2Te_3 thin film superlattice that is grown by metal-organic chemical vapor deposition on GaAs substrates [24]. The final TEC has 7 × 7 p-n couples with a total dimension of 3.5 × 3.5 × 0.1 mm^3 as shown in Figure 1.6(b). The TEC is later integrated between a Si chip and a heat spreader and can provide a 15 °C temperature reduction for a 1300 $W \cdot cm^{-2}$ hot spot.

Bulman *et al.* have achieved a cooling flux of 258 $W \cdot cm^{-2}$ using thin film Bi_2Te_3-based superlattice thermoelectric modules [13]. The Bi_2Te_3 superlattice is fabricated using metalorganic chemical vapor deposition and has a thickness of around 8 μm. Su *et al.* have demonstrated a planar TEC based on nanograined SiGe thin film as shown in Figure 1.6(c) [25,26]. A maximum cooling of 10.3 °C is achieved in the single-stage microrefrigerator with a power consumption of 56 μW, while a maximum cooling of 11.2 °C is achieved in the two-stage microrefrigerator with a power consumption of 0.41 mW at room temperature.

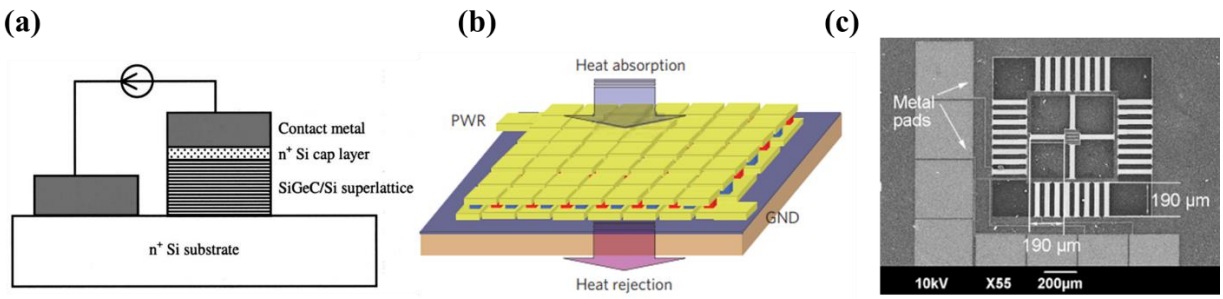

Figure 1.6 (a) Schematic of the SiGeC/Si microcooler. Image adapted from [19] (b) Schematic of the 7 × 7 superlattice thin-film thermoelectric array. Image adapted from [24]. (c) Scanning electron microscope (SEM) image of the two-stage nanograined SiGe thin film microrefrigerator. Image adapted from [25].

Silicon-based TECs have been developed due to the clear advantage in the fabrication process and a high power factor ($S^2\sigma$). Zhang *et al.* have experimentally demonstrated a silicon-based monolithic cooler as shown in Figure 1.7(a) [27]. The bulk silicon is p-type doped with a doping concentration around 10^{19} cm^{-3} and has an electrical resistivity in the range of 0.001 ~ 0.006 Ω·cm. A metal layer of Pt/Al/Pt/Au with a thickness of 0.1/1.0/0.1/1.5 μm is deposited as the metal contact for the current supply. The temperature reduction for a 40 × 40 μm^2 micro-cooler at room temperature is 1.2 °C, which is equivalent to a cooling flux of 580 $W \cdot cm^{-2}$.

Wang *et al.* have theoretically explored the cooling performance of a silicon-based lateral TEC [28]. At 100 °C, it is found that the silicon micro-cooler with 100 μm × 100 μm cooler size can achieve a peak cooling of 6.2 °C, which is equivalent to a cooling flux of 1 $kW \cdot cm^{-2}$. Wang *et al.* further investigate the cooling performance of bulk silicon micro-cooler on a 70×70 μm^2, 680 $W \cdot cm^{-2}$ hot spot [29]. The schematic is shown in Figure 1.7(b). A 3D analytical thermal model of the silicon chip, including the localized Peltier cooling, Peltier heating, Joule heating, hot spot and background heating, and conductive/convective cooling is developed to predict the hot spot

temperature change. With the optimal conduction, the hot spot temperature can be reduced by 3 °C.

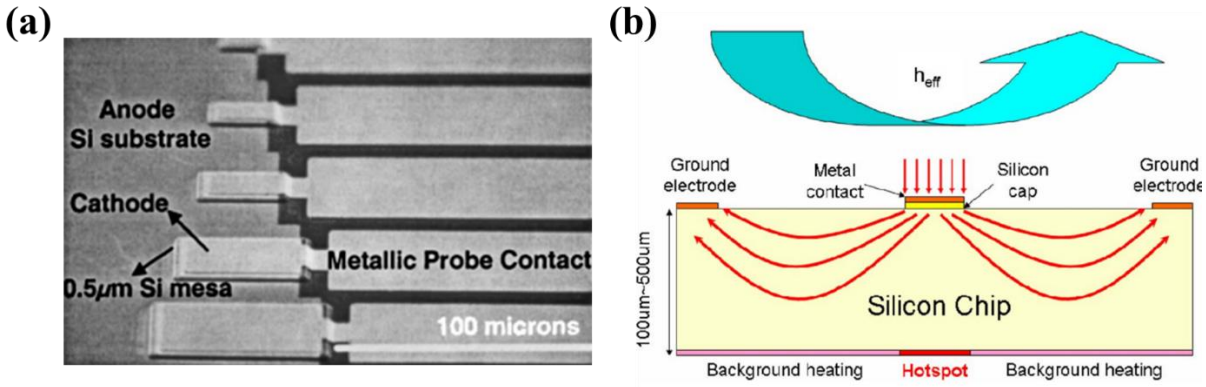

Figure 1.7 (a) SEM image of the silicon micro-cooler array. Image adapted from [27]. (b) Silicon thermoelectric micro-cooler for on-chip hot spot cooling. The arrows indicate the current direction. Image adapted from [29].

Manno *et al.* have fabricated the bulk silicon-based TEC as shown in Figure 1.8(a) [30]. A 300 nm SiO_2 is used as the insulation layer and a 1 μm Au is used as the electrical conductor. The temperature distribution of the TEC is measured using an IR camera. The device temperature distribution of a 500 μm cooler with/without current is shown in Figure 1.8(b), which also shows parasitic effects, such as Joule heating generated at the solder pads. Due to the low emissivity of the metal electrodes, it is hard to measure the cooler temperature, and the Peltier cooling temperature reduction in the surrounding silicon substrate is measured to be around 0.5 °C.

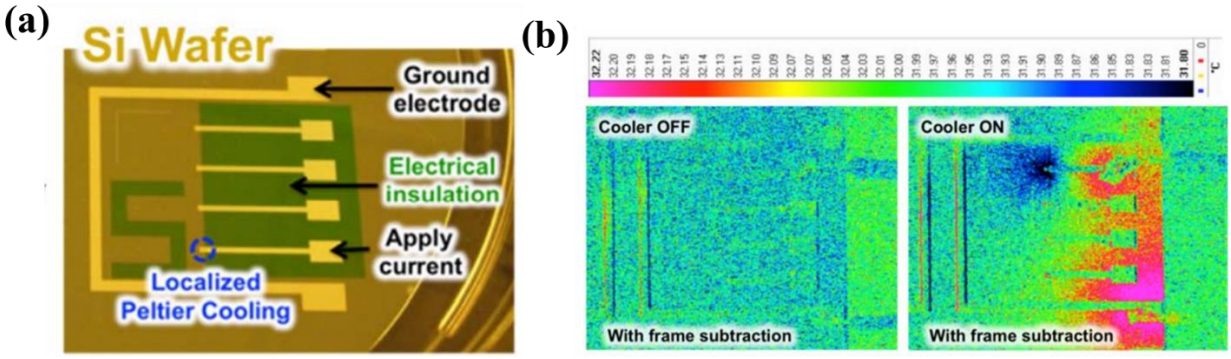

Figure 1.8 (a) Photograph of monolithic thermoelectric cooler fabricated on a silicon wafer. (b) IR images showing the temperature distribution on the silicon chip when the cooler is off and on. Images adapted from [30].

The hot spot cooling performance of the silicon-based TEC is also measured. The test setup involves the silicon cooler, an IR camera, an electrical power supply, and a laser heat source as shown in Figure 1.9(a). The hot spot is generated by a laser on the backside of the silicon wafer with a heat flux of around 15 $W \cdot cm^{-2}$.

The transient response of the hot spot temperature with TEC is also investigated. Figure 1.9(b) shows the hot spot temperature as a function of time. When the cooler is activated with a 0.5 A applied current, the hot spot temperature immediately reduces and approaches its steady-state value. Figure 1.9(c) shows the time-dependent hot spot temperature with a current pulse that has a magnitude three times greater than the optimal steady-state applied current. With the current pulse, the hot spot temperature reduces immediately due to the increased Peltier cooling, and gradually increases due to the diffusion of the Joule heating. When the current is removed, there is a sharp increase in hot spot temperature, which is caused by the removal of Peltier cooling but continued diffusion of the Joule heating.

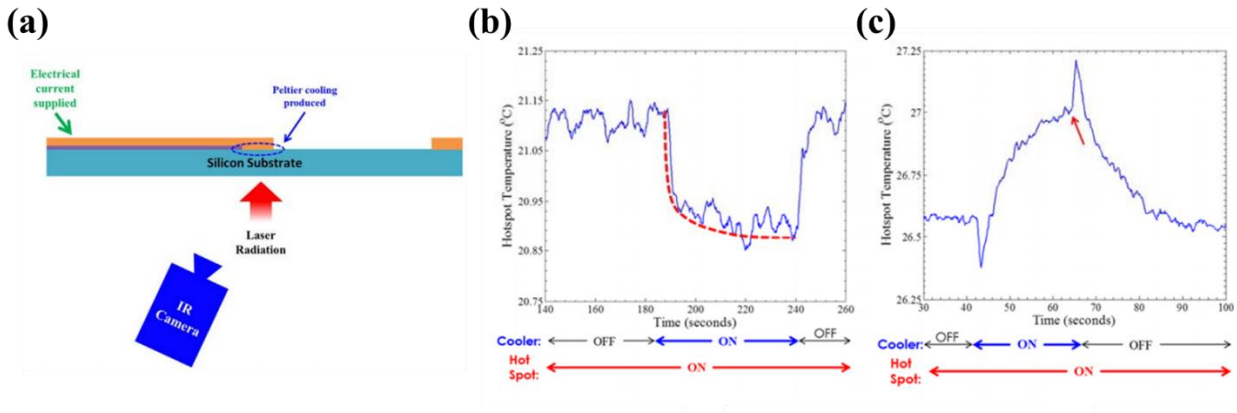

Figure 1.9 (a) Schematic of the measurement setup used to test the hot spot cooling capability of the silicon micro-cooler. Hot spot temperature reduction over time with (b) optimal current under steady-state and (c) a current pulse of three times large magnitude than that of the optimal current under steady-state. Images adapted from [30].

1.3 Silicon-based thermoelectric materials

1.3.1 Size effect in silicon

As the most widely used semiconductor material, silicon has recently received much attention in thermoelectric applications due to the advantages of its abundance, non-toxicity, and easy integration in electronics [31].

The lattice thermal conductivity of silicon can be obtained using kinetic theory as $k = \frac{1}{3}C\upsilon\Lambda$, where C, υ, and Λ are the volumetric heat capacity, speed of sound, and phonon mean free path (MFP), respectively [32]. The phonon MPF represents the average distance a phonon travels without scattering with other phonons and can be calculated using Matthiessen's rule as $\frac{1}{\Lambda} = \frac{1}{\Lambda_U} + \frac{1}{\Lambda_d} + \frac{1}{\Lambda_{e-ph}} + \frac{1}{\Lambda_b}$, where Λ_U, Λ_d, $\Lambda_{e\text{-}ph}$, and Λ_b represents the phonon MFP determined by the Umklapp, defect, electron-phonon, and boundary scatterings. The first three terms are intrinsic

phonon MFP in bulk materials and the last term becomes much more important at very low temperatures or with small critical dimensions. Silicon nanostructures are promising for thermoelectric applications because of the difference in the average MFP between electrons and phonons in silicon. It is possible to reduce the thermal conductivity without significantly impact the electrical conductivity.

The reduced thermal conductivity from its bulk values has been demonstrated in silicon micro- or nano- structures due to the boundary scattering. Ju and Goodson have measured the in-plane thermal conductivity of silicon thin films with thickness down to 74 nm and demonstrated a strong size effect in silicon thin film that the thermal conductivity can be reduced by 50% at room temperature [33].

Later, the thermal conductivity of silicon nanowires has also been studied and the measured thermal conductivity of silicon nanowires can be two magnitudes lower than that of the bulk value [34,35]. Hochbaum *et al.* have studied the impact of surface roughness and measured the thermal conductivity of rough silicon nanowires with diameters in the range of 20-300 nm. The thermal conductivity of a 50 nm diameter rough silicon nanowire is 100 times smaller than that of its bulk value, yielding a room temperature zT of 0.6 [36]. Silicon nanowires demonstrate significantly improved thermoelectric properties, however, their weak mechanical strength and strong dependence on both diameter and surface morphology remain as big challenges for thermoelectric applications [37].

1.3.2 Thermoelectric properties of holey silicon

Silicon thin films have demonstrated reduced thermal conductivity due to the size effect and the thermal conductivity can be further reduced by introducing microporous or nanoporous structures to enhance the phonon boundary scattering.

Song and Chen have measured the thermal conductivity of silicon membranes with periodic etched through-membrane pores [36]. The neck size of the microporous silicon is in the range of 2-10 μm. Its thermal conductivity is smaller than silicon thin film with the same thickness suggesting strong size effects.

Yu *et al.* have measured the thermal and electrical conductivities of silicon nanomesh with neck sizes of 18 nm and 23 nm and a thickness of 22 nm [38]. The silicon nanomesh has substantially reduced thermal conductivity as low as 1.9 $W \cdot m^{-1}K^{-1}$ at room temperature while preserving bulk-like electrical conductivity.

Tang *et al.* have fabricated and measured thermoelectric properties of holey silicon, where high-density nanoscopic holes are created in thin single-crystalline silicon membranes using block copolymer lithography [37]. The holey silicon has a pitch size (*p*) in the range of 55-350 nm and a neck size (*n*) in the range of 23-152 nm. The SEM image of holey silicon with 55 nm pitch size and 23 nm neck size is shown in Figure 1.10 (a).

The in-plane thermal conductivity of holey silicon is significantly reduced due to a strong "necking effect". The thermal conductivity reduces with smaller necks and the thermal conductivity of a 23 nm neck holey silicon can be as low as 1.73-2.03 $W \cdot m^{-1}K^{-1}$ at room temperature as shown in Figure 1.10 (b).

The electrical conductivity and Seebeck coefficient of the 23 nm neck size holey silicon are also measured with a doping concentration of 5×10^{19} cm^{-3} as shown in Figure 1.10(c). Since

the electron MFP in highly doped silicon is in the range of 1-10 nm and is smaller than the neck size, the power factor of holey silicon is moderately deteriorated compared to that of the silicon thin film. Due to the strong "necking effect" on the thermal transport, the *zT* of a 55 nm pitch size holey silicon at room temperature is increased to 0.4 as shown in Figure 1.10(d).

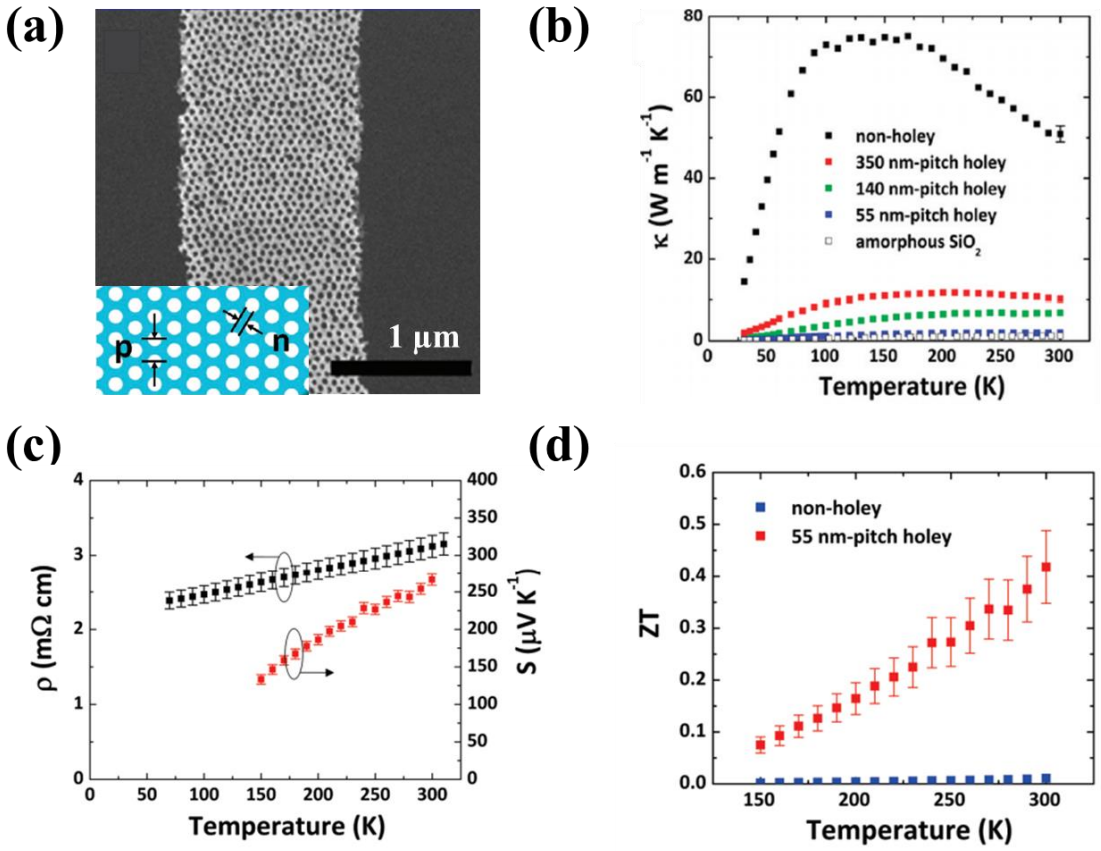

Figure 1.10 (a) SEM images of holey silicon with 23 nm neck size (*n*), 55 nm pitch size (*p*) and 100 nm thickness. (b) Temperature-dependent thermal conductivities of silicon thin film, amorphous silica, and holey silicon with different neck sizes. (c) Temperature-dependent electrical properties of boron-doped 23 nm neck holey silicon. (d) Temperature-dependent *zT* of silicon thin film and 23 nm neck holey silicon. Images adapted from [37].

Kim *et al.* [39] and Nakagawa *et al.* [40] have measured the thermal conductivity of silicon phononic crystal with a neck size in the range of tens or hundreds of nanometers. The measured thermal conductivity is significantly reduced compared to that of the bulk silicon.

Lee *et al.* have measured the cross-plane thermal conductivity of holey silicon with 20 nm neck size and a thickness in the range of 35 – 200 nm [41]. The holey silicon device is fabricated using block copolymer. The holey silicon with different thicknesses is fabricated by consuming silicon via thermal oxidation and buffered hydrofluoric acid etch. 3ω method is used to measure the thermal conductivity and the cross-sectional image of the holey silicon device is shown in Figure 1.11(a).

The length-dependent thermal conductivity of holey silicon is shown in Figure 1.11(b). With the same neck size, the strong length dependence of the thermal conductivity indicates that ballistic phonon transport dominates heat conduction in the cross-plane direction of holey silicon. A simple scaling model using the average MFP of bulk silicon is shown by the gray dashed line in Figure 1.11(b). A semiempirical model accounting for the phonon spectral dependence attributes the length-dependent data to the presence of long-wavelength phonons that have the MFP greater than the length of holey silicon nanostructures is shown by the gray dotted line in Figure 1.11(b).

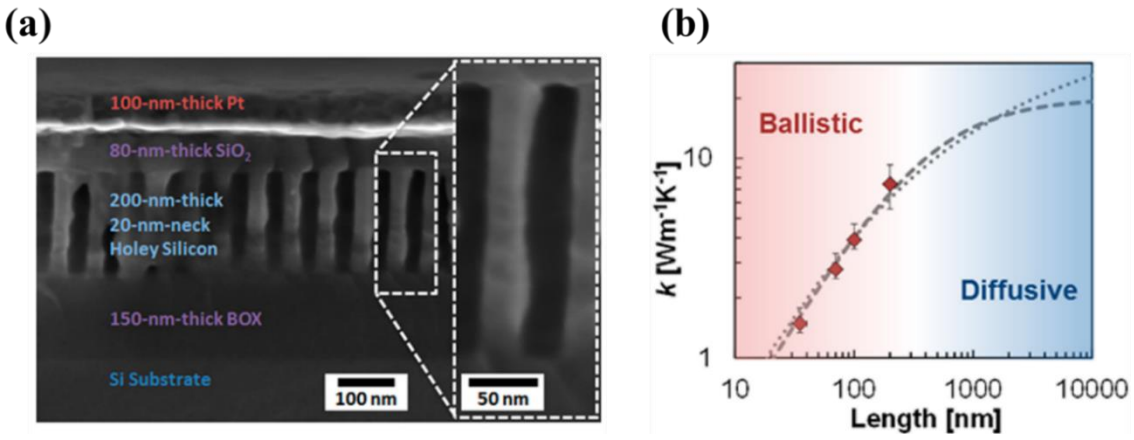

Figure 1.11 (a) Cross-plane thermal conductivity experimental setup. (b) Length-dependent thermal conductivity of holey silicon at room temperature with 20 nm neck size. The strong length dependence indicates that ballistic phonon transport dominates heat conduction in the length scale of 35-200 nm. Images adapted from [41].

Anufriev *et al.* have measured the thermal conductivity of phononic crystals with different neck sizes and lattice types [42]. They find that when the neck size is down to several tens of nanometers, thermal conductivity is controlled by the neck size and becomes independent of the surface-to-volume ratio, lattice type, and other geometrical parameters.

Lim *et al.* have simultaneously measured thermoelectric properties of holey silicon in one microdevice [43]. The holey silicon has a neck size in the range of 16-34 nm and a fixed pitch size of 60 nm. At room temperature, holey silicon with neck size of 16 nm provides the minimum measured thermal conductivity of 1.8 $W \cdot m^{-1}K^{-1}$, while the 24 nm neck size holey silicon provides the maximum zT values of 0.05. The zT value is mainly limited by the reduced electrical conductivity due to the ion implantation and surface defects but is still 5 times larger compared to that of the silicon thin film.

Lee *et al.* have measured the thermal conductivity of silicon nanomesh with periodic and aperiodic patterns [44]. They conclude that the phonon coherence is unimportant for thermal transport with periodicities of 100 nm or higher and temperatures above 14 K, while phonon backscattering, or size effect, is responsible for the thermal conductivity reduction.

Ma *et al.* have measured the electrical properties of holey silicon thin film with a neck size between 120 and 230 nm [45]. They find that while the electrical conductivity of holey silicon is close to that of the bulk silicon with comparable doping, the power factor of holey silicon at optimal doping is 50% lower than that of the bulk silicon due to the phonon drag effect that reduces

the Seebeck coefficient. They also predict that the holey silicon with 20 nm neck size and the optimal doping of 2×10^{19} cm^{-3} will provide the maximum *zT* of 0.5 at room temperature.

Liu *et al.* have measured the thermoelectric properties of holey silicon with neck size of 45 nm and doping concentration around 3-10 × 10^{19} cm^{-3} at elevated temperatures [46]. They find that the *zT* of holey silicon device is around 0.09 at room temperature and at least 0.29 at 650 K. The *zT* of holey silicon can be further improved by optimizing the feature sizes and using surface doping.

1.4 Outline of Doctoral Research

Chapter 2 presents the thermal conductivity anisotropy in holey silicon and its impact on the lateral thermoelectric cooling devices for hot spot thermal management. The effects of micro-cooler size, thermal conductivity anisotropy, and substrate size and thickness are evaluated in detail. Chapter 3 presents the TSV-integrated holey silicon-based TEC that combines passive and active cooling solutions. This chapter also explores the metal-filled holey silicon and its impact on the on-state and off-state TEC performance. Chapter 4 demonstrates the transient supercooling effect in the holey silicon-based lateral TEC. The effects of the Thomson coefficient, current pulse shapes, consecutive pulses, current pulse amplitudes, and durations are studied in detail. The transient performance of holey silicon-based TEC with phase change material fillers is also investigated. Chapter 5 presents the experimental demonstration of the holey silicon-based TEC. The holey silicon TEC is fabricated through standard semiconductor processes, and its performance is measured through infrared thermography. The steady-state and transient performances of holey silicon are investigated in detail. Chapter 6 demonstrates a floorplan optimization algorithm for the thermal management of 3D ICs to address the trade-off between

thermal and electrical performance. The impacts of TTSVs on the wirelength, area, and peak temperature of the 3D IC are investigated in detail. Chapter 7 offers concluding remarks on the thermal management of hot spots through holey silicon-based active thermoelectric cooling and TTSV-based passive cooling strategies. The opportunities for future research are also discussed.

Chapter 2: Thermal Conductivity Anisotropy in Holey Silicon Nanostructures and Its Impact on Thermoelectric Cooling

Artificial nanostructures have improved prospects of thermoelectric systems by enabling selective scattering of phonons and demonstrating significant thermal conductivity reductions. While the low thermal conductivity provides necessary temperature gradients for thermoelectric conversion, the heat generation is detrimental to electronic systems where high thermal conductivity is preferred. The contrasting needs of thermal conductivity are evident in thermoelectric cooling systems, which call for a fundamental breakthrough. In this chapter, we show a silicon nanostructure with vertically etched holes, or holey silicon, uniquely combines the low thermal conductivity in the in-plane direction and the high thermal conductivity in the cross-plane direction, and that the anisotropy is ideal for lateral thermoelectric cooling. The low in-plane thermal conductivity due to substantial phonon boundary scattering in small necks sustains large temperature gradients for lateral Peltier junctions. The high cross-plane thermal conductivity due to persistent long-wavelength phonons effectively dissipates heat from a hot spot to the on-chip cooling system. Our scaling analysis based on spectral phonon properties captures the anisotropic size effects in holey silicon and predicts the thermal conductivity anisotropy ratio up to 20. Our numerical simulations demonstrate the thermoelectric cooling effectiveness of holey silicon is at least 30% greater than that of high-thermal-conductivity bulk silicon and 400% greater than that of low-thermal-conductivity chalcogenides; these results contrast with the conventional perception preferring either high or low thermal conductivity materials. The thermal conductivity anisotropy is even more favorable in laterally confined systems and will provide effective thermal management solutions for advanced electronics.

2.1 Introduction

Recent trends toward nanoscale and high power electronics have made heat dissipation from local hot spots to heat sink structures increasingly challenging [47–50]. Among various thermal management solutions, thermoelectric cooling offers unique attributes including solid-state operation [51] and system scalability [52] that are particularly attractive for addressing the local heat dissipation issues [3,24,53]. While advances in thermoelectric materials through nanostructuring and controlled doping have made significant progress in improving the figure of merit [54,55], most materials are based on complex semiconductors [55,56] and low-dimensional structures [57,58] that are incompatible with microelectronic processes. Silicon, on the other hand, offers clearly favorable attributes that facilitate the integration with existing microelectronic processes. However, the high thermal conductivity of silicon has worked against conventional metrics of thermoelectric applications, in which large temperature gradients are desirable. In recent studies, silicon nanostructures have demonstrated significant thermal conductivity reductions and improved the prospects of thermoelectric technology [36,37,59]. The low thermal conductivity nanostructures, however, are not favorable for cooling electronics, and the contrasting needs of thermal conductivity are evident in lateral thermoelectric cooling systems. Using bulk silicon for lateral thermoelectric cooling [29], the high thermal conductivity will require a large system size to maintain the necessary temperature gradients for the Peltier junctions. Using conventional nanostructures, the low thermal conductivity will limit the heat dissipation. Here we show a silicon nanostructure with vertically etched holes, or holey silicon [37,41,43], uniquely combines the low thermal conductivity in the in-plane direction and the high thermal conductivity in the cross-plane direction, and that the anisotropy is ideal for lateral thermoelectric cooling. In this chapter, we identify the fundamental mechanisms of anisotropic thermal conductivities in the in-plane and the

cross-plane directions of holey silicon using spectral phonon transport theories and develop size dependent models to predict the impact of the anisotropy in lateral thermoelectric cooling systems. We further evaluate the thermoelectric cooling effectiveness of holey silicon, in comparison to other material systems, at varying dimensions and attribute its excellent performance to the thermal conductivity anisotropy.

2.2 Analytical and Numerical Modeling Methods

2.2.1 Cross-plane and in-plane thermal transport in holey silicon

The cross-plane thermal conductivity of holey silicon has been characterized by experiments, for holey silicon with a neck size of 20 nm, a pitch size of 60 nm, and a thickness ranges of 35-200 nm, the cross-plane thermal conductivity ranges from 1.5 to 7.5 $W \cdot m^{-1}K^{-1}$ [41]. Size dependent thermal conductivities of silicon thin films and nanowires have been reasonably well understood by approximating the phonon mean free path (MFP) to a critical dimension such as the film thickness or the diameter [37,43,44,60,61]. For holey silicon, the cross-plane thermal conductivity is accurately described by the consideration of an effective cross-sectional area that accounts for the neck size and the pitch size [41]. Figure 2.1 shows a schematic of a holey silicon unit cell with the effective cross-sectional area that captures the dominant phonon boundary scattering effect. Here we have reproduced the spectral scaling model to predict the cross-plane thermal conductivity of holey silicon (k_{HS_z}) with varying neck sizes (n) and thickness (t):

$$k_{HS_z} = \int_0^{\omega_D} k_{z_\infty}(\omega, n) \times \left(1 + \frac{\lambda_{z_\infty}(\omega,n)}{t/2}\right)^{-1} d\omega \tag{2.1}$$

where ω is the phonon frequency, ω_D is the Debye cut-off frequency, and $k_{z_\infty}(\omega, n)$ and $\lambda_{z_\infty}(\omega, n)$ is the thermal conductivity and the phonon MFP of a silicon nanowire which can

be calculated by Landauer formalism [60]:

$$k_{z_\infty} = \frac{2L}{\pi^2 {d_{eff}}^2} \int_0^\infty \left(\frac{N_1(\omega)}{1+L/\lambda_l(\omega)} + \frac{N_2(\omega)}{1+L/d_{eff}}\right) \frac{\hbar^2\omega^2}{k_B T^2} \times \frac{\exp(\hbar\omega/k_B T)}{(\exp(\hbar\omega/k_B T)-1)^2} d\omega \quad (2.2)$$

where T is the temperature, L is the length and d_{eff} is the effective diameter that represents an equivalent cross-sectional area of a nanowire. For each holey silicon, the effective diameter is determined by the neck size (n) and the pitch size (p) by $d_{eff} = \sqrt{\frac{\sqrt{3}}{\pi}p^2 - \frac{(p-n)^2}{2}}$. The use of d_{eff} in the scaling model is known to accurately captured the thermal conductivity data of holey silicon. $\lambda_l(\omega)$ is the frequency dependent MFP due to lateral boundary scattering which can be expressed as $\lambda_l(\omega) = 4\pi^2 \times (4B\frac{\hbar^2}{d^3}\left(\frac{\omega}{\omega_D}\right)^2 + AB\frac{\hbar^2}{a^2 d}(\frac{\omega}{\omega_D})^4)^{-1}$ [62], where A and B are dimensionless fitting parameters and a is the lattice spacing. The $\lambda_{z_\infty}(\omega, n)$ is determined by combining the lateral boundary scattering with bulk silicon Umklapp scattering ($\lambda_U(\omega)$) and point-defect scattering ($\lambda_D(\omega)$) [41,63]:

$$\lambda_{z_\infty}(\omega, n) = (\lambda(\omega)^{-1} + \lambda_U(\omega)^{-1} + \lambda_D(\omega)^{-1})^{-1} \quad (2.3)$$

The total number of modes at a given frequency is defined as $N = 4 + C(\frac{d}{a})^2 \times (\frac{\omega}{\omega_D})^2$ where C is the fitting parameter [62]. $N_1(\omega)$ is the number of modes with mean free path $\lambda_l(\omega)$ which is given by $N(\min(\omega, v/h))$, where h is the surface disorder and v is the average phonon group velocity. $N_2(\omega)$ is the number of modes with MFP limited to d which is defined as $N - N_1$.

The in-plane thermal conductivity of holey silicon with varying neck sizes have been characterized in separate studies [37,43], but analytical models have not been presented to capture the scaling trend. Consistent with the scaling model approach that captured the length (thickness) dependence in the cross-plane thermal conductivity of holey silicon, we extend the analysis to

predict the neck size dependence in the in-plane thermal conductivity. Based on the Matthiessen's rule [63,64] we can express the thermal conductivity in terms of MFPs. Assuming the properties of holey silicon do not change with varying *n* except for the MFP limited by boundary scattering between holes (λ_{holes}), we can show the in-plane thermal conductivity of holey silicon (k_{HS_x}) as follows:

$$k_{HS_x} = \frac{1}{3} Cv \left(\frac{1}{\lambda_U} + \frac{1}{\lambda_D} + \frac{1}{\lambda_{thickness}} + \frac{1}{\lambda_{holes}} \right)^{-1} = \frac{1}{3} Cv \left(\frac{1}{\lambda_{x_\infty}} + \frac{1}{\lambda_{holes}} \right)^{-1} = k_{x_\infty} \left(1 + \frac{\lambda_{x_\infty}}{\lambda_{holes}} \right)^{-1} \quad (2.4)$$

where λ_U is the MFP limited by Umklapp scattering, λ_D is the MFP limited by point-defect scattering. $\lambda_{thickness}$ is the MFP limited by boundary scattering at top and bottom surfaces and λ_{holes} is the MFP limited by boundary scattering at hole surfaces. k_{x_∞} is the in-plane thermal conductivity of holey silicon of infinitely long neck size, which corresponds to a silicon film with no holes. λ_{x_∞} is the average MFP of a silicon film and λ_{holes} is approximated as *n/2* assuming the average distance allowed for thermal transport in the in-plane direction is one-half of the neck size [41,65]. We use a spectral scaling model to account for the phonon frequency dependence [66,67] and predict the in-plane thermal conductivity of holey silicon as a function of the neck size and the thickness as follows:

$$k_{HS_x} = \int_0^{\omega_D} k_{x_\infty}(\omega, t) \times \left(1 + \frac{\lambda_{x_\infty}(\omega,t)}{n/2}\right)^{-1} d\omega \quad (2.5)$$

We use an adjusted Debye cut-off frequency (ω_D, ~52 THz) that is determined by the experimental data, as suggested by Mingo *et al* [63]. $k_{x_\infty}(\omega, t)$ and $\lambda_{x_\infty}(\omega, t)$ are the in-plane thermal conductivity and the phonon mean free path of silicon thin film. $k_{x_\infty}(\omega, t)$ is then computed by the Holland model [68]:

$$k_{x_\infty} = \frac{1}{3} \sum_j v_j^2 \int_0^{\frac{\theta_j}{T}} C_{V,j}(x_\omega, T)[\tau_j(x_\omega, T, t) \times F(\delta)] dx_\omega \quad (2.6)$$

The subscript j indicates transverse and longitudinal phonon modes, v_j is the phonon group velocity of different modes. $x_\omega = \hbar\omega/k_B T$ is the non-dimensional phonon frequency. $C_{V,j}(x_\omega, T)$ is the phonon specific heat per unit volume, Θ_j is the Debye temperature and $\tau_j(x_\omega, T, t)$ is the phonon relaxation time in the absence of the vertical phonon boundary scattering. The vertical boundary scattering effect is then captured by the reduction function [69–71]:

$$F(\delta) = 1 - \frac{3(1-s)}{2\delta}\int_1^\infty \left(\frac{1}{t^3} - \frac{1}{t^5}\right) \times \frac{1-\exp(-\delta t)}{(1-s\times exp(-\delta t)} dt \quad (2.7)$$

where $\delta = d/\lambda_{x_j}$, is the ratio of the thickness (d) for silicon thin films to the phonon mean free path ($\lambda_{x_j} = v_j \times \tau_j(x_\omega, T, t)$) and s is the specularity. The specularity s ranges from 0 to 1, indicating fully diffuse to fully specular surface conditions. In this manuscript, we assume the surface boundaries of holey silicon are fully diffuse (*s=0*) [72]. For transverse and longitudinal phonon modes, the $\lambda_{x_\infty}(\omega, t)$ is defined as $\lambda_{x_\infty}(\omega, t) = v_j \times \tau_j(x_\omega, T, t) \times F(\delta)$, respectively.

2.2.2 Numerical simulations of the on-chip cooling system

The device-level heat transfer and thermoelectric effects are simulated using ANSYS™, and the finite element simulations account for thermal conductivity size effects in holey silicon by using the properties predicted from the semi-classical phonon transport models (Eq. (2.1 - 2.7)). Figure 2.1 shows the structure of the holey silicon thermoelectric on-chip cooling system. The heat generation by electronics is modeled as a combination of 70 W·cm^{-2} background heating and 700 W·cm^{-2} hot spot heating, which is chosen as representative values for modern electronics and to be consistent with previous thermoelectric cooling studies [29,73,74]. A metal contact is integrated into the center as micro-cooler and a ground electrode is designed to carry electric current. For the

exploration of system dimensions, the micro-cooler size, lateral substrate size, and holey silicon substrate thickness are varied from 50 × 50 μm^2 to 500 × 500 μm^2, 12000 ×12000 μm^2 to 1000 ×1000 μm^2 and 50 to 150 μm, respectively. The top of the holey silicon undergoes convective heat transfer to 25 ^oC ambient air. In our simulations, we use a constant convection coefficient value of 8700 $W \cdot m^{-2}K^{-1}$ to represent the use of an advanced heat exchanger [29,74]. With moderate heat exchangers, we may expect a lower convection coefficient value [75], the impact of thermoelectric cooling will be greater due to increased temperature gradients within solids and the increase importance of thermoelectric effects. For p-type holey silicon, the whole system is activated by the electric current entering the metal contact, flowing laterally through the holey silicon substrate and exciting at the ground electrode. Inside p-type holey silicon, the flow of positive holes serves to transport the absorbed heat away from the micro-cooler/substrate interface and dissipates it at the secondary interface between holey silicon and ground electrode. Previous study revealed that the electric contact resistance between metal and highly doped silicon is between 1×10^{-11} and 1×10^{-10} $\Omega \cdot m^2$ [76,77], in this study, the electric contact resistance of 1×10^{-10} $\Omega \cdot m^2$ is applied.

A temperature cooling effectiveness (TCE) is defined to evaluate the cooling performance [29]:

$$\Delta T^* = \frac{T_{heating\ ON,\ cooling\ OFF} - T_{heating\ ON,\ cooling\ ON}}{T_{heating\ ON,\ cooling\ OFF} - T_{heating\ OFF,\ cooling\ OFF}} = \frac{\Delta T_{thermoelectric\ cooling}}{\Delta T_{hotspot\ heating}} \quad (2.8)$$

The $T_{heating\ ON/OFF,cooling\ ON/OFF}$ is the hotspot temperature when the hot spot heat flux is applied/not applied and the micro-cooler is working/not working. If $\Delta T^* >= 1$, the micro-cooler effectively cools down the hot spot to a temperature that is smaller than the case of background heating only. If $0 < \Delta T^* < 1$, the micro-cooler can reduce the hot spot temperature, but the

temperature is higher than is the case of background heating only. If $\Delta T^* <= 0$, the Joule heating generated by the applied current exceeds the thermoelectric cooling.

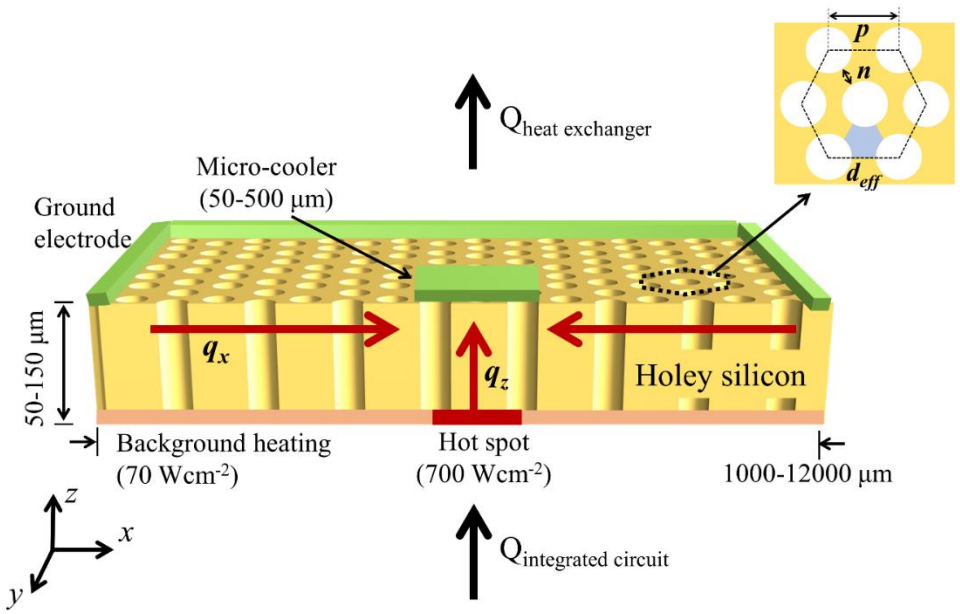

Figure 2.1 A holey silicon-based thermoelectric cooling system. The black arrows indicate heat flows from an integrated circuit chip to holey silicon substrate ($Q_{integrated\ circuits}$), and conventional heat flows to a heat exchanger in the vertical direction ($Q_{heat\ exchanger}$), respectively. The red arrows indicate the heat flow inside the holey silicon substrate in the lateral direction (q_x) and vertical direction (q_z). The holey silicon neck and pitch sizes are presented by n and p, respectively. The effective diameter (d_{eff}) and effective cross-sectional area of silicon nanowire and holey silicon is shown by the blue area.

2.3 Results and Discussion

2.3.1 Thermal and electrical properties of holey silicon

Figure 2.2(a) shows the cross-plane thermal conductivity prediction of holey silicon with neck sizes of 10 nm to 60 nm and thicknesses of 10 nm to 100 μm. The neck size determines the cross-sectional area of transport, and the phonon boundary scattering induced by the neck is

modeled equivalent to that of nanowire surface boundaries. Our cross-plane thermal conductivity predictions based on the spectral scaling model match the reported holey silicon data [41] and the nanowire data [60,78] and attribute the thickness dependence to the presence of low-frequency phonons that are persistent with lateral boundaries. This is done without using the bulk silicon thermal conductivity or the average mean free path as a fitting parameter.

Figure 2.2(b) shows a successful match between the modeling predictions of in-plane thermal conductivity and the reported data [37,43]. In the scales of large neck sizes, our model captures the thickness dependent thermal conductivities of bulk silicon [79] and thin films [43]. For holey silicon with small neck sizes, the thickness dependence disappears because the phonon boundary scattering with the neck dominates thermal transport. In the scales of small neck sizes (< 100 nm), the in-plane thermal conductivity of holey silicon has almost the same value regardless of the thickness, either 100 nm or 100 μm. Insert of figure 2.2(b) shows the thermal conductivity accumulation of 100 nm thick holey silicon at 300 K. Most of the heat is carried by phonons with a frequency larger than 4 THz, which corresponds to a wavelength of about 2 to 3 nm. This phonon wavelength is similar to the previous research of 23-nm neck size silicon nanomeshes [80]. Our modeling work does not consider any phonon coherence or wave related effects because the smallest dimension of holey silicon is 20 nm, which is much greater than the dominant phonon wavelength at room temperature and above [80]. Some 2D materials such as black phosphorous are known to have a thermal conductivity anisotropy due to suppressed phonon group velocities and zone folding effects [81], and multilayer stacks of 2D material may offer a strong thermal conductivity anisotropy. However, the 2D materials and superlattices [29] are not favorable for lateral thermoelectric cooling systems due to the low cross-plane thermal conductivity [80].

While the thickness governs thermal transport in the cross-plane direction, the neck size

governs the thermal transport in the in-plane direction, enabling the development of thermal conductivity anisotropy. By designing holey silicon with a large thickness and a small neck size, we can predict the thermal conductivity anisotropy that is preferable for thermoelectric cooling. The thermal conductivity anisotropy ratios, predicted by the spectral scaling models, for 100 μm-thick holey silicon with 10, 20, 40 and 60 nm neck sizes are 23, 13, 9 and 7, respectively. Although the 10 nm neck size holey silicon has the highest anisotropy ratio, the neck size needs to be larger than the electron mean free path, which is ranging between 1 ~ 15 nm in highly doped silicon [82] to maintain sufficient electrical properties [37]. For this reason, we choose the 20-nm neck size holey silicon for the numerical simulation. At the operation temperature of 100 °C, the p-type silicon with a doping concentration of is known to provide the best thermoelectric power factor [83,84], and the corresponding electrical properties are used in our simulations.

The in-plane thermal conductivity of holey silicon with 20 nm neck size reduces from 3 to 2 $W \cdot m^{-1}K^{-1}$ due to the extra phonon-dopant scattering [43]. Considering the influence of dopants, the anisotropy ratio of holey silicon with a neck size of 20 nm and a thickness of 100 μm is estimated as 20 and the predicted thermal conductivity set is {2, 2, 40} $W \cdot m^{-1}K^{-1}$ (k_x, k_y, k_z). In our thermoelectric device simulations, the effective thermal and electrical properties accounting for the porosity are used [37].

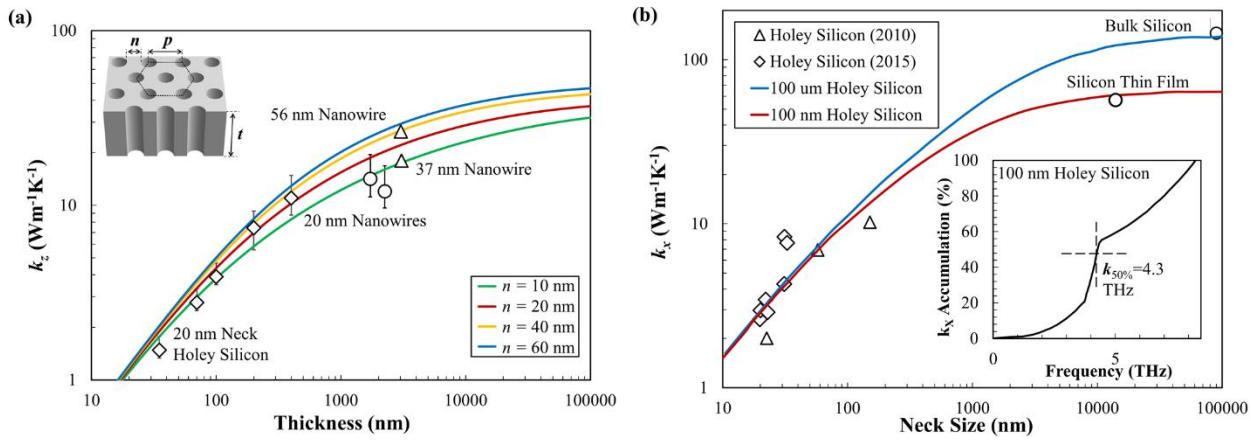

Figure 2.2 The spectral scaling models for in-plane and cross-plane thermal transport in holey silicon nanostructures. (a) k_z prediction of holey silicon with neck sizes of 10 to 60 nm and thickness of 10 to 100 μm at room temperature. Insert is the structure of holey silicon, n, p, and t represent the neck size, pitch size and thickness, respectively. The 56 nm and 37 nm silicon nanowire data is from [34] and the 20 nm nanowire data is from [60]. (b) k_x prediction of holey silicon with neck size changing from 10 to 10^5 nm and thickness of 100 nm and 100 μm at room temperature. Insert is the thermal conductivity accumulation plot, above 50% of the heat is carried by phonons with frequency over 4 THz which corresponds to a wavelength of 2 ~ 3 nm and is much smaller than the neck size. The 2010 holey silicon data is from [37], and the 2015 holey silicon data is from [43].

2.3.2 Effects of micro-cooler size and substrate thickness

As the applied current in thermoelectric cooling systems increases, there is an important trade-off between Peltier cooling (~I) and the Joule heating (~I^2). As shown in Figure 2.3(a), the optimal current strongly depends on the micro-cooler size to hot spot size ratio, and larger micro-coolers needs a higher applied current to reach the maximum cooling performance. Due to various heat transfer effects, thermoelectric cooling systems require careful optimization. We have performed simulations with various system dimensions to address the trade-offs and optimize the cooling performance (Figure 2.3(b)). There is a clear trade-off between thermoelectric cooling and Joule heating as a function of the micro-cooler size to the hot spot size ratio. For varying substrate thickness, there is a trade-off between the effects of heat spreading and the cross-plane thermal resistance [29,74]. The simulation results show that the competing effects yield the highest cooing effectiveness of 1.7 with a hotspot temperature reduction of 40 ^{o}C when the micro-cooler size and substrate thickness are 250×250 μm^2 and 100 μm, respectively.

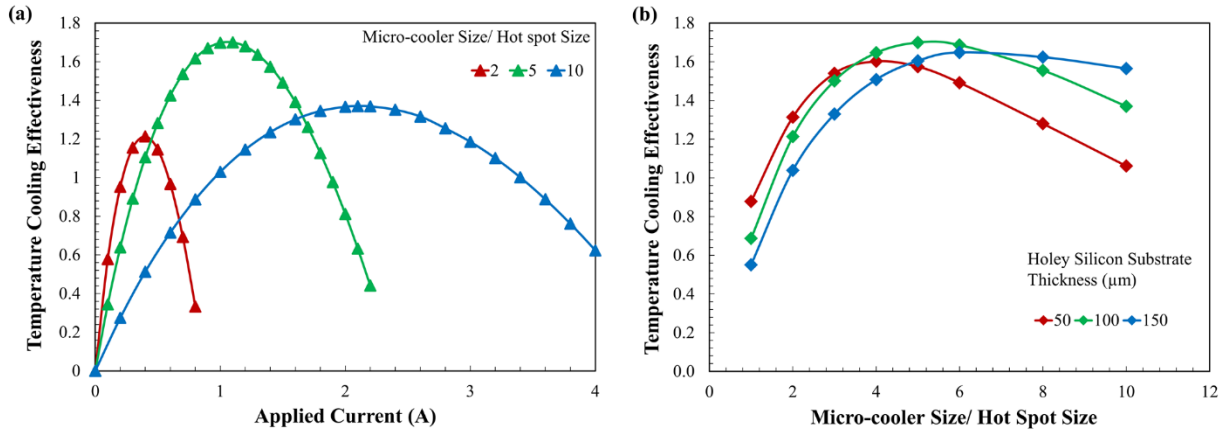

Figure 2.3(a) The temperature cooling effectiveness (TCE) as a function of applied current for varying thermoelectric cooling system dimensions. As the applied current increases, the TCE initially increases due to thermoelectric cooling and then decreases due to Joule heating. When the TCE reaches the maximum, the corresponding current is recorded as the optimal applied current of this design. (b) The optimal TCE of varying system dimensions. The micro-cooler size and holey silicon substrate thickness vary from 50 × 50 μm^2 to 500 × 500 μm^2 and from 50-150 μm, respectively.

2.3.3 Effects of thermal conductivity anisotropy

We fix the substrate size and hot spot size at 12000×12000 μm^2 and 50×50 μm^2 and set the micro-cooler size and substrate thickness at 250×250 μm^2 and 100 μm, respectively, as discussed in the last session. Under this geometry, we change the in-plane and cross-plane thermal conductivity from 1 to 110 $Wm^{-1}K^{-1}$ separately to evaluate the roles of thermal conductivity anisotropy. Figure 2.4(a) shows that for the cross-plane direction, the TCE increases with increase cross-plane thermal conductivity due to the facilitated heat transfer from hot spot to micro-cooler. Figure 2-4(b) shows that for the in-plane direction, the TCE decreases with increase in-plane thermal conductivity, because high in-plane thermal conductivity cannot maintain enough temperature gradients for Peltier effect. For comparison, the TCE of bulk silicon [29], nanocrystalline BiSbTe bulk alloy [57], and Ge [74] substrates are also simulated with the

optimized current. The nanocrystalline BiSbTe is known to have the highest thermoelectric figure of merit, but the low cross-plane thermal conductivity limits the heat dissipation. The Si and Ge based cooling systems have high thermal conductivities, which are good for heat dissipation but do not sustain enough lateral temperature gradient required for thermoelectric cooling. For holey silicon, its unique combination of low in-plane and high cross-plane thermal conductivities enables a low-temperature cooling junction and an efficient heat transfer path between the hot spot and the micro-cooler, making it ideal for on-chip thermoelectric cooling systems.

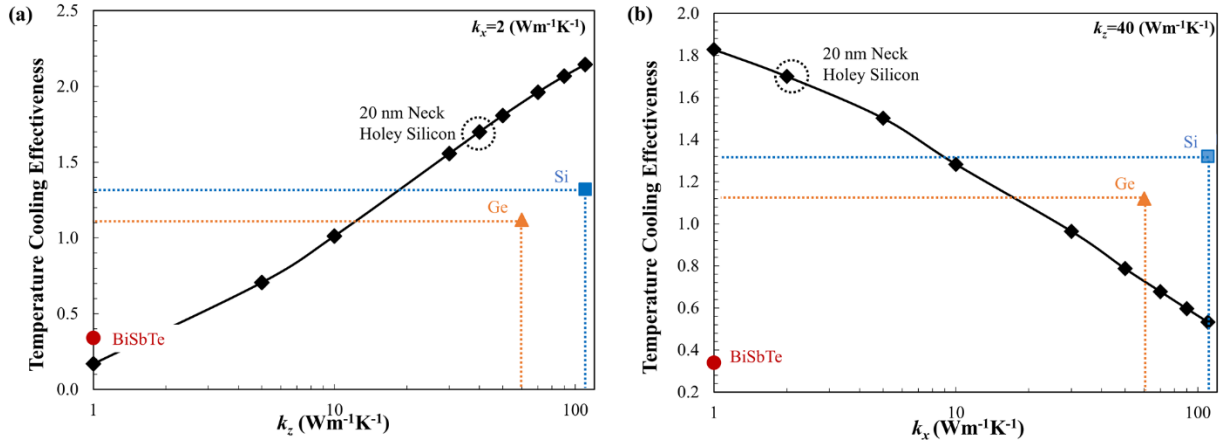

Figure 2.4 (a) The TCE increases as the cross-plane thermal conductivity changes from 1 to 110 $Wm^{-1}K^{-1}$ due to the facilitated heat transfer between micro-cooler and hot spot. (b) The TCE decreases as the in-plane thermal conductivity changes from 1 to 110 $W{\cdot}m^{-1}K^{-1}$ due to the insufficient temperature gradients in the lateral direction. The black circles represent the cooling effectiveness of 20 nm neck size holey silicon-based system. The blue, brown and red dots are the TCE of Silicon [29], Ge [74], and BiSbTe [57]-based system under the optimal condition.

2.3.4 Effects of lateral substrate size

The lateral substrate size effect is evaluated to address the scalability of electronic systems. While the micro-cooler size is fixed at 250×250 μm^2 and substrate thickness is fixed at 100 μm, the lateral substrate size is varied from 12000×12000 μm^2 to 1000×1000 μm^2. Figure 2.5(a) shows that for bulk silicon and Ge, the cooling effectiveness substantially decreases as the cooling system

is laterally confined. In contrast, the nanocrystalline BiSbTe and holey silicon-based system continues to offer effective cooling due to the low in-plane thermal conductivity. Figure 2.5(b) shows the temperature profiles of holey silicon and bulk silicon-based system with 1000×1000 μm^2 substrate size. For holey silicon based-system, when the micro-cooler is operating with 0.9 A optimal applied current (the corresponding input power is 0.07W), a temperature gradient more than 50 ^oC is maintained between the micro-cooler and the ground electrode because of the low in-plane thermal conductivity. The hot spot temperature is reduced by more than 30 ^oC. However, for the bulk silicon-based system with the same lateral substrate size and the same operation conditions, the temperature gradient between the micro-cooler and the ground electrode is less than 10 ^oC and the hot spot temperature reduction is less than 1 ^oC. The high thermal conductivity of bulk silicon limits the thermoelectric cooling performance while the low in-plane thermal conductivity of holey silicon allows thermoelectric cooling systems to maintain lateral temperature gradients required for the Peltier effects even in laterally confined systems, making them more attractive for compact electronics. For comparison to passive cooling systems, we have considered the use of copper as the substrate material. Under the same boundary conditions, a copper block provides a more uniform and lower temperature rise than the holey-silicon-based system when no current is applied. With the optimally applied current, the holey-silicon based thermoelectric cooling still provides a temperature reduction near the hot spot more than 20 ^oC more than the copper-based system while offering clear advantages in local cooling, active control, and device compatibility.

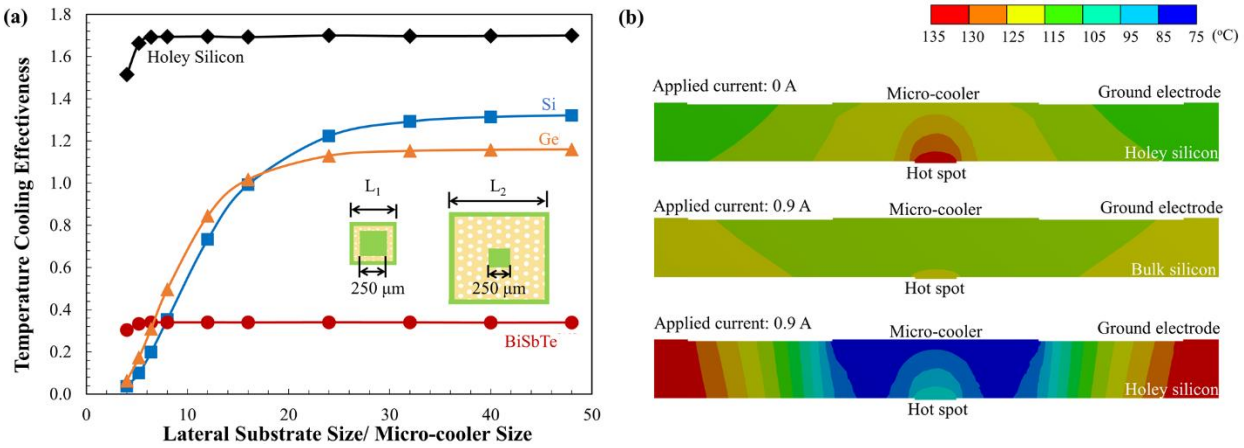

Figure 2.5 (a). TCE analysis of holey silicon, bulk silicon, Ge, and BiSbTe-based thermoelectric cooling systems of varying lateral dimensions. (b) Cross-sectional temperature profile of holey silicon and silicon-based systems with 250×250 μm^2 micro-cooler and 1000×1000 μm^2 lateral substrate. With the same applied current (0.9 A) and input power (0.07 W), the temperature gradient between micro-cooler and ground electrode of holey silicon-based system is 40 ^oC greater than bulk silicon-based system, and the hot spot temperature of holey silicon-based system is 15 ^oC lower than bulk silicon-based system.

2.4 Conclusions

This chapter demonstrates semi-classical spectral scaling models that capture the unique thermal conductivity anisotropy in holey silicon and points out the significant impact of anisotropy in thermoelectric cooling systems. The modeling results show the possibilities of designing holey silicon with a large anisotropy ratio and outperforming conventional materials that are traditionally considered as a better thermal conductor or a better thermoelectric material. The anisotropic holey silicon enables breakthroughs in thermal management of electronics, especially for laterally confined systems and for addressing local hot spots. The fundamental mechanisms of thermal conductivity anisotropy and its impact on thermoelectric cooling that are presented in this chapter provide new insights into understanding direction-dependent thermal transport properties and designing artificial nanostructures for advanced electronic systems.

Chapter 3: Thermal Conductivity Anisotropy in Holey Silicon Nanostructures and Its Impact on Thermoelectric Cooling

The trends toward higher power, higher frequency, and smaller scale electronics are making heat dissipation ever more challenging. Passive thermal management based on high thermal conductivity materials or through-silicon vias (TSVs) may not provide sufficient cooling for hot spots reaching 1 $kW \cdot cm^{-2}$, and active thermal management by thermoelectric cooling (TEC) may require large power consumption or suffer from a large off-state thermal resistance of thermoelectric materials. Here we address these issues by integrating a holey silicon-based TEC with a TSV that directly draws heat from a hot spot to combine active and passive cooling approaches. Our simulations of the TSV-integrated TEC demonstrate exceptional cooling performance, which reduces the hot spot temperature from 154 °C to 68 °C while dissipating a heat flux of 1 $kW \cdot cm^{-2}$ and consuming 0.5 W for TEC operation. The off-state hot spot temperature, 154 °C, is 24 °C lower than that of the same TEC with no TSV, and the on-state hot spot temperature, 68 °C, is 67 °C lower than that of the same TEC with no TSV. We also investigate the cooling prospects of metal-filled holey silicon by modeling the electron-phonon coupling and size dependent transport phenomena, which can further increase the thermal conductivity anisotropy and improve the TEC performance depending on the metal-to-silicon interfacial resistance. These results show the combined passive and active cooling in TSV-integrated TEC offers effective hot spot thermal management solutions for advanced electronics.

3.1 Introduction

Recent advances in device miniaturization and design complexity have posed increasing challenges in heat dissipation from local hot spots to large heat sinks [48,49,85]. Passive cooling solutions based on high thermal conductivity materials may not meet the increasing demand of local heat removal, particularly for hot spots reaching 1 $kWcm^{-2}$ and beyond [3]. Liquid cooling based on single- or two-phase heat exchangers may provide unnecessary overcooling of a large area and entail packaging and cost issues [3,73,86,87]. Thermoelectric cooling (TEC) has attracted attention by offering solid-state operation and system scalability but the material compatibility with microelectronic processes and the limited cooling performance have been the bottlenecks [24,51,54,55,57,88]. A lateral TEC design based on a widely used semiconductor, silicon, has been developed for hot spot management. However, the high thermal conductivity of silicon has worked against the TEC performance [29]. On the other hand, nanostructured silicon with vertically etched holes, or holey silicon, shows effective hot spot cooling performance by offering low in-plane thermal conducitivty for Peltier effects and high cross-plane thermal conductivity for heat dissipation [37,41,43,89]. While the in-plane thermal resistance maintains enough temperature gradients for TEC, the cross-plane thermal resistance generates temperature gradients between the hot spot and the Peltier cooler, which can be detrimental to the cooling performance for large hot spot heat fluxes. In this chapter, we present a new TEC design by extending the Peltier cooler into the substrate or incorporating a through-silicon-via (TSV) [90] to increase the area of thermoelectric cooling and reduce the thermal resistance between the hot spot and the Peltier cooler. We also investigate the cooling prospects of filling metals into the holes of holey silicon, or metal-filled holey silicon; the high cross-plane thermal conductivity of holey silicon is increased due to high-thermal-conductivity metal inclusions, and the low in-plane thermal conductivity of

holey silicon is maintained due to the presence of metal-silicon interfaces and the corresponding thermal boundary resistance. The thermal boundary resistance can be characterized by the Debye temperature ratio [91–93], and among various metals, Au is an ideal filler for holey silicon due to a high Debye temperature ratio of 3.9 and additional electron-phonon coupling effects [94]. The theoretical predictions of Au-silicon thermal boundary resistance can be obtained by combining the diffuse mismatch model (DMM) [94–96] for interfacial phonon scatterings and two-temperature model (TTM) [94,97,98] for electron-phonon coupling effects. The thermal properties of Au-filled holey silicon are then calculated using the effective medium theories with a wide range of thermal boundary resistances [96,99]. In this chapter, we use theoretical models to predict the properties of holey silicon and Au-filled holey silicon and evaluate the cooling performance of TSV-integrated TEC, in comparison to no-TSV TEC and passive cooling method, with varying system dimensions and substrate materials.

3.2 Analytical Models for Cross-plane and In-plane Thermal Transport in Au-filled Holey Silicon

The thermal conductivity of Au-filled holey silicon is calculated using effective medium theories [96,99]:

$$k_{AFHS_z} = k_{HS_z}(1-\varphi) + k_{Au}\varphi \tag{3.1}$$

$$k_{AFHS_x} = k_{HS_x}\frac{\left(\frac{k_{Au}}{k_{HS_x}}-\frac{k_{Au}}{R_C^{-1}a}-1\right)\varphi+\left(1+\frac{k_{Au}}{R_C^{-1}a}+\frac{k_{Au}}{k_{HS_x}}\right)}{\left(1+\frac{k_{Au}}{R_C^{-1}a}-\frac{k_{Au}}{k_{HS_x}}\right)\varphi+\left(1+\frac{k_{Au}}{R_C^{-1}a}+\frac{k_{Au}}{k_{HS_x}}\right)} \tag{3.2}$$

where k_{AFHS_z} and k_{AFHS_x} are the cross-plane and in-plane thermal conductivities of Au-filled holey silicon. k_{Au}, a and φ are the thermal conductivity, radius and volume fraction of Au inclusions. R_c is the thermal boundary resistance at Au-silicon interface.

The thermal conductivity of Au inclusions (k_{Au}) can be equivalent to Au nanowires due to the identical shape. Theoretical predictions of Au nanowires are required due to the lack of experimental data. The thermal conductivity contribution from electrons can be derived based on the Wiedemann-Franz law because of the well-studied size effects on the electrical resistivity [100]. The total electrical resistivity of an Au nanowire is represented by combining the modified Fuchs-Sondheimer (FS) model [101] for surface boundary scattering and the Mayadas-Shatzkes (MS) model [102] for grain-boundary scattering [103]:

$$\rho_{total} = \rho_{FS} + \rho_{MS} - \rho_0 = \left(1 + \frac{3}{4}(1-s)\frac{\lambda_e}{d}\right)\rho_0 + \left(1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3\, ln\left(1 + \frac{1}{\alpha}\right)\right)^{-1}\rho_0 - \rho_0 \quad (3.3)$$

where ρ_{FS} and ρ_{MS} are the electrical resistivity of Au with electron scattering by surface and grain-boundaries. ρ_0 is the electrical resistivity of bulk Au. λ_e is the Au electron MFP, which is 41.7 nm at room temperature [104] and d is the diameter of the Au nanowire. s is the surface specularity, which is assumed to be 0 for fully diffuse surface conditions. α is expressed as $\frac{\lambda_e}{d_g}(\frac{R}{1-R})$, where d_g is the grain size, which is assumed to be the radius of Au nanowire. *R* is the electron wave-function reflection coefficient, which is assumed to be 0.5. The choice of fitting parameters is consistent with the values reported in the literature [100]. The electron contribution to the thermal conductivity is then calculated based on Wiedemann-Franz law [100]:

$$k_{Au_e} = \frac{\rho_0}{\rho_{total}} k_e \quad (3.4)$$

where k_e is the electron thermal conductivity of bulk Au, which is 313 $Wm^{-1}K^{-1}$ at room temperature [104,105]. For phonon thermal conductivity ($k_{Au_{ph}}$), we assume there is no grain-boundary scattering on long-wavelength phonons and only consider the surface scattering:

$$k_{Au_{ph}} = k_{ph}\left(1 + \frac{\lambda_{ph}}{d}\right)^{-1} \tag{3.5}$$

where k_{ph} and λ_{ph} are the phonon thermal conductivity and MFP of bulk Au. For simplicity, we use constant values of 5 $W \cdot m^{-1}K^{-1}$ and 10 nm for k_{ph} and λ_{ph}, respectively [100,106].

The thermal boundary resistance exists at the Au-silicon interface due to the scattering of incident phonons and the energy exchange between phonons and electrons. The DMM considers phonon transmission across the interfaces as [96]:

$$R_{DMM} = \left(\frac{1}{4}\sum_{j=1}^{3}\int_0^{\omega_{1,j}} v_{1,j}(\omega)\alpha_1(\omega)\hbar\omega DOS_1(\omega)\frac{\partial f_o}{\partial T}d\omega\right)^{-1} \tag{3.6}$$

where R_{DMM} is the thermal boundary resistance from the interfacial phonon scattering. v_j is the group velocity of mode j, $\hbar$ is the Planck's constant, and f_o is the Bose-Einstein distribution function. DOS is the density of states, which is calculated by the linear Debye approximation for phonon dispersion relation. The DMM assumes phonon scattering to be fully diffuse at the interface and hence the transmission coefficient is no longer dependent on the angle of incidence:

$$\alpha_1(\omega) = \frac{\sum_j v_{2,j}^{-2}}{\sum_j v_{2,j}^{-2} + \sum_j v_{1,j}^{-2}} \tag{3.7}$$

The thermal boundary resistance from electron-phonon coupling effects is evaluated by the commonly referenced TTM [98]. The thermal conductance associated with the electron phonon energy exchange can be estimated as $h_{ep} = \sqrt{Gk_{Au_{ph}}}$, where G is the electron-phonon coupling

constant [97]. Different *G* values have been reported for Au and we use a *G* of 2.2 ×10^{16} $Wm^{-3}K^{-1}$ in our simulations [107–110].

The total thermal boundary resistance considers the interfacial phonon-phonon thermal resistance and electron-phonon thermal resistance in a series connection [97]:

$$R_c = h^{-1} = \left(\frac{k_{Au_{ph}} \sqrt{\frac{G}{k_{Au_{hm}}}}}{1+\frac{k_{Au_{ph}}}{h_{DMM}} \sqrt{\frac{G}{k_{Au_{hm}}}} - \frac{k_{Au_{hm}}}{k_{Au_e}}} \right)^{-1} \tag{3.8}$$

where the $k_{Au_{hm}} = (\frac{1}{k_{Au_{ph}}} + \frac{1}{k_{Au_e}})^{-1}$, is the harmonic mean of the phonon and electron thermal conductivities of Au inclusions and *h* is the thermal boundary conductance.

3.3 Finite-element Simulations of TEC Systems

The device-level electro-thermal simulations are conducted using COMSOL Multiphysics and the material properties are from theoretical models in the last session. Figure 3.1 shows the schematic of TEC designs. For no-TSV TEC, a thin metal contact is integrated into the substrate and is on top of the hot spot to serve as the Peltier cooler. For TSV-integrated TEC, a metal TSV is extended from the Peltier cooler to the substrate and is directly in contact with the hot spot. Current is applied on the surface of the Peltier cooler and leaves at the ground electrode. The voltage difference from the center to the periphery of the substrate drives Peltier cooling and heating. Heat generated by electronics are simulated as 100 $W \cdot cm^{-2}$ background heat and a 1 $kW \cdot cm^{-2}$ hot spot, which are chosen as potential values for future electronics [16]. TEC designs are assumed to be positioned in between the heat source and a conventional heat sink. The top

surface of the substrate undergoes convection heat transfer to 25 °C ambient temperature. We apply a convection coefficient of 10 $kWm^{-2}K^{-1}$ in the simulation to represent the use of an advanced heat exchanger [16,29,74,89]. For lower convection coefficients, we may expect a greater impact of TEC due to the increased temperature gradients within the substrate [89]. The hot spot size is fixed at 50×50 μm^2. The substrate thickness is fixed at 100 μm as die-level thickness [29,74]. We have varied the Peltier cooler size from 5×5 to 500×500 μm^2 and changed the substrate size from 1×1 to 10×10 mm^2 to evaluate the impacts of system dimensions.

The Coefficient of Performance (COP) is defined as the net heat absorbed at the Peltier cooling junction (Q_c) divided by the applied electric power (Q_p) and has been widely applied to evaluate the performance of TEC with vertical p-n junctions [111]. For TSV-integrated TEC with holey silicon substrate, the COP is estimated as 0.4 when the applied current is 1 A, and the temperatures are 68 °C (T_c) and 127 °C (T_h) at the Peltier cooling and heating junctions ($COP = Q_c/Q_p = \frac{SI_{opt}T_c - Ak_{HS_x}\Delta T/L - 0.5I_{opt}^2R}{I_{opt}^2R + SI_{opt}\Delta T} = \frac{T_c}{T_h - T_c}\frac{\left(\sqrt{1+ZT_m} - T_h/T_c\right)}{\left(\sqrt{1+ZT_m}+1\right)}$, where S is the Seebeck coefficient of holey silicon. ΔT is the temperature gradient between Peltier cooling and heating junctions. R and I_{opt} are the electrical resistance and the optimal applied current of the TEC. A and L are the cross-sectional area and length of the TEC. $T_m = \frac{1}{2}(T_h + T_c)$, $Z = \frac{\sigma S^2}{k}$ and σ is the intrinsic electrical conductivity of holey silicon) [111]. However, this COP is developed for TEC designs that are vertically configured with one-dimensional heat transfer and is not suitable for lateral TEC designs because of the thermal and electrical spreading effects [112]. In this chapter, we have used the hot spot temperature and temperature cooling effectiveness (TCE) to evaluate the cooling performance as suggested by the previous studies [29,74,89]. The TCE is defined as:

$$\Delta T^* = \frac{T_{heating\ ON, cooling\ OFF} - T_{heating\ ON, cooling\ ON}}{T_{heating\ ON, cooling\ OFF} - T_{heating\ OFF, cooling\ OFF}} = \frac{\Delta T_{thermoelectric\ cooling}}{\Delta T_{hot\ spot\ cooling}} \tag{3.9}$$

The $T_{heating\ ON/OFF,cooling\ ON/OFF}$ is the hot spot temperature when the hot spot heat flux is applied/not applied, and the Peltier cooler is on/off. If $\Delta T^* \geq 1$, the TEC can cool down the hot spot to a temperature that is smaller than the scenario with only background heat. If $0 < \Delta T^* < 1$, the TEC can cool the hot spot, but its temperature is larger than the scenario with only background heat. If $\Delta T^* \leq 0$, the Joule heating generated by the TEC exceeds the Peltier cooling, and there is no cooling on the hot spot.

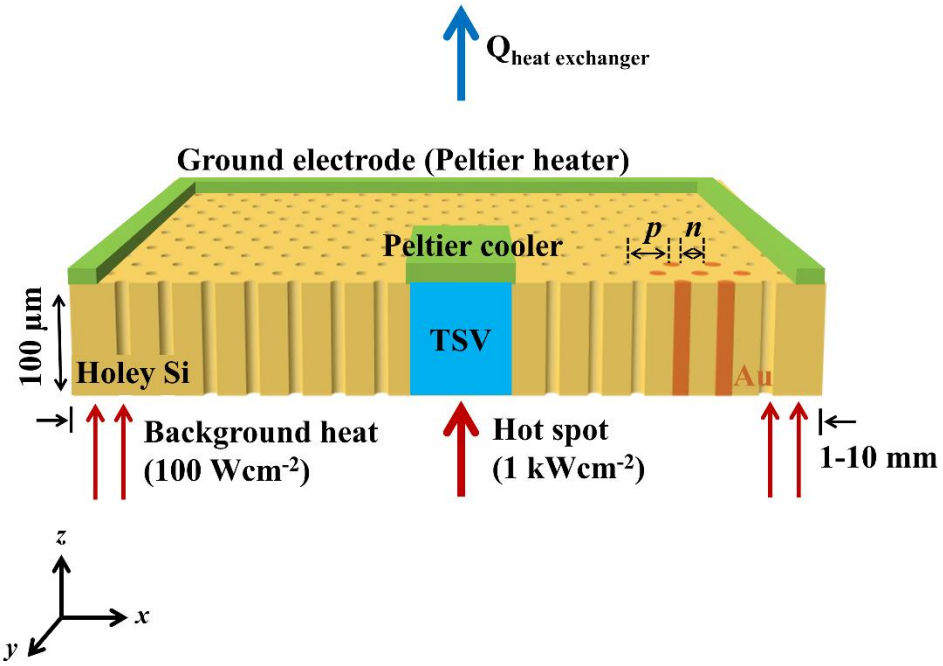

Figure 3.1 The schematic of lateral TEC designs. The no-TSV TEC only has a Peltier cooler (green block) on top of the hot spot and the TSV-integrated TEC attributes a metal TSV (blue block) that is extended from the Peltier cooler and is in contact with the hot spot. Holey silicon is the substrate with a neck size of 20 nm and a pitch size of 60 nm. When Au-filled holey silicon is used as the substrate, all the holes of holey silicon are filled with Au. The red arrows represent the heat fluxes from electronics to TEC designs, which are simulated as 100 Wcm^{-2} background heat and a 1 $kWcm^{-2}$ hot spot. The blue arrow represents the convection heat transfer from the TEC to a heat exchanger, which is simulated with a 10 $kW \cdot m^{-2}K^{-1}$ convection coefficient and 25 °C ambient temperature.

3.4 Results and Discussion

3.4.1 Thermal and electrical properties of holey silicon and Au-filled holey silicon

Figure 3.2(a) shows the cross-plane thermal conductivity predictions of 20 nm neck-holey silicon with the thickness ranging from 10 nm to 100 μm. The spectral scaling model matches with the reported holey silicon and silicon nanowires data [34,41,60]. The thermal conductivity increases with thickness, which is attributed to the presence of long-wavelength phonons that are persistent with lateral boundaries. Figure 3.2(b) shows the in-plane thermal conductivity predictions of 100 μm-thick holey silicon with neck size ranging from 10 nm to 100 μm. When the neck size is smaller than 100 nm, there is a good agreement between the experimental data of 100 nm-thick holey silicon and theoretical predictions of 100 μm-thick holey silicon. The thickness dependence becomes weak because the phonon boundary scattering with the neck dominates the in-plane heat transport [89]. For 100 μm-thick holey silicon, higher thermal conductivity anisotropies can be achieved with smaller neck sizes. In this chapter, we use a neck size of 20 nm to maintain sufficient electrical properties for TEC applications [37,89].

The electron and phonon thermal conductivities of Au inclusions with 40 nm diameter are 70 $W \cdot m^{-1}K^{-1}$ and 4 $W \cdot m^{-1}K^{-1}$ based on Eq. (3.8) and (3.9). The values are consistent with the Boltzmann transport equation (BTE) predictions of Au nanowires with similar dimensions [100]. The room temperature thermal boundary resistance between Au inclusions and 20 nm neck-holey silicon is 14 $m^2K(GW)^{-1}$ based on DMM and increases to 17 $m^2K(GW)^{-1}$ after combining the electron-phonon coupling effect. Figure 3.2(a) shows the prediction of the cross-plane thermal conductivity of Au-filled holey silicon. The thermal boundary resistance has no influence on the cross-plane thermal transport, resulting in a 130 % increase in the thermal conductivity. Figure

3.2(b) shows the in-plane thermal conductivity predictions of Au-filled holey silicon. When the neck size is 20 nm and thermal boundary resistance is 17 $m^2K(GW)^{-1}$, the thermal conductivity of Au-filled holey silicon is 2 $W \cdot m^{-1}K^{-1}$, which is smaller than the intrinsic thermal conductivity of holey silicon but larger than its effective value. The thermal boundary resistance is intrinsically determined by the mismatch in acoustic properties and the energy transfer between dissimilar energy carriers. The experimentally reported thermal interface resistances are often greater than the theoretical predictions, especially for vertical surfaces, primarily due to surface roughness, imperfect interfaces, etc. [113]. We find that when the thermal boundary resistance is 15 times greater than the theoretical prediction, the in-plane thermal conductivity of Au-filled holey silicon will close to the effective value of holey silicon. The corresponding thermal boundary resistance is considered as the higher limit (high R_c) and the theoretical prediction is considered as the lower limit (low R_c) in finite-element simulations.

The room-temperature thermal properties of holey silicon and Au-filled holey silicon are applied because the thermal conductivity variations within the simulated temperature range are expected to be small due to the dominated temperature-independent boundary scattering [37,41,43]. The temperature-dependent Umklapp process results in decreasing thermal conductivity trend at high temperatures, which is even favourable to TEC [61].

In the finite-element simulations, we have used the reported electrical properties of p-type silicon with a doping concentration of 2.5×10^{19} cm^{-3}, which provides an electrical conductivity of 2.8×10^{4} $S \cdot m^{-1}$ and a Seebeck coefficient of 440 μVK^{-1} in the range of operating temperature (50-150 °C) [83,84,112]. They have been applied for holey silicon with the consideration of porosity. The electrical effects of Au inclusions are not included in the finite-element simulations because of their negligible impacts. The electrical conductivity of Au-filled

holey silicon can be obtained using Eq. (3.6) by changing the thermal conductivity (k) to electrical conductivity (σ) and thermal boundary resistance (R_c) to electrical contact resistance (ρ_c) [99]. The typical electrical contact resistance at metal-highly doped silicon interface is known as 1×10^{-6} $\Omega\cdot cm^2$ [112] and the corresponding difference in the electrical conductivity of holey silicon and Au-filled holey silicon is less than 2%, which results in an even smaller difference in the hot spot temperature in TEC simulations. The impact of Au inclusions on the Peltier coefficient of holey silicon is negligible because the Peltier effects happening at the electrode-holey silicon interface dominate the cooling performance. On the other hand, with the typical electrical contact resistance (1×10^{-6} Ωcm^2), only limited current can flow across the boundary into Au inclusions, and the corresponding Peltier effect is negligible [99].

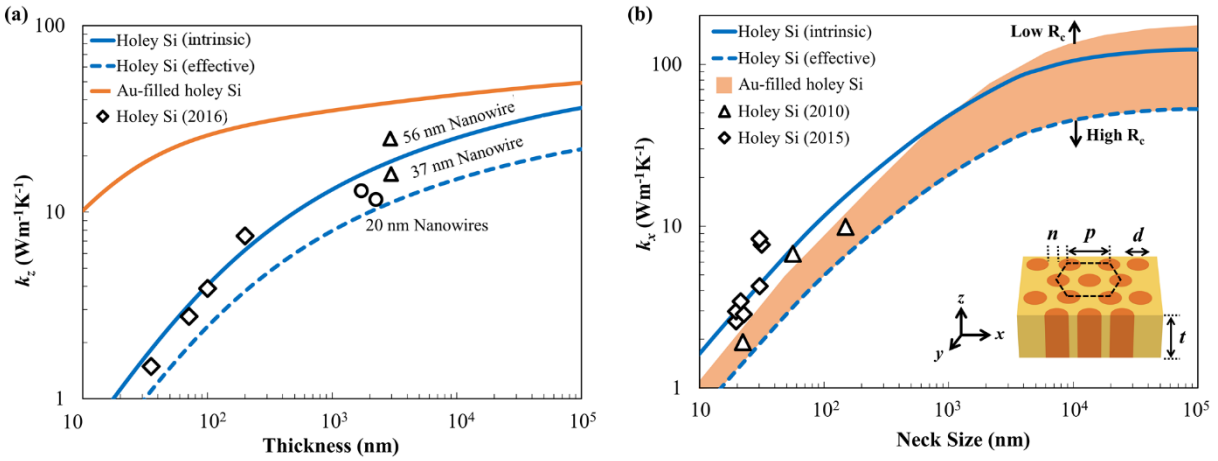

Figure 3.2 The theoretical models for in-plane and cross-plane thermal conductivities of holey silicon and Au-filled holey silicon. The blue solid line represents the intrinsic thermal conductivity of holey silicon. The red and blue dash lines represent the thermal conductivity of Au-filled holey silicon and the effective thermal conductivity of holey silicon, which are the values used in the finite-element simulations. (a) k_z predictions of holey silicon and Au-filled holey silicon with 20 nm neck size and 10 nm-100 μm thicknesses. The 56 nm and 37 nm silicon nanowire data is from [34] and the 20 nm nanowire data is from [60]. (b) k_x predictions of holey silicon and Au-filled holey silicon with neck size ranging in 10 nm-100 μm and thickness of 100 μm. The orange area represents the possible k_x of Au-filled holey silicon with thermal boundary resistance changing

from low R_c (17 $m^2K\cdot(GW)^{-1}$) to high R_c (255 $m^2K\cdot(GW)^{-1}$). Inset is the structure of Au-filled holey silicon, and *n*, *p*, *t* and *d* represent the neck size, pitch size, Au inclusion diameter and the thickness, respectively. The 2010 holey silicon data is from [37], and the 2015 holey silicon data is from [43].

3.4.2 Effects of TSV on the TEC designs for on-state and off-state conditions

An effective TEC requires a balance between Peltier cooling and Joule heating. It has been well established that for each system dimension, there is an optimal applied current that produces the most effective cooling. We have performed simulations with various applied currents and presented the minimum hot spot temperature for each dimension. Figure 3.3 (a) shows the minimum hot spot temperature with a Peltier cooler/ hot spot size ratio changing from 0.1 to 10. The variation of hot spot temperature is caused by the trade-offs between Peltier cooling, Joule heating and thermal spreading. These competing effects yield the minimum hot spot temperature when the Peltier cooler/ hot spot size ratio is 6 for no-TSV TEC and 2 for TSV-integrated TEC.

Figure 3.3(b) and (c) show the temperature profiles of no-TSV TEC and TSV-integrated TEC with holey silicon and Au-filled holey silicon (with low R_c) substrates. The Peltier cooler/ hot spot size ratio is fixed at 2 for both designs for comparison. The no-TSV TEC favors Au-filled holey silicon due to its high thermal conductivity anisotropy. The Peltier cooling happens at the interface between the metal contact and the substrate. Holey silicon attributes higher in-plane thermal resistance, which maintains a greater temperature gradient for Peltier effects and the Peltier cooler temperature is 6 °C lower than that of Au-filled holey silicon. However, the low cross-plane thermal conductivity of holey silicon generates a large temperature gradient between the hot spot and the Peltier cooler, resulting in a higher hot spot temperature than that of Au-filled holey silicon. For TSV-integrated TEC, the Peltier cooling happens at the TSV-substrate interface

and the Peltier cooling flux is directly applied to the hot spot through high-thermal-conductivity TSV. The TEC performance is determined by the in-plane thermal resistance of the substrate. Holey silicon substrate maintains a 60 °C temperature gradient in the in-plane direction with 1 A optimal applied current (the corresponding power consumption is 0.5 W) and the hot spot temperature is 15 °C lower than that of Au-filled holey silicon substrate.

Conventional thermoelectric materials with low thermal conductivity [55,57] may provide effective hot spot cooling with TSV-integrated TEC, but their high thermal resistance limits the heat dissipation for the rest of the electronics. On the other hand, Au-filled holey silicon with high thermal conductivity anisotropy provides comparable hot spot cooling performance while offering low cross-plane thermal resistance for heat dissipation. Figure 3.3(a) shows that the hot spot temperature of Au-filled holey silicon will be close to that of holey silicon depending on the thermal boundary resistance. Figure 3.3(a) also shows that the TSV-integrated TEC outperforms a Cu block when the Peltier cooler/ hot spot size ratio is greater than 0.2. The corresponding Peltier cooler size is 10×10 μm^2, which is within the typical feature sizes of TSVs in modern electronics (the feature size ranges in 1-50 μm and thickness up to 150 μm) [114]. The potential cost of Au inclusions can be accommodated by using Au only at the interface for high boundary resistance and use Cu in the rest.

For off-state conditions, the hot spot temperature is determined by the passive heat conduction. The off-state temperature profiles are shown in Figure 3.3(b) and (c) for both TEC designs. By inserting a TSV that directly draws heat from the hot spot, the hot spot temperatures of TSV-integrated TEC are 24 °C and 12 °C lower than those of no-TSV TEC with holey silicon and Au-filled holey silicon substrates, respectively. By filling metals in the holey silicon, Au-filled

holey silicon has lower thermal resistance, and the hot spot temperatures are 19 °C and 7 °C lower than those of holey silicon substrates with no-TSV TEC and TSV-integrated TEC, respectively.

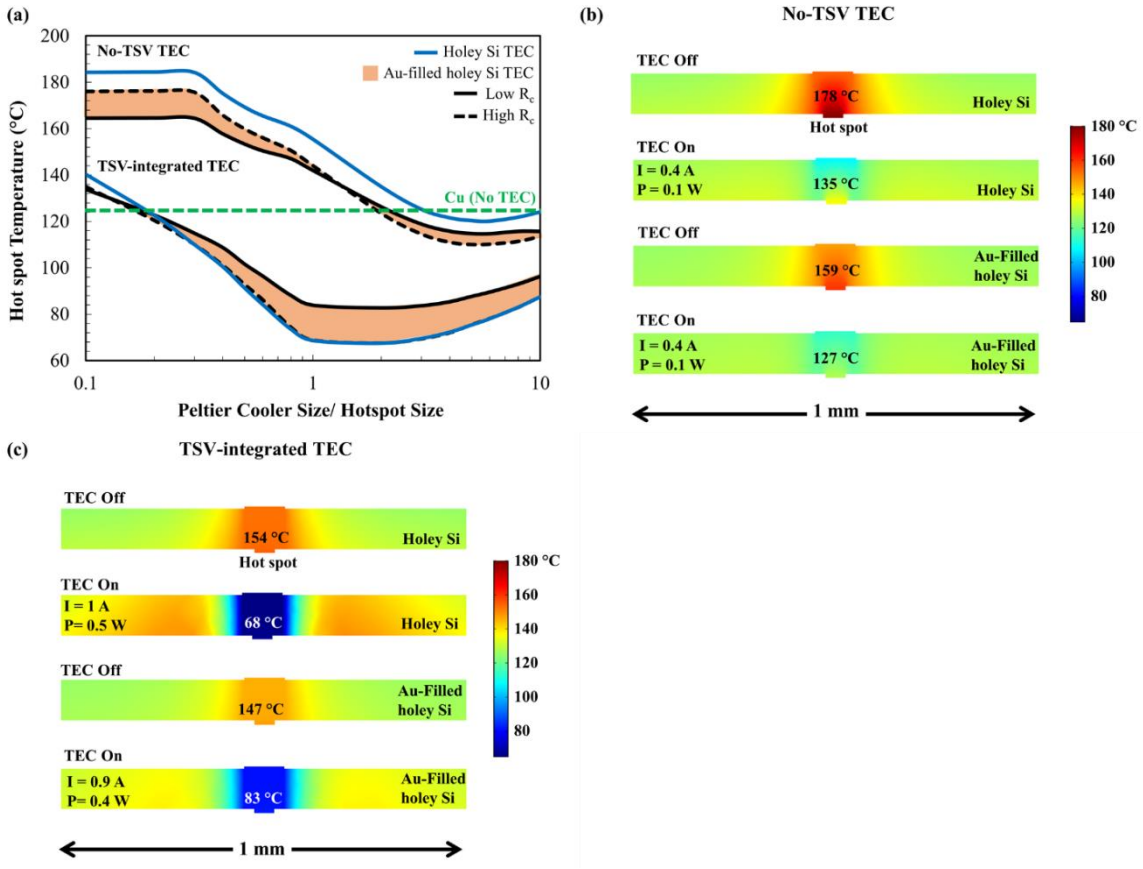

Figure 3.3 (a) The hot spot temperatures of TEC designs with holey silicon or Au-filled holey silicon substrates. The Peltier cooler/ hot spot size ratio varies from 0.1 to 10 for both designs. The hot spot temperature with a 10×10 mm^2 Cu block is shown by the green dash line for comparison. The black solid and dash lines are hot spot temperatures of the Au-filled holey silicon substrate with a low R_c (17 $m^2K\cdot(GW)^{-1}$) and a high R_c (255 $m^2K\cdot(GW)^{-1}$). The area between them represents the possible hot spot temperatures that can be achieved for the Au-filled holey silicon substrate. (b) Cross-sectional temperature profiles of no-TSV TEC with holey silicon and Au-filled holey silicon (low R_c) substrates. The Peltier cooler/ hotspot size ratio is 2. The optimal applied currents and power consumptions are also provided for both substrates. (c) Cross-sectional temperature profiles of TSV-integrated TEC with holey silicon and Au-filled holey silicon (low R_c) substrates. The Peltier cooler/ hotspot size ratio is 2. The optimal applied currents and power consumptions are also provided for both substrates.

3.4.3 Effects of the substrate on the TSV-inserted TEC designs for on-state and off-state conditions

The impacts of the substrate can be evaluated by changing its thermal conductivity and dimensions. We first fix the substrate size and Peltier cooler size at 10×10 mm^2 and 100×100 μm^2 (the Peltier cooler/hot spot size ratio is 2) and keep the substrate cross-plane thermal conductivity the same as 20 nm neck-holey silicon. The in-plane thermal conductivity of the substrate is changed from 1 to 100 $Wm^{-1}K^{-1}$ because it governs the performance of TSV-integrated TEC. Figure 3.4(a) shows the hot spot temperatures of TSV-integrated TEC. For on-state conditions, the hot spot temperature increases with increasing in-plane thermal conductivity due to the reduced temperature gradients for Peltier effects. For off-state conditions, the hot spot temperature decreases with increasing in-plane thermal conductivity due to the reduced thermal resistance. The in-plane thermal conductivities of Au-filled holey silicon with low and high R_c are also shown in Figure 3-4(a). Au-filled holey silicon offers a new way to vary the substrate in-plane thermal conductivity while reducing the cross-plane thermal resistance, which can satisfy the requirements of on-state and off-state hot spot temperatures for different electronics.

We then use TCE to evaluate impacts of substrate size with different substrate materials to address the system scalability. The substrate size is changed from 10×10 to 1×1 mm^2 and the Peltier cooler size is fixed at 100×100 μm^2 (the Peltier cooler/hot spot size ratio is 2). Figure 3.4(b) shows the TCEs of different substrates with different lateral sizes. Due to the low in-plane thermal conductivity of holey silicon and high thermal boundary resistance of Au-silicon interface, holey silicon and Au-filled holey silicon-based TSV-integrated TECs remain effective even at a confined space and offer scalable cooling performance that is unachievable for bulk silicon. The scalabilities

of TSV-integrated TECs with holey silicon or Au-filled holey silicon are consistent with no-TSV TEC, which are attractive for portable devices or laterally confined systems.

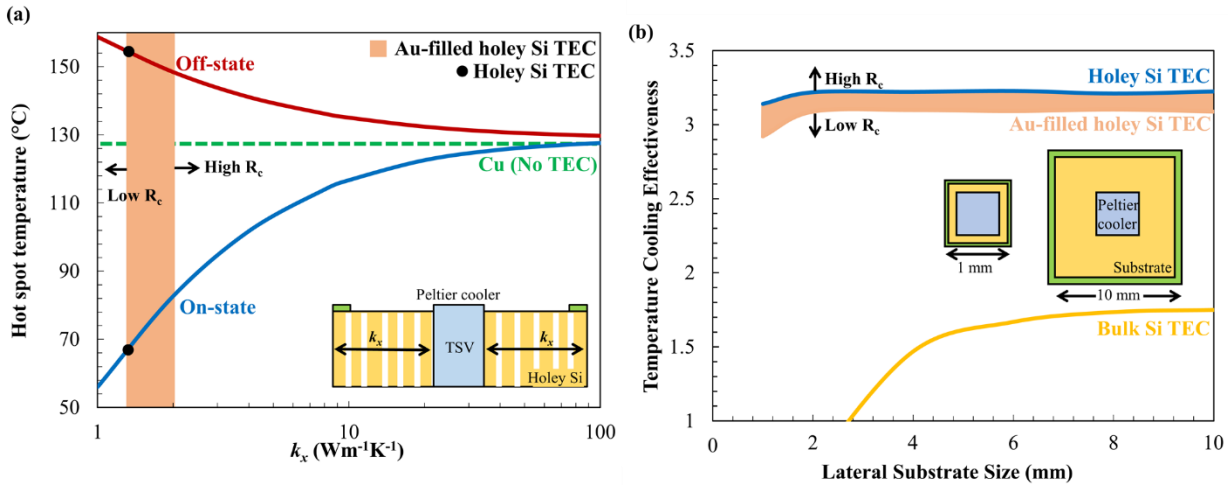

Figure 3.4 (a) The on-state and off-state hot spot temperatures of TSV-integrated TEC with different substrate in-plane thermal conductivities. Holey silicon is represented as black dots and Au-filled holey silicon is represented as an orange area with R_c of 17 $m^2K\cdot(GW)^{-1}$ and 255 $m^2K\cdot(GW)^{-1}$ as boundaries. The lateral substrate size is fixed at 10×10 mm^2. (b) The TCEs of TSV-integrated TEC with holey silicon, Au-filled holey silicon, and bulk silicon substrates. The lateral substrate size is changed from 10×10 to 1×1 mm^2.

3.5 Conclusions

This chapter demonstrates a TSV-integrated TEC that provides exceptional hot spot cooling performance by combining the passive cooling from a metal TSV and the active cooling from holey silicon. The TSV-integrated TEC not only presents negligible temperature gradients between Peltier cooler and hot spot but also fully takes advantage of the thermal conductivity anisotropy of holey silicon. We further investigate the prospects of utilizing metal-filled holey silicon, which attributes even higher thermal conductivity anisotropy. Its high cross-plane thermal conductivity due to metal inclusions is favorable to heat dissipation and its low in-plane thermal

conductivity due to metal-silicon boundary resistance is favorable to thermoelectric cooling. The TSV-integrated TEC along with holey silicon or Au-filled holey silicon substrates offer transformative solutions to hot spot management and will become even more attractive for space constrained electronic devices.

Chapter 4: Transient Cooling and Heating Effects in Holey Silicon-based Lateral Thermoelectric Devices for Hot Spot Thermal Management

Lateral thermoelectric devices, where the Peltier cooling and heating occur in a lateral direction, have shown promise for thermal management of on-chip hot spots, and because of the device orientation, thermoelectric materials with anisotropic properties such as holey silicon have shown even more promising cooling potential. However, the role of anisotropy in transient cooling and heating effects is little known, and thermal management optimization using a pulse has not been considered with anisotropic materials. Here we study temporal and spatial interplays of Peltier, Joule, and Thomson effects in a holey silicon-based lateral thermoelectric device with varying pulse conditions and material properties. Our simulations show a supercooling effect, driven by Peltier cooling before Joule heating diffuses in, and that holey silicon with anisotropic thermal conductivities is favorable by delaying the diffusion in the lateral direction while allowing rapid heat dissipation in the vertical direction. Depending on the local temperature distribution, the Thomson effect is shown to strengthen the supercooling effect. A holey silicon-based thermoelectric device with a 1 $kW \cdot cm^{-2}$ hot spot shows temperature reductions from 117 to 102 °C in steady-state and temporarily to 100 °C with optimal pulse conditions. The transient cooling performance can be further improved by incorporating phase change materials within holey silicon, in which their melting process delays a temperature overshoot. The anisotropy, specific heat, and latent heat play important roles in determining the transient cooling performance. Our findings show that lateral thermoelectric devices with anisotropic properties are promising for dynamic thermal management of on-chip hot spots.

4.1 Introduction

On-chip hot spots with high power, high density, and heterogeneous packaging have posed increasing challenges for thermal management [22,49]. Dr. Avram Bar-Cohen and his group had made significant contributions in the areas of electronics packaging and thermal management over the years, and among them was hot-spot thermal management using thermoelectric coolers (TECs) [3,13,116–121,14–17,29,74,112,115]. In 2007, Bar-Cohen *et al*, first demonstrated a concept of lateral TECs for on-chip hot spot cooling where metal contact and ground electrodes are placed on a silicon substrate and the Peltier cooling and heating occur in the lateral direction across the substrate [112]. Later, the Bar-Cohen group explored other substrate materials such as germanium [3,74,117–119]. The Peltier cooling junction is positioned right on top of a hot spot to dissipate the heat in the vertical direction and the Peltier heating junction is positioned away from the hot spot. The past studies have shown that lateral TECs may provide a greater cooling flux than that of vertical TECs and are promising for thermal management of on-chip hot spots.

Because of the device orientation and directions of heat transfer in the lateral TEC, a combination of low thermal conductivity in the in-plane direction and high thermal conductivity in the cross-plane direction is desirable [89]. To address the unique need for thermal conductivity anisotropy, holey silicon [37,41,43] has been considered as a promised material for lateral TECs. In holey silicon, the low in-plane thermal conductivity due to phonon boundary scattering in small necks is expected to sustain a large temperature gradient between Peltier cooling and heating junctions for lateral TECs, and the high cross-plane thermal conductivity is expected to dissipate the heat effectively from a hot spot to a bulk heat sink. The TEC performance was studied to be further improved by incorporating a metallic through-silicon-via (TSV) within a holey silicon substrate where the Peltier cooler can directly draw heat from the hot spot [122].

While the role of anisotropy had been studied for steady-state, optimal thermal management strategies using a pulse or with a supercooling effect have not been considered with anisotropic materials. The transient behavior involves temporal and spatial interplays between the interfacial Peltier effect and the volumetric Joule heating and Thomson effects. By applying a current pulse with an amplitude larger than the steady-state optimal applied current, a supercooling effect can be achieved at the Peltier cooling junction before the diffusion of Joule heating takes it over. Snyder *et al.* [123] and Yang *et al.* [124] theoretically and experimentally studied the relationship between the transient cooling parameters, such as minimum temperature achieved, maximum temperature overshoot, and the time to reach the minimum temperature, etc., and the current pulse amplitude, thermoelectric element length, thermoelectric figure of merit, and thermal diffusivity. Manno *et al.* [120] explored the transient behavior of a lateral TEC on a Geranium hot spot and demonstrated a 30 % improvement in the hot spot temperature reduction. Lv *et al.* [125] investigated the transient supercooling performance of a TEC with various pulse shapes and found that the optimal shape was determined by the time to reach the minimum temperature and the pulse width. Selvam *et al.* [126] evaluated the transient performance of a TEC with phase-change-material (PCM) filled heat sink, a 3 °C temperature reduction can be further achieved with PCM under a square-shaped current pulse. However, the low thermal conductivity of PCM limits the TEC performance. Previous studies adopted constant material properties in the simulation of transient supercooling, in which the Thomson effect was ignored [120,126–130]. However, several researchers found that the Thomson effect should be considered for a more accurate TEC model for the steady-state simulations [131–133]. The Thomson effect yields heat evolution or absorption in a medium carrying an electrical current while sustaining a temperature gradient [134], which may support or impede device cooling depending on the temperature distribution. A detailed

discussion about the impact of the Thomson effect on the transient supercooling of a lateral TEC is still missing.

In this chapter, we study the temporal and spatial interplays of Peltier, Joule, and Thomson effects in holey silicon-based lateral TEC with varying pulse conditions and material properties. Our simulations show that the transient Thomson effect in the lateral TEC is supportive of supercooling due to the unique temperature distribution. The effects of current pulse shape, amplitude, and duration on the normalized minimum and maximum hot spot temperature changes, the normalized time to reach them, and holding times for supercooling and overheat regimes are evaluated. Moreover, the transient cooling performance of PCM-filled holey silicon is evaluated. The effects of PCM density, heat capacity, and latent heat are explored. Our findings show that the lateral TECs with anisotropic properties can be potentially applied for dynamic thermal control of on-chip hot spots.

4.2 Simulation of Holey Silicon-based Thermoelectric Cooler for On-chip Hot Spots

4.2.1 Numerical modeling of transient thermoelectric cooling

The device-level thermoelectric simulation is performed using COMSOL Multiphysics with the consideration of the Peltier effect, Joule heating, and Thomson effect. The following equations are solved for thermoelectric phenomena [135]

$$\rho c_p \frac{\partial T}{\partial t} + \nabla(-\mathrm{k}\nabla T + ST\boldsymbol{J}) = \boldsymbol{J} \cdot \boldsymbol{E} \tag{4.1}$$

$$\nabla(\sigma(\nabla \mathrm{V} - S\nabla \mathrm{T})) = 0 \tag{4.2}$$

where ρ is the density ($kg \cdot m^{-3}$), cp is the specific heat capacity ($J \cdot kg^{-1}K^{-1}$), k is the thermal conductivity ($W \cdot m^{-1}K^{-1}$), and S is the Seebeck coefficient ($V \cdot K^{-1}$). $\boldsymbol{J}$ is the current density ($A \cdot m^{-2}$), $\boldsymbol{E}$ is the electrical field ($V \cdot m^{-1}$), σ is the electrical conductivity ($S \cdot m^{-1}$), and V is the electrical potential (V).

Figure 4.1(a) shows the schematic of holey silicon-based lateral TEC with a TSV as the Peltier cooler. The heat generation by electronics is modeled as a combination of an 80 $W \cdot cm^{-2}$ background heat and a 1 $kW \cdot cm^{-2}$ hot spot, which are chosen as representative values for modern electronics [29,89]. The top of the holey silicon TEC undergoes convective heat transfer from 25 ^{o}C ambient air. A constant convection coefficient (h) of 10 $kW \cdot m^{-2}K^{-1}$ is used to represent the use of an advanced heat exchanger. Similar h values are used in previous studies for the thermal management of hot spots in the order of 1 $kW \cdot cm^{-2}$. For example, 5-20 $kW \cdot m^{-2}K^{-1}$ was used in [136] and 8.7 $kW \cdot m^{-2}K^{-1}$ was used in [29,120]. With moderate heat exchangers, we may expect a lower convection coefficient and a higher hot spot temperature. In this case, the impact of thermoelectric cooling will be greater [89] and lead to more temperature reduction in the supercooling regime. The temperature overshoot in the overheating regime will also be increased due to the limited heat dissipation of Joule heating. Current ($I(t)$) is applied to the central Peltier cooler and left the TEC at the ground electrode ($V = 0V$). The flow of positive holes transports the absorbed heat away from the Peltier cooler/holey silicon interface (Peltier cooling) and dissipates it at the secondary interface between the holey silicon and the ground electrode (Peltier heating). The material of metal contact is assumed to be aluminum and electric contact resistance of 1×10^{-6} Ωcm^2 is applied between the metal and holey silicon substrate [76,77]. The Peltier cooler (l_{cooler}) and holey silicon (l_{HS}) sizes are 200 μm and 10 mm, respectively. The thickness of holey silicon, $t_{HS,}$ is set to be 100 μm for better thermal spreading [89,122]. The hot spot dimension is 50×50×5

μm^3 ($x \times y \times z$) and its thermal conductivity is the same as silicon at 100 °C (100 $W \cdot m^{-1}K^{-1}$). The volume average temperature of the hot spot is used to evaluate the TEC performance. The hot spot has a constant heat flux to provide a general analysis of the transient supercooling. For electronics with dynamic hot spots, specific studies are required to provide the optimal cooling performance.

The transient simulation is performed with a time step of 0.1 ms. With the thermal boundary conditions and the optimal applied current ($I_{s\text{-}s}$), we define the thermal time constant of the system as the time required to change 63.2% of the hot spot temperature from the initial/ambient temperature (25 °C) to the minimum achievable hot spot temperature in steady-state ($T_{s\text{-}s}$) The thermal time constant is around 15 ms. 1/3 of the thermal time constant, τ = 5 ms, is used as an arbitrary constant throughout this chapter to normalize the time. Figure 4.1(b) shows an example of the time-dependent applied current and the normalized hot spot temperature change. The x-axis is the ratio between time and τ. $\Delta T_{tran} = T_{hot\ spot} - T_{s\text{-}s}$, where $T_{hot\ spot}$ is the transient hot spot temperature. $\Delta T_{tran}/\Delta T_{s\text{-}s}$ is the normalized transient hot spot temperature change, which represents the ratio between transient hot spot temperature change and the maximum hot spot temperature reduction in steady-state. For transient simulations, a constant current of $I_{s\text{-}s}$ is first applied until the hot spot temperature reaches $T_{s\text{-}s}$ and then a square-shaped current pulse with an amplitude of I_p and a duration of t_p is applied to the Peltier cooler. The hot spot temperature reduces instantly due to the enhanced Peltier cooling (supercooling) and then increases due to the diffusion of the Joule heating (overheating). After the current pulse ends, the hot spot temperature gradually returns to $T_{s\text{-}s}$. Six parameters are used to evaluate the transient supercooling performance of the lateral TEC as shown in Figure 4.1(b). $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ are the maximum normalized hot spot temperature change in supercooling and overhearing periods. $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ are the normalized

time to reach $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$. $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ are the normalized holding times for supercooling and overheating periods.

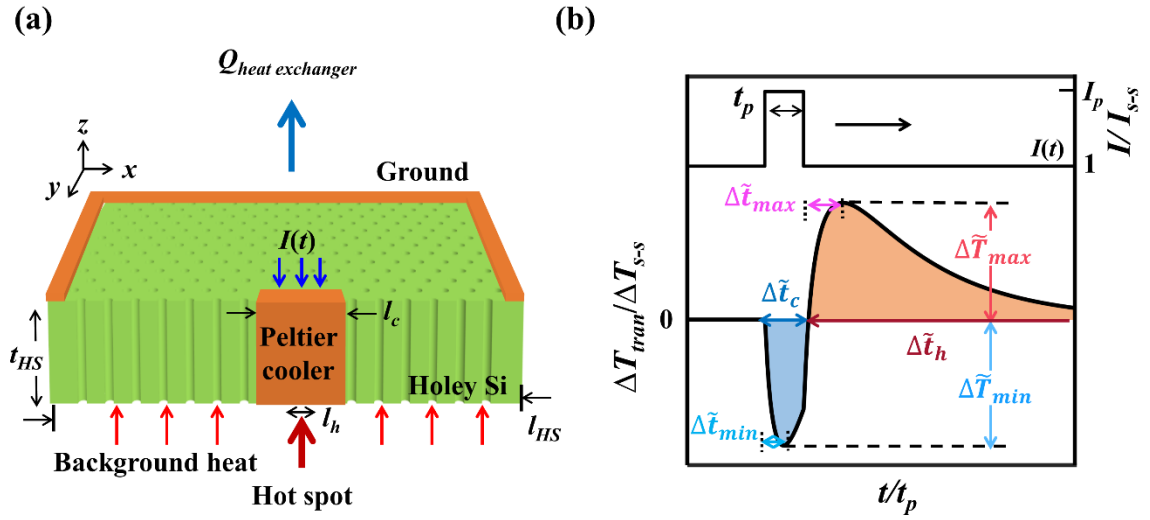

Figure 4.1 (a) The schematic of holey silicon-based TEC. Hot spot, Peltier cooler, and holey silicon sizes are 50 µm, 200 µm, and 10 mm, respectively. The chip thickness is 100 µm. For boundary conditions, the hot spot is in the center of the chip and has a heat flux of 1 kW·cm^{-2}. The background area is 10 mm × 10 mm and has a heat flux of 80 W·cm^{-2}. Convection is uniformly applied to the top surface of the TEC. Current (I(t)) is applied to the Peltier cooler and ground (V = 0V) is applied to the ground electrode. (b) A current pulse of I_p amplitude and t_p duration and the transient hot spot temperature change. τ = 5 ms is a constant to normalize the time. Blue and red regions indicate supercooling and overheating regimes. $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ are the maximum normalized temperature change in supercooling and overheating periods, respectively. $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ are the normalized time to reach $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$. $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ are the normalized holding times for supercooling and overheating regimes.

4.2.2 Thermoelectric properties of holey silicon

The thermal conductivity of holey silicon had been measured with various neck sizes and thicknesses [37,41,43,45,46,137]. Spectral scaling models were developed to predict the in-plane (k_x) and cross-plane (k_z) thermal conductivities of holey silicon with varying dimensions [41,89]. Few papers had measured the electrical properties of holey silicon at elevated temperatures and

the impact of nanoscale structures on the electrical conductivity and Seebeck coefficient of holey silicon are not fully understood [45,46]. In this chapter, we linearly fit the measured electrical properties of a highly doped p-type holey silicon with a 45 nm neck size [46]. k_x and k_y of holey silicon with a neck size of 45 nm and a porosity (φ) of 24 % are calculated based on spectral scaling models to be consistent with the sample used for electrical measurement. The effective medium theory is used to count the impact of porosity for thermal and electrical conductivities [44,138]. Figure 4.2(a) shows the predicted effective k_x and k_y of holey silicon at a temperature range of 300 - 700 K. k_y is much larger than k_x due to the different phonon transport mechanisms and the thermal anisotropy is around 10. Figure 4.2(b) shows the fitting lines of S and the effective σ with the same neck size and temperature range. Temperature-dependent thermal conductivity and electrical properties are used in the numerical simulations.

The density (ρ_{HS}) and specific heat capacity (cp_{HS}) of holey silicon are assumed to be constant values of 700 $J \cdot kg^{-1}K^{-1}$ and 1770 $kg \cdot m^{-3}$ ($\rho_{Si} \times (1-\varphi)$) in the simulation. For PCM integrated holey silicon, the effective density, ρ_{PCM-HS}, is defined as:

$$\rho_{PCM-HS} = \varphi \times \rho_{PCM} + (1-\varphi) \times \rho_{HS} \tag{4.3}$$

and the effective specific heat capacity, cp_{PCM-HS}, is calculated as:

$$cp_{PCM-HS} = cp_{HS} \times \frac{(1-\varphi)\times\rho_{HS}}{\rho_{PCM-HS}} + cp_{PCM} \times \frac{\varphi\times\rho_{PCM}}{\rho_{PCM-HS}} \tag{4.4}$$

For PCM-filled holey silicon, the effective latent heat (L_{eff}) is calculated as

$$L_{PCM-HS} = \frac{\varphi\times\rho_{PCM}}{\rho_{PCM-HS}} \times L_{PCM} \tag{4.5}$$

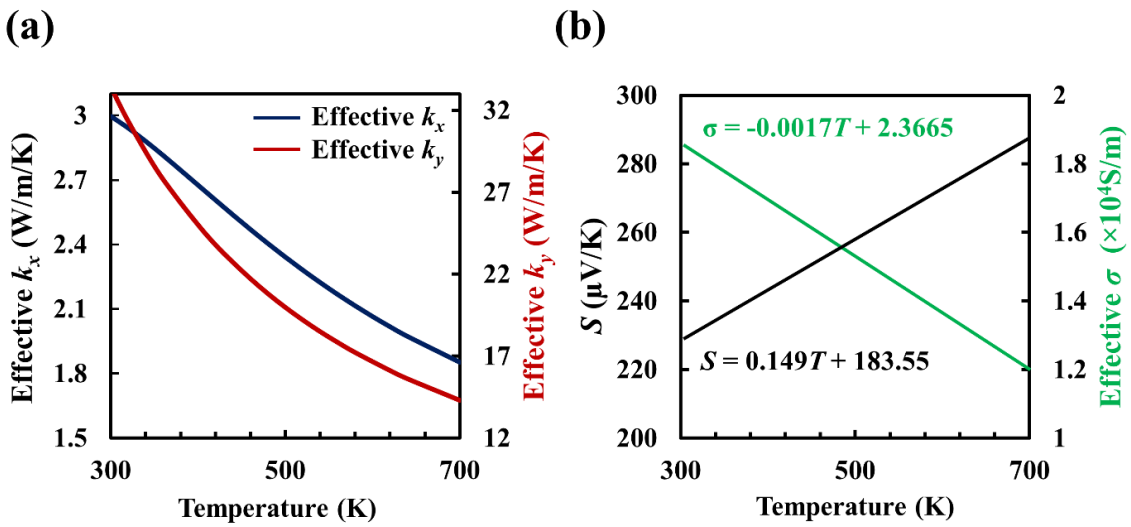

Figure 4.2 (a) Temperature-dependent effective k_x and k_y of holey silicon predicted from spectral scaling models and effective medium theory. k_z is larger than k_x with an anisotropy around 10. (b) Temperature dependent S and effective σ of holey silicon as linear fits from the experimental data. Equations used in the numerical simulations are also shown.

4.3 Results and Discussion

The transient behavior of holey silicon-based TEC is studied in COMSOL Multiphysics with temperature-dependent material properties. The steady-state simulation of holey silicon-based TEC is first performed to determine the minimum hot spot temperature ($T_{s\text{-}s}$) and the optimal applied current ($I_{s\text{-}s}$). With the optimal applied current ($I_{s\text{-}s}$ = 0.8 A), the hot spot temperature reduces from 117.2 °C ($T_{TEC\text{-}off}$) to 102.2 °C ($T_{s\text{-}s}$) and the maximum temperature reduction in steady-state is 15 °C ($\Delta T_{s-s} = T_{TEC-off} - T_{s-s}$). Transient supercooling can be achieved by applying a current pulse with a larger amplitude than $I_{s\text{-}s}$. Figure 4.3(a) shows the current change with a pulse of 1.5$I_{s\text{-}s}$ and 5 ms (t_p/τ = 1) duration and the normalized hot spot temperature change. By applying a current pulse, the hot spot temperature can be further reduced by 10% more than that of the steady-state temperature reduction. The hot spot temperature later increases due to the

diffusion of the Joule heating, and the overshoot is also around 10 %. Figure 4.3(b) shows cross-sectional temperature profiles of holey silicon-based TEC. The hot spot temperature is 117.2 °C ($T_{TEC\text{-}off}$) when TEC is off and is 102.2 °C ($T_{s\text{-}s}$) when TEC is on with $I_{s\text{-}s}$. With the square-shaped current pulse, the hot spot temperature first reduces to 100.7 °C and then increases to 103.7 °C before recovers to T_{s-s}.

The heat rate change of the Peltier cooling can be calculated by integrating over the contact area between the Peltier cooler and the holey silicon, which has a length of the Peltier cooler size (l_{cooler} = 200 μm) and a height of the holey silicon thickness (t_{HS} = 100 μm):

$$q_{Peltier} = \iint T\Delta S|\boldsymbol{J}|\, dA \tag{4.6}$$

and the Joule heating change can be calculated by integrating over the whole volume of the holey silicon substrate:

$$q_{Joule} = \iiint \frac{|J|^2}{\sigma}\, dV \tag{4.7}$$

The change of the Thomson effect can be also represented by integrating over the holey silicon volume:

$$q_{Thomson} = \iiint -\boldsymbol{J}T\frac{dS}{dT}\nabla T\, dV \tag{4.8}$$

where the Thomson coefficient, μ_T, is defined as $T(\mathrm{d}S/\mathrm{d}T)$. When TEC is operating with $I_{s\text{-}s}$ ($t/\tau < 0$), the Peltier cooling, Joule heating, and Thomson effect is calculated to be 0.092 W, 0.224 W, and -0.0047 W. When the step-shaped current pulse is applied ($0 \le t/\tau \le 1$), the Peltier cooling, Joule heating, and Thomson effect are changed to 0.108 W, 0.504 W, and -0.007 W, which are increased by 1.5, 2.25, and 1.5 times, respectively. Although the Thomson heat rate is small compared to that of the Peltier cooling and Joule heating, its impact will be more significant with

high μ_T materials. For example, by increasing the μ_T from 55 μV·K^{-1} to 450 μV·K^{-1}, the Thomson effect will be increased to 0.038 W, which is comparable to the Peltier cooling effect. Optimal pulse conditions and material properties are needed to maximize the supercooling effect and minimize the overheating effect. The effects of the Thomson coefficient, current pulse shapes, consecutive pulses, current pulse amplitude and duration, substrate volumetric heat capacity, and latent heat on the transient supercooling performance of holey silicon-based TEC are discussed in the rest of this section.

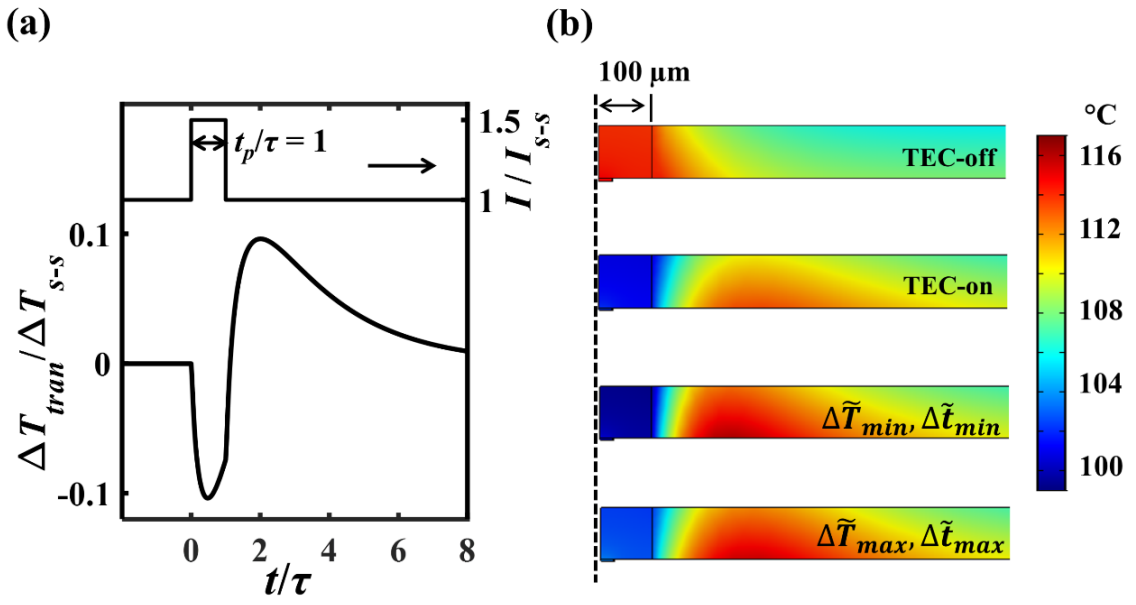

Figure 4.3 (a) Current pulse of 1.5$I_{s\text{-}s}$ and 5 ms (t_p/τ = 1) duration. The normalized hot spot temperature change is shown at the bottom. (b) Cross-sectional temperature profiles of half of the holey silicon-based TEC when hot spot temperature is at $T_{TEC\text{-}off}$, $T_{s\text{-}s}$, $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$, respectively. The double-sided arrow with 100 μm represents half of the Peltier cooler size (l_{cooler} = 200 μm).

4.3.1 Effects of the Thomson coefficient

The Thomson effect occurs inside the holey silicon substrate when the TEC is operating with an applied current. The μ_T of highly doped holey silicon used in our simulation is around 55

μV/K at 100 °C [46]. Figure 4.4(a) shows the temperature distribution along the holey silicon substrate from the Peltier cooler to the edge of the chip with $I_{s\text{-}s}$. Temperature first increases and then decreases along with holey silicon due to the Peltier cooling and Joule heating effects, yielding a large positive temperature gradient ($+\nabla T$) and a small negative temperature gradient ($-\nabla T$). Current flows from the Peltier cooler to the edge of the chip as shown in the inset of Figure 4.4(a). Thomson cooling first occurs as the temperature gradient is in the same direction of the current and then Thomson heating occurs as the change of temperature gradient direction. Due to the different values of the temperature gradients ($+\nabla T > -\nabla T$) as shown in Figure 4.4(a), a net Thomson cooling effect is applied to the hot spot. To evaluate the impact of μ_T on the transient supercooling, we change the μ_T from 0 to 450 μV/K with almost the same S at the interface between holey silicon and the Peltier cooler. Figure 4.4(b) shows the normalized transient hot spot temperature change with different μ_T. A square-shaped current pulse with an amplitude of $1.5I_{s\text{-}s}$ and a duration of τ is applied to the Peltier cooler. While the steady-state performance of four different μ_T has a similar hot spot temperature reduction of 15 °C due to the same S at the holey silicon/Peltier cooler interface, both supercooling and overheating performance are improved from the increase of μ_T due to the large temperature gradient change in transient cooling. For silicon-based material, μ_T can be controlled by modifying the doping concentration and dopant type [45,139]. The measured μ_T of phosphorus-doped holey silicon can be greater than 200 $\mu V \cdot K^{-1}$ with a doping concentration of 8×10^{18} cm^3 at 100 °C [139]. However, adjusting the doping concentration will also impact the overall cooling performance due to the change in electrical properties. For holey silicon-based TEC, the Thomson effect can be improved by increasing the temperature gradient, e.g., increase the current pulse amplitude, increase the hot spot heat flux, or reduce k_x of holey silicon. On the other hand, thermoelectric materials with a high μ_T and a high

thermoelectric figure of merit may benefit more from the supportive Thomson effect, especially at high temperatures. For example, the measured μ_T of single-crystal SnSe and K-doped PbTeSe can be up to 800 μV·K^{-1} at around 500 °C [140,141], and 400 μV·K^{-1} at 300 °C [140,142], respectively.

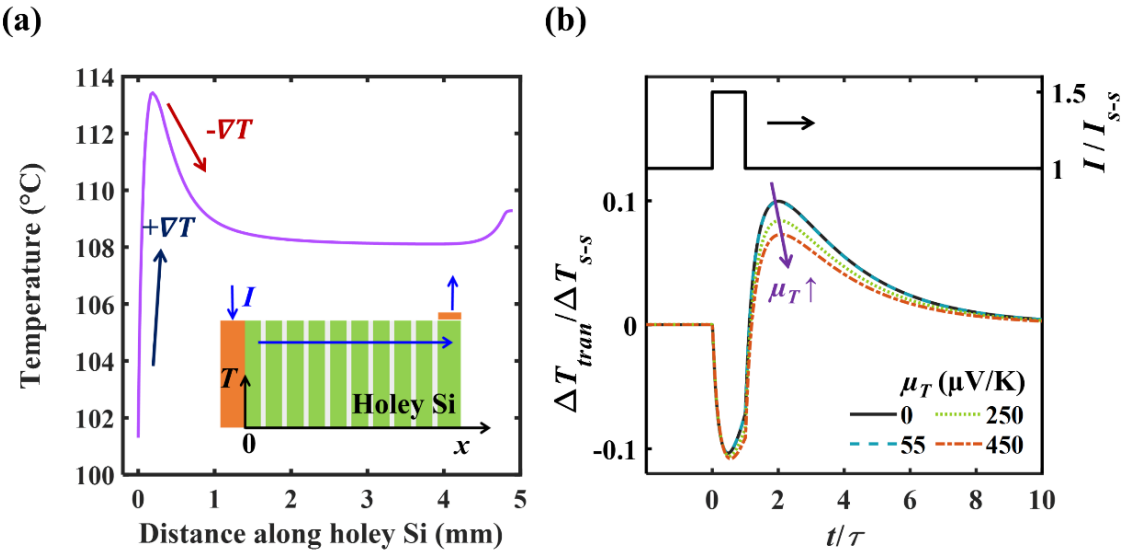

Figure 4.4 (a) Temperature distribution of along holey silicon substrate when the TEC is operating at $I_{s\text{-}s}$. A large positive temperature gradient (+∇T) and a small negative temperature gradient (-∇T) can be seen due to the impact of Peltier cooling and Joule heating effects. Inset shows the cross-sectional view of half of the holey silicon-based TEC. Current flows from the Peltier cooler to the edge of the chip. (b) Transient supercooling performance of holey silicon-based TEC with different μ_T. A step-shaped current pulse with an amplitude of 1.5$I_{s\text{-}s}$ and a duration of τ is applied..

4.3.2 Effects of current pulse shapes and consecutive pulses

The current pulse shape affects the transient supercooling significantly. To evaluate the impact of current pulse shapes, four different shapes (step, triangular, ramp up, and ramp down) with the same amplitude of 2$I_{s\text{-}s}$ and duration of τ are applied to the Peltier cooler. Figure 4.5(a) shows the current pulse shapes and the normalized transient hot spot temperature change. Figure 4.5(b) shows $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$. The triangular-shaped current pulse yields the largest temperature reduction in the supercooling regime and a small temperature overshoot in the overheating regime.

The step-shaped current pulse generates the greatest temperature overshoot that is 30% of the steady-state temperature reduction due to the largest area of current over time. The temperature overshoot for triangular-, ramp up- and ramp down-shaped current pulses are similar due to the same area of current over time. $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ are shown in Figure 4.5(c). $\Delta\tilde{t}_{min}$is related to the time for the current to reach I_p, so that ramp down- and step-shaped pulses have much smaller $\Delta\tilde{t}_{min}$ values. $\Delta\tilde{t}_{max}$ is similar for triangular-, ramp up-, and ramp down-shaped current pulses. The step-shaped pulse has the largest $\Delta\tilde{t}_{max}$ as it has the largest temperature overshoot due to the Joule heating effect. $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ are shown in Figure 4.5(d). The ramp up-shaped current pulse has the longest $\Delta\tilde{t}_c$ due to the minimum slope of current over time that leads to the smallest changing rate of Peltier cooling and Joule heating. The triangular-, ramp up- and ramp down-shaped current pulses have similar $\Delta\tilde{t}_h$ that is much shorter than that of the step-shaped current pulse. The maximum temperature is the key parameter for the thermal management of electronics [121], the triangular-shaped current pulse is selected to evaluate the effects of consecutive pulses, pulse amplitudes, and pulse durations as it provides the maximum temperature reduction in the supercooling regimes.

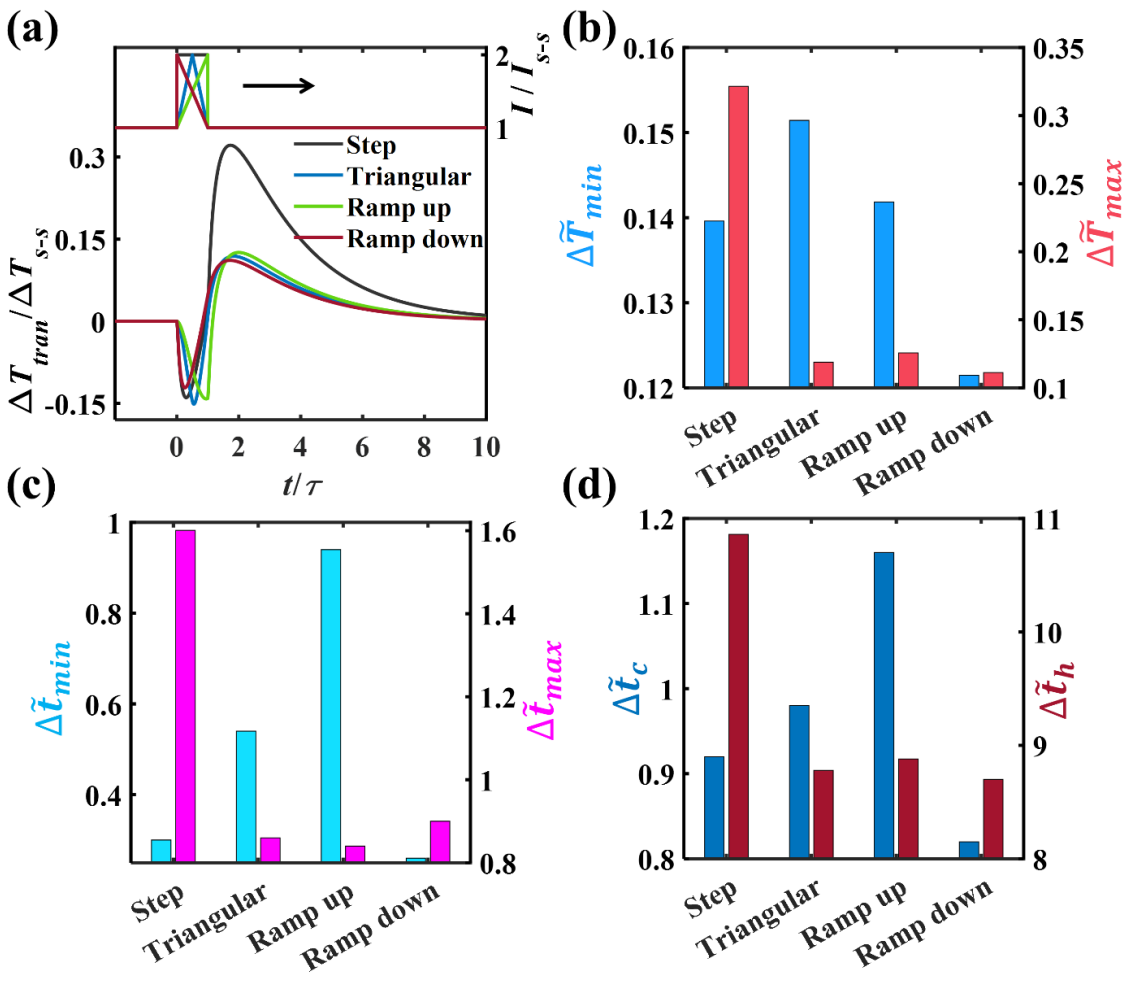

Figure 4.5 (a) Step, triangular, ramp up, and ramp down current pulse shapes and the normalized transient hot spot temperature change. The current pulse amplitude and duration are $2I_{s\text{-}s}$ and τ. (b) $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ for four different current pulse shapes. (c) $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ for four current pulse shapes. (d) $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ for four current pulse shapes.

We have simulated the hot spot temperature with three consecutive pulses to evaluate its impact on the hot spot temperature. The triangular-shaped current pulse with $2I_{s\text{-}s}$ amplitude and τ duration is used as the single pulse. Two representative pulse spacings (t_s) equaling 10τ and τ are used, which are larger than and smaller than the holding time of overheating regime of a single pulse, respectively. Figure 4.6(a) shows that when t_s/τ =10 and is larger than the $\Delta\tilde{t}_h$ of a single pulse, the hot spot temperature profile is a simple repeat of the single pulse case. Figure 4.6(b)

shows that when t_s/τ = 1 and is smaller than the $\Delta\tilde{t}_h$ of a single pulse, there are multiple cooling and heating regimes. When the first pulse is applied, the hot spot temperature profile is the same as the single pulse case. When the second pulse is applied, the hot spot temperature reduces immediately, and the minimum temperature is still lower than $T_{s\text{-}s}$. When the third pulse is applied, the hot spot temperature still reduces, but its minimum value becomes greater than $T_{s\text{-}s}$. The increased Peltier cooling from the current pulse is not sufficient to resist the Joule heating transferred to the hot spot. Moreover, the final temperature overshoot is much larger compared to that of the single pulse case due to the accumulated Joule heating. Compared to a single current pulse, consecutive pulses provide multiple cooling and heating regimes that may benefit the thermal management of hot spots with dynamic profiles. However, the temperature overshoot is much larger due to the accumulated Joule heating, which will be more severe for systems with low convection coefficients. In the rest of this chapter, we focus on the impact of a single current pulse to provide a general understanding of the transient supercooling in holey silicon-based TEC.

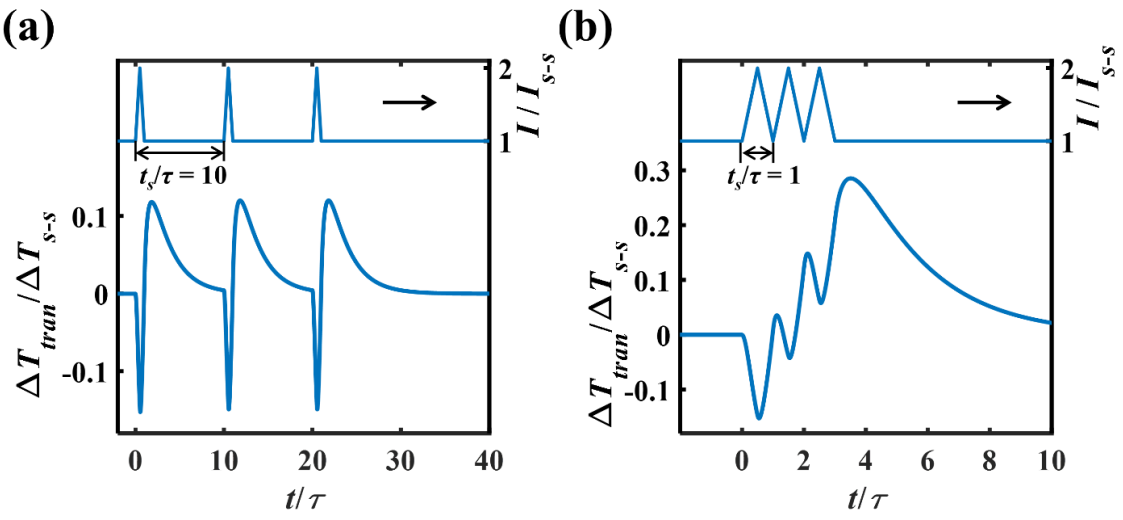

Figure 4.6 Transient hot spot temperature change with consecutive current pulses. The triangular-shaped current pulse with $2I_{s\text{-}s}$ amplitude and τ duration is used as the single pulse. t_s/τ equals (a) 10 (larger than $\Delta\tilde{t}_h$ of the single pulse) and (b) 1 (smaller than $\Delta\tilde{t}_h$ of the single pulse).

4.3.3 Effects of current pulse amplitudes and durations

To evaluate the impact of current pulse amplitude (I_p), the triangular-shaped current pulse with the same current pulse duration, τ, and different amplitudes of $1.5I_{s\text{-}s}$, $2I_{s\text{-}s}$, and $2.5I_{s\text{-}s}$ are applied to the Peltier cooler. Figure 4.7(a) shows the current pulses and the normalized transient hot spot temperature change. With the same current pulse duration, the current with a greater amplitude has a larger slope over time, which leads to a stronger Peltier cooling effect and a faster hot spot temperature reduction. However, a larger pulse amplitude also produces more Joule heating that is detrimental to the supercooling effect. Figure 4.7(b) shows $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ change with pulse amplitudes. $\Delta\tilde{T}_{min}$ increases with the increase of current pulse amplitude while $\Delta\tilde{T}_{max}$ increases more substantially. Figure 4.7(c) shows that $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ decreases with the increase of current pulse amplitude because the rapid change of current leads to a fast enhancement of Peltier cooling and Joule heating. Figure 4.7(d) shows that $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ decreases and increases with the increase of pulse amplitude, respectively. A fast change of current produces more Joule heating at the same time, which transfers back to the hot spot area that reduces and increases $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$, respectively. Increasing the current pulse amplitude could be potentially used for dynamic hot spots with a larger heat flux but a shorter duration.

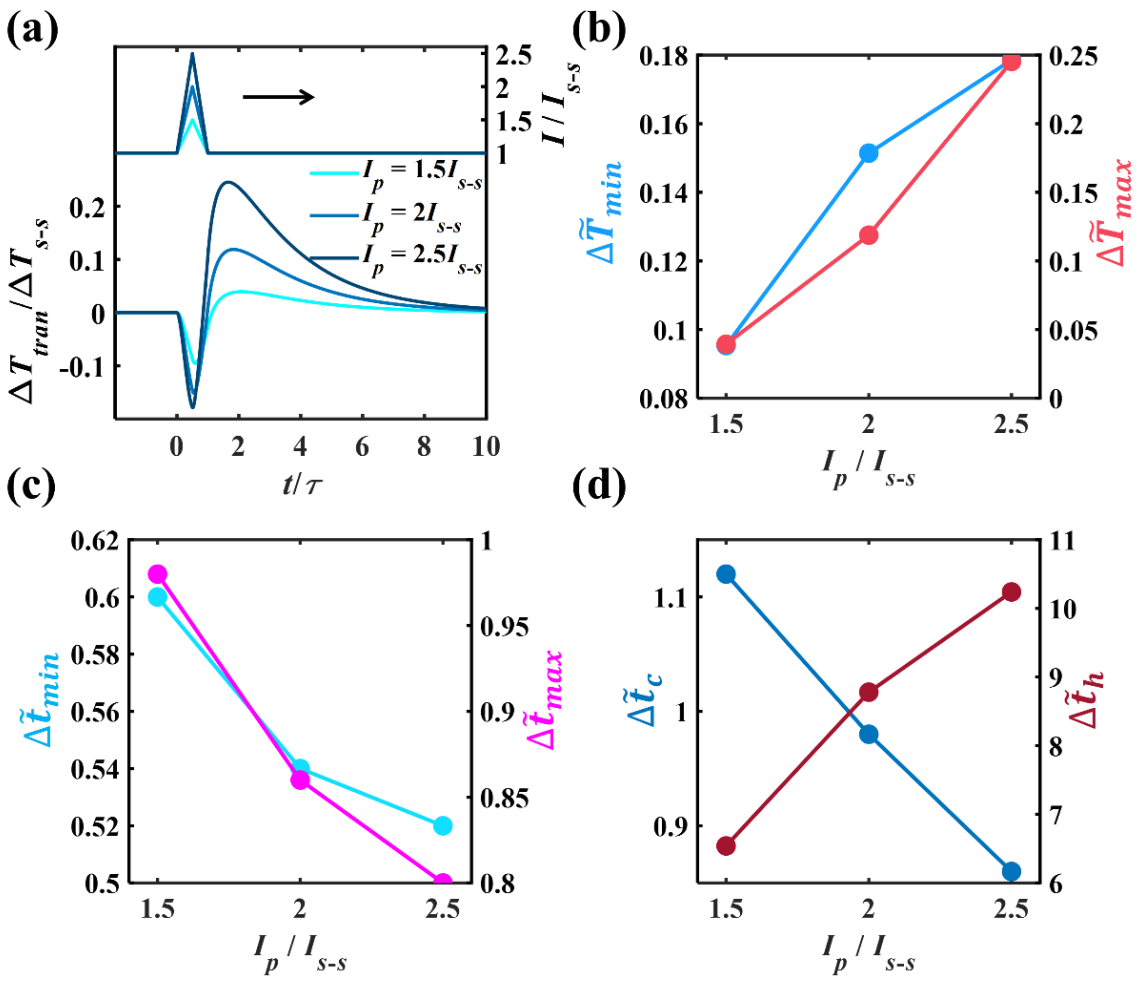

Figure 4.7 (a) Triangular-shaped current pulse and the normalized transient hot spot temperature change. The current pulses have amplitudes of $1.5I_{s\text{-}s}$, $2I_{s\text{-}s}$, and $2.5I_{s\text{-}s}$ and the same duration of τ. (b) $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ for three different current pulse amplitudes. (c) $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ for three different current pulse amplitudes. (d) $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ for three different current pulse amplitudes.

To evaluate the impact of current pulse duration, the triangular-shaped current pulse with durations (t_p) of 0.5τ, 0.75τ, τ, 1.5τ, and 2τ, and the same amplitude of $2I_{s\text{-}s}$ are used in the simulation. Figure 4-8(a) shows the current pulses and the normalized transient hot spot temperature change with time (t_p of 0.5τ, τ, and 2τ are shown for clarity). With the same current pulse amplitude, a larger pulse duration means a longer time to reach I_p and a wider span over time, which results in a slowly enhanced Peltier cooling effect and produces more Joule heating.

Figure 4.8(b) shows $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ change with pulse duration. $\Delta\tilde{T}_{min}$ first increases and then decreases with the pulse duration. For small pulse durations, at the moment that the current pulse reaches the maximum current, the enhanced Peltier cooling is still larger than the Joule heating that transferred back to the hot spot, indicating that the hot spot temperature can still be reduced. For large pulse durations, the Joule heating surpasses the enhanced Peltier cooling before the current pulse reaches the maximum value, resulting in a small hot spot temperature reduction. The optimal current pulse duration can be achieved between τ and 2τ. $\Delta\tilde{T}_{max}$ simply increases with current pulse width as the increase of Joule heating. Figure 4.8(c) and (d) shows that $\Delta\tilde{t}_{min}$, $\Delta\tilde{t}_{max}$, $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ increase with pulse duration. A larger pulse duration yields a slower enhancement of Peltier cooling, a longer time to reach the minimum hot spot temperature, and thus a longer holding time. A larger pulse duration also produces more Joule heating and inevitably leads to a larger $\Delta\tilde{t}_{max}$ and $\Delta\tilde{t}_h$. Increasing the current pulse duration could be potentially used for the dynamic hot spot with a longer duration but a lower heat flux.

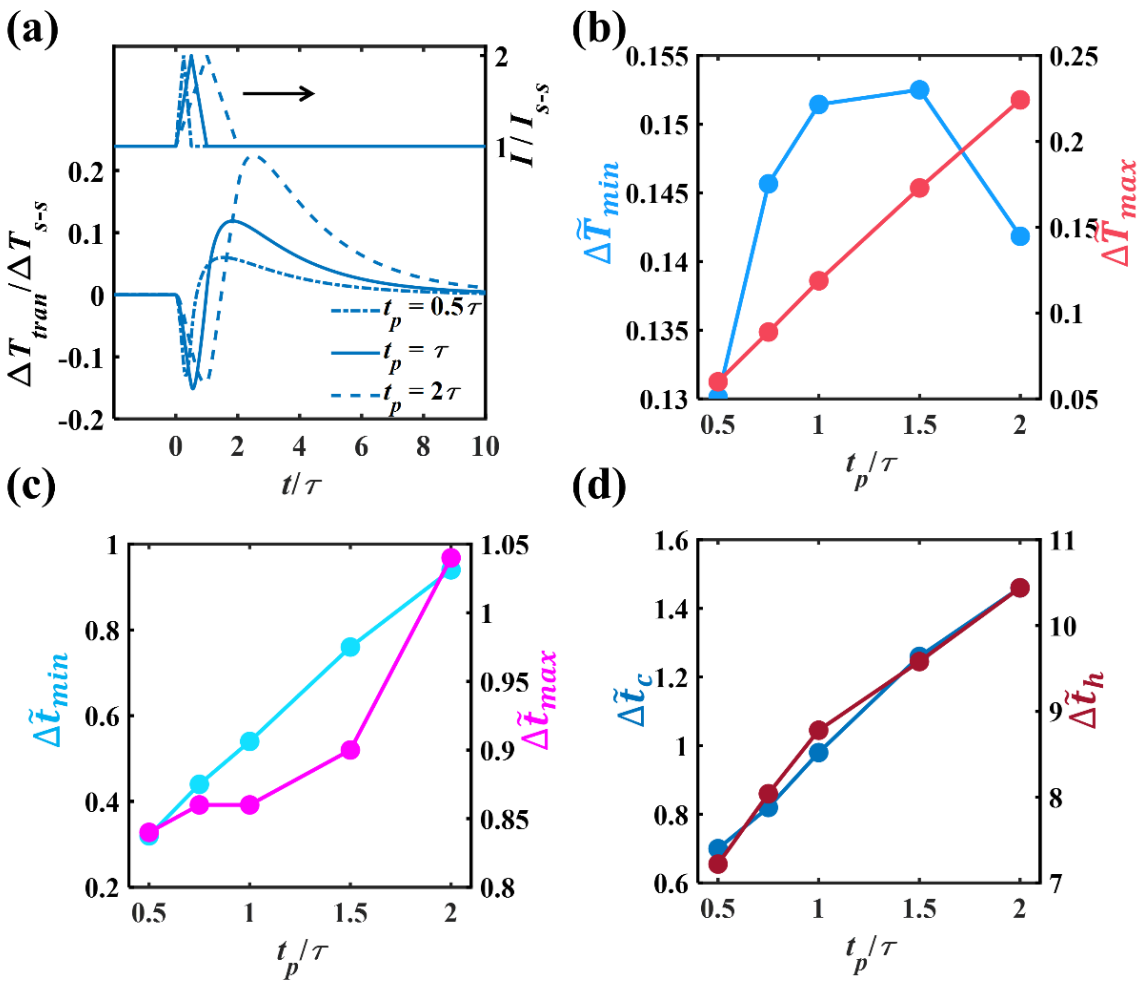

Figure 4.8 (a) Triangular-shaped current pulse and the normalized transient hot spot temperature change. The current pulses have the same amplitude of $1.5I_{s\text{-}s}$ and three durations of 0.5τ, τ, and 2τ. (b) $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ for five different current pulse durations. (c) $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ for five different current pulse durations. (d) $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ for five different current pulse durations.

4.3.4 Effects of phase change materials

The porous nature of holey silicon makes it possible to be integrated with different materials such as metal [122]. PCMs could be incorporated in holey silicon holes and improve the transient supercooling performance by increasing the substrate volumetric heat capacity and absorbing extra energy through phase change. We assume the holey silicon has the same

dimensions as previous sections to show the impacts of PCM fillers. The effects of substrate volumetric heat capacity (density and heat capacity) and latent heat on the transient supercooling are studied separately. In real applications, the filling of PCM with small holes could be challenging. Different holey silicon parameters and pre-treatment methods could be considered to improve the integration of PCM with holey silicon. Thin metal layers can be deposited on the silicon surface to improve the wetting with metallic PCM [143]. Prewetting solutions [144] and vacuum treatment [145] had been used to form polymer liners for high aspect ratio TSV applications. Similar methods could be potentially used to improve the wetting performance and reduce voids for polymer-based PCM.

The impact of substrate density and specific heat capacity can be combined as the change in volumetric heat capacity ($c = cp \times \rho$) as shown in Eq. (4.1). In our simulation, two different fillers that have densities of 900 kg·m^{-3} and 1000 kg·cm^{-3} and specific heat capacities of 1450 J·kg^{-1}K^{-1} and 2500 J·kg^{-1}K^{-1} are assumed to evaluate the impact of substrate volumetric heat capacity. Based on Eq. (4.5) and (4.6), the effective volumetric heat capacities of the PCM-filled holey silicon are calculated to be $1.25c_{HS}$ and $1.5c_{HS}$ and are used in the simulation with other material properties the same as holey silicon. Figure 4-9(a) shows the current pulse condition (triangular-shaped, $2I_{s\text{-}s}$, τ) and the normalized transient hot spot temperature change. Figure 4.9(b) shows that $\Delta\tilde{T}_{min}$ increases while $\Delta\tilde{T}_{max}$ decreases with the increase of substrate volumetric heat capacity. Figure 4.9(c) and (d) shows that $\Delta\tilde{t}_{min}$, $\Delta\tilde{t}_{max}$, $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ increase with the increase of substrate volumetric heat capacity. The increase of volumetric heat reduces the heat transfer rate inside the substrate which delays the diffusion of Joule heating without affecting the heat transfer between the Peltier cooler and hot spot.

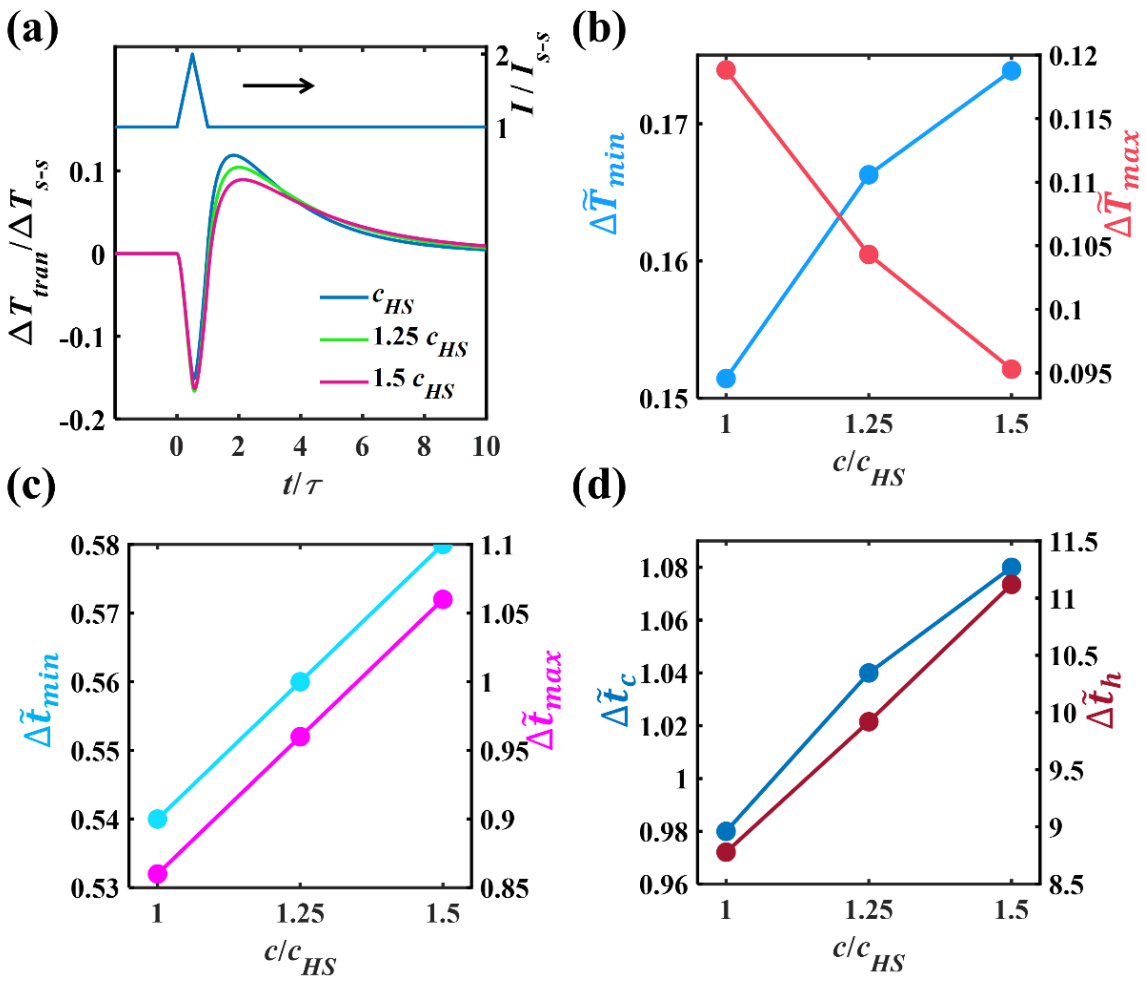

Figure 4.9 (a) Triangular-shaped current pulse and the normalized transient hot spot temperature change. The current pulse has an amplitude of $1.5I_{s\text{-}s}$ and a duration of τ. Three different substrate volumetric heat capacities c_{HS}, $1.2c_{HS}$, and $1.5c_{HS}$ are considered. (b) $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ for three different substrate volumetric heats. (c) $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ for three different substrate volumetric heats. (d) $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ for three different substrate volumetric heats.

Latent heat describes the energy release or absorption during a phase transition process with a narrow temperature range. The value of latent heat and phase transition temperature of PCMs vary with different materials [123,126,146]. In our simulations, latent heats of 150 kJ·kg^{-1} and 300 kJ·kg^{-1} are assumed for the PCM fillers. The effective latent heat of the PCM-filled holey silicon is calculated from eq. (4.7) to be 16 kJ·kg^{-1} and 32 kJ·kg^{-1}, respectively. The transition

temperature of PCM is set to be $T_{s\text{-}s}$. To evaluate the impact of latent heat, the same pulse condition and material properties are used. Figure 4.10(a) shows the current pulse condition and the normalized transient hot spot temperature change. PCM stores the thermal energy from the Joule heating effect at a narrow temperature range and releases it slowly, which increases the temperature reduction and reduces the temperature overshoot in supercooling and overheating regimes as shown in Figure 4.10(b). $\Delta\tilde{t}_{min}$, $\Delta\tilde{t}_{max}$, $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ all increase with the increase of latent heat as shown in Figure 4.10(c) and (d). The volumetric heat capacity and latent heat show a similar impact on the transient supercooling and the beneficial effect of PCM fillers is the combination of these two effects.

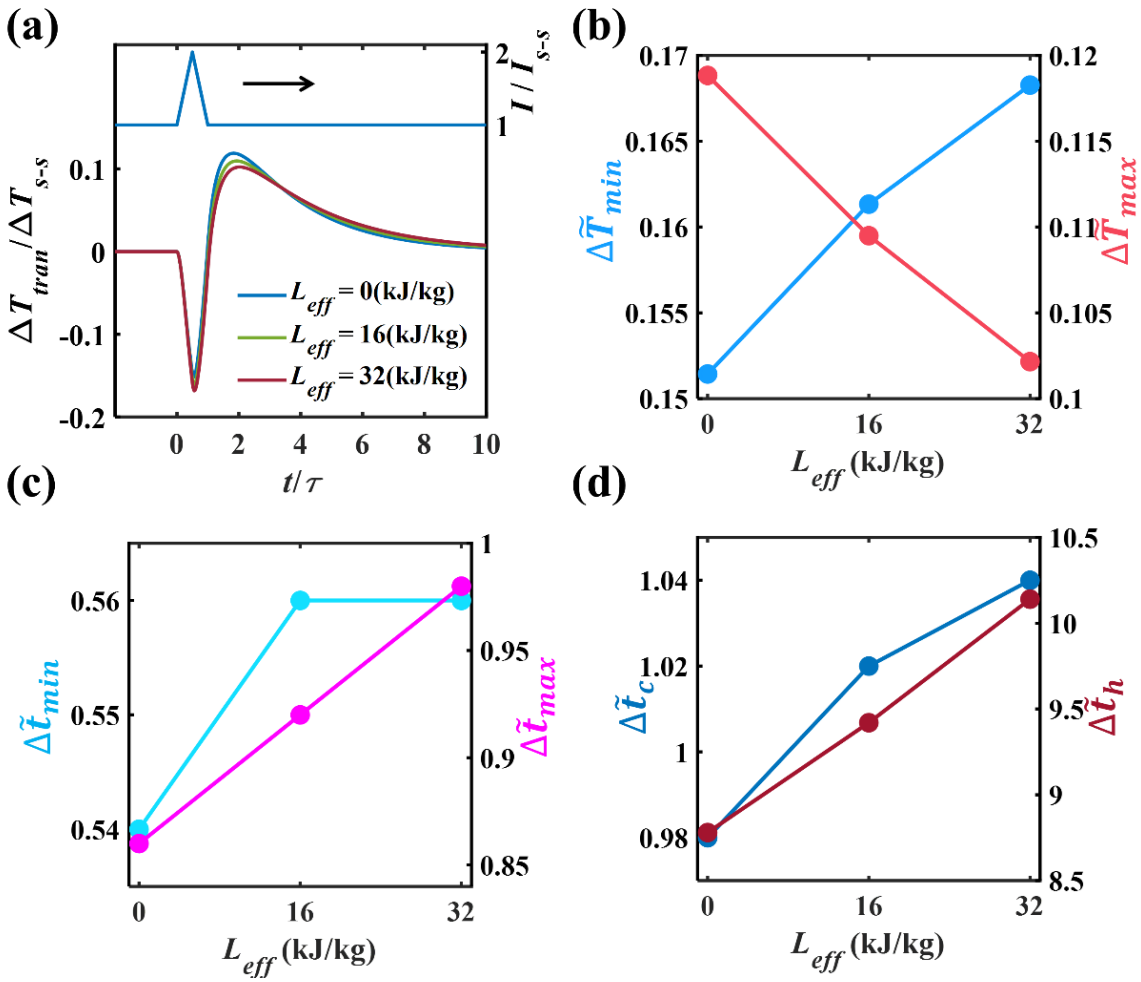

Figure 4.10 (a) Triangular-shaped current pulse and the normalized transient hot spot temperature change. The current pulse has an amplitude of $1.5I_{s\text{-}s}$ and a duration of τ. Three different substrate effective latent heats, 0 kJ·kg^{-1}, 16 kJ·kg^{-1}, and 32 kJ·kg^{-1} are considered. (b) $\Delta\tilde{T}_{min}$ and $\Delta\tilde{T}_{max}$ for three different substrate effective latent heats. (c) $\Delta\tilde{t}_{min}$ and $\Delta\tilde{t}_{max}$ for three different substrate effective latent heats. (d) $\Delta\tilde{t}_c$ and $\Delta\tilde{t}_h$ for three different substrate effective latent heats.

4.4 Conclusions

This chapter demonstrates the transient supercooling performance of a holey silicon-based lateral TEC by studying the temporal and spatial interplays of Peltier cooling, Joule heating, and Thomson effects with varying pulse conditions and material properties. A supercooling regime driven by Peltier cooling effect can be achieved before the Joule heating diffuse in and the thermal conductivity anisotropy is favorable by delaying the diffusion in the lateral direction while allowing rapid heat dissipation in the vertical direction. Our simulation results show that the Thomson effect is supportive of the transient supercooling due to the unique temperature distribution inside the holey silicon substrate. The impact of the Thomson effect becomes more significant with larger Thomson coefficients. A triangular-shaped current pulse can provide a 15% improvement in the hot spot temperature reduction compared to what is achievable in steady-state. Our simulation results show that the supercooling temperature reduction or holding time can be further improved by increasing the current pulse amplitude or duration, respectively. The transient supercooling performance can also be enhanced by incorporating with PCMs, in which the increase of substrate volumetric heat and the thermal energy absorption via phase transition delays the temperature overshoot. The holey silicon-based lateral TEC with anisotropic properties is promising to provide dynamic thermal management to on-chip hot spots.

Chapter 5: Experimental Demonstration of the Holey Silicon-based Thermoelectric Coolers

Lateral thermoelectric devices, where the Peltier cooling occurs over a small area, have shown promise for thermal management of on-chip hot spots, and because of the thermal transport direction, thermoelectric materials with anisotropic properties such as holey silicon have shown even more promising cooling potential. However, the experimental demonstration of the holey silicon-based thermoelectric cooling device has not been shown due to the challenges in fabricating high etching ratio holey silicon structures and integrating them into microscale devices. Here, we show the fabrication and measurement of an 80% etched holey silicon-based thermoelectric cooling device. With a Peltier cooler size of 300 μm and a holey silicon neck size of 2 μm, we report cooling of 0.96, 1.21, and 1.51 °C at 50, 100, and 150 °C background temperatures, respectively. The transient supercooling performance of the holey silicon-based thermoelectric cooler is also demonstrated, and the cooler temperature reduction can be further improved from 1.21 °C to 1.56 °C with a square-shaped current pulse at 100 °C background temperature. The impacts of current pulse amplitude and duration are also discussed. The holey silicon-based thermoelectric cooler offers excellent localized cooling capability and could be potentially used for the control of electronic hot spots.

5.1 Introduction

Recent trends toward nanoscale devices and three-dimensional integration call for a breakthrough in the thermal management of advanced electronics [22,49]. Moreover, the heat generation of electronic chips is highly non-uniform, which creates local hot spots with elevated temperature and heat flux [3,147]. Cooling strategies based on high-thermal-conductivity materials

or advanced heat exchangers can be potentially used to provide cooling to a large area with a high overall power [86,87]. However, they cannot offer site-specific cooling to local hot spots, and thus may provide unnecessary overcooling and lead to inefficient and bulky thermal systems [24]. Thermoelectric cooling devices have been demonstrated as an effective method for hot spot management and offer unique attributes including solid-state operation and system scalability [13,16,20,24,148,149]. Significant advances have also been made in increasing the thermoelectric figure of merit through nanostructuring and controlled doping [54,55].

While previous efforts have shown the promise of thermoelectric cooling devices for hot spot management, most materials are based on complex semiconductors or low-dimensional structures that are not compatible with microelectronic processes [55–58]. Silicon, on the other hand, offers advantageous attributes that facilitate the integration with electronics and has been considered for lateral thermoelectric cooling devices [29,112,148]. The high lattice thermal conductivity of silicon is the major limit to its cooling performance. And in recent years, silicon nanostructures have been demonstrated significantly reduced thermal conductivity and improved prospects for thermoelectric applications [35–37,43,46]. Among them, holey silicon has attracted increasing attention due to its improved thermoelectric properties and unique thermal conductivity anisotropy [89]. For holey silicon-based lateral thermoelectric devices, the low in-plane thermal conductivity caused by the substantial phonon boundary scattering in small necks is expected to sustain a large temperature gradient for Peltier junctions, and the high cross-plane thermal conductivity due to the persistence of long wavelength phonons is expected to facilitate heat dissipation from a heat source to a heat sink. Our previous numerical studies have shown that holey silicon is favorable for hot spot cooling under steady-state and transient conditions [89,122,150].

In this chapter, we have experimentally demonstrated the local cooling abilities of holey silicon-based lateral thermoelectric devices. We fabricate holey silicon-based lateral thermoelectric devices through standard semiconductor processes. An Infrared (IR) thermography-based method is developed to measure the cooler temperature change and to show the temperature distribution across the whole device. The cooler temperature reduction is evaluated with different background temperatures and time scales. Numerical models are also developed to capture the measurement data and to predict the hot spot cooling performance. Our results show that holey silicon-based thermoelectric devices provide more temperature reduction than that of bulk silicon-based devices due to the size effect and could be potentially used for the thermal management of on-chip hot spots.

5.2 Holey Silicon-based Thermoelectric Cooler Development

In this section, the design and fabrication recipes of holey silicon-based TEC are discussed. Numerical models are also developed to capture the measurement data and to predict the cooling performance of a fully etched holey silicon-based TEC.

5.2.1 Design of the holey silicon-based thermoelectric cooler

A special SOI-like wafer is used for the holey silicon TEC fabrication. The wafer contains a 25 μm device layer, a 500 μm Pyrex layer, and a 500 μm silicon layer. The device layer is used for TEC fabrication, which is designed to be around 25 μm to facilitate the etching of holey silicon. The 500 μm Pyrex wafer is anodically bonded to the device layer to sustain the temperature gradient between the Peltier junctions. The bottom 500 μm Si layer is bonded to the other side of

the Pyrex layer to provide mechanical support during the fabrication. Figure 5.1(a) shows the top-down view of the holey silicon-based TEC. The Peltier cooler and ground electrode are deposited on the silicon substrate and separated by holey silicon. Figure 5.1(b) shows the cross-sectional view along the black dashed line. Metal wires are bonded to the Peltier cooler and ground electrode to provide current for the TEC operation. The Peltier cooler and ground electrode are placed close to the edge of the chip to reduce the length of the metal wire to reduce the impact from wire Joule heating.

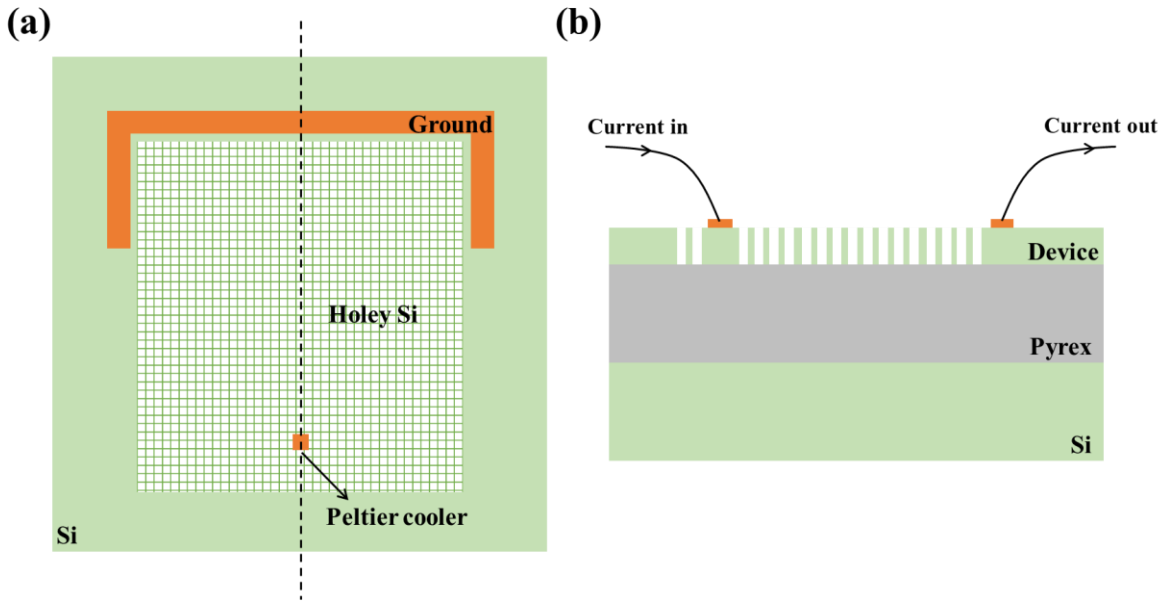

Figure 5.1 (a). The top-down schematic of the holey silicon-based TEC. (b) The cross-sectional view of the holey silicon-based TEC.

5.2.2 Fabrication recipes of the holey silicon-based thermoelectric cooler

One advantage of the holey silicon-based TEC is that it can be fabricated through standard semiconductor processes. The fabrication of the holey silicon-based TEC involves the fabrication of the special SOI-like wafer, two steps of lithography, one step of metal deposition, and one step of dry etching as shown in Figure 5.2. The first step is to fabricate the special SOI-like wafer. It

starts with a 500 µm thick highly doped silicon wafer (Figure 5.2(a)), which is anodically bonded to a 500 µm Pyrex wafer (Figure 5.2(b)). The silicon wafer is then ground down to around 25 µm and the surface of the silicon layer is polished as shown in Figure 5.2(c). Finally, another 500 µm silicon wafer is bonded to the other side of the Pyrex wafer to be used for mechanical support as shown in Figure 5.2(d). The second step is device fabrication. A 2.6 µm thick Shipley 1827 photoresist (PR) is spin coated on the device layer (500 rpm for 10s and 3000 rpm for 30s). The PR is later exposed using Karl Suss MA6 mask aligner (Low vacuum contact and 24s expose time) and developed in MF 319 solution for 1 minute. The whole wafer is then immersed in Buffered Oxide Etch solution for 1 minute to remove the native oxide layer on the silicon surface. The following step is metal deposition, where a Ti adhesion layer (0.4 Å/s, 100 Å) and an Ag electrode layer (0.8 Å/s, 3000 Å) are deposited on the wafer surface using Temescal CV-8 electron beam evaporator. The next step is the lift-off process, where the wafer is immersed in acetone solution with sonication to dissolve the PR and to remove the metal layer that is not in contact with the device layer directly. The metal electrodes can be seen after the lift-off process as shown in Figure 5.2(e). The final process is holey silicon fabrication. Lithography is first performed to transfer the holey silicon pattern from the mask to the device layer, and then deep reactive ion etching (DRIE) is performed on the wafer to use PR as the mask to etch holey silicon structures. The holey silicon-based TEC can be seen after the removal of the unetched PR as shown in Figure 5.2(f). After dry etching, the wafer is diced into individual TEC devices using ADT 7910 dicing saw.

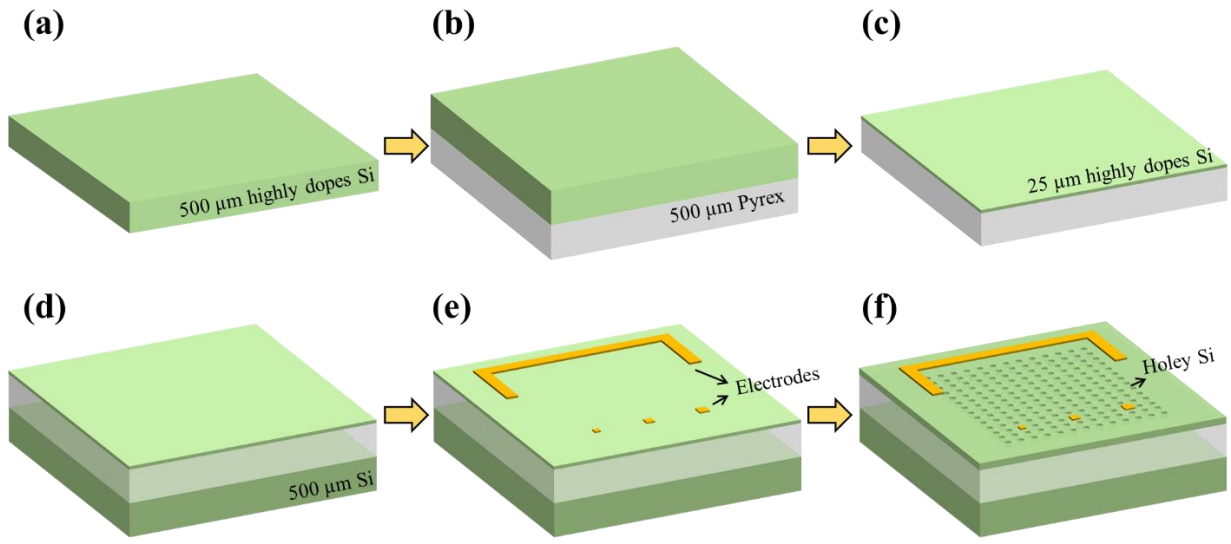

Figure 5.2 The fabrication process of the holey silicon-based TEC. (a) A 500 µm thick highly doped silicon wafer. (b) Anodic wafer bonding of silicon and Pyrex. (c) Si wafer grinding and polishing. (d) Anodic wafer bonding of another 500 µm thick silicon with the other side of the Pyrex. (e) Metal deposition and lift off. (f) Dry etching.

5.3 Measurement of the Holey Silicon-based thermoelectric cooler

An IR thermography-based method is used for the TEC measurement. After dicing into individual devices, the holey silicon-based TEC is placed on a chip carrier for wire bonding. Two 25 µm Al wires are bonded to the Peltier cooler and ground as shown in Figure 5.3(a). Because the holey silicon-based TEC has multiple structures with different emissivity values, an emissivity coating (Rust-Oleum high heat primer) is applied to the surface of the TEC device. A piece of Pyrex wafer is pasted close to the TEC device using sliver paste to calibrate the emissivity of the coating. The emissivity of the Pyrex wafer is measured to be 0.816±0.005 using a Fourie-transform infrared (FTIR) spectrometer. The chip carrier is connected to a Cu state that is put on a heater as shown in Figure 5.3(b). The temperature of the heater is controlled through a Lake Shore temperature controller (Model 335) as the background temperature for the TEC measurement. Two

wires from the Agilent E3631A power supply are connected to the pin of the chip carrier to provide electrical current to the TEC device. The whole setup is put inside a vacuum chamber (JANIS VPF-800) to improve the IR image quality and to stabilize the temperature as shown in Figure 5.3(c).

A FLIR A655sc IR camera is used for the IR measurement, which has a resolution of 25 μm/pixel and can detect the temperature difference down to 30 mK. After the device temperature is stabilized, the emissivity of the cooler area is calibrated with the emissivity of the Pyrex. At 100 °C background temperature, the emissivity of the cooler is calibrated to be 0.82. The average temperature of the green box with 82 pixels is recorded as the cooler temperature as shown in Figure 5. Before the measurement, the TEC device is first stabilized for 30 mins in the vacuum chamber until the temperature stabilizes at the background temperature. Then, current/voltage is applied to the Peltier cooler and the cooler temperature reduction at steady-state is recorded.

The frame subtraction method is used to show the cooling performance. The frame when the TEC is off is used as the reference and is subtracted by the frame when TEC is on. The temperature difference between the two frames shows the TEC performance. If the frame subtracted value is negative, it means Peltier cooling as the temperature is reduced, and if the frame subtracted value is positive, it means Peltier heating as the temperature is increased. The accuracy of the IR camera is ±2% of the reading and the standard deviation during the measurement is 0.1 °C [151]. For each current, the cooler temperature reduction is measured at least three times.

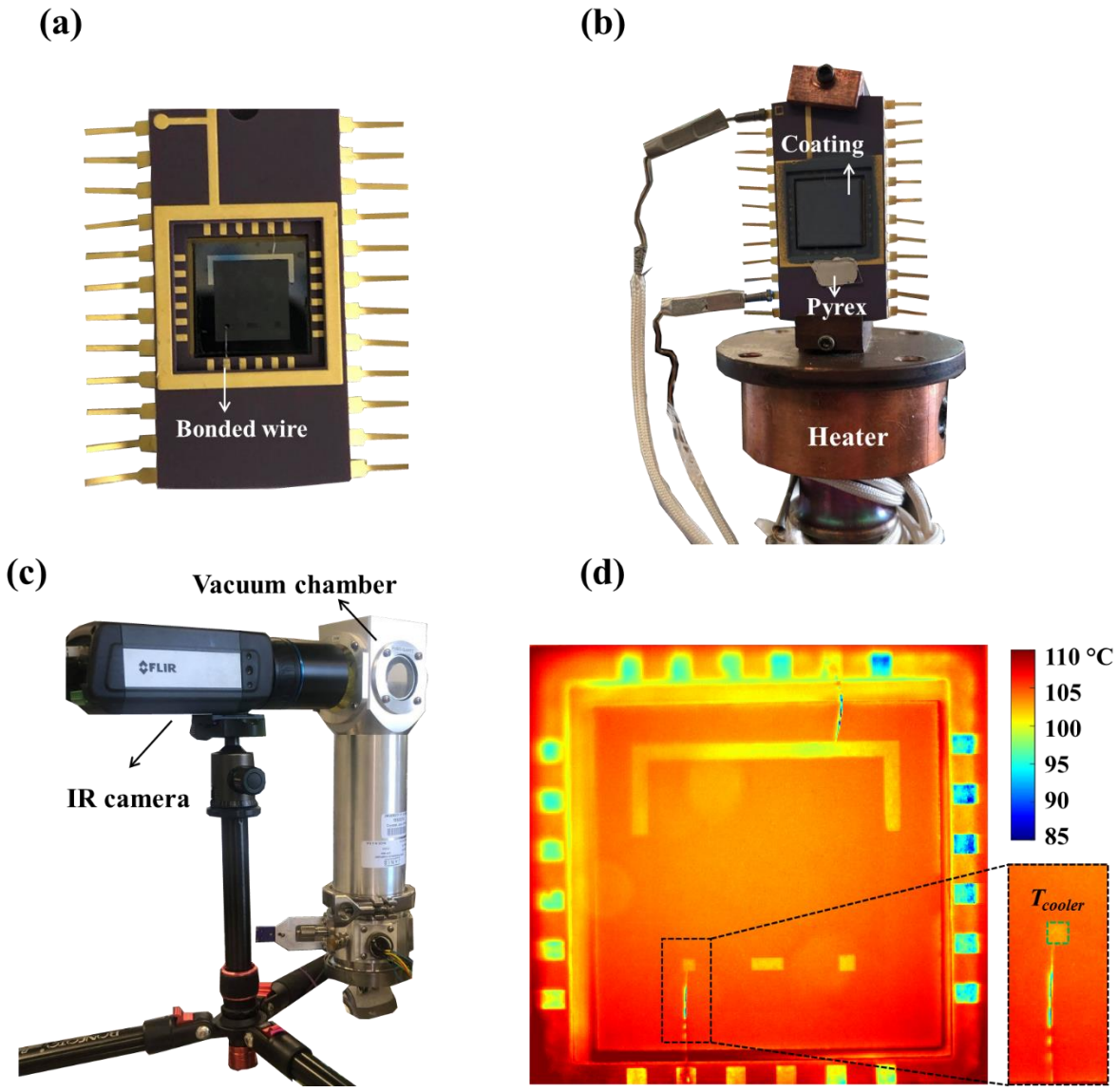

Figure 5.3 (a) Holey silicon-based TEC device in a chip holder after wire bonding. (b) Electrical connection for the chip holder. The heater with a temperature controller is used to set up the background temperature. The Pyrex wafer piece is used to calibrate the emissivity of the coating. (c) The chip holder and heater are placed inside a vacuum chamber for IR measurement. (d) IR image example of the TEC device at 100 °C background temperature. The average temperature of the green box is used as the average temperature for the cooler.

5.4 Results and Discussion

5.4.1 Characterization of the fabricated holey silicon

The holey silicon-based TEC is characterized with SEM for the neck size and etching depth. Figure 3 shows the top-down and cross-sectional SEM images of the TEC device. Figure 5.4(a) shows the top-down view of the holey silicon-based TEC over the Peltier cooler area. Figure 5.4(b) shows the zoom-in image of the holey silicon, the pitch size of the holey silicon is around 10.2 μm and the neck size of the holey silicon is around 1.9 μm. Figure 5.4(c) shows the cross-sectional SEM image of the holey silicon structure. The thickness of the device layer is 26 μm and the etching depth of the holey silicon is 21 μm, which equals to 80% etching ratio. The anodic bonding interface between the device layer and the Pyrex substrate can also be seen.

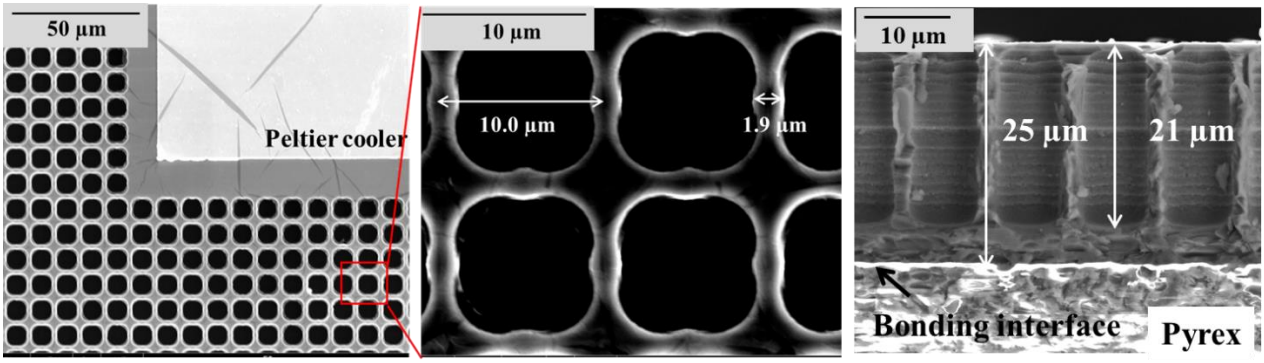

Figure 5.4 (a) The top-down SEM image for the holey silicon-based TEC over the Peltier cooler area. (b) Zoom-in image of the holey silicon area. (c) Cross-sectional SEM image of the holey silicon. The anodic bonding interface can also be seen.

5.4.2 Steady-state performance of the holey silicon-based thermoelectric cooler

The steady-state cooling performance of the holey silicon-based TEC is first measured at 100 °C background temperature. Figure 5.5(a) shows the cooler temperature change with applied current. A parabolic curve can be seen that the cooler temperature first decreases with the increase of current and increases. The maximum cooler temperature reduction is -1.2 °C and the optimal applied current is 0.046A. A numerical model is also developed to capture the measurement data. The thermal conductivity of the holey silicon is calculated based on the spectrum scaling model [89] and the electrical properties are from the literature [29] assuming a doping concentration of

around 10^{19} cm^{-3}. The effective thermal conductivity of holey silicon is calculated to be {12, 12, 30} $W \cdot m^{-1} \cdot K^{-1}$ and the effective electrical conductivity and the Seebeck coefficient of holey silicon are 0.32×10^4 $S \cdot m^{-1}$ and 540 $\mu V \cdot K^{-1}$, respectively. A convection coefficient of 600 $Wm^{-2}K^{-1}$ is applied to the backside of the silicon substrate with an external temperature of 100 °C, which is the fitting parameter from the experiments. The Joule heating from the bonded wire is also considered. The electrical resistance of the bonded wire is estimated based on the length of the wire, which are 0.2 Ω and 0.15 Ω for the wire connects to the Peltier cooler and ground electrode, respectively. The cooler temperature change from the numerical model fits with the experimental data well as shown in Figure 5.5(a). As shown in the cross-sectional image, the holey silicon is 80% etched and the cooling performance will be better with 100% etching as the unetched silicon under the holey silicon has much larger thermal conductivity and loses heat. Numerical simulation is further performed for 0% etched case (bulk Si TEC) and 100% etched case. The maximum cooler temperature reduction is -0.8 °C for the 0% etched case and the maximum cooler temperature reduction is 1.6 °C for the fully etched case. Increasing the etch depth can further enhance the cooling performance of the holey silicon-based TEC.

One advantage of the IR thermography-based method is the ability to show the temperature distribution of the whole device. Figure 5.5(b) shows the frame subtracted temperature profiles of the holey silicon-based TEC with the optimal applied current ($I_{s\text{-}s}$ = 0.046A), the cooler area has reduced temperature and the ground electrode area has increased temperature. Figure 5.5(c) shows the TEC temperature distribution from the numerical modeling at the same current. The temperature profile fits with the measurement result. Black arrows indicate the normalized current distribution. It can be seen that the current moves from the Peltier cooler to three different places of the ground electrode, which leads to three hot spots over the ground electrode.

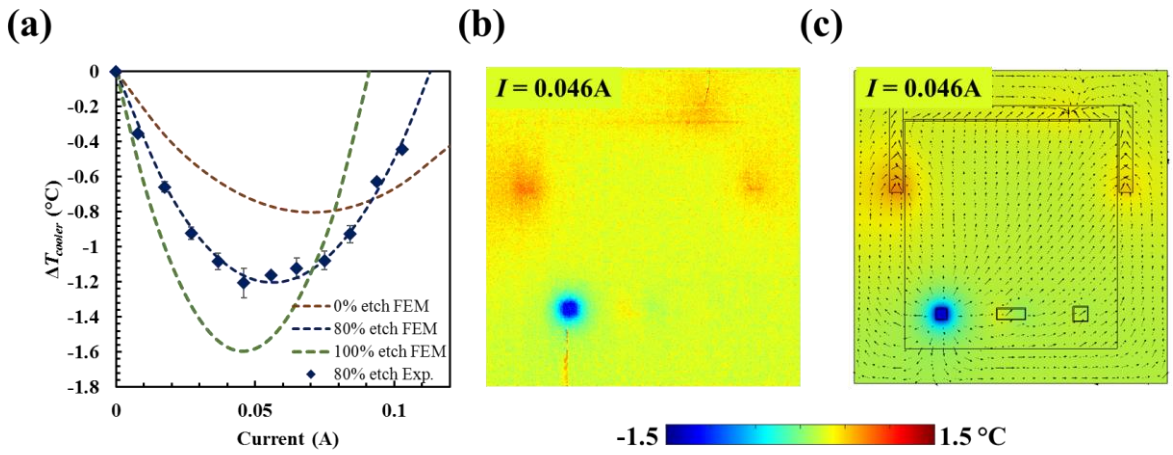

Figure 5.5 (a) Numerical and experimental results of the 80% etched TEC's cooler temperature change at 100 °C background temperature. Numerical results of the 0% and 100% etched TEC are also shown for comparison. (b) The experimental temperature profile of the holey silicon-based TEC at 0.046 A. (c) Numerical temperature profile of the holey silicon-based TEC at 0.046 A.

The cooler temperature reduction is also related to the background temperature. Three different background temperatures of 50 °C, 100 °C, and 150 °C are considered in the measurement. Figure 5.6 shows experimental and simulation data of the cooler temperature change with different background temperatures. Different convection coefficients are considered for different background temperatures as the Cu stage and sliver paste resistance increases with the temperature. 700 $Wm^{-2}K^{-1}$, 600 $Wm^{-2}K^{-1}$, and 500 $Wm^{-2}K^{-1}$ are used for 50 °C, 100 °C, and 150 °C background temperatures, respectively. It can be seen that with the increase of the background temperature, the cooler temperature reduction increases.

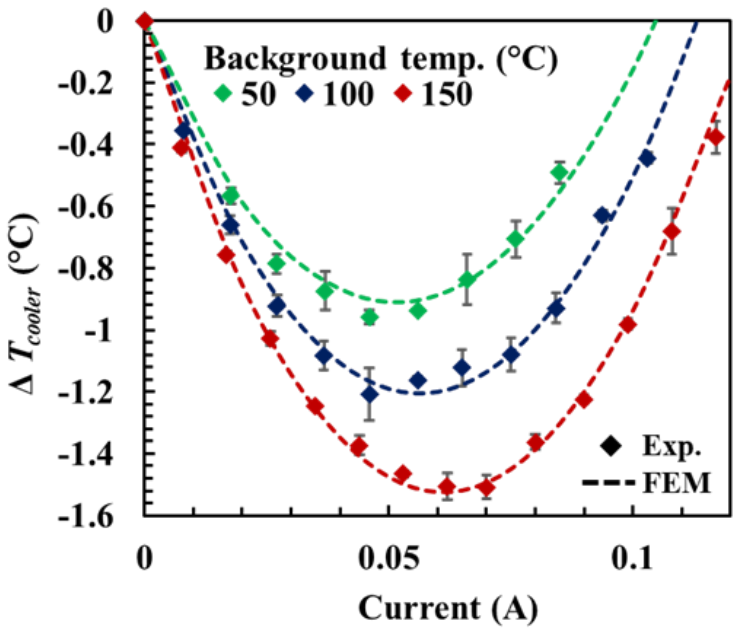

Figure 5.6 (a) Cooler temperature change of the 80% etched holey silicon-based TEC at 50 °C, 100 °C, and 150 °C background temperatures.

5.4.3 Transient performance of the holey silicon-based thermoelectric cooler

The transient performance of the holey silicon-based TEC is also evaluated. As we have previously discussed, transient supercooling can be achieved for the holey silicon-based TEC with a current pulse. When a current pulse is applied, the Peltier cooler temperature reduces immediately as the Peltier effect is an interfacial effect, and then the Peltier cooler temperature increases due to the diffusion of the Joule heating as the Joule heating effect is a volumetric effect. Figure 5.7(a) shows one example of the transient supercooling at 100 °C background temperature. A current of 0.046 A ($I_{s\text{-}s}$, optimal current at steady-state) is first applied to the Peltier cooler for 160s until the Peltier cooler temperature reduction (ΔT_{cooler}) is stabilized at -1.2 °C. The temperature profile of the steady-state cooling is shown in Figure 5.7(b). A square-shaped current pulse with 2s duration and 0.0092 A ($2I_{s\text{-}s}$) is then applied to the Peltier cooler. The cooler temperature reduces immediately as the increased Peltier cooling. Figure 5.7(c) shows the

temperature profile of the supercooling regime with the minimum temperature, the cooler temperature reduction is increased to 1.56 °C. Joule heating generated by the increased current gradually diffuses to the Peltier cooler area, and the cooler temperature starts to increase. Figure 8(d) shows the overheating regime with the maximum temperature, the cooler temperature reduction is increased to 0.84 °C that is larger than the steady-state temperature reduction with the optimal applied current.

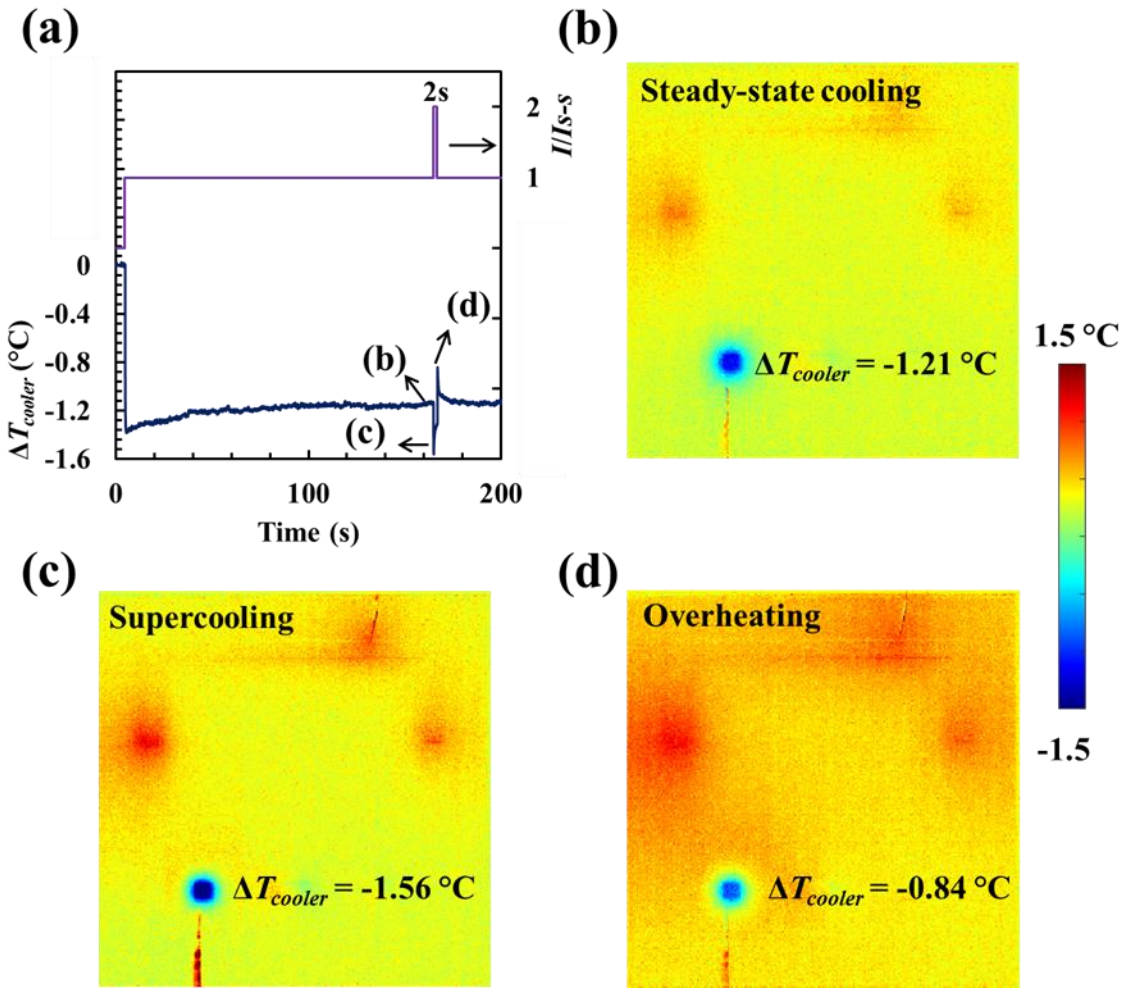

Figure 5.7 (a) Transient cooler temperature change with the optimal applied current ($I_{s\text{-}s}$ = 0.046 A) and a square-shaped current pulse ($2I_{s\text{-}s}$ amplitude and 2s duration). (b) IR temperature profiles for the steady-state cooling. (c) IR temperature profile for the supercooling regime when the cooler

temperature reaches the minimum value. (d) IR temperature profile for the overheating regime when the cooler temperature reaches the maximum value.

The transient supercooling performance is also impacted by the current pulse amplitude and duration. To evaluate their impacts, the cooler temperature change with different current pulse amplitude and duration are shown in Figure 9. Figure 5.8(a) shows the cooler temperature change with current pulse amplitudes of $1.6I_{s\text{-}s}$, $2I_{s\text{-}s}$, and $2.4I_{s\text{-}s}$, and 3s duration. With the increase of the current pulse amplitude, the supercooling temperature reduction increases, but the temperature overshoot also increases, and the cooling period decreases. Figure 5.8(b) shows the cooler temperature change with current pulse durations of 1s, 2s, and 3s, and $2I_{s\text{-}s}$ amplitude. The minimum temperature that can be achieved with supercooling does not change with the current pulse duration change, while the cooling period extends with the increase of current pulse duration. The temperature overshoot also increases with the increase of current pulse duration due to the increased Joule heating.

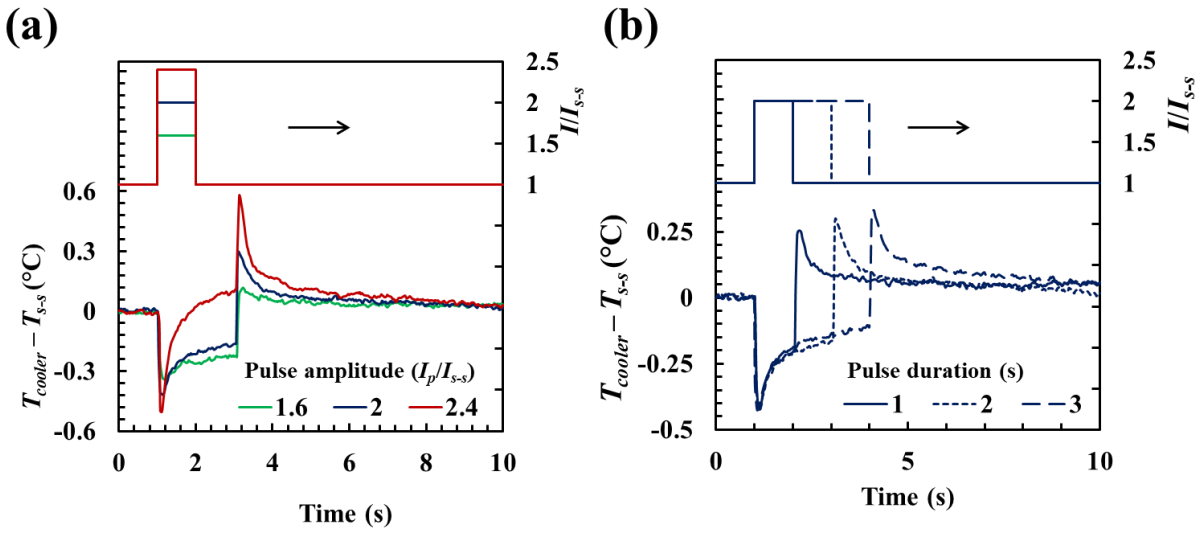

Figure 5.8 (a) Transient cooler temperature change with square-shaped current pulses. The current pulse amplitudes are $1.6I_{s\text{-}s}$, $2I_{s\text{-}s}$, and $2.4I_{s\text{-}s}$, respectively, and the duration is fixed at 2s. (b)

Transient cooler temperature change with square-shaped current pulses. The current pulse durations are 1s, 2s, and 3s, respectively, and the amplitude is fixed at $2I_{s\text{-}s}$.

5.5 Conclusions

In this chapter, we have experimentally demonstrated the cooling performance of the holey silicon-based TEC. The holey silicon-based TEC is successfully fabricated through standard semiconductor processes. An IR thermography-based method is developed to measure the cooler temperature reduction. The holey silicon-based TEC provides 1.2 °C temperature reduction at 100 °C background temperature, and the temperature reduction can be increased to 1.5 °C at 150 °C background temperature. Transient supercooling is also demonstrated for the holey silicon-based TEC. With a square-shaped current pulse of $2I_{s\text{-}s}$ amplitude and 2s duration, the cooler temperature reduction can be temporarily increased to 1.56 °C at 100 °C background temperature. The supercooling temperature reduction can be increased by increasing the current pulse amplitude, and the supercooling period can be extended by increasing the current pulse duration. The transient supercooling can be used for the thermal management of dynamic hot spots.

Chapter 6: Thermal TSV Optimization and Hierarchical Floorplanning for 3D Integrated Circuits

While 3D ICs offer many advantages over 2D ICs, thermal management challenges remain unresolved. Thermal through-silicon-vias (TTSVs) are TSVs that facilitate heat transfer across stacked dies without carrying signal and provide a potential thermal management solution to 3D ICs. However, the use of TTSVs increases the distance between IC blocks and signal delay. The trade-off between temperature and wirelength is difficult to avoid in TTSV-integrated 3D ICs. Here we present a hierarchical approach to optimize the floorplan of a 3D Nehalem-based multi-core processor via simulated annealing (SA). Our simulations show that an increase in TTSV area accompanies a decrease in peak temperature, but the wirelength strongly depends on the TTSV placement, which is uniquely optimized for each case of the allowed TTSV area. Compared to the floorplan with a fixed TTSV placement that places TTSV between cores, our algorithm optimally places TTSVs between IC blocks and finds an optimal floorplan with the minimum cost of peak temperature, wirelength, and area at 6% TTSV area overhead. The peak temperature is reduced from 116 °C to 100 °C with only 3.5% increase in wirelength. Our floorplan optimization method can provide effective thermal management solutions to 3D ICs.

6.1 Introduction

As the CMOS technology continuously scales down into the deep submicron regime and approaches the physical limits of minimization, the performance improvement through device scaling becomes more challenging [152]. 3D integration technology [153–156] is based on interlayer connections and through-silicon-vias (TSVs), which offers several benefits over 2D integration including higher packaging density, lower wire delay, and less power consumption [8,157]. 3D ICs

encounter inevitable thermal management problems because of two main reasons: 1) high power density caused by a large number of active layers per unit area; 2) high thermal resistance caused by the stacked structure and low-thermal-conductivity interconnect layers [158–161]. Moreover, the aggressive wafer thinning process makes the thermal management of 3D ICs more challenging [89].

Various approaches have been proposed to address thermal issues in 3D ICs [162]. Forced liquid cooling solutions based on single- or two-phase flow with micro-channels are effective in reducing the on-chip temperature [163–167], but liquid cooling approaches may entail packaging issues. Thermoelectric cooling (TEC) has received considerable attention as a solid-state cooling solution for local hotspots [3,122]. However, TEC consumes extra power and has low energy efficiency [168]. On the other hand, TSVs are widely used in 3D ICs and can provide passive cooling due to high-thermal-conductivity metal vias. While signal TSVs (STSVs) are TSVs that carry both electrical signal and heat between dies [169–171], thermal TSVs (TTSVs) are dummy TSVs that facilitate heat transfer across 3D ICs.

Applying TTSVs uniformly across the die or specifically near hotspots can reduce the peak temperature [90,172–174]. However, TTSVs occupy additional space and increase the distance between IC blocks, which affect the performance by increasing the power consumption and signal delay (e.g., $Delay = \frac{1}{2} R_{wire} C_{wire}$, R_{wire} and C_{wire} are the total wire resistance and capacitance that are proportional to wirelength [175]). The corresponding trade-off between temperature and wirelength needs to be addressed for the TTSV placement. Wong and Lim [176] presented a simulated annealing (SA)-based floorplanning technique with a random walk based TTSV insertion algorithm, which achieves a 17% temperature reduction with 3% TTSV density. However, inserting TTSV to the hottest unit may not be possible because the TSVs are usually ten times larger than logic gates and cannot be placed anywhere but only in the white space between IC blocks [177]. Li

et al. [178] developed a two-stage TTSV insertion process: the vertical via distribution is solved by an analytical solution and the lateral via distribution is determined with SA-based floorplanning and white space redistribution. However, they underestimated the thermal resistance of μbump interconnections, which is measured to be 10× higher than that of metal vias [179]. Zhao *et al.* [180] adopted the integer multicommodity min-cost network to minimize the wirelength, TTSVs are also considered to reduce the temperature of superheated regions. Previous studies examined the TSV placement optimization with MCNC or GSRC benchmarks such as n100 and ami33 but not multi-threaded benchmarks [5,176,177,180], and the lateral heat transfer of TSVs is not accurately captured [181,182]. In our study, multi-threaded application benchmarks are applied to the system-level simulator and the TTSV placement optimization occurs early in the design phase. We also develop an effective medium theory (EMT)-based model to capture the direction-dependent thermal conductivity of TSVs. Finally, we present a hierarchical floorplanning method based on TTSV placement optimization and multi-level core arrangement algorithms for 3D multi-core processors. The contributions of this chapter are summarized as follows:

1) We conduct full system-level simulations using Gem5 [183] to extract the component activities of Splash-2 benchmarks [184] and calculate the power density of each IC block of a 3D Nehalem-based multicore processor (referred to as 3D Nehalem in the rest of the chapter) [185] using McPAT (Multicore, Power, Area, and Timing) [186]. The critical benchmark (BARNES) with the maximum power density is selected to guide the floorplan optimization process as the worst-case scenario.

2) We develop analytical models based on EMT to capture the lateral and vertical effective thermal conductivities of TSVs with the consideration of the liner layer. The models provide

comparable results to the finite-element method (FEM) without complex meshing and computing processes.

3) We provide a TTSV placement algorithm based on SA, which optimizes area, wirelength, and temperature of the floorplan to effectively address the hotspot issue in 3D ICs. TTSV blocks with the direction-dependent thermal conductivities and varying area overheads are considered during the optimization process.

4) We present a hierarchical approach to generate the floorplan of multi-core 3D ICs, which utilizes an optimized single-core to complete the core layer floorplan based on a symmetric operation and fully takes the advantage of high-thermal-conductivity channels created by TTSVs. The impacts of TTSV area overhead on the peak temperature and wirelength of 3D ICs are discussed in detail.

6.2 System-level Simulation and Power Consumption for the 3D Nehalem

For an accurate thermal analysis of a 3D multi-core processor, the information about the power density for each IC block is required. In this section, we conduct system-level simulation to get the component activities using Gem5 and calculate the power consumption of each IC block using McPAT.

Gem5 is adopted for the component activities, which is an event-driven system simulator with a modular platform for system-level architecture as well as processor microarchitecture research [183]. Splash-2 benchmarks are cross-compiled for the X86 (Nehalem) Instruction Set Architecture (ISA). The full system-level simulation is conducted for each Splash-2 benchmark to extract all the defined component activities, including the number of instructions for both integer

and floating-point units, L1/ L2/ memory reads and writes with hit and miss rates, Network-on-Chip statistics and other related parameters.

Data activity of each IC block along with the system configurations are applied to McPAT, which is an integrated power, area and timing modeling framework for multithreaded, many core and multi-core architectures [186]. The McPAT calculates the dynamic power, static leakage power and short circuit power.

We modify an X86 ISA out-of-order Nehalem processor, which is a family of Intel Architecture (IA) multi-core processors based on a 45 nm technology [185]. Each core has one L1 instruction cache (32 KB), one L1 data cache (32 KB), and one private L2 cache (256 MB). A 16 MB L3 cache is shared between all the cores. The clock frequency is set to 2 GHz, which equals to a 0.5-ns periodicity. The architecture parameters are summarized in Table 6.1.

The 3D Nehalem is used as a platform to demonstrate the performance of our floorplanning algorithm. For newer technology nodes with transistor size smaller than 45 nm, our algorithm could also work because the cooling performance of TTSVs becomes more significant with increasing peak temperature and power density [174]. The 3D Nehalem is composed of two core layers with 4 cores in each layer, one L2 cache layer and one L3 cache layer that share data between threads. Figure 6.1(a) shows all the IC blocks in one core:

1) FP_0: includes the floating-point register file, floating-point units, and complex ALUs and is responsible for divisions and multiplications.

2) Int_0: includes the integer register file, integer units, and integer ALUs and is responsible for integer and logic operations.

3) Icache_0 and D_cache_0: represent the instruction cache and the load/store data cache.

4) Itlb_0 and Dtlb_0: represent the instruction and data translation lookaside buffers.

5) Ifetch_0: is responsible for fetching instructions.

6) Others_0: includes the remaining blocks such as renaming units and Reorder Buffer (ROB).

L2 cache layer contains all L2 caches for eight cores as shown in Figure 6.1(b). The floorplan of the L3 cache is shown in Figure 6.1(c). The core and cache layers are connected through STSVs and electrical μbumps for signal communication. For the 3D Nehalem with TTSVs, the area of L2 and L3 cache layers will be increased correspondingly for geometry matching.

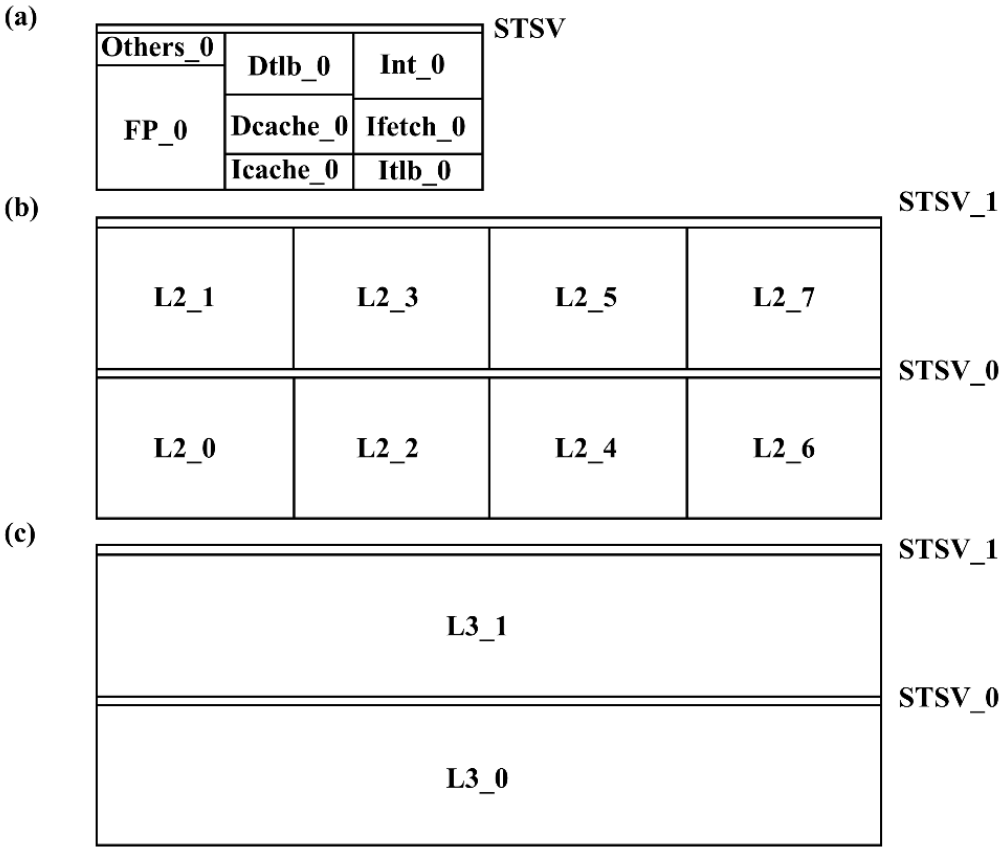

Figure 6.1 (a) IC blocks and STSVs of core 0 out of 8 cores for the 3D Nehalem. (b) The floorplan of the L2 cache. (c) The floorplan of the L3 cache. For the 3D Nehalem with TTSVs, the area of L2 and L3 cache layers is increased for geometry matching.

Table 6.1 Processor parameters

Item	Description
Processor	X86 Nehalem-based 2 GHz processor with 8 cores.
L1 icache	Private, 32 KB, 2-way set associate, 64 B blocks, 4 cycles latency, pseudo Least Recently Used (LRU) replacement.
L1 dcache	Private, 32 KB, 2-way set associate, 64B blocks, 4 cycles latency, pseudo LRU replacement.
L2 cache	Private, 256 KB, 4-way set associatice, 64B blocks, 12 cycles latency, with pseudo LRU replacement.
L3 cache	Shared, 16 MB, 8-way set associative, 64B blocks, 30 cycles latency, with pseudo LRU replacement, MOESI cache coherence.
Main memory	1 GB DRAM.

6.3 Thermal Characterization and Modeling for the 3D Nehalem and TSVs

In this section, we demonstrate the thermal modeling for the 3D Nehalem and analytical models for the effective thermal conductivity of TSV unit cells in the lateral and vertical directions.

6.3.1 Thermal modeling of the 3D Nehalem

The 3D Nehalem is constructed with the "processor-on-top" organization [173]. The two core layers are placed close to the heat sink for cooling purpose and the third and fourth layers are L2 and L3 caches as shown in Figure 6.2. The temperature profiles of the 3D Nehalem with TSVs are simulated using HotSpot [187], which utilizes a circuit-solving technique to solve an RC network of thermal resistances and capacitances by employing the thermal-electrical duality. Each layer is divided into a 64 × 64 grid, which provides sufficiently high simulation accuracy while keeping the computational burden affordable. For example, at 6% TTSV area overhead, the peak temperature of a 64 × 64 grid is less than 0.4% (0.4 °C) times larger compared to that of the 256 ×

256 grid while the simulation time is 143 times shorter (180 s vs. 25740 s). Each cell is modeled with its own power density and thermal properties as shown in Figure 6-2. HotSpot applies an air-cooling boundary condition on the heat sink with a convection resistance of 0.1 KW^{-1} and an ambient temperature of 45 °C.

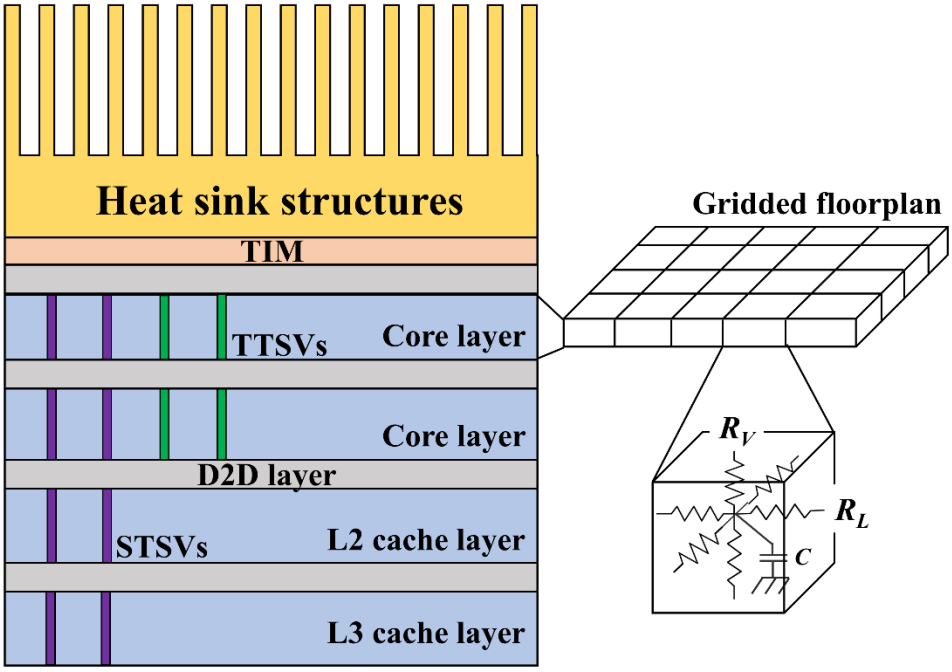

Figure 6.2. Schematic of 3D Nehalem with two core layers, one L2 cache layer and one L3 cache layer. Green and purple blocks represent TTSVs and STSVs, respectively. Thermal interface material (TIM) is used to connect the silicon die with heat sink structures. The grid model is also shown, where each grid cell is modeled with one thermal capacitor (C) and 6 thermal resistors with 4 resistors in the lateral direction (R_L) and 2 resistors in the vertical direction (R_V).

Die-to-Die (D2D) layer (µbump interconnects) and metal layers are used to connect chips while TSVs run across the die. The detailed structures of the D2D layer and the metal layer in the STSV, TTSV, and IC block regions are shown in Figure 6.3(a), (b), and (c), respectively. In the STSV region, we assume the STSVs are manufactured after the device layer but before the metal layer using the via-middle technology and only cross the silicon die [188]. Electrical µbumps are

used to connect STSVs and metal layers to allow inter-die communication. In the TTSV region, we assume TTSVs are manufactured after the metal and device layer using the via-last process and cross both the metal layer and silicon die. Dummy µbumps are used to connect TTSVs in different layers for heat dissipation [173]. The thermal conductivity of the D2D layer under the TSV regions are calculated as $k_{\mu bump} \times \varphi$, where $k_{\mu bump}$ = 40 W·m^{-1}K^{-1} is the thermal conductivity of µbump [189] and φ is the volume fraction of µbumps in the D2D layer, which is assumed to be the same as TSVs (20%). In a TTSV unit cell, the Cu via only have a volume fraction of 20% and the possible routing congestions caused by the TTSVs in the metal layer could be solved by replacing TTSVs with smaller metal vias [190]. In the IC block region, dummy µbumps are used to provide mechanical support for stacking. The D2D layer under IC blocks has a thermal conductivity of 1.5 W·m^{-1}K^{-1} due to the low-thermal-conductivity layers such as SiO_2 or SiN incroporated in the fabrication process as shown in Figure 6.3 [191]. Thermal conductivities and dimensions for the 3D Nehalem components used in simulations are obtained from previous studies and are summarized below in Table 6.2 [154,173,192,193].

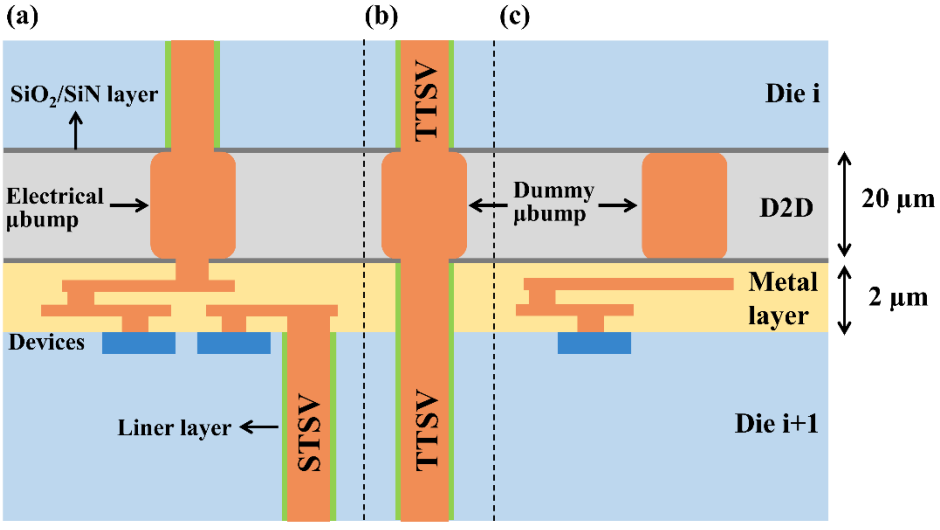

Figure 6.3. The schematics of the silicon die, D2D layer, and the metal layer in (a) STSV, (b) TTSV, and (c) IC block regions, respectively.

Table 6.2 Properties and dimensions of the 3D Nehalem components

Components	Dimensions or thickness	Thermal conductivity ($W \cdot m^{-1}K^{-1}$)
Heat sink	$6.0 \times 6.0 \times 0.7$ cm^3	400
Heat spreader	$3.0 \times 3.0 \times 0.1$ cm^3	400
TIM	20 μm	5
Silicon die	100 μm	100
Metal layer	2 μm	9
D2D under IC block	20 μm	1.5
D2D under TSV	20 μm	8

6.3.2 Analytical models for the TSV unit cell

STSVs are placed in four dies for signal communication. TTSVs are used for heat dissipation, which are placed only in core layers because caches have constrained shape and low power density. The schematic of the TSV block is shown in Figure 6.4(a), whose thermal conductivity is obtained using the TSV unit cell. The pitch size (p) of the TSV is fixed to be 20 μm and the diameter (d) is fixed to be 10 μm [194,195]. The material of metal via is Cu (k_{Cu} = 400 $W \cdot m^{-1}K^{-1}$) and the material of liner is Si_3N_4 (k_{liner} = 30 $W \cdot m^{-1}K^{-1}$), which is used for the isolation purpose with a thickness of 100 nm [196].

The lateral thermal conductivity of TSV has a significant impact on the temperature profiles of 3D ICs [181]. FEM has been applied to capture the effective thermal conductivity of TSV, but the model complexity and computation cost increase with the fine pitch size and small liner thickness. We have developed a modified EMT model, where the impact of liner layer is simplified as the thermal boundary resistance between Cu and Si. $k_{x\ TSV\ unit}$ is the effective lateral thermal conductivity when a heat flow (q_x) is applied to the lateral side of the unit cell as shown in Figure 6.4(b). As the heat goes from left to right of the TSV unit cell, inside the liner layer, the

majority of the isothermal curve is parallel to the liner layer due to its small thickness and low thermal conductivity [182]. So that inside the liner layer, the majority of heat flow is perpendicular to it and its thermal resistance can be represented as:

$$R_{liner} = \int_{d/2}^{d/2+\delta} \frac{dr}{2\pi r h k_{liner}} \tag{6.1}$$

where δ is the liner layer thickness and h is the height of the TSV unit cell. $k_{x\ TSV\ unit}$ can be represented by Hasselman EMT as [99]:

$$k_{x\ TSV\ unit} = k_{Si} \frac{\left(\frac{k_{Cu}}{k_{Si}} - \frac{k_{Cu}}{R_c^{-1} r} - 1\right)\varphi + 1 + \frac{k_{Cu}}{R_c^{-1} r} + \frac{k_{Cu}}{k_{Si}}}{\left(-\frac{k_{Cu}}{k_{Si}} \frac{k_{Cu}}{R_c^{-1} r} + 1\right)\varphi + 1 + \frac{k_{Cu}}{R_c^{-1} r} + \frac{k_{Cu}}{k_{Si}}} \tag{6.2}$$

where k_{Si} and k_{Cu} are the thermal conductivities of the Si substrate and Cu via. φ is the volume fraction of Cu via. R_c is the thermal boundary resistance that is equivalent to $\pi d h R_{liner}$. When a heat flow (q_z) is applied at the bottom of the TSV unit cell as shown in Figure 6.4(c), the vertical effective thermal conductivity is calculated as:

$$k_{z\ TSV\ unit} = k_{Si}(1 - \varphi - \phi) + k_{Cu}\varphi + k_{Si_3N_4}\phi \tag{6.3}$$

where $\phi$is the volume fraction of the liner layer. The lateral and vertical thermal conductivities of TSV unit cell with varying TSV diameters are shown in Figure 6.4(d). The analytical solutions fit well with the FEM simulations. The lateral thermal conductivity is much smaller compared to that of the vertical direction. Simply using the vertical thermal conductivity of TSV for both lateral and vertical directions will overestimate its cooling performance in reducing the peak temperature.

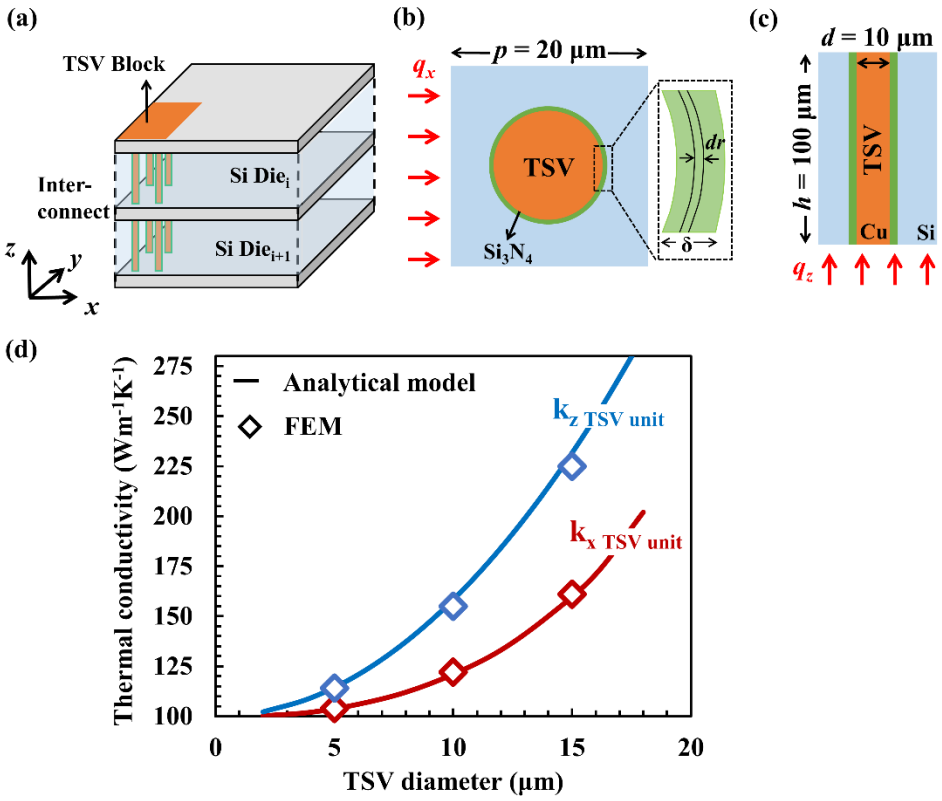

Figure 6.4 (a) Schematic of the TSV block. (b) Schematic of the *xy*-plane view of the TSV unit cell. (c) Schematic of the *xz*-plane view of the TSV unit cell. (d) The effective lateral and vertical thermal conductivities of the TSV unit cell with varying dimensions. The solid lines represent the analytical solutions and diamonds represent the FEM results. Blue and red colors represent vertical and lateral directions, respectively.

6.4 TTSV Placement Optimization and Hierarchical Floorplanning for the 3D Nehalem

In this section, we explain the optimization flow and algorithms for multipurpose floorplan optimization and hierarchical floorplanning. Our optimization is at floorplan level and we assume that every IC block is fully optimized, and the placement and routing of standard cells are done. Since the TTSVs are placed between IC blocks, it will not affect the standard cells inside the IC

block. The heat generated by the IC blocks can be dissipated through TSV blocks that are placed close to them.

6.4.1 Optimization flow

The objective of this floorplan optimization method is to maximize the heat conduction of TTSV while simultaneously minimizing their negative impacts on wirelength and area. The whole optimization flow is shown in Figure 6.5. The simulation flow is performed to optimize the floorplan of a single core and generate the corresponding 3D ICs with a fixed area of IC blocks and TTSV area overhead *i* ($i = A_{TSV}/A_{IC\ blocks}$, 1% TTSV area overhead contains 280 TTSVs). During the one-core optimization, the number of TTSV blocks in one core is *n* (4, 8, 16). Each TTSV block has a fixed area of A_{TSV}/n and an aspect ratio ranging from 1 to 8. The maximum TTSV block number, *N*, is bound of the simulation. If *N* is too small, each TTSV block will be too large and has restricted arrangement. If *N* is too large, the search space and computation cost of SA will be extended significantly. We assume *N* = 16 for our simulation efforts. After the one-core optimization and the hierarchical floorplanning, the optimal 3D IC is chosen with the minimum cost of the normalized area ($\frac{A_{x\%-TTSV}}{A_{no-TTSV}}$), wirelength ($\frac{WL_{x\%-TTSV}}{WL_{no-TTSV}}$) and peak temperature ($\frac{T_{x\%-TTSV}}{T_{no-TTSV}}$), where $A_{x\%-TTSV}$, $WL_{x\%-TTSV}$, and $T_{x\%-TTSV}$ are the area, wirelength and peak temperature at *x*% TTSV area overhead, and $A_{no-TTSV}$, $WL_{no-TTSV}$, and $T_{no-TTSV}$ are the area, wirelength, and peak temperature of the optimized no-TTSV case. The weight factors for the normalized area, wirelength, and peak temperature are set to be 1 to find the optimal 3D IC design at each TTSV area overhead, which could be changed depending on the area of interest.

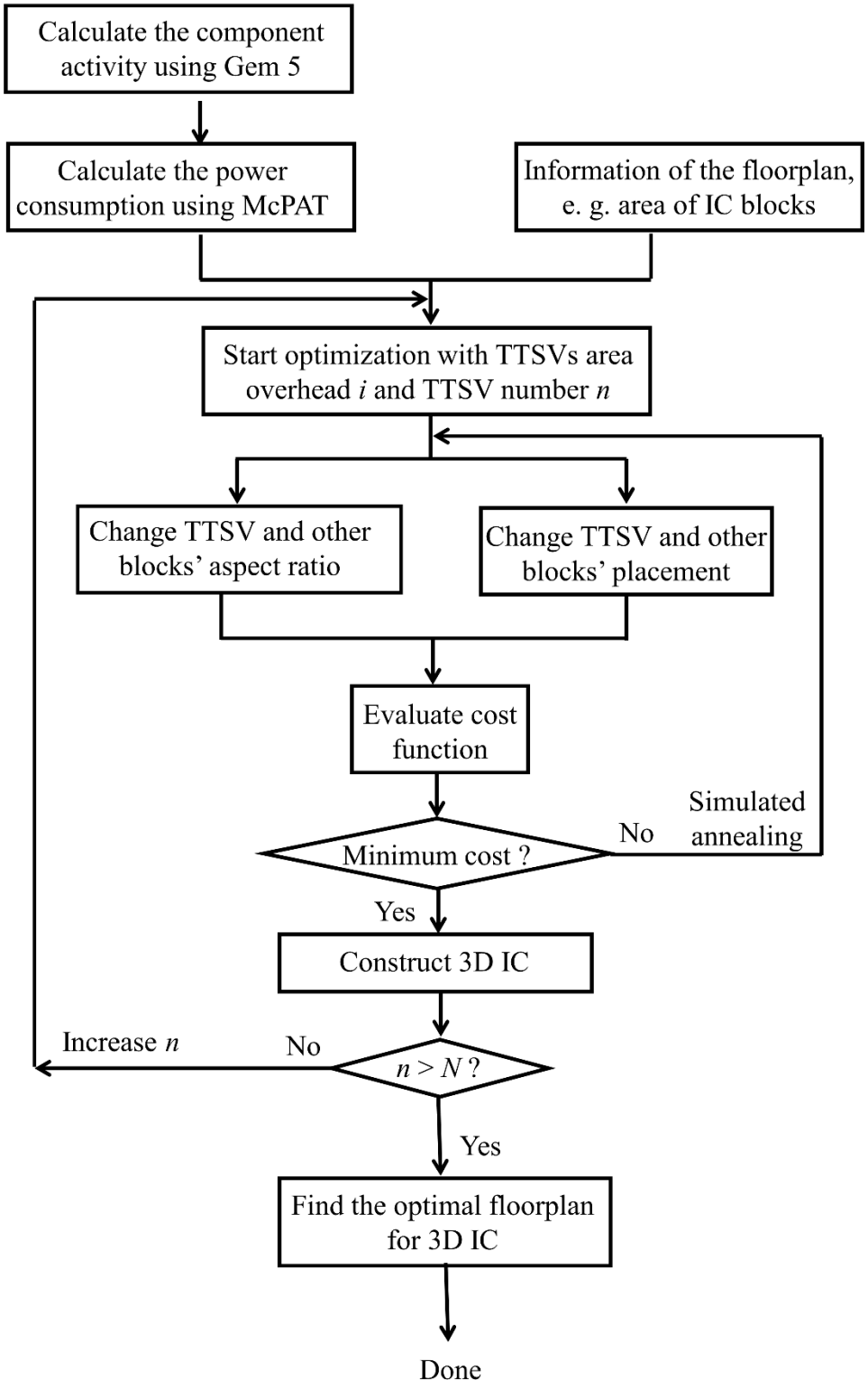

Figure 6.5 The floorplan optimization flow for 3D Nehalem.

6.4.2 Problem formation for floorplan optimization

The goal is to find an efficient solution for the TTSV placement early in the design process and optimize the total area, wirelength, and peak temperature. Our assumptions for this work are: a floorplan (*flp*) consisting of:

- m blocks $B_{0:m-1}$, namely, B_0, B_1 … B_{m-1}. Each block has its associated area $A_{0:m-1}$, namely, A_0, A_1 … A_{m-1} with a restricted acceptable minimum and maximum aspect ratio.
- n TTSV blocks $TTSV_{0:n-1}$, namely, $TTSV_0$, $TTSV_1$ … $TTSVn_{-1}$. Similarly, each block has its associated area, $TTSVA_{0:n-1}$, namely, $TTSVA_0$, $TTSVA_1$ … $TTSVA_{n-1}$ with restricted acceptable minimum and maximum aspect ratios.
- Vector A, representing the area of all blocks, is the concatenation of $A_{0:m-1}$ and $TTSVA_{0:n-1}$.
    - Wire density matrix WD of size $m \times m$, $WD = \begin{pmatrix} 0 & w_{0,1} & \dots & w_{0,m-1} \\ w_{1,0} & 0 & \dots & w_{1,m-1} \\ \dots & w_{i,j} & w_{i,i} & \dots \\ w_{m-1,0} & w_{m-1,1} & \dots & w_{m-1,m-1} \end{pmatrix}$, and Manhattan distance matrix L of size $m \times m$, $L = \begin{pmatrix} 0 & l_{0,1} & \dots & l_{0,m-1} \\ l_{1,0} & 0 & \dots & l_{1,m-1} \\ \dots & l_{i,j} & l_{i,i} & \dots \\ l_{m-1,0} & l_{m-1,1} & \dots & l_{m-1,m-1} \end{pmatrix}$ between blocks B_i and $B_j \in B_{0:m-1}$ $\forall i, j \in [0, m-1]$.

Our algorithm calculates the following:

- IC block activities, which represent the number of instructions executed in all functional blocks, the number of all reads and writes in cache units are calculated using Gem5.
- Power consumption for each block B_0, B_1 … B_m, which is estimated and stored in P containing P_0, P_1, … P_m, using McPAT.

- The peak temperature of each block, which is generated using HotSpot and stored in T represented as: $T_0, T_1, \ldots, T_{(n-1)+(m-1)}$.

  The objective function is represented by:

$$Optimal\_flp(B_{0:m-1}, TTSV_{0:n-1}, A, WL, P)$$

subjects to a cost function:

$$F_{cost} = \alpha \cdot A + \beta \cdot WL + \gamma \cdot T \tag{6.4}$$

where α, β and γ are weight factors with units of m^{-2}, $m^{-1,}$ and K^{-1}, respectively. A is the total area of the floorplan, WL is the wirelength, and T is the peak temperature, respectively. During the one-core optimization process with TTSV area overhead ranging from 0% to 10%, α is assigned to be 5×10^6 m^{-2} so that $\alpha \cdot A$ ranges from 180 ~ 200. β is assigned to be 25 m^{-1} so that $\beta \cdot WL$ ranges from 7 ~ 11. γ is assigned to be 2 K^{-1} so that $\gamma \cdot T$ ranges from 669 ~ 673. We put relatively more weight on the peak temperature over other factors in the cost function to address the thermal management issues in 3D ICs. Different weight factors could also be applied to different scenarios. WL is added to limit the negative impact of TTSV on the performance, which is defined as [197]:

$$WL = \frac{1}{2}\sum_{i=0}^{m-1}\sum_{j=0}^{m-1} w_{ij}\, l_{ij} \tag{6.5}$$

where w_{ij} and l_{ij} are the wire density (Table 6.3) and Manhattan distance between different IC blocks.

The corresponding 3D structure is created using $Create\_3D\_structure(flp_{best})$, where flp_{best} is the best floorplan generated by $Optimal\_flp()$ with all IC blocks represented by their width, height, and position in the floorplan as an (x, y) pair.

Table 6.3 Wire density for different IC blocks

From	to	Wire density	From	to	Wire density
Int	FP	1	Icache	Itlb	4
Int	Icache	4	Icache	Dtlb	1
Int	Dachce	4	Icache	Ifetch	3
Int	Itlb	2	Icache	Others	1
Int	Dtlb	2	Dcache	Itlb	1
Int	Ifetch	2	Dcache	Dtlb	4
Int	Others	1	Dcache	Ifetch	1
FP	Icache	1	Dcache	Others	1
FP	Dcache	4	Itlb	Dtlb	1
FP	Itlb	1	Itlb	Ifetch	1
FP	Dtlb	1	Itlb	Others	1
FP	Ifetch	1	Dtlb	Ifetch	1
FP	Others	1	Dtlb	Others	1
Icache	Dcache	1	Ifetch	Others	1

6.4.3 Simulated annealing-based optimization algorithm

The SA-based floorplan optimization algorithm is $Optimal\_flp$, which is used to optimize the block placement for a single core. The output of the optimized floorplan is fed to the multi-core arrangement algorithm, $Create\_3D\_structure$, to construct the 3D ICs. Algorithm 1 ($Optimal\_flp$) accepts the floorplan description including processor parameters (see Table 6.1) as an input, and generates the optimized floorplan based on SA, flp_{best}. Line 1 denotes all the Gem5 generated activities in set $B_{0:m-1}$, which are fed to McPAT to estimate the static and dynamic power consumption (stored in P) on Line 2. Lines 3-24 comprehensively describe the SA process with parameter values and expressions listed in Table 6.4. On Line 3, we populate an initial floorplan in flp_c using the normalized polish expression, $12*3*\cdots m$, which corresponds to placing the m blocks horizontally next to each other [198]. With the initial floorplan defined, the power trace is applied to each block to calculate its F_{cost} shown on Line 4. Lines 5-6 set flp_{best}, $cost_{best}$ and the

annealing temperature, T, to their initial values. The annealing process stopping condition is reaching either the maximum number of allowable steps, 3000, or the cooling limit restricted by T_{cold} as shown in line 7. Lines 8-11 present that the number of block movements initialized on Line 8, governs the generation of the random floorplan, flp_{new}, on Line 10.

The new floorplan, flp_{new}, is produced for testing, if the calculated cost, $cost_{new}$, on Line 11 is moving downhill in the optimization curve or has been tried twice the total amount of the block movements. If the new generated floorplan cost, $cost_{new}$, is less than the current one, then the cost function downhill movement section, which is represented by Lines 12 -15, stores the best floorplan so far in flp_{best} with its associated $cost_{best}$. Otherwise current floorplan is given a chance with acceptance likelihood of the Boltzmann probability function $e^{-\frac{cost_{new}-cost_c}{T}}$ in the uphill movement from Lines 16-19 or it will be rejected on Line 20. If at any time the ratio of rejection, R_{reject}, is not satisfied, the annealing process for the current iteration is terminated on Line 22. The best floorplan stored at flp_{best} is returned on Line 24.

ALGORITHM 1. $Optimal\_flp$: SA- Based Floorplan Optimization Algorithm

Input: *flp* description explained in problem formulation and processor parameter (e.g. Table 6.1).
Output: the best optimized floorplan using SA, $flp_{best.}$

1. *Activities*=Generate activities using Gem5 with processor parameter in Table 6.1;
2. *P* = Generate power traces using McPAT;
   //initializations
3. flp_c = Initialize_flp();
4. $\$cost_c\$ = F_{cost}$ (flp_c, *P*, *α*, *β*, *γ*); //Eq. (4)
5. $flp_{best} = flp_c$, $cost_{best} = cost_c$;
6. $T = T_{initial}$;//SA
7. **for** $s=0$; $T>=T_{cold}$ *and* $s<Steps_{max}$; s++;
8. $Mvs= Mv * (m+n)$, $Downs =0$, $Rejects = 0$;
9. **for** $q =0$; $q<2*Mvs$ **and** $Downs<Mvs$; q++;
10. $flp_{new} = make\_random\_move(flp_c)$;
11. $cost_{new} = F_{cost} (flp_{new}, P, \alpha, \beta, \gamma)$;
    // SA downhill movement
12. **if** $cost_{new} < cost_c$ **then** *downs++;*
13. **if** $cost_{new} < cost_{best}$ **then**
14. $flp_{best} = flp_c$, $cost_{best} = cost_{new}$;
    end if
15. $flp_c = flp_{new}$, $cost_c = cost_{new}$;
    // SA uphill movement
16. **else if** pseudo-*rand()* $< e^{-\frac{cost_{new}-cost_c}{T}}$ **then**
17. **if** $cost_{new} < cost_{best}$ **then**
18. $flp_{best} = flp_c$, $cost_{best} = cost_{new}$;
    end if
19. $flp_c = flp_{new}$, $cost_c = cost_{new}$;
20. **else** *Rejects++;*
    end if
21. **end for** // for each try *q*
22. **If** $\frac{Rejects}{Tries} > Rreject$ **then break**
    end if
23. $T = T * R_{cool}$;
    end for // for each *s*
24. **return** flp_{best};

Table 6.4 Simulated annealing parameters

Symbol	DESCRIPTION	Value/expression
$Steps_{max}$	Maximum number of iterations	3000
P_0	Initial probability	0.99
D_{avg}	Average change in the cost function	1
$Rreject$	Rejection ratio to stop annealing	0.99
$Rcool$	Ratio of annealing cooling schedule	0.99557
flp_c, flp_{best}	Current floorplan, Best floorplan	
flp_{new}	New floorplan	
$cost_{c,}\ cost_{best}$	Current cost, Best cost	
$cost_{new}$	New cost	
Mv	No. of block moves per step	15
Mvs	All block movements	$Mv * m$
$T_{initial}$	Initial annealing temperature	$-\frac{D_{avg}}{\log(P_0)}$
T	Current annealing temperature	
T_{cold}	Cooling temperature	$\frac{D_{avg}}{\log(\frac{1-Rreject}{2})}$
ΔF_{Cost}	$F_{cost\_new} - F_{cost\_old}$	

6.4.4 Multilevel core arrangement for the 3D Nehalem

Algorithm 2 ($Create\_3D\_structure$) receives the output of the Algorithm 1, flp_{best}, as core 0 and its final output is the constructed multi-core 3D IC. Algorithm 2 has four parts, the first part identifies the position of the peak temperature region (critical hotspot) within core 0 on Line 1, which will be in one of the four possible positions shown in Figure 6-6(a). When there are multiple IC blocks with the same peak temperature, each of them can be treated as the critical hotspot to generate the corresponding 3D IC. Among them, the 3D IC with the minimum peak temperature will be the optimal design.

The second part transforms the core 0 orientation to position 1 to separate hotspots, which are the black dots in Figure 6.6(a). To change core 0 orientation, let (x_{c0}, y_{c0}) denote the left bottom edge of core 0. If it is already in position 1, no additional step is needed (Lines 2-3). Lines 4-6, shown in Figure 6.6(b), check if core 0 is in position 2. If true, then core 0 is flipped along the *x* axis by changing (x_{c0}, y_{c0}) to (x_{c0}, $-y_{c0}$), and shifted up by adding the core 0 height (h) to the y axis as (x_{c0}, $-y_{c0}+h$). Lines 7-9 are shown in Figure 6.6(c). If core 0 is in position 3, it is flipped along the *y* axis by changing (x_{c0}, y_{c0}) to ($-x_{c0}$, y_{c0}), then shifted right by adding the core 0 width (w) to the *x* axis as ($x_{c0}+w$, y_{c0}). For Lines 10-14, if core 0 is in position 4, the combined actions of positions 2 and 3 are performed (Figure 6.6(d)) by flipping along the *x* axis and shifting up, then flipping along the *y* axis and shifting right, and (x_{c0}, y_{c0}) becomes ($-x_{c0}+w$, $-y_{c0}+h$).

The third part constructs the 2D layer as shown in Figure 6.6(e) and Lines 15-20, by duplicating core 0, flipping it along the *x* axis and adding its height twice, (x_{c1}, y_{c1}) is changed to (x_{c1}, $-y_{c1}+2*h$). After generating (*core 0, core 1*) pair, the pair is duplicated, flipped along the *y* axis, and then shifted right twice to generate the layer with 4 cores (*core 0*, *core 1*, *core 2*, and *core 3*).

In the fourth and last part (Line 21), the 3D structure is generated by copying and stacking (*core 0*, *core 1*, *core 2*, and *core 3*) to (*core 4*, *core 5*, *core 6*, and *core 7*) to take the advantage of high thermal conductivity channels created by TTSVs and dummy µbumps. (see Figure 6.6(f)). After generating the core layers, heat sinks and cache layers are added to complete the 3D IC.

ALGORITHM 2. *Create_3D_structure*- Multi-level Core Arrangement Algorithm

Input: the best optimized floorplan using SA, flp_{best} (i.e. *core 0* in Figure 6.6(a)).

Output: 3D structure of four cores in one layer and another four cores in another layer.

1. *position* = find the core quarter containing the maximum temperature block; //Figure 6.6(a)
   //position the maximum temperature blocks in the bottom left corner on *core 0*
2. **if** *position == 1* **then**
3. //do nothing
4. **else if** *position == 2* **then** //Figure 6.6(b) i
5. flip *core 0* along *x* axis; //Figure 6.6(b) ii
6. shift *core 0* up by its height; //Figure 6.6(b) iii
7. **else if** *position == 3* **then** // Figure 6.6(c) i
8. flip *core 0* along *y* axis; // Figure 6.6(c) ii
9. shift *core 0* right by its width; // Figure 6.6(c) iii
10. **else** // *position == 4* // Figure 6.6(d) i
11. flip *core 0* along *x* axis; // Figure 6.6(d) ii
12. shift *core 0* up by its height; // Figure 6.6(d) iii
13. flip *core 0* along *y* axis; // Figure 6.6(d) v
14. shift *core 0* up by its width; // Figure 6.6(d) vi

    end if
    //construct a 2D layer with 4 cores
15. copy *core 0* to a new *core 1*;
16. flip *core 1* along *x* axis; // Figure 6.6(e) ii
17. shift *core 1* up by its height ×2;
18. copy (*core 0, core 1*) to a new (*core 2, core 3*);
19. flip (*core 2, core 3*) along *y* axis; // Figure 6.6(e) iv
20. shift (*core 2, core 3*) up by its width ×2;
    //construct a 2D layer with 4 cores
21. *3D_structure* = copy (*core 0, core 1, core2, core 3*) to a new layer (*core 4, core 5, core6, core 7*);
22. **return** *3D_structure*;

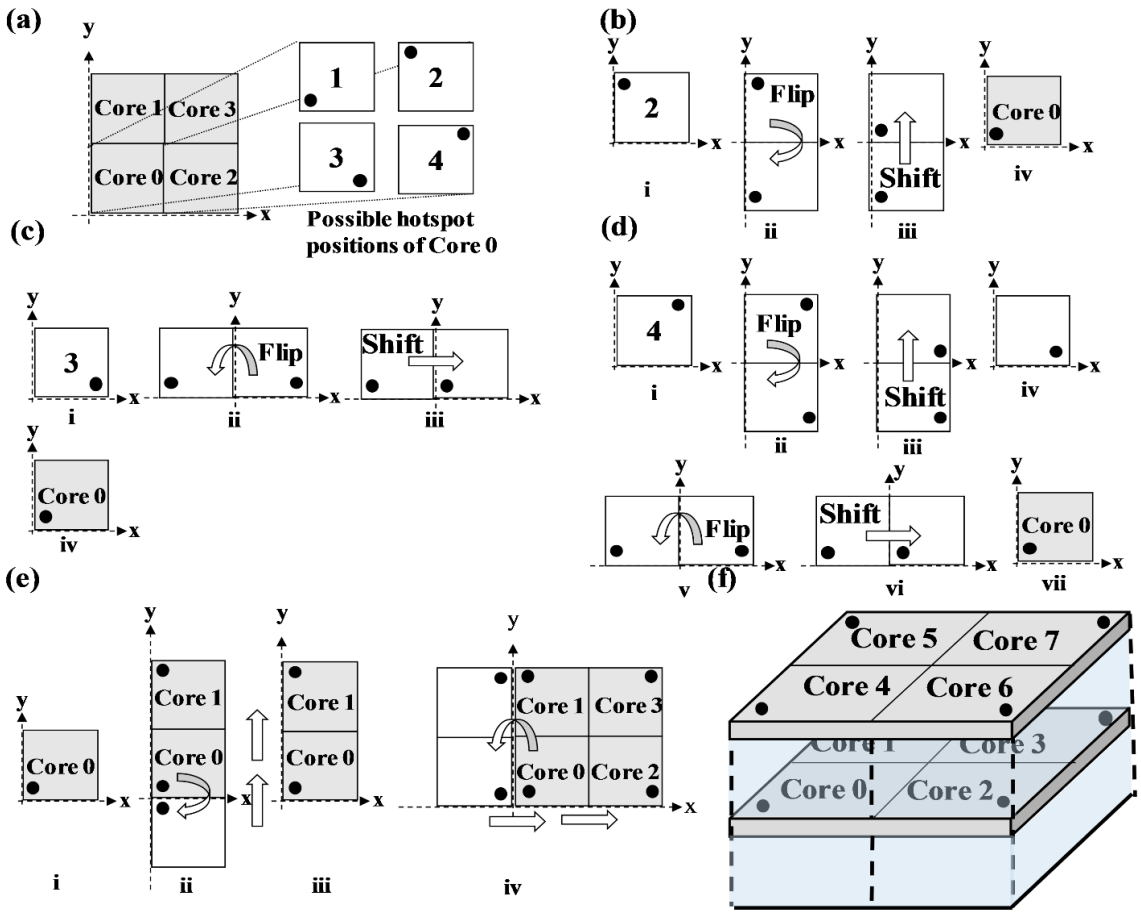

Figure 6.6. (a) Four cores in the *x*, *y* coordinates with all possible maximum temperature block ($B_{T_{max}}$) positions of core 0. (b) Operations required to transform $B_{T_{max}}$ from position 2 to 1. (c) Operations required to transform $B_{T_{max}}$ from position 3 to 1. (d) Operations required to transform $B_{T_{max}}$ from position 4 to 1. (e) Operations required to create 2D with four cores: core 0, 1, 2 and 3. (f) The resulted 3D structure (only core layers are shown).

6.5 Results and Discussion

In this section, the power densities of the 3D Nehalem running Splash-2 benchmarks are presented and the effectiveness of our TTSV placement method is evaluated. The impacts of TTSV on the area, wirelength, and peak temperature of multi-core 3D ICs are studied in detail.

6.5.1 Power density of the 3D Nehalem running Splash-2 benchmarks

Power consumptions of Spalsh-2 benchmarks are extracted from McPAT based on the component activities obtained from Gem5 [199]. Figure 6.7 shows the power density of each IC block in one core. Among all the benchmarks, BARNES has the maximum power density that even exceeds 500 $W \cdot cm^{-2}$. Among all the IC blocks, Itlb has the maximum power density for most of the benchmarks making it the critical hotspot in the 3D ICs. TTSVs are placed close to Itlb during the optimization process to facilitate heat removal, so the optimal floorplan with TTSV will provide effective cooling to most of the benchmarks as well. In the following simulations, BARNES is used to guide the floorplan optimization with different TTSV overheads. The optimal floorplan is adopted to calculate the peak temperatures of all Splash-2 benchmarks to evaluate its performance.

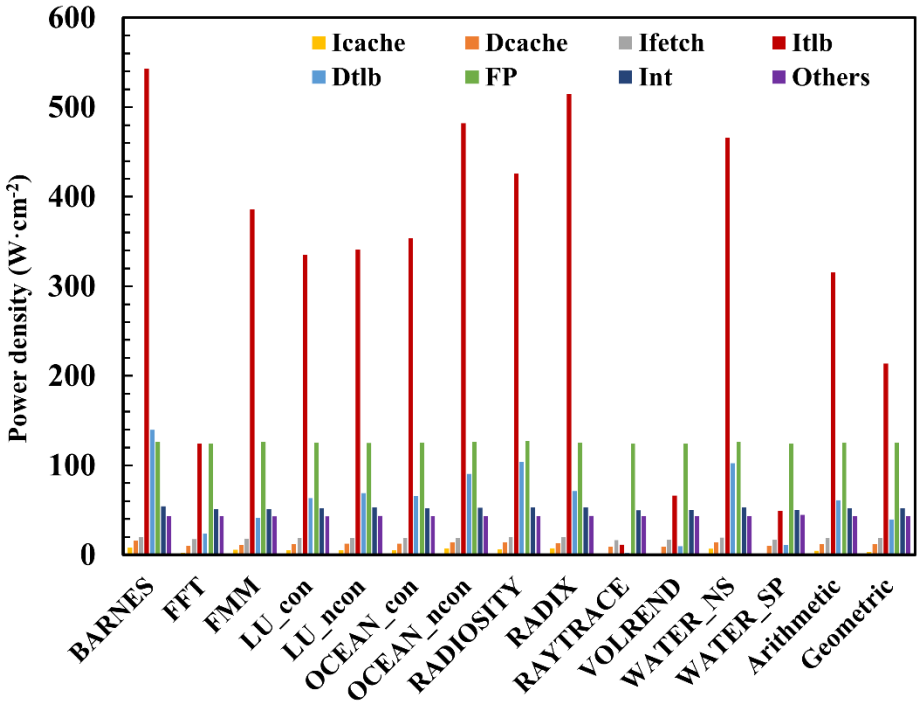

Figure 6.7. The power densities for Splash-2 benchmarks for all the IC blocks in one core of the 3D Nehalem.

6.5.2 Trade-off in area, wirelength, and peak temperature

In the simulated annealing, the cost function considers area, wirelength, and peak temperature. Using the floorplan with 8 TTSV blocks and 6% TTSV area overhead as an example. The convergence processes of all the objective values and the total cost are shown in Figure 6.8. The objectives of all the variables have a decreasing tend with iteration steps and the total cost decreases with the iteration steps until the maximum allowable step is reached. For the 3D IC, the chip area, wirelength, and peak temperature are shown in Figure 6.9 with peak temperature as the primary *y* axis and wirelength or chip area as the secondary *y* axis. The chip area increases with TTSV area overhead, which is composed of the area of TTSV and white space. The wirelength strongly depends on the placement of TTSV while the peak temperature reduces consistently with TTSV area overhead. The impact of TTSVs on the wirelength and peak temperature are discussed in next sections.

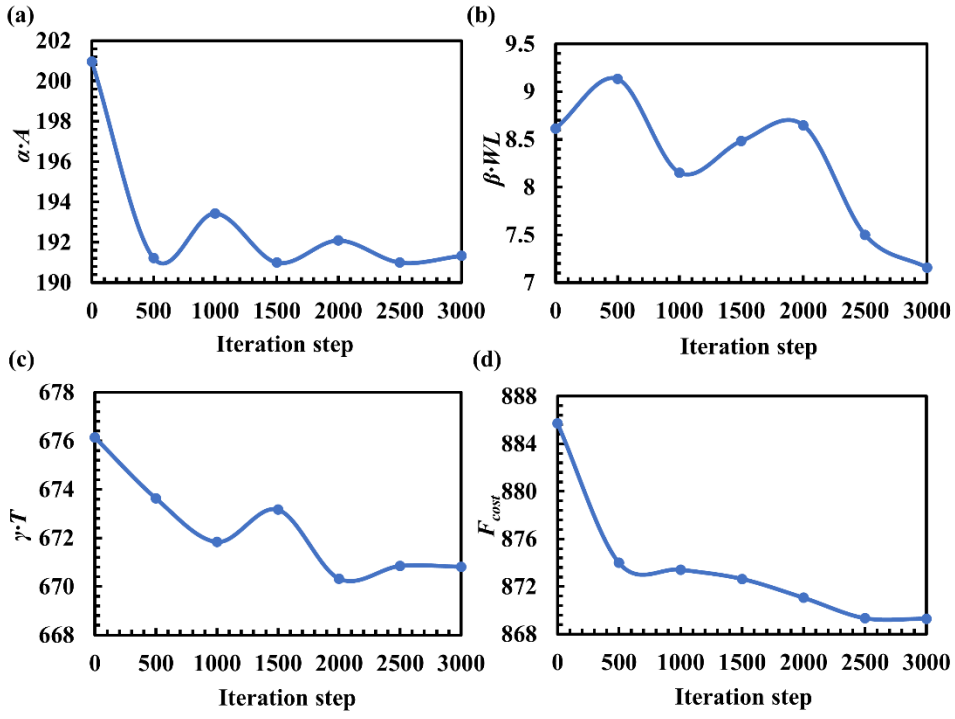

Figure 6.8 The convergence processes for (a) area, (b) wirelength, (c) peak temperatuer, and (d) total cost in the simulated annealing. The 3D Nehalem with 8 TTSV blocks and 6% area overhead is used as an example.

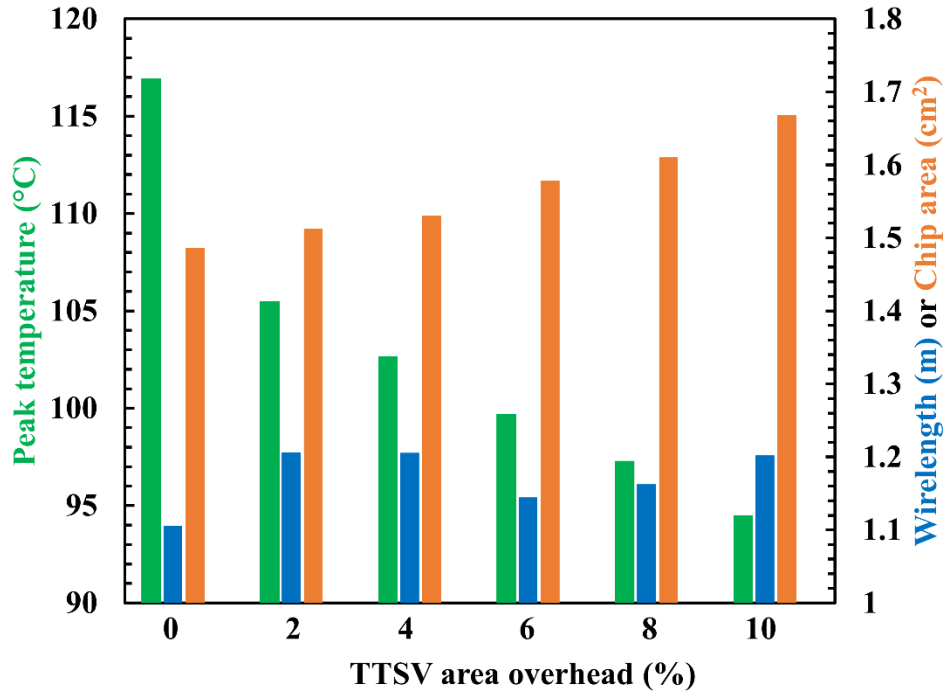

Figure 6.9 The total chip area, wirelength, and peak temperature change with different TTSV area overheads of the 3D Nehalem.

6.5.3 Impact of TTSVs on wirelength of the 3D Nehalem

The floorplan without TTSV has the minimum wirelength as no TTSV/white space between IC blocks. The wirelength increase of the TTSV-incorporated 3D Nehalem is compared to the no-TTSV case. Figure 6.10(a) shows that as the TTSV area overhead increases, the wirelength increases first, and then decreases until 6% overhead. After that, the wirelength increases again. The change of wirelength is strongly dependent on the TTSV placement.

The SA-optimized single-core floorplan at 0% TTSV area overhead is shown in Figure 6.10(b), where the hotspot, Itlb, is surrounded by other IC blocks inside the core. As the TTSV area overhead increases, TTSVs are placed around Itlb for heat dissipation, which increase the wirelength by enlarging the distance between IC blocks. The schematic of the optimized floorplan at 2% TTSV area overhead is shown in Figure 6.10(c). Wirelength decreases at 6% TTSV area overhead and the corresponding floorplan is shown in Figure 6.10(d), where Itlb is moved to the corner of the core. Part of the TTSVs is located at the core edge, which facilitates heat removal without increasing the wirelength. Finally, as the TTSV area overhead increases, the wirelength starts to increase due to the increased area of TTSVs placed between Itlb and other IC blocks. The schematic of the optimized floorplan at 10% TTSV area overhead is shown in Figure 6.10(e).

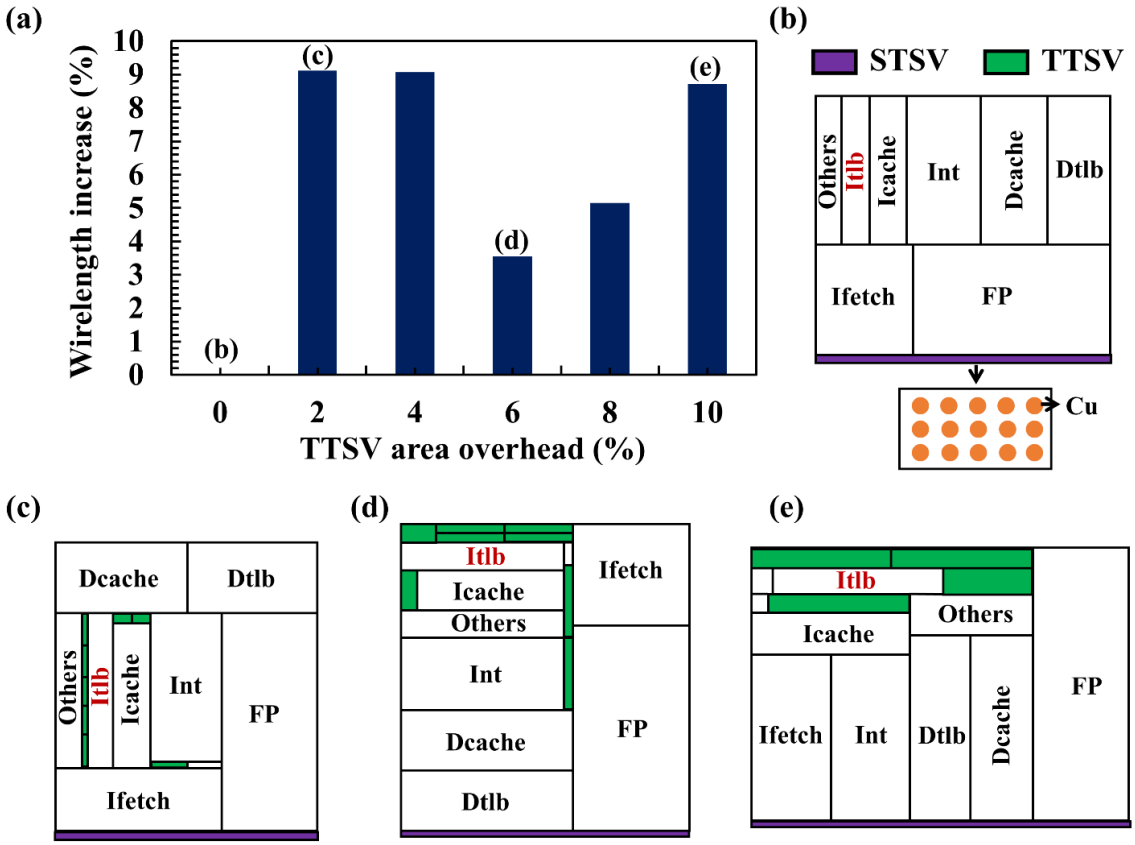

Figure 6.10 (a) The wirelength increases with different TTSV area overheads. The wirelength of the no-TTSV case is considered as 1 to normalize the wirelength. (b), (c), (d), and (e) are the optimal floorplan at 0%, 2%, 6%, and 10 % TTSV area overheads. Itlb block is highlighted in red, the green, purple, and white blocks indicate the TTSV, STSV, and white space, respectively. The zoom-in schematic of the TSV with Cu vias is also shown.

6.5.4 Impact of TTSVs on the peak temperature of the 3D Nehalem

To evaluate the cooling performance of our algorithm, the peak temperatures of TTSV-integrated 3D Nehalem with/without TTSVs placement optimization are compared as shown in Figure 6.11(a). Based on the floorplan shown in Figure 6.10(b), TTSVs are added between cores as the non-optimized or fixed TTSV arrangement (Figure 6.11(b)). For different TTSV area overheads, the width of TTSV blocks (*t*) will be increased with the same arrangement. By using our floorplanning method, TTSVs can be optimally placed around hotspots to facilitate heat dissipation as the floorplans shown in Figure 6.10(c), (d), and (e) at 2%, 6%, and 10% TTSV area overheads.

Figure 6-11(a) shows the peak temperatures of the non-optimized and optimized TTSV arrangement cases at different TTSV area overheads running the BARNES benchmark. With the TTSV placement optimization, peak temperatures of the optimized floorplans are much lower than that of the non-optimized case. When the TTSV area overhead is at 2%, the peak temperature reduction is 11.4 °C (9.8%) for the optimized case, providing the maximum temperature reduction per 1% TTSV area overhead. The substantial temperature change is caused by the sudden reduction in power density and thermal resistance around Itlb (TTSVs consume zero power and create high-thermal-conductivity channels around hotspot). When the TTSV area overhead is at 10%, the peak temperature reduction is 22.4 °C (19%) for the optimized case while the peak temperature reduction is only 1.7 °C (1.4%) for the non-optimized case. Compared to the fixed

TTSV placement, our floorplan optimization method can effectively address the hotspot issue in multi-core 3D ICs.

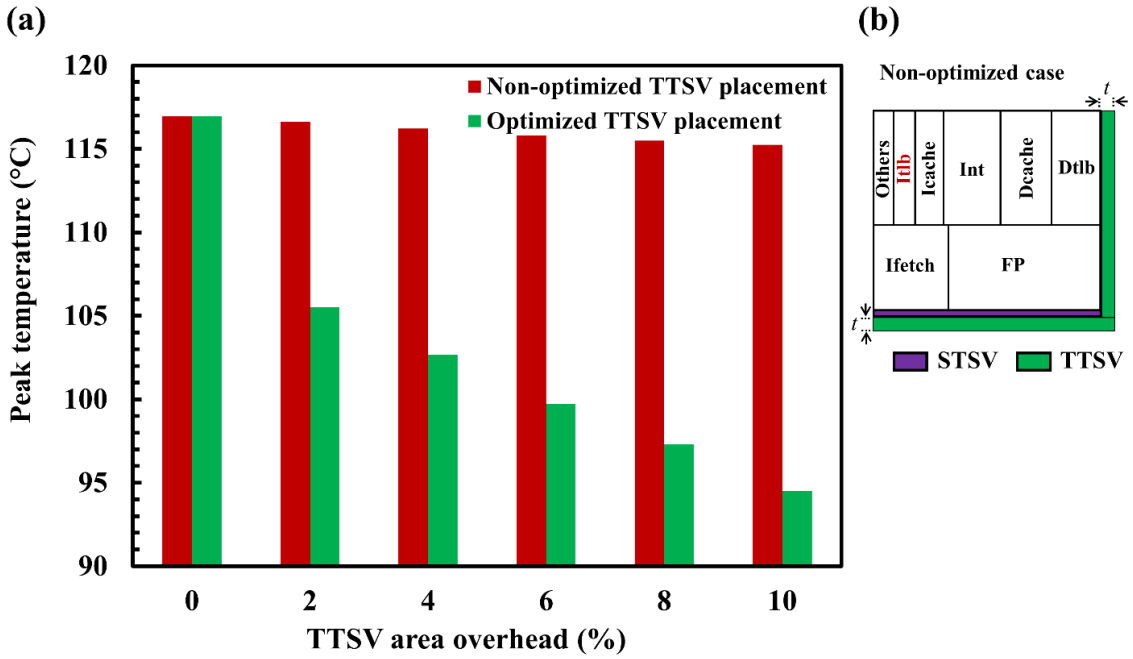

Figure 6.11 (a) The peak temperature changes for the 3D Nehalem with and without TTSV placement optimization running BARNES benchmark. The peak temperature of the 3D Nehalem is reduced with the increase of TTSV area overhead. (b) The floorplan of the non-optimized TTSV placement, the TTSV block width (*t*) will increase with larger TTSV area overhead.

The peak temperature decreases with the TTSV area overhead and the wirelength has a small value at 6% TTSV area overhead as discussed in the previous section, which leads to an optimal floorplan at 6% TTSV area overhead that has the minimum cost in terms of the normalized area, wirelength, and peak temperature along all other area overheads. As shown in Figure 6.2, the second core layer presents the maximum on-chip temperature because of its high power density and large thermal resistance to the heat sink. The corresponding core layer temperature profiles with/without TTSV placement optimization at 6% TTSV overhead are compared in Figure 6.12(a) and (b) with the same temperature legend. With the same TTSV area overhead, the peak

temperatures of the 3D Nehalem with TTSV placement optimization are 16 °C lower compared to that of the non-optimized TTSV arrangement. Apart from Itlb, temperatures of other IC blocks are close, which means that the optimally arranged TTSVs can provide localized cooling to hotspots. The temperature profiles of the entire 3D Nehalem are shown in Figure 6.12(c) and (d) with the non-optimized and optimized TTSV arrangement, respectively. By optimizing the TTSV placement inside the core layers, the peak temperatures of the core layers are reduced as well as the temperatures of L2 and L3 cache layers, which means that placing TTSVs only in the core layer can effectively cool the entire 3D ICs including the cache layers. Optimizing the TTSV placement does not directly optimize the temperature uniformity in the heat sink when the cost function is defined to minimize the peak temperature. As the peak temperature of the 3D IC decreases by using TTSVs, the change in the peak temperature and temperature uniformity in the heat sink is negligible, which is mainly because of its large volume and high thermal conductivity. For example, the peak temperature of the heat sink decreases from 69.0 °C to 68.4 °C and 68.4 °C by using 6% TTSV with and without placement optimization and the temperature uniformities are all approximately 1.0 °C (the temperature uniformity is defined as $\sqrt{\frac{\sum_{i=1}^{N}(T_i-\bar{T})^2}{N-1}}$, where N is the grid size, i is the grid number, T_i is the temperature of each gird, and $\bar{T}$ is the average temperature of all the grids in the heat sink). While the goal of our current optimization is to find a solution with the minimum peak temperature, wirelength and area overhead, the algorithm can be readily extended to consider other aspects such as temperature uniformity and provide optimal solutions to meet varying demands of circuit designers and device engineers.

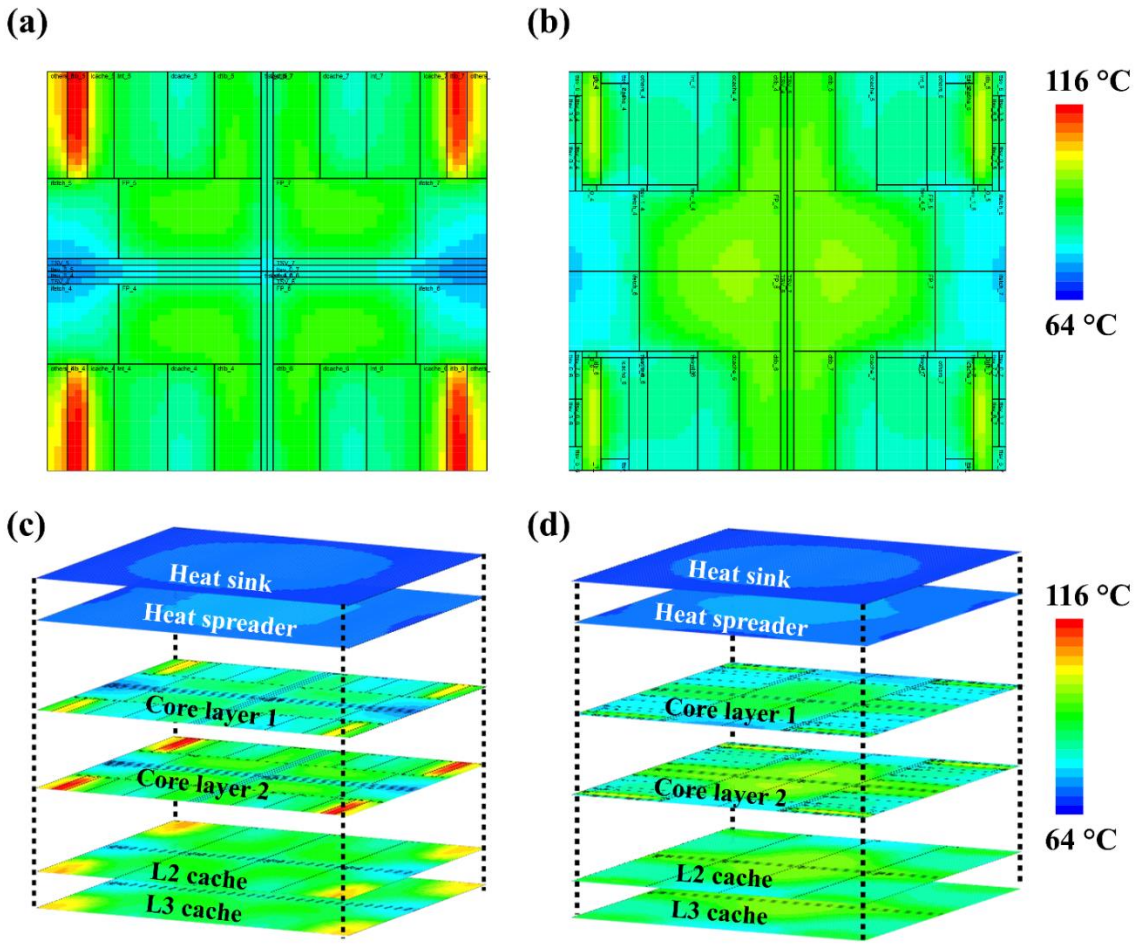

Figure 6.12 (a) and (b) are the temperature profiles of the second core layer of the 3D Nehalem for the non-optimized and optimized TTSV arrangement at 6% TTSV area overhead. (c) and (d) are the corresponding temperature profiles of the entire 3D Nehalem, the D2D layers are hidden for clarity.

Using BARNES benchmark to guide the floorplan. optimization shows significant peak temperature reduction. To further evaluate it, we conduct simulations running other Splash-2 benchmarks with the same floorplan. The peak temperature comparison is shown in Figure 6.12. The peak temperature of Splash-2 benchmarks that is larger than 100 °C has been substantially reduced. BARNES benchmark has the maximum temperature reduction of 16.9 °C and other benchmarks have temperature reductions ranged from 11.2 °C to 15.5 °C, indicating that the

optimized floorplans based on BARNES are also effective for other Splash-2 benchmarks. Some benchmarks have increased peak temperature that is mainly caused by different power distribution. However, those benchmarks' maximum power density and peak temperatures are much lower compared to that of the BARNES. Moreover, the peak temperature increase is less than 2 °C, which can be considered as negligible. In general, the optimal floorplan is thermally advantageous. An average peak temperature reduction of 5 °C can be achieved for all the Splash-2 benchmarks as shown by the arithmetic and geometric means in Figure 6.13.

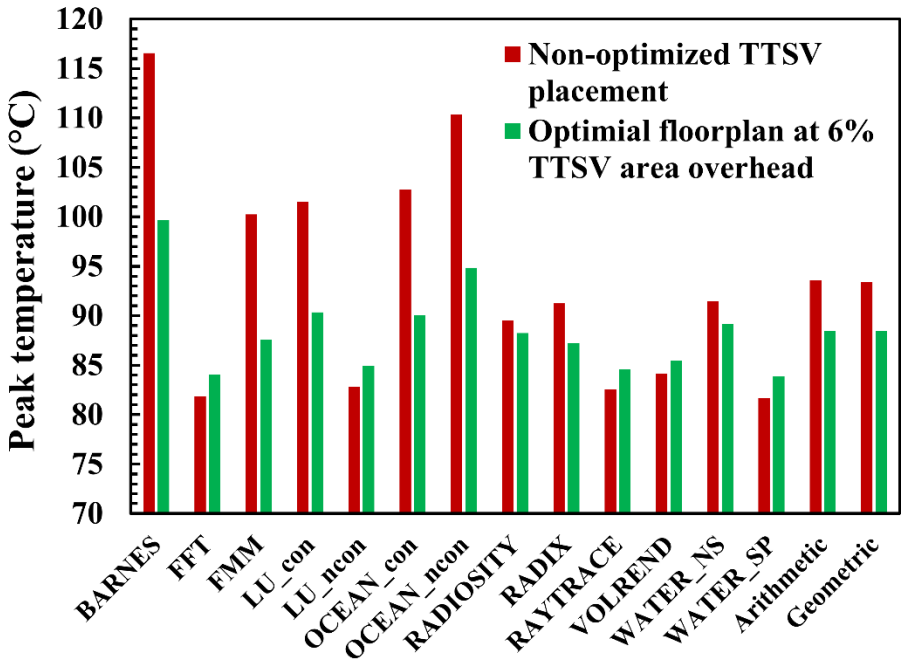

Figure 6.13. Peak temperatures for the 3D Nehalem without the TTSVs placement optimization and the optimal floorplan at 6% TTSV area overhead running Spalsh-2 benchmark. The arithmetic and the geometric means are also shown in the figure.

6.6 Conclusions

This chapter demonstrates a hierarchical floorplanning approach for 3D multicore processors, which address the trade-off in peak temperature, wirelength and area of the floorplan through a SA-based TTSV placement optimization algorithm. Our simulation results show that the optimally arranged TTSVs effectively reduce the peak temperature with moderate overheads in wirelength and area. The peak temperature decreases consistently with the TTSV area overhead while the wirelength change is strongly related to the TTSV placement, which is uniquely optimized with different TTSV area overheads. Depending on the TTSV placement and area overhead, an optimal floorplan can be found in terms of peak temperature, wirelength and area and is applicable to most of the Splash-2 benchmarks without further modification. The presented method can provide a potential thermal management solution to 3D multi-core ICs and effectively address the multi-purpose floorplanning problem.

Chapter 7: Conclusions and Suggestions

7.1 Summary

This dissertation describes active and passive cooling solutions for the thermal management of hot spots with heat fluxes of 1 $kW \cdot cm^{-2}$ or higher. Holey silicon-based thermoelectric cooling devices are developed for on-chip hot spots that are in the length of tens or hundreds of micrometers. Thermal through silicon via placement optimization algorithm is developed for "hot" IC blocks to address the trade-off between thermal and electrical performance of 3D ICs.

Silicon nanostructures with vertically etched holes, or holey silicon, uniquely provide the low thermal conductivity in the in-plane direction due to the substantial phonon boundary scattering, and high thermal conductivity in the cross-plane direction due to the persistent long wavelength phonons. This anisotropy is ideal for lateral thermoelectric cooling devices for hot spot management as the low in-plane thermal conductivity sustains the necessary temperature gradient for the Peltier junctions, and the high cross-plane thermal conductivity effectively dissipates heat from the hot spot to the on-chip cooling system. Our numerical simulations demonstrate that the thermoelectric cooling effectiveness of holey silicon is at least 30% greater than that of the high-thermal-conductivity bulk silicon and 400% greater than that of low-thermal-conductivity chalcogenides (chapter 2).

The cooling performance of the holey silicon-based TEC can be further enhanced by integrating the Peltier cooler with a TSV like structure that directly draws heat from the hot spot to combine active and passive cooling strategies. Our simulations show that the TSV-integrated TEC can reduce the hot spot temperature from 154 °C to 68 °C while dissipating a heat flux of 1

$kW \cdot cm^{-2}$ and consuming 0.5 W for operation. The on-state and off-state hot spot temperatures are 67 °C and 24 °C lower than that of the same TEC with no TSV, respectively. The thermal conductivity anisotropy of the holey silicon substrate can be further improved by metal inclusions. The on-state and off-state TEC performance can be adjusted depending on the metal-silicon interfacial resistance (chapter 3).

The transient performance of the holey silicon-based TEC is also explored by studying the temporal and spatial interplays of the Peltier, Joule, and Thomson effects. Our simulations show that a supercooling effect can be achieved by using a current pulse, which is driven by the Peltier cooling before the Joule heating diffuses in, and the thermal conductivity anisotropy is favorable by delaying the diffusion in the in-plane direction while allowing rapid heat dissipation in the vertical direction. A holey silicon-based TEC with a 1 $kW \cdot cm^{-2}$ hot spot shows temperature reductions from 117 to 102 °C in steady-state and temporarily to 100 °C with optimal pulse conditions. The transient performance can be further improved by incorporating phase change materials within holey silicon, in which their melting process delays the temperature overshoot (chapter 4).

The fabrication and measurement of the holey silicon-based TEC using a special SOI-like wafer are demonstrated. The cooling performance of the holey silicon-based TEC is measured at different background temperatures and time scales. The holey silicon-based TEC provides 1.2 °C temperature reduction at 100 °C background temperature, and the temperature reduction can be increased to 1.5 °C at 150 °C background temperature. The holey silicon-based TEC provides more temperature reduction than that of the bulk Si-based TEC and the cooling performance can be further improved with increased etching ratio or decreased neck size. The transient supercooling of the holey silicon-based TEC is also demonstrated, which temporarily provides more temperature

reduction than that can be achieved under steady-state. With a square-shaped current pulse of $2I_{s\text{-}s}$ amplitude and 2s duration, the cooler temperature reduction can be temporarily increased to 1.56 ℃ at 100 ℃ background temperature. The supercooling temperature reduction can be increased by increasing the current pulse amplitude, and the supercooling period can be extended by increasing the current pulse duration (Chapter 5).

3D integration technology based on interlayer connections and through silicon vias offers many advantages over 2D ICs, however, its thermal management challenges remain unresolved. In chapter 6, we have demonstrated a hierarchical approach to optimize the floorplan of a 3D Nehalem-based multicore processor to address the trade-off between peak temperature, wirelength, and die area. Our simulations show an increase in the thermal TSV area accompanies a decrease in peak temperature, but the wirelength strongly depends on the thermal TSV placement, which is uniquely optimized for each case of the allowed thermal TSV area. Compared to the floorplan with a fixed thermal TSV placement, our algorithm optimally places thermal TSVs between cores. An optimal floorplan is found at 6% thermal TSV area overhead, in which the peak temperature is reduced from 116 to 100 ℃ with only a 3.5% increase in wirelength (Chapter 6).

7.2 Suggestions for Future Works

Thermal management of electronic hot spots has received great attention as the advances in device miniaturization, design complexity, and 3D integration. My doctoral research has developed active and passive hot spot thermal management solutions based on holey silicon thermoelectric micro-coolers and thermal through silicon via placement optimization. My research has improved the understanding of the role of anisotropy in thermoelectric cooling systems, and

the trade-off between thermal and electrical performance of 3D ICs. However, there is still a lot to learn and to be explored to further improve the hot spot cooling performance.

7.2.1 Holey silicon-based thermoelectric cooler for dynamic hot spots

In chapter 4, we have discussed the transient supercooling of the holey silicon-based TEC for a constant heat flux hot spot to provide a general understanding of its transient performance. However, hot spots may have transient profiles in many high-power systems, and the applied current pulse could be further optimized based on the specific hot spot profile for the best cooling performance. Here, we present preliminary simulations to show the effectiveness of transient supercooling on the thermal management of a dynamic hot spot. Figure 7.1 shows the profile of a dynamic hot spot that changes from 1 kW·cm^{-2} to 2 kW·cm^{-2} with a 2 ms duration. A constant current ($I_{s\text{-}s}$) and a triangular-shaped current pulse with 5 ms duration are applied to the Peltier cooler. Figure 7.2 shows the transient hot spot temperature change. By applying a triangular-shaped current pulse, the hot spot temperature is lower compared to that of the case with a constant current. The performance can be further optimized by studying the impacts of different current pulse profiles, amplitudes, durations, and the starting time of the pulse.

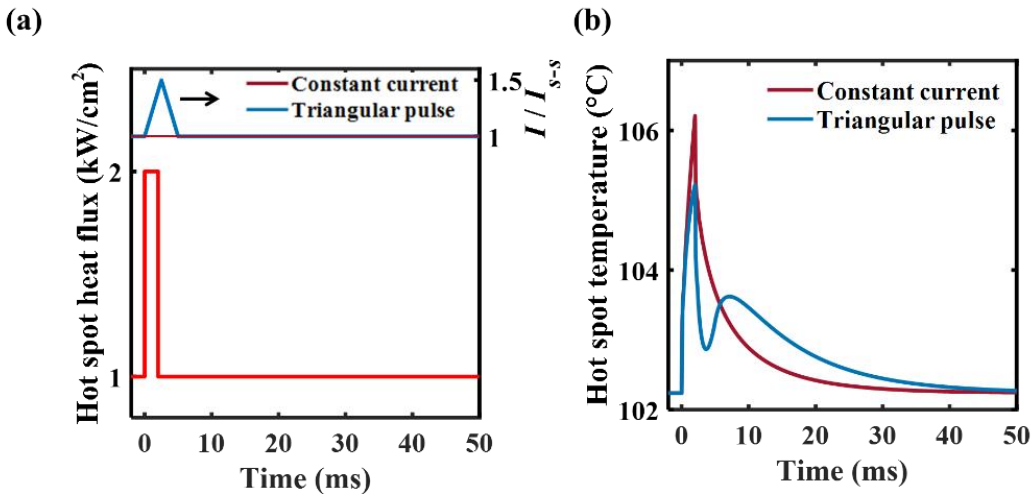

Figure 7.1 (a) Profiles of a dynamic hot spot and applied currents. The hot spot heat flux is changed from 1 kW·cm^{-2} to 2 kW·cm^{-2} with a 2 ms duration. A constant current and a triangular-shaped current pulse with 5 ms duration and 1.5$I_{s\text{-}s}$ amplitude are applied to the Peltier cooler, respectively. (b) The hot spot temperature change with a constant current and a triangular-shaped current pulse.

7.2.2 Experimental demonstration of holey silicon-based TEC for hot spot cooling

In chapter 5, we have presented the experimental demonstration of the holey silicon-based TEC and measured the cooler temperature reduction with varying background temperatures. As discussed in chapter 5, the testing of the holey silicon-based micro-cooler is performed by supplying current to the cooler and ground electrode through wire bonding and measuring the temperature distribution through an IR camera. An emissivity coating is used to cover the whole device, which increases the accuracy of IR measurement. The hot spot cooling ability of the holey silicon-based TEC could be tested with a laser radiation created local hot spot. The hot spot heat flux can be controlled by adjusting the output power of the laser [200]. Figure 7.2(a) shows the schematic of the potential test setup. The transient supercooling on the hot spot could also be tested with the same setup.

Another method is to use the Joule heating generated by the metal trace as hot spot heat. The ground electrode design would be the same as the holey silicon-based TEC while the cooler design needs to be modified to be compatible with the metal trace. Figure 7.2(b) shows the top-down image in the cooler area. The blue pattern indicates the SiO_2 layer that acts as the insulator for the metal trace. The metal trace has a zigzag structure that increases the electrical resistance for Joule heating generation. The metal traces are extended to the edge of the holey silicon-based TEC for wire bonding. The shape of the Peltier cooler is modified to surround the metal trace to provide localized cooling. The holey silicon area is shown by the green color.

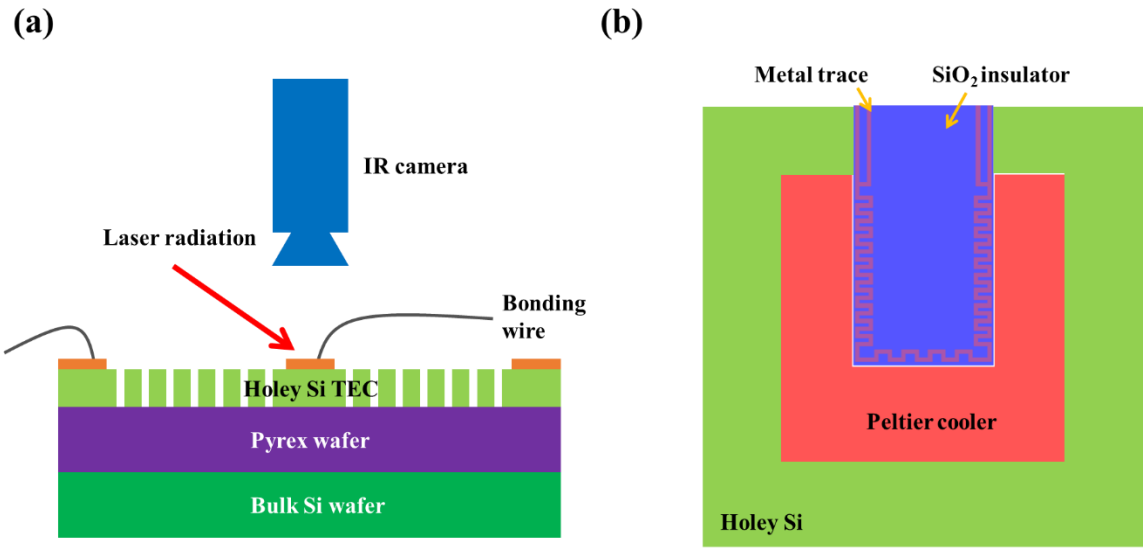

Figure 7.2 (a) Test setup to use laser radiation as the local hot spot. (b) Top-down schematic at the cooler area to use the Joule heating generated by a metal trace as the hot spot.

7.2.3 Signal-ground TSV pair optimization

In chapter 6, we have discussed the thermal TSV placement optimization algorithm that addresses the trade-off between the peak temperature, wirelength, and die area for the 3D IC floorplanning. Signal TSVs are used for electrical communication between dies and are also made with high-thermal-conductivity metals that can be used for heat dissipation. The trade-off between thermal and electrical performance of signal TSVs and the co-optimization of thermal and signal TSV design need to be explored.

A simple one-dimensional thermal model is constructed for the thermal analysis. We assume the 3D IC has 8 dies, and each die has a power generation of 2W. Every die is composed of a silicon substrate, the back-end-of-line (BEOL) layer, and a bonding layer. The material properties and structure dimensions used for the thermal analysis are listed in Table 7.1. For the thermal performance, the peak temperature reduces as the decrease of TSV pitch size because the metal via has higher thermal conductivity than silicon.

Table 7.1 Material properties and structure dimensions for the 3D IC

	k (W/m/K)	Thickness (um)
Si die	100	40
Bonding	0.15	10
BEOL	1.5	20
TSV	400	40

Electromagnetic simulations are performed using Ansys's high-frequency structure simulator (HFSS) for the signal-ground (S-G) TSV pair. Figure 7.3(a) shows the simulation domain of the S-G TSV pair. The transparent box is the air box that has a dimension of 600×600×150 μm^3 and has the radiation boundary condition. The green box is the silicon box that as a dimension of 400×400×50 μm^3. Lumped ports are applied to the orange and blue cylinders, which are signal and ground TSVs, respectively. Figure 7.3(b) shows a zoom-in image of the S-G TSV pair, a 0.1 μm thick SiO_2 layer is added to the TSV as the liner. *h* and *p* are the TSV height and pitch, respectively. For the electrical performance, the insertion loss increases as the decrease of pitch size, which is caused by the increase of coupling capacitance. A cost function is defined to find the optimal TSV design:

$$cost = aT_{normalized} + bS21_{normalized} \tag{7.1}$$

where *a* and *b* are the weight factors for thermal and electrical performance, and we assume that *a* = *b* = 1. $\boldsymbol{T_{normalized}} = \frac{\boldsymbol{T-T_{min}}}{\boldsymbol{T_{max}-T_{min}}}$ is the normalized peak temperature and $\boldsymbol{S21_{normalized}} = \frac{\boldsymbol{S21-S21_{max}}}{\boldsymbol{S21_{min}-S21_{max}}}$ is the normalized insertion loss, which is obtained using HFSS. Figure 7.3(c) shows the change of the normalized temperature and insertion loss with the pitch size and figure 7.3(d)

shows that an optimal pitch size can be found to provide the minimum cost. Further study could be performed with more detailed thermal and electrical models for the S-G TSV pair optimization.

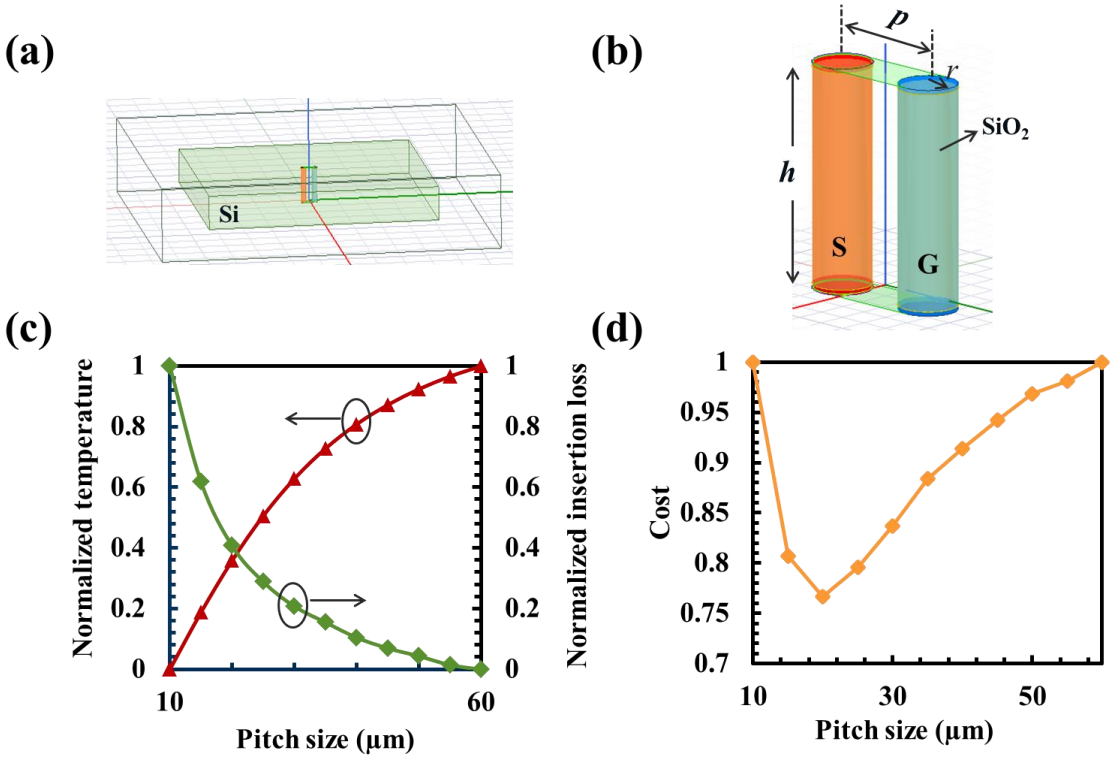

Figure 7.3 (a) Simulation domain of the S-G TSV pair. (b) Zoom-in image of the S-G TSV pair. (c) Normalized temperature and insertion loss change with pitch size for the S-G TSV pair. (d) Cost change with pitch size.

7.2.4 Coaxial TSV optimization

Coaxial TSV is the best TSV configuration in electrical performance that has a central signal-carrying via (S) surrounded by a concentric ground return (G) as shown in Figure 7.4(a) [201]. Dielectric materials, such as SiO_2 are filled between the S-G pair. h, r_d, r, and t_g are the TSV height, dielectric radius, conductor radius, and ground thickness, respectively. In our simulations, r_d is ranged from 5 to 10 μm, and h is ranged from 30 to 100 μm. r and t_g are fixed at 3 μm and 1 μm, respectively. Figure 7.4 (b) shows the insertion loss comparison between the coaxial TSV and

the S-G TSV pair with the same TSV height and via radius. The coaxial TSV provides much lower insertion loss up to 10 GHz. Increasing the dielectric radius decreases the insertion loss due to the reduced coupling capacitance but increases the peak temperature due to the increased thermal resistance as shown in Figure 7(c). An optimal radius could be found that provides the minimum cost. A more detailed analysis could be performed for the coaxial TSV optimization.

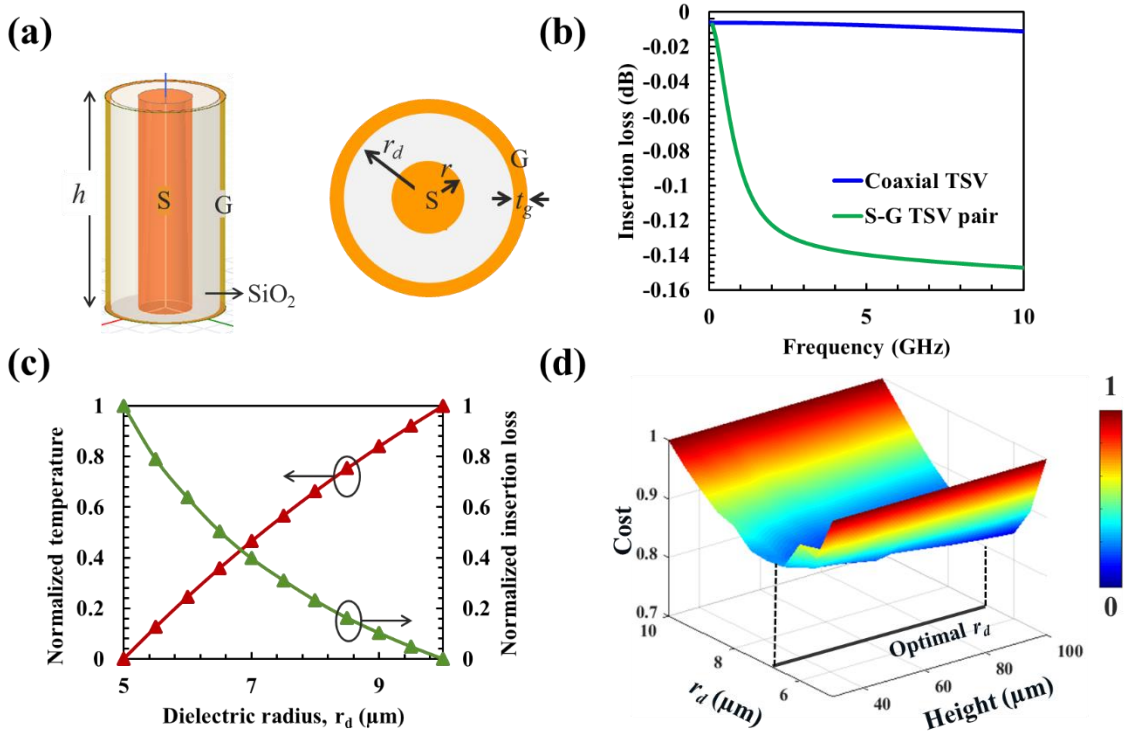

Figure 7.4 (a) Schematic of the coaxial TSV. (b) Insertion loss comparison between the coaxial TSV and S-G TSV pair. (c) Normalized temperature and insertion loss change for coaxial TSV with different dielectric radius. (d) Cost change of the coaxial TSV with different dielectric radius and heights.

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Appendix A: Microfabrication Recipes of Holey Silicon-based TEC

Fabrication process flow:

1. Fabrication of the SOI-like wafer

- Pyrex wafer double-side polishing
- 500 μm thick Pyrex and 500 μm thick silicon wafer anodic bonding
- Silicon grind to 25 μm and polishing the surface
- Anodic wafer bonding of another 500 μm silicon wafer with the other side of the Pyrex wafer

2. Lithography for metal electrodes

- Wafer clean with DI water, Acetone, methanol, and Isopropyl Alcohol
- Wafer dry with nitrogen air
- Dehydration bake 5 minutes in a 90 °C oven
- Apply Shipley 1827 photoresist (spin 10s at 500 rpm and 30s at 3000 rpm)
- Soft bake 30 minute in a 90 °C oven
- Expose with Karl Suss MA6 mask aligner (low vacuum, 24s)
- Develop using MF-319 (1 minute with slight agitation)
- Risen with DI wafer for 1 minute followed by nitrogen blow dry

3. Metal deposition using Temescal CV-8 e-beam evaporator

- Wafer rinse in buffered oxide etch for 1 minute to remove native oxide layer
- Pump down the chamber (1×10^{-6} torr)
- Deposit 20 nm Ti (0.4 $Å\cdot s^{-1}$)
- Deposit 300 nm Ag (0.4 $Å\cdot s^{-1}$ for first 20 nm and 1 $Å\cdot s^{-1}$ for the rest)

- Put in acetone for 12 hours for lift-off (sonication if necessary)

4. Dry etching

- Lithography process is the same as for metal deposition with one extra alignment process
- Hard bake in a 90 °C oven for 30 minutes
- Bosch process to etch through the wafer (rate: 3-4 $\mu m \cdot min^{-1}$)

5. Wafer dicing using ADT dicing 7910

- Apply photoresist for protection (30s at 500 rpm)
- Hard bake in a 90 °C oven for 30 minutes
- Cutting speed: 1 $mm \cdot s^{-1}$
- Depth from the chuck up: 0.02 mm