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A Resonant 1:5 Cockcroft-Walton Converter Utilizing GaN FET Switches with N-Phase and Split-Phase Clocking

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Abstract—Recent demonstrations of merged inductor-capacitor (LC) switching converters have resulted in record power densities being achieved at high voltage conversion ratios. To do so, sophisticated switch control schemes may be required. This work demonstrates N-phase and Split-phase switching techniques applied to a resonant Cockcroft-Walton converter. For the same hardware, the lower resonant switching frequency of the N-phase scheme significantly improves light-load efficiency relative to the Split-phase scheme. However, the N-phase approach suffers reverse body diode turn-on at large voltage ripple contributing to the Split-phase scheme obtaining the highest power density. Converter performance combining both switching techniques is analyzed using a discrete 1:5 Cockcroft-Walton converter implemented using gallium nitride FETs, multi-layer ceramic chip (MLCC) capacitors, and a 68 nH inductor. The resulting converter achieves a peak efficiency of 94.9% and 94% for the N-phase and Split-phase schemes respectively with the N-phase scheme seeing a 30% reduction in losses at light-load. The converter achieves a maximum output power of 190W, resulting in a record power density of 483.3 kW/liter (7,920 W/inch³) and specific power of 243 kW/kg.

I. INTRODUCTION

Hybrid inductor-capacitor (LC) switching converters are known to be capable of achieving high power densities due to their efficient utilization of passive component energy density and elimination of transient inrush currents which typically incur significant loss in conventional switched-capacitor converters [1-7]. Resonant and soft-charged hybrid-LC converters may employ zero-current switching (ZCS) and zero-voltage switching (ZVS) to significantly improve efficiency relative to hard-charged purely capacitive converters, although some topologies lend themselves more easily to hybridization than others [8]. To enable additional converter topologies that benefit from hybrid resonant or soft-charged action, asynchronous near-ZVS can be employed using the natural response of diodes, as in [9-11], or more complex active switching regimes must be implemented. This work focuses on two advanced active switching strategies applied to a fixed-ratio resonant hybrid-LC topology. Specifically, the Cockcroft-Walton (CW) is selected (Fig. 1) due to its reduced switch and capacitor voltage stress as compared with other switched-capacitor (SC) topologies [12].

This paper presents three primary contributions. First, a comparison of two recently published switching schemes, N-

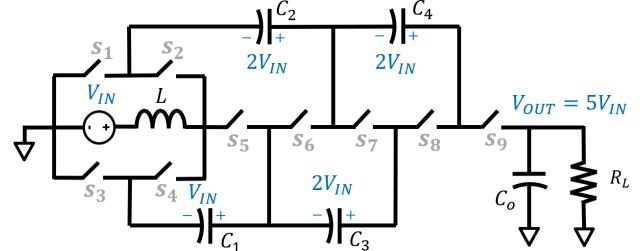


Fig. 1. An example inductively loaded hybrid-LC 1:5 Cockcroft-Walton converter with average light-load voltage stress across fly capacitors labeled.

phase switching [12] and Split-phase switching [13], is presented and demonstrates the advantages of each. It is found that for the same hardware the N-phase scheme is more light-load efficient, whereas the Split-phase scheme excels at heavy loads. Second, this work is the first demonstration of active Split-phase clocking applied to a CW converter, having previously only been demonstrated with the Dickson topology [5,13,14]. Third, the use of gallium nitride FETs and new high-density isolated level-shift and gate driver integrated circuits results in a record-breaking ([7,15-17]) power density of 483.3 kW/liter (7,920 W/inch³) at a high conversion ratio, excluding only the volume of the low voltage clock generation circuitry, which is expected to consume negligible volume in a commercial implementation.

Section II describes the N-phase and Split-phase techniques before detailing the tradeoffs of each and how they might be implemented as part of a unified solution. Section III presents the discrete prototype and measured results before Sections IV and V conclude with a comparison to previously published converters and a brief summary.

II. THEORY OF OPERATION

A. N-Phase Switching

Fig. 2 depicts the phase progression for an N-phase clocking scheme applied to a 1:N hybrid-LC CW converter, where N=5. Each phase contains a series RLC circuit and, in resonant operation, each phase terminates once the inductor current has returned to 0A. Since there is only ever one active voltage loop that includes the inductor, all switches experience ZCS. As discussed in [12], the same current sensing hardware, placed in series with the inductor, can be reused for all N phases,

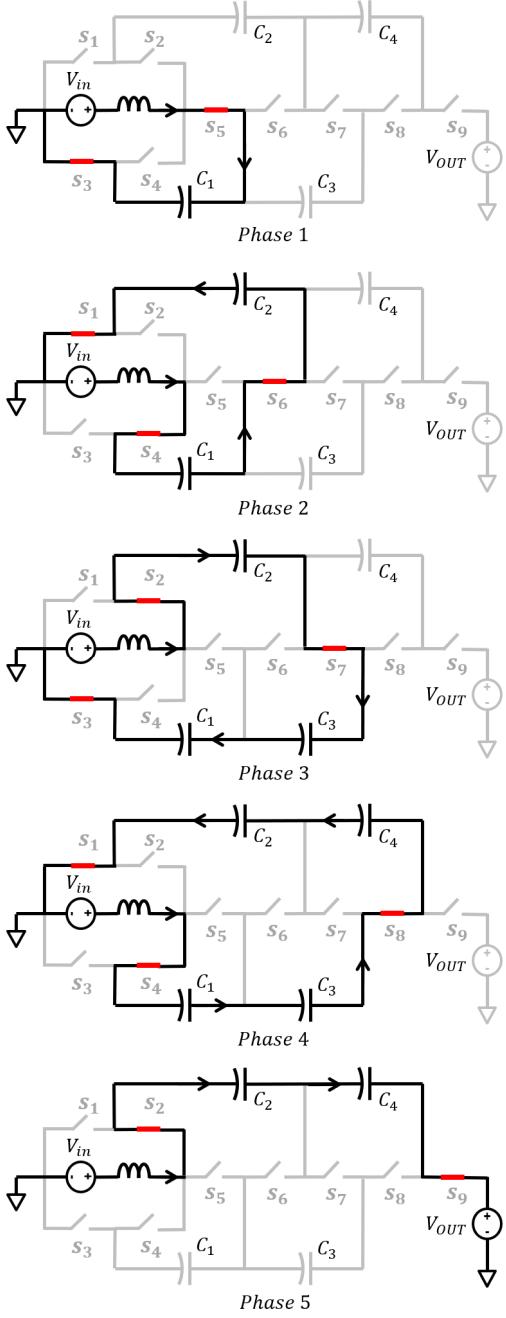


Fig. 2. Phases for a 1:5 CW converter using N-phase switching.

simplifying design and potentially reducing quiescent current draw when compared with the multiple sensors required for the Split-phase scheme discussed in [13] and in part B here. Fig. 3 shows simulated voltage and current waveforms of an $N=5$ CW converter with a load of 160Ω , $V_{IN}=18V$, and ideal resistive switch models. Smooth sinusoidal voltage transitions across fly capacitors implies resonant switching with no abrupt and inefficient charge sharing. Also depicted is the voltage stress across three critical switches. Highlighted in red, one can discern a negative voltage bias being periodically applied to switches S_5 , S_6 , and S_9 that can result in reverse body diode turn-on as internal voltage ripple increases with increased load. At lower voltages, or when diode forward voltage is more significant

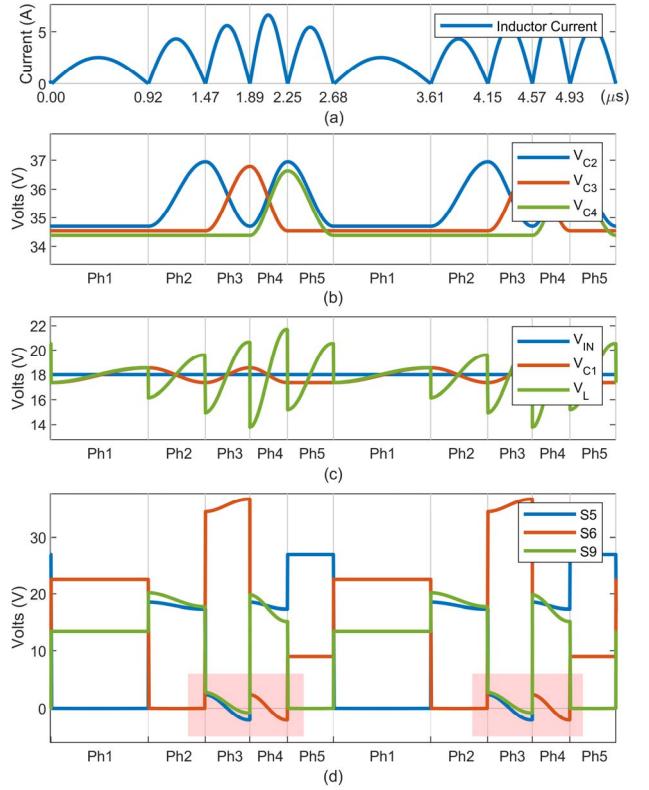


Fig. 3. Simulated N-phase waveforms. (a) Inductor current exhibiting ZCS. (b) and (c) show smooth voltage transitions across fly capacitors and the absolute voltage of switch-node V_L ; the voltage on the inductor terminal opposed to the input. (d) voltage stress across switches S_5 , S_6 , and S_9 with their periodic reverse voltage bias highlighted in red.

(such as with GaN), this heavy-load diode conduction loss can result in significantly reduced efficiency.

B. Split-Phase Switching

The Split-phase approach, discussed in [5] and [13], is an active switching approach that mimics the naturally occurring near-ZVS of an inductively loaded diode-based charge pump [9-11]. By replacing diodes with active switches, the loss due to forward voltage drop can effectively be removed. When operated in resonant mode, in addition to ZCS it also relies on timing sensitive ZVS at several switches throughout the converter and so requires additional sensing circuitry when compared with the N-phase technique. However, lower output impedance and a faster switching frequency result in Split-phase clocking achieving high output power with lower output voltage ripple.

Fig. 4 shows the phase configurations required to effect Split-phase operation for a 1:5 CW converter. Each major phase contains sub-phases which only initialize once ZVS conditions are met: during phase 1 switch S_6 , and during phase 2 switches S_9 and S_5 each engage once ZVS conditions are met. Fig. 5 (a)-(c) depicts simulated voltage and current waveforms showing Split-phase operation at an increased load of 75Ω for improved clarity. Note that phase 1b doesn't engage until $V_{C3}=V_{C4}$, likewise phase 2c commences once $V_{C2}=V_{C3}$, corresponding to ZVS on S_5 . As with N-phase switching, smooth voltage transitions on fly capacitors indicate efficient energy transfer

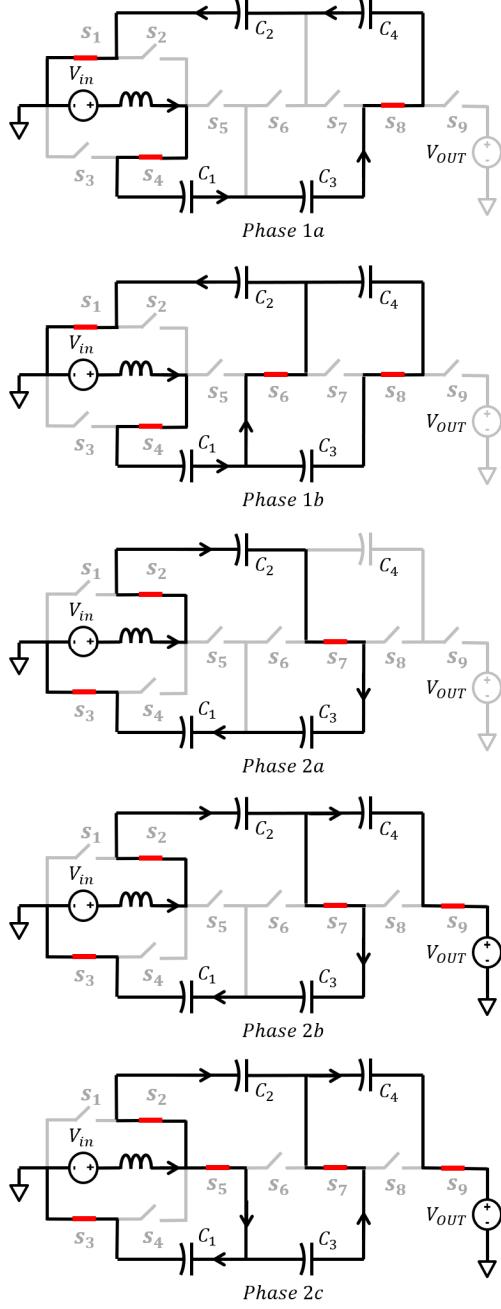


Fig. 4. Phases for a 1:5 CW converter using Split-phase switching.

with no abrupt charge sharing. Fig. 5 (d) shows switch voltage stress, with ZVS indicated in green for switches S₅ and S₉ in phase 2 and S₆ in phase 1.

C. Comparison

By assessing the phase transitions of both schemes using this 1:5 example (Figures 2 and 4), one can see that the N-phase exhibits an increased switching activity of 13 switch cycles per period in contrast to the Split-phase which exhibits 9 switch cycles. However, as seen in Figures 3 and 5, for identical component selection the N-Phase scheme operates over 60% slower than the Split-phase scheme when both are operated at resonance. This results in the N-phase scheme seeing an overall

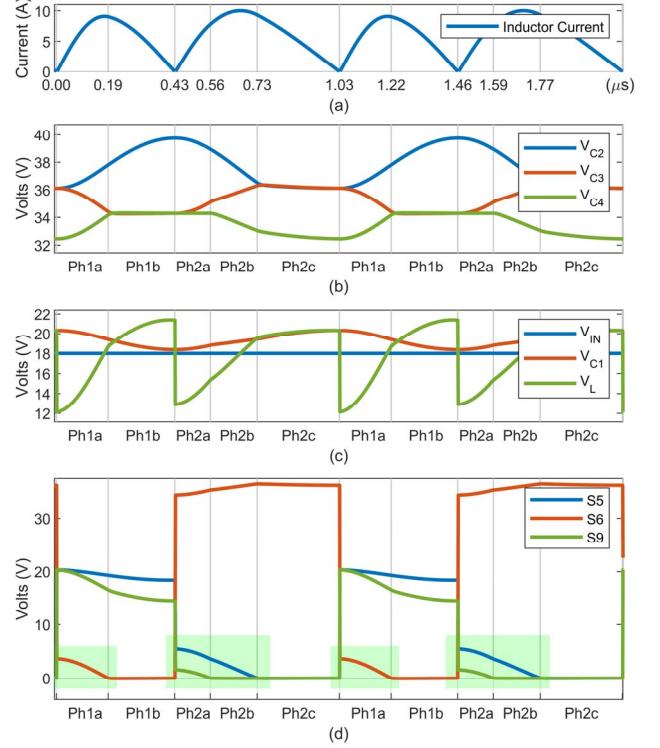


Fig. 5. Simulated Split-phase waveforms. (a) Inductor current exhibiting ZCS. (b) and (c) show smooth voltage transitions across fly capacitors and the absolute voltage of switch-node V_L; the voltage on the inductor terminal opposed to the input. (d) voltage stress across switches S₅, S₆, and S₉ with ZVS events highlighted in green.

reduction in switching losses, improving its light-load efficiency significantly. The reduced sensing hardware requirement and associated losses for the N-phase scheme would likely further compound this effect in a commercial implementation.

Figure 6 shows simulated efficiency versus output power for both control schemes using the same components. As anticipated, the Split-phase achieves highest efficiency at heavy-loads, with the N-phase offering significant light-load improvement. At P_{OUT}=100W the N-Phase scheme delivers a 20% reduction in losses with that margin widening significantly at lighter loads.

Also depicted in Fig. 6 is a projected efficiency curve if body diode turn-on were included. This effect is unique to the N-phase switching scheme and limits its heavy-load efficiency, further justifying use of Split-phase switching in this region of operation. It is worth noting that in this case gallium nitride's increased intrinsic body diode forward voltage, relative to silicon's, may actually serve to improve efficiency for reverse biases less than 2V. However, once this reverse bias is exceeded losses accumulate quickly. To circumvent this, back-to-back NMOS transistors may be employed for switches experiencing a reverse bias, but this will also increase conduction and dynamic losses. Whether or not this approach should be taken will depend on several factors, including available devices, operating point, complexity, and cost.

Since either N-Phase or Split-phase switching can be implemented using the exact same hardware, a combined

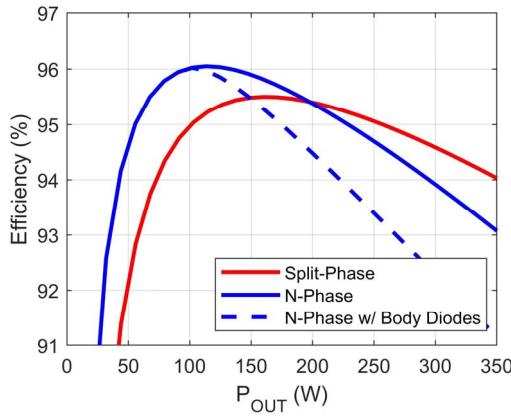


Fig. 6. Simulated efficiency versus output power for both N-Phase and Split-phase control schemes using the exact same device models. Also included is the projected N-phase efficiency response if reverse body diodes are included.

control scheme incorporating both has obvious benefits. Such a scheme would select the more favorable switching technique as a function of operating point, ensuring that efficiency is maximized across the entire load range. For example, in the case of Fig. 6, N-phase switching would be used for loads less than 150W, with the controller transitioning into Split-phase switching at heavier loads.

Both N-phase and Split-phase regimes contain multiple identical phases, and as such these are likely merging points whereby a control algorithm could transition from one switching scheme to the other. Furthermore, future work may assess hybridized switching schemes containing states from both methods, potentially interpolating between each to yield a maximized efficiency curve.

If further improved light-load efficiency is desired, Pulse-Frequency-Modulation (PFM) or Dynamic Off-Time Modulation (DOTM) [18] techniques may also be applied to either N-phase or Split-phase schemes, although, due to the N-phase's inherent light-load advantage, applying such techniques to N-phase operation may be preferable. While not explicitly demonstrated in this work, there are no apparent pitfalls to implementing these modes of operation.

III. DISCRETE PROTOTYPE

A. Design

A discrete 1:5 CW prototype, photographed in Fig. 7, was constructed using gallium nitride FETs. Its total volume of 393 mm³ is calculated by a best-fit cuboid enclosing all active circuitry except the low voltage clock generation (a Tektronix HFS9003 stimulus system). Fig. 8 shows the converter's volume breakdown and Table I lists components used. The prototype was assembled on a low-cost 0.8mm PCB. As such, more advanced assembly techniques on thinner substrates would reduce solution volume significantly. No specific commercial application was targeted for this prototype, but the maximum input voltage was limited by the level-shifters, with a maximum offset of 100V relative to ground. As such, V_{IN} was limited to 20V.

Fig. 9 depicts the power stage and associated gate-driver circuitry. Each switch's gate driver is powered by tapping energy off of the forward power path. Charge is fed onto C_{BP} during the time interval(s) that the primary switching device (S_X) is off, capitalizing on the blocking potential that accumulates across it. To do so, a 5.6V Zener diode reference is source-followed through M₁, effecting a high-speed voltage regulator with minimal quiescent draw or start-up timing requirements. D₁ restricts reverse current flow out of the driver circuitry when the primary switch is on or reverse-biased. This approach was implemented for its simplicity and gives independence to each gate-driver, avoiding bootstrapping problems such as overcharging and diminishing supply voltage due to successive diode drops throughout a distributed bootstrap network. However, at blocking voltages much higher than the driver supply voltage, poor efficiency of the linear regulators strongly motivates adoption of effective bootstrapping techniques, such as [19], in future work.

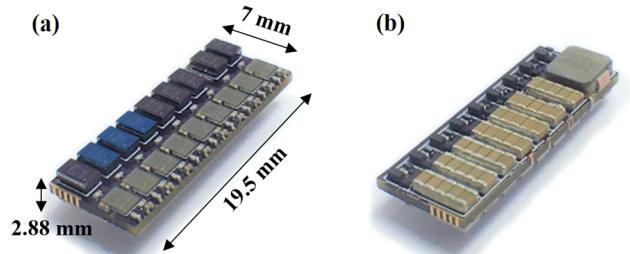


Fig. 7. Photograph of prototype constructed on 0.8mm FR4 with 2oz Cu. (a) Top PCB side contains GaN FETs, gate-drivers and level-shifting. (b) Bottom contains inductor, capacitors, and bootstrapping circuitry.

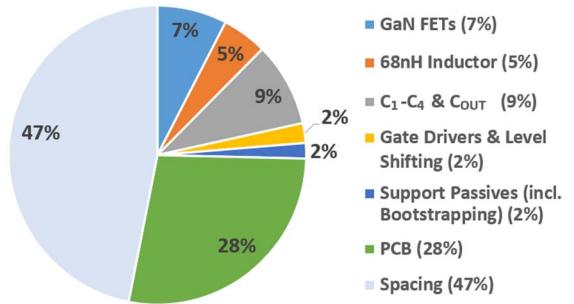


Fig. 8. Volume breakdown of best-fit cuboid encompassing prototype converter. Excludes low voltage clock generation circuitry.

TABLE I. COMPONENT DETAILS

| Component | Description | Part Number |
|-----------------------------------|----------------------------------|--------------------|
| S ₁₋₅ , S ₉ | eGaN FET, 40V, 16A, 5mΩ | EPC2049 |
| S ₆₋₈ | eGaN FET, 100V, 16A, 7mΩ | EPC2045 |
| L | 68nH, 22A DC, 3.2mΩ | IHSR1616ABER68NM01 |
| C ₁₋₄ | 5 x 1μF, 50V, X5R, 1608M | GRT188R61H105KE13 |
| C _{OUT} | 15 x 0.1μF, 100V, X7R, 1608M | GCL188R72A104KA01 |
| U ₁ | 2A/4A, Level-Shift & Gate Driver | PE29102 |
| C _{BP} | 1μF, 6.3V, X5R, 0603M | GRM033R60J105MEA2D |
| R _G | 2.4Ω, 5%, 1/20W, 0603M | RC0201JR-072R4L |
| R _{Z 1-5, 9} | 82kΩ, 1%, 1/20W, 0603M | RC0201FR-0782KL |
| R _{Z 6-8} | 150kΩ, 1%, 1/20W, 0603M | RMCF0201FT150K |
| D ₁ | Diode, 100V, 100mA, 0603M | CDSZC01100-HF |
| D _Z | 5.6V Zener Diode, 100mW, 0603M | SDZT15R5.6 |
| M ₁ | MOSFET, 60V, 320mA, 2Ω | DMN62D1LFB-7B |

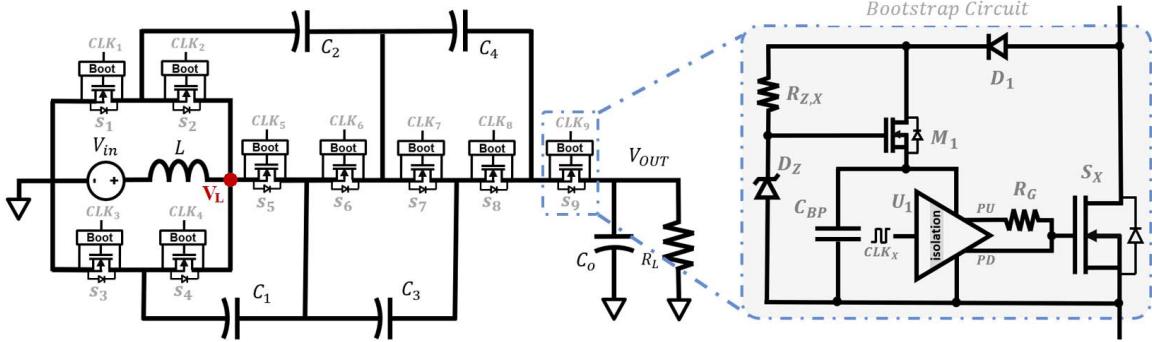


Fig. 9. Schematic of constructed power stage and gate-driver bootstrapping circuitry. D_2 , $R_{Z,X}$, M_1 and D_1 effect a high-speed voltage regulator. Separate pull-up/down outputs on the gate-driver allow independent clock edge tuning for reliability at high speed.

B. Results

Figures 10 and 11 depict measured voltage waveforms at similar load points to the previous simulations, verifying the theory of operation described in Section II. Both figures show significant quantization noise due to single-ended oscilloscope probes requiring a 100V range to measure the absolute voltages of all nodes.

Figures 12 and 13 depict measured efficiency for both N-phase and Split-phase switching schemes using the exact same hardware. As expected, the Split-phase technique obtains the highest output power, while at light load the N-phase approach exhibits up to a 30% reduction in losses making it the preferred switching scheme in this region of operation. Fig. 14 shows measured efficiency curves for a range of input voltages, with the appropriate switching scheme (N-phase or Split-phase) selected for each operating point.

Since these ZCS resonant converters are fixed ratio, output voltage decreases with increased load. This decrease was

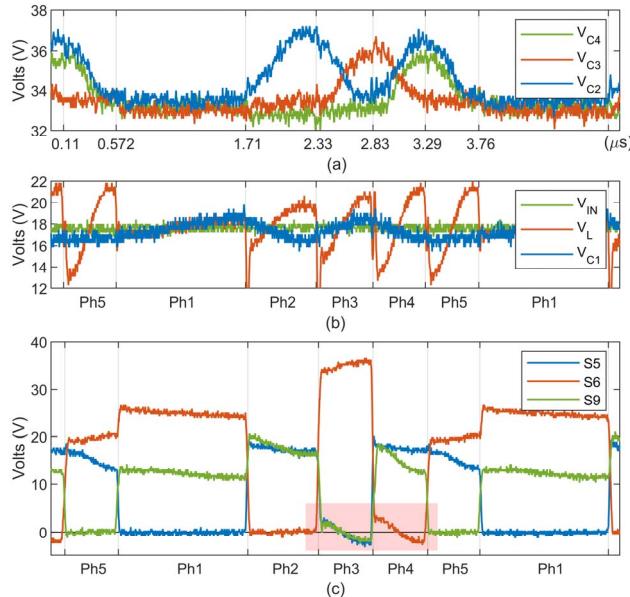


Fig. 10. Measured voltage waveforms for N-Phase CW. (a) and (b) show smooth fly capacitor voltage ripple, implying resonant action, and switch node voltage V_L . (c) shows switch voltage stress with borderline reverse body-diode turn-on highlighted in red.

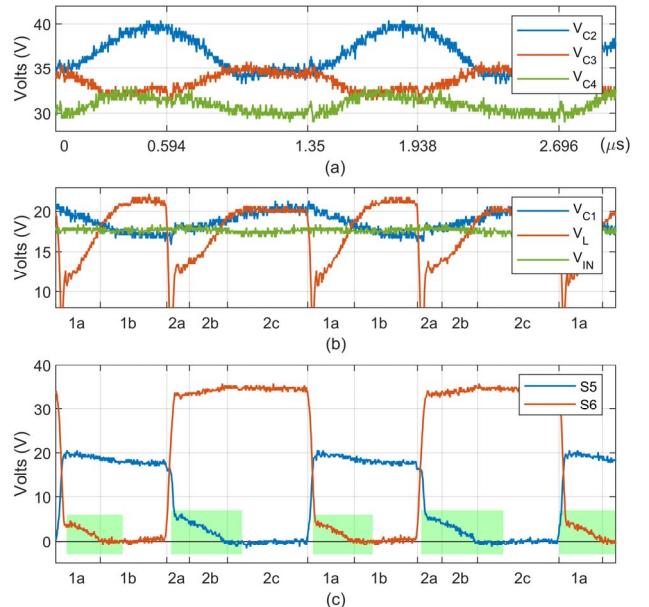


Fig. 11. Measured voltage waveforms for Split-phase CW. (a) and (b) show smooth fly capacitor voltage ripple, implying resonant action, and switch node voltage V_L . (c) shows switch voltage stress with ZVS occurrences highlighted in green.

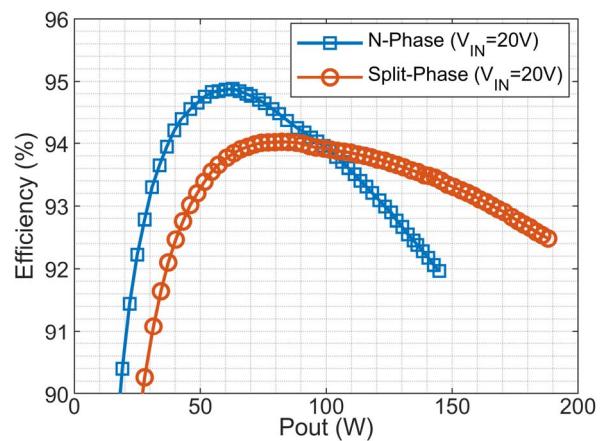


Fig. 12. Measured efficiency versus output power with $V_{IN}=20V$. N-phase and Split-phase techniques depicted in blue and red respectively.

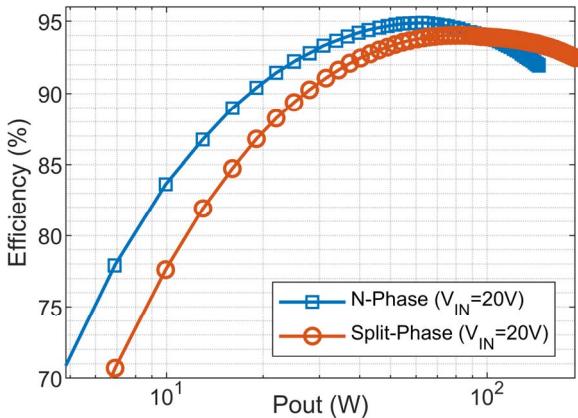


Fig. 13. Measured light-load efficiency versus output power with $V_{IN}=20V$. N-phase and Split-phase techniques depicted in blue and red respectively.

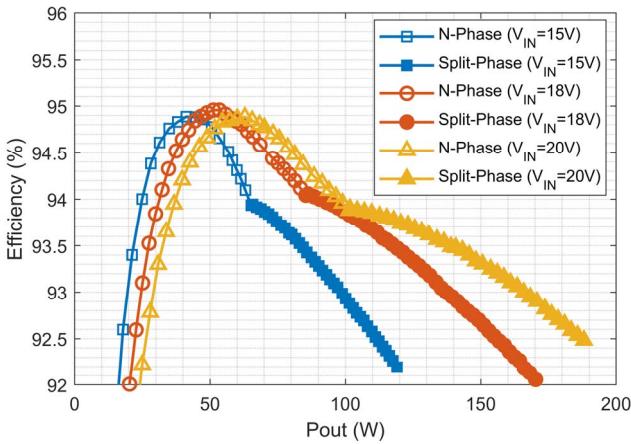


Fig. 14. Measured efficiency versus output power for combined N-phase and Split-phase methods for several input voltages.

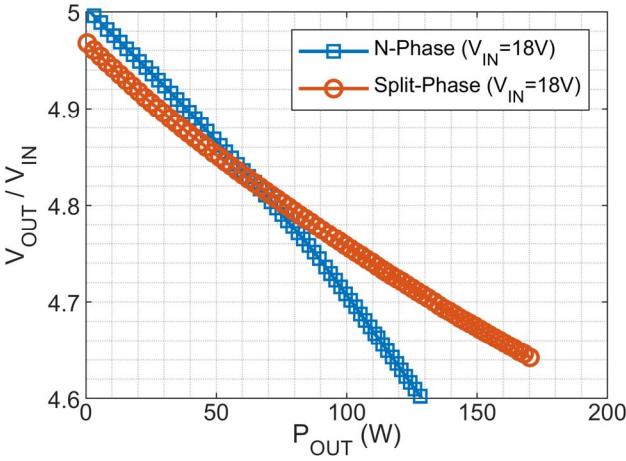


Fig. 15. Measured conversion ratio versus output power for $V_{IN}=18V$. N-phase and Split-phase techniques depicted in blue and red respectively.

measured and is shown in Fig. 15. To achieve output voltage regulation, switching frequency may be increased until the converter enters soft-charging for both switching schemes discussed above [20].

IV. PREVIOUS WORK

Table II compares this work with several other recent relevant studies. Using power density as a comparative figure of merit poses several challenges, primarily due to the differing way it can be presented. As such, Table II presents two different calculation methods with fully disclosed omissions: the first uses maximum output power ($P_{OUT-MAX}$) divided by the volume of a best-fit cuboid encompassing the active converter volume. The second uses $P_{OUT-MAX}$ divided only by the component volume of the power stage (switches, fly capacitors, and inductor(s)) plus that of the gate drivers. Input and output capacitors have been omitted as their full extent is often not reported, although estimates can be made for a desired ripple if switching frequency and power throughput is known. Several different methods exist by which to level shift and provide power to the gate drivers (dictated by cost, size, operating voltage, speed, etc.), and as such this circuitry in addition to any small support passives has been excluded, with only the active gate driving structure included. It is worth noting that operating voltage will significantly impact this metric, with lower voltages suffering worse I^2R losses for the same power throughput, although tempered by reduced voltage blocking requirements. Additionally, conversion ratio cannot be overlooked with larger conversion ratios proving more difficult to realize at high density (e.g., [14]). When compared with [5], the most similar prior work, this prototype achieves a 49% increase in select component volume power density despite a larger conversion ratio at reduced voltage, with roughly equivalent thermal dissipation density (<9% increase). This is likely in large part due to the reduced voltage stress of the CW structure being used in place of the Dickson, as discussed in [12].

V. CONCLUSION

This work is the first comparative study of two recently published switching techniques proposed for hybrid inductor-capacitor (LC) switching converters: N-phase and Split-phase switching. This work also demonstrates the first application of active Split-phase switching to the Cockcroft-Walton topology. A discrete prototype demonstrates that while the Split-phase approach yields highest power density, the N-phase clocking scheme yields superior light-load efficiency when using the exact same hardware. This motivates adoption of combined switching schemes in conjunction with pulse-frequency modulation (PFM) and/or other light-load techniques to yield improved converter performance.

With the proliferation of chip-scale packaging of power components, dramatic increases in power density can be achieved with diverse technologies available in co-packaged modules. Leveraging this, in addition to the methods described above, to the authors' knowledge this work achieves the highest power density published to date at 483.3 kW/liter (7,920 W/inch³), when including all gate drivers, level-shifting, and gate driver power delivery, with 75% of the total volume being consumed by the PCB and free space. Improved substrates and assembly processes will likely increase this metric further, however, as packaging and topological improvements yield record power densities, good thermal design becomes integral to successful implementation.

TABLE II. COMPARISON WITH EXISTING WORK

| | [5] Macy 2015 | [7] Zichao 2018 | [14] Seo 2018 | [12] Ellis 2019 | This work |
|--|---|---|--|---|--|
| Conversion Ratio: | 1-to-4 | 4-to-1 | 6-to-1 (Regulated) | 1-to-5 | 1-to-5 |
| Topology: | Dickson | Cascaded 2:1 | Dickson | Cockcroft-Walton | Cockcroft-Walton |
| Clocking Scheme: | Split-Phase | Conventional | Split-Phase (Dual Inductor) | N-Phase | N-Phase & Split-Phase |
| Switch Type: | GaN FET | MOSFET | GaN FET & Diode | MOSFET | GaN FET |
| f _{sw} : | 1.2MHz | 100kHz | 300kHz | 380kHz | 363kHz & 744kHz |
| Inductor: | 100nH | 188nH & 82nH | 2 x 1.5μH | 30nH PCB-Trace | 68nH |
| Peak Efficiency: | 92% | 98.9% | 95.02% | 95% | 94.9% |
| P _{OUT-MAX} : | 263W | 600W | 20W | 30.6W | 190W |
| V _{IN} @ P _{OUT-MAX} : | 33V | 60V | 48V | 8V | 19.7V |
| Eff. @ P _{OUT-MAX} : | <90% | 98% | ~94.5% | 87.5% | 92.5% |
| V _{OUT} @ P _{OUT-MAX} : | 117V | 15V | 2V | 34.83V | 92V |
| Power Density using best-fit cuboid <i>list of exclusions</i> | 61.7 kW/liter (1,011 W/inch ³) <i>excl. level-shift, driver supply, & clock gen</i> | 133 kW/liter (2,180 W/inch ³) <i>excl. clock gen only</i> | - | 686.4 kW/liter (11,248 W/inch ³) <i>excl. level-shift, driver supply, & clock gen</i> | 483.3 kW/liter (7,920 W/inch³) <i>excl. clock gen only</i> |
| Power Density using select components ^(a) | 1.636 MW/liter (26,818 W/inch ³) | 472 kW/liter (7,734 W/inch ³) | 14.5 kW/liter (238 W/inch ³) | 2.107 MW/liter (34,530 W/inch ³) | 2.437 MW/liter (39,936 W/inch³) |
| Heat Dissipation using select components ^(a) | >181.7 kW/liter (>2.97 kW/inch ³) | 9.6 kW/liter (157 W/inch ³) | 0.84 kW/liter (13.8 W/inch ³) | 301 kW/liter (4.93 kW/inch ³) | 197.6 kW/liter (3.2 kW/inch³) |

^a Components used in calculation: gate drivers, power switches, fly capacitors, and inductor(s).

VI. ACKNOWLEDGMENTS

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