UNIVERISTY OF CALIFORNIA

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Robust High Temperature Operation of Quantum Dot Lasers Grown on Silicon

A dissertation submitted in partial satisfaction of the

requirements for the degree

Doctor of Philosophy

in

Materials

by

Chen Shang

Committee in charge:

Professor John E. Bowers, Chair

Professor Chris Palmstrom

Professor Jonathan Klamkin

Professor Kunal Mukherjee

March 2022

The dissertation of Chen Shang is approved.

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Professor Kunal Mukherjee

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January 2022

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Dedicated to Yating Wan

ACKNOWLEDGEMENTS

The acknowledgement section of anyone's thesis is probably the only place where it's ok for one to be a bit emotional on a permanent record and show his or her personal side before going into the scientific details of the research. Histories are normally presented in either a chronicle or a biographical manner, and I would like to take this chance to re-live the past 5 years in a mixed style and to appreciate the incredible help and support that got me here.

It indeed feels like that the 5-year-PhD has flown by faster than the 3-year-high school. Looking back at it, a lot has happened, from obtaining a PhD degree in the professional life to getting married in the personal life, but it's always the little things that make up the memory. It all started from a phone call with an area code of "805" somewhere around April or May of 2016 as I was finishing up the final report for the senior design project in one of the cubicles in Hicks Library at Purdue. "It's a good offer and you should accept it," says Prof. John Bowers from the other side of the phone and at least that's what I still remember clearly from that 10 minute-ish conversation. Somehow it cleared all my concerns about where to work and live for the next half decade. It turns out to be one of the best decisions I have made so far, and it has indeed altered the course of my life greatly.

Thanks to Prof. John Bowers, I was able to pursue any ideas I might have, good or bad, without worrying about money. His "big picture" guidance has helped me stay on track and focus on what's important before wasting too much energy chasing hoaxes. I still remembered the time when he shared slides on his cross-country bike trip and the time when he jumped onto the table with excitement after seeing the photoluminescent intensities of the on-GaAs and on-Si samples were the same. I then thought it would be pretty cool if I could be like that in my 60's. I would also like to thank him and Ariel for hosting the wedding ceremony and the reception dinner for me and Yating on their mountain top house. It would be a forever cherishable memory, and for that I'm eternally grateful. But I really should have gone for the ski trip when I had the chance. My interaction with

Prof. Arthur Gossard has been mostly limited to the legends I heard about him and John English during their Bell Labs days from Alan and Justin. There was one time after me helping to present someone else's work at a project review meeting, Prof. Gossard said to me, "You are a good presenter." Hearing that from a professor I have admired from afar, I don't think I have ever felt nervous giving talks at professional settings ever since. Prof. Chris Palmstrom's "harsh" questions and the "Are you sure?" when I provided less well-thought answers during my first-year prelim are still ringing in my head. Later I realized that Prof. Palmstrom might having been trying to save me from providing more "less well-thought" answers. Since then, I have put in more critical thinking about the papers I read and the "well done" from him after my second-year qualification exam was indeed a relief. His input on determining the crystalline orientation with in-situ RHEED beam has accelerated my research as well. I would also like to thank Prof. Jonathan Klamkin for providing the MOCVD templates for my research in the LUMOS project.

Prof. Kunal Mukherjee probably deserves to be on the author list, or at least in the acknowledgement, of all my publications on on-Si devices. Leveraging from his expertise on semiconductor dislocations, the on-Si device performances have been significantly boosted. His comment on my work of reducing the defect level on the GaAs virtual substrate on Si, "better than what's been achieved in the past 20 years," really meant something to me. The amazing work from Prof. Matthew Begley and Prof. Danial Gianola on thin film mechanics has helped me with a better understanding of the film cracking issue and provided insights on new ways of defect management. Special thanks to Dr. Robert Herrick and Dr. Weng Chow for their collaborations on reliability and fundamental modelling of the quantum dot lasers. Thanks to Caitlin Eichberg, and previously Tina Hang, for taking a very good care of the reimbursements and purchase orders.

Everything presented in this thesis would not be possible without the help of my immediate colleagues. I came here with absolutely zero knowledge about III-V semiconductors and couldn't even tell the difference between device fabrication and material growth. As one could imagine, I

would require a lot of help just to get started. Thanks to Justin Norman and Daehwan Jung for their unreserved trainings on the growth systems and material characterization tools and shared background readings, I was then able to quickly gain the basic skills and knowledges on what I would be dealing with. They continued to be very helpful for the next few years to answer most of my immediate questions on either specific observations or general strategies on conducting growth experiments. Thanks to Mario Dumont for letting me pick his brain for that deep pool of knowledge on semiconductor devices and for his willingness to get his hands dirty during system maintenance. I really should have taken a picture of the 25 pounds of arsenic debris and other past students' mistakes he dug out from the bottom of the growth chamber during a major system opening.

That being said, I couldn't offer enough gratitude to John English and Kurt Olsson for their unparalleled skills on MBE (most broken equipment) systems. Without them, I'm positive that the chamber wouldn't survive the maintenance cycles, let alone the major opening in 2019 when it was basically disassembled. Soon after that, the COVID-19 pandemic struck hard. Many thanks to Kurt and everyone in the MBE lab for maintaining a reasonable schedule to get as much as research done during those hard times. I would also like to thank Eamonn Hughes, and previously Jennifer Selvidge and Aidan Taylor, for allocating some of their TEM slots for my materials. Their timely and high-quality feedback have offered valuable information for me to gauge the crystal quality and debug the growth conditions. The new student in the project, Rosalyn Koscica, has also done a great job in data gathering and summarizing. Thanks everyone else in the Bowers group, MJ, Paolo, Jon, Lin, Chao, Warren, Zeyu, Joel, Kaiyin, Trevor, Ted, Andy, Josh, Alex, Eric, Tony, Minh, and Alfredo, for offering a helping hand when needed and establishing a pleasant working environment.

People outside of my academic life also deserve to be recognized. Awesome people I met on my very first day here, Yichao Chow, Wanying Ho, and Clayton Qwah, and later, Alex Chang, Brent Tan, the Carters family, and Zach Biegler, have helped me stay sane. The trips to Yosemite, San Diego, and Las Vegas; potluck dinners, board games, birthdays, and holiday gatherings have forever

made their marks on my Ph.D. journey. Special thanks to Brent Tan and his family for their hospitality during me and my wife's trip to Singapore. I really do hope to see you guys again.

The one person that has witnessed and participated in almost every aspect of my Ph.D. endeavor is my wife, Yating Wan. From not remembering who I was after talking face to face just a day before in Feb. 2017, to being too nervous and saying "Thank you" instead of "Yes" to my proposal at 2019 Bowies, to getting married on Feb. 16th 2020 at Prof. Bowers' place, and to now at the start of the next phase in life. I have never imaged myself getting married at the age of 27. It seems hard to find someone who would truly understand and endure your frustrations, share your happiness and achievements, and believe in you before you believe in yourself. I feel blessed find one and to have her by my side.

Finally, of course, my parents. A Ph.D. doesn't just take 5 years but the entire life up until now to build up to it. When I was still in high school, my father once told me that he had to find a secure job to put bread on the table and I shouldn't have that burden and go do what I want. Thanks to their emotional and financial support, I was able to weather any obstacles with a mind at ease.

CURRICULUM VITAE

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Personal Particulars

Chen Shang obtained his B.S. degree in the Department of Material Science and Engineering at Purdue University in 2016 (GPA: 3.97/4.0), and graduated with the Distinguished Graduate Award, which is the highest recognition for undergraduates at Purdue. He then joined the group of Prof. John Bowers (US NAE) of ECE and Materials at the University of California, Santa Barbara where he is finishing Ph.D. by early 2022. He has published **32 (7 as first author/contributed equally author) high quality peer-reviewed journal papers**, 17 peer-reviewed international conference proceedings (4 as first author). Google Scholar Citations: 655, h-index: 18. He has received several prestigious awards and fellowships.

RESEARCH INTERESTS:

Overview: Quantum dots (QDs), either epitaxially grown or fabricated in solutions, have widely tunable chemical, physical, electrical, and optical properties. A further and more clearer understanding of the QD surfaces, atomic arrangements, strain states, and metastable characteristics would help controlling such properties more precisely for applications in imaging, sensing, quantum computing, displays, solar energy harvesting, and communication.

1. **Solid state LiDAR for 3D sensing and autonomous driving**

   Most commercial LiDAR systems today utilize discrete free-space optical components and a mechanical apparatus for beam steering. To reduce the cost and to increase the reliability of LiDAR systems, optical phased arrays with integrated on-chip light source, either heterogeneously or monolithically, would be an ideal candidate. QD light source potentially requires no isolator within the package and provides a wide range of wavelength tunability. Such compact and reliable systems could be integrated with automobiles for self-driving cars, as what Tesla is trying to accomplish.

2. **Quantum computing**

   QDs are inherently two-level systems that can be used as qubits for quantum computers and secure communication. Epitaxial QDs as single sources have demonstrated high fidelity and close to zero $g^{(2)}(\tau=0)$. Though the coherence properties of QD qubits are superior, they are still behind atoms or defect centers (like NV centers). The other challenges, in addition to improving the photon source, would be to integrate with photonic circuits, increase operation temperature, and realizing all that near 1550 nm. Quantum computing and quantum key distribution for secure communication have been a big interest to major tech giants, like Microsoft, Google, Facebook, et al.

3. **Bioimaging and biophotonics**

   Biochemical sensors, either to detect hazardous materials in the environment or to trace molecule in an organism for diagnostics, need to be cheap to build, easy to operate, and robust against environment conditions. Photonic integrated circuit-based architecture is thus a promising candidate. The properties of the light propagating inside a waveguide are very sensitive to the index changes, which could then be translated to high detection sensitivity when chemical agents bind with the waveguide (e.g. MZIs, ring resonators, etc.). The on-chip light source, which is required for this architecture. recently has witnessed a breakthrough in the reliability of the epitaxially grown QD lasers on Si. Colloidal QDs, with their large surface-to-volume ratio and highly tunable surface chemical potential, are good candidates for receptors tailored for specific chemical species. The

colloidal QDs can also be tethered to specific proteins, antibodies, or other biological species and be used as optically addressable biolabels for tracing the molecules inside an organism for diagnoses.

4. Communication

Epitaxially grown QDs lasers on Si, emitting near 1.3 μm for data center chip-to-chip communications, have demonstrated remarkable reliability at elevated temperatures due to their insensitivity to crystal defects. Delta-function-like density of states in these nanoparticles results in low threshold current and temperature sensitivity. Low linewidth enhancement factor also promises isolator-free operation. To monolithically integrate such devices with SiPh platforms, growing the epi stack within a pre-patterned template with all other photonic circuit components included is a viable yet challenging path. Monolithic integration is the most economical approach for obtaining on-chip light source. If this approach would succeed, it would be of great interest to Intel for their 3rd Generation of light source integration, following hybrid and heterogenous approaches.

5. Next generation displays

In highly monodisperse colloidal QD samples, the narrow linewidth (<30 nm for QD and >60 nm for OLEDs) enables the high color purity for the next-generation display (Rec. 2100). Colloidal QDs films, sandwiched between electron and hole injection layers, can be used to implement RGB LEDs with high color purity. The close-to-unity PL quantum yield of such QDs also promises high brightness. Such displays would be of great interest to Samsung and Apple for their screens.

EDUCATION AND WORKING EXPERIENCE:

1. **University of California, Santa Barbara, CA** Sep. 2016—now
   PHD candidate in the Materials Department, Advisor: **Prof. John Bowers (bowers@ece.ucsb.edu)**
   Topic: "Molecular beam epitaxy of III-V Quantum Dot Lasers on Silicon substrates"
2. **Purdue University, West Lafayette, IN** Sep. 2012— May. 2016
   Bachelor in Material Science and Engineering, **GPA: 3.96/4.0**
   - **Distinguished Graduate Award (2 awardees in Material Science and Engineering in Purdue).**

ACADEMIC AWARDS:

1.	AIM Photonic Fellowship	Jul. 2019—Dec. 2019
2.	Peter J. Frenkel Foundation Fellowship	Sep. 2018—Jun. 2019
3.	Edward J. Sopcak Memorial Scholarship in Purdue University	Aug. 2013—May. 2014
4.	Hoffman Memorial Scholarship in Purdue University	Aug. 2014—May. 2015
5.	National Society of Collegiate Scholars	Sep. 2013 — May. 2016
6.	Honor Society Scholarship	Jun. 2014 — May. 2016
7.	Distinguished Graduate Award (2 per year per school)	May. 2016

TEACHING:

1. Year 2017-2018: Teaching Assistant of "Matrl 200C – Structure Evolution" at UCSB

PHD RESEARCH PROJECTS:

- **High Efficiency Quantum-Dot Photonic Integrated Circuit Technology Epitaxially Grown on Silicon**

(Period 4/1/2016 to 6/30/2019, budget; $2,037,285);

- **Frequency Stabilized Coherent Optical Low-Energy WDM DC Interconnects**. (Period 9/18/2019 to now, budget; $2,037,285);
- **Defense Advanced Research Projects Agency**-LUMOS-Hetro-Epitaxy Laser Integration on Silicon (2/6/2020 to now, total budget: $19,481,140);

***Undergraduate projects are summarized at the end.**

SKILLS SET:

- 5 years of molecular beam epitaxy growth experience specialized in quantum dot lasers and metamorphic growth of III-V on Si
- In-depth knowledge of metamorphic growth, optoelectronics, material characterization, diode lasers, etc.;
- Hand-on experimental experiences of static laser characteristics measurements.

PUBLICATIONS:

- **Journal Articles**

I. First-author papers

1. **C. Shang,** "Microstructure Development during Compaction of Granular Systems" The Journal of Purdue Undergraduate Research, Vol. 5, Article 29. DOI: 10.5703/1288284315672 (2015).
2. **C. Shang**, Y. Wan, J. Norman, N Collins, I MacFarlane, M Dumont, S Liu, Q. Li, K. M. Lau, A. C. Gossard, and J. E. Bowers*, "Low-Threshold Epitaxially Grown 1.3-μm InAs Quantum Dot Lasers on Patterned (001) Si", *IEEE Journal of Selected Topics in Quantum Electronics* 25 (6), 1-7 (2019).
3. **C. Shang**, J. Selvidge, E. Hughes, J. C. Norman, A.A. Taylor, A. C. Gossard, K. Mukherjee, J. E. Bowers, "A Pathway to Thin GaAs Virtual Substrate on On-Axis Si (001) with Ultralow Threading Dislocation Density", *Physica Status Solidi (a)* (2020): 2000402
4. **C. Shang**#, E. Hughes#, Y. Wan#, M. Dumont, R. Koscica, J. Selvidge, R. Herrick, A.C. Gossard, K. Mukherjee, and J. E. Bowers, "High-temperature reliable quantum-dot lasers on Si with misfit and threading dislocation filters", Optica 8(5),749-754 (2021). **(Impact: 11.1)**
5. **C. Shang#,** Yating Wan#, Jenny Selvidge, Eamonn Hughes, Robert Herrick, Kunal Mukherjee, Frederic Grillot, Weng W. Chow, John E. Bowers, "Advances in quantum dot lasers and integration with Si photonic integrated circuits", ACS Photonics (2021), Article ASAP, **Invited. (Impact: 6.88), selected as cover.**
6. **C. Shang,** M. Begley, D. Gianola, J. Bowers, "Crack Propagation in Low Dislocation Density Quantum Dot Lasers Epitaxially Grown on Si", APL Materials, submitted.
7. Y. Wan#, D. Jung#, **C. Shang#**, N. Collins, I. Macfarlane, J. Norman, M. Dumont, A. C. Gossard, and J. E. Bowers*, "Low-threshold continuous-wave operation of electrically-pumped 1.55 μm InAs quantum dash microring lasers", *ACS Photonics*, 6 (2), pp 279–285 (2019). **(Impact: 6.88) (#Equally contributing authors).**

8. Y. Wan[#], **C. Shang[#]**, J. Norman, B. Shi, Q. Li, N Collins, M Dumont, K. M. Lau, A. C. Gossard, and J. E. Bowers*, "Low threshold quantum dot lasers directly grown on planar (001) Si", *IEEE Journal of Selected Topics in Quantum Electronics.* 26, 1-9, 2020. **([#]Equally contributing authors).**
9. Y. Wan[#], **C. Shang[#]**, J. Huang, Z. Xie, A. Jain, D. Inoue, B. Chen, J. Norman, A. C. Gossard, and J. E. Bowers*, "Low-dark current 1.55 μm InAs quantum dash waveguide photodiodes", *ACS nano* 14(3), 3519-3527, 2020. **(Impact: 13.9, [#]Equally contributing authors).**
10. **C. Shang,** Y. Wan, E. Hughes, R. Koscica, J. Bowers, "Degradation of quantum well lasers epitaxially grownon Si". [In preparation]

II. Co-author papers

1. D. Jung, J. Norman, MJ Kennedy, **C. Shang,** B. Shin, Y. Wan, A. C. Gossard, J. E. Bowers*, "High efficiency low threshold current 1.3 μm InAs quantum dot lasers on on-axis (001) GaP/Si," *Appl. Phys. Lett.* 111, 122107 (2017).
2. Y. Wan, D. Jung, J. Norman, **C. Shang,** L. Macfarlane, Q. Li, MJ. Kennedy, Z. Zhang, A. C. Gossard, E. L. Hu, K. M. Lau, and J. E. Bowers*, "O-band electrically injected InAs quantum-dot micro-ring lasers on V-groove patterned and unpatterned (001) silicon", *Optics Express,* 25(22), 2017.
3. Y. Wan, Z. Zhang, R. Chao, J. Norman, D. Jung, **C. Shang,** Q. Li, MJ. Kennedy, D. Liang, C. Zhang, J. Shi, A. C. Gossard, E. L. Hu, K. M. Lau, and J. E. Bowers*, "Monolithically Integrated InAs/InGaAs Quantum Dot Photodetectors on Silicon Substrates", *Optics Express,* 25(22), 2017. (**Featured by Semiconductor Today as a spotlight)**.
4. J. Bowers, J. Norman, D. Jung, S. Liu, Y. Wan, **C. Shang**, R. Herrick, A. Gossard, "Mode-Locked Quantum Dot Lasers Epitaxially Grown on Si", *Applied Physics Letters,* 112, 15, 153507, (2018).
5. J. Norman, D. Jung, Z. Zhang, Y. Wan, S. Liu, **C. Shang,** R. W. Herrick, W. W. Chow, A. C. Gossard, J. E. Bowers, "A Review of High-Performance Quantum Dot Lasers on Silicon.", *IEEE Journal of Quantum Electronics* 55(2), 1-11(2019). **(Invited)**.
6. Y. Wan, D. Innoue, D. Jung, J. Norman, **C. Shang**, A. C. Gossard, and J. E. Bowers*, "Directly modulated quantum dot lasers on Si with milliamp threshold and high temperature stability", *Photonics Research,* 6(8), 776-781 (2018). **(Impact: 5.522, selected as the Cover of the Photonics Research, and top 10 cited articles on Integrated Optics published in 2018)**
7. J. Huang, Y. Wan, D. Jung, J. Norman, **C. Shang**, Q. Li, K. M. Lau, A. C. Gossard, J. E. Bowers, and B. Chen, "Defect characterization of InAs/InGaAs quantum dot pin photodetector grown on GaAs-on-V-grooved-Si substrate", *ACS Photonics* (2019). **(Impact: 6.88)**
8. K. Sun, D. Jung, **C. Shang,** A. Liu, J. Morgan, J. Zang, Q. Li, J. Klamkin, J. E. Bowers, A. Beling "Low dark current III–V on silicon photodiodes by heteroepitaxy", *Optics express* 26 (10), 13605-13613
9. D. Inoue, Y. Wan, D. Jung, J. Norman, **C. Shang**, N. Nishyama, S. Arai, A. C. Gossard, and J. E. Bowers, "Low-dark current 10 Gbit/s operation of InAs/InGaAs quantum dot p-i-n photodiode grown on on-axis (001) GaP/Si", *Applied Physics Letters,* 113(9), 093506 (2018).
10. Y. Wan, S. Zhang, J. Norman, MJ Kennedy, W. He, S. Liu, C. Xiang, **C. Shang,** J. He, A. C. Gossard, and J. E. Bowers*, "Tunable quantum dot lasers directly grown on Si", *Optica,* 6(11), (2019). **(Impact: 9.263).**

11. B. Chen, Y. Wan, Z. Xie, J. Huang, **C. Shang**, J. Norman, Q. Li, Y. Tong, K. M. Lau, A. C. Gossard, and J. E. Bowers, "Low-dark current high gain InAs quantum dot avalanche photodetectors monolithically grown on Si", *ACS Photonics* , 7(2), 528-533, 2020.
12. B. Dong, J. Duan, **C. Shang,** H. Huang, A. B. Sawadogo, D. Jung, Y. Wan, J. E. Bowers, and F. Grillot, "Influence of the polarization anisotropy on the linewidth enhancement factor and reflection sensitivity of 1.55-μm InP-based InAs quantum dash lasers", *Appl. Phys. Lett.* 115, 091101 (2019).
13. J. Norman, Z. Zhang, D. Jung, **C. Shang**, MJ Kennedy, M. Dumont, R.W Herrick, A. C. Gossard, and J. E. Bowers, "The importance of p-doping for quantum dot laser on silicon performance", *IEEE Journal of Quantum Electronics* 55 (6), 1-11, 2019.
14. Y. Wan, J. Norman, Y. Tong, MJ Kennedy, W. He, J. Selvidge, **C. Shang**, M. Dumont, A. Malik, H. K. Tsang, A. C. Gossard, and J. E. Bowers*, "1.3 μm quantum-dot distributed feedback lasers directly grown on (001) Si", *Laser & Photonics Reviews.* **(published online and selected as back cover of the issue).**
15. J. Selvidge, J. Norman, E. T. Hughes, **C. Shang**, D. Jung, A. A. Taylor, MJ Kennedy, R. Herrick, J. E. Bowers, K. Mukherjee, "Defect filtering for thermal expansion induced dislocations in III-V lasers on silicon", *Applied Physics Letters* 117(12), 122101
16. Y. Wan, S. Zhang, J. Norman, MJ Kennedy, W. He, Y. Tong, **C. Shang**, J. He, H. K. Tsang, A. C. Gossard, and J. E. Bowers*, "Directly modulated single-mode tunable quantum dot lasers at 1.3 μm", *Laser & Photonics Reviews.* 14(3), 1900348, 2020 **(Impact: 9.056, selected as back cover of the issue).**
17. J. Selvidge, E. Hughes, J. Norman, **C. Shang**, MJ. Kennedy, M. Dumont, A. Netherton, Z. Zhang, R. Herrick, J. Bowers, K. Mukherjee, "Reduced dislocation growths leads to long lifetime InAs quantum dot lasers on Si at high temperatures", *Applied Physics Letters* 118 (19), 192101.
18. L. Galletti, A. Rashidi, D. Kealhofer, M. Goyal, B. Guo, Y. Li, **C. Shang**, J. Bowers, S. Stemmer, "Quantum hall effect of the topological insulator state of cadmium arsenide in corbino geometry", *Applied Physics Letters* 118 (26), 261901.
19. E. Hughes, B. Haidet, B. Bonef, J. Selvidge, **C. Shang**, J. Norman, J. Bowers, K, Mukherjee, "Advances in heteroepitaxial integration of III-V and IV-VI semiconductors with electron channeling contrast imaging", *Microscopy and Microanalysis* 27(S1), 908-910
20. K. Mukherjee, J. Selvidge, E. Hughes, J. Norman, **C. Shang**, R. Herrick, J. Bowers, "Kinetically limited misfit dislocations formed during post-growth cooling in III-V lasers on Silicon", *Journal of Applied Physics*, 2021, accepted.

- **Conference Proceedings**

I. First author

1. **C. Shang,** Y. Wan, D. Jung, J. Norman, MJ Kennedy, D. Liang, C. Zhang, A. C. Gossard, J. E. Bowers*, "Quantum dot micro-lasers integrated with photodetectors and optical amplifiers on (001) Si via waveguide coupling," CLEO: Science and Innovations, SM2I. 6.
2. **C. Shang,** Y. Wan, J. Norman, D. Jung, Q. Li, K. M. Lau, A. C. Gossard, and J. E. Bowers*, "Triple reduction of threshold current for 1.3 μm InAs quantum dot lasers on patterned, on-axis (001) Si", *in 2019 CLEO: Science and Innovations*, pp. STu3N.1Optical Society of America.

3. **C. Shang**, J. Norman, A. C. Gossard, J. E. Bowers*, "GaAs epitaxy on (001) Si: below 1×10^6 cm^{-2} dislocation density with 2.4 μm buffer thickness", in 2020 CLEO: Science and Innovations.
4. **C. Shang**, E. Hughes, Y. Wan, M. Dumont, R. Koscica, J. Selvidge, R. Herrick, A. C. Gossard, K. Mukherjee, and J. E. Bowers, "High Temperature reliable epitaxially grown quantum dot lasers on (001) Si with record performance", in 2021 CLEO: Postdeadline Papers Presentation II, SF1B.7

II. co-authors

1. K. Sun, D. Jung, **C. Shang,** A. Liu, J. E. Bowers, A. Beling, "Low-dark current III-V photodiodes grown on silicon substrate", Photonics Conference (IPC), 2017 IEEE, 95-96.
2. Y. Wan, D. Innoue, D. Jung, J. Norman, **C. Shang,** A. C. Gossard, J. E. Bowers*, "Directly modulated quantum dot micro-ring lasers at 1.3 μm on (001) GaP/Si with low-threshold current.", Progress In Electromagnetics Research Symposium (PIERS), 2018. **(Invited)**.
3. D. Jung, J. Norman, MJ Kennedy, R. Herrick, **C. Shang,** C. Jan, A. C. Gossard, J. E. Bowers, "Low Threshold Current 1.3 μm Fabry-Perot III-V Quantum Dot Lasers on (001) Si with Superior Reliability" , 2018 Optical Fiber Communications Conference and Exposition (OFC), 1-3, 2018.
4. J. Norman, D. Jung, MJ Kennedy, **C. Shang,** A. C. Gossard, J. E. Bowers, "Low threshold epitaxial InAs quantum dot lasers on on-axis GaP/Si (001)", Photonics Conference (IPC), IEEE, 403-404, 2017.
5. S. Liu, X. Wu, J. Norman, D. Jung, M. Dumont, **C. Shang,** Y. Wan, MJ Kennedy, B. Dong, D. Auth, S. Breuer, F. Grillot, W. Chow, A. C. Gossard, J. E. Bowers, "High-performance mode-locked lasers on silicon", in *Physics and Simulation of Optoelectronic Devices XXVIII* 11274, 112741K, 2020.
6. J. C. Norman, S. Liu, Y. Wan, Z. Zhang, **C. Shang,** J. G. Selvidge, M. Dumont, MJ Kennedy, D. Jung, J. Duan, H. Huang, R. W. Herrick, F. Grillot, A. C. Gossard, J. E. Bowers, "Epitaxial integration of high-performance quantum-dot lasers on silicon", in *Silicon Photonics XV* 11285, 1128504, 2020.
7. D. Jung, J. Norman, S. Liu, **C. Shang**, Y. Wan, A. Gossard, J. E. Bowers, "Growth of Broadband Gain Quantum Dot Mode-Locked Laser on Si with Varied InGaAs Well Thickness", in *International Conference on Optical MEMS and Nanophotonics (OMN),* 24-25, 2019.
8. Y. Wan, D. Jung, **C. Shang,** N. Collins, I. Macfarlane, J. Norman, M. Dumont, A. C. Gossard, and J. E. Bowers*, "Low threshold 1.55 μm Quantum dash microring lasers", *in 2019 CLEO: Science and Innovations*, pp. STu4J.3. Optical Society of America.
9. P. Bhasker, C. Shang, J. E. Bowers, N. Dagli, "Low Loss, Compact Waveguides in GaAs/Oxidized AlGaAs Layers Directly Grown on Silicon", *CLEO: Science and Innovations*, STh3N. 7, 2019.
10. Y. Wan, S. Zhang, J. Norman, MJ Kennedy, W. He, Y. Tong, **C. Shang,** J. He, H. K. Tsang, A. C. Gossard, and J. E. Bowers*, "1.3 μm tunable quantum dot lasers", *CLEO* 2020.

Oral presentations

1. **C. Shang,** D. Jung, Y. Wan, J. Norman, A. C. Gossard, J. E. Bowers*, "InP-based quantum dash lasers emitting at 1.55 m with low threshold current density," *Electronic Materials Conference (EMC),* 2018.

2. **C. Shang**, J. Norman, A. C. Gossard, J. E. Bowers*, "Effectiveness of $In_{0.15}Ga_{0.85}As$ dislocation filter on GaAs surface with different threading dislocation density", North America Molecular Beam Epitaxy Conference, 2019.
3. J. Norman, D. Jung, Z. Zhang, M. J. Kennedy, K. Turnlund, **C. Shang,** Y. Wan, A. C. Gossard, and J. E. Bowers*, "The impact of threading dislocation density in InAs/GaAs quantum dot lasers grown on (001) silicon," in *International Conference on Molecular Beam Epitaxy (ICMBE),* 2017.
4. J. Norman, D. Jung, P. Pintus, Y. Wan, Q. Li, P. Bhasker, Z. Zhang, **C. Shang,** M. J. Kennedy, N. Dagli, K. M. Lau, A. C. Gossard, and J. E. Bowers*, "InAs Quantum Dot Devices for Epitaxial Photonic Integrated Circuits on Silicon," in *International Conference on Molecular Beam Epitaxy (ICMBE),* 2018.
5. J. Norman, Z. Zhang, D. Jung, Y. Wan, S. Liu, **C. Shang**, R. W. Herrick, A. C. Gossard, and J. E. Bowers*, " Reliable, Feedback Insensitive p-Modulation Doped Quantum Dot Lasers Epitaxially Grown on CMOS Compatible Silicon Substrates" *ISPEC*, 2018. (**Invited**).

MEDIA COVERAGE:

- My contributed work of **"Monolithically Integrated InAs/InGaAs Quantum Dot Photodetectors on Silicon Substrates"** was reported by *Semiconductor Today* with a spotlight summary titled "Monolithic indium arsenide quantum dots on silicon optoelectronics" http://www.semiconductor-today.com/news_items/2017/nov/ucsb_221117.shtml

UNDERGRADUATE PROJECTS:

1. Research assistant, NanoHUB, with Dr. Tanya Faltens Aug 2013-May 2014

• First author of the design and development of an educational level simulation tool on n-MOSFET that simulates the output the device based on the material properties of each component of the transistor. The tool is designed to illustrate basic concepts of n-MOSFET to sophomore and early junior students. **The current number of users of my developed simulation tool is about 3800.** Link: https://nanohub.org/tools/mosfetsat

• Help research and develop a research level simulation tool on magnetic tunnel junction device (MTJ). Unlike traditional transistors, MTJ stores information by the spin of electrons which can be controlled by the magnetic field applied. **The current number of users of my developed simulation tool is about 210.** Link: https://nanohub.org/tools/mtjlab

• **Presented my research results to the NSF board** on their last site visit to NanoHUB on April 26th 2014, where the board members assessed how the funding had been used and decided whether to maintain the level of funding. I was selected to demonstrate the ongoing and finished projects. The board member was impressed and encouraged me to mention the talk on the resume.

2. SURF-Summer Undergraduate Research Fellowship May 2014-Aug 2014

• Performed research with Prof. Marcial Gonzalez on the compaction process of granular materials. Exploring the contact mechanisms, mainly Hertz' theory and nonlocal contact formulation (NLC), and their accuracy in predicting the behavior of powder compact. Hertz's theory assumes the contacts are independent, while NLC releases this assumption. Thus the predicted results deviate more at higher level of confinement and the results from NLC have a better match to the experimental results.

• Periodical result is published in Purdue Undergraduate Research Journal (JPUR) and illustrated in the first version of a simulation tool that I and the Prof. Gonzalez developed on granular material compaction process. Link: https://nanohub.org/tools/gscompaction

3. Individual Research-Behavior of monodispersed binary mixture, with Prof. Marcial Gonzalez

• Explore the particle-die relative size effect on the behavior of the mixture compact. As the particle size increases with respect to the die, the particle-wall normal interactions start to play an important role in the mixture behavior, thus the particle size is kept small enough to make the prediction more practical.

• Utilize the Hertz's theory and study the non-linear nature of powder mixture compact. The traditional mixture rule does not apply to the powder mixture compact, as the force required to reach a certain relative density does not vary linearly with respect to composition.

• A force chain approach is exercised to capture the non-linear nature, considering the fact that the force within the compact is supported by multiple particle chains. The results are very promising and the approach has a great potential to be extended to more complex contact mechanisms and particle geometries. The full paper might be published next year.

LIST OF FIGURES

Figure 1: Left panel shows the stimulated emission process with in InP, a typical direct bandgap semiconductor. The right panel shows that the recombination process requires phonon participation in an indirect bandgap semiconductor, i.e. Si... 2

Figure 2: Schematic illustration of (a) hybrid and (b) heterogenous integration. 3

Figure 3: Common crystalline defects of (a) threading dislocations from the plastic relaxation due to the lattice mismatch and (b) anti-phase domains formed at the step edges of the Si substrate due to polarity mismatch. 5

Figure 4: Growth modes are generally determined by the relationship between surface free energies of the film-vacuum interface γe, the film-substrate interface γi, and the substrate-vacuum interface γs. (a) Frank-van der Merwe growth mode: $\gamma e + \gamma i < \gamma s$. (b) Volmer-Weber growth mode: $\gamma e + \gamma i > \gamma s$. (c) Stranski-Krastanov growth mode: the film initially wets the substrate as in the FWM growth mode, and transition to 3D islands after building up enough strain energy (APL tutorial). 8

Figure 5: (a) Energy quantization occurs when the spatial extend of the electronic wave functions is smaller than the Bohr exciton diameter (aB). The bandgap and the energy spacing between the states can be tuned with the QD diameter (D)[33]. (b)-(e) Schematics of the 3d, 2d, 1d, and 0d structures and their corresponding density of states, respectively. 9

Figure 6: (a) Example room temperature PL of InAs QDs emitting around 1300 nm. The inset shows the exposed QDs morphology with a surface density of approximately 6×10^{10} cm^{-2}. (b) Calculated modal gain of QDs and QWs with respect to the injection current density. The red triangles and the grey circle are the measured values for QD and QW lasers, respectively. The case with $\Delta inh = 20\ meV$ matched with the experimental results[36]. 10

Figure 7: (a) Filtered CL maps for different transitions at 300K. (b) Temperature dependent CL intensity line scan across the identified MD, located at the origin, in different transitions. (c) and (d) are the PVTEM images of dislocations in the plane of a QD and a QW laser after aging for the same time, respectively. Clear dislocation network has been developed in the QW laser[34]. 12

Figure 8: (a) Theoretical normalized threshold current with respect to temperature. For a 0D particle, the threshold current is expected to be independent of temperature[31]. (b) L-I characteristics of the QD laser from 30 to 220 °C under CW operation with HR coatings on both facets[44]. (c) Energy band diagram of 1.3 μm InAs QD grown on GaAs embedded in a 6 nm $In_{0.15}Ga_{0.85}As$ QW matrix[45]. 13

Figure 9: (a) Threshold current density and its components with respect to temperature. Inset: zoomed in j_{QD} and j_{OCL}. j_{QD}=j_{OCL} at 344 K; the dotted line represents j_{QD} calculated on the assumption of charge neutrality in QDs. (b) Characteristic temperature limited by the excited state recombination and VCN in QDs. 15

Figure 10: (a) Combination map between Δinh, N_p, and G_{th} for $|\alpha_H(\nu_{pk})|_{min}$ (b) $|\alpha_H(\nu_{pk})|_{min}$ obtainable with these combinations[35] 17

Figure 11: (a) Optical (upper) and RF (lower) spectra of the QD lasers on Si as a function of the feedback level. (b) Optical (upper) and RF (lower) spectra of the QW lasers as a function of the feedback level. The maps were obtained at an injection level of $3\times I_{th}$[64]. 18

Figure 12: Normalized signal power versus probe power in a probe-drive laser experiment for (a) undoped and (b) p-doped lasers. The frequency detuning, Δ, corresponds to the same mode number difference. Dashed lines are calculated from multimode laser theory and the solid lines are the calculated from selected ξ values. 19

Figure 13: (A) TDD of the post-TCA GaAs-on-Si template. The minimum TDD achievable via TCA at the given GaAs thickness is about 3×10^7 cm^{-2}. (B) Nomarski microscope image of the GaAs surface after annealing above and below 745 °C pyrometry temperature. Gallium droplets are observed when T_{max} is higher than 745 °C. (C) ECCI images of the as-grown GaAs with no TCA (top) and after 16 cycles of TCA (bottom). The TDD is about 4.18×10^8 cm^{-2} with no TCA and decreases to $3\times10^7$$cm^{-2}$after extensive TCA. 24

Figure 14: (A)-(D) Representative ECCI images of the SLS sample with GaAs layer thickness, x = 10, 5, 2, and 0, respectively. The insets are zoomed ECCI images showing clear TDs in the white circles. The scale bar in the insets is 1 μm. The surface TDD is much lower in the sample with a continuous 200 nm $In_{0.15}Ga_{0.85}As$ filter. (E)-(H) Nomarski microscope images of the sample with x = 10, 5, 2, and 0, respectively. Surface crosshatch and FTs are more obvious with thinner GaAs in between the $In_{0.15}Ga_{0.85}As$ layers. (I)-(L) RSMs of the sample with x = 10, 5, 2, and 0, respectively. The SLS is more relaxed as x decreases to 0. 28

Figure 15: TDD and degree of relaxation of the SLS as a function of GaAs layer thickness in between the $In_{0.15}Ga_{0.85}As$ layers. The SLS with no GaAs layers (x = 0) is about 3 times more relaxed than x = 10 case. The TDD is much lower in the sample with a higher degree of relaxation in the SLS. Though TDD is low for x = 2 and x = 0 cases, FTs are observed on top of the GaAs capping layer. 29

Figure 16: Schematic illustrations of the expected TD motion in (A), (C), and (D), and qualitative strain states in (B), (D), and (F), at different stages of relaxation within a SLS structure. Not all periods are drawn for simplicity. Tensile relaxation

in the GaAs layers is expected to happen later during growth as no strain energy is accumulated in the first few periods of the SLS. Thus, the tensile strain would hinder the relaxation process.....31

Figure 17: (A) TDD measured before and after GaAs capping layer with a single 200 nm InGaAs filter. The TDD starts to increase once the indium composition in the InGaAs layer is above 20%. The inset shows an example Nomarski image of samples with more than 20% of indium in the InGaAs filter layer. No large enough clear regions for ECCI measurements. (B) Example ECCI image of sample with more than 20% indium in the InGaAs layer before GaAs capping. "Blocked" TDs are circled.....32

Figure 18: (A) The experimental sample structure for the proposed "asymmetric step-graded filter" with maximum indium content of 10%. The plot to the left of the schematic structure shows the indium composition of each layer with respect to the distance measured from the top of the GaAs-on-Si template. (B) Representative ECCI image of the structure showing a TDD of 2×10^6 cm^{-2}. (C) RSM of the annealed structure shows 88.9% relaxation in the $In_{0.05}Ga_{0.95}As$ layer and 58% relaxation in the $In_{0.10}Ga_{0.90}As$ layer with respect to GaAs. 34

Figure 19: Bright field STEM images of the asymmetric graded filter structure with annealing at each InGaAs layer. (A) XSTEM showing the graded filter layers, with **g** = **220**. The top GaAs layer appears to be TD free. (B) and (C) PVSTEM on different areas, imaged in a (220) two-beam condition. MD arrays are shown due to the tilt of the foil with respect to the sample surface. An area of at least 65 μm^2 appears to be TD free.....35

Figure 20: (a) The MD elongates to relax the compressive strain during growth and the TD segment glides through the crystal. (b) During cooling, MD shortens in length to partially release the tensile strain. The TD segment thus experiences a "reverse-glide" process[118].....39

Figure 21: (a) Formation process of the MD touching the active region. (b) Defect configuration with the inserted InGaAs QW as the trapping layer. Monochromatic cathodoluminescent of the QD ground state emission (c) without and (d) with the inserted trapping layer[111].....40

Figure 22: Tomographic reconstruction of a laser stack with TLs inserted in the top (p-side) and the bottom (n-side) cladding layers. 1 out of 7 MDs on the p-side has escaped the trapping effect. It is also observed that p-side has noticeably more MDs than the n-side[122].....41

Figure 23: (a) Schematic illustration of the possible bypassing effect, leaving a new MD near the active region. (b) Contour maps of the calculated τex for a range of t_s and t_{TL}. The "safe-zone" ($\tau ex < 0$) is much bigger for the case with lower thermal strain[118].....42

Figure 24: Schematic illustration of the tradeoff between TLs placed (a) closer and (b) further away from the active region. 42

Figure 25: (a) Cross section SEM of an as-grown epi stack with a TDD < 1×10^{6} cm^{-2}. (b) A sample that didn't crack after cooling, yet experience server cracking after oxide hard mask deposition. 43

Figure 26: (a) Flat GaP-on-Si template before growth. (b) Deposition of III-V (blue) causes the sample to curve due to the compressive stress. (c) The compressive stress is relaxed through defect formation. (d) Crack formation as the film stress state is reversed and there are not enough defects to help release the tensile strain. (e) Deposited oxide hard mask (green) would tend to bend the sample backward, which causes more severe crack situations. 44

Figure 27: Buffer structures with a surface TDD of (a) 4×10^{8} cm^{-2}, (b) 3×10^{7} cm^{-2}, and (c) 1×10^{6} cm^{-2}. The red dashed lines in (b) and (c) indicate where TCA was applied. (d)-(f) are the ECCI images of the corresponding buffer structures above. (g) Schematic of the laser stack with varying aluminum composition and thickness of the top and bottom cladding layers. 46

Figure 28: (a) Post-cooling wafer curvatures with respect to the TDD, epi thicknesses, and cooling rates. The horizontal lines indicate the lowest possible radius of curvature for both the thin (blue) and the thick (red) epi design estimated from the Stoney's formula (b) Cracks were observed in orthogonal directions when the thick epi is quenched on a 1×10^{6} cm^{-2} TDD template, (c) while only cracks along the [1 -1 0] direction were observed when the same structure was cooled slowly. (d) Such cracks penetrate all III-V layers with the Si substrate still intact. 47

Figure 29: ERRs, obtained from the stresses computed from wafer curvature measurements, for isolated channeling cracks as a function of cooling rate, for three dislocation densities. 54

Figure 30: (a) Stress as a function of cooling rate, for three dislocation densities, with wafer curvature results superimposed. (b) Contour map of predicted energy release rate as a function of dislocation density and cooling rate; conditions above the critical line are expected to crack, while those below the line are not expected to crack. The predicted stresses are higher than those observed for the middle of the top row, such that cracking is predicted despite observations to the contrary. (c) The contour of the critical film thickness for crack formation with respect to the dislocation density and the cooling rate for the given film toughness. 55

Figure 31: Bias change for 10 mW output power aged at 80 °C for bonded QW lasers. 59

Figure 32: (a) Room temperature aging data for the epitaxial QD lasers on Si with three different levels of TDD. (b) 60 °C aging data. The Gen III laser lifetime dropped from >100 years to ~6000 hours. Introducing p-MD brought increased the lifetime to about 8 years due to improved differential gain at higher temperatures. 59

Figure 33: (a) Detailed schematics of the three on-Si lasers grown. Sample A is the previous best laser structure with a TDD of 7×10^6 cm^{-2} and no TLs. Sample B has the same TDD but with TLs inserted and Sample C has a TDD no more than 1×10^6 cm^{-2} and TLs inserted. (b) Room temperature PL spectrum of the as-grown lasers. 61

Figure 34: (a) and (b) are representative LI curve of the best performing devices. (c)-(e) are the comparisons between devices from different epi designs on threshold currents, slope efficiencies, and characteristic temperatures, respectively. 61

Figure 35: (a) Net modal gain as a function of injection current density and (b) transparency current density as a function of wavelength on one as-cleaved device from each sample. 63

Figure 36: (a) The front of the aging system. Each CMM holds four fixtures. (b) The back of the aging system. 64

Figure 37: Zoomed in views of the individual fixtures. (a) The drawer-like configuration of the fixture; (b) the removable top cover and (b) the singulated devices on mounted carriers. 64

Figure 38: (a), (b), and (c) are LI evolutions for the lasers from Sample A, B, and C aged at 80 °C, respectively. The lasers from Sample A have experienced a threshold current increase of 104% within 4000 hours and Sample B has seen a 27.6% increase. The threshold currents of the best devices from Sample C have only increases by 10.4%.....66

Figure 39: Indium growth rate/InGaAs composition calibration with XRD. Five different Indium fluxes were used while keeping the Ga flux the same. RSMs confirmed that the InGaAs layers were 100 % strained. The plot of the In growth rate vs. flux should be linear. 69

Figure 40: (a) Schematic of the hetero-epitaxial laser integration on Si (HELIOS) platform. (b) Butt-coupling configuration with double SiN core and Si waveguide. (c) The simulated coupling efficiency with respect to the gap between the laser and the nitride cores and the core width. (d) Proposed full epi stack for the in-trench optical gain. 71

Figure 41: On-chip gain for (a) optical communication and (b) solid state LiDAR system. 72

Figure 42: (a) The initial template with oxide fences in different directions and width. (b) Close up SEM images of the oxide fence with Ge deposited on the Si surface. (c) Cross-section SEM image after depositing 100 nm GaAs. (d) and (e) are cross-section SEMs after depositing 1 um GaAs. 73

Figure 43: (a) Nomarski top-down image and (b) cross-section SEM image after depositing 1 μm GaAs on the Ge/Si template. Non-selective polycrystalline III-V material is clearly visible. 74

Figure 44: (a) Illustration of the PSE process. Both Group III and Group V fluxes are supplied during the deposition time (τd) and only Group V flux is supplied during the desorption time (τint). The The τint is normally longer than τd. Group V flux is there to protect the crystalline surface inside the trench. (b) Schematic of the adatom actions during the desorption time. 75

Figure 45: Continuous deposition with 0.1 μm/h and 40 V/III ratio at (a) 630 °C, (b) 600 °C), and (c) 580 °C. PSE deposition at 630 °C with a growth rate of 0.1 μm/h and a V/III ratio of (d) 450, (e) 100, and (f) between 10 and 40. Compared with the previous results, it seems the growth temperature and growth rate control the selectivity and V/III control the crystal quality. PSE relaxes the requirements of growth rates and growth temperature for perfect selectivity.....76

Figure 46: Pyrometer temperature profiles with respected to the heater thermal couple setting measured on GaAs substrate, on oxide patterned Si wafer, and on polycrystalline III-V deposited on the oxide mask. The red horizontal line the QD growth temperature on GaAs. Thus, if the temperature calibration is done on the oxide, the actual III-V temperature would be well-above 550 °C, which would evaporate the QDs. 77

Figure 47: (a) All the proposed trench architectures. The top is for the test growths and the bottom is for the full device build. (b) An example coupon with trenches in both horizontal and vertical directions with different widths and lengths. 78

Figure 48: (a) and (b) are cross-section SEM images for the as-grown GaAs film. The thin GaP layer is clearly visible, and the GaAs film thickness is as designed across all trenches regardless of the width. (c) and (d) are PVTEM images taken 800 nm below the surface and on top of the surface and, respectively.....79

Figure 49: (a) and (b) are the top-down SEM of the as-grown initial 1.6 μm GaAs. The surface morphology in the horizontal trench is slightly rougher. (c) and (d) are the post-TCA surface morphology of the same sample. The surface of the GaAs within the horizontal trench is significantly rougher than the one in the vertical trench. 80

Figure 50: (a) Cross-section SEM if the post-TCA in-trench GaAs film. Though the polycrystalline on the oxide wall has been removed, the in-trench material has been partially removed as well. (b) Schematic illustration of the hypothesis of how the III-V is evaporated. 81

Figure 51: (a) Cross-section TEM of the in-trench full stack. (b) The raw EDS data scanned across the InGaAs graded filter layers. (c) The extracted indium composition profile.....82

Figure 52: Zoomed in XTEM around the active region for (a) foil normal perpendicular to the trench long edge and (b) foil normal parallel to the trench long edge. 83

Figure 53: (a) and (b) are the PL sample structures for the 1300 nm QD and 1178 nm QD, respectively. (c) and (d) are the room temperature PL spectrum for the corresponding sample structures. (e) and (f) illustrate the deposition profile of InAs. The red arrows point to when the on-set of nucleation was observed in RHEED for the corresponding structure. 86

Figure 54: (a) The room temperature PL spectra of the four different scenarios. The number labels correspond to the Sample No. in Table 2. The red vertical dotted line denotes the target 1178nm wavelength. (b) and (c) are the schematic illustrations of the split and the continuous capping sequence, respectively.....87

Figure 55: (a) and (b) are the initial and the proposed deposition sequences of the InAs QDs on bare GaAs surface, respectively. (c) Room temperature PL spectrum of samples with different number of post-nucleation bursts. The black curve is the reference sample with the original deposition sequence. The numbers on the curves indicate the number of bursts used. The vertical red dotted line is the target wavelength. (d) Extracted emission wavelengths with different number of bursts. The horizontal dotted line indicated the target wavelength. (e) Schematic of the dot with elastic strain relaxation. 89

Figure 56: Room temperature PL of the 1178 nm InAs QDs. The inset shows the AFM image of the QDs. The surface QD density is about 3×10^{10} cm^{-2}.....90

Figure 57: (a) PL spectrum of the growth temperature series. The vertical red dotted line is the target wavelength. (b) Extracted emission wavelength vs. growth temperature. (c) Extracted FWHM and energy separation vs. growth temperature. 91

Figure 58: (a) Cross-section SEM of the as-cleaved FP lasers with a shallow etch ridge. (b) Temperature dependent LI curves. CW operation is maintained to 45 °C. (c) Room temperature spectrum of the cleave/cleave and the HR/cleave devices. 92

Figure 59: (a) and (b) are the SEM images of the etched gratings for the DFB laser emitting at 1178 nm. 93

Figure 60: (a) PL structure used to optimize the growth conditions for 1550 nm InAs Qdashes. DA stands for “digital alloy”. The structure is finished with uncapped Qdashes for morphology study. (b) A typical AFM scan showing the Qdash morphology. 94

Figure 61: Qdash formation process. (a) the initial nucleation center with shallow facets and close-to-square base; (b) attachment of the adatoms to the existing nucleation sites from both the [1 1 0] and [1 -1 0] directions; (c) islands elongated along the [1 -1 0] direction formed due to a higher surface diffusion; (d) shorter and rounder islands form during the post growth annealing process in reaction to the high residual strain in the elongated dashes. 94

Figure 62: (a) AFM scans of the uncapped surface Qdashes with different GI time[142]. (b) Room temperature PL of the corresponding GI time.....96

Figure 63: (a) Schematic of the laser epi stack. All quaternary alloys were grown digitally. (b) LI curve comparison between the perpendicular and the parallel ridge configuration. (c) The extracted threshold current density and the maximum output power for the two different ridge configurations.....97

Figure 64. (a) Schematic diagram of the fabricated waveguide photodetector. (b) Top-view and (c) cross-sectional views of the fabricated device. 97

Figure 65: (a) Temperature dependent measurement of the Current-voltage characteristics of a 30 × 50 μm^2 device. Inset: Arrhenius plot of temperature dependent dark current at -1 V.....98

Figure 66: Dark current density as a function of (b) the device area and (c) the device perimeter/area for a series of devices with a fixed PD mesa length of 50 μm at room temperature. 99

Figure 67: SEM images of the fabricated device. Top-view (a) and cross-sectional views (b), (c) of a fabricated microring laser. Highlighted color sections: red, microring laser (a) and active region (b); blue, III–V; yellow, selected metal contacts. 100

Figure 68: (a) Light-current-voltage characteristics, inset: LI curve in the log-log scale. (b) Zoomed-in view of the spectrum taken at 50 mA. (c) Emission spectra at increasing injection currents of a micro-ring laser with a radius of 100 μm and a ring width of 4 μm under CW operation at room temperature. (d) Micro-ring laser with a radius of 100 μm and ring width of 4 μm shows continuous-wave lasing up to 55°C. (e) Plots of threshold current versus stage temperature for four different laser devices with various outer-ring radii. Inset: extracted characteristic temperature T_0 as a function of outer-ring radius. 101

Figure 69: (a) Schematic of the buffer structure with ASG filter. (b) Example PVTEM measured on top of the GaAs capping layer. (d) Schematic of the full laser stack with inserted TLs. The materials were chosen to minimize the band offset. (d) XTEM with [0 0 1] surface normal. P-side appears to have more MDs than the n-side. (e) Zoomed-in view on the active region, showing that the MDs are effectively blocked away from the active region. 105

Figure 70: Reintroduced aging results of the bonded QW lasers at 80 °C after 25000 hours. The solid red line roughly depicts the change in the bias required for 10 mW output power in the best epitaxial QD lasers. 105

Figure 71: PVTEM image of a QD laser active region. The yellow arrow points to an example MD. The “coffee-bin” contrasts are the QDs. 107

Figure 72: Projected global biosensor market in the next few years. 108

Figure 73: Water absorption spectrum suggesting that a light source working around 500-600 nm would be ideal.....109

Figure 74: Example architecture of an on-chip biosensor. The laser was picked and glued onto the platform with photonic wire bonds (PWB) connecting the laser to the sensor waveguides. A monolithic light source via direction epitaxy would greatly reduce the cost and improve scalability.....110

Figure 75: Schematic of a QD quantum light emitter coupled to a resonant cavity to improve extraction efficiency.....110

LIST OF TABLES

Table 1: Cost per area and maximum available size of GaAs, InP, Si, and SOI wafers. 4

Table 2: Sample thicknesses, compositions, cooling rates, post cooling curvatures, and measured crack density of all 9 samples investigated. 47

Table 3: Material parameters used in the calculations obtained from the reported values. 52

Table 4: Summary of the main aging results in the last few years[53,86,122,133]. 66

Table 5: Four test conditions on the GaAs capping layers and the resulted PL qualities are summarized. 88

Abstract

Robust High Temperature Operation of Quantum Dot Lasers Grown on Silicon

by

Chen Shang

Epitaxially grown quantum dot (QD) lasers are emerging as an economical approach to obtain on-chip light sources. Thanks to the three-dimensional confinement of carriers, QDs show greatly improved tolerance to defects which makes them the ideal candidate for the optical gain medium in monolithically integrated on-chip light source and promises other advantages such as low transparency current density, high temperature operation, isolator-free operation, and enhanced four-wave-mixing. These material properties distinguish them from traditional III−V/Si quantum wells (QWs) and have spawned intense interest to explore a full set of photonic integration using epitaxial growth technology.

By reducing the threading dislocation density to less than 1.5×10^{6} cm^{-2} and blocking misfit dislocations near the active region with newly introduced defect management tools, the extrapolated lifetime of the epitaxially grown QD lasers on CMOS compatible (001) Si substrate has been boosted to more than 200,000 hours at 80 °C under CW operation. Unfortunately, as the III-V films become less defective, they are more brittle and subject to crack formation, and wafers experience higher deflection due to higher residual tension from the coefficient of thermal expansion mismatch. To ensure wafer manufacturability and device yield, thinner stack design with material having less thermal expansion mismatch with the Si substrate is of great importance.

In parallel, the attempts to deposit the stack in the pre-patterned pockets on Si photonic chips for monolithic integration have been initiated. Despite the lack of *in situ* temperature and surface quality monitors due to the covered oxide, blanket-substrate level film quality has been achieved with low crystalline defect density. The stress asymmetry introduced by the pocket geometry would potentially introduce another design space for defect management. Preliminary observations suggest that a proper alignment of the crystallographic orientation to the pocket geometry could eliminate the misfit dislocations near the active region by fundamentally lowering the residual tensile stress. Combined with the more optimized defect management tools, epitaxially grown QD lasers with lifetime comparable to the commercialized bonded QW laser on Si may finally be on the horizon.

Table of Content

Chapter 1 Introduction 1
Chapter 2 Fundamentals of Quantum Dots 7
2.1 Discrete density of states 9
2.2 Insensitivity to defects 11
2.3 Improved temperature dependence 13
2.4 Reduced linewidth enhancement factor 15
2.5 Enhanced four wave mixing 18
2.6 Summary 19
Chapter 3 Obtaining thin and low defect virtual substrates on (001) Si 21
3.1 Challenges 21
3.2 Limit of TCA 23
3.3 Dislocation filter efficiency 26
3.3.1 Efficiency of InGaAs/GaAs strained layer superlattice 27
3.3.2 Effect of indium content in the InGaAs dislocation filter layer 32
3.4 Proposed more efficient filter structure 33
3.5 Summary 35
Chapter 4 The monster hiding in plain sight: CTE mismatch 37
4.1 Formation of MDs near the active region 38
4.2 Suggested optimization of the trapping layer design 40
4.3 Cracking and wafer warping 43
4.3.1 Experimental procedure and results 44
4.3.2 Mathematical model 49
4.3.3 Results and discussion 53
4.4 Summary 56
Chapter 5 Breakthrough reliability at elevated temperatures 58
5.1 New generation of QD lasers on Si 59
5.2 Aging experiment setup and results 63
5.3 Proposed new laser design 67
5.4 A short note on growth calibration 68
5.5 Summary 70

Chapter 6 Toward Monolithic Integration with Si Photonic Circuits 71
6.1 Initial attempts 72
6.2 Temperature discrepancy 76
6.3 High crystalline quality 78
6.4 Summary 84
Chapter 7 Extending QD technology to other wavelengths 85
7.1 1178 nm QD laser on GaAs 85
7.1.1 Growth development 85
7.1.2 Device demonstration 92
7.2 1550 nm Qdash laser on InP 93
7.2.1 Growth 93
7.2.2 Device demonstration 96
7.3 Summary 102
Chapter 8 Summary, future work, and other interesting applications 104
8.1 Approaching the heterogeneously integrated QW laser performance 104
8.2 Interesting new directions 108
8.2.1 Monolithic on-chip light source for photonics biosensors 108
8.2.2 QDs as ideal quantum light emitters 110
8.3 Conclusions 111
Reference 113

Chapter 1
Introduction

There are approximately 5 billion people and 30 billion devices connected to the Internet. The global Internet traffic has well-surpassed the zettabyte threshold (2^{70} bytes) and has reached 3 times the threshold in 2020 with a compound annual growth rate of at least 25%[1,2]. This calls for high-density, high-speed, and broadband data interconnects at a low-cost for signal processing and high-performance computing. The three key metrics for future interconnect technology are bandwidth density, energy efficiency, and low latency. At the present rate of progress, electrical interconnects with copper wires are not going to fulfill the demand in the next decade[3]. The bandwidth of the conventional inter-chip interconnects with electric wires is limited due to the low channel line rate and low I/O pin density, and thus low bandwidth density. There are currently no known solutions to improve the line rate with electrical interconnects on a PCB. The maximum length of the electric wires is also limited due to their high transmission loss on the PCB and reflections at connectors.

On the other hand, optical interconnects with photonics are a promising technology to manage the rapid increase of data demand as optical signals inherently have wide bandwidth, low latency, low power consumption, and low mutual interference, compared with those of electrical signals. Photonic technologies are not only useful in datacom and telecom applications with high bandwidth data transmission, but also in navigation, spectroscopy, optical clock, biosensing and imaging, and many other applications. Yet, the photonic devices have remained bulky and too expensive to be used in PCs and servers to replace electric wires. In that sense, Si photonics was introduced. In analogy to

the historical scaling of Si-based electronics in CMOS technology governed by "Moore's Law", integration of photonic components allows the optical systems to be developed in compact form factors. Leveraging the well-established CMOS process control and 300 mm Si wafers, photonics components could be manufactured with high volume, high yield, low cost, and high integration density. The system miniaturization enables new applications: the deployable gas and biomolecular sensing systems, compact solid-state LiDAR for automobiles, and on-chip gyroscopes, etc.

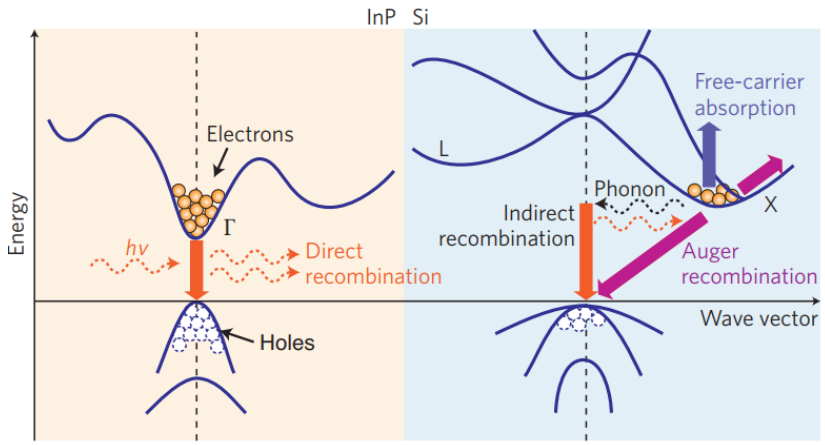

Figure 1: Left panel shows the stimulated emission process in InP, a typical direct bandgap semiconductor. The right panel shows that the recombination process requires phonon participation in an indirect bandgap semiconductor, i.e. Si.

Si is suitable for photonics applications as the Si crystal and its native oxide are transparent in telecom and datacom wavelengths. The high refractive index contrast also ensures excellent optical confinement. In combination with Ge, Si_3N_4, and other dielectrics, waveguides covering optical wavelengths from ultraviolet to infrared could be designed on silicon-on-insulator substrates. Unfortunately, Si and Ge are indirect bandgap materials, which make them poor light emitters as a momentum transfer through phonon emission is required, schematically illustrated in Figure 1. Consequently, the best Group-IV laser has a threshold currently density of[4] 300 kA/cm^2, which is about four orders of magnitude larger than what could be achieved with direct bandgap III-V materials. The other downside of Si and Ge is that they can only cover wavelengths around near-infrared for modulation and detection.

Thus, integrating III-V materials with Si photonic platforms is the go-to approach to achieve a fully functional Si photonic integrated circuit. Currently, heterogeneously integration through wafer bonding, introduced in 2006[5], is the only approach that has received mass commercial production and Intel is producing optical transceivers in volume using heterogenous integration. Compared to the hybrid integration approach, where extremely precise alignment is required for butt-coupling during packaging, the alignment is greatly simplified as it's done in the lithographic steps and the light is evanescently coupled to the Si waveguide below. Heterogenous integration on Si can accommodate not only III-V materials for gain, detection, and modulation, but can also include more exotic materials, e.g. $LiNbO_3$ and Ce:YIG for high performance modulators, nonlinearities, and magnetic properties.

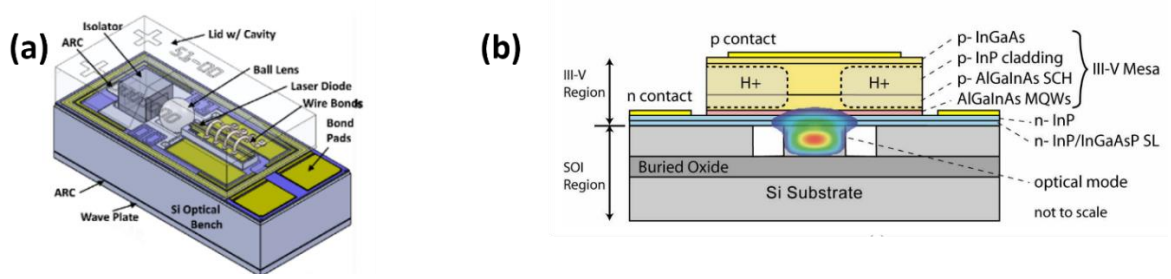

Figure 2: Schematic illustration of (a) hybrid and (b) heterogenous integration.

Despite all the obvious benefits of heterogenous integration approach, the associated technical complexity is still considerable, in particular the stringent requirements of the extremely clean and smooth III-V surfaces. Moreover, the heterogeneously integrated light sources may consume considerable real estate on the Si photonic chip and heat sinking is challenging due to the high thermal resistance introduced by the bonding layer and the buried oxide. Economically, the potential low-cost model of Si photonics is based on the hypothesis that the work could be done on the full surface of 300 mm SOI wafers. Yet the maximum available size of the III-V wafers is not suitable to fulfill this requirement (200 mm for GaAs, 150 mm for InP). Also, since the III-V material is only required on

a smaller portion of the device area, most of the III-V wafer is lost by the layer patterning on the required areas. The cost of III-V materials is much higher than Si and SOI wafers. Such material waste potentially puts a substantial overhead on the overall cost.

Table 1: Cost per area and maximum available size of GaAs, InP, Si, and SOI wafers.

	GaAs	**InP**	**Si**	**SOI**
Substrate cost($/cm^{-2})	1.65	4.55	0.20	1.30
Maximum diameter (mm)	200	150	450	450

To further reduce the cost of integration and fully utilize the economy of scale of CMOS manufacturing, monolithic integration via direct epitaxial growth is considered as the ultimate solution. The need for III-V wafers and the bonding process will then be eliminated. The epitaxy architecture also provides the best natural heat sinking for laser operation as the III-V material is covalently bonded to the Si substrate. Yet, due to the dissimilarities between non-nitride III-V and Si, namely the polarity mismatch, lattice constant mismatch, and thermal mismatch, high density electrically active crystalline defects are generated during hetero-epitaxial growth. The polarity mismatch, which results in the formation of antiphase domains, has largely been solved. Threading dislocations (TDs) with a density of 10^9~10^{10} cm^{-2} at the III-V/Si interface could be generated as the III-V film relaxes in response to the lattice mismatch. The TD density (TDD) drops as the film thickness increases, yet the lowest TDD values previously reported with a reasonable film thickness are in the high-10^6 cm^{-2}. A new design that further reduces the TDD to no more than 1×10^6 cm^{-2} will be discussed in Chapter 3. The coefficient of thermal expansion (CTE) mismatch is known to cause wafer warping and film cracking. It was recently discovered that the CTE is also responsible for the

formation of misfit dislocations (MDs) near the active region. A new tool to remove the MDs and a mathematical model that provides guidance in future epitaxial design to reduce cracking/warping will be introduced in Chapter 4.

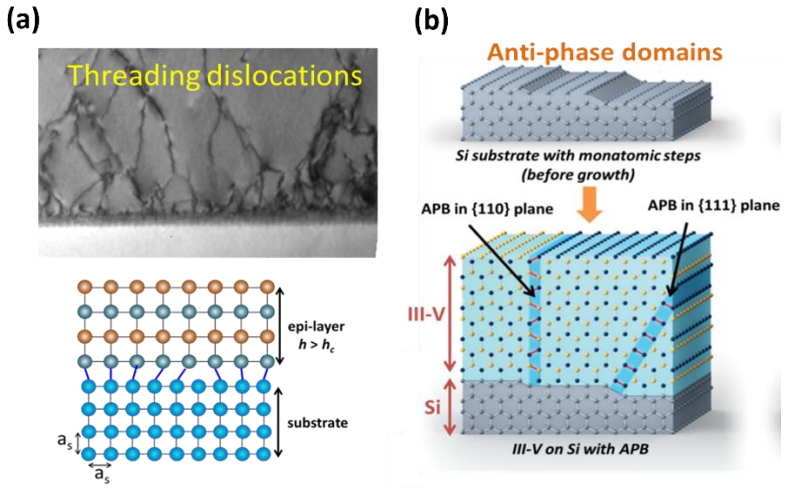

Figure 3: Common crystalline defects of (a) threading dislocations from the plastic relaxation due to the lattice mismatch and (b) anti-phase domains formed at the step edges of the Si substrate due to polarity mismatch.

Due to these inevitable crystalline defects, the best QW lasers perform poorly with lifetimes of just 1000 hours, insufficient for commercial applications[4]. To achieve native substrate laser performance and reliability, an active region with quantum dots (QDs) is adopted for their insensitivity to defects as the carriers are confined within the local potentials. Other inherent advantages of QDs over QWs will be discussed in Chapter 2. Chapter 3 introduces a new type of dislocation filter structure that results in ultra-low defect density GaAs virtual substrate on Si and Chapter 4 taggles the issues with CTE mismatch: MD trapping layers are introduced, and a mathematical model is developed to describe and solve the film cracking and wafer warping problem. Together with use of the newly introduced defect management techniques, record breaking reliability of the epitaxial QD lasers emitting around 1300 nm has been achieved in Chapter 5 with an extrapolated lifetime > 200 k hours at 80 °C. The attempt to deposit such high-quality laser epi in the pre-patterned Si photonic chip for

true monolithic integration is summarized in Chapter 6. A short note on the development of QD lasers emitting at 1178 nm for optical clock and 1550 nm for long haul communication can be found in Chapter 7. Finally in Chapter 8, proposed future work for obtaining native substrate level reliability on Si is introduced. Applications of such high performance monolithic on-chip light sources in the near future are briefly discussed in the thesis finale.

Chapter 2
Fundamentals of Quantum Dots

For the past 40-ish years, epitaxial QDs have been the subject of intense research interest in physics, materials science, and electrical engineering for their unique and highly tunable properties, and such efforts have fueled the realization of numerous optoelectronic applications. Historically in the early 90s, before the introduction of the self-assembled QDs, three-dimensional confinement was achieved either by fabricating narrow pillars with a small disc of a quantum well (QW)[6–8] or by depleting carriers from specific regions of the underlying QWs with electrostatic gates on the sample surface[9–11]. It was the etched pillar approached that coined the term "Quantum dots". These two approaches allow the precise placement of the QDs but are potentially expensive and time consuming for the required complicated post-growth processing. The other problem is that the maximum QD density (~ 10^8 cm^{-2}) practically achievable with these two approached is much lower than the required density (> 10^{10} cm^{-2}) for efficient QD-based light emitters[12]. The surface recombination and the variable size with these "fabricated dots" also make them less appealing to real applications.

The self-assembled QDs inherently provides a straightforward approach to realize the required QD surface density and requires no post-growth processing to define the dots. Yet, the growth process that resulted in the formation of these 3D crystal islands was not originally designed to create these QD light emitters. It's been known since the early 80s that certain combinations of film and substrate would start with a smooth growth front and transition to 3D island formation after reaching the critical

thickness. This growth mode is known as the Stranski-Krastanov (SK) growth mode[13], typically demonstrated in Ge-on-Si and $In_xGa_{(1-x)}As$-on-GaAs systems with large lattice mismatch[13,14].

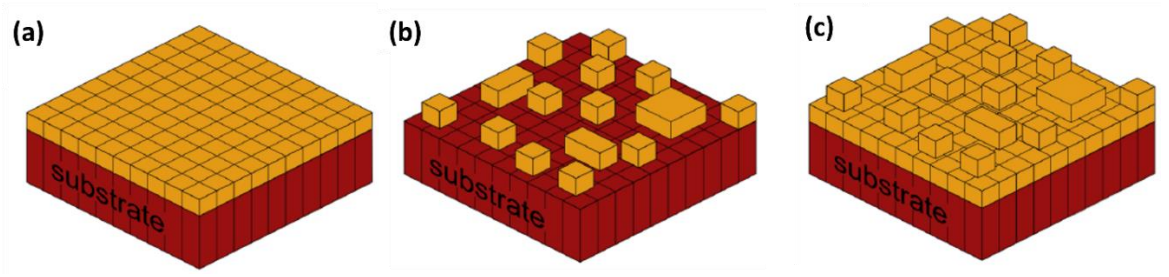

Figure 4: Growth modes are generally determined by the relationship between surface free energies of the film-vacuum interface γ_e, the film-substrate interface γ_i, and the substrate-vacuum interface γ_s. (a) Frank-van der Merwe growth mode: $\gamma_e + \gamma_i < \gamma_s$. (b) Volmer-Weber growth mode: $\gamma_e + \gamma_i > \gamma_s$. (c) Stranski-Krastanov growth mode: the film initially wets the substrate as in the FWM growth mode, and transition to 3D islands after building up enough strain energy (APL tutorial).

There were considerable efforts to suppress the formation of the self-assembled islands as they indeed would roughen the surface[15–18]. The attitude toward these nanoparticles took a 180 ° turn once researchers realized that these islands were dislocation free despite the high lattice mismatch between the film and substrate[19–21], and the spatial extent of electronic wave functions in these islands were smaller than the Bohr exciton diameter[22,23]. Thus, these 3D islands could behave as optically active QDs trapping carriers in all 3 dimensions when buried in a wider bandgap material. Since then, self-assembled QDs as light emitters have been demonstrated on various types of material systems, from Group IVs[14] to III-Vs[13,24–28] and to II-VIs[29,30], among which InAs QDs on GaAs is the most mature system for datacom and telecom laser applications. Leveraging from the promised lower threshold current and high temperature operation[31], high performance InAs QD lasers operating around 1310 nm have been demonstrated. Expected low sensitivity to crystalline defects and to optical feedback are the two most important advantages of QDs over QWs due to the stronger carrier localization, making QDs the ideal candidate for realizing high performance light sources epitaxially grown on Si and eliminating optical isolators within the integrated package. In the next sections, the physical

principles of the fundamental advantages of QD lasers for telecom and datacom applications will be briefly discussed.

2.1 Discrete density of states

When the extent of the electronic wavefunction, in any direction, of a semiconductor structure is reduced to smaller than the Bohr exciton diameter, energy quantization happens[12]. Unlike QWs, where this quantization occurs only in one-dimension, typical InAs QDs on GaAs experience energy quantization in all 3 dimensions, resulting in a series of discrete delta functions for their density of states when surrounded by higher bandgap matrix materials. Thus, QDs are also considered as "artificial atoms" with tunable energy states[32].

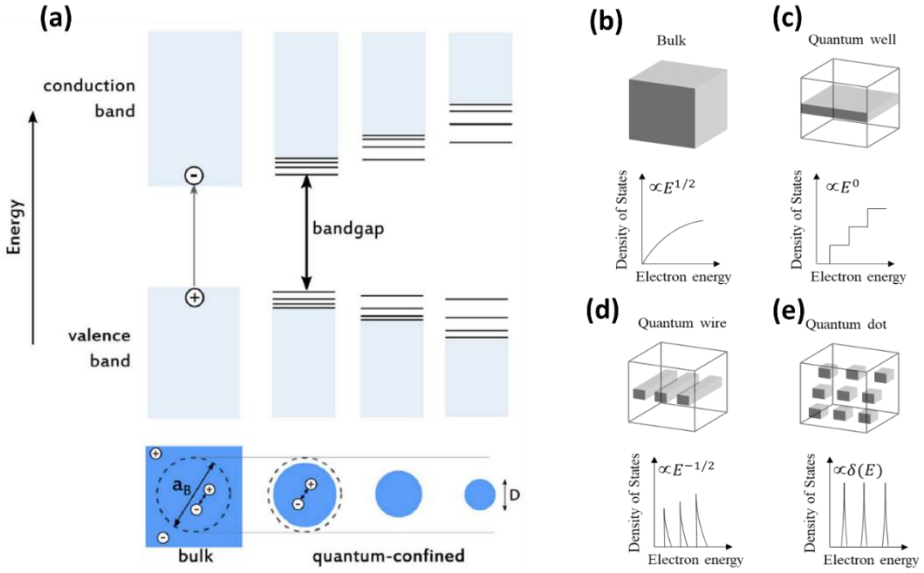

Figure 5: (a) Energy quantization occurs when the spatial extent of the electronic wave functions is smaller than the Bohr exciton diameter (a_B). The bandgap and the energy spacing between the states can be tuned with the QD diameter (D)[33]. (b)-(e) Schematics of the 3d, 2d, 1d, and 0d structures and their corresponding density of states, respectively.

In practice, self-assembled QDs grown via the SK growth mode experience inhomogeneous broadening due to growth variations, mostly in size and composition, and are connected through a thin wetting layer[34]. Figure 6a shows the example room temperature photoluminescence (PL)

spectrum of InAs QDs grown on a GaAs substrate with labeled ground state (GS), the first excited state (FES) and the second excited state (SES). The measured full-wave-at-half-maximum (FWHM) of the ground state peak is 28 meV, which translates to an inhomogeneous broadening Δ_{inh} of approximately 14 meV[35]. This value of Δ_{inh} for typical self-assembled QDs is small compared to the energy separation between the quantum states (around 80 meV) [35,36]. Thus, the states in the QD ensemble remain discrete, resulting in a clearly distinguishable GS and FES. With this discrete density of states, the carrier density required for population inversion is reduced. Therefore, the short carrier lifetime of the ground state supports a high level of radiative optical transitions per unit volume. This mechanism contributes to a low threshold carrier density. Figure 6b shows the calculated and measured modal gain for an older generation of QD and QW lasers. This suggests that an InAs QD active region with all QDs having the same size ($\Delta_{inh} = 0$) is highly desirable, yet such task might be close to impossible[36].

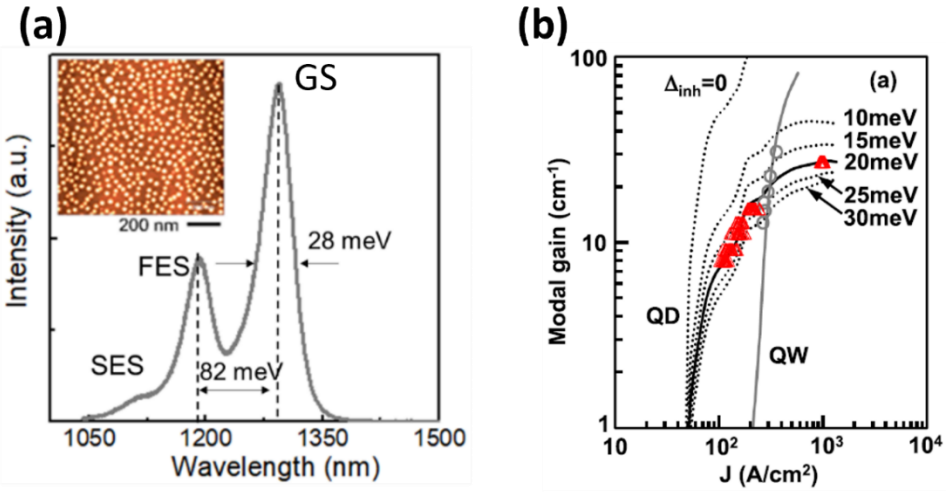

Figure 6: (a) Example room temperature PL of InAs QDs emitting around 1300 nm. The inset shows the exposed QDs morphology with a surface density of approximately 6×10^{10} cm^{-2}. (b) Calculated modal gain of QDs and QWs with respect to the injection current density. The red triangles and the grey circle are the measured values for QD and QW lasers, respectively. The case with $\Delta_{inh} = 20\ meV$ matched with the experimental results[36].

The inevitable finite inhomogeneous broadening is beneficial in a QD optical amplifier. Since each QD can only experience stimulated recombination at its local energy, the amplification produced by one dot is independent from other dots in the device and minimum cross-gain modulation and cross-phase modulation could be expected from a QD amplifier, compared to a QW amplifier where the carriers could move freely with microns of diffusion length. High performance QD amplifiers have then been demonstrated on CMOS compactible Si[37].

2.2 Insensitivity to defects

Naturally localized carriers in QDs contribute to strongly suppressed carrier diffusion compared to that of QWs[38]. Reduced lateral carrier diffusion length is known to minimize problems associated with surface recombination, and thus facilitate device miniaturization without imposing a penalty on the lasing threshold[39]. Carrier diffusion length can be measured with the cathodoluminescence (CL) intensity loss near a misfit dislocation (MD). Example 10 kV CL maps done at 300 K on an epitaxially grown InAs QD material on Si are shown in Figure 7a, filtered for the GS, the FES, and the SES. A typical MD was identified (circled in yellow) and the normalized intensity profiles across the MD are shown in Figure 7b. Compared to a GaAs or an InGaAs QW where carriers have a diffusion length on the order of 2 μm at 10 K[39], the measured carrier diffusion length in an InAs QD structure is as low as 0.5 μm at room temperature, as evident from Figure 7b[40], consistent with earlier research[38] .

With this much reduced diffusion length in QDs, Fabry–Pérot (FP) QD lasers grown on Si showed that reducing the ridge width shows a continuous decrease of threshold currents down to 2 μm ridge width with no sign of threshold current density increase[41]. Micro-ring resonators fabricated from the same material demonstrate a monotonically decreased threshold currents with the reduction of the ring radius[42]. Threshold currents below 1 mA were achieved with a radii as small as 4 μm [43]. Decreased carrier diffusion length also reduces the sensitivity to crystalline defects. Another important aspect that can be seen from Figure 7b is that the excited state transitions are more affected

by the nearby defects due to higher carrier escape rates. Thus, maintaining a ground state operation is essential for reliable and high performance epitaxially grown devices.

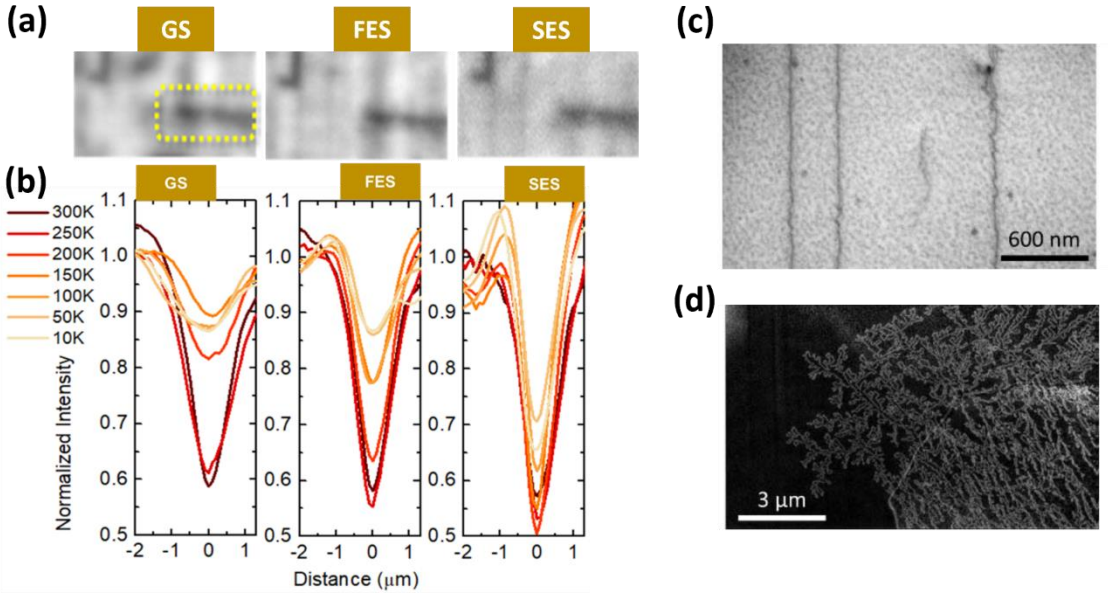

Figure 7: (a) Filtered CL maps for different transitions at 300K. (b) Temperature dependent CL intensity line scan across the identified MD, located at the origin, in different transitions. (c) and (d) are the PVTEM images of dislocations in the plane of a QD and a QW laser after aging for the same time, respectively. Clear dislocation network has been developed in the QW laser[34].

Since crystalline defects are unavoidable in epitaxially grown III-V material on Si, this makes QD emitters an ideal candidate for monolithic light source integration. Due to the reduced carrier diffusion length in QDs, the crystalline defects are less "visible," resulting in a limited recombination enhanced dislocation climb (REDC). As clearly shown in Figure 7c and d for the post-aging QD and QW devices grown on Si, minimum dislocation climb has been observed in QD devices while the dislocations in the QW devices have grown into a network via REDC[34]. Consequently, QD devices grown on Si have demonstrated record high reliability at elevated temperatures. More details will be discussed in Chapter 5.

2.3 Improved temperature dependence

As the energy separation between the quantum states are a few times larger than kT at room temperature, the threshold current of QD active region is expected to be insensitive to the temperature change[31]. The infinite characteristic temperature, T_0, was obtained under the assumption that the thermal spreading of carriers should vanish for the delta function density of states, shown in Figure 8a.

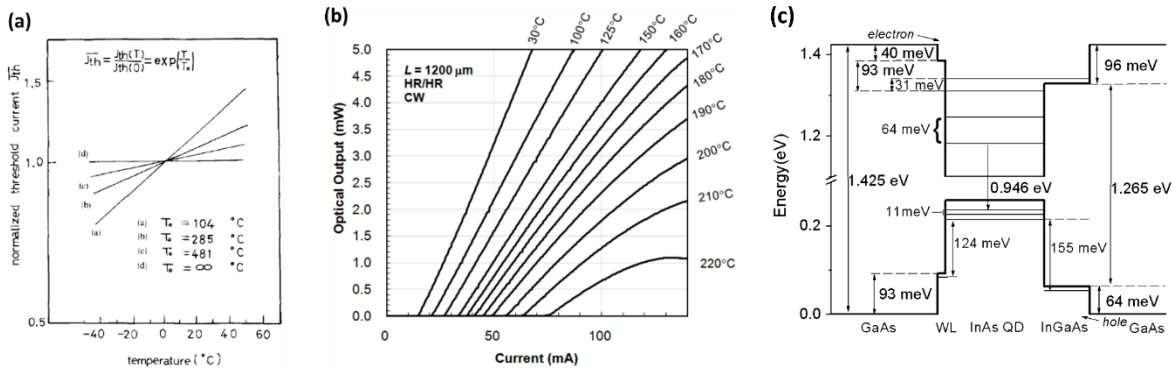

Figure 8: (a) Theoretical normalized threshold current with respect to temperature. For a 0D particle, the threshold current is expected to be independent of temperature[31]. (b) L-I characteristics of the QD laser from 30 to 220 °C under CW operation with HR coatings on both facets[44]. (c) Energy band diagram of 1.3 μm InAs QD grown on GaAs embedded in a 6 nm $In_{0.15}Ga_{0.85}As$ QW matrix[45].

Yet, for the technologically relevant InAs QD on GaAs or on InP material systems, the valence band offsets are much smaller than those in the conduction band. The energy level spacing in the valence band is then below kT at room temperature, as depicted in Figure 8c[45]. This increases the threshold as the holes are less concentrated at the top of the valence band[46] and its temperature dependence as the holes can thermalize and escape the dots. In that case, the thermal escape rate of carriers in QDs increases exponentially with temperature and is accompanied by a sharp increase in the threshold current[34,42,43,47,48]. In order to compensate for the thermal escape of holes, extra holes must be provided. *P*-type modulation doping in the barriers between each dot layer has proven to be effective, and both

the first principal theories and experimental results have demonstrated higher material gain[49–52]. As a result, with a proper *p* modulation doping, a characteristic temperature (T_0) as high as 175 K and CW operation to at least 220 °C have been obtained in a packaged InAs QD laser grown on a native GaAs substrate, shown in Figure 8b[44]. Recently, a T_0 as high as 167 K has been extracted from epitaxially grown and unpackaged devices on (001) Si and the maximum lasing temperature is >110 °C[53]. More details will be shown in Chapter 5.

Other than the parasitic recombination outside the QDs due to carrier escape as the dominant source of threshold temperature dependence, the remaining identified minor contributors include excited state recombination, inhomogeneous broadening, and violation of charge neutrality (VCN)[54]. Local charge neutrality is maintained in the QWs for the large capacitance. On the other hand, the capacitance of a QD layer is limited by the surface dot density, which is typically one or two orders of magnitude lower than the 2D carrier density in QWs[54,55]. The electron- and hole-level occupancies in QDs obtained from the solution of the electrostatic-field distribution across the junction are indeed different, meaning the QDs are charged. In a self-consistent study, the T_0 was expressed as the following, where the j_{QD} and j_{OCL} are the threshold current component from the QDs and the surrounding optical confinement layers, respectively. T_0^{QD} and T_0^{OCL} are the characteristic temperature components from the QDs and the surrounding optical confinement layers[56].

$$\frac{1}{T_0} = \frac{j_{QD}}{j_{QD}+j_{OCL}}\frac{1}{T_0^{QD}} + \frac{j_{OCL}}{j_{QD}+j_{OCL}}\frac{1}{T_0^{OCL}} \quad (1)$$

As shown in Figure 9a below, at low temperature where the carrier escape is suppressed, the threshold is dominated by the recombination in QDs and a high T_0 is expected. At higher temperature when j_{OCL} becomes the major contributor, T_0 is then expected to decrease drastically. Figure 9b shows the calculated T_0^{QD} limited by VCN (T_0^{VCN}) and excited state recombination (T_0^{exc}) at a given transition energy difference (Δ)[54]. The T_0 limited by the inhomogeneous broadening was found to be around

1500 K[57]. Thus, the minor contribution to the threshold current temperature dependence could be neglected. Eliminating the recombination channels outside of the QDs through bandgap engineering or even tunnelling injection could potentially increase the T_0 to above 1000 K, which is effectively temperature independent operation.

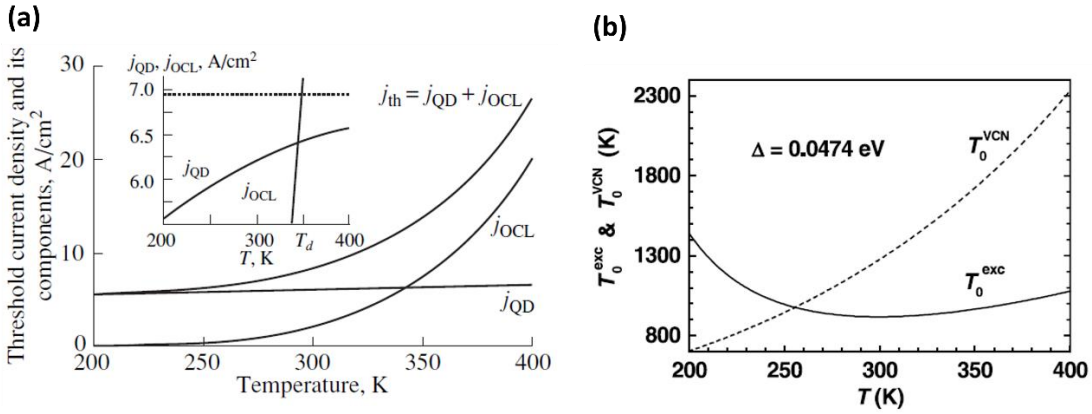

Figure 9: (a) Threshold current density and its components with respect to temperature. Inset: zoomed in j_{QD} and j_{OCL}. j_{QD}=j_{OCL} at 344 K; the dotted line represents j_{QD} calculated on the assumption of charge neutrality in QDs. (b) Characteristic temperature limited by the excited state recombination and VCN in QDs.

2.4 Reduced linewidth enhancement factor

Another important advantage of QDs, stemming also from the carrier localization, is the small linewidth enhancement factor, α_H, which is crucial for applications ranging from datacom and telecom to LiDAR and chemical sensing. The α_H can be expressed as a function of the carrier induced refractive index δn, gain G, and the carrier density N_e[35], and are closely related to both the laser linewidth, Δv, and the critical feedback level, f_{crit}[58].

$$\alpha_H = -2K\frac{d(\delta n)}{dN_e}\left(\frac{dG}{dN_e}\right)^{-1} \quad (2)$$

$$\Delta v = \Delta v_{ST}(1+{\alpha_H}^2) \quad (3)$$

$$f_{crit} = C\left(\frac{1+\alpha_H^2}{\alpha_H^4}\right) \quad (4)$$

Here, Δv_{ST} is the modified Schawlow-Townes linewidth, and C is a structural constant. An α_H value in the range of 2 to 5 for QW lasers[59–61] results in a broadened linewidth and a critical feedback level smaller than 0.01% of the output power before coherence collapse[62]. Both effects require additional components in the package. QD lasers have a lower α_H as the carriers are confined in individual potential wells and changes in the index or gain are localized. Yet, due to inhomogeneous broadening in the self-assembled QDs, the off-resonance QD subgroups would contribute to an increase in α_H [58]. To obtain low α_H values, it's important to reduce Δ_{inh} as well as improve the differential gain. With optimized growth conditions, state-of-the-art self-assembled QDs has an extracted Δ_{inh} as low as 10 meV. As stated above, adding extra holes through *p*-type modulation doping, the compensated thermalization of the less confined holes contributes to enhanced population inversion and thus much improved gain in the material[52]. Figure 10a shows the necessary combinations of Δ_{inh}, *p*-doped density N_p, and threshold gain G_{th} to achieve lasing at the gain peak with the minimum absolute value of α_H ($|\alpha_H(\nu_{pk})|_{min}$). Figure 10b shows the resulting $|\alpha_H(\nu_{pk})|_{min}$ with those combinations. It's important to note that in Figure 10b, there is a sizable region to reach zero α_H at the gain peak ($\alpha_H(\nu_{pk})$ =0), which can be obtained with a subset of Δ_{inh}, N_p, and G_{th} that are reachable in present QD lasers. This parametric study, supported with experiments, suggests that QD lasers may be configured to operate with vanishing α_H operation[35].

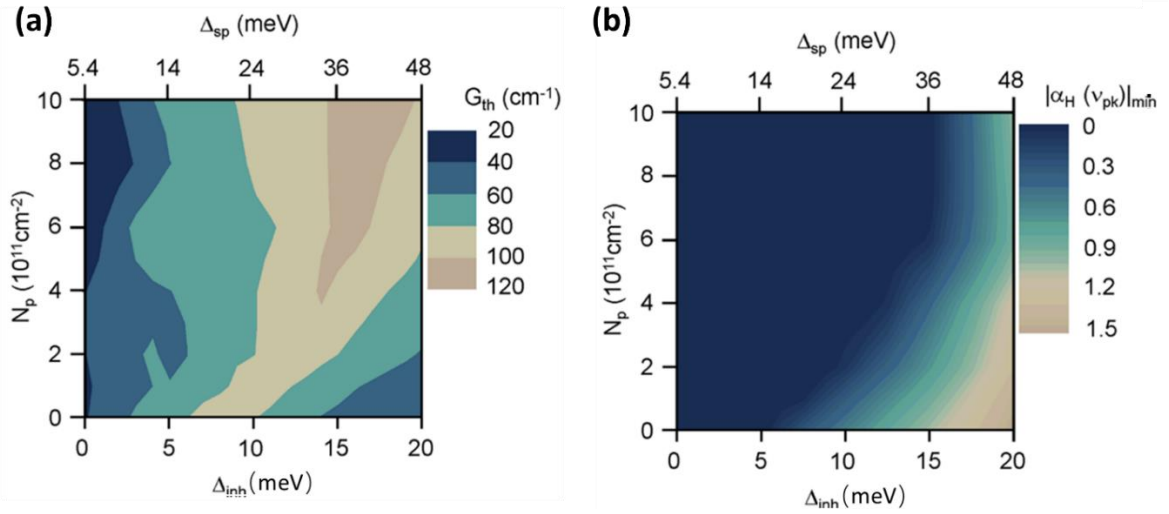

Figure 10: (a) Combination map between Δ_{inh}, N_p, and G_{th} for $|\alpha_H(\nu_{pk})|_{min}$ (b) $|\alpha_H(\nu_{pk})|_{min}$ obtainable with these combinations[35]

α_H values below unity at gain peak have been measured with the lowest reported value being 0.097 at a *p*-modulation doping level equivalent to 20 extra holes per dot[35,58,63]. *FP* lasers fabricated from the same QD material grown on Si have demonstrated an exceptional tolerance to optical feedback. As shown in Figure 11a, QD lasers on Si have only showed a small redshift of the modal wavelength up to 100% external reflection at $3\times I_{th}$ in the optical spectra, and no sign of nonlinear oscillations is observed in the RF response. On the contrary, just at a feedback level of 1.7%, the QW lasers experience coherence collapse with strong broadening of the modes and intense chaotic oscillations in the RF domain, as shown in Figure 11b[64]. Similar results have been shown in a more recent study as well[65]. Such high tolerance to optical feedback of QD lasers paves the way to achieve isolator-free photonic integrated circuit packaging in the future.

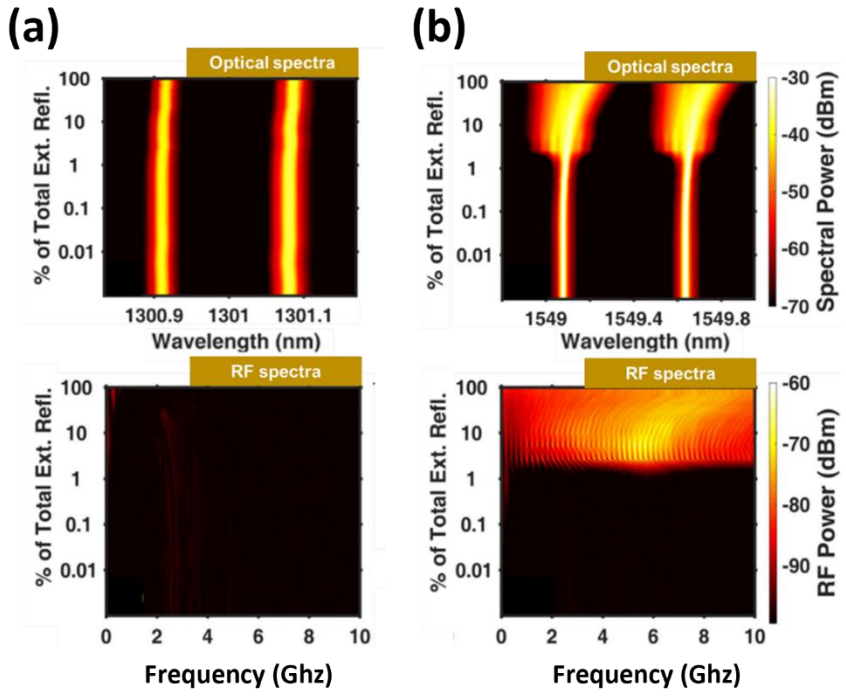

Figure 11: (a) Optical (upper) and RF (lower) spectra of the QD lasers on Si as a function of the feedback level. (b) Optical (upper) and RF (lower) spectra of the QW lasers as a function of the feedback level. The maps were obtained at an injection level of $3\times I_{th}$[64].

2.5 Enhanced four wave mixing

Due to the symmetric gain spectrum of QDs under equilibrium state filling with a small Δ_{inh}[56] ($\Delta_{inh} < kT$), QDs devices exhibit enhanced four-wave mixing (FWM) through third order nonlinear interactions. Measured FWM conversion efficiencies on InAs QD laser with *p*MD are close to the theoretical limit from the first principal calculations[66]. Figure 12 shows the results of probe-drive laser experiments on InAs QD lasers grown on Si, for active regions with undoped and *p*-modulation doped spacer layers. The drive laser power was fixed and the probe-drive mode number difference, Δm, is 2 in both cases. The experimental results in both cases are bounded by a choice of net FWM coefficient, $\xi \equiv \frac{\chi^{(3)}}{g_s}$, between 4 and 8×10^{-21} m^3V^{-2}, where $\chi^{(3)}$ is the third-order nonlinear susceptibility and g_s is the material gain. The gain in signal power is higher for lasers with *p*-doped

active region than those with undoped active region, despite the same value of ξ. Duan *et* al. suggested that the gain competition and $\chi^{(3)}$ should be considered on equal footing when evaluating mode-locking performance[66].

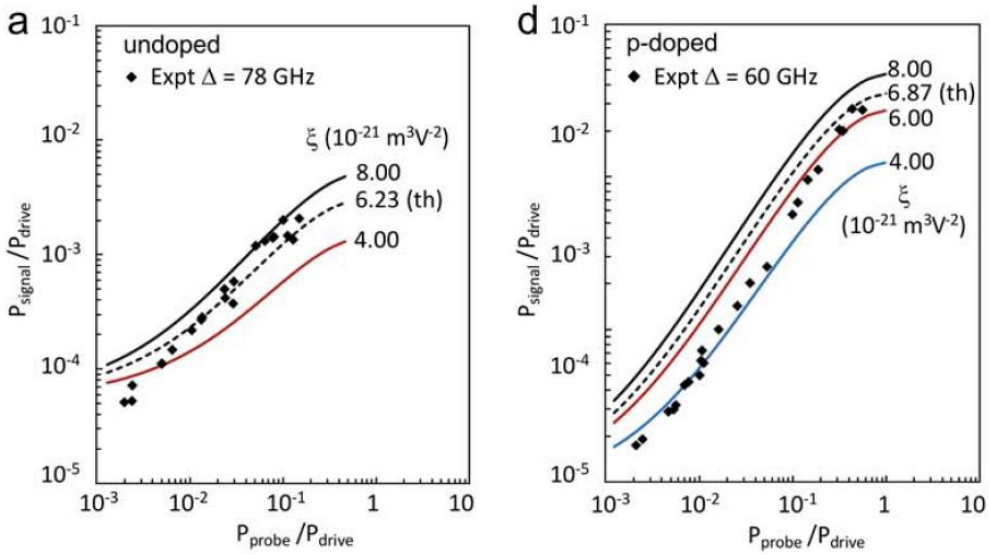

Figure 12: Normalized signal power versus probe power in a probe-drive laser experiment for (a) undoped and (b) p-doped lasers. The frequency detuning, Δ, corresponds to the same mode number difference. Dashed lines are calculated from multimode laser theory and the solid lines are the calculated from selected ξ values.

Strong FWM is theorized to facilitate single-section mode-locked lasers (MLL) which have higher output power and simpler fabrication procedures compared to the two-section MLL with a saturate absorber [67]. Such devices have also been demonstrated experimentally [68,69]. High performing MLLs could greatly simplify the design of wavelength-division multiplexing (WDM) systems.

2.6 Summary

Benefiting from the 3D confinement of the carriers, the delta-function-like density of states in QDs provide them with unique properties compared to the QW counterpart. In the non-exhaustive list above, the low defect sensitivity and dislocation climb inhibiting ability are the most important advantages of QDs making them the ideal candidate for monolithically integrated light emitters. Yet,

insensitivity does not equal immunity. In order to achieve the native substrate performance and enjoy the lower threshold current and the potential isolator-free operation at elevated temperatures on Si, the crystalline defects from the heteroepitaxial growths must be eliminated. New methods for defect reduction will be introduced in the next two chapters which have consequently led to the breakthrough in high temperature reliability.

Chapter 3
Obtaining thin and low defect virtual substrates on (001) Si

3.1 Challenges

Direct epitaxial growth of III-V material on Si could be utilized for the benefit of large wafer size, lower cost, and better thermal conductivity of Si relative to heterogeneous silicon-on-insulator platforms[70]. The main problem with direct epitaxial growth is the dissimilarity between III-V materials and Si. Anti-phase domains (APD) can form when growing III-V material on on-axis Si (001) due to the polarity mismatch[71]. This problem has largely been solved with various approaches, ranging from highly optimized Si wafer preparation and well-controlled initial III-V nucleation[72–74] to the use of patterned Si with exposed high index surfaces[75–77]. Large thermal expansion coefficient mismatch may result in surface cracking and wafer bowing during the post-growth cooling process. Before the onset of the above-mentioned macroscopic effects from the CTE mismatch, researchers have discovered that a more subtle change in the crystal, yet more influential to the device performance, would initiate in response to the CTE mismatch. This problem can be mitigated with lower cooling rates, thinner stacks, careful sample cleaning prior to growth, and better design of sample holders. Details are discussed in Chapter 4.

As many researchers previously believed, the most detrimental and yet unsolved issue of direct epitaxial growth is the high density of threading dislocations originating from the high lattice constant mismatch. Various methods have been explored to reduce the threading dislocation density (TDD).

Inserting buffer layers with strained dislocation filter layers (DFLs) and thermal treatments during or after buffer growth have been two of the most successful methods. Thermal cyclic annealing (TCA) is known to be an effective technique for reducing the TDD for GaAs films grown on Si substrates[78]. Due to the thermal expansion mismatch between Si and GaAs, which is about 3 ppm/K across the temperature range of interest, temperatures above or below the GaAs film growth temperature generate additional compressive or tensile stress, respectively. The induced thermal stresses promote the lateral motion of the existing TDs in the GaAs film, and the probability of TD interaction is then increased, which could potentially lead to TD reduction and annihilation. DFLs promote the lateral motion of TDs through plastic relaxation within the intentionally lattice-mismatched layer. Different DFL structures and materials have been studied extensively[79,80]. More recently, several groups have demonstrated successes in TDD reduction with the use of multiple strained layer superlattice (SLS) structures as DFLs[81–83]. Combined with InAs quantum dots as the active region, high-performance light sources epitaxially grown on Si have been demonstrated[77,84,85]. The reliability of the InAs QD laser grown by molecular beam epitaxy (MBE) emitting around 1.3 μm grown on Si (001) has a strong and monotonic exponential dependence on the TDD of the GaAs-on-Si virtual substrate. Previous reports indicate that the extrapolated time required for doubling the initial threshold current at room temperature increases from about 800 h to more than 10,000,000 h as the TDD decreases from[86] 2.5×10^{8} cm^{-2} to 7.6×10^{6} cm^{-2}. The extrapolated lifetime at elevated temperatures for normal operating conditions in data centers is still poor compared to the devices grown on native GaAs substrates. Further reducing the TDD for epitaxially grown GaAs-on-Si virtual substrates is still of great importance and yet becomes increasingly challenging at low TDD levels as the likelihood of two TDs interacting with each other becomes extremely low. The theoretical lower limit of TDD for any heteroepitaxial structure is about[87] 10^{4}-10^{5} cm^{-2}. A TDD of 1.2×10^{6} cm^{-2} has been obtained on an off-cut Si wafer with a 4 μm buffer layer[88] and a TDD lower than 10^{5} cm^{-2} has only been achieved with thick and fully relaxed compositionally graded layers[89]. However, neither of these is ideal for practical

applications due to the buffer thickness and wafer orientation. In the next sections in this Chapter, a systematic study of the two widely used TD reduction techniques are discussed. An "asymmetric graded filter" structure is then proposed, and the resulting TDD is lower than 1.5×10^{6} cm^{-2} within 2.55 μm buffer thickness.

3.2 Limit of TCA

All the samples were grown in a Veeco Gen-II solid source MBE. The APD-free GaP/Si(001) on-axis template is commercially available via $NAsP_{III/V}$, GmbH[71]. Multiple 1.6 μm GaAs on GaP-on-Si samples were grown under the conditions described elsewhere[83]. TCA was then performed on the GaAs on GaP-on-Si samples. We varied the number of cycles to evaluate its impact on the TDD. In these experiments, the low temperature limit is 400 °C and the high temperature limit was set as high as possible until the surface quality degraded due to an insufficient supply of arsenic. The sample was held at the maximum annealing temperature (T_{max}) for 5 minutes during each cycle. The arsenic beam-equivalent pressure during TCA was set to 1.2×10^{-5} torr. It has been suggested that gallium droplets form on the GaAs surface if the temperature is too high, regardless of the arsenic supply[90]. This high temperature limit was found to be 745 °C in our chamber. To ensure reproducibility, the maximum cycling temperature was dialed down to 735 °C. The TDD was then measured after TCA with electron-channeling contrast imaging (ECCI). At least 100 threading dislocations are counted for each sample to ensure statistical significance. A channeling condition consisting of both {040} and {220} is used so that TDs with all known Burger's vectors are visible[83]. The TDs would then appear to be bright spots due to the local violation of the channeling conditions.

The effect of higher temperature thermal annealing on the defect level in GaAs films grown on Si (001) has been studied by several groups. Higher annealing temperature results in higher compressive strain in the GaAs layer which leads to fewer cycles for the same threading dislocation reduction[78,91,92]. GaAs surface quality can also be significantly improved[93] as the misplaced atoms due to enhanced

growth near defects and asymmetric surface diffusion would be redistributed to their energetical favorable sites. Yet, previously reported annealing temperatures are either thermocouple target temperature or ambient temperature in the furnaces. The TCA temperature limits have not been fully explored for an in-situ MBE chamber with pyrometry-based temperature measurement and arsenic overpressure. Figure 13a shows the TDD measured on top of the GaAs film after different TCA processes. The GaAs film was grown at 580 °C. The thermal mismatch strain can be calculated with the following equation.

$$\varepsilon_{thermal} = \int_{T_g}^{T_{max}} \left(\alpha_f(T) - \alpha_s(T)\right) dT \tag{5}$$

where α_f and α_s are the temperature dependent linear thermal expansion coefficient of the film and the substrate, respectively. Both α_f and α_s can be approximated to be linearly depend on T within the temperature range of interest[94,95]. T_g is the growth temperature and T_{max} is the annealing temperature.

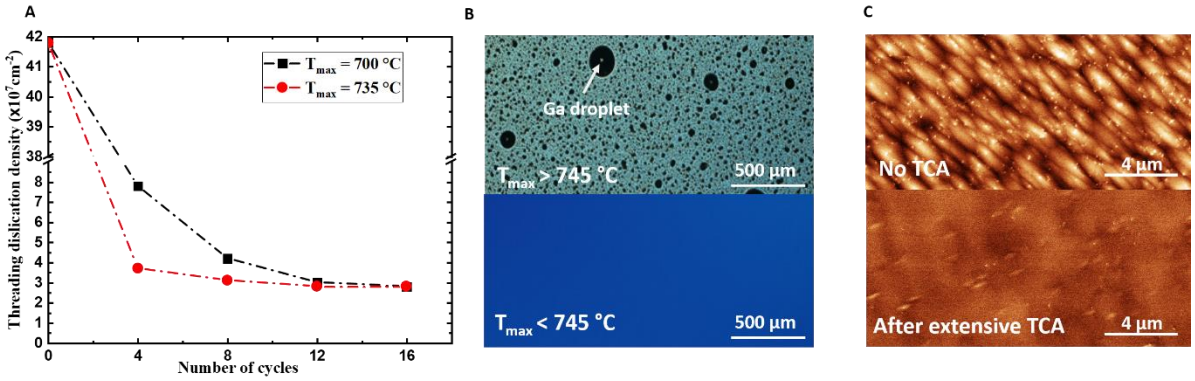

Figure 13: (A) TDD of the post-TCA GaAs-on-Si template. The minimum TDD achievable via TCA at the given GaAs thickness is about 3×10^7 cm^{-2}. (B) Nomarski microscope image of the GaAs surface after annealing above and below 745 °C pyrometry temperature. Gallium droplets are observed when T_{max} is higher than 745 °C. (C) ECCI images of the as-grown GaAs with no TCA (top) and after 16 cycles of TCA (bottom). The TDD is about 4.18×10^8 cm^{-2} with no TCA and decreases to 3×10^7cm^{-2}after extensive TCA.

By increasing the temperature to 700 °C, an additional 0.037% compressive strain was introduced due to the thermal expansion mismatch between GaAs and Si, which in turn generated a biaxial compressive stress of about 70 MPa. Thus, the TDs would be moving at a velocity of approximately 1 mm/s at 700 °C according to the dislocation velocity measured in GaAs[96]. During the hold time of 5 minutes, the TDs should have enough time to move across the entire sample (2cm-by-2cm). Since the thermal mismatch is small, only a small portion of the existing TDs need to move to relax the thermal stress. Thus, the full cycling process including the low temperature step is required to re-establish the thermal stress in each cycle. Only glissile TDs can move under the induced thermal stress.

The glissile TDs can either react with existing TDs, glissile or sessile, or propagate to the edge of the wafer and exit the crystal, in both cases reducing the TDD. It was previously discussed that the reactions between the TDs in a zinc-blend crystal maintain a glissile vs. sessile ratio of 1:1[87], and this has also been experimentally observed[97]. Therefore, the supply of glissile TDs does not quickly run out. Thus, the plateauing of the TDD with respect to the number of cycles is primarily due to work hardening as the misfit dislocations (MDs) at the GaAs/Si interface elongate in each cycle.

Figure 13a indicates that additional cycling produces a minimum reduction of TDD after 12 cycles. Increasing the maximum annealing temperature to 735 °C generates a thermal mismatch strain of 0.049%, which translates to about 93 MPa of bilateral compressive stress. With higher stress, similar TDD reduction is achieved at 4 (or 8) cycles as with 8 (or 12) cycles with lower thermal mismatch stress. It is then expected that the plateau can be reached much sooner if the annealing temperature is sufficiently high. Yet, when the annealing temperature is above 745 °C, the GaAs surface quality

degrades catastrophically with the formation of Ga droplet[90], as shown in Figure 13b. The surface morphology difference[93], illustrated in Figure 13c, is observable by naked eye.

3.3 Dislocation filter efficiency

The technique of using strained-layer structures as DFLs has been widely applied. A SLS is the most used structure in GaAs-on-Si buffer layers[82,83,98]. The idea of using alternating signs of misfit strain is to enhance the probability for dislocation interactions as the threading segments move back and forth[99]. The first use of SLS as DFL was proposed by Matthews and Blakeslee with $GaAs_{0.5}P_{0.5}$/GaAs superlattice[100,101]. The design parameter space for optimizing the effectiveness of SLS is huge, including strain state and thickness of each period, total number of periods, thickness ratio of the two alternating materials in each period, and growth conditions. $In_{0.2}Ga_{0.8}As$/GaAs SLS was found to be more effective than $GaAs_{0.8}P_{0.2}$/GaAs when grown on a 2 μm thick $In_{0.1}Ga_{0.9}As$ buffer layer on native GaAs substrate[80]. The difference was attributed to a larger interlayer strain and elastic constants difference despite the fact that the signs of the initial strain were also different. The SLS structure with lattice-matched alternating layers in each period was found to be effective in a dislocation filter as well, though a minimum strain between the alternation layers was expected[102]. While such layers with alternating strain undoubtedly have a role to play in blocking new TDs from possible spiral or Frank-Read multiplication sources[103], it is not very clear if they help in enhancing existing TD-TD reactions and annihilations. Hull et al. show that SLSs in SiGe on Si do not perform any better than a single composition layer with the same average composition in terms of relaxable strain energy[104]. This may be more pertinent in MBE growth given the sluggish relaxation kinetics at 500 °C. The efficiency of the InGaAs DFL as an example was investigated based on the growth conditions, indium composition, and structure.

3.3.1 Efficiency of InGaAs/GaAs strained layer superlattice

As mentioned above, the design space for the InGaAs/GaAs SLS structure is huge. Yet, the TDD level close to the 10^5 cm^{-2} region has not been reported within reasonable buffer thickness on CMOS compatible Si using the SLS DFL structure. To investigate the effectiveness of the InGaAs/GaAs SLS structures, varying periods tending towards a constant composition layer with the same equivalent average strain were experimental studied. $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (*x* nm)×20 SLS as dislocation filter layers have been grown on the GaAs-on-Si template with a TDD of 3×10^7 cm^{-2}, with the *x* taking the values of 10, 7, 5, 2, and 0. The structure is capped with 300 nm of GaAs. All filter structures were grown at 500 °C with a growth rate of 0.3 nm/s and a V/III ratio of 20. The additional film thickness introduced by the filter layers and the capping layer was not expected to reduce the defect density significantly. Quantitative degree of relaxation was evaluated from reciprocal space maps (RSMs) taken with a Rigaku Smartlab system, where the large-angular-range and high-resolution RSMs were taken quickly due to the Hypix2000 large-area detector. The results are summarized in Figure 14 (the case for x = 7 nm is not shown).

The observed TDs on the surface are circled in the ECCI images. The filtering efficiency is improved significantly with a thinner GaAs layer in between the $In_{0.15}Ga_{0.85}As$ layers, with the continuous 200 nm $In_{0.15}Ga_{0.85}As$ (x = 0 nm) having the highest efficiency. The efficiency of the filter layer depends on the degree of relaxation, especially the degree of relaxation of the InGaAs layer. It can be seen from both the ECCI images, Figure 14A-D, and the Nomarski images, Figure 14E-H, that the surface crosshatch pattern becomes more prominent as the x value decreases to 0. Only very mild surface crosshatch can be observed with the $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (10 nm) SLS structure. Faceted trenches (FTs) can be observed in the x = 2 and x = 0 cases. Both the more prominent surface crosshatch pattern[105] and the formation of FTs qualitatively suggest a higher degree of relaxation in

the single $In_{0.15}Ga_{0.85}As$ layer[106]. The RSMs, centered around the GaAs {224} peak, of the SLS structures are shown in Figure 14I-L. The degree of relaxation, R, is defined as

$$R = \frac{a_L - a_S}{a_L^0 - a_S} \times 100\% \quad (6)$$

where a_S is the in-plane lattice constant of the substrate, which is that of GaAs in this case (5.653 Å). a_L^0 is the in-plane lattice constant of the $In_{0.15}Ga_{0.85}As$ layer if it is fully relaxed (5.714 Å) and a_L is the measured in-plane lattice constant of the $In_{0.15}Ga_{0.85}As$ layer, which can be extracted from the RSMs.

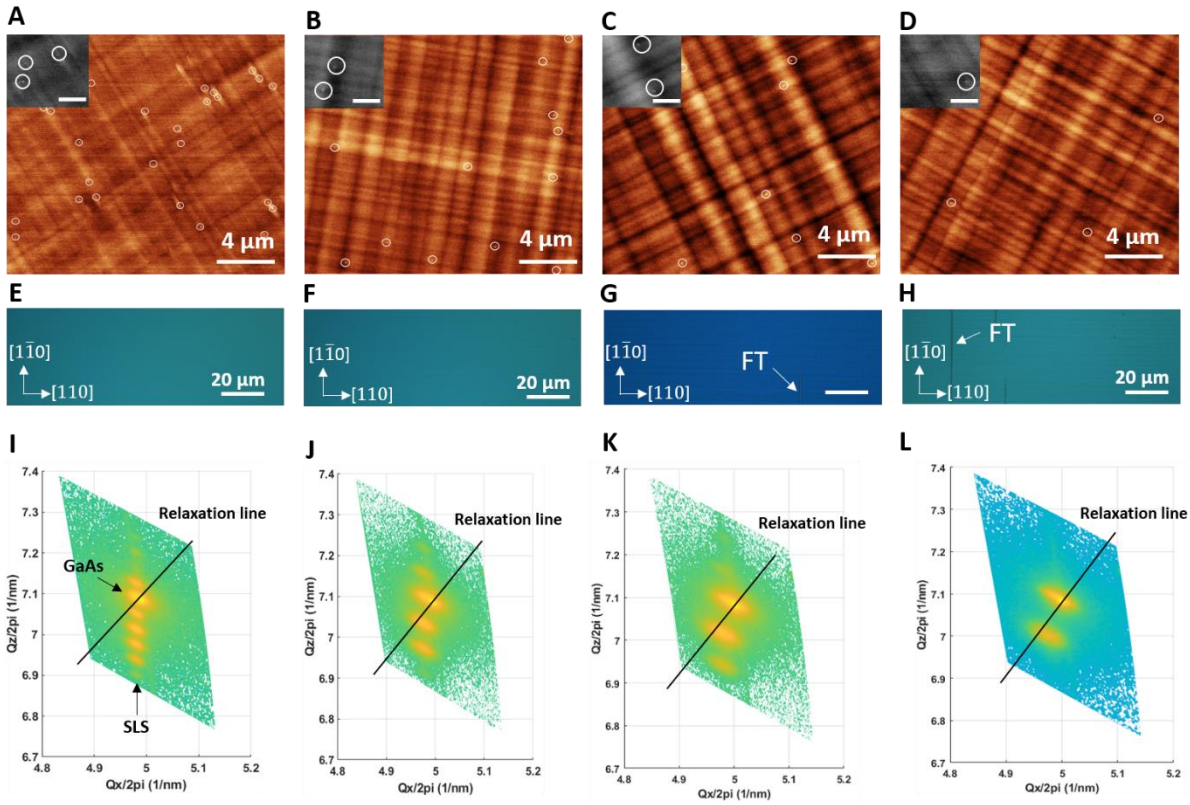

Figure 14: (A)-(D) Representative ECCI images of the SLS sample with GaAs layer thickness, x = 10, 5, 2, and 0, respectively. The insets are zoomed ECCI images showing clear TDs in the white circles. The scale bar in the insets is 1 µm. The surface TDD is much lower in the sample with a continuous 200 nm $In_{0.15}Ga_{0.85}As$ filter. (E)-(H) Nomarski microscope images of the sample with x = 10, 5, 2, and 0, respectively. Surface crosshatch and FTs are more obvious with

thinner GaAs in between the $In_{0.15}Ga_{0.85}As$ layers. (I)-(L) RSMs of the sample with x = 10, 5, 2, and 0, respectively. The SLS is more relaxed as x decreases to 0.

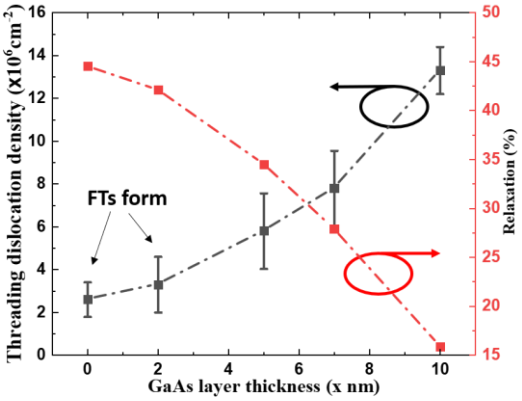

Figure 15: TDD and degree of relaxation of the SLS as a function of GaAs layer thickness in between the $In_{0.15}Ga_{0.85}As$ layers. The SLS with no GaAs layers (x = 0) is about 3 times more relaxed than x = 10 case. The TDD is much lower in the sample with a higher degree of relaxation in the SLS. Though TDD is low for x = 2 and x = 0 cases, FTs are observed on top of the GaAs capping layer.

Figure 15 shows the surface TDD and relaxation of the SLS structures. The relaxation for the as-grown $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (10 nm) structure is 17.6%, which increases to 44.6% as the GaAs layer thickness decreases to 0 nm. These relaxation values match well with the previously reported data[103]. The surface TDD simultaneously decreases from 1.3×10^7 cm^{-2} to 2.1×10^6 cm^{-2}. Thus, the degree of relaxation in the $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (x nm) DFL has a direct and significant impact on the filtering efficiency, though a mild diminishing return is observed.

The schematics in Figure 16A-F qualitatively illustrate the relaxation process in a SLS structure. Here positive strain values are used to denote compression and the initial mismatch strain between $In_{0.15}Ga_{0.85}As$ and GaAs-on-Si template is denoted as ε_0. Though the calculated Mathew-Blakeslee critical thickness is about 9 nm, the thickness required for significant plastic relaxation can be much larger[103], and this thickness is found to be about 100 nm under our MBE growth conditions. Thus, the first few periods of the SLS are close to fully strained with respect to the GaAs-on-Si template, and

the TDs from the GaAs-on-Si template would propagate continuously, as shown in Figure 16A and B. After reaching the thickness required for significant plastic relaxation in the $In_{0.15}Ga_{0.85}As$ layers, all layers within the SLS structure relax together and the TDs move to relax the compressive mismatch strain, as shown in Figure 16C and D.

The GaAs layers in between the $In_{0.15}Ga_{0.85}As$ layers would then be under tension. Segments of the TDs in the GaAs layer would then experience a force opposite to the preferred propagation direction in the $In_{0.15}Ga_{0.85}As$ layers. Since the SLS structure relaxes in response to the compressive strain, having segments experiencing opposite forces would hinder the relaxation process, given the finite growth time and dislocation velocity. As the accumulative tensile strain energy exceeds the value required for significant tensile relaxation, TD segments within the GaAs layers would prefer to move in the opposite direction as the segments in the $In_{0.15}Ga_{0.85}As$ layers, which would further hinder the overall relaxation of the SLS structures, as shown in Figure 16E and F. Thus, the thicker the GaAs in between the $In_{0.15}Ga_{0.85}As$, the less the relaxation, with $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (10 nm) being the worst case. It has been reported previously that a SLS with intentional tensile layers is less efficient than the InGaAs/GaAs SLS[107]. Thus, having the tensile GaAs layer within a SLS structure degrades the filtering efficiency.

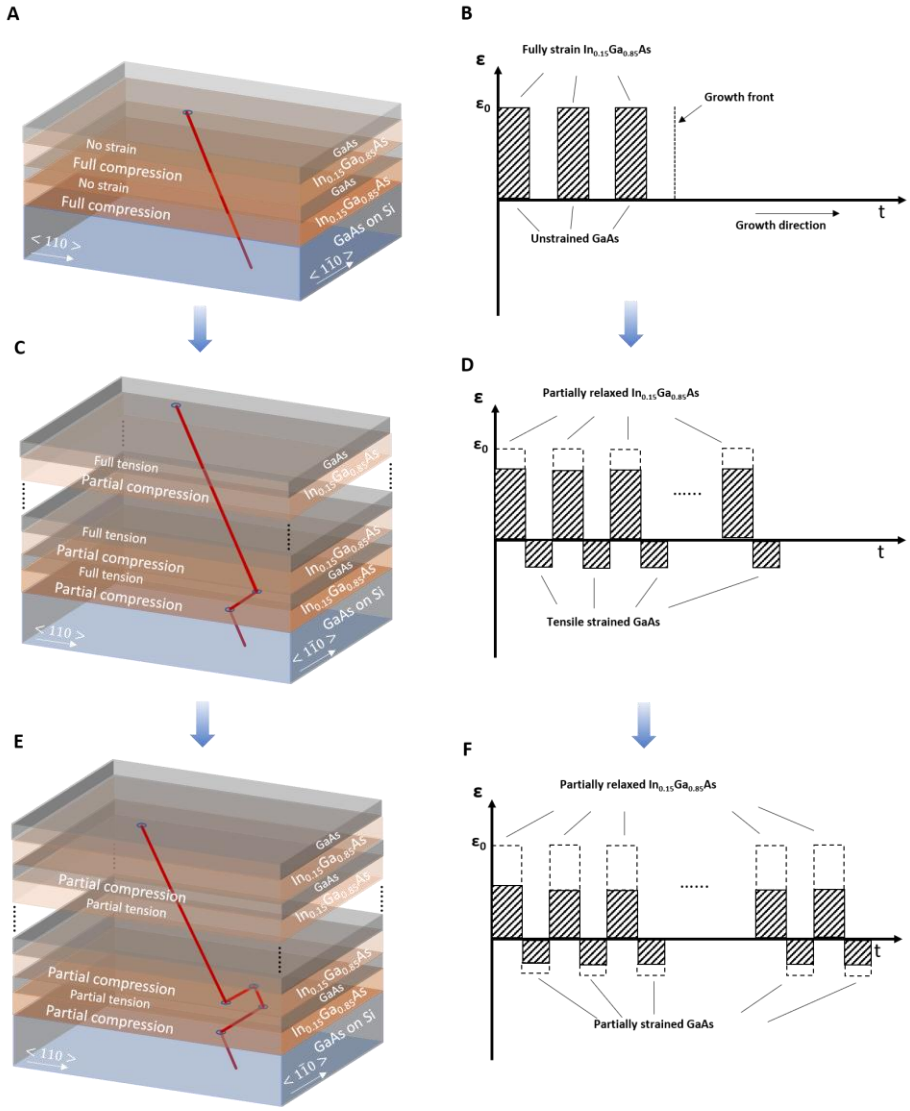

Figure 16: Schematic illustrations of the expected TD motion in (A), (C), and (D), and qualitative strain states in (B), (D), and (F), at different stages of relaxation within a SLS structure. Not all periods are drawn for simplicity. Tensile relaxation in the GaAs layers is expected to happen later during growth as no strain energy is accumulated in the first few periods of the SLS. Thus, the tensile strain would hinder the relaxation process.

It is important to realize that a SLS is not inherently worse than a single layer filter. Tensile relaxation in the GaAs layer indeed is beneficial to TDD reduction, as discussed later in Sec.3.2.2. But to utilize the tensile relaxation benefit in a SLS structure, each layer within the SLS structure needs to relax significantly. This would require thick layers in each SLS period, since the thickness required for

significant relaxation is about one order of magnitude higher than the Matthew-Blakeslee critical thickness.

3.3.2 Effect of indium content in the InGaAs dislocation filter layer

Given that the single layers provide greater TD reduction for a given amount of average strain, we explore this further by testing the composition range over which we may increase the average strain while minimizing new multiplication. Higher average strain intuitively imposes a risk of work hardening for a given thickness[103] and forming FTs in the top GaAs capping layer due to the abrupt tensile relaxation, which has been observed in other tensile relaxed films[108]. 200 nm single layer InGaAs filters with 10%, 15%, 17.5%, 20%, and 25% indium composition were grown. The results plotted in Figure 17A indicate that the TDD started to increase when the indium composition is higher than 20%.

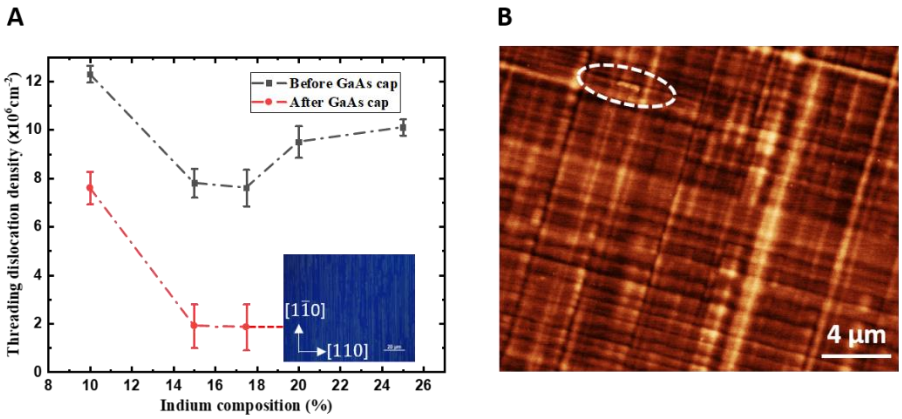

Figure 17: (A) TDD measured before and after GaAs capping layer with a single 200 nm InGaAs filter. The TDD starts to increase once the indium composition in the InGaAs layer is above 20%. The inset shows an example Nomarski image of samples with more than 20% of indium in the InGaAs filter layer. No large enough clear regions for ECCI measurements. (B) Example ECCI image of sample with more than 20% indium in the InGaAs layer before GaAs capping. "Blocked" TDs are circled.

Figure 17B shows an example ECCI image of 20% InGaAs samples. A clear "blocking" effect has been observed where some TDs are aligned parallel to the crosshatch pattern. The surface

crosshatch pattern is known to be the result of the underlying MD array[105]. The interaction between the stress fields of perpendicular misfits may result in the "blocking" of the threading segment[103]. The blocked TDs would then appear aligned with the surface crosshatch pattern. 300 nm GaAs capping layers were then grown on top of the InGaAs filter layer and the TDD is further reduced through the tensile relaxation in the GaAs capping layer. The formation of FTs was clearly observed in the top GaAs layer with the underlying InGaAs having an indium content higher than 15%, example shown in the inset of Figure 17A. The post-GaAs-cap TDD of the samples with indium content higher than 20% cannot be measured by ECCI due to the high density of FTs. Thus, the tensile relaxation in the top GaAs layer, which would cause the TDs to move in the opposite direction as they do in the compressively relaxed InGaAs, is beneficial to TDD reduction. Yet, stacking multiple 200 nm single layer InGaAs filters with 300 nm GaAs spacers in between does not result in further TDD reduction.

3.4 Proposed more efficient filter structure

The previous three experiments ultimately lead to a defect filter strategy involving TCA and a quasi-single layer with compositional grading to minimize the formation of FTs and reduce the "blocking" effect. As discussed in the previous sections, the efficiency of the single layer filter drops when the indium content is above 17.5%. Thus, the maximum indium content in the first proposed structure is limited to 10%. Single layer InGaAs filters will be used as the building blocks for the proposed filter structure.

In order to have a DFL structure with higher efficiency, a higher level of relaxation in the DFL is required. Here, we propose an "asymmetric step-graded filter" structure as shown in Figure 18A. Graded filters are known to be helpful in promoting more efficient relaxation, as the "blocking" effect is reduced[87]. The indium content is graded in steps up to the maximum value of 10%, with 5% increments in each layer, and then graded down to 0%. The layer thickness on the tensile side is intentionally thicker as tensile relaxation is expected to be harder to initiate[109] and may result in the

formation of FTs[108,110]. In the as-grown structure with 10% maximum indium content, the $In_{0.05}Ga_{0.95}As$ layer is 80.2% relaxed and the $In_{0.10}Ga_{0.90}As$ layer is 49% relaxed with respect to the GaAs-on-Si template. For the same structure where each InGaAs layer is subject to a 10-minute annealing at 530 °C under arsenic overpressure and the growth is interrupted during the annealing process, the relaxation is further promoted to 88.9% and 58% for the $In_{0.05}Ga_{0.95}As$ and $In_{0.10}Ga_{0.90}As$, respectively.

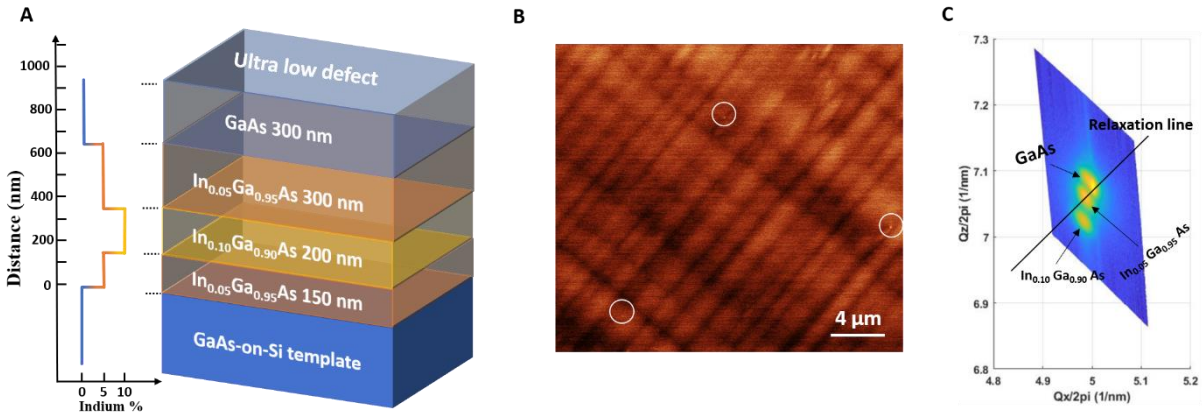

Figure 18: (A) The experimental sample structure for the proposed "asymmetric step-graded filter" with maximum indium content of 10%. The plot to the left of the schematic structure shows the indium composition of each layer with respect to the distance measured from the top of the GaAs-on-Si template. (B) Representative ECCI image of the structure showing a TDD of 2×10^6 cm^{-2}. (C) RSM of the annealed structure shows 88.9% relaxation in the $In_{0.05}Ga_{0.95}As$ layer and 58% relaxation in the $In_{0.10}Ga_{0.90}As$ layer with respect to GaAs.

The surface TDD measured in the annealed sample is $1\times10^6\pm2\times10^5$ cm^{-2} at 95% confidence interval. An example ECCI image is shown in Figure 18B. Thirty-three percent of all ECCI images taken, which cover a total area of about 2000 μm^2, are entirely free of TDs. The RSM for the annealed structure is shown in Figure 18C. The TDD of the nominal structure with a single 200 nm $In_{0.10}Ga_{0.90}As$ filter is about 7.2×10^6 cm^{-2} with the same total sample thickness, and the relaxation of the $In_{0.10}Ga_{0.90}As$ layer is expected to be only about 35%. The RMS surface roughness of the top GaAs surface is about 2.1 nm. Figure 19 shows the XSTEM and PVSTEM images of the asymmetric step-

graded filter structure with annealing. Both samples are prepared with Helios 600 DualBeam workstation (FEI, USA) and imaged with a Talos F200X (Thermo Scientific, USA) at 200 kV with (220) and (2 $\bar{2}$ 0) two-beam diffraction conditions for the PVSTEM and XSTEM samples, respectively. The XSTEM in Figure 19A shows the clear asymmetric step-graded filter structure with darker color suggesting higher indium composition. Though MD arrays at the last GaAs/$In_{0.05}Ga_{0.95}As$ interface are revealed in the bright field PVSTEM in Figure 19B and C due to the tilt of the PVSTEM foil, not a single TD is shown in the clear regions. Assuming there is one TD in the clear regions, the measured TDD via PVSTEM is about 1.5×10^{6} cm^{-2}.

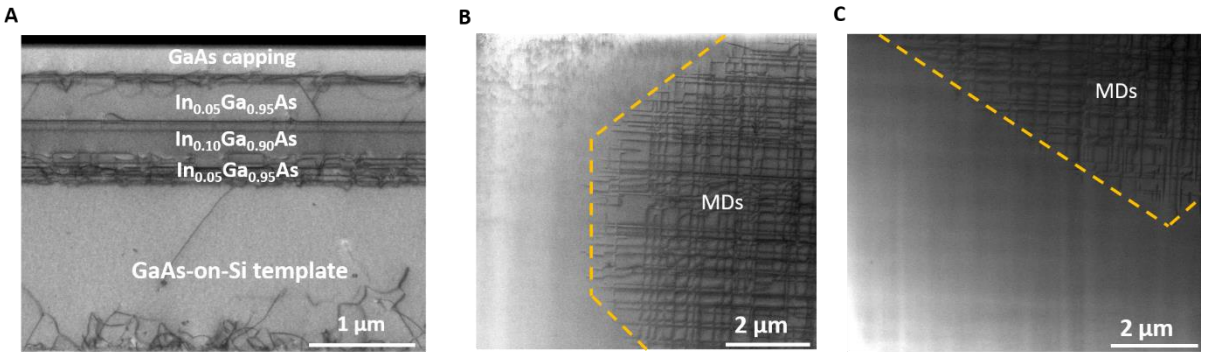

Figure 19: Bright field STEM images of the asymmetric graded filter structure with annealing at each InGaAs layer. (A) XSTEM showing the graded filter layers, with **g** = **220**. The top GaAs layer appears to be TD free. (B) and (C) PVSTEM on different areas, imaged in a (220) two-beam condition. MD arrays are shown due to the tilt of the foil with respect to the sample surface. An area of at least 65 μm^2 appears to be TD free.

3.5 Summary

The traditional SLS dislocation filter structure should have been discarded. The compressive relaxation is hindered by the presence of the tensile layers in between and a thick single continuous compressive layer is then more effective in the material system under consideration. Stacking the single layers in a "step graded" manner on both the compressive and tensile side further promotes relaxation by reducing the work hardening effect from the orthogonal misfit arrays. The degree of

relaxation and the efficiency of the “step graded” filter could be further promoted in a “continuous graded” filter. Having the filter layer peaks aligned on the relaxation line in the RSMs would be maximum possible efficiency for a given filter design.

Chapter 4
The monster hiding in plain sight: CTE mismatch

The CTE mismatch has been neglected in university research labs as wafer warping is a negligible problem for the small sample sizes and most of the effort has been devoted to dealing with the defects from the compressive lattice mismatch. Recent discoveries and observations show that CTE mismatch has played a much bigger role is the crystal/wafer quality and the device performance[111]. The findings could potentially overthrow the long-held belief of threading dislocations being the most detrimental factor in epitaxial grown devices. The CTE mismatch, approximately 3 ppm/K for GaAs/AlGaAs films on Si[112,113], changes the stress state of the film from compression to tension during cooling, and the film-substrate assembly reacts to such tension in three general ways. The first is crack formation[114–116]. The CTE mismatch between III-V materials and Si substrate is known to cause film cracking after cooling from the growth temperatures, normally around 550 °C for MBE, to room temperature as the III-V films are generally thick to reduce the threading dislocation density before the active region. However, such abrupt process is the least effective as the relaxation is only penetrates a few microns into the crack surface[114]. Wafer warping is another macroscopic consequence of the CTE mismatch as films are expected to experience residual tensile stress after cooling. The film-substrate assembly curves to accommodate for the residual stress but does not provide relaxation The mathematical relationship between the residual stress and wafer curvature is described by the Stoney's formula[117]:

$$\kappa = \frac{1}{R} = \frac{(1-\nu_s)6\sigma h}{E_s H^2} \quad (7)$$

where R is the radius of curvature, E_s and ν_s are the elastic modulus and Poisson's ratio of the substrate, respectively, and H is the substrate thickness. Thus, for a GaAs/AlGaAs film of approximately 6 μm thickness cooled from 550 °C to room temperature, the residual tensile stress is approximately 240 MPa, which translates to a radius of curvature of ~13 m. Hence, the wafer curvature is not a noticeable problem in university research labs for the small sample sizes (13 m radius correspond to a deflection of ~2 μm for samples with 2×2 cm^2 in size). However, this effect should be considered for such devices on 300 mm wafers for the eventual commercialization, where device yield and manufacturability are of paramount importance, and large wafer deflections would render the wafer not manufacturable. Another more subtle effect of the CTE mismatch, which is more detrimental to device performance, is the formation of misfit dislocations (MDs) near the active region due to the reverse glide process of the existing defects. In the following sections, all three mechanisms will be discussed.

4.1 Formation of MDs near the active region

Before cooling, the extended defects, both MDs and TDs, in the III-V crystal formed to relax the compressive strain from the lattice mismatch. Since Si is mechanically a lot more rigid against heat than GaAs/AlGaAs, the III-V film strain state changes from compression to tension during the post-growth cooling process. The III-V film thickness is normally well-above the critical thickness for plastic relaxation with a 3 ppm/k thermal mismatch. Existing defects, especially the MDs, would "shrink" to partially release the thermal tension[118]. This process is schematically illustrated in Figure 20.

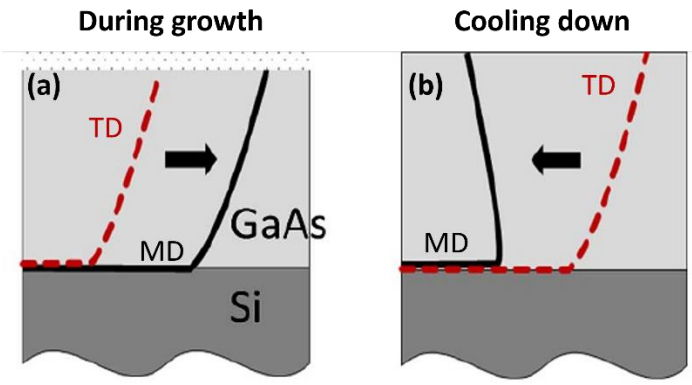

Figure 20: (a) The MD elongates to relax the compressive strain during growth and the TD segment glides through the crystal. (b) During cooling, the MD shortens in length to partially release the tensile strain. The TD segment thus experiences a "reverse-glide" process[118].

This explains why measured residual tension is always lower than the theoretical value calculated from the CTE mismatch and the temperature change between growth and room temperatures. Most of the studies that focused on the CTE mismatch between III-V and Si used simple GaAs or AlGaAs films. However, the existence of a InAs/InGaAs DWELL active region in the middle of a laser stack complicates the picture. The TD segment sees a much higher energy barrier when gliding through the InGaAs QW due to alloy hardening[119,120]. The InAs dots within the InGaAs further raises the barrier due to precipitate hardening[121]. Consequently, the TD segment within the active region is relatively "pinned" as the rest of the TD glides through the crystal which leave MDs touching the active region in its wake.

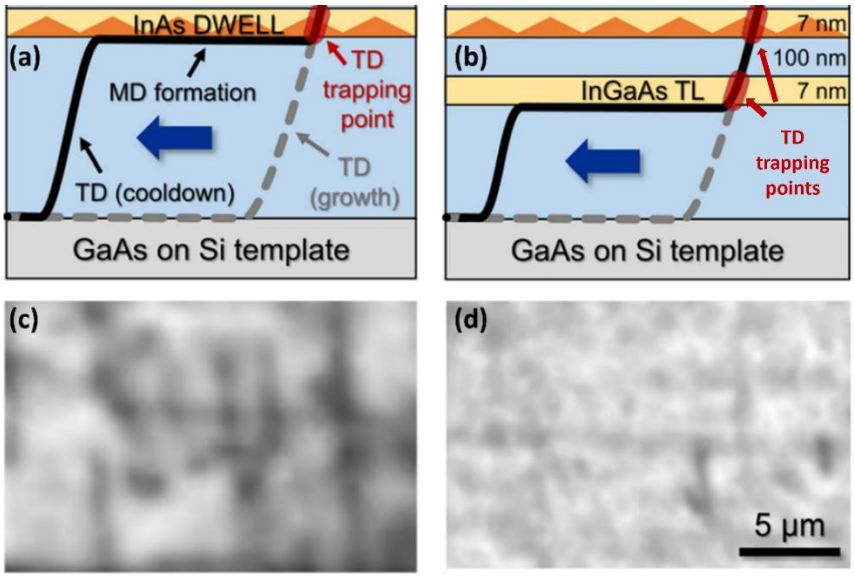

Figure 21: (a) Formation process of the MD touching the active region. (b) Defect configuration with the inserted InGaAs QW as the trapping layer. Monochromatic cathodoluminescence of the QD ground state emission (c) without and (d) with the inserted trapping layer[111].

MDs are more detrimental to the device performance than TDs as the MDs have a larger interaction area with the QDs. As shown in the cathodoluminescence (CL) image in Figure 21c, the MDs are non-radiative recombination centers and appears as dark lines. The solution is to utilize the hardening effect from the QWs and force the MDs to occur further from the active region, as shown in Figure 21b. The inserted InGaAs QW (TL) further extends the pinned TD segment, and the resulted MD does not touch the active region. As a result, the CL image lights up, as shown in Figure 21d, suggesting much less non-radiative recombination, which should translate to better device performance.

4.2 Suggested optimization of the trapping layer design

Currently, the trapping layer has the same indium composition and thickness as the QWs in the active region to avoid additional complication in the growth process. As shown in the tomographic

reconstruction below in Figure 22, the "trapping effect" is not perfect yet and a smaller number of MDs have escaped.

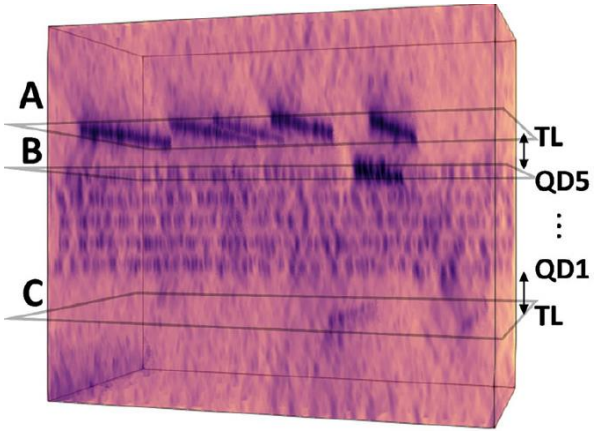

Figure 22: Tomographic reconstruction of a laser stack with TLs inserted in the top (p-side) and the bottom (n-side) cladding layers. 1 out of 7 MDs on the p-side has escaped the trapping effect. It is also observed that p-side has noticeably more MDs than the n-side[122].

The mechanical stability of the trapping effect has been theoretically investigated[118] suggesting a maximum allowed distance between the TL and the QD active region. When the excess stress (τ_{ex}) is above 0, the TD segment between the TL and the QD active region become unstable and bypass the trapping effect. Such bypassing process renders the TL non-effective as MDs can still form near the active region. As shown in Figure 23b, for the case of 0.15% thermal tensile strain, the $\tau_{ex} = 0$ case occurs when t_s = 110-150 nm. The result suggests that the bypassing effect could be reduced if the TLs are placed closer to the active region. Using a thicker TL or higher indium composition in the TL should be helpful as well. The maximum spacing requirement is greatly relaxed if the thermal strain is reduced to 0.1%. This thermal strain has a strong dependence on the TDD, film thickness, and the post-growth cooling rate, which will be discussed in the next section.

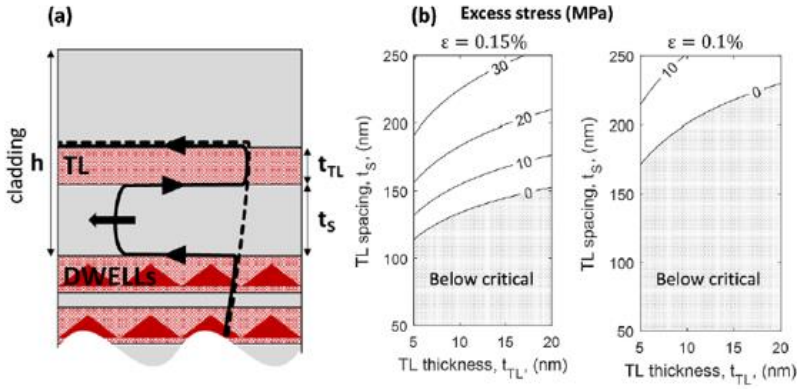

Figure 23: (a) Schematic illustration of the possible bypassing effect, leaving a new MD near the active region. (b) Contour maps of the calculated τ_{ex} for a range of t_s and t_{TL}. The "safe-zone" ($\tau_{ex} < 0$) is much bigger for the case with lower thermal strain[118].

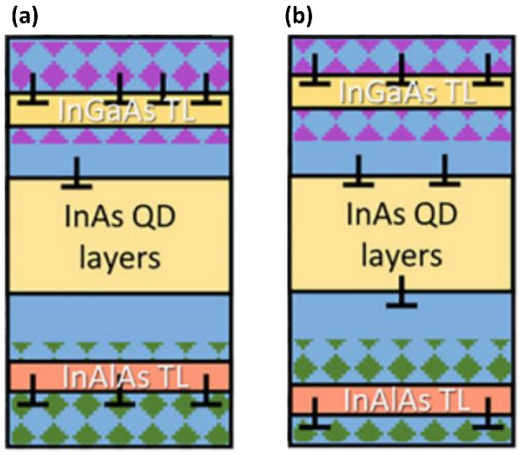

Figure 24: Schematic illustration of the tradeoff between TLs placed (a) closer and (b) further away from the active region[122].

On the other hand, the TLs need to be buried deep into the highly doped cladding region. The TL works not only to keep the MDs away from the QDs, but also to suppress the non-radiative recombination rate in the MDs. Thus, the MDs would need to be pushed into the highly doped cladding layers[122]. Figure 24 schematically illustrates this trade-off. The trapping effect is mechanically more stable when the TLs are closer to the active region, but the MDs would be in a lower doped region where non-radiative recombination is more prominent. More experiments are required to locate the optimum design for the trapping layer in terms of location, thickness, and indium composition. Such an optimum is expected to be a function of the laser stack design as well.

4.3 Cracking and wafer warping

The phenomena of crack formation and wafer warping will be discussed simultaneously since both are directly related to the residual thermal stress in the III-V film. Reducing the TDD has always been the focus for better device lifetimes. The TDD has been reduced to a point (TDD $\leq 1\times10^{6}$ cm^{-2}) where film cracking and wafer warping become more prominent after cooling, even on small samples. The expected cause is that the film becomes more brittle with lower number of existing defects. As mentioned in the previous section, existing defects experience a reverse glide process which partially help release the tensile strain. As the defect density is further reduced, a larger portion of the tensile strain would relax through crack formation and the sample curves up to accommodate for the high residual tension.

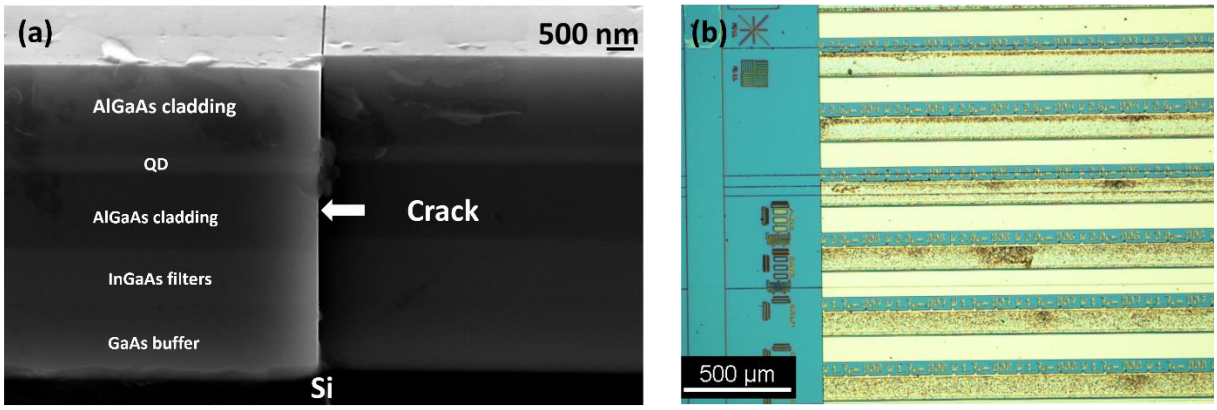

Figure 25: (a) Cross section SEM of an as-grown epi stack with a TDD < 1×10^{6} cm^{-2}. (b) A sample that didn't crack after cooling, yet experience server cracking after oxide hard mask deposition.

As shown in Figure 25a, cracks penetrate all III-V layers down to the Si substrate. In rare cases, cracking into the Si substrate has been observed. Even if, for some reason, the as-grown epi stack doesn't crack much, the film would experience severe cracking during fabrication as shown in Figure 25b. The standard 200 nm oxide hard mask exerts additional stress which can encourage the film to

crack. A simplified process of the different stress states that the sample goes through during growth, post-growth cooling, and fabrication is illustrated below in Figure 26.

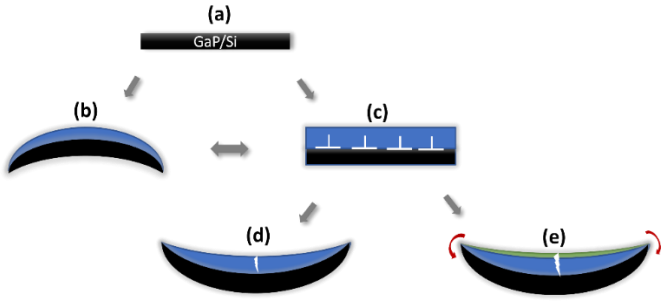

Figure 26: (a) Flat GaP-on-Si template before growth. (b) Deposition of III-V (blue) causes the sample to curve due to the compressive stress. (c) The compressive stress is relaxed through defect formation. (d) Crack formation as the film stress state is reversed and there are not enough defects to help release the tensile strain. (e) Deposited oxide hard mask (green) tends to bend the sample backward, which causes more severe crack situations.

The cracks severely reduce the device yield as the cleaving process becomes less reliable. High wafer curvature makes the wafer less manufacturable, especially for larger samples due to the higher deflection. The cracking and wafer warping issues are investigated both experimentally and theoretically; a mathematical model for GaAs/AlGaAs films on Si is proposed to describe the critical parameters for crack formation in terms of film thickness, post-growth cooling rate, and the defect density. To test this model, samples with different combinations of the above parameters are grown on a (001) Si template. The predicted remaining tensile strain after cooling and onset of cracking match well with observations. It is the first time that film fracture mechanics and dislocation-mediated plastic relaxation are combined to describe a well-known and yet unsolved problem in heteroepitaxial growth for optoelectronic devices.

4.3.1 Experimental procedure and results

All samples were grown in a Veeco Gen-II solid source MBE system on APD-free GaP/Si templates[71] produced on a slightly *p*-doped Czochralski Si wafer with a small offcut, approximately 0.15°, toward

the <110> directions. The initial 100 nm GaAs nucleation layer was grown at 500 °C and 0.1 µm/h and was cleaved into 2 cm-by-2 cm pieces. The sample holders were designed in a way that the samples were loosely held in place, with spring fingers barely touching the sample corners. Thus, the samples were allowed to deflect freely. Three different buffer layer structures were then grown on top to produce GaAs virtual substrates on Si with three different levels of TDDs. Figure 27 shows the schematics of the buffer structures and the corresponding electron channeling contrast images (ECCI) measured at the top surface. The buffer structure with a TDD of approximately 4×10^{8} cm^{-2} was generated by simply growing an additional 2.45 µm GaAs on top of the nucleation layer. To generate a TDD of 3×10^{7} cm^{-2}, thermal cyclic annealing (TCA) was applied after 1.6 µm of GaAs, where the sample temperature oscillated between 400 °C and 700 °C for 12 cycles under arsenic overpressure, followed by 950 nm GaAs. A TDD of 1×10^{6} cm^{-2} was achieved with the asymmetric graded InGaAs dislocation filter layer structure grown on top of a post-TCA 1.6 µm GaAs surface, as shown in Figure 27c. A $In_{0.1}Ga_{0.9}As$ layer was sandwiched between two $In_{0.05}Ga_{0.95}As$ layers and the structure was completed with a 300 nm GaAs capping layer. The InGaAs layers were grown at 500 °C with a 530 °C annealing step at each interface. The TDD of the buffer structure in Figure 27c has been verified with both ECCI and plan-view transmission electron microscopy[123]. All buffer layer structures had the same total thickness.

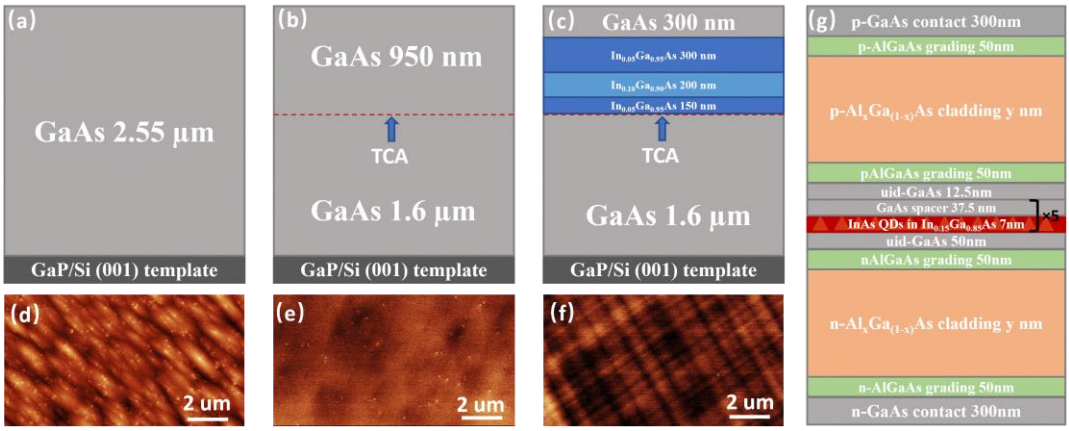

Figure 27: Buffer structures with a surface TDD of (a) 4×10^{8} cm^{-2}, (b) 3×10^{7} cm^{-2}, and (c) 1×10^{6} cm^{-2}. The red dashed lines in (b) and (c) indicate where TCA was applied. (d)-(f) are the ECCI images of the corresponding buffer structures above. (g) Schematic of the laser stack with varying aluminum composition and thickness of the top and bottom cladding layers.

To mimic the actual high performance QD laser material, full laser stacks with the QD active region and all the required doping profile were then grown on top of the buffer structures. The schematic of the simplified laser stack is shown in Figure 27g, with the aluminum composition and the thickness of the cladding layers as variables. A laser stack with 1.4 µm thick $Al_{0.4}Ga_{0.6}As$ cladding layers is referred to as "thick epi" while a laser stack with 700 nm thick $Al_{0.7}Ga_{0.3}As$ cladding layers is referred to as "thin epi". The laser stacks were grown under the same growth conditions. The layers below the QD active region were grown at 580 °C and the layers above the active region were grown at 540 °C to minimize the interdiffusion between the QDs and the surrounding material while maintaining a decent crystal quality. The QD active region was grown at 495 °C. The post-growth cooling rates were chosen to be either 1 °C/min or 100 °C/min, where the heater power was switched off after growing the top layer. The cooling rates were maintained from the final growth temperature to well-below 350 °C. The detailed parameters of all samples under investigation can be found in Table 2. The room temperature wafer curvatures, which could be translated to residual stresses, were measured in the Tencor Flexus system where a scanning laser detector was used to measure the surface position

across the sample width along the [1 1 0] and the [1 -1 0] crystal orientation and the curvatures measured in both directions were virtually the same. The surface cracking severity was investigated under scanning electron microscope (SEM). The results are summarized in Figure 28 below.

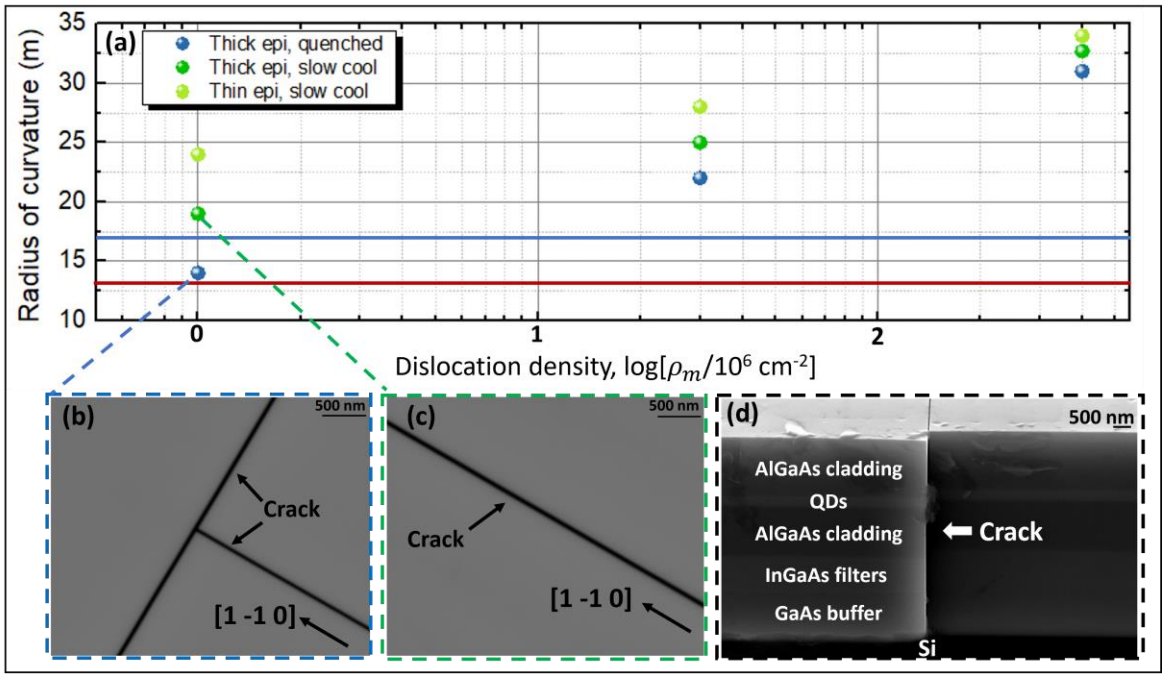

Figure 28: (a) Post-cooling wafer curvatures with respect to the TDD, epi thicknesses, and cooling rates. The horizontal lines indicate the lowest possible radius of curvature for both the thin (blue) and the thick (red) epi design estimated from the Stoney's formula (b) Cracks were observed in orthogonal directions when the thick epi is quenched on a 1×10^6 cm^{-2} TDD template, (c) while only cracks along the [1 -1 0] direction were observed when the same structure was cooled slowly. (d) Such cracks penetrate all III-V layers with the Si substrate still intact.

Table 2: Sample thicknesses, compositions, cooling rates, post cooling curvatures, and measured crack density of all 9 samples investigated.

Substrate	GaAs buffer layer		Laser stack			Post growth		
Thickness (µm)	Thickness (µm)	TDD (cm^{-2})	Thickness (µm)	Cladding layer Al composition	Final growth temperature (°C)	Cooling rate (°C/min)	Radius of curvature (m)	Linear crack density (cm^{-2})
		4×10^8	3.52	40%		100	31	0
						1	32.4	0
			2.1	70%			34	0
		3.5×10^8	3.52	40%		100	22	0

775	2.55				540	1	25	0
			2.1	70%			28	0
		1×10^6	3.52	40%		100	14	11
						1	19	2.5
			2.1	70%			24	0

For a given film thickness and a cooling rate, the samples with lower TDD exhibit smaller radii of curvature and thus higher residual tension after cooling down to room temperature. Though the III-V layers grown on the Si substrate do not relax completely, the residual compression from the lattice mismatch at the growth temperature before cooling can be neglected. Since the nucleation process of QDs is extremely sensitive to the strain state of the surface, this claim is supported by the fact that the nucleation of the QDs happened after depositing the same amount of InAs on all investigated samples as if the dots were grown on GaAs native substrate, irrespective of the starting dislocation density. Thus, the higher residual tension in the post-cooling incurred in the lower TDD samples can be ascribed to the lack of existing defects, which provides the only pathway for partially relaxing the tensile stress during their reverse glide and corresponding plastic dissipation. Similarly, the kinetics of thermally activated dislocation motion provide the rationale for the dependence of the residual tension on cooling rate. Regardless of the epi thickness and the cooling rate, and despite the wafer curvature difference, no cracks were observed at a TDD level of 3×10^7 cm^{-2} or 4×10^8 cm^{-2}, indicating that the plastic strains at such defect levels result in a lower equi-biaxial stress in the film after cooling. At a TDD level of 1×10^6 cm^{-2}, the fast cooled thick epi experienced cracking in both [1 1 0] and [1 -1 0] directions, as shown in Figure 28(b), with a linear crack density of approximately 11 cm^{-1}. Lowering the cooling rate to 1 °C/min resulted in a higher radius of curvature, and cracks were only observed along the [1 -1 0] direction with a linear density of approximately 2.5 cm^{-1}, as shown in Figure 28(c). A crack-free film with 1×10^6 cm^{-2} TDD is achieved with the thin epi cooled at 1 °C/min.

The fact that cracks were only observed when $R \leq \sim 20$ m implies that the cracking is avoided when plasticity during cooling relieves approximately one third of the thermal misfit stress. It is also

observed that at higher defect levels, the post-cooling wafer curvature (or the residual tensile stress) shows a weaker dependence epi stack thickness and the cooling rate. The interaction of defect density, cooling rate, and thickness on cracking can be understood using the model presented in the following section.

4.3.2 Mathematical model

For simplicity, the system is modeled as a single, monolithic, isotropic, elastic-plastic film on an isotropic, elastic, semi-infinite substrate. The laser stack and the buffer layer are treated as a single layer whose properties are taken as the average of the sublayers. Furthermore, it is assumed that the film is subject to biaxial stress and deformation, and that the film is stress-free immediately after deposition (as justified above). The substrate is also assumed to be thick enough that the sample curvature does not significantly alter the computed film stress. Cooling generates thermal misfit strains that induce plastic flow via thermally activated dislocation glide, which mitigates thermoelastic stresses that drive cracking. An increase in dislocation density will increase the plastic strains, lower the stress, and in turn lower the likelihood of cracking. Conversely, increasing the cooling rate will decrease the plastic strains, increase the stress, and in turn increase the likelihood of cracking.

The equi-biaxial stress in the film upon cooling can be written as:

$$\sigma(t) = \bar{E}[(\alpha_s - \alpha_f)(T(t) - T_0) - \varepsilon_{pl}(t)] \quad (8)$$

where $\bar{E} = E_f/(1 - v_f)$ is the biaxial modulus of film (with E_f as the elastic modulus and v_f the Poisson's ratio of the film), $\alpha_{s,f}$ are the coefficients of thermal expansion of the substrate and the film, respectively. As mentioned above, though the CTE values are temperature dependent, the CTE mismatch has a rather weak temperature dependence over the temperature range of interest (~300 K to 800 K), and the one obtains virtually identical results if this effect is included using the reported

values[112,113]. *T(t)* is the current temperature at time t, T_0 is the stress-free deposition temperature, and $\varepsilon_{pl}(t)$ is the equi-biaxial plastic strain that arises during cooling (in the absence of plastic strain, the thermal misfit in the laser stack and substrate upon cooldown corresponds to about ~ 240 MPa in the film). The evolution of plastic strains is assumed to be accommodated by thermally activated dislocation glide and driven by thermal misfit stress and line-tension from the TDs (which is additive to the misfit stress because of the reverse glide process[118]), such that the plastic strain rate is given by:

$$\dot{\varepsilon}_{pl} = b\rho_m v_0 exp\left[-\frac{Q}{kT(t)}\right]\left[\frac{n\sigma(t)}{\tau_*} + \frac{\mu b}{4n\pi(1-\nu)\tau_* h} ln(\alpha_e \frac{h}{b})\right]^m \quad (9)$$

where the dot denotes the time derivative, b is the Burger's vector of the threading dislocations, ρ_m is the dislocation density, v_0 is a characteristic reference velocity, Q is the activation energy for dislocation glide, k is Boltzmann's constant, $T(t)$ is the absolute temperature, μ is the shear modulus of the film ($\mu = E_f/(2(1+\nu_f))$), $\alpha_e \approx 1$ is a geometric constant, τ_* is a characteristic shear stress controlling creep rate, and h is the film thickness. The dimensionless factor n relates the resolved shear stress on the slip plane to the in-plane direct stresses generated by misfit, i.e. $\tau = n\sigma$; for high symmetry systems such as the one considered here, $n \approx 0.5$. This expression reflects the cumulative plastic strain rate owing to the collective glide of a population of dislocations[124], with a dislocation velocity mediated by temperature (first exponential term) and an effective stress (term in brackets). The latter includes the thermal misfit stress acting on the glide plane (first term in brackets) and the line tension of the TDs during reverse glide (second term in brackets); a similar treatment is discussed elsewhere[118]. Cases with and without the line-tension term are discussed in a later section.

The governing equations can be simplified to reveal controlling dimensionless parameters as follows. We consider a linear cooling step according to $T(t) = T_0 - Rt$, where T_0 is the initial stress-free reference temperature, and r is the cooling rate. Cooling from T_0 to a final temperature T_f therefore occurs over

the interval $t_f = (T_0 - T_f)/r$. The dimensionless time is defined as $\theta = t/t_f = Rt/(T_0 - T_f)$, such that stress and plastic strain evolve over the interval $0 \leq \theta \leq 1$. We define the dimensionless stress as $\Sigma(\theta) = \sigma(t)/\sigma_0$, where $\sigma_0 = \bar{E}_f(\alpha_f - \alpha_s)(T_0 - T_f)$ is the thermoelastic misfit stress, i.e., the stress that would occur in the absence of intervening plasticity (i.e., $\sigma_0 \sim 240$MPa). For convenience, we define a normalized plastic strain as $\xi(\theta) = \bar{E}_f \varepsilon_{pl}(\theta)/\sigma_0$. With these normalizations, the governing equations can be re-written as:

$$\Sigma(\theta) = \theta - \xi(\theta) \tag{10}$$

$$\xi'(\theta) = \tilde{\rho}\tilde{\sigma}_c^m exp\left(-\frac{\tilde{Q}}{1-\psi\tau}\right)[\Sigma(\theta) + \tilde{\sigma}_l]^m \tag{11}$$

where the prime denotes differentiation with respect to the normalized time θ, and the controlling parameters are:

$$\tilde{\rho} = \frac{E_f b \rho_m v_0 t_f}{2\sigma_0} = \frac{E_f b \rho_m v_0 \Delta T_0}{2R\sigma_0} = \frac{E_f b \rho_m v_0 \Delta T_0}{2RE_f(\alpha_s - \alpha_f)\Delta T_0} = \frac{b\rho_m v_0}{2R(\alpha_s - \alpha_f)} = dimentionless\ disl.dens. \tag{12}$$

$$\tilde{Q} = \frac{Q}{kT_0} = dimensionless\ activation\ energy\ (at\ deposition) \tag{13}$$

$$\tilde{\sigma}_c = \frac{\sigma_0}{\sigma_*} = \frac{E_f(\alpha_s - \alpha_f)\Delta T_0}{\sigma_*} = dimensionless\ thermal\ stress\ rel.to\ creep\ stress \tag{14}$$

$$\tilde{\sigma}_l = \frac{b}{4\pi(1-\nu)h(\alpha_s - \alpha_f)\Delta T_0} ln\frac{\alpha_e h}{b} = dimensionless\ line\ tension\ rel.to\ thermal\ stress \tag{15}$$

$$\psi = \frac{T_0}{T_0 - T_f} \approx 1 = initial\ temperature\ relative\ to\ change \tag{16}$$

A single non-linear ordinary differential equation for stress as a function of time can be obtained by taking the derivative of Eqn. (3) with respect to τ and using Eqn. (4) to eliminate the plastic strain rate term. The problem is solved with $\Sigma(0) = 0$ (zero stress at the start of cooling), while $\Sigma(1)$

represents the final stress state after cooling. Table 3 provides a summary of the expected ranges of input parameters for the present system, which are used to generate results in the next section.

Table 3: Material parameters used in the calculations obtained from the reported values.

Substrate			Film			Plasticity				
Elastic modulus (GPa)	**Poisson's ratio**	**CTE (K^{-1})**	**Elastic modulus (GPa)**	**Poisson's ratio**	**CTE (K^{-1})**	**b (Å)**	**Q (J)**	**τ_* (MPa)**	**ν_0 (m/s)**	**m**
155	0.26	2.6×10^{-6}	107	0.35	5.45×10^{-6}	4	2.1×10^{-19}	1	1.9×10^{3}	1.7

The 300 mm Si substrates used are produced from CZ-grown crystals within standard CMOS-compatible specifications. The residual doping is *p*-type with a vendor determined resistivity of approximately 15 ohmcm. All lasers were grown on cleaved pieces from the center of the 300 mm template. Based on the commonly accepted values for Si and experiments done on the specific type of Si wafer, an educated guess was performed for the elastic properties of the Si template used[125,126]. The elastic parameters for the film are the weighted averages of the values from the literature[127]. The CTE values for both the substrate and the film are the room temperature values. The Burger's vector, b, equals $\frac{a}{\sqrt{2}}$, which is approximately 4 Å, where a is the lattice constant. For the empirical plasticity parameters used for the thermally activated glide model, the values were obtained by Yonenaga and Sumino[128], and a similar treatment was used elsewhere[118].

With the measured residual stress via wafer curvature, the propensity for cracking can be analyzed by computing the energy released by a channeling crack through the film[129]. The steady-state energy release rate for an isolated crack that extends large distances relative to the film thickness is considered here, which represents the maximum possible crack driving force. For the present system (where the modulus of the film is lower than that of the substrate), this is given by:

$$G(\theta) = \frac{\pi}{2}\frac{(\sigma(t))^2 h(1-\nu_f^2)}{E_f} = \frac{\pi}{2}\frac{\sigma_0^2 h(1-\nu_f^2)}{E_f}\Sigma(\theta)^2 = G_0\Sigma(\theta)^2 \quad (10)$$

where G_0 represents the maximum possible energy release rate in the absence of intervening plasticity, i.e., the driving force for cracking arising from thermoelastic misfit strains that are not mitigated plastic strains. Note again that with the present normalization, $\Sigma(\tau) \leq 1$.

4.3.3 Results and discussion

Figure 29 plots the energy release rate (ERR) for isolated channeling cracks obtained from stresses calculated directly from wafer curvature measurements after cooling (shown in Figure 28). Since G $\propto \sigma^2$, the ERR results also reflect the differences in the final stress state resulting from differences in dislocation density and cooling rate. The boundary between cases with and without cracking falls between $1.5 < G < 2$ J/m^2; only the thick epi and low dislocation density samples experience cracking, i.e. the solid circles above the toughness line. At the lower cooling rate and the lowest dislocation density, the linear crack density is a factor of four smaller than the higher cooling rate, strongly suggesting the critical energy release rate is just below 1.8 J/m^2. This corresponds to a toughness of $K_C = 0.37$ MPa$\sqrt{m}$ and falls in the middle of the range reported elsewhere[130–132]. It should be noted that in the absence of intervening plasticity, the thermoelastic misfit stresses from cooling have a driving force of G ~ 5 J/m^2, which is well above the reported toughness values for GaAs; as such, cracking will occur in all of the present cases in the absence of any dislocation-mediated relaxation. Since the ERR scales linearly with stack thickness, this implies that a stack thickness below ~ 2.04 μm will not crack even in the limit of zero dislocation density.

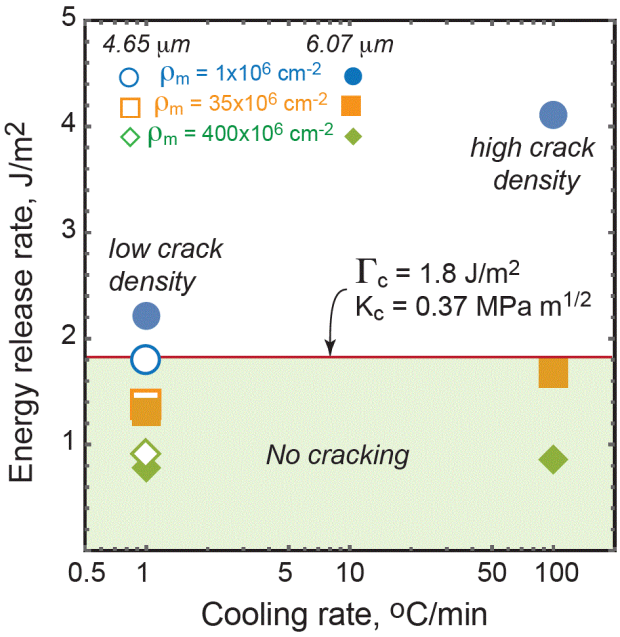

Figure 29: ERRs, obtained from the stresses computed from wafer curvature measurements, for isolated channeling cracks as a function of cooling rate, for three dislocation densities.

The plasticity model described above provides some insight regarding the coupling between dislocation density and cooling rate. Figure 30a plots the residual stresses obtained as a function of cooling rate for the dislocation densities observed in the experiments. The results are scaled by the thermal misfit stresses that occur in the absence of intervening plasticity; calculations for cases both with and without the line-tension are included. Including the line-tension term lowers the predicted final residual stresses; these cases result in better agreement with the experiments for higher defect levels (ρ_m= 3.5×10^7 cm^{-2} and 4×10^8 cm^{-2}) but poorer agreement for low defect levels (ρ_m = 1×10^6 cm^{-2}). The discrepancy may arise from additional dislocation pinning in the InGaAs filters in the low defect template. Figure 30b plots contours of the corresponding energy release rates as a function of both cooling rate and dislocation density. The results shown in Figure 30a, b, and c were generated with Q = 2.1×10^{-19} J and m = 1.7 and without line tension, as this provides better agreement with cases with the low defect density. The contour for 1.75 J/m^2 < G < 2 J/m^2 separates conditions expected to crack (above the shaded zone) and those not expected to crack (below the shaded zone).

The shaded zone in Figure 30b illustrates the trade-off between dislocation density and cooling rate, with slower cooling required to avoid cracking for lower dislocation densities. The ERR prediction gives a weaker dependence on defect density and cooling rate with increasing defect density and decreasing cooling rate, respectively, which is consistent with the experimental observation that the residual tensile stress is less sensitive to film thickness or cooling rate at higher TDD. Despite the differences between the stress prediction and the experimental measurements of wafer curvature, the correct conclusion regarding cracking is obtained for 5 of the 6 experimental conditions. Due to the over-prediction of stress for a cooling rate of 100 °C/min and dislocation density of ρ_m = 35×10^6 cm^{-2}, one predicts cracking that is not observed experimentally. Figure 30c shows the contours of the maximum tolerable film thickness to avoid crack formation as a function of defect density and cooling rate. It suggests that for a ρ_m = 1×10^6 cm^{-2} and a cooling rate of 1 °C/min, the film would not crack until 6~6.5 µm. Yet, a 6.07 µm film cracked at that TDD level and cooling rate, suggesting an underestimate of the residual stress, similar to the results shown in Figure 30a. Clearly, improvements to the plasticity model that incorporate the true complexity of the device layers and other potential dissipation pathways will provide more accurate estimates of stress and more precise regime maps. Future work should focus on more detailed dislocation motion models, defect annihilation and pinning during the reverse glide process.

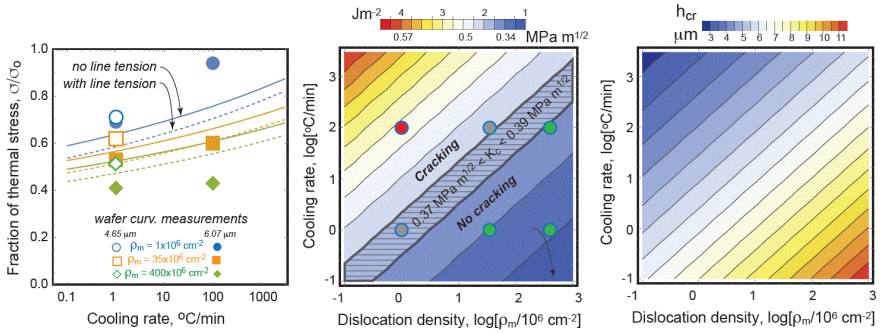

Figure 30: (a) Stress as a function of cooling rate, for three dislocation densities, with wafer curvature results superimposed. (b) Contour map of predicted energy release rate as a function of dislocation density and cooling rate; conditions above the critical line are expected to crack, while those below the line are not expected to crack. The predicted stresses are higher

than those observed for the middle of the top row, such that cracking is predicted despite observations to the contrary. (c) The contour of the critical film thickness for crack formation with respect to the dislocation density and the cooling rate for the given film toughness.

It is worth mentioning again that both the physical experimental setup and the mathematical model allow the samples to deflect freely during cooling down. Additional constraints may act to increase the stress and likelihood of cracking. Growing such laser materials inside pre-defined trenches would mitigate the issues with the residual tension, provided the GaAs debonds from the side walls. In such cases, the edges of the strips are stress-free, and the stress at the center is lower than in blanket films, provided the width of the trenches is comparable to the length-scale associated with shear transfer along the film/substrate interface[129]. Aligning the trenches along the [1 -1 0] crystal direction, together with thinner epi design and slower cooling rate, would significantly suppress the likelihood of cracking.

4.4 Summary

The above findings of the formation of MDs near the active region suggest that the previously improved device performance from TDD reduction could be attributed to removing the MDs one-by-one. Inserting TLs aims to attack the problem by directly repelling the MDs into the highly doped cladding layers. Further optimization is required in terms of the composition, thickness, and location with respect to the specific laser stack design. Yet, the film is expected to be more rigid as longer segments of the TDs are pinned.

Though the model developed to predict the onset of cracking exhibit acceptable accuracy, it under predicts the relaxation for the high defect samples and over predicts for the low defect samples. This suggests that other paths of relaxation and defect pinning exist, respectively. Currently, the model assumes the III-V film is uniform with averaged properties from all the consecutive layers. A detailed breakdown of each layer and dislocation model with core structure, doping effect, and active region/filter layer pinning effect included would greatly increase the model accuracy. Prediction of

the crack asymmetry, crack density, and the temperature at which the crack initiates would then be possible.

Chapter 5
Breakthrough reliability at elevated temperatures

As mentioned in earlier chapters, direct epitaxial growth of III-V material on Si represents a more economically favorable option than bonding, with additional room for improvement as this scheme provides the best natural heatsinking for laser operation. Yet, due to the dissimilarities between III-V materials and Si, electrically active cyrstalline defects, especially the TDs that penetrate all device layers and the MDs formed near the active region, are generated during the hetero-epitaxial growth. Previously, the device extrapolated life time, defined as the time required to double the initial threshold current, of the MBE grown InAs QD lasers was improved from 800 h to more than 10,000,000 h at room temperature after reducing the TDD from 3×10^{8} cm^{-2} down to 7.6×10^{6} cm^{-2}. Including *p*-modulation doping resulted in a lifetime of 7 years at 60 °C[133]. However, such performance is not enough for real world applications where the ambient temperature is around 70 °C to 80 °C within the datacenter racks. The extrapolated lifetime is also not long enough. Figure 31 shown below is the aging data done at Intel on bonded QW lasers operating at 80 °C, and no apparent degradation was observed after 25,000 hours. Thus, epitaxially grown devices would need to reach such performance to be commercially viable.

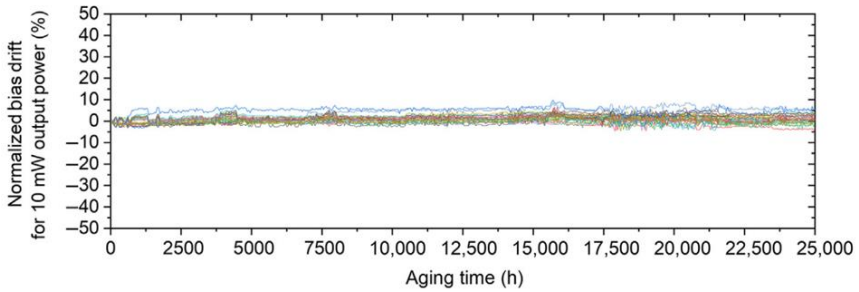

Figure 31: Bias change for 10 mW output power aged at 80 °C for bonded QW lasers.

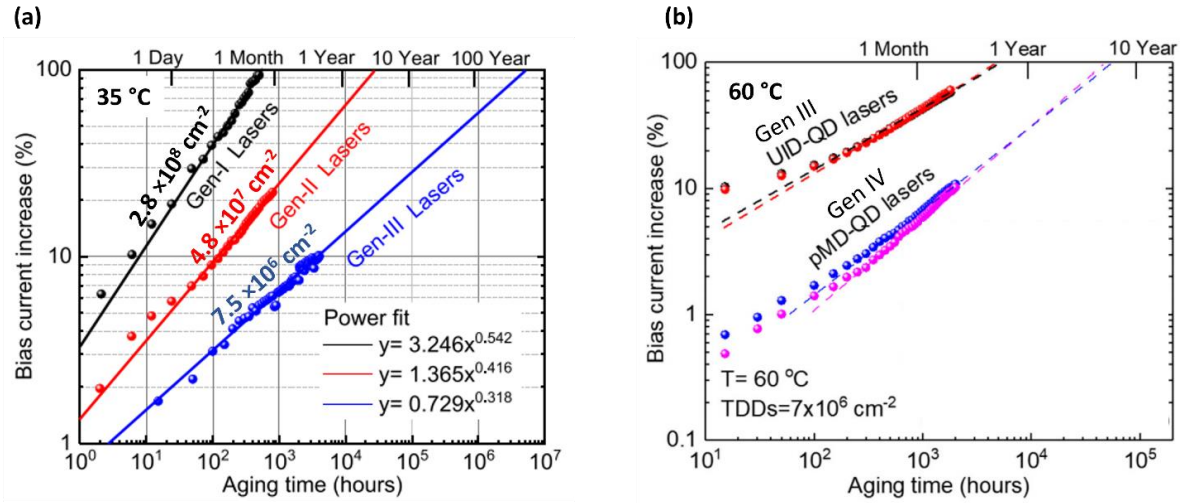

Figure 32: (a) Room temperature aging data for the epitaxial QD lasers on Si with three different levels of TDD. (b) 60 °C aging data. The Gen III laser lifetime dropped from >100 years to ~6000 hours. Introducing *p*-modulation doping increased the lifetime to about 8 years due to improved differential gain at higher temperatures.

5.1 New generation of QD lasers on Si

With the previously introduced defect management tools, asymmetric graded (ASG) dislocation filters for lower TDD and TLs for MDs, the device performance is expected to be greatly improved. To demonstrate the expected longer lifetime at higher ambient temperatures, multiple on-Si lasers were grown as shown below. All the samples were grown in a Veeco Gen-II solid source MBE on an APD-free GaP/Si(001) on-axis template. The growth of the initial 1.6 µm GaAs and the TCA process were described in detail in Chapter 3. Two different DFL designs were implemented. The first design involved a single 200 nm $In_{0.10}Ga_{0.90}As$ insertion layer referred to as the baseline (TDD = 7×10^6 cm$^-$

^{2}), while the second design utilized the ASG filters for low a TDD template (TDD $\leq 1.5\times10^{6}$ cm^{-2}). Both designs were completed with a GaAs capping layer to bring the lattice constant back to that of GaAs, and the total buffer thicknesses were kept the same. Two laser stack designs were utilized. The TLs consisted of 7-nm-thick *p*-$In_{0.15}Ga_{0.85}As$, and *n*-$In_{0.15}Al_{0.85}As$ strained quantum wells (QWs) were inserted in the *p*- and *n*-cladding layers, respectively. The materials were chosen for band alignment to minimize disturbance in the electrical properties of the laser stack. The QWs were 180 nm away from the QD active region. The active region, with an expanded schematic shown below, consists of 5 layers of InAs QDs embedded in $In_{0.15}Ga_{0.85}As$ QWs. 10 nm GaAs within each barrier layer between the dot layers was *p*-doped to 5×10^{17} cm^{-2}, namely the pMD, for high temperature performance[52]. The optimum growth temperature for nucleating QDs was 495 °C with an indium growth rate of 0.11 ML/s and a V/III ratio of 35. The laser stack without TLs was grown on the baseline buffer structure with *p*-modulation doping for comparison (the previous best laser, Sample A). Detailed sample structures are shown in Figure 33a and the room temperature photoluminescence (PL) spectra of the as-grown samples are shown in Figure 33b. The inset shows the AFM image of the uncapped dots. By growing on the low TDD template and by inserting the TLs (Sample C), the PL intensity increases approximately 60% compared to the standard design (Sample A). The as-grown materials were then fabricated into narrow ridge Fabry-Perot (FP) lasers with ridge width varied from 2 to 5 μm. The fabricated lasers were then cleaved into 1500 μm long bars after thinning down the Si substrate to approximately 180 μm.

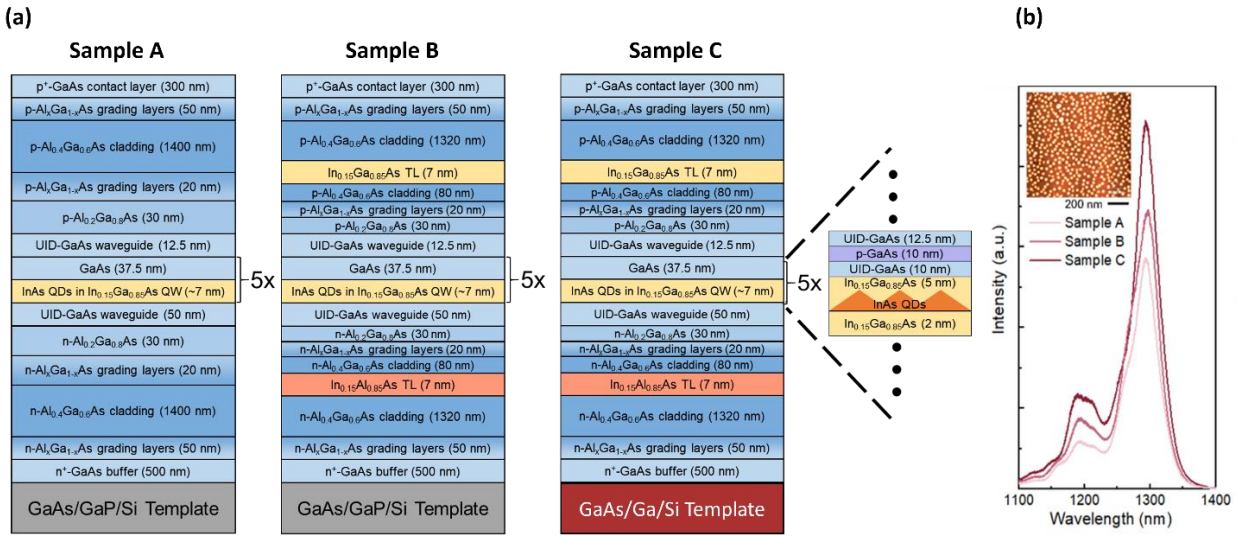

Figure 33: (a) Detailed schematics of the three on-Si lasers grown. Sample A is the previous best laser structure with a TDD of 7×10^6 cm^{-2} and no TLs. Sample B has the same TDD but with TLs inserted, and Sample C has a TDD no more than 1×10^6 cm^{-2} and TLs inserted. (b) Room temperature PL spectrum of the as-grown lasers.

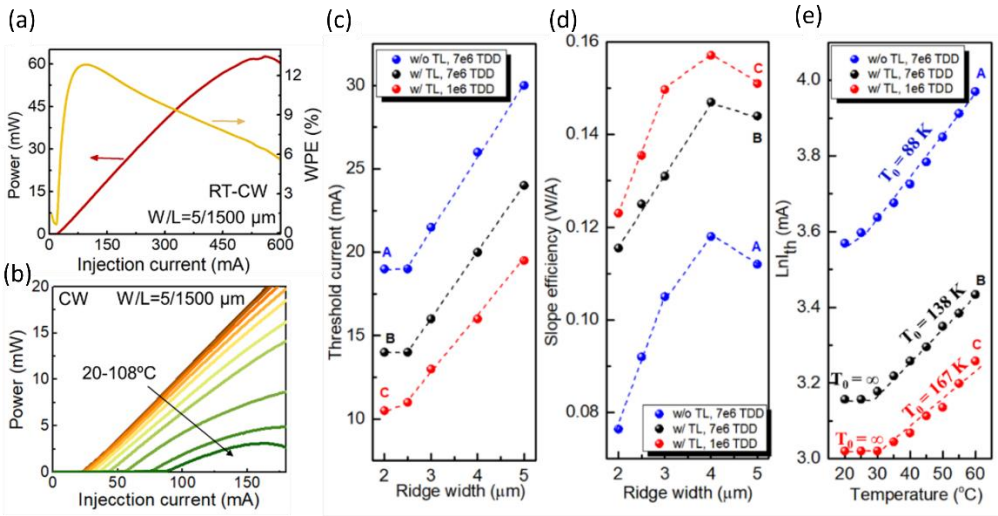

Figure 34: (a) and (b) are representative LI curve of the best performing devices. (c)-(e) are the comparisons between devices from different epi designs on threshold currents, slope efficiencies, and characteristic temperatures, respectively.

All light current voltage (LIV) characteristics are measured under CW conditions. A representative room temperature (RT) LI curve from Sample C is shown in Figure 34a, with a double-sided wall-plug efficiency of 12.6% and a maximum single side output power of 65 mW. Figure 34b shows the

exhaustive temperature measurements done on the same device. A maximum CW lasing temperature of 108 °C was obtained, limited by the maximum stage temperature. Figure 34c-e summarize the LIV characteristics of the best as-cleaved devices from all three samples. Sample A has an overall similar performance compared to our previously reported results with the same buffer TDD and laser stack design[134]. By inserting the TLs in the top and bottom cladding layers (Sample B), the threshold current, slope efficiency, and high temperature performance are all significantly improved compared to Sample A. Incorporating the ASG buffer with the TLs (Sample C) provides additional improvement in the performance. A record low RT threshold current density for *p*-modulation doped InAs QD laser of 266 A/cm^2 and a high slope efficiency of 0.158 W/A were achieved in Sample C. In Figure 34e, by fitting to the exponential function of $I_{th} = I_0 \exp\left(\frac{T}{T_0}\right)$, where I_{th} is the threshold current at a given stage temperature T, the CW characteristic temperature, T_0, was measured to be as high as 167 K for Sample C between 30 °C and 60 °C. The threshold current was essentially unchanged between 20 °C to 35 °C. The high temperature performance was only measured up to 60 °C for most of the devices in order to not degrade their performance before aging.

To investigate the origin of the performance improvements, a representative device from each of the three designs was chosen to measure the modal gain and transparency current density, using this method described elsewhere[74]. Nearly identical gain coefficients were extracted for all three devices with a logarithmic gain model in Figure 35a, while the devices from Sample B and C had a noticeably lower transparency current density, as shown in Figure 35b. The reduction in transparency current, attributed to reduced Shockley-Read-Hall recombination from defects, is believed to be the source of performance improvements in Sample B and C.

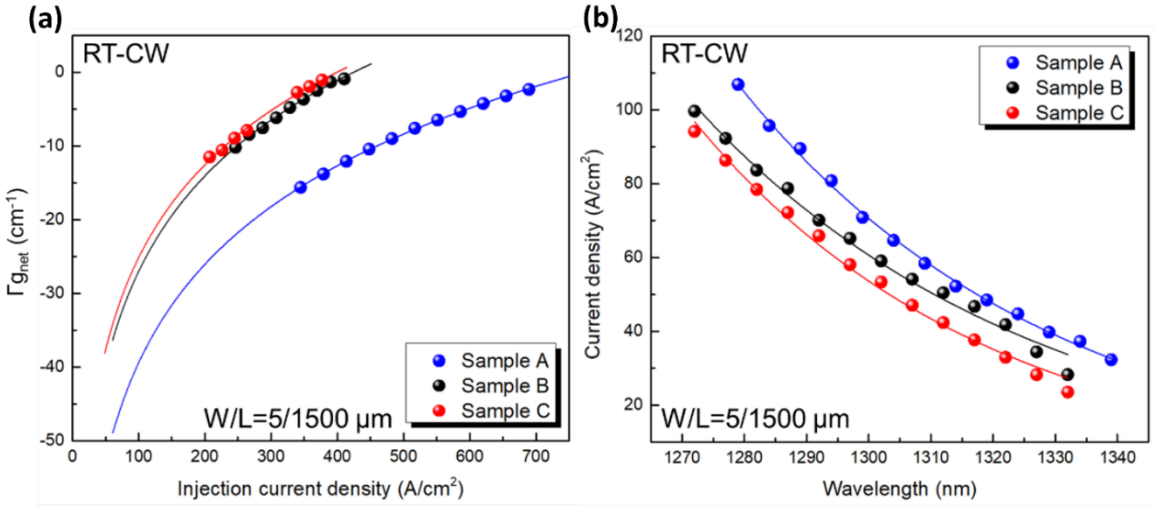

Figure 35: (a) Net modal gain as a function of injection current density, and (b) transparency current density as a function of wavelength on one as-cleaved device from each sample.

5.2 Aging experiment setup and results

High-reflective (HR) coatings were then applied on both facets of laser bars chosen for aging, with 60% reflectivity on the front and 99% reflectivity on the rear. The devices were singulated into small dies and mounted onto AlN carriers. The device-carrier assemblies were loaded into an ILX LRS-9434 reliability test rack with the front facet facing the internal photodetectors. The LRS-9434 is a high-density, high reliability laser lifetime test system provided by Intel. Different test scenarios can be executed simultaneously in the chamber. As shown in Figure 36, the aging rack holds up to eleven independent control measure modules (CMMs). Each CMM can include up to four laser diode fixtures. The AC power cables and the Ethernet cables for software control of the aging tests are routed at the back of the rack. The aging rack is able to test up to 1408 devices simultaneously with a 500 mA maximum drive current per device, and the ambient temperature can be tuned from 40 °C to 120 °C. The control software, ReliaTest, allows real-time viewing of both the currently running test data and the data for the completed tests. Intuitive graphical user interface simplifies the test control.

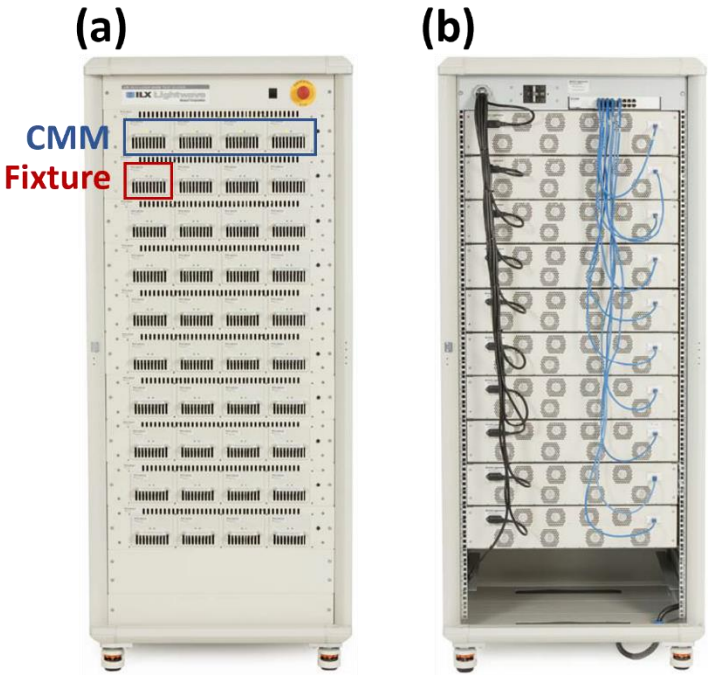

Figure 36: (a) The front of the aging system. Each CMM holds four fixtures. (b) The back of the aging system.

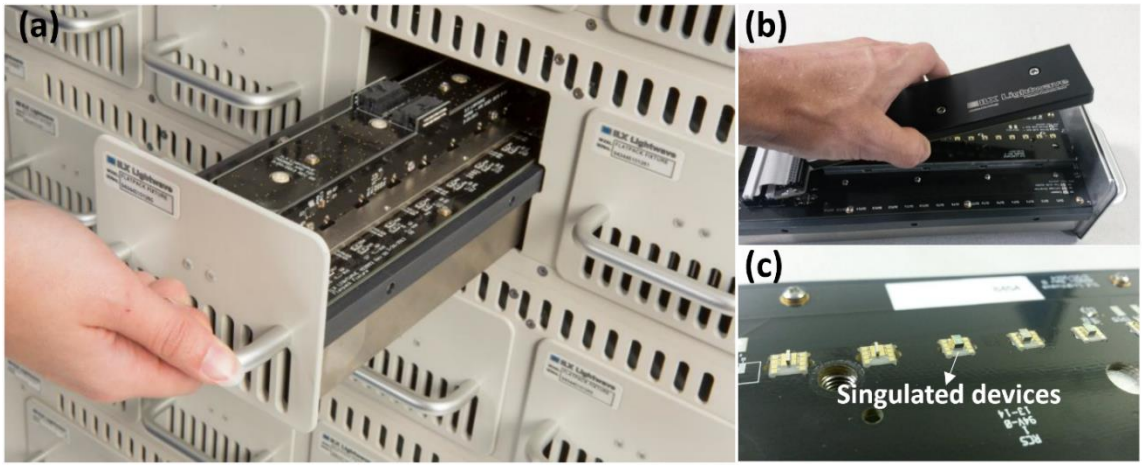

Figure 37: Zoomed in views of the individual fixtures. (a) The drawer-like configuration of the fixture; (b) the removable top cover and (b) the singulated devices on mounted carriers.

The removable fixture consists of a stainless-steel airflow plenum, face plate with handle and air intake, main PCB, nickel-plated temperature-controlled aluminum device plate, rear connector with alignment features, and clamping/optical power measurement assembly. Figure 37c illustrates an

example of the singulated devices/AlN carrier assembly. Each fixture is able to hold up to 16 carriers and 2 devices could be attached to each carrier.

Since the ambient temperature at which the on-chip lasers would be operating in datacenter processors is up to 80 °C, all devices were aged at 80 °C and biased at 2 times their average 80 °C threshold currents. LIV characteristics were measured automatically before aging and after each 50-hour interval during the 4000-hour aging run. The evolution of LI curves for the hero devices from each sample are shown in Figure 38a-c. Previously, devices from Sample A showed an extrapolated lifetime of about 8 years at 60 °C. Yet, such devices "died" within the first 4000 hours of aging at 80 °C, suggesting a strong temperature acceleration of the degradation process. Compared with Sample A, adding the TLs in Sample B has greatly improved the stability of the LI curves over the course of 80 °C aging. The threshold current change was reduced from 104% to 27.6%. Using the low TDD buffer in addition to the TLs in Sample C further reduced the threshold increase to only 10.4%. This suggests that effectively removing the MDs formed during the post-growth cooling process with the inserted TLs is the key to high device reliability. This makes sense as reducing TDD is effectively removing MDs one at a time, and inserting TLs attacks the MD problem directly. Figure 38d shows the aging data for the hero device from Sample C. The extrapolated lifetime from the hero devices from Sample C was found to be more than 200,000 hours. Table 4 summarizes the progress of in obtaining the highly reliable epitaxial QD lasers on Si over the last few years. With minimum change in the actual laser epi design, the extrapolated lifetime has been increased from 800 hours at room temperature to more than 200,000 hours at 80 °C by carefully managing the crystalline defects.

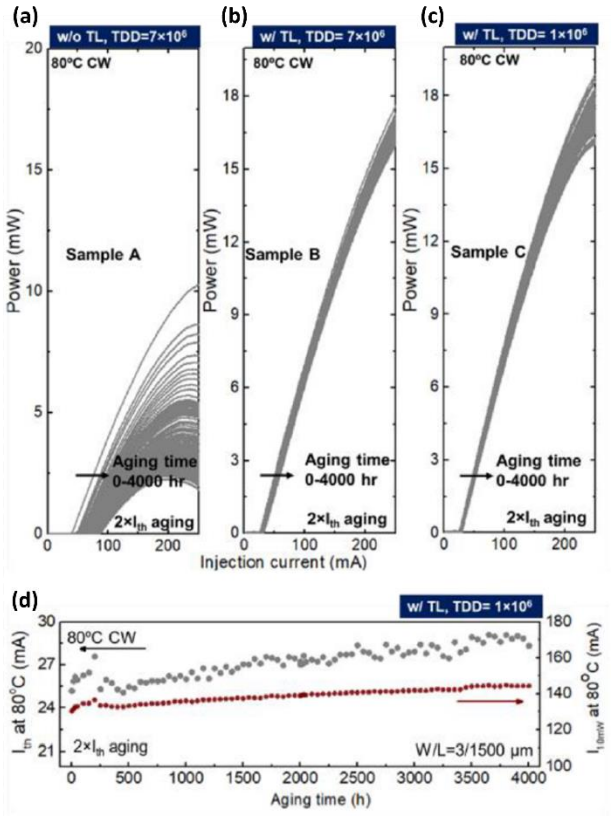

Figure 38: (a), (b), and (c) are LI evolutions for the lasers from Sample A, B, and C aged at 80 °C, respectively. The lasers from Sample A have experienced a threshold current increase of 104% within 4000 hours and Sample B has seen a 27.6% increase. The threshold currents of the best devices from Sample C have only increases by 10.4%.

Table 4: Summary of the main aging results in the last few years[53,86,122,133].

material generation	innovation	TDD (cm^{-2})	TL position (nm)	pMD (cm^{-3})	aging temp (°C)	extrapolated lifetime (h)		
						35 °C	60 °C	80 °C
Gen I	GaP/Si to remove APD	2×10^8	N/A	0	35	**~800**	N/A	N/A
Gen II	TCA to reduce TDD	7×10^7	N/A	0	35	**~20 K**	~2 K	N/A
Gen III	SLS to reduce TDD	7×10^6	N/A	0	35/60	**>1 M**	**~2500**	N/A
Gen IV	pMD for high T performance	7×10^6	N/A	5×10^{17}	60	~9 M	**~70 K**	<500
Gen V.A	TLs to block MDs	3×10^7	180	5×10^{17}	60	>1 M	**>1 M**	~11 K
Gen V.B		3×10^7	80	5×10^{17}	60/80	>1 M	**~90 K**	**~30 K**
Gen V.C		7×10^6	180	5×10^{17}	80	>1 M	~1 M	**~100 K**
Gen VI	ASG filter for record low TDD	1×10^6	180	5×10^{17}	80	>1 M	>1 M	**>200 K**

For a long time, reducing TDD in the buffer was the primary path in achieving reliable epitaxially grown on-chip light sources. However, with dislocation interactions being the only mechanism of

filtering in bulk films, the likelihood of two dislocations meeting each other becomes extremely low once TDD gets sufficiently low. Even with the ASG structure here to reduce the TDD to lower than 1×10^6 cm^{-2}, this value is still two to three orders of magnitude higher than that of the state-of-the-art native III-V wafers at 10^3-10^4 cm^{-2}. Material quality comparable to the latter is not likely to happen for bulk III-V deposition, but it should be possible for QD deposition. The above systematic comparisons of aging data show that the successful application of TLs can improve the reliability of on-Si lasers by over 200 times compared to those without such TLs and is the key in achieving highly robust laser operation. Unlike conventional dislocation mitigation strategies, the TL reduces neither the number of TDs nor the number of MDs. By shifting the position of MDs away from the QD layer, the impact of defects on device performance can be greatly mitigated[111]. Though the obtained device reliability is still not sufficient for actual datacenter applications, the above demonstration points out that the path to further obtaining more reliable monolithically integrated on-chip light source is to develop strategies to effectively removing the MDs from the active region.

5.3 Proposed new laser design

Although devices from Sample C have shown record long extrapolated lifetime at 80 °C, as can be inferred from the results shown in Chapter 4, high density of cracks were found in the as-grown Sample C material due to the low defect density. These cracks not only limit the device yield from Sample C, but they could also be affect the device performance as well since they would potentially block the heat flow. For the same geometry, devices from Sample C experience thermal rollover about 100 to 150 mA sooner than those from Sample B, despite the lower threshold, higher slope efficiency, and higher T_0. As suggested in Chapter 4, growing thinner III-V layers and cooling slower would reduce the likelihood of crack formation and at a total III-V layer thickness of 2.04 μm, no cracks should be observed even with zero dislocation density. This 2.04 μm total III-V thickness is not that realistic, as thick enough layers are required for optical confinement, defect reduction, and electrical

contacts. However, the results suggest that if a much thinner stack than the current design (6.5 μm) could be obtained, another benefit besides having crack-free III-V films would be less MDs near the active region as the need for tensile relaxation via TD reverse glide is reduced. In order to compensate for the reduced optical confinement with the thinner laser stack, the aluminum composition in the cladding layers was then increased from 40% to 70%. The cladding layer thickness could then be reduced from 1.4 μm to 700 nm on each side. The intensity difference between the sample (high vs. low TDD, with vs. without TLs) is smaller, suggesting that the MD formation is less prominent in the thinner stacks. It is also possible to reduce the buffer layer thickness with better filter designs to maintain the defect density level. However, fabrication of the 70% Al lasers proves to be trickier as the high aluminum content layers are subject for void formation. These voids add another layer of uncertainty to the device performance. No meaningful conclusion can be drawn on whether thin lasers would function better or worse before the void problem is solved with tighter fabrication tolerance.

5.4 A short note on growth calibration

As was seen in the PL spectra of the as-grown lasers in Figure 33(b), despite the intensity differences, the PL wavelengths of the ground state emission are all centered at 1293 nm (±1 nm). The PL wavelength is extremely sensitive to the InGaAs composition and the QD quality in the active region (given that the temperature is calibrated accurately), and thus, the In and Ga growth rates. The Ga, together with Al, growth rate is calibrated with distributed Bragg reflector (DBR) stacks, and this method is accurate within 1%. However, the indium growth rates are originally calibrated via RHEED oscillations when growing InAs on InAs native substrates. This method is inherently less accurate as it would depend on the software used and the RHEED screen quality. Since the indium is grown on a InAs substrate but not on GaAs, a growth rate conversion is required, and the indium sticking coefficient would change if other Group III atoms are present during the growth. Historically, for the

above-mentioned reasons, the wavelengths of the best PL structure between each growth campaigns have been swinging from 1275 nm to 1295 nm.

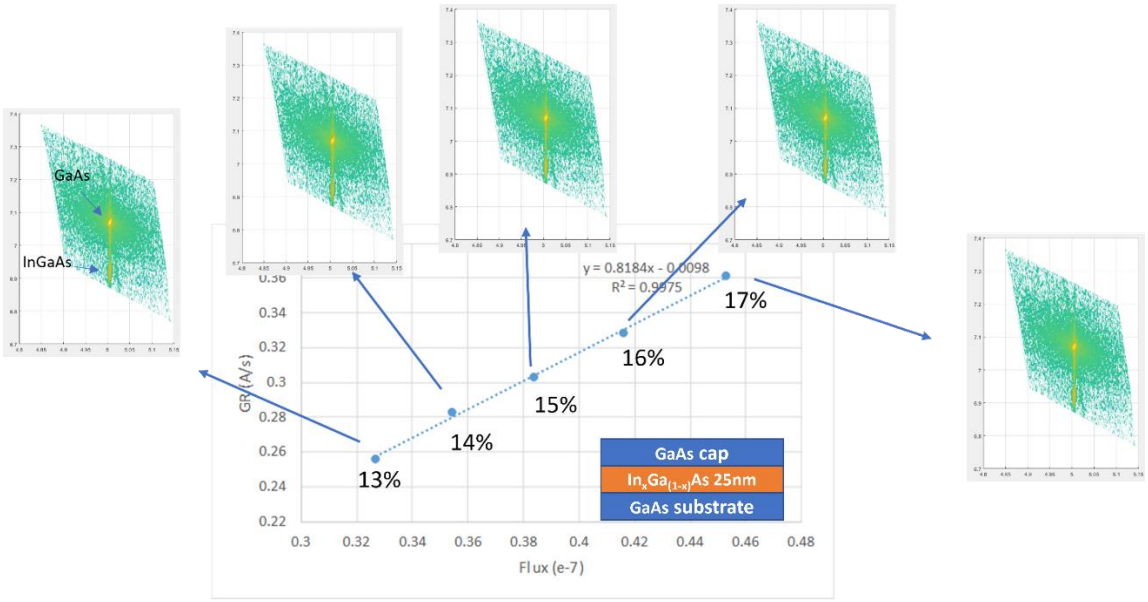

Figure 39: Indium growth rate/InGaAs composition calibration with XRD. Five different Indium fluxes were used while keeping the Ga flux the same. RSMs confirmed that the InGaAs layers were 100 % strained. The plot of the In growth rate vs. flux should be linear.

In order to have a more accurate indium growth rate calibration, so that the active region difference between each laser sample is negligible during the aging test, another calibration is proposed using XRD. The sample structure is very simple as shown in the Figure 39. The $In_xGa_{(1-x)}As$ thickness is chosen to be 25 nm. The indium composition of interests falls between 10% to 20%, and a layer thickness of 25 nm ensures that the InGaAs layer is fully strained to make the XRD data easier to interpret. The 25 nm is also the minimum acceptable thickness to have enough signal on the XRD. The RSM scans have shown that the InGaAs layers with different compositions are indeed fully strained and the extracted indium compositions fall in a straight line with respected to the indium fluxes. Using this calibration method, the PL wavelength hits 1293 nm on every laser growth. Thus,

the PL intensity and the device performance difference could be sole attributed to the laser stack quality.

5.5 Summary

For the first time, the epitaxially grown QD lasers on Si has demonstrated an over 200,000 hour extrapolated lifetime at 80 °C under CW operation. This is achieved by carefully managing the crystalline defects with ASG filters and TLs. Yet, as the defect level is approaching the native substrate level, the film exhibits higher tendency to crack as the plastic flow strain is reduce. The surface cracks limit the device yield and the potentially the performance. As suggested in Chapter 4, thinner stack designs would be preferential to circumvent the cracking issue by lowering the energy release rate. Only then the full potential of the low defect templates and the TLs on improving the device performance could be explored.

Chapter 6
Toward Monolithic Integration with Si Photonic Circuits

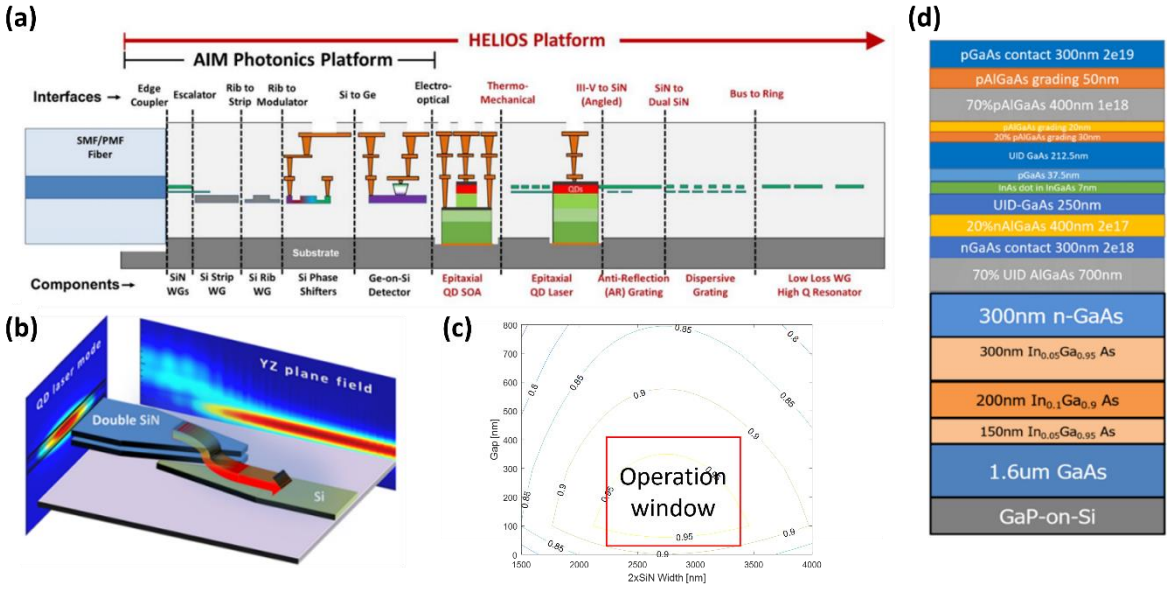

Figure 40: (a) Schematic of the hetero-epitaxial laser integration on Si (HELIOS) platform. (b) Butt-coupling configuration with double SiN core and Si waveguide. (c) The simulated coupling efficiency with respect to the gap between the laser and the nitride cores and the core width. (d) Proposed full epi stack for the in-trench optical gain.

High performance InAs quantum dot lasers grown on planar (001) Si has for the first time entered the realm for commercialization. The demonstration of long lifetime at 80 °C is comforting but not enough. Such devices need to be integrated onto existing Si photonics chips through direct epitaxial growth. However, even for the best laser stack on Si, the QD active region is still about 3.5 μm above the Si substrate which makes it close to impossible to evanescently couple the light to the Si. One

promising approach would be to deposit the material stack onto a pre-patterned template with all other passive components already laid out within the oxide. Pockets for laser deposition would be etched open down to the Si handle wafer to make room for the buffer layer and part of the bottom cladding layer. The vertical alignment of the laser active region to the existing waveguides would be accurate within a few nanometers due to the precise control of the layer thickness in a growth chamber.

The main challenge would be to realize the same material quality in the pockets as on a planar Si surface. Beam flux shadowing from the mask material and the inability to measure the surface temperature and observe the surface quality in-situ would be the major issues to solve. Nevertheless, the potential impact for obtaining such high-performance light source in the pockets on a Si photonic chip is well worth the effort. The resulted integrated platform would not only revolutionize photonic chips for communication, but also other applications that require on-chip gain elements, e.g. LiDAR with optical phased arrays.

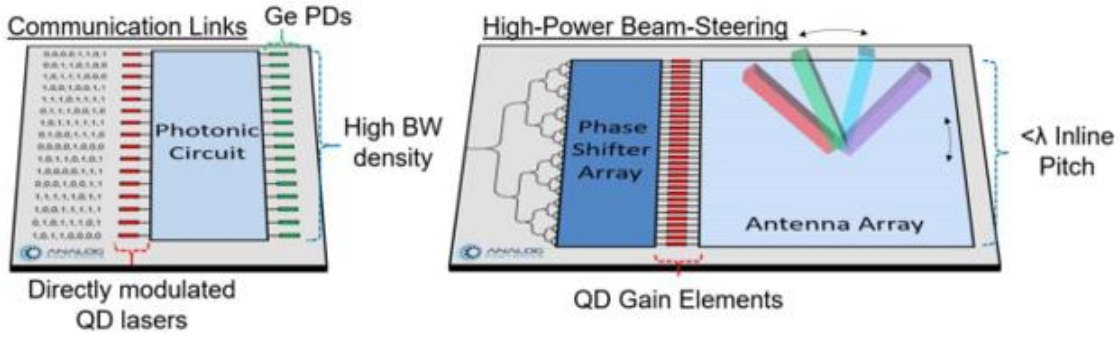

Figure 41: On-chip gain for (a) optical communication and (b) solid state LiDAR system.

6.1 Initial attempts

The first proposed template architecture has large exposed (111) Si surface with (001) flat bottom. The purpose is to eliminate the antiphase domains with the high index planes, similar to the previous V-grooved template with much smaller (111) Si surfaces. A thin layer of Ge was first deposited to help with oxide desorption in our III-V-only chamber. However, such architecture was quickly

abandoned as it was extremely difficult to achieve high quality crystals on both (001) and (111) surface simultaneously, possibly due to the different optimum growth conditions. After depositing a thin 100 nm GaAs, it is observed that the (111) surface is noticeably rougher than the GaAs deposited on (001) surface since the original growth conditions were tuned on a (001) surface. The initial template and the preliminary growth results are summarized in Figure 42. On top of that, the crystal doesn't planarize nicely after filling the trench with GaAs (not shown here).

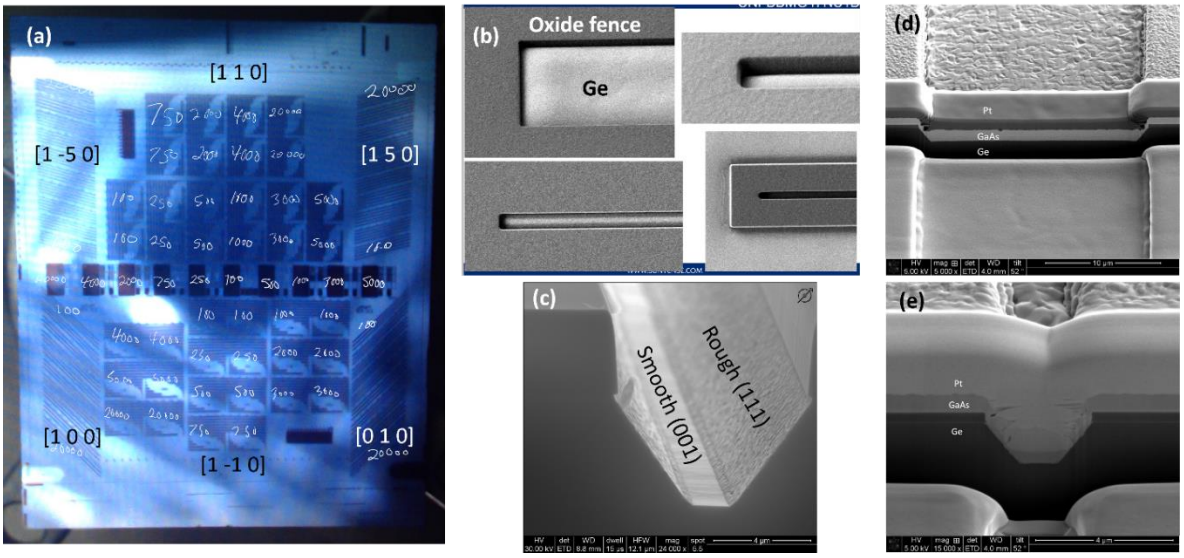

Figure 42: (a) The initial template with oxide fences in different directions and width. (b) Close up SEM images of the oxide fence with Ge deposited on the Si surface. (c) Cross-section SEM image after depositing 100 nm GaAs. (d) and (e) are cross-section SEMs after depositing 1 um GaAs.

Nonetheless, the attempt to achieve selective MBE growth on the oxide patterned wafer was carried out on the initial templates as well. The MBE is inherently not selective under normal growth conditions (580 °C and 1 μm/h growth rate) as the atoms are mass-spread onto the sample surface in a ballistic manner during the growth, and polycrystalline III-V would form on the oxide surface. As shown below in Figure 43, both the oxide mask and the crystal surface would be covered with III-V materials under the conventional growth conditions.

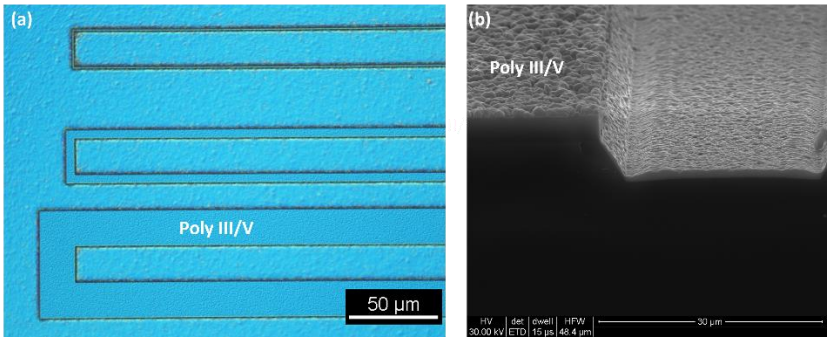

Figure 43: (a) Nomarski top-down image and (b) cross-section SEM image after depositing 1 µm GaAs on the Ge/Si template. Non-selective polycrystalline III-V material is clearly visible.

Yet, the net deposition is a result of the impinging flux minus the desorption flux. The desorption of III-V adatoms on the SiO_2 surface is much higher than on a III-V surface. Thus, it is possible to achieve selective growth if the effective impinging flux could be tuned to be lower than the desorption flux[135]. The proposed technique to achieve selective growth is called punctuated supplied epitaxy (PSE), where the Group III fluxes are turned off periodically, schematically shown in Figure 44. In the absence of the Group III fluxes, the adatoms on the oxide surface would either leave the oxide surface or diffuse into the nearby trenches provided that the surface temperature is sufficiently high. Both the GaAs/AlGaAs and InGaAs could be grown selectively with the PSE technique[135,136]. It can also be expected that if the growth temperature is high and the Group III flux is low, selective growth could be achieved even under continuous deposition.

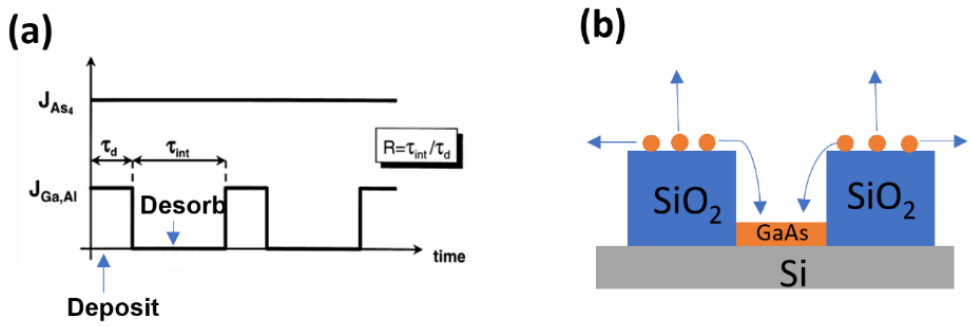

Figure 44: (a) Illustration of the PSE process. Both Group III and Group V fluxes are supplied during the deposition time (τ_d) and only Group V flux is supplied during the desorption time (τ_{int}). The The τ_{int} is normally longer than τ_d. Group V flux is there to protect the crystalline surface inside the trench. (b) Schematic of the adatom actions during the desorption time.

Various growth conditions were experimented, and the degree of selectivity was examined mostly by Nomarski imaging. As shown in Figure 45 below, when the growth temperature is 630 °C and the growth rate is 0.1 μm/h, perfect selectivity can be achieved even with continuous deposition. However, the PSE approach resulted in a more pristine crystal quality. On top of that, similar selectivity and crystal quality as shown in Figure 45f could be achieved at 580 °C with a growth rate up to 0.3 μm/h using PSE whereas the selectivity is lost when the growth rate is increase to 0.12 μm/h at 580 °C for continuous deposition. Unfortunately, the selective MBE growth experimented with here requires a very long growth time (>2 days) to deposit the whole laser stack due to the slow growth rates and the periodic pauses. As such, it is then considered not viable for the later device development. The required temperature for AlGaAs selective area growth would potentially cause severe interdiffusion of the QDs with the surrounding matrix. In order to achieve perfect selectivity with a reasonable growth temperature and growth rate (~1 μm/h), the growth chamber may need to be upgraded with a hydrogen plasma source[137].

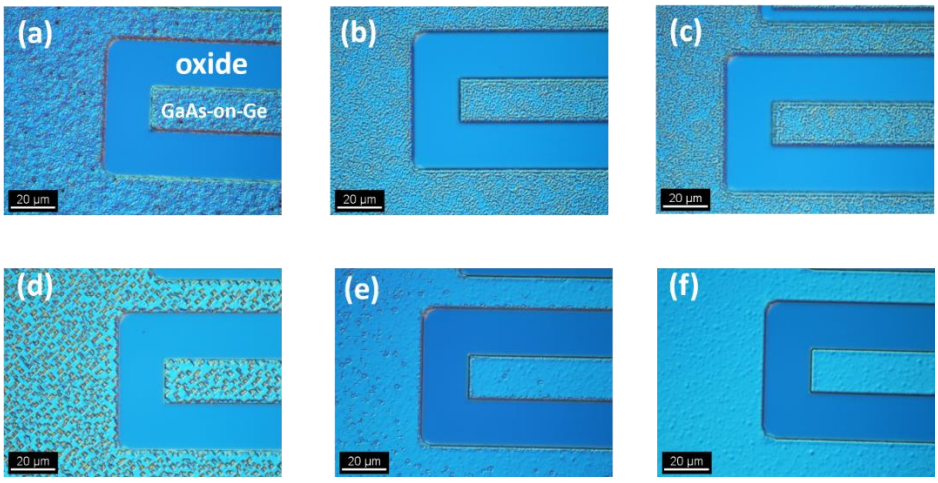

Figure 45: Continuous deposition with 0.1 µm/h and 40 V/III ratio at (a) 630 °C, (b) 600 °C), and (c) 580 °C. PSE deposition at 630 °C with a growth rate of 0.1 µm/h and a V/III ratio of (d) 450, (e) 100, and (f) between 10 and 40. Compared with the previous results, it seems the growth temperature and growth rate control the selectivity and V/III control the crystal quality. PSE relaxes the requirements of growth rates and growth temperature for perfect selectivity.

6.2 Temperature discrepancy

In the test templates shown above, the majority of the sample area is exposed with Ge or III-V. It is then straight forward to measure the surface temperature with pyrometer and monitor the surface quality in-situ with RHEED. However, in the templates for the actual device build, the oxide mask covers most of the surface which makes the pyrometer reading less reliable and completely forbidden the use of RHEED. Since the silicon substrate is normally doped, the sample temperature measurement during growth would still have to rely on pyrometry, which depends not only on the actual sample temperature but also the on emissivity of the surface. It has been observed that for the same sample geometry, the sample with the oxide mask gives a lower temperature reading compared to that measured on planar GaP/Si. Once the oxide mask is covered with polycrystalline III-V due to the non-selective growth, the temperature reading is higher than that measured on planar GaP/Si. The pyrometer temperature profiles obtained from three different surfaces are shown below in Figure 46.

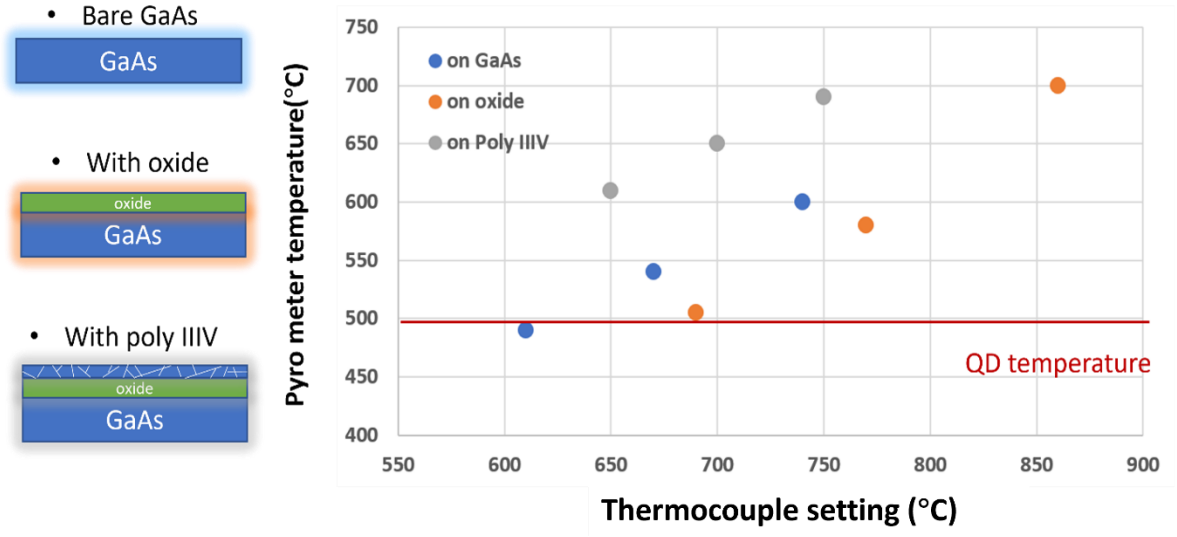

Figure 46: Pyrometer temperature profiles with respect to the heater thermocouple setting measured on GaAs substrate, on oxide patterned Si wafer, and on polycrystalline III-V deposited on the oxide mask. The red horizontal line the QD growth temperature on GaAs. Thus, if the temperature calibration is done on the oxide, the actual III-V temperature would be well above 550 °C, which would evaporate the QDs.

The consequence is that if the temperature profile calibrated on the oxide surface is used, the growth temperature of the QDs would be underestimated from the pyro reading. Since the optimum QD growth temperature (~495 °C) is very close to the temperature (~505 °C) above which the QDs would be evaporated from the surface, the temperature underestimation may evaporate all the QDs. On the other hand, the temperature would be severely overestimated if trusting the pyro reading during the QD growth after the oxide mask is covered with polycrystalline cladding materials. Thus, the most accurate way to calibrate the sample temperature would be to record the heater power required for the bare GaP/Si profile. In the next section, it will be shown that a high crystalline quality could be achieved in the pockets when trusting the heater power, yet QD contrast was not observed in the active region. This could be because the oxide mask has a much lower heat conductivity than the III-V material in the pockets. Thus, even though the sample was heated to the same temperature as if it were just a bare GaP/Si piece with the same geometry, more heat would be channeled through the III-

V pocket. This inherent temperature uncertainty on the in-pocket III-V surface from the sample architecture may need arbitrary heater power tuning until the existence of the QDs is observed.

6.3 High crystalline quality

In order to obtain high quality III-V crystals inside the trenches, multiple trench architectures have been investigated, as shown below. As mentioned previously, the trenches with large exposed (111) Si surfaces have been ruled out, with or without a Ge layer. Any structure with bare Si surface is not suitable for the III-V MBE chamber and a recess into the Si substrate is required to make room for the buffer layer. Thus, Trench 5C, flat-bottom Si with selective GaP is the most promising starting point for the MBE in-trench growth. Figure 47a shows summary of all trench types tested.

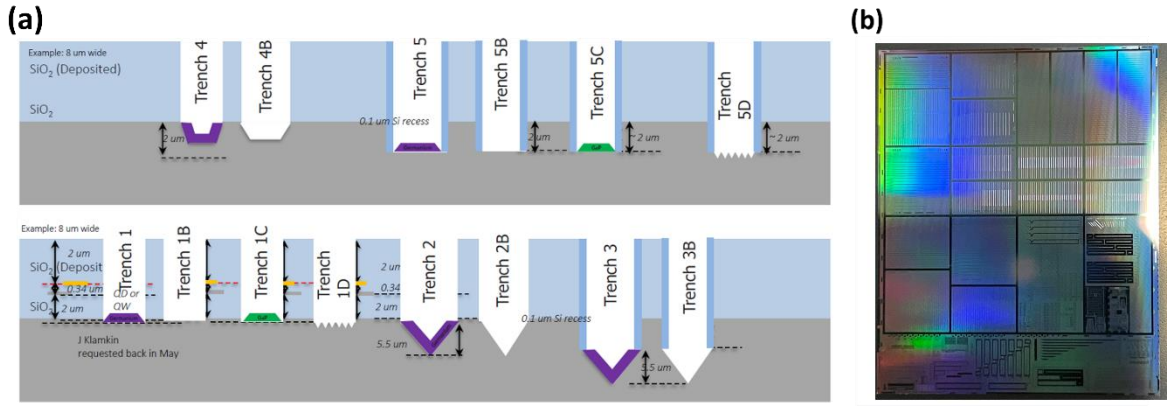

Figure 47: (a) All the proposed trench architectures. The top is for the test growths and the bottom is for the full device build. (b) An example coupon with trenches in both horizontal and vertical directions with different widths and lengths.

The initial 1.6 μm GaAs was deposited in a Trench 5C structure with the same growth conditions as was done on a blanket GaP/Si wafer. All growth temperatures were calibrated with respect to the heater power. The cross-section SEMs of the as-grown material are shown below. The defect densities were measured via PVTEM as the trenches are too small to establish long range periodicity for ECCI.

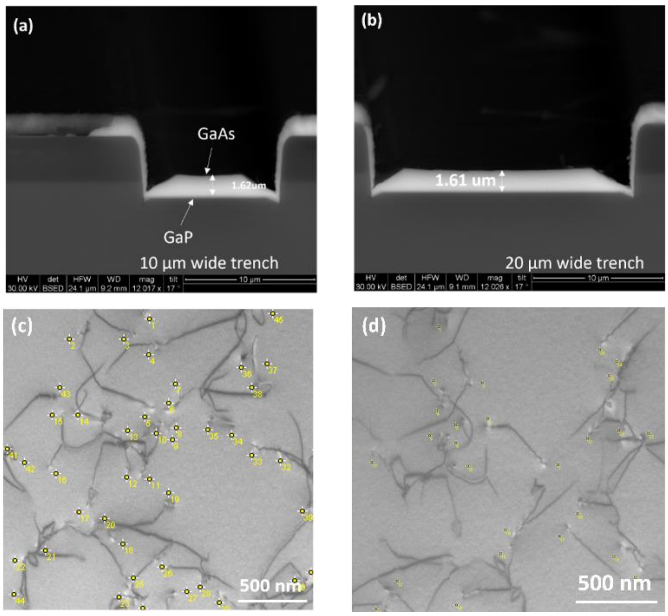

Figure 48: (a) and (b) are cross-section SEM images for the as-grown GaAs film. The thin GaP layer is clearly visible, and the GaAs film thickness is as designed across all trenches regardless of the width. (c) and (d) are PVTEM images taken 800 nm below the surface and on top of the surface, respectively.

It can be seen from Figure 48a,b that the 1.6 µm of GaAs has been successfully deposited on the thin GaP layer inside the trench and the thicknesses are as-designed, regardless of the trench width (10 µm and above, noticeable beam shadowing for narrower trenches). This suggests that the in-trench growth rates are the same as on blanket substrates. The measured TDD via PVTEM is about 5×10^{8} cm^{-2} on the surface of the GaAs layer and 2×10^{9} cm^{-2} at 800 nm below the surface. These TDD values are the same as those measured on a blanket sample. It has been observed that surface morphology of the as-grown GaAs shows a discrepancy between horizontal and vertical trenches and such differences are amplified after the TCA process, as shown below in Figure 49. This discrepancy has been expected from the beginning of the project as the surface diffusion is asymmetric in the III-V materials, being considerably faster in the [1 -1 0] direction. Thus, when the trench is favorably aligned with the crystal strips, the surface morphology is better than the ones in the orthogonal direction. An in-depth investigation is required to fully understand this discrepancy.

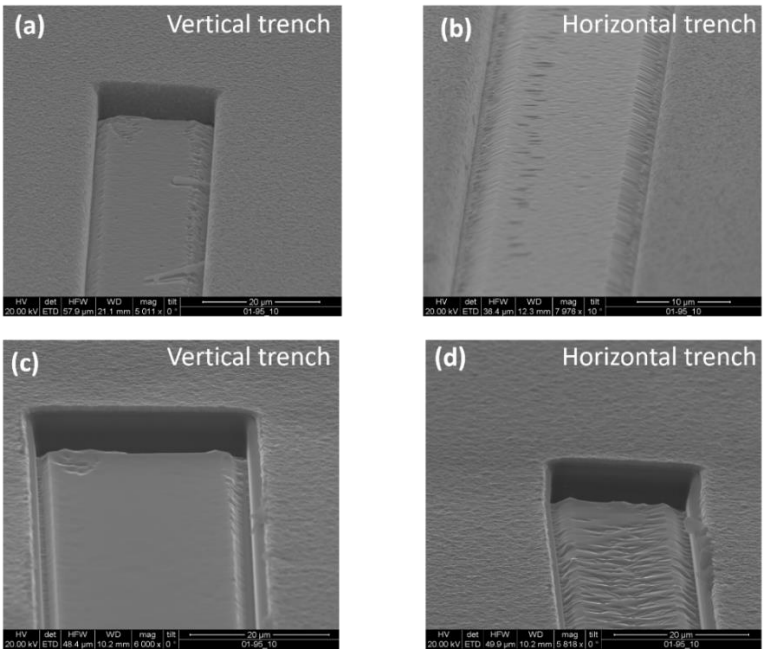

Figure 49: (a) and (b) are the top-down SEM of the as-grown initial 1.6 µm GaAs. The surface morphology in the horizontal trench is slightly rougher. (c) and (d) are the post-TCA surface morphology of the same sample. The surface of the GaAs within the horizontal trench is significantly rougher than the one in the vertical trench.

Beside the roughened surface after TCA, another interesting observation was made on the post-TCA GaAs strips, as shown in Figure 50 below. Before the TCA process, the GaAs film thickness was 1.6 µm and was reduced to approximately 960 nm after TCA, which suggests that Ga and As atoms were evaporated during the TCA process. This III-V evaporation phenomena was not observed when performing the TCA process on the GaAs grown on blanket GaP/Si template. A proposed explanation is as follows. During the TCA process, the surface atoms would diffuse laterally to find the most energetically favorable sites to bond[93]. Different from the case on a blanket substrate where atoms would just diffuse randomly, the atoms would now prefer to gather around the top corners of the in-trench strips. This is possibly due to the inter-surface diffusion and required strain relaxation that are thermally activated [138,139]. As more atoms accumulate around the corners and the "horn-shaped" tips are developed, the vapor pressure might have increased to a point where the arsenic overpressure is

overcome and III-V sublimation is then initiated. Of course, a lot more experiments and in-depth material characterizations are needed to verify the above hypothesis. Nevertheless, this observation suggests that the TCA process, which is very effective is reducing TDD, must be removed for the in-trench growths.

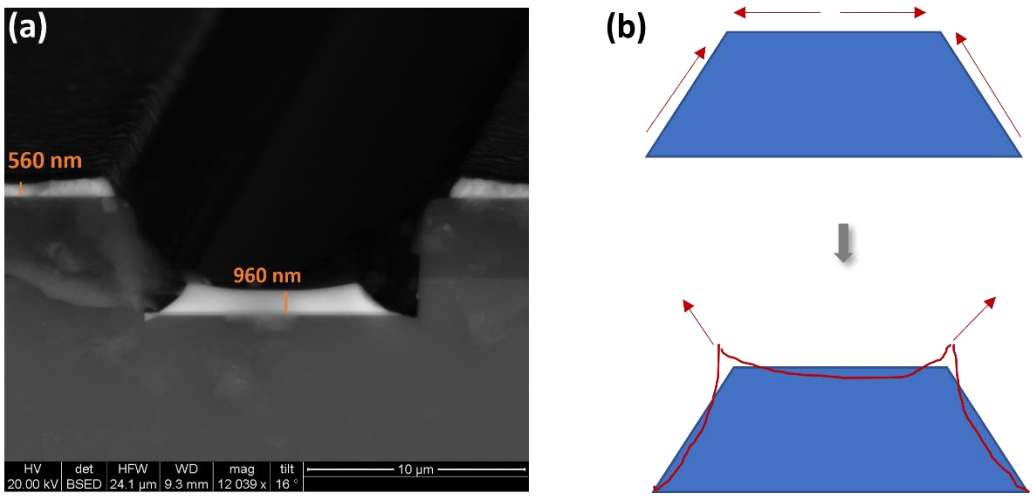

Figure 50: (a) Cross-section SEM if the post-TCA in-trench GaAs film. Though the polycrystalline material on the oxide wall has been removed, the in-trench material has been partially removed as well. (b) Schematic illustration of the hypothesis of how the III-V is evaporated.

An attempt to deposit the full stack (buffer + laser epi) was carried out after calibrating the sample temperature with respect to the heater power and the TCA process was not used. A cross-sectional TEM image of the in-trench full stack is shown below. The crystal quality is the same as if it were grown on a blanket GaP/Si wafer with no observed APDs and all layer thicknesses are the same as designed, shown in Figure 51a. The InGaAs dislocation filters and the active region contrast are clearly visible. As mentioned above, the underestimation of the sample temperature is considered as the major challenge in growing high quality QD laser stacks in the trenches. In order to gauge the severity of the underestimation, an EDS scan was performed across the InGaAs graded filter layers. The extracted indium composition profile is shown in Figure 51c, and the values are the same as the

intended compositions. This suggests that the actual surface temperature when growing the InGaAs filters was not higher than 540 °C, when the heater power was set for 495 °C. It has previously been observed that the InGaAs composition could not be maintained above 540 °C. With. these as-designed InGaAs graded filter layers, the TDD was reduced from 5×10^{8} cm^{-2} on top of the bottom GaAs layer to $1\sim2\times10^{7}$ cm^{-2} after the buffer layer structure, suggesting a dislocation filter efficiency of approximately 97%.

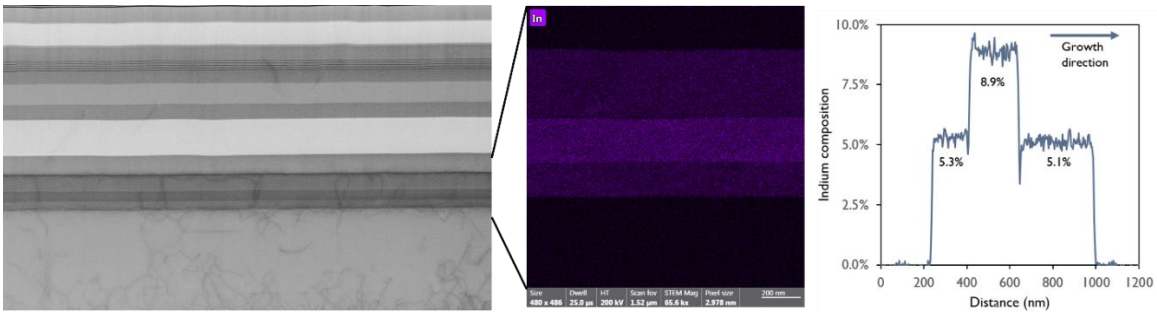

Figure 51: (a) Cross-sectional TEM of the in-trench full stack. (b) The raw EDS data scanned across the InGaAs graded filter layers. (c) The extracted indium composition profile.

A zoomed in view around the active region is shown in Figure 52. Though the contrast from the InGaAs QW is clearly visible, no QD contrast was observed. This suggests that the actual surface temperature when growing the QDs was at least higher than 510 °C for the In adatoms to have zero sticking coefficient when the heater power was set for 495 °C. This maximum surface temperature for QD nucleation was determined from a growth temperature series done on GaAs native substrates, which will be briefly discussed later in Figure 57 in Chapter 7. Combined with the argument above, the actual surface temperature is underestimated by approximately 15 °C to 45 °C. This discrepancy is because the indium adatom sticking coefficient has a higher temperature tolerance when other Group III elements are present during growth (Ga or Al). Thus, the heater power would then need to be arbitrarily tuned down slowly until high quality QDs are obtained in the in-trench laser stack.

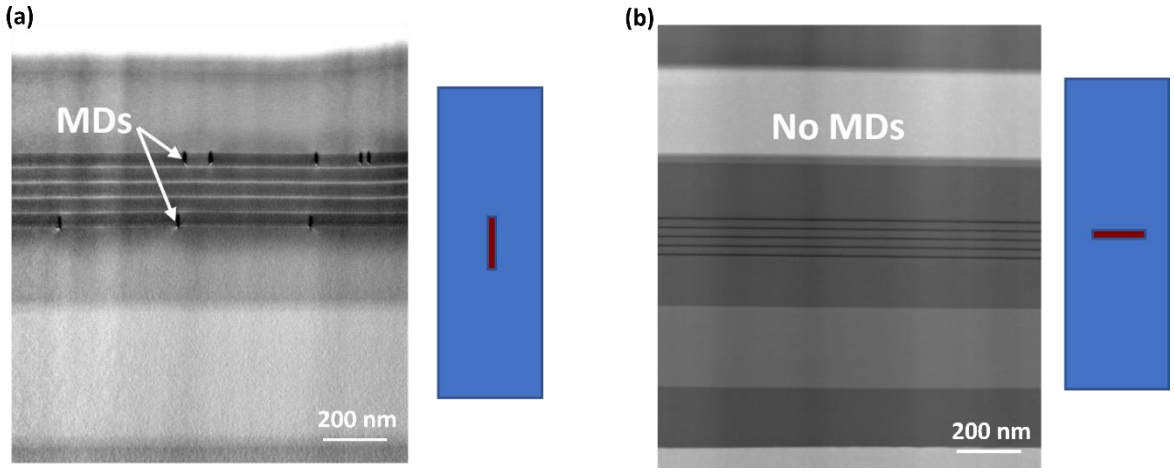

Figure 52: Zoomed in XTEM around the active region for (a) foil normal perpendicular to the trench long edge and (b) foil normal parallel to the trench long edge.

The zoomed in view shown in Figure 52a was obtained from a TEM foil with its surface normal perpendicular to the trench direction. MDs near the top and bottom of the active region are clearly visible, formed during the post-growth cooling process. Yet, on the same sample, no MDs were observed on a TEM foil with its surface normal aligned with the trench direction, and this suggests that the tensile stress is much less across the short edge of the trench, shown in Figure 52b. As stated at the end of Chapter 4, this stress asymmetry is expected for these narrow strips of III-V grown in the trenches. According to the book by Prof. Matthew Begley[129], the edges of strips are stress-free, and the stress level would reach that obtained on a blanket film about 2 to 4 times the film thickness toward the center of the strips. Since the film thickness is around 5.5 μm and the trench lengths are a few thousands of microns, the stress state along the trench has reached the blanket film level. Thus, MDs would form in response to the tensile relaxation during cooling (Chapter 4). In the direction across the trench, since the trenches are 15 to 20 μm wide, the tensile stress is expected to be less than on a blanket film. Consequently, no MDs were observed in the foil with its surface normal aligned with the trench direction. Since the post-cooling MDs near the active region are distributed

asymmetrically in the blanket materials, shown elsewhere[122], aligning the trench to the direction with denser MDs (measured on the blanket film) would potentially minimize the number of MDs.

6.4 Summary

Reproducing the high quality QD laser materials in the pre-patterned pockets on Si photonic chips with butt-coupling configuration is currently the most promising approach to achieve true monolithic integration of III-V light source. Due to the lack of in-situ monitors, growing blindly in the pockets is not a trivial task. After trying out on multiple template architectures and carefully tuning the growth conditions, blanket-substrate-level crystal quality has been achieved with GaP-seasoned pockets. Yet, possibly due to the inherent hotter temperature inside the pockets, QD contrast has not been observed despite the accurate indium composition in the filter layers. Arbitrarily tuning the heater power to locate the condition for QD nucleation is needed. Fortunately, the pocket geometry offers another way of reducing the MD density by aligning the [1 1 0] crystal orientation with the pocket long edge. It is then expected that the in-pocket lasers could perform better than those grown on blanket templates if the same QD quality could be achieved.

Chapter 7
Extending QD technology to other wavelengths

The emission wavelength of the InAs QDs is highly tunable, primarily depending on the amount of InAs deposited, surrounding materials, the lattice mismatch with the substrate, and even how the InAs QDs are buried. Though the main focus of my research has been focusing on the 1300 nm lasers for datacom applications, QD lasers emitting around 1550 nm on InP substrate for telecom applications and 1178 nm on GaAs as the pump source for Na atom clock have also been investigated. In this chapter, the growth optimization and device demonstration of lasers emitting at those wavelengths will be briefly discussed.

7.1 1178 nm QD laser on GaAs

7.1.1 Growth development

In order to develop a InAs QD source that is not documented in literature, it is only logical to start with known growth conditions for depositing InAs QDs on GaAs native substrate. Thus, the starting growth conditions were chosen to be 490 °C for the growth temperature, 0.113 ML/s for the growth rate, and 35 for the V/III ratio. Since it is always easier to redshift the emission wavelength by depositing more InAs or embed the QDs within InGaAs QWs, the first step to develop a 1178 nm source is to determine the minimum wavelength obtainable under the above-mentioned growth conditions with no InGaAs QWs. The comparisons between the 1300 nm QD and the attempted 1178 nm QD PL sample structures, room temperature PL spectra, and the amount of InAs deposited before the on-set of nucleation are shown in Figure 53 below.

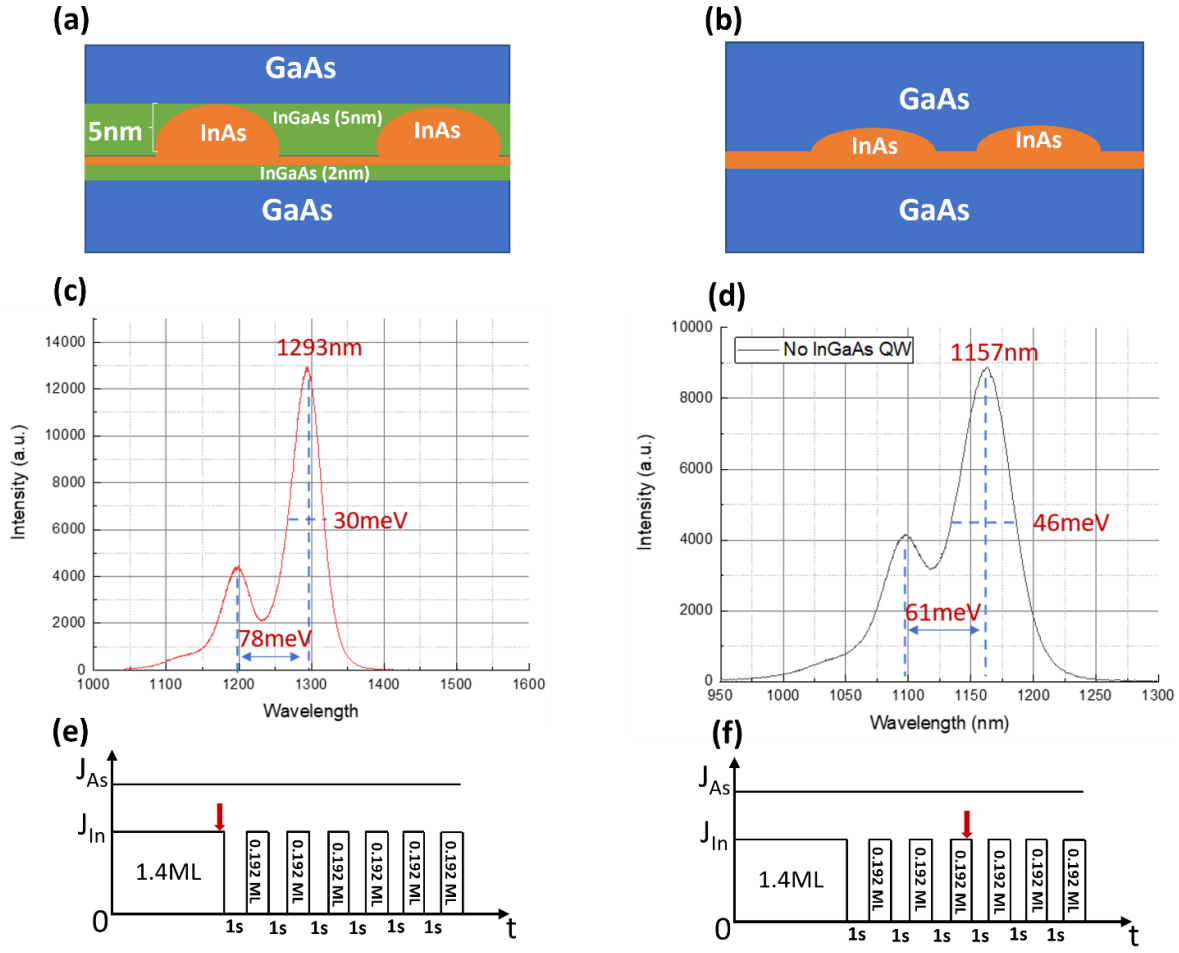

Figure 53: (a) and (b) are the PL sample structures for the 1300 nm QD and 1178 nm QD, respectively. (c) and (d) are the room temperature PL spectra for the corresponding sample structures. (e) and (f) illustrate the deposition profile of InAs. The red arrows point to when the on-set of nucleation was observed in RHEED for the corresponding structure.

For the QDs emitting around 1300 nm, the InAs was deposited on a 2 nm $In_{0.15}Ga_{0.85}As$ layer and capped with a 5 nm $In_{0.15}Ga_{0.85}As$ layer while the attempted 1178 nm QDs were deposited on a GaAs surface and capped with GaAs, shown in Figure 53a and b, respectively. The PL spectrum of the well-optimized 1300 nm QDs shows a FWHM of 30 meV, and the energy separation between the ground state and the first excited state is 78 meV. Though the PL spectrum for the first-attempt 1178 nm QDs shows a wider FWHM and narrower energy separation, the intensity is acceptable considering that

the detector used has a lower responsivity around 1157 nm than around 1300 nm. The ~20 nm bluer emission wavelength is less of an issue since, as mentioned above, it is always easier to redshift the wavelength. Here, it is found that how the QDs are buried also strongly affects the emission wavelength. It is worth mentioning that for the structures shown in Figure 53a and b, the capping layers, either the InGaAs cap for 1300 nm QDs or the GaAs cap for the attempted 1178 nm QDs, were not deposited continuously. 3 nm of the capping layers were first deposited, followed by a 10 s pause, and then another 2 nm of the capping layers. Another 10 s pause was then introduced before finishing up the PL structure with a thick GaAs layer. This is referred to as "split capping." The two different capping sequence is roughly illustrated below. Together with two different growth rates for the GaAs capping layer, four different capping scenarios were experimentally tested. The results are summarized in Table 5.

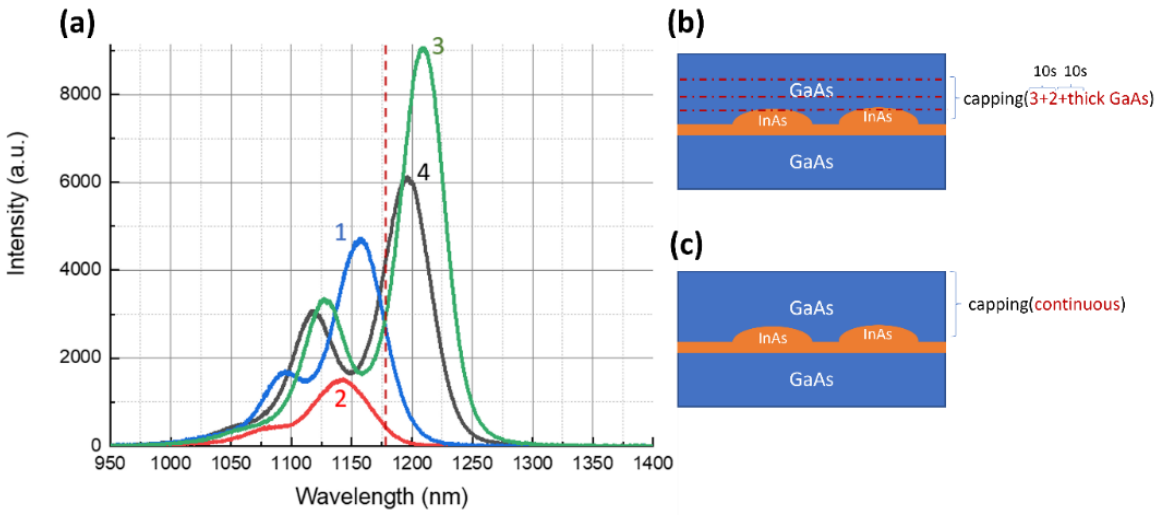

Figure 54: (a) The room temperature PL spectra of the four different scenarios. The number labels correspond to the Sample No. in Table 2. The red vertical dotted line denotes the target 1178nm wavelength. (b) and (c) are the schematic illustrations of the split and the continuous capping sequence, respectively.

Table 5: Four test conditions on the GaAs capping layers and the resulted PL qualities are summarized.

Sample No.	Capping sequence	Capping rate	WL (nm)	FWHM (meV)	Separation (meV)
1	Split	1 μm/h	1157	42	63
2	Split	1.8 Å/s	1142	48	61
3	Continuous	1 μm/h	1203	32	75
4	Continuous	1.8 Å/s	1195	40	71

It has been observed that a continuous capping layer would significantly redshift the emission wavelength by approximately 50 nm and improve both the FWHM and the energy separation. A higher capping rate could also provide an ~10 nm redshift in wavelength and marginal improvements in FHMW while slightly degrading the energy separation, which is tolerable. However, as shown in Figure 54a, the redshifts obtained by growing the capping layer continuously overshot the target wavelength. Then it was expected that if the capping layer was grown not completely continuously but with shorter pause time (less than 10s), the wavelength could be fined tuned between the two end points. Before doing so, the deposition sequence for nucleating InAs QDs on GaAs would need to be adjusted. As shown in Figure 53e and f, the 1.4 ML of InAs was deposited first followed by six 0.192 ML bursts separated by a 1s pause. Since this deposition sequence was optimized for 1300 nm QDs, when it was executed on the $In_{0.15}Ga_{0.85}As$ pre-layer, the nucleation happened at 1.3 to 1.4 ML as intended. The nucleation was delayed to the third burst when the deposition sequence was executed on bare GaAs surface for the 1178nm QDs. This was expected due to the lack of the initial compressive strain from the $In_{0.15}Ga_{0.85}As$ pre-layer. It is known that the QD quality would be better if the continuous deposition of the InAs material is maintained until nucleation is observed. Thus, since nucleation happened after the third burst, which was about 2 ML InAs, the continuous deposition was extend to 2 ML before switching to the 0.192 ML bursts.

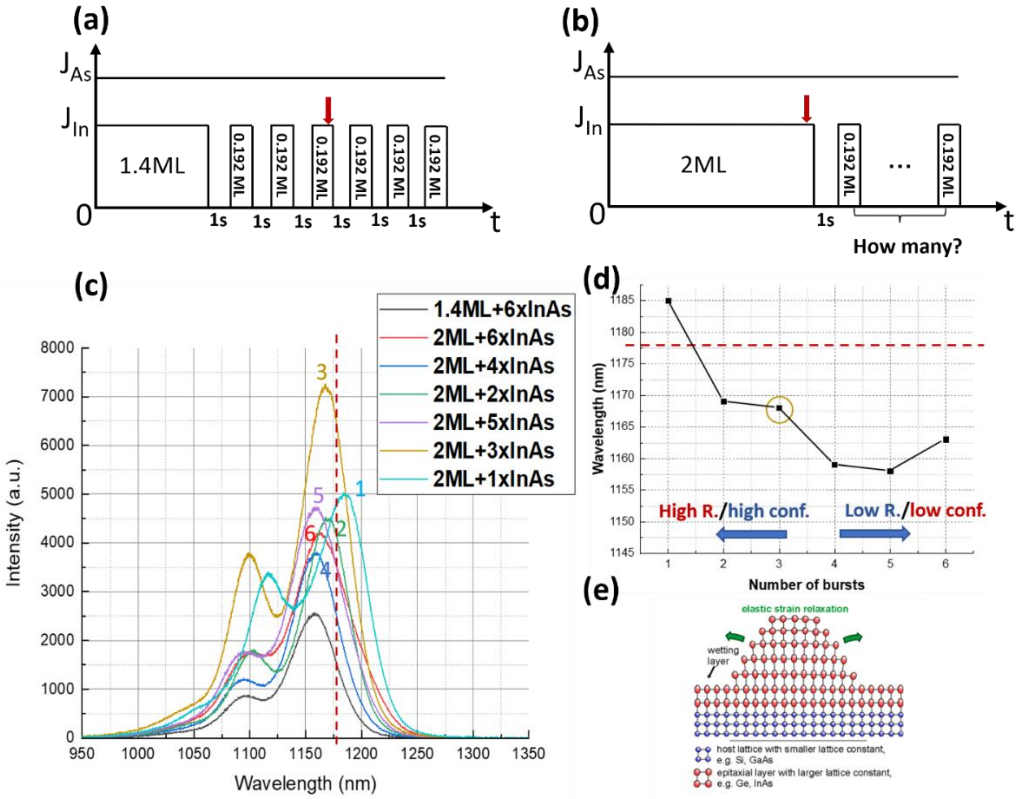

Figure 55: (a) and (b) are the initial and the proposed deposition sequences of the InAs QDs on bare GaAs surface, respectively. (c) Room temperature PL spectra of samples with different number of post-nucleation bursts. The black curve is the reference sample with the original deposition sequence. The numbers on the curves indicate the number of bursts used. The vertical red dotted line is the target wavelength. (d) Extracted emission wavelengths with different number of bursts. The horizontal dotted line indicates the target wavelength. (e) Schematic of the dot with elastic strain relaxation.

As shown in Figure 55a and b, where the red arrows indicate the observed on-set of nucleation, the nucleation on bare GaAs happened after continuously depositing 2 ML of InAs. Then the question was how many 0.192 ML bursts should be included. As shown in the PL spectrum in Figure 55c, the best PL intensity was achieved with three bursts after the on-set of nucleation at 2 ML, which was about 2.57 ML in total, the same as having six bursts after 1.4 ML. It was also observed that, regardless of the number of post-nucleation bursts, continuously depositing the InAs material until the on-set of nucleation resulted in better dot quality as was expected. Figure 55d shows the extracted

emission wavelengths with respect to the number of post-nucleation bursts. Counter intuitively, a blueshift was observed with more InAs deposited up to five bursts. Normally, a redshift is expected when depositing more InAs material for the bigger dots and less confinement. This abnormality could be attributed to a reduced degree of elastic relaxation, as schematically shown in Figure 55e. The strain of the dots could be partially relaxed through their elastic expansion and this process is expected to be less effective when a higher percentage of the atoms within the QDs are buried. A more in-depth study on the microscopic structure of the QDs is required to confirm this hypothesis.

The above experiments suggested that the "2 ML+3 bursts" deposition sequence should be utilized for growing InAs QDs on bare GaAs. The emission wavelength of this structure was about 1167 nm. It is worth mentioning that the GaAs capping layer was deposited in a split manner with 10 s pauses in between. As mentioned above, the wavelength could be fine-tuned by adjusting the pause duration during the capping layer growth. After reducing the pause duration from 10 s to 8 s, the emission wavelength was tuned to exactly 1178 nm, as shown below in Figure 56.

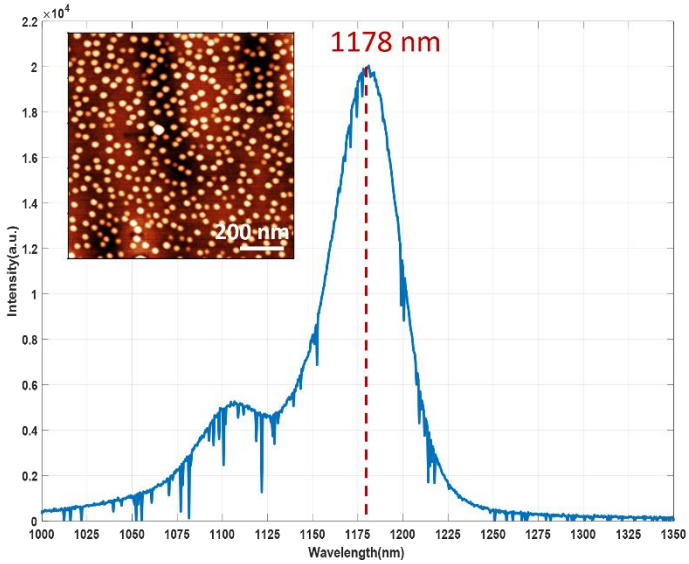

Figure 56: Room temperature PL of the 1178 nm InAs QDs. The inset shows the AFM image of the QDs. The surface QD density is about 3×10^{10} cm^{-2}.

The active region structure to obtain the 1178 nm QD emission has then been achieved under the given QD growth conditions: 490 °C growth temperature, 0.113 ML/s growth rate, and 35 V/III ratio. Below are the PL spectra of a growth temperature series.

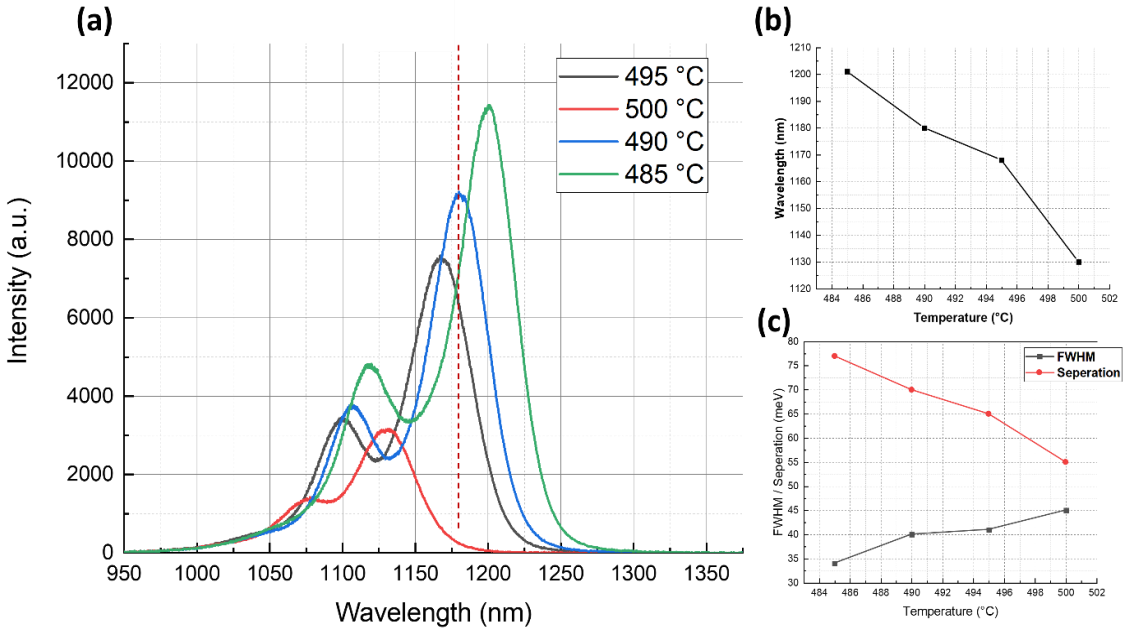

Figure 57: (a) PL spectra of the growth temperature series. The vertical red dotted line is the target wavelength. (b) Extracted emission wavelength vs. growth temperature. (c) Extracted FWHM and energy separation vs. growth temperature.

As shown in Figure 57, both the emission wavelength and the PL intensity have a very strong monotonic dependence on the growth temperature. Similar trend was observed in the FWHM and the energy separation in Figure 57c and lower growth temperature is favorable. Thus, the 1178 nm emission wavelength obtained at 490 °C is a "local optimum." The convolution between the growth conditions and the deposition sequence/sample structure would need to be thoroughly investigated to locate the "absolute optimum." The strong monotonic dependence of the wavelength on the growth temperature has not been observed for the 1300 nm QDs, possibly due to the dependence of the InGaAs quality on the growth temperature. Thus, the 1178 nm QD temperature series could also be

used to confirm the accuracy of the temperature calibration for each growth campaign since the "oxide desorb" method has an inherent 5 °C uncertainty.

7.1.2 Device demonstration

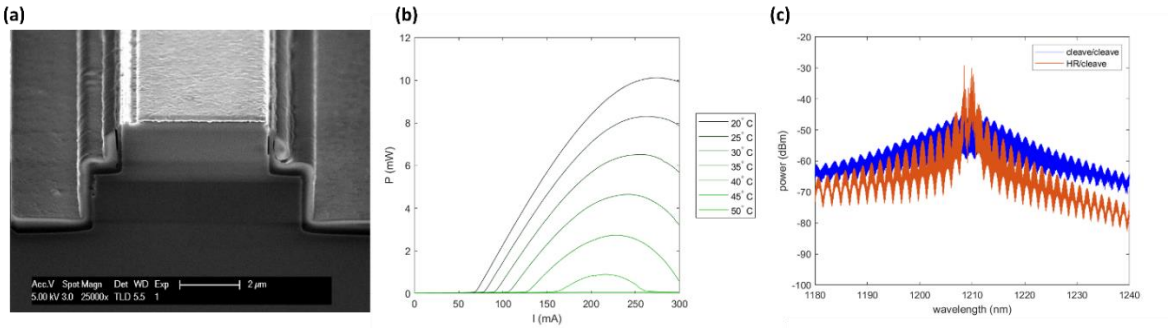

Figure 58: (a) Cross-section SEM of the as-cleaved FP lasers with a shallow etch ridge. (b) Temperature dependent LI curves. CW operation is maintained to 45 °C. (c) Room temperature spectrum of the cleave/cleave and the HR/cleave devices.

A full laser stack with 5 layers of 1178 nm QDs as the active region was grown on native n-GaAs substrate. The QD layers were separated by 40 nm GaAs spacer layers to prohibit strain coupling between the dot layers. The material was then fabricated into FP narrow ridge lasers, as shown in Figure 58a. Possibly due to the lower dot density, the lasers shorter than 2000 μm did not lase with as-cleaved facets. After applying HR coating on one facet of the cleaved laser bars, lasers no shorter than 1500 μm showed lasing characteristics and the previously lasing devices experienced reduced threshold currents. A set of representative CW LI curves were shown in Figure 58b, measured on a 2×1750 μm^2 device. CW operation was maintained up to 45 °C stage temperature. The high threshold current, low output power, and low maximum operating temperature could also be due to the low dot density. Even though a higher dot density might be possible with finer tuning of the growth conditions, it is less likely to reach that of the 1300 nm QDs as less InAs was deposited after nucleation. However, without the InGaAs QWs, the 1178 nm QDs layers could be stacked to an arbitrary number of layers without worrying about relaxation. Figure 58c shows the room temperature spectrum of a 3×1750

μm^2 device. The HR/cleave facet configuration showed lasing characteristics, but the center wavelength was around 1209 nm instead of the target 1178 nm. A possible cause was a slight colder growth temperature. As previously suggested in Figure 57a, only 5 °C colder than the target growth temperature could result in a 30 nm redshift in the emission wavelength. Considering that the PL optimizations were done on quarters of 2-inch GaAs wafers while the laser was grown on a full 3-inch *n*-GaAs, such small temperature variation could be expected depending on the spot size of the pyrometer. In order to hit the target wavelength, a split of QD growth temperatures might be required. Below, Figure 59 shows the grating structures patterned with e-beam lithography for the re-grown DFB lasers emitting around 1178 nm. The gratings were patterned and etched after depositing the active region and before growing the top cladding layers. The regrowth and the consecutive fabrication processes are currently still on-going.

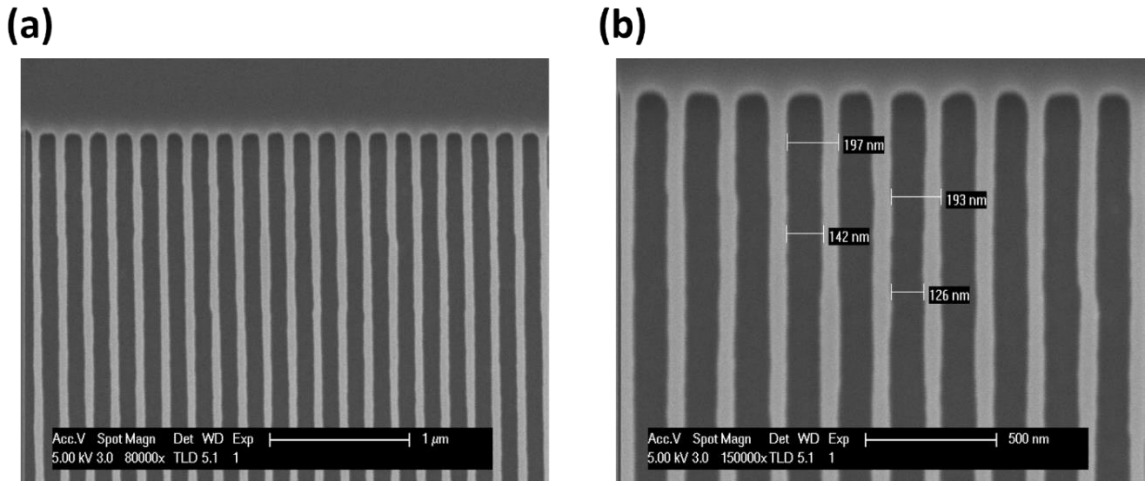

Figure 59: (a) and (b) are the SEM images of the etched gratings for the DFB laser emitting at 1178 nm.

7.2 1550 nm Qdash laser on InP

7.2.1 Growth

Though it is possible to reach 1550 nm emission wavelength with InAs QDs embedded in $In_{0.35}Ga_{0.65}As$ QWs grown on GaAs, the highly strained $In_{0.35}Ga_{0.65}As$ QWs limit the number of active layers one can stack before the QWs relax. This puts a hard limit on the gain given a fixed property

of each individual dot layer. Such limitations could be overcome by growing the InAs nanoparticles on an InP substrate. A lower lattice mismatch would inherently redshift the emission wavelength and the use of lattice matched $In_{0.532}Ga_{0.468}As$ and $In_{0.523}Al_{0.477}As$ materials to construct the laser structure introduces no strain. It was determined from a series of PL sample growths that the optimum growth conditions for nucleating InAs nanoparticles on InP lattice constant were 485 °C for the growth temperature, 0.4 ML/s for the growth rate, 18 for the V/III ratio, and 3.25 ML for the total amount of InAs deposite. The PL structure and a typical AFM scan on the surface particles are shown below in Figure 60.

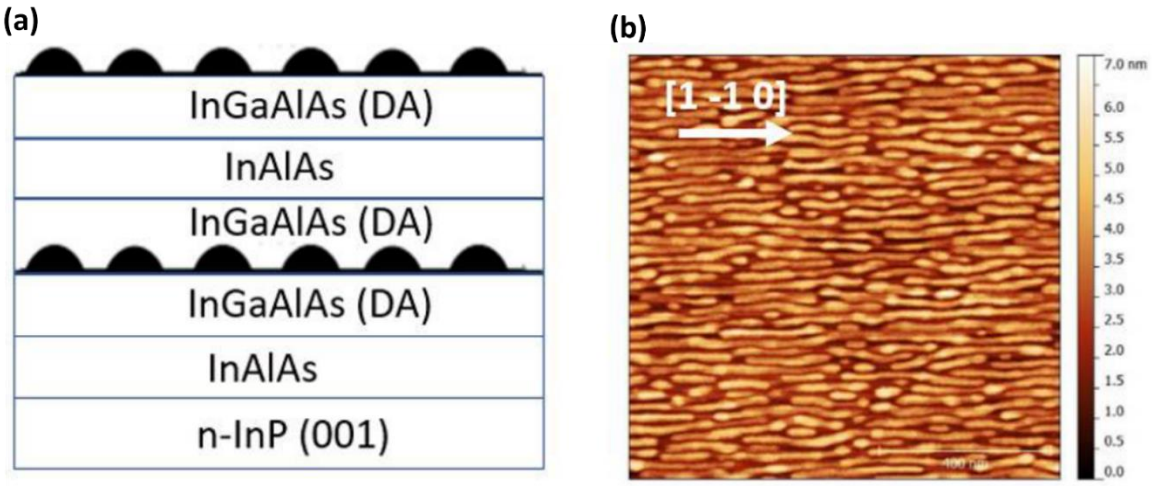

Figure 60: (a) PL structure used to optimize the growth conditions for 1550 nm InAs Qdashes. DA stands for "digital alloy". The structure is finished with uncapped Qdashes for morphology study. (b) A typical AFM scan showing the Qdash morphology.

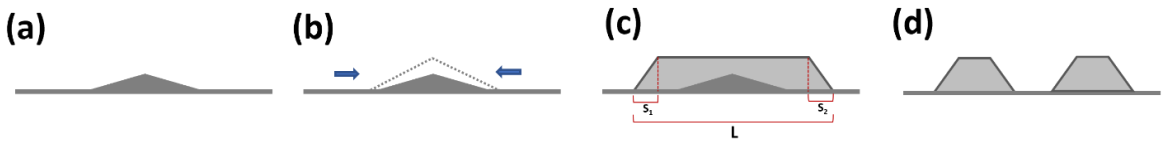

Figure 61: Qdash formation process. (a) the initial nucleation center with shallow facets and close-to-square base; (b) attachment of the adatoms to the existing nucleation sites from both the [1 1 0] and [1 -1 0] directions; (c) islands elongated

along the [1 -1 0] direction formed due to a higher surface diffusion; (d) shorter and rounder islands form during the post growth annealing process in reaction to the high residual strain in the elongated dashes.

Due to the lower lattice mismatch and asymmetric adatom surface diffusion, the InAs nanoparticles nucleated on InP lattice constant showed elongated based along the [1 -1 0], commonly referred to as Qdashes. The proposed Qdash formation mechanism is schematically shown in Figure 61. The initial nucleation center was a square-based pyramid with low angle facets, typically the {1 1 5} facets. The indium atoms deposited afterwards would tend to diffuse toward the existing nucleation centers, known as the heterogeneous nucleation process. The surface diffusivity of the indium adatoms is much larger along the surface reconstruction dimer row direction, namely the [1 -1 0] direction[140], resulting in the elongated dashes in the [1 -1 0] direction. Yet, the as-grown Qdashes are expected to be less stable as they are still highly strained. The percentage of the strain relaxed is proportional to the ratio of $\frac{S_1+S_2}{L}$[141]. The variables are defined graphically in Figure 61c. Compared to the dome-like 1300 nm QDs, the Qdashes would have much smaller $\frac{S_1+S_2}{L}$ value. However, due to the lower lattice mismatch, the InAs Qdashes could be sustained on InP during growth while the InAs grown on GaAs would "snap" into dots during growth for the much higher lattice mismatch. The high residual strain within the as-deposited Qdashes would cause the dashes to evolve. As schematically shown in Figure 61d, the Qdashes are expected to "break" into shorter islands when left uncapped at the growth temperature. Experimental evidence is shown in Figure 62.

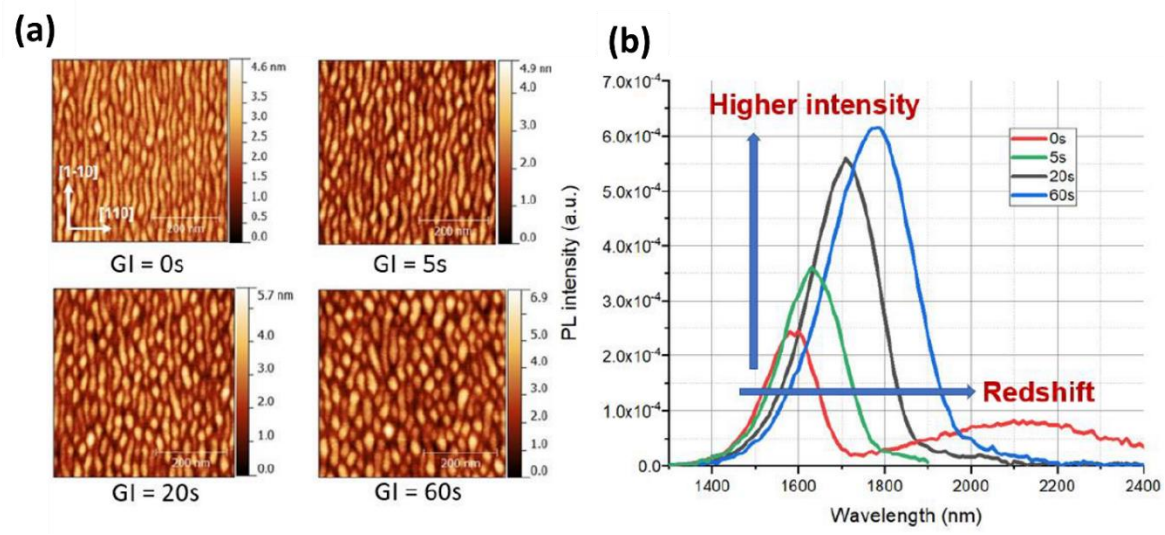

Figure 62: (a) AFM scans of the uncapped surface Qdashes with different GI time[142]. (b) Room temperature PL of the corresponding GI time.

Figure 62a shows the Qdash morphology evolution as a function of the growth interruption (GI) time after depositing the InAs Qdashes. As the GI time was increased from 0 s to 60 s, the Qdash morphology become more "dot-like", and the height of the nanoparticles was increased as well. Consequently, the emission wavelength experienced a significant redshift and higher intensity. The increase in intensity was achieved at the expense of larger FWHM as the "breaking into dot" process is somewhat random. The above GI experiment was done with 3.75 ML total InAs. The total amount of InAs was reduced to 3.25 ML in the laser to make room for the redshift during growth interruption.

7.2.2 Device demonstration

Since the Qdashes are obviously elongated along the [1 -1 0] direction, the FP lasers fabricated from this material are expected to perform differently when the ridge is parallel or perpendicular to the dash elongated direction. Thus, FP lasers with ridges in both directions were fabricated for comparison. As shown below in Figure 63, the lasers showed obvious lower threshold currents, higher maximum output power, and later rollover when the ridge is perpendicular to the dash elongated direction. Since these dashes are 100 to 200 nm long and about 20 nm wide, they can be considered

as 1D nanowires. The performance difference could then be attributed to the stronger interaction between the electric field and the dipole within the dashes, and thus a higher material gain, when the ridge is perpendicular to the dash elongation direction.

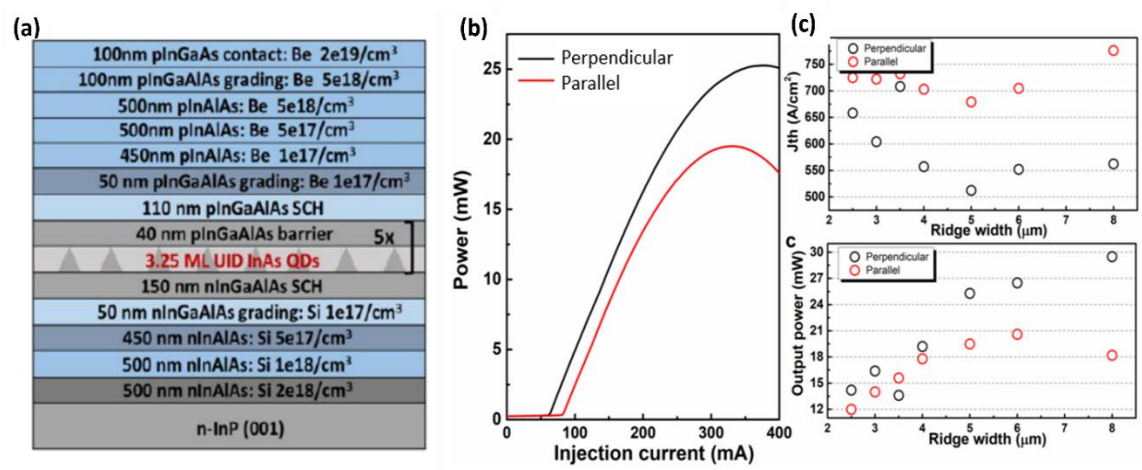

Figure 63: (a) Schematic of the laser epi stack. All quaternary alloys were grown digitally. (b) LI curve comparison between the perpendicular and the parallel ridge configuration. (c) The extracted threshold current density and the maximum output power for the two different ridge configurations.

The same laser material has also been fabricated into photodetectors (PDs). The schematic and the cross-sectional view and top-view scanning electron microscope (SEM) images of a fabricated device are shown in Figure 64.

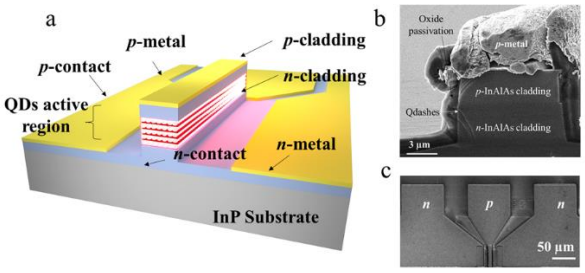

Figure 64. (a) Schematic diagram of the fabricated waveguide photodetector. (b) Top-view and (c) cross-sectional views of the fabricated device.

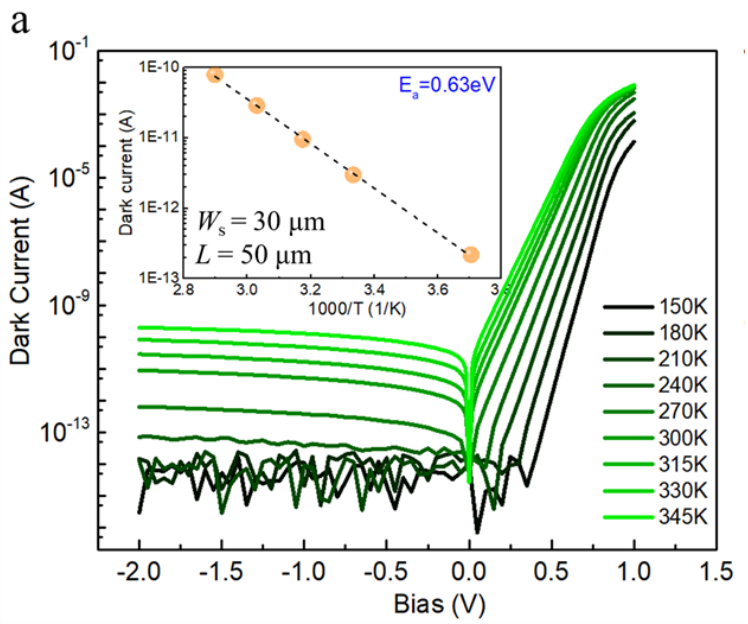

Figure 65: (a) Temperature dependent measurement of the Current-voltage characteristics of a 30 × 50 µm^2 device. Inset: Arrhenius plot of temperature dependent dark current at -1 V.

The dark current voltage (I-V) curves of a 30 × 50 µm^2 photodiode were measured from 150–345 K in a variable temperature probe station and recorded by a semiconductor device analyzer, as shown in Figure 65. Due to the detection limit, dark currents measured below 240 K are too low to be resolved. At room temperature, a dark current of 5.2 pA is obtained under a bias voltage of -1 V, which corresponds to an ultra-low dark current density of 3.3×10^{-7}A/cm^2. Linear fitting of the Arrhenius plot of the temperature dependent dark current biased at -1 V is shown in the inset in Figure 65. The extracted activation energy (E_a) of 0.63 eV is ~78% of the InAs Qdash bandgap (Eg) (~0.8 eV) at room temperature, indicating that the dark current is dominated by both the diffusion and generation-recombination components.

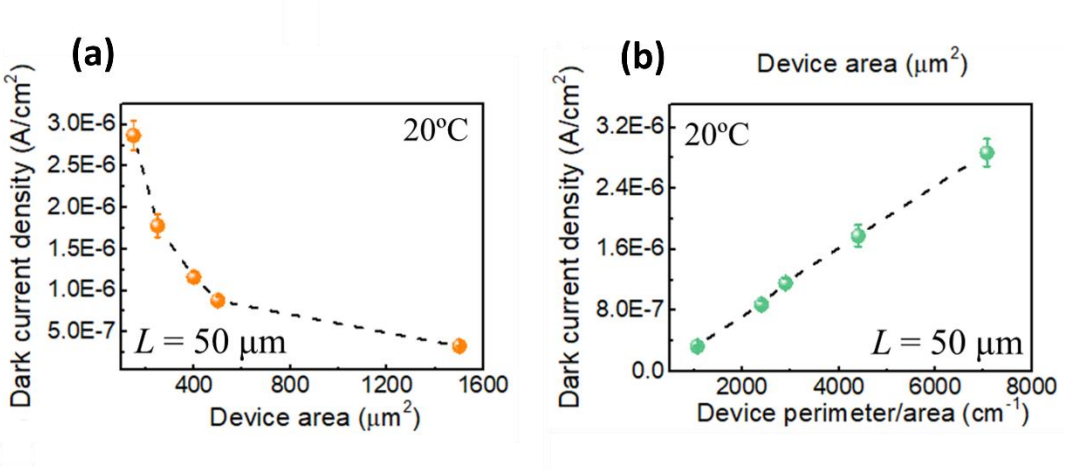

Figure 66: Dark current density as a function of (b) the device area and (c) the device perimeter/area for a series of devices with a fixed PD mesa length of 50 µm at room temperature.

For a fixed PD mesa length of 50 µm, dark current and dark current density are plotted as a function of the device area, and device perimeter/area respectively for a series of devices at room temperature, shown in Figure 66. The average dark current density with the narrowest stripes (2.8×10^{-6}A/cm^2 for 3 µm stripes) yielded ~8-fold increase compared to devices with a wide stripe (3.3×10^{-7}A/cm^2 for 30 µm stripes). The slope between the dark current density and device perimeter/area indicates that the surface leakage still exists and requires further improvement of the device passivation process. Still, the dark current density of 3.3×10^{-7}A/cm^2 is around five orders of magnitude lower than state-of-art Ge PDs and two orders of magnitude lower than the commercial InGaAs PDs[143]. More in depth characterization of the PDs can be found elsewhere[144].

Micro-ring lasers have also been fabricated and characterized on this material platform[145]. Ring-waveguide lasers based on the whispering gallery mode (WGM) with radii ranging from 25 µm to 100 µm and a ring width of 4 µm have been investigated. An example set of top-view and cross-sectional SEM images of a ring with 60 µm radii is shown in Figure 67.

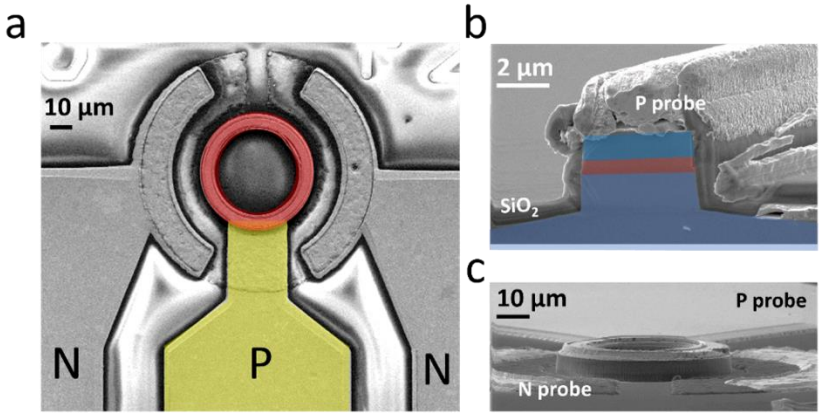

Figure 67: SEM images of the fabricated device. Top-view (a) and cross-sectional views (b), (c) of a fabricated microring laser. Highlighted color sections: red, microring laser (a) and active region (b); blue, III–V; yellow, selected metal contacts.

The output power was measured by capturing the radiation out-coupling from the ring cavity by an integrating sphere placed 5 mm from the ring cavity edge. A ~90° azimuthal light-radiation-collection angle was estimated for such geometry. Considering the angular directivity pattern of radiation and the detector's spectral sensitivity, the optical power magnitude (0.18 mW at an injection current of 80 mA) presented here is an underestimate. Figure 68a shows the light-current-voltage (L-I-V) characteristics of a representative ring laser of outer R=100 µm and ring width (W) 4 µm, with a threshold current (I_{th}) of 13 mA. A logarithmic plot of the LI curve is presented in the inset in Figure 68a, exhibiting a 'S-shaped' nonlinear transition from spontaneous emission to stimulated emission. CW operation with no sign of performance degradation and power roll-off was observed up to injection current values as high as 5 times threshold. The corresponding threshold current density J_{th} has an ultra-low value of 528 A/cm^2, which indicates excellent non-radiative recombination suppression at the deeply etched sidewalls of the Qdash structures.

The spectra shown in Figure 68b were measured by coupling output light into a lensed fiber connected to an optical spectrum analyzer. Only a few unique modes with spectrally distant spacing were observed. This is most likely caused by relatively few WGMs falling within the gain spectrum of the

QDashes. Due to the different overlap of WGMs with the QDashes, each WGM can have different quality factors and different susceptibility to defects and imperfections. Here, an extinction ratio over 26 dB was observed for the primary lasing mode at ~1530 nm near the PL intensity maximum of the ground-state optical transition in QDashes, due to the advantages in spatial overlapping of emitters to the surrounding cavity, radiative emission rate, or resonance in frequency. The peak at 1550 nm was plotted separately in Figure 68b, and the fine mode spacing was measured to be ~1.06 nm. The group refractive index of the cavity was calculated to be 3.6 accordingly.

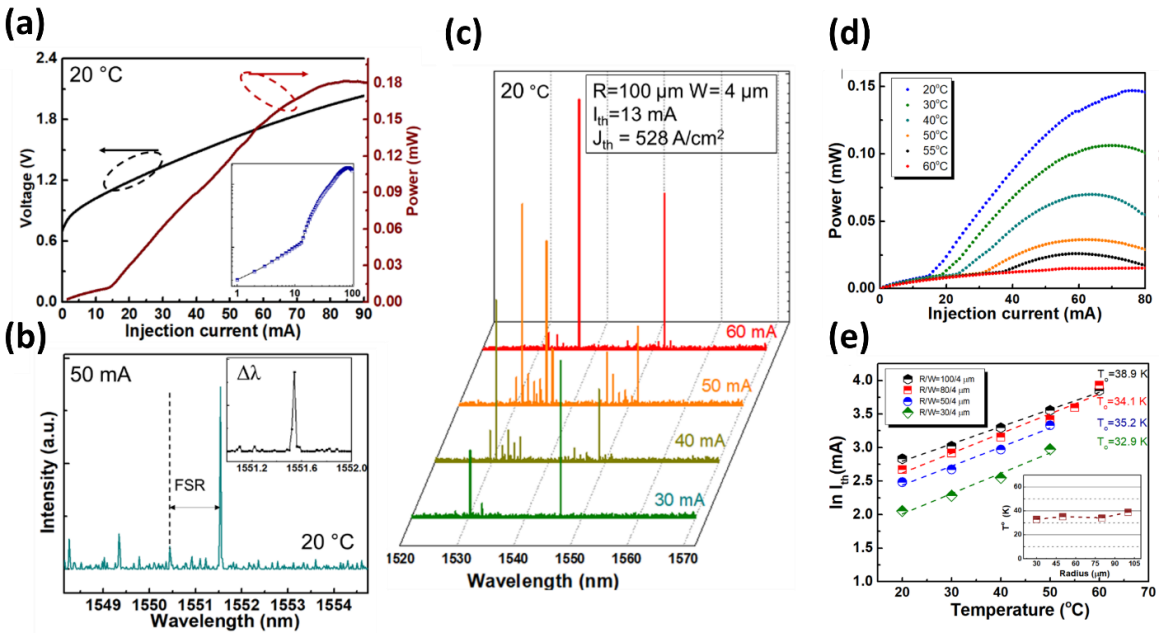

Figure 68: (a) Light-current-voltage characteristics, inset: LI curve in the log-log scale. (b) Zoomed-in view of the spectrum taken at 50 mA. (c) Emission spectra at increasing injection currents of a micro-ring laser with a radius of 100 μm and a ring width of 4 μm under CW operation at room temperature. (d) Micro-ring laser with a radius of 100 μm and ring width of 4 μm shows continuous-wave lasing up to 55°C. (e) Plots of threshold current versus stage temperature for four different laser devices with various outer-ring radii. Inset: extracted characteristic temperature T_0 as a function of outer-ring radius.

High-temperature CW operation of the same device (r=100 μm, w=4 μm) was demonstrated up to 55°C. Temperature dependent lasing of this device is shown in Figure 68d. A plot of the CW threshold

current versus the stage temperature for this device, along with three other lasers of various outer-ring radii, is shown in Figure 68e. The characteristic temperature T_0 was extracted by fitting the increase in threshold using an exponential function $I_{th}(T) \propto \exp(T/T_0)$, and found to be ~39 K. This is a record-high value for 1.55 μm microring QDash lasers. The inset in Fig. 6(b) shows the extracted T_0 as a function of outer-ring radius. Decrease in the ring cavity size leads to a slight deterioration of the maximum operating temperature, decreasing from 55°C to 50°C when the outer-ring radius scales from 100 μm to 30 μm. T_0, however, stays almost constant in the range of 30-40 K. This suggests minimal increase of thermal resistance for smaller ring cavities.

7.3 Summary

InAs QDs grown on GaAs can be tuned to emit around 1178 nm for pumping a sodium optical clock. Without the InGaAs pre-layer, as in the 1300 nm InAs QD lasers, the nucleation is delayed from 1.4 ML to 1.9 ML. Adjusting the deposition sequence has significantly improved the PL intensity and 2.55 ML of total amount of InAs renders the best PL, the same as the 1300 nm QDs. Unlike the 1300 nm QD with InGaAs prelayer and capping layer, the PL properties of the 1178 nm QDs experience a monotonic and very sensitive dependence on the growth temperature. Although it would indeed make hitting the target wavelength tricky, it provides a very sensitive gauge for the accuracy of the temperature calibration.

Due to the lower lattice mismatch and asymmetric surface adatom diffusion, the InAs nanoparticles emitting around 1550 nm grown on InP elongate in the [1 -1 0] direction and the nanoparticles are generally noted as Qdashes. Since the strain is less relaxed in the Qdashes, post-growth annealing of the exposed Qdashes results in more circular islands with wider size distribution. FP lasers with ridges aligned to the [1 1 0] crystal orientation shows lower threshold current and higher outpower power due to the stronger interaction between the electric field and the dipole within the dashes. Other high-

performance devices, namely PDs and micro-ring lasers, have also been demonstrate with the same material stack.

Chapter 8
Summary, future work, and other interesting applications

8.1 Approaching the heterogeneously integrated QW laser performance

Monolithic integration of III-V light sources on Si has always been considered as the ultimate solution for realizing on-chip light sources for Si photonics. Epitaxially grown devices could leverage most of the existing CMOS manufacturing, which ensures low cost and high yield. However, due to the unavoidable crystalline defects originated from the dissimilarities of III-Vs and Si, the performance and reliability of the epitaxially grown devices severely lag behind the heterogeneously integrated counter parts. Considerable amount of effort has been devoted to eliminating the defects, mainly the threading dislocations as they penetrate all device layers and are expected to be the most detrimental factor of device performance. Many research groups have successfully developed low defect (~7 to 9×10^6 cm^{-2}) GaAs virtual substrate structures grown on CMOS compatible Si with strained layer superlattice[81–83]. However, the achieved TDD is still high compared to the technological desirable levels ($<10^5$ cm^{-2}). In Chapter 3, an asymmetric step graded filter has been introduced which has greatly promoted the degree of relaxation, resulting in a TDD lower than 1.5×10^6 cm^{-2}. The recently discovered MD formation near the active region from the CTE mismatch has opened up another design space for defect management. The inserted trapping layers effectively block the MDs from touching the active region and into the highly doped cladding layers, where the non-radiative recombination rate would be greatly suppressed. This discovery suggests that the improved lifetime from reducing the TDD alone[86] could just be removing the sources for MDs one at a time.

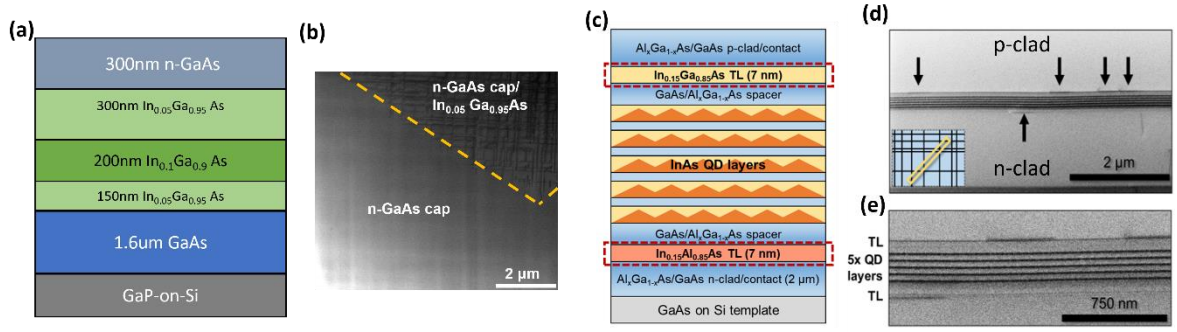

Figure 69: (a) Schematic of the buffer structure with ASG filter. (b) Example PVTEM measured on top of the GaAs capping layer. (d) Schematic of the full laser stack with inserted TLs. The materials were chosen to minimize the band offset. (d) XTEM with [0 0 1] surface normal. *P*-side appears to have more MDs than the *n*-side. (e) Zoomed-in view on the active region, showing that the MDs are effectively blocked away from the active region.

After about 3 to 4 years with six generations of devices, with the newly introduced defect management tools, the extrapolated lifetime of these epitaxially grown QD laser has been improved from 800 hours at room temperature to over 200,000 hours at 80 °C. This is indeed a significant achievement bringing these epitaxial devices one big step forward to the real-world application. However, just as a friendly reminder, there is still a noticeable gap in terms of reliability between the epitaxial QD lasers and bonded QW lasers. As shown in Figure 70 below, the red solid line needs to be further flattened and the effort required for that 10% improvement might be a lot more compared to going from 800 h at room temperature to more than 200,000 h at 80 °C.

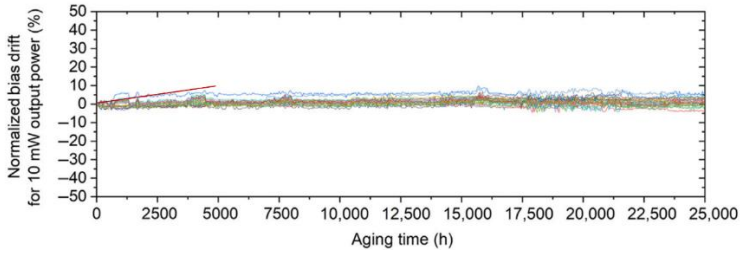

Figure 70: Reintroduced aging results of the bonded QW lasers at 80 °C after 25000 hours. The solid red line roughly depicts the change in the bias required for 10 mW output power in the best epitaxial QD lasers.

Fortunately, as discussed in Chapter 3 and 4, the "ASG" filter and the MD trapping layers are far from being optimized. For the ASG filter structure, it is known that a continuous grading would be more effective in promoting relaxation than a step graded structure as the misfit arrays would form at the most energetically favorable locations rather than at fixed interfaces[146]. Since the strain energy is proportional to $\varepsilon^2 h$, it is worth trying both the linear and parabolic gradings on both the compressive and tensile side of the ASG structures. As suggested in Figure 22, the current trapping layer design, which uses the same indium composition as the active region QWs to avoid growth complications, is imperfect with MDs leaking through the trapping layer. Investigating the full design space of the trapping layers, in terms of indium composition, thickness, and location, with respect to the specific laser stack might be needed to locate the optimum trapping layer structure. However, better TD elimination with better filters and better MD blocking with optimized trapping layers would inevitably render the crystal more brittle with higher residual tensile stress. To avoid film cracking, designs with thinner total III-V film thickness are preferential, as suggested in the latter half of Chapter 4.

It is worth pointing out that thinner film design is only to "go around" the cracking issue when the film becomes more fragile by lowering the energy release rate. The residual tensile stress is not reduced. Such high residual tension could possibly hurt the device performance for the distorted band structure[12,147] and driving point defects promoting REDC. To fundamentally reduce the residual tensile stress, using GaAsP as the cladding material could be a viable option due the lower CTE, if a phosphorus source is available. A more accessible approach in our chamber is to utilize pocket geometry introduced in Chapter 6. While using the same materials and growth conditions, it is possible to fundamentally reduce the residual tension by growing in narrow trenches. Evidentially, no MDs elongated along the trench long edge were observed for the lower tension across the trench. Another idea to fundamentally reduce the number of MDs near the active region then comes into the

picture. The distribution of the MDs near the active region is asymmetric. A much higher linear density has been observed along the [1 -1 0] direction[122]. Thus, as shown in Figure 71 below, if the trench (blue rectangle) long edge is aligned with the [1 1 0] direction, it is possible to eliminate the MDs in the [1 1 0] direction. The remaining MDs in the [1 -1 0] direction could potentially be less detrimental as they affect a much smaller area.

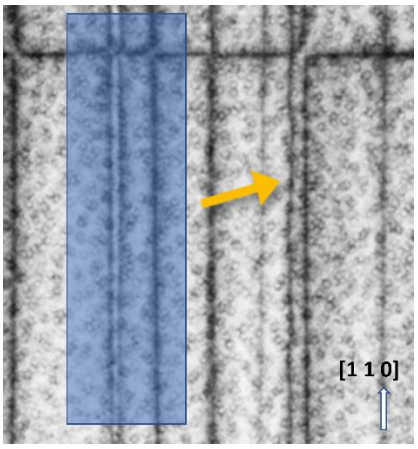

Figure 71: PVTEM image of a QD laser active region. The yellow arrow points to an example MD. The "coffee-bin" contrasts are the QDs.

The challenge would be to identify the crystal orientation of the in-trench GaP surface. Even though the GaP would potentially randomly pick between the [1 1 0] and the [1 -1 0] orientation when deposited on a non-polar Si substrate, since the Si wafer used has a small offcut, with the exact same growth conditions, the GaP should have the same crystal orientation with respect to the 300 mm Si wafer between manufacture cycles. If this MD elimination strategy were to succeed, the in-trench lasers are then expected to outperform the devices grown on blanket GaP/Si template, despite the higher threading dislocation density. It is worth demonstrating this strategy on blanket GaP/Si with in-house patterned oxide trenches before trying this out on the fully patterned chips.

8.2 Interesting new directions

8.2.1 Monolithic on-chip light source for photonics biosensors

The global biosensor market size has reached USD 21.96 billion in 2020 and is forecasted to exceed USD 34 billion by 2026. Within this market, optical biosensors, via evanescent field detection, are identified as the most lucrative technology.

Figure 72: Projected global biosensor market in the next few years.

Medical testing and diagnostics outside of the clinic is the new normal, which has been further boosted during the COVID-19 pandemic. This would require handheld medical devices that are cheap to build, light weight, and robust against environmental fluctuations. The well-developed silicon photonics integrated circuit, among other available technologies for fabricating photonic biosensors, is one of the most promising for its compatibility with CMOS foundry processes.

Similar to the communication applications, the major roadblock for obtaining a cheap lab-on-a-chip is the lack of monolithically integrated light source. Provided that the QD lasers on planar Si, or more ideally on patterned Si template with PIC laid out, could demonstrate comparable performance to heterogeneously integrated counterparts, a true lab-on-a-chip could be realized with low cost and could be deposited and fabricated on 300 mm Si. Since most of the bio-samples for quick testing would be in aqueous solutions, e.g. blood, saliva, and urine, designing a light source that has minimum water absorption would be required for high sensor performance. From the wafer absorption spectrum

below, a laser emitting around 450 nm would be ideal, but absorption in the green-red range is also acceptable. To achieve this, a QD laser emitting at 1178 nm, mentioned in Chapter 6, could be a candidate after frequency doubling. Interferometer structures, either MZI or YI[148], currently hold the highest sensitivity and lowest detection limit among other detection architectures and such structures could readily be made with Si waveguides and its native oxide cladding. The waveguides could potentially be specifically functionalized with colloidal QD coatings to increase the selectivity of the detectors for the programmable surfaces of these colloidal QDs. The sensitivity and detection limit could also be improved as QDs receptors have no "orientation".

Figure 73: Water absorption spectrum suggesting that a light source working around 500-600 nm would be ideal.

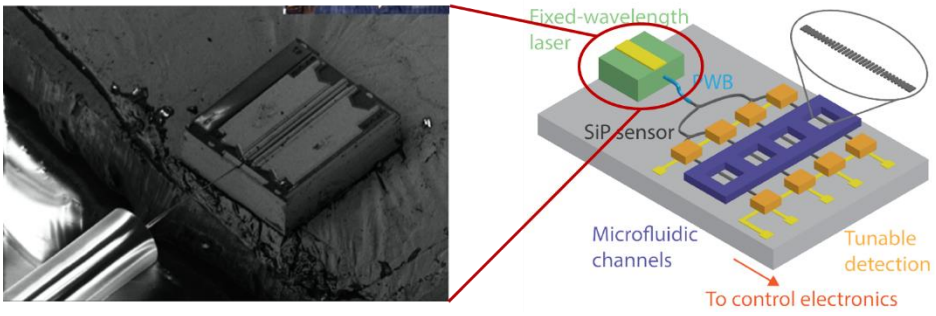

Figure 74: Example architecture of an on-chip biosensor. The laser was picked and glued onto the platform with photonic wire bonds (PWB) connecting the laser to the sensor waveguides. A monolithic light source via direction epitaxy would greatly reduce the cost and improve scalability[149].

Combining the monolithic on-chip light source, Si-based detection architecture, microfluidics systems, on-chip detection, and read out, a high-performance handheld biosensor could be realized. Such devices could be deployed anywhere around the globe since they don't need a well-established lab to function. Early detection of various types of cancers, Alzheimer, infectious diseases, and general health monitoring could potentially be made possible at every household.

8.2.2 QDs as ideal quantum light emitters

All the above research and applications are focusing on QDs as an on-chip light source for their exceptional insensitivity to crystalline defects. But these nanoparticles, confining carriers in all three dimensions, are "artificial atoms" as well, which naturally makes them good quantum light emitters.

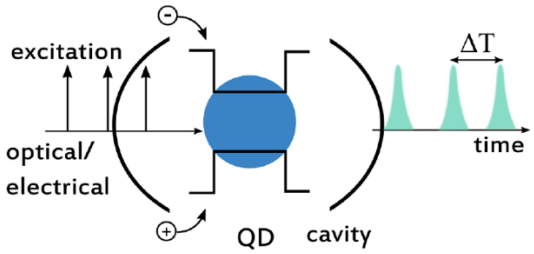

Figure 75: Schematic of a QD quantum light emitter coupled to a resonant cavity to improve extraction efficiency.

Most quantum light experiments are done with pumping nonlinear waveguides or cavities via spontaneous four-wave mixing or spontaneous parametric down-conversion since these parametric sources work at room temperature and can be made highly identical. However, these parametric sources are non-deterministic which greatly hinders the scalability. On the other hand, QDs are naturally deterministic single/entangled photon sources. Recently the performance of epitaxial QD quantum light source has exceeded that from the parametric sources in terms of purity, indistinguishability, and brightness.

The QDs are ideal emitters for polarization entangled photon pairs through biexciton cascade process[150]. Polarization entanglement is beneficially for quantum communication as PM fibers are well-established. Locally generated entangled photon pairs with the source are also better suited for quantum repeaters. The main limitation for QDs to generate perfect polarization entangled photons is the fine structure splitting (FSS) from geometric asymmetry originated from the asymmetric surface adatom diffusion on the III-V surfaces. The tolerance of the diffusion asymmetry could be tuned with external fields, either electromagnetic or hydraulic. It is always more desirable and cheaper to tune the FSS with the built-in fields from the crystal itself. From my experience, higher lattice mismatch would result in dots with more symmetric shape and lower FSS. It has also been reported in literature that InAs/GaAs QDs (~7% mismatch) experience smaller FSS compared to the InAs/InP QDs (~3% mismatch). By growing on the Si substrate, the In(Ga)As QDs could be deposited at any arbitrary lattice constant, thus enabling a wide tuning range for zero FSS. Epitaxial QDs are also advantageous as they could be deposited within an optical cavity to increase the extraction efficiency and be fabricated into a quantum light diode which could be triggered electrically.

8.3 Conclusions

The newly introduced ASG structure that has greatly improved the degree of relaxation in the filter layers and the inserted TLs that have removed MDs from the active region have significantly boosted

the high temperature performance of the epitaxial QD lasers on Si. The more than 200,000 hour extrapolated lifetime at 80 °C has restored the promises of monolithically integrated light source on Si photonic chips. Both tools are still at the "proof-of-concept" stage and are subject to further optimization. Clear path has been laid out for potentially obtaining native substrate defect level with continuous grading schemes and perfect TLs in terms of composition, thickness, and location. Yet, lower defect levels and stronger MD blocking effect render the film more brittle and more likely to crack with higher wafer curvature. A simplified model uniting thin film fracture mechanics and dislocation-mediated plastic relaxation suggests that thinner stack is required to generate less warped and crack-free film with the same residual tensile stress.

Blanket-substrate-level crystalline quality has been achieved within the pre-patterned pockets on Si photonics chips for monolithic integrations. The chip architecture unexpectedly provides a way to fundamentally lower the residual tensile stress and thus the MD density. This alone should further promote device performance and reliability as strain is known to encourage dislocation climb and potentially alter the band structure. Provided that the epitaxial QD lasers on Si with effectively infinite lifetime could be obtained soon, it would not only benefit the communication applications but anywhere that might require an on-chip gain element.

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