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Design and Implementation of a Three-Phase Eight-Level Flying Capacitor Multilevel Rectifier for Future Data Center Power Delivery

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***Abstract*—The rapid rise in the power consumption of data centers, coupled to the growth of artificial intelligence training and inference, is forcing an evolution in rack power delivery architectures as rack power levels are pushed beyond 100 kW. Future data centers are expected to utilize ultra-dense, in-rack three-phase rectifiers and 800 V distribution to mitigate distribution losses and cabling weight. This work discusses the design and evaluation of a flying capacitor multilevel (FCML) converter as a three-phase PFC rectifier for future data center power delivery networks, where efficiency and size will be increasingly important. This work presents several innovative solutions related to EMI, PS-PWM control, and gate driving to address practical considerations. A hardware prototype was constructed and tested up to a dc voltage of 700 V, 4.98 kW at a conversion efficiency of 98.5%.**

I. Introduction

Global capacity for AI-focused data centers are expected to rise at an annual rate of 20%, nearly quadrupling by the end of the decade [1]. Increased site power demand and rising thermal design powers of modern CPU/GPU/xPUs [2] are motivating the design of racks which consume significantly more power, with current designs surpassing $100\,\mathrm{kW}$ [3], and $1\,\mathrm{MW}$ racks being proposed [4], [5]. This is forcing a departure from traditional $48\,\mathrm{V}$ rack power delivery utilizing single-phase rectifiers [6], as cabling losses and weight would be excessive. To improve the site efficiency and increase rack power levels, future data centers are expected to use $800\,\mathrm{V}$ as the rack distribution voltage [4], [5], [7]. At these voltage levels, the common $650\,\mathrm{V}$ power semiconductor (Si or GaN) cannot be used in conventional topologies, necessitating alternative approaches to achieve high efficiency and small size. One such topology that has demonstrated superior performance is the flying capacitor multi-level (FCML) converter [8]. In this work, we propose the use of a high-level count, eight-level FCML converter design, and overcome practical and industry-relevant challenges. Specifically, the design presented in this work emphasizes EMI filter design, advanced three-phase modulation schemes for the FCML converter, and high efficiency gate drive power delivery.

Supported by Fannie and John Hertz Foundation

II. Three-Phase Flying Capacitor Multilevel Rectifier

The flying capacitor multilevel (FCML) converter [8] is a hybrid switched capacitor topology that enables efficient and power dense power conversion through two key mechanisms. First, due to the multilevel structure of flying capacitors network, the FCML converter enables the utilization of low voltage switches compared to conventional two- or three-level converters. This improves converter efficiency as both the conduction and switching losses of series-stacked low voltage switches is significantly lower than those of a single switch rated for blocking the full system voltage [9]. Second, inductor volt-seconds may be reduced through interleaved switching, resulting in switch node voltages v_{sw} which have a reduced ac amplitude and increased frequency compared to two-level converters. The reduction in inductor volt-seconds enables significantly smaller and more efficient magnetic components. In this work, we operate the FCML converter with phase-shifted PWM (PS-PWM). In this scheme, all high-side switches are driven with signals of the same duty cycle and the switching signals are equally phase shifted throughout the switching period.

This work focuses on the design, optimization, and practical realization of a three-phase FCML rectifier aimed at the power level, efficiency, and power density required for future data center power delivery architectures. Fig. 1 shows a schematic drawing of the designed three-phase, eight-level FCML rectifier. Compared to previous high-performance single-phase prototypes [10], [11], this work leverages the inductor current ripple reduction properties of three-phase systems. Although three single-phase inverters could be combined to form a valid three-phase inverter/rectifier (as was done in [12], [13]), the ac-side filter inductors must store increased energy as this architecture does not effective leverage the common-mode voltage of three-phase systems.

A. Modulation Considerations

Center-aligned PWM is a powerful technique to reduce inductor energy storage requirements in three-phase converters (e.g., motor drive inverters [14]). This modulation scheme

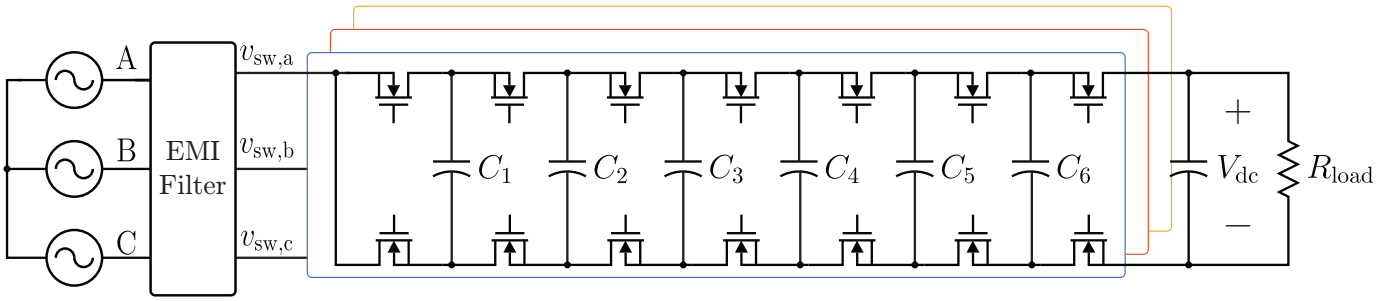


Fig. 1: Three-phase eight-level FCML ac/dc converter schematic. The FCML converter enables the utilization of low voltage semiconductors and reduced magnetic stress to achieve the efficiency and power density goals of next generation data center power delivery. The implemented EMI filter is illustrated in Fig. 3(a).

results in the center of all three switch node voltage pulses occurring at the same time. Center-aligned PWM synthesizes a neutral point voltage which enables an effective doubling in the inductor current ripple frequency compared to the switching frequency. One common implementation to achieve center-aligned PWM utilizes triangle PWM carriers with the carriers aligned in time.

In an FCML converter, the time at which the center of the switch node voltage pulse occurs varies with duty cycle with respect to the PWM carriers. To achieve center-aligned v_{sw} pulses throughout the entire line cycle, the phase shifts of the PS-PWM carriers of phase B and phase C relative to phase A cannot be constant and must vary with the duty cycle [15], [16]. To achieve the switch node voltage alignment, two sets of PS-PWM carriers are used for the phase B and C FCML converters. The first set of carriers is fully aligned with those of phase A while the second set is phase shifted by $2\pi/(2(N-1))\,\mathrm{rad}$. The second set of carriers for phase B is utilized if its duty cycle region is different from that of phase A. The duty cycle regions are calculated according to the procedure outlined [16]. The same process is used for determining which sets of carriers to use for phase C. Fig. 2 shows simulated switch node voltages v_{sw} and inductor currents i_{L} for the eight-level FCML rectifier investigated in this work. As can be seen, the switch node pulses are center-aligned and the inductor ripple frequency is increased, most clearly seen in $i_{L,\mathrm{a}}$.

Space vector modulation (SVM) [17] is widely used for both increasing the synthesizable ac voltage amplitude (i.e., extending the linear modulation range), reducing the line current distortion, and reducing the inductor current ripple. This increase in modulation depth is enabled by a decrease in the deviation in duty cycle from 50% by injecting appropriate zero voltage vectors [14]. In an FCML converter, this decrease in the extrema of the duty cycle increases the flying capacitor voltage ripple. The flying capacitor voltage ripple is proportional to both the time when the capacitor is charging or discharging and the inductor current. The flying capacitor

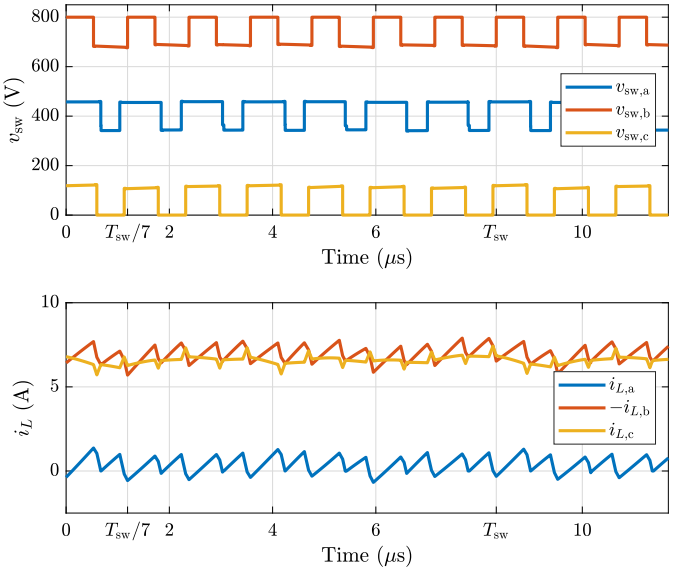


Fig. 2: Simulated switch node voltages v_{sw} and inductor currents i_L. The v_{sw} pulses are center-aligned and the inductor currents i_L have a ripple component at $2(N-1)f_{\mathrm{sw}}$. The converter supplied $5.5\,\mathrm{A_{rms}}$ to a $50\,\Omega$ wye-connected resistive load from an $800\,\mathrm{V}$ dc source.

charging or discharging time Δt is given by

$$\Delta t = \begin{cases} DT_{\mathrm{sw}} & 0 < D < \frac{1}{N-1} \\ (1-D)T_{\mathrm{sw}} & D > \frac{N-2}{N-1} \\ \frac{T_{\mathrm{sw}}}{N-1} & \text{othw.} \end{cases} \tag{1}$$

where N is the number of voltage levels apparent in the switch node voltage. Since SVM reduces the extrema of the duty cycle, the flying capacitor (dis)charging time is increased at the peak of the line current and the flying capacitor voltage ripple is increased. SVM thus allows a decrease in inductor size at the cost of increased flying capacitor voltage ripple.

B. EMI Filter Design

The conducted emissions of grid-connected rectifiers are regulated by standards such as CISPR 32 [4]. This work presents the design of a differential mode filter which meets the relevant standards with significant margin. The differential mode filter can be viewed as a passive network which must attenuate the harmonics of the switch node voltage v_{sw} to

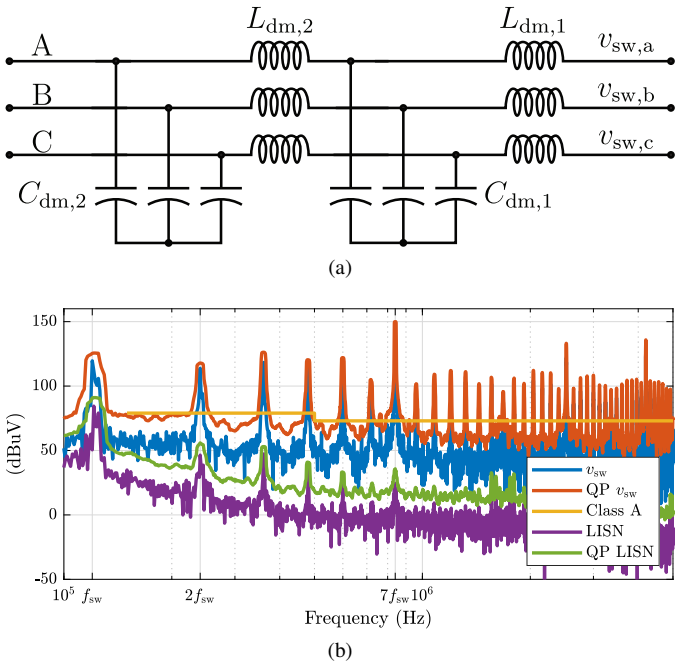


Fig. 3: (a) Two-stage differential mode EMI filter schematic designed to meet the CISPR 32 Class A standard. Component values are provided in Table I. (b) Simulated spectra of the switch node voltage v_{sw} and the voltage measured across the 50 Ω LISN resistor. Traces QP v_{sw} and QP LISN are conservative estimates of the quasi-peak measurements.

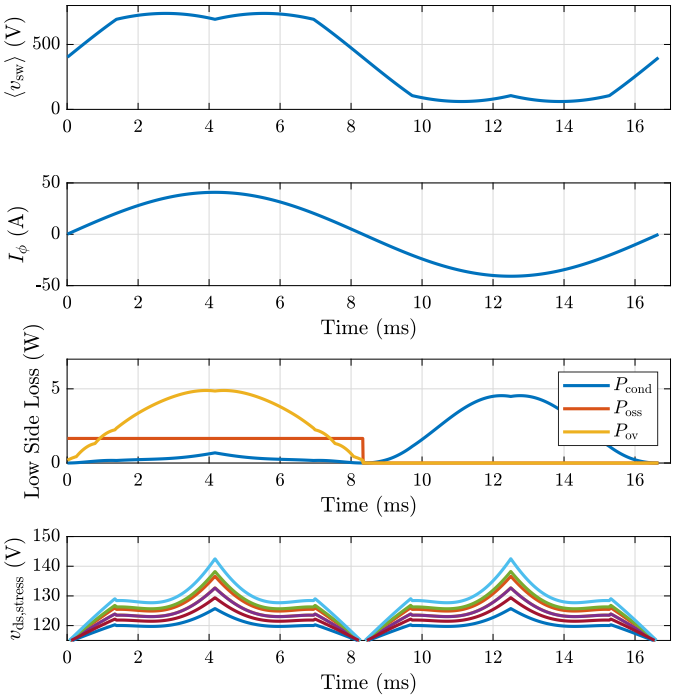


Fig. 4: Analytical average switch node voltage, phase current, low side transistor losses, and transistor voltage stress for one phase. The converter is connected to a 480 $\mathrm{V_{rms}}$ line-to-line grid, processing $P_{\mathrm{out}} = 8\,\mathrm{kW}$ per phase at $f_{\mathrm{sw}} = 120\,\mathrm{kHz}$. Switching losses are broken down into overlap losses P_{ov} and switch output capacitance hard-switching loss P_{oss}. This design operates the flying capacitors with significant voltage ripple to improve power density while maintaining sufficient transistor voltage stress margin.

a level acceptable as measured by the receiver resistor as part of a line impedance stabilization network (LISN). If the converter switching frequency f_{sw} is chosen to be sufficiently below the minimum frequency of interest (for CISPR 32, 150 kHz), the harmonics of f_{sw}, rather than f_{sw} itself, must be attenuated, resulting in reduced filter attenuation requirements and volume. Ideally, the lowest frequency contained within the switch node voltage of an FCML converter is $(N-1)f_{\mathrm{sw}}$. However, if the flying capacitor voltage ripple and flying capacitor voltage imbalance are considered, the harmonics from $2f_{\mathrm{sw}}$ to $(N-2)f_{\mathrm{sw}}$ must similarly be attenuated. In this work, a switching frequency of 120 kHz was selected to prevent the sideband of the switching frequency from appearing in the CISPR measurement band which begins at 150 kHz. At the nominal output power of 24 kW, the simulated emissions at $2f_{\mathrm{sw}}$ (240 kHz) were 121 $\mathrm{dB}\mu\mathrm{V}$ while the emissions at $(N-1)f_{\mathrm{sw}}$ (840 kHz) were 150 $\mathrm{dB}\mu\mathrm{V}$. To meet the CISPR Class A limit with 12 dB of margin, the filter must achieve 54 dB of attenuation at 240 kHz and 89 dB of attenuation at 840 kHz. Assuming a two-stage filter design, this 240 kHz attenuation requirement determines the filter attenuation specification as a filter designed to attenuate the $(N-1)f_{\mathrm{sw}}$ harmonic would not have enough attenuation at $2f_{\mathrm{sw}}$ to meet the limit with sufficient margin, a departure from the finding in [18]. Fig. 3 shows the implemented EMI filter topology and simulation results. Traces QP v_{sw} and QP LISN are conservative estimates of the quasi-peak measurements typically regulated by standards such as CISPR 32 by accounting for the resolution bandwidth of the EMC test receiver [19]. The implemented filter values are provided in Table I. To minimize filter volume, both components are chosen to be of the same value (i.e., $L_{\mathrm{dm},1} = L_{\mathrm{dm},2}$ and $C_{\mathrm{dm},1} = C_{\mathrm{dm},2}$) [20]. C_{dm} was chosen such that 10° of phase displacement due to the filter would occur at 10% of the nominal output power [21]. The corner frequency of this two-stage filter must be

$$f_{\mathrm{corner}} = 2f_{\mathrm{sw}}(A)^{1/4}, \tag{2}$$

where A is the (linear) desired attenuation as the attenuation increases at a rate of 80 $\mathrm{dB/decade}$ beyond the corner frequency of the filters. The differential filter inductance to achieve this corner frequency is then

$$L_{\mathrm{dm}} = \frac{1}{(2\pi f_{\mathrm{corner}})^2 C_{\mathrm{dm}}}. \tag{3}$$

C. Performance Characteristics

Fig. 4(a) shows the analytical low-side transistor losses over one grid period for one of the three phases. The transistor overlap losses were calculated according to the procedure in [22]. Recent work [11] has shown that operating the flying capacitors with significant voltage ripple can result in designs with improved power density without excessive efficiency penalties. To achieve both large flying capacitor voltage ripple and utilization of the high performing 200 V EPC GaN devices, an eight-level design was selected. Fig. 4(b) shows the

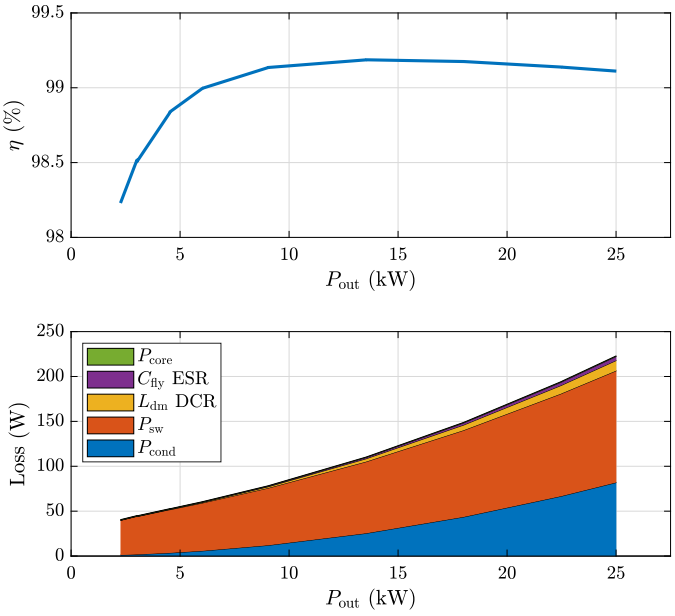


Fig. 5: Simulated efficiency and breakdown of the primary loss mechanisms. The eight-level FCML rectifier operates from a 800 V dc voltage to create a 480 V_{rms} line-to-line grid across a three-phase, wye-connected resistive load. The simulated peak efficiency is 99.2% at an output power of 13.5 kW while the full load efficiency is 99.1% at an output power of 25 kW.

calculated transistor $v_{\text{ds,stress}}$ as a result of the flying capacitor voltage ripple. For switches connected to two flying capacitors, $v_{\text{ds,stress}}$ is the difference in adjacent flying capacitor voltages. For the final two switch pairs, $v_{\text{ds,stress},1} = v_{C,1}$ while $v_{\text{ds,stress},7} = V_{\text{dc}} - v_{C,6}$. This stress accounts for the flying capacitor small-signal capacitance de-rating with respect to voltage and the charging/discharging time across the line cycle. Due to utilizing space vector modulation, the peak $v_{\text{ds,stress}}$ occurs at the peak of the line cycle.

Fig. 5 provides the simulated efficiency and loss breakdown for the proposed converter, when the converter operates as an inverter driving a wye-connected resistive load. The converter attains a simulated peak efficiency of 99.2% and a full-load efficiency of 99.1% at an output power of 13.5 kW and 25 kW respectively. At the full load operating point, the losses per device are 4.9 W, the primary limit for the converter's output power. The core losses of the inductors within the EMI filter and the semiconductor losses were calculated according to the manufacturer-provided models.

D. Controller Design

Power factor correction (PFC) control is accomplished with a conventional multi-loop controller in the direct-quadrature (dq) domain [14], shown in Fig. 6. The outer, slower dc bus voltage controller commands a d-axis current reference while the q-axis reference current is zero to achieve unity power factor operation. A three-phase synchronously rotating reference frame PLL [23], [24] is used to obtain the grid angle.

A small dead time (0.3% of the switching period) is inserted between switching events of the same switching cell to prevent shoot through. This dead time, however, induces a 5th harmonic ripple in the line current [25] creating a disturbance the controller must reject. To reduce the THD of the line current, an adaptive feedforward Cancellation (AFC) controller is implemented [13], [26]. The AFC controller provides a large gain at the 6th harmonic (360 Hz), enabling the controller to reject the periodic dead time disturbance and other harmonics of this disturbance.

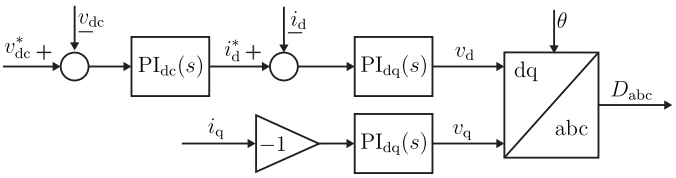
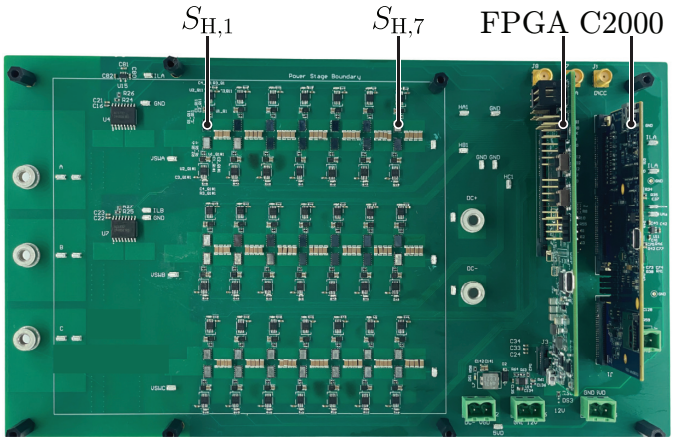
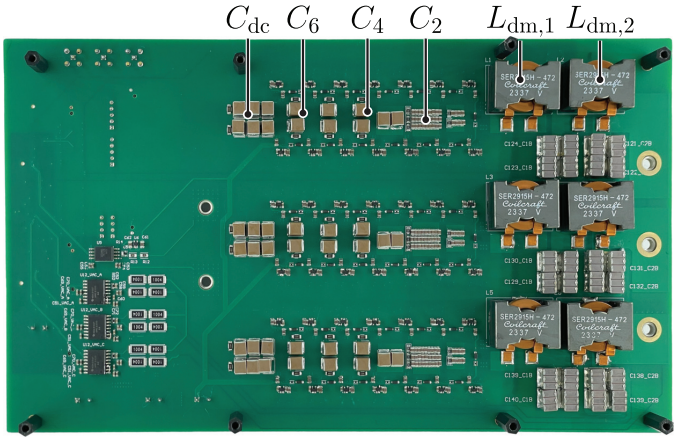


Fig. 6: Power factor correction (PFC) multi-loop controller structure. A three-phase PLL (not shown) is used to obtain the grid angle from the measured grid voltage.



(a)



(b)

Fig. 7: Photograph of the developed hardware prototype. The PCB area is 11" × 6.3" while the power stage area is 6.45" × 5.54". The height of the power stage is 0.72". When operated at the design output power of $P_{\text{out}} = 25\,\text{kW}$, the prototype achieves a power stage power density of $60.24\,\text{kW/dm}^3$.

TABLE I: Component List

Component	Description	Part Number
Power Semi.	200 V, 3.5 mΩ	EPC2304
Gate Driver	5 V, 7 A source, 5 A sink	LMG1025
Dig. Isolator	2.5 kV_{rms}, 150 Mbps	IL710
$L_{dm,1}$ & $L_{dm,2}$	4.7 μH, $I_{sat} = 48$ A	SER2915H-472KL
$C_{dm,1}$ & $C_{dm,2}$	4×300 nF	CAA573C0G2J304J640LH
C_{dc}	$N_s = 2,\ N_p = 9$	C5750X6S2W225K250KAF
$C_{fly,decoupling}$	4×10 nF	C1206C103KFRAC7800
C_1	4.7 μF, $N_s = 2,\ N_p = 8$	C2012X5R2A475K125AC
C_2	4.7 μF, $N_s = 3,\ N_p = 18$	C2012X5R2A475K125AC
C_3	2.2 μF, $N_s = 1,\ N_p = 12$	C5750X6S2W225K250KA
C_4	2.2 μF, $N_s = 2,\ N_p = 6$	C5750X6S2W225K250KA
C_5	2.2 μF, $N_s = 2,\ N_p = 6$	C5750X6S2W225K250KA
C_6	2.2 μF, $N_s = 2,\ N_p = 6$	C5750X6S2W225K250KA

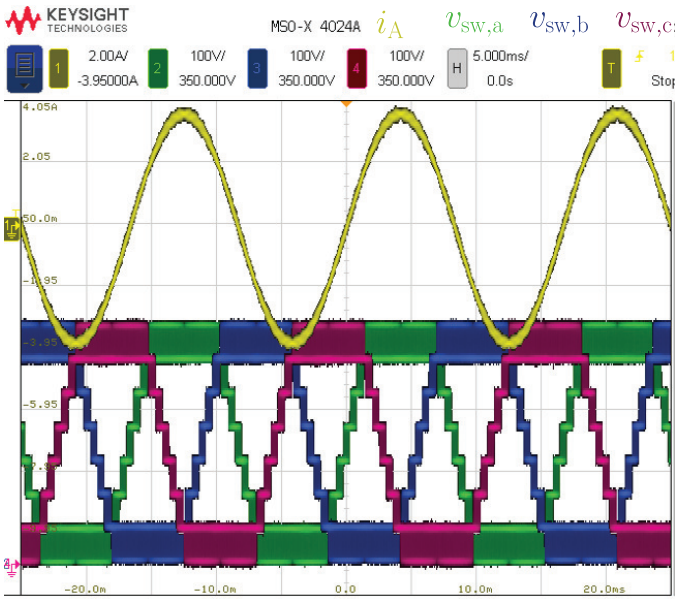
III. Experimental Results

A three-phase eight-level FCML converter prototype was designed and fabricated. Fig. 7 provides annotated photographs of the top and bottom of the hardware prototype. Relevant component parameters are provided in Table I. N_s denotes the number of capacitors connected in series and N_p the number connected in parallel. To create the dense flying capacitor array, series combinations of 100 V MLCC capacitors were used for capacitors C_1 and C_3 while series combinations of 450 V capacitors were used for C_3 through C_6 and C_{dc}. Each switch pair is operated at a switching frequency of $f_{sw} = 120$ kHz. Space vector modulation [17] was implemented via adding an offset to all three duty cycles [14].

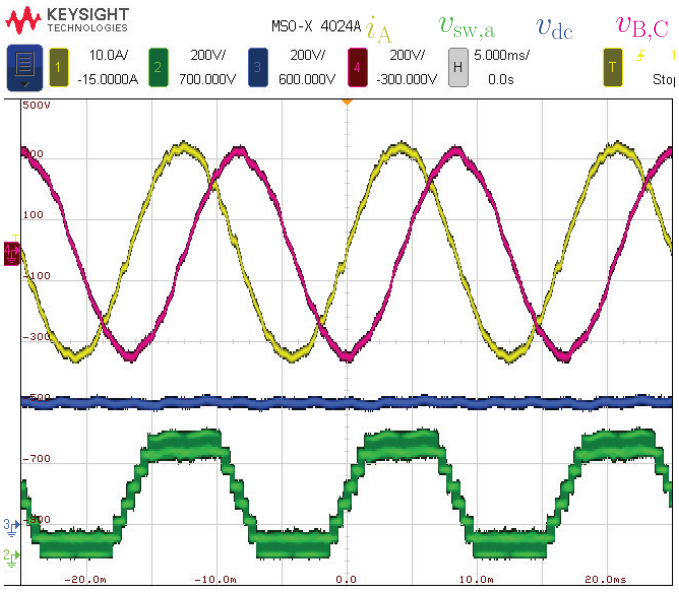
Gate drive power was generated with a cascaded bootstrap network [27] with a bootstrap supply voltage of 15 V. Given a minimum duty cycle of 5% and a gate charge of $Q_g = 25$ nC [28], the diode forward current is $I_F = Q_g/(DT_{sw}) = 60$ mA, assuming the cascaded bootstrap switched-capacitor network operates in the slow switching limit. At this forward current, the utilized Schottky diodes exhibit an approximate 0.7 V drop. The total voltage drop of the chain of diodes in the cascaded bootstrap scheme resulted in $13 \cdot 0.7\,\text{V} = 9.1\,\text{V}$ of total diode drops. Each gate drive IC is fed through an LDO that obtains its power from the corresponding bootstrap capacitor. Allotting 500 mV of headroom to the LDO at the end of the cascaded bootstrap chain results in a 14.6 V minimum gate drive voltage. Digital isolators were used to provide source-referenced signals to the gate drivers.

A TI C2000 F28379D DSP samples the grid voltages, inductor currents, and dc bus voltage, then computes the desired duty cycles according to the control law described in Fig. 6. The DSP commands an Altera 10M50DA FPGA over a SPI communication link to generate the 42 PWM signals. The power stage volume is 0.415 dm^3 resulting in a power stage power density of 60.24 kW/dm^3 for the design output power of $P_{out} = 25$ kW.

The prototype was tested as an inverter up to a dc voltage of 700 V and an ac line-to-line voltage of 415.2 V_{rms}. The inverter was connected to a three-phase wye-connected resistive load. The converter was operated up to an output power of $P_{out} = 5.06$ kW achieving a conversion efficiency of $\eta = 98.5\%$ as measured by a Yokogawa WT3000 power analyzer. Converter waveforms while operating as an inverter are provided in Fig. 8(a), showcasing the smooth sinusoidal output current with low THD. Moreover, the discrete and evenly spaced switching waveforms for the three phases indicates excellent flying capacitor voltage balancing. Fig. 8(b) illustrates operation as a PFC rectifier connected to a 238 V_{vrms} line-to-line grid. The ac voltage was provided by a three-phase



(a)



(b)

Fig. 8: (a) Measured phase A current and switch node voltages when operated as an inverter with $V_{dc} = 387$ V. The symmetry apparent in the switch node voltages indicates that the flying capacitor voltages are at their balanced values. (b) Operation as a PFC rectifier with $V_{dc} = 393.5$ V and $I_{dc} = 12$ A for an output power of $P_{dc} = 4.73$ kW and an efficiency of $\eta = 98.75\%$. The current THD is 2.86%.

variable transformer connected in series with a three-phase, wye-to-wye transformer. The converter powered a constant current electronic load with $I_{\mathrm{dc}} = 12\,\mathrm{A}$ for an output power of $4.75\,\mathrm{kW}$. At this operating point, the converter efficiency was 98.75% and the current THD was 2.86% over a frequency range from dc to $3\,\mathrm{kHz}$. The gate drive power loss was $2.65\,\mathrm{W}$, reducing the conversion efficiency including gate drive loss to 98.73%. Equipment limitations prevented evaluation of the hardware prototype at the nominal full power rating.

IV. Conclusion

Innovations in data center computation and cooling are enabling significant increases in data center rack power consumption. To maintain high efficiency rack power delivery, architectures will require high rack voltages and high-performance three-phase rectifiers. This work detailed the design and implementation of a three-phase, eight-level FCML rectifier to achieve high performance ac/dc conversion. The FCML converter's utilization of low voltage semiconductors and capacitive energy storage enables efficient and power dense rectifiers. This work detailed the EMI filter design, converter modulation, and gate drive power delivery to achieve practical high level count FCML rectifiers, showcasing high efficiency (98.73%) at an output power of $4.75\,\mathrm{kW}$ while achieving power factor correction with a current THD of 2.86%. A hardware prototype was constructed to validate the proposed converter.

Acknowledgment

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References

[1] "AI data center growth: Meeting the demand | McKinsey." [Online]. Available: https://www.mckinsey.com/industries/technology-media-and-telecommunications/our-insights/ai-power-expanding-data-center-capacity-to-meet-growing-demand/

[2] Y. Zhu, J. Zou, and R. C. N. Pilawa-Podgurski, "A 1500-A/48-V-to-1-V Switching Bus Converter for Next-Generation Ultra-High-Power Processors," *IEEE Transactions on Power Electronics*, vol. 39, no. 9, pp. 11 340–11 355, Sep. 2024.

[3] Continuum Labs, "NVIDIA GB200 NVL72." [Online]. Available: https://training.continuumlabs.ai/infrastructure/servers-and-chips/nvidia-gb200-nvl72

[4] Microsoft, Meta, Google, "Diablo 400 Project: Rack and Power," May 2025. [Online]. Available: https://www.opencompute.org/documents/ocp-specification-diablo-400-v0p5p2-2025-05-30-pdf

[5] J. Huntington and M. Tu, "800 VDC Architecture for Next-Generation AI Infrastructure," 2025. [Online]. Available: https://developer.nvidia.com/blog/building-the-800-vdc-ecosystem-for-efficient-scalable-ai-factories/

[6] Hamid Keyhani, Ted Tang, Dmitriy Shapiro, John Fernandes, Ben Kim, Tiffany Jin, and Rommel Mercado, "Open Rack V3 48V PSU Specification," Nov. 2022.

[7] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative Evaluation of MVAC-LVDC SST and Hybrid Transformer Concepts for Future Datacenters," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, May 2022, pp. 2027–2034.

[8] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, Jun. 1992, pp. 397–403 vol.1.

[9] J. Azurza Anderson, G. Zulauf, P. Papamanolis, S. Hobi, S. Mirić, and J. W. Kolar, "Three Levels Are Not Enough: Scaling Laws for Multilevel Converters in AC/DC Applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 3967–3986, Apr. 2021.

[10] N. Pallo, S. Coday, J. Schaadt, P. Assem, and R. C. N. Pilawa-Podgurski, "A 10-Level Flying Capacitor Multi-Level Dual-Interleaved Power Module for Scalable and Power-Dense Electric Drives," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2020, pp. 893–898.

[11] L. Horowitz and R. C. Pilawa-Podgurski, "A 14-level FCML Inverter for Electric Vehicles with Optimal Capacitors Achieving 175 kW/kg and 380 kW/L Power Density," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2024, pp. 1009–1013.

[12] N. Pallo, R. S. Bayliss, and R. C. N. Pilawa-Podgurski, "A Multi-Phase Segmented Drive Comprising Arrayed Flying Capacitor Multi-Level Modules," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Jun. 2021, pp. 192–199.

[13] R. S. Bayliss, R. K. Iyer, R. Liou, and R. C. Pilawa-Podgurski, "A Segmented Electric Aircraft Drivetrain Employing 10-Level Flying Capacitor Multi-Level Dual- Interleaved Power Modules," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2023, pp. 225–230.

[14] S.-H. Kim, *Electric Motor Control: DC, AC and BLDC Motors*, 1st ed. Amsterdam, Netherlands: Elsevier, 2017.

[15] A. M. Y. M. Ghias, J. Pou, G. J. Capella, P. Acuna, and V. G. Agelidis, "On Improving Phase-Shifted PWM for Flying Capacitor Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5384–5388, Aug. 2016.

[16] Y.-L. Syu, Z. Liao, P. Assem, D. Chou, and R. C. N. Pilawa-Podgurski, "Phase-Shifted PWM with Dynamic Phase Shift Control and Zero Sequence Injection to Minimize Inductor Current Ripple in Three-Phase Flying Capacitor Multilevel Converters," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*. Aalborg, Denmark: IEEE, Nov. 2020, pp. 1–7.

[17] H. W. v. d. Broeck, H. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988.

[18] R. Hartwig, A. Hensler, T. Ellinger, S. Ag, and T. Ilmenau, "EMI Filter for a Three-Phase 800 kHz Nine-Level Flying Capacitor GaN Multilevel Inverter," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Sep. 2021, pp. P.1–P.10.

[19] M. L. Heldwein, "EMC Filtering of Three-Phase PWM Converters," Doctoral Thesis, ETH Zurich, Zürich, 2008.

[20] M. L. Heldwein and J. W. Kolar, "Design Of Minimum Volume Emc Input Filters For An Ultra Compact Three-phase Pwm Rectifier," *Eletrônica de Potência*, vol. 14, no. 2, pp. 85–96, May 2009.

[21] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for high switching frequency three-phase/level PWM rectifier systems," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, USA, Feb. 2010, pp. 986–993.

[22] A. Gorgerino, "Hard Switching Losses Calculations," Efficient Power Conversion, Tech. Rep., 2024.

[23] R. Teodorescu, M. Liserre, and P. Rodríguez, "Grid Synchronization in Three-Phase Power Converters," in *Grid converters for photovoltaic and wind power systems*. Piscataway, New Jersey: IEEE, 2011, pp. 169–204.

[24] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 58–63, Jan. 1997.

[25] S.-H. Han, T.-H. Jo, J.-H. Park, H.-G. Kim, T.-W. Chun, and E.-C. Nho, "Dead time compensation for grid-connected PWM inverter," in *8th International Conference on Power Electronics - ECCE Asia*, Jeju, Korea (South), May 2011, pp. 876–881.

[26] J. H. Cattell, "Adaptive feedforward cancellation viewed from an oscillator amplitude control perspective," Thesis, Massachusetts Institute of Technology, 2003. [Online]. Available: https://dspace.mit.edu/handle/1721.1/28280

[27] C. Klumpner and N. Shattock, "A Cost-Effective Solution to Power the Gate Drivers of Multilevel Inverters using the Bootstrap Power Supply Technique," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Feb. 2009, pp. 1773–1779.

[28] "EPC2304 Datasheet," 2025. [Online]. Available: https://epc-co.com/epc/portals/0/epc/documents/datasheets/EPC2304_datasheet.pdf