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High Frequency Multiphase Clock Generation Using Multipath Oscillators and Applications

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High Frequency Multiphase Clock Generation Using Multipath Oscillators and Applications

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy in Electrical Engineering

By

Amr Amin Abou-El-Sonoun

2012

ABSTRACT OF THE DISSERTATION

High Frequency Multiphase Clock Generation Using

Multipath Oscillators and Applications

by

Amr Amin Abou-El-Sonoun

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2012

Professor Chih-Kong Ken Yang, Chair

Oscillators and frequency dividers are core building blocks in communications systems and processors used to provide proper synchronization for the flow of information. Different variations of the conventional ring oscillator that involve coupling of different oscillator-stages or different oscillators have been introduced to provide multiple-phases without penalizing the oscillation frequency. These variations, known as multipath ring oscillators, enable system designers to relax the performance-power trade-off through parallelism. These oscillator

structures, however, introduce additional degrees of freedom and expand the design space considerably which makes the process of designing them optimally a very difficult task.

This dissertation introduces an accurate analytical model and comprehensive analysis for multipath ring oscillators and frequency dividers. The results of the analysis are incorporated into an optimization algorithm that allows a designer to arrive at the desired optimal design at a very short time. The analysis explains the factors that affect the different performance metrics including the number of phases, oscillation frequency, phase noise, and oscillation-mode stability.

As an example application, a 48 Gb/s serializing transmitter is designed in 65nm CMOS technology using superharmonic injection-locked multipath ring oscillators to generate multiphase sampling clock signals for the various stages of the serializer. The ability to generate multiple clock phases at relatively high frequencies and low power cost allows significant power and area savings in the overall Transmitter.

The dissertation of Amr Amin Abou-El-Sonoun is approved.

Milos Ercegovac

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2012

To my parents

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PUBLICATIONS

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Amr A. Hafez, C.-K. Ken Yang, "Analysis and Design of Superharmonic Injection-Locked Multipath Ring Oscillators," Submitted to *IEEE Trans. Circuits and Systems—I: Regular Papers*.

Amr A. Hafez, C.-K. Ken Yang, "Design and Optimization of Multipath Ring Oscillators," *IEEE Trans. Circuits and Systems—I: Regular Papers*, vol. 58, no. 10, Oct. 2011, pp. 2332-2345.

David Murphy, Amr A. Hafez, Ahmad Mirzaei, Mohyee Mikhemar, Hooman Darabi, M.-C. Frank Chang, Asad Abidi, "A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure," *ISSCC*, Feb. 2012, pp. 74-75.

Tamer A. Ali, Amr A. Hafez, Robert Drost, Ronald Ho, C.-K. Ken Yang, "A 4.6GHz MDLL with -46dBc Reference Spur and Aperture Position Tuning," *ISSCC*, Feb. 2011, pp. 466-467.

CHAPTER 1

Introduction

Oscillators and frequency dividers are core building blocks in communication systems and processors to provide proper synchronization of the flow of information.

A multiphase clock generator is a core building block in many applications that allows a system designer to relax the performance-power trade-off by exploiting parallelism [1]. Numerous examples of applications that use multiphase clock generators exist. Some are discussed in Section 1.1. In such applications, the benefit of parallelism is largely based on the assumption that multiphase generation can be achieved efficiently and with low overhead.

A common approach to generating multiphase clocks is to use either ring oscillators or frequency divided outputs of an *LC* oscillator with high quality factor and low phase noise. Complex structures known as multipath oscillators that involve coupling of multiple oscillators and oscillator stages have been introduced in order to improve oscillator performance. These structures, however, introduce additional degrees of freedom and expand the design space considerably.

This dissertation introduces an analytical model and comprehensive analysis for multipath ring oscillators and frequency dividers to aid designers in arriving at a near optimal design. Section 1.2 of this chapter motivates this analysis by describing the design complexity of this type of oscillators and dividers. The organization of the dissertation is then presented in Section 1.3.

1.1. Examples of Multiphase Clocking Applications

Any application that involves the interleaving of multiple paths requires multiple clock phases. Common examples include interleaved data-converters and sub-rate clock and data recovery systems. Fig. 1 shows an example where a 4-way interleaved analog-to-digital converter is used to achieve a sampling rate 4 times higher than that of a single unit converter.

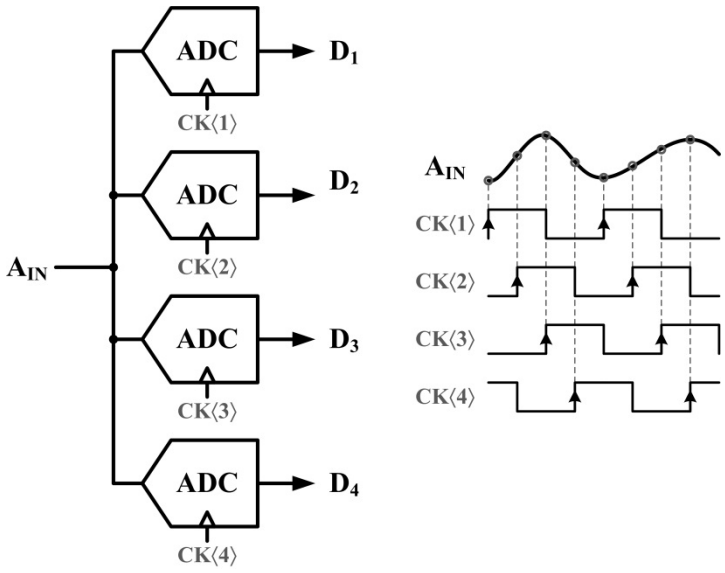


Fig. 1.1. A four-way interleaved analog-to-digital converter.

Another important application where a multiphase clock is needed is software-defined radios. These radios are expected to operate in different frequency-bands making it very expensive to achieve band selection using off-chip filters. To prevent signals from out of the desired band from interfering with the desired signal, a receiver has to use multiple signal paths driven by different phases of the local oscillator to achieve harmonic rejection [2-3].

In an application such as high-speed serial link transceivers, not only multiple phases but multiple divided clock frequencies are usually needed to perform data serialization and deserialization. These clock signals are typically generated using a chain of frequency-dividers

that is driven by the output of a high-frequency oscillator [5-9]. For serial links operating at tens of Gb/s, these dividers consume a considerable amount of power to meet the target operation frequencies over all process corners. In many cases, bandwidth extension techniques using expensive passive inductors must also be used to meet the target speeds. This dissertation uses a 48 Gb/s serial link transmitter as a design example to illustrate the area and power benefits of using injection-locked multipath oscillators to frequency divide and generate multiphase clocks.

1.2. Motivation

To generate a multiphase clock, a ring oscillator can be used in a phase-locked loop as shown in Fig. 1.2(a). A conventional inverter-based ring oscillator, as shown in Fig. 1.3, consists of a single loop of an odd number of inverters. While compact, easy to design, and tunable over a wide frequency range, this oscillator suffers from several limitations. For example, it is not possible to increase the number of phases while maintaining the same oscillation frequency since the frequency is inversely proportional to the number of inverters in the loop. In other words, the time resolution of the oscillator is limited to one inverter delay and cannot be improved below this limit. In addition, the number of phases that can be obtained from this oscillator is limited to odd values. Otherwise, if an even number of inverters is used, the circuit remains in a latched state and does not oscillate.

To overcome the limitations of conventional ring oscillators, several variations have been proposed. These variations all share the property that instead of having each phase in the oscillator driven by a single inverter, or a single *path*, each phase can be driven by two or more inverters, or multi-*paths*. Each of these paths is driven by a different phase in the oscillator [10-

19]. These variations are collectively known as *multipath* ring oscillators or MPROs as opposed to the conventional *single-path* ring oscillators, SPROs.

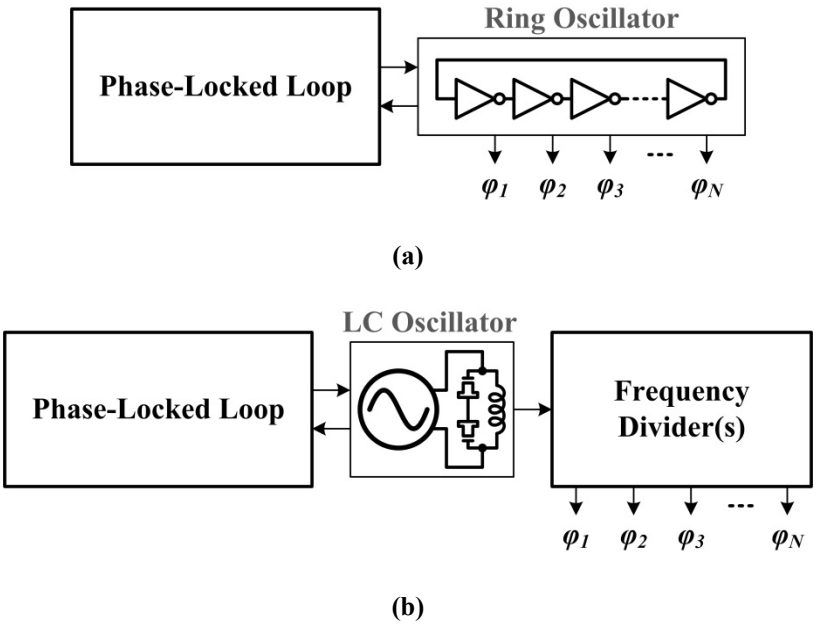


Fig. 1.2. Multiphase generation: (a) Using a multiphase ring oscillator. (b) Using an *LC* oscillator and a multiphase frequency-divider.

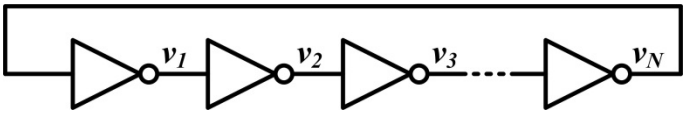


Fig. 1.3. A conventional *N*-phase inverter-based ring oscillator.

In MPROs, the selection of which phase to use to drive each path and the relative sizing of these different paths add additional degrees of freedom to the design of the oscillator. These degrees of freedom, if properly used, can allow a designer to overcome the limitations of conventional SPROs. However, these degrees of freedom also expand the design space of the oscillator considerably making its design a more difficult task.

Previous MPRO analyses have been either limited to a qualitative argument or otherwise restricted to certain special cases. Since the number of possible coupling structures is very large

and it keeps increasing as the number of output phases increases, the existing analysis does not allow a designer to explore the whole design space and find the optimum design. Accordingly, a new analytical framework that explains the operation of these oscillators is needed if the full potential of such structures is to be utilized.

One thing that makes the MPRO design problem even more complicated is its property of having multiple possible oscillation modes. Without a clear understanding of what makes one of these modes dominant, it is very likely that a designer might end-up having an oscillator that can start-up each time in a different oscillation mode depending on the initial state of the oscillator. This is of course unacceptable in any practical application. This problem, which is characteristic of multipath oscillators, is one that has been almost totally overlooked in all previous publications.

In this dissertation, we introduce an accurate analytical model and a comprehensive analysis for multipath ring oscillators. We explain the effect of the oscillator coupling structure on the different performance metrics including the number of phases, oscillation frequency, phase noise, and oscillation-mode stability. We use the presented model to formulate an optimization algorithm that allows a designer to find the optimum coupling structure of an MPRO, needed to achieve certain design goals, in a very short time.

While ring oscillators are very compact and can be tuned over a wide frequency range, they are typically suitable for applications that require relatively less stringent phase noise specifications as compared to high-quality factor oscillators such as *LC* oscillators. For applications like RF and high-speed serial-link transceivers, better phase-noise performance than can be provided by ring oscillators is needed. Accordingly, *LC* oscillators are typically used. To

generate multiple phases, it is possible in principle to use a multiphase *LC* oscillator. However, due to the high cost of high-Q on-chip passive inductors in terms of chip area, it is very rare to generate more than 4 phases using a multiphase *LC* oscillator. Alternatively, a multiphase clock with high spectral purity can be generated from an *LC* oscillator using frequency-dividers as shown in Fig. 1.2(b). This method has been shown to have less jitter as compared to other approaches such as delay-locked loops [4] for the same power budget.

Frequency division at very high frequencies can be achieved efficiently at using injection-locking [20-29]. While injection-locked *LC* oscillators can operate at higher frequencies than ring oscillators, they suffer a narrow locking-range due to their high quality factor. This makes them sensitive to process, supply-voltage, and temperature (PVT) variations. In addition, injection-locked *LC* oscillators are not suitable for multiphase generation due to the need for multiple inductors which would cost a lot of area.

Injection-locked ring oscillators, on the other, hand have wider locking-ranges but they operate at lower frequencies. Similar to a ring oscillator, a conventional injection-locked ring oscillator has a maximum locking frequency that decreases with the number of phases at its output. This means that same trade-off between phase resolution, operation frequency, and power consumption still exists in frequency dividers realized as injection-locked ring oscillators.

In this work, we show that conventional latch-based dividers can be analyzed as superharmonic injection locked ring oscillators. Accordingly, the performance of these dividers can be extended in the same way the performance of a ring oscillator can. We propose, for the first time, the use of superharmonic injection-locked multipath ring oscillators (SHIL-MPROs) to achieve frequency division at higher frequencies for the same number of output phases. The

theory we propose explains the different factors that limit the locking range of a SHIL-MPRO and how it can be maximized for a certain number of output phases by choosing the optimum coupling structure of the core MPRO and the input clocking configuration.

1.3. Thesis Organization

The dissertation consists of seven chapters. Chapter 2 gives the necessary background on oscillators, MPROs, frequency dividers, and serializing transmitters. It begins with a brief discussion for the important performance metrics of an oscillator followed with a review for the different forms of MPROs that have been proposed in the literature before. The chapter then reviews the different categories of multiphase frequency dividers. Finally, it gives a quick overview of high-speed serial link transmitters and the factors that limit their operation range.

In Chapter 3, we present our analysis for MPROs. We derive accurate expressions for the oscillation frequency and phase noise. We show that for the same power consumption, if the oscillator is designed correctly, the number of phases can be increased without decreasing the oscillation frequency or degrading the phase noise. We also explain how the oscillator should be designed to oscillate at the desired oscillation mode independent on the initial conditions.

The analysis for MPROs is extended to dividers in Chapter 4. Theoretically, the maximum division frequency of a frequency divider can be decoupled from the number of phases at its output when multipath coupling is used. We derive accurate expressions for the locking range and use them to find the optimum structure to maximize the division frequency. The results of the model are incorporated into a design procedure that can rapidly explore various coupling and sizing of the multipath structure.

We explain the details of the serializer design in Chapter 5 and discuss the measurement results in Chapter 6. Finally, conclusions and future work are discussed in Chapter 7.

CHAPTER 2

Background

This chapter begins with a quick review of some basics of oscillators followed by the evolution of multipath ring oscillators. We then give a brief summary of the different methods to design a multiphase frequency divider. The definitions in this chapter are used in the next two chapters where the analysis is explained in detail. Since a high-speed serial-link transmitter is used an application to demonstrate the design of SHIL-MPROs, the last section in this chapter introduces the components and design challenges of serial link transmitters. We explain the timing constraints that limit its operating range and show how they can be relaxed using high-speed multiphase frequency dividers. We show that if these dividers can be designed at a low power cost, significant savings in power and complexity for the overall transmitter can be achieved.

2.1. Oscillators Basics

An oscillatory system can be defined as an autonomous dynamical system that possesses an asymptotically stable limit cycle in its state space [30]. A more circuit-oriented definition is a circuit that generates one or more periodic waveforms at its output. These waveforms can be characterized by a certain frequency and amplitude and each of them has a certain phase.

If the harmonic content of the oscillator output can be neglected compared to its fundamental frequency component, the oscillator output can ideally be expressed as $v_{out}(t)=A_o\cos(\omega_o t+\Phi_o)$ where A_o is the oscillation amplitude, ω_o is the angular frequency, and Φ_o is a fixed phase angle.

In practice, due to the various sources of noise and interference in a real circuit, both the amplitude and the phase of the oscillator output suffer from small fluctuations around their nominal average values. Accordingly, the oscillator output can be more practically expressed as

$$v_{out}(t) = \left[A_o + a(t)\right]\cos\left[\omega_o t + \Phi_o + \varphi_n(t)\right] \tag{2.1}$$

where $a(t)$ and $\varphi_n(t)$ represent the amplitude and phase fluctuations, respectively.

While small amplitude fluctuations can be tolerated in most practical applications, phase fluctuations, commonly known as phase noise, are usually problematic. Fig. 2.1 shows the effect of phase noise on the output of the oscillator in both the frequency and time domains. In the frequency domain, random phase noise causes the output spectrum to broaden in shape compared to the ideal impulse-shaped spectrum of a noiseless oscillator. In applications like RF transceivers, this broadening is highly undesirable since it causes signal interference. In the time domain, phase noise causes the zero-crossing instants of the oscillator output to deviate from their ideal positions at integer multiples of the nominal oscillation-period. These deviations, known as timing jitter, are highly undesirable in applications like high-speed digital circuits and serial link transceivers since they reduce the timing margin where the system operates correctly.

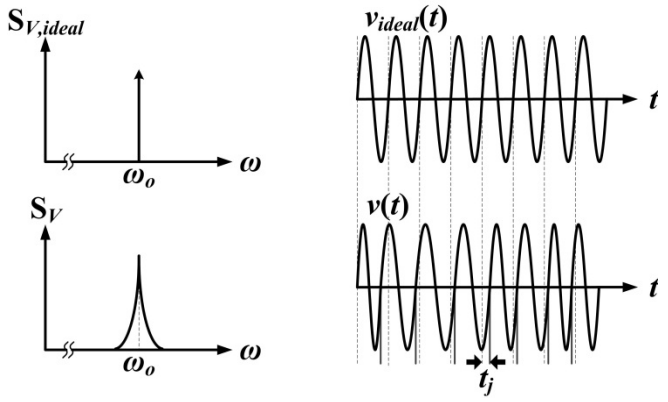


Fig. 2.1. Spectral broadening and timing jitter due to phase noise.

Phase noise of an oscillator is measured in terms of the single-sideband phase noise spectrum $L(\Delta\omega)$. This is defined as the signal power in a 1-Hz bandwidth at a certain frequency offset, $\Delta\omega$, from the nominal carrier frequency, ω_o. The different mechanisms by which device noise is converted into phase noise have been well studied by different researchers before [31-37]. In general, for hundreds of Hz offset frequencies and above, it is fairly accurate to assume that thermal noise causes phase noise $L(\Delta\omega)$ that is proportional to $(1/\Delta\omega)^2$ while flicker noise produces phase noise skirts proportional to $(1/\Delta\omega)^3$. Fig. 2.2 shows a typical single-sideband phase noise spectrum for an electrical oscillator built in CMOS technology.

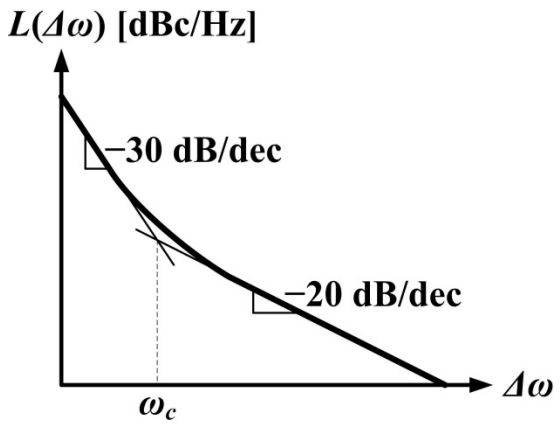


Fig. 2.2. Typical single-sideband phase noise spectrum.

Phase noise caused by random device noise can be reduced in a certain oscillator by scaling the whole design so that it burns more power. Accordingly, if two different oscillator topologies are to be compared in terms of their phase noise performance, the two oscillators must be compared when scaled to burn the same power. In addition, oscillators running at higher frequency are more sensitive to device noise due to their shorter oscillation periods. Accordingly, to compare two different topologies, the oscillation frequency must also be the same for the two oscillators.

To help compare the performance of different kinds of oscillators, a figure of merit (*FOM*) is typically used that factors out the effect of power consumption, oscillation frequency, and offset frequency where the phase noise is measured. This *FOM* , given by (2.2), will be used in the next chapter to compare the performance of different ring oscillators in terms of phase noise.

$$FOM = 10 \times \log\left[\frac{(\omega o/\Delta\omega)^2}{L(\Delta\omega) \times P_{(mW)}}\right] \tag{2.2}$$

2.2. Multipath Ring Oscillators

Fig. 2.3 shows the schematic of a typical 5-stage inverter-based ring oscillator. For this oscillator to operate correctly, the number of inverters in the loop and accordingly the number of phases at the output has to be an odd number. The oscillation frequency of this oscillator is inversely proportional to the number of stages. Accordingly, the time resolution of the oscillator is limited to one inverter-delay.

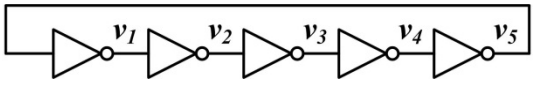


Fig. 2.3. Typical 5-stage inverter-based ring oscillator.

To overcome the limitations of conventional single-path ring oscillators, several forms of multipath ring oscillators have been introduced [10-19]. The simplest of these forms is the dual-path ring oscillator from which three different forms have been proposed.

The first of these forms is the coupled oscillator proposed by Maneatis in 1993 [10]. In this oscillator, the number of phases can be increased, according to Maneatis, without changing the oscillation frequency. This is achieved by coupling a number of rings using a second path as

shown in Fig. 2.4 which causes the phases of the different rings to shift with respect to each other, effectively increasing the phase resolution of the overall oscillator.

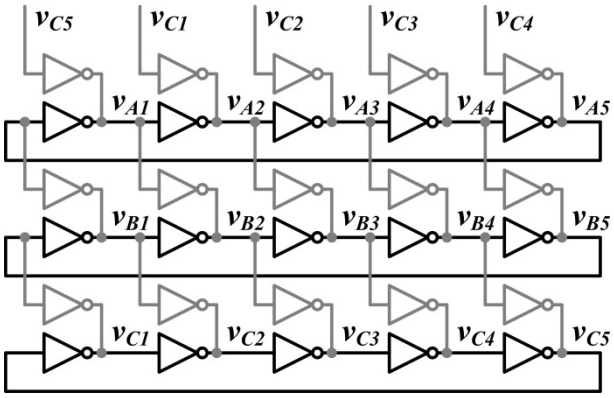


Fig. 2.4. A 3×5 coupled-oscillator.

The second of form of dual-path ring oscillators is the negative-delay-skewed oscillator proposed by Lee in 1997 [11]. In this oscillator, the time resolution is improved by reducing the delay per stage below 1 inverter-delay. This is achieved, as shown in Fig. 2.5, by driving each output with an early signal, or a signal with a negative-delay, to accelerate the transition at the output. The optimum skew has been derived analytically in [12] using a linear model and verified by simulation.

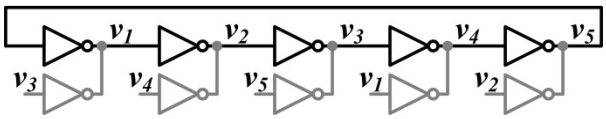


Fig. 2.5. A 5-stage ring-oscillator using negative delay-skewed inverters.

Fig. 2.6 shows the third form of dual-path ring oscillators which uses cross-coupling to achieve differential operation [13]. While the three proposed forms qualitatively seem different, the three of them can be analyzed using one unified theory as will be shown in the next chapter.

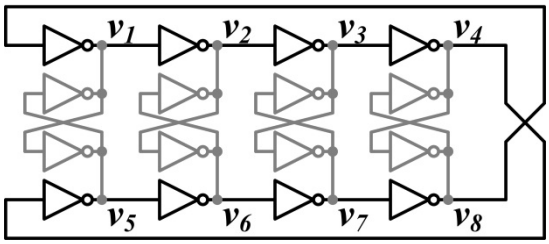


Fig. 2.6. An 8-phase ring oscillator using cross-coupling to achieve differential operation.

The triple-path ring oscillator can be considered the second step in the evolution of multipath ring oscillators. Fig. 2.7 shows an example where both delay-skew and cross-coupling are used to reduce the delay per stage and achieve differential operation, simultaneously [14-16].

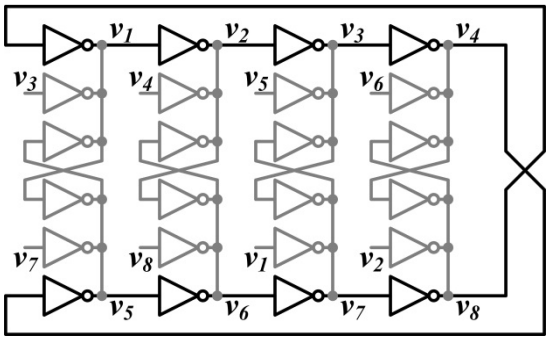


Fig. 2.7. An 8-phase triple-path ring oscillator using cross-coupling to achieve differential operation and negative delay skew to reduce the delay per stage.

In general, we can add more and more paths per stage. As the total number of phases increases, the degrees of freedom increase very rapidly so that it becomes very hard for a designer to find the optimum configuration that meets his design targets just by qualitative analysis. And moreover, it becomes very difficult to verify this configuration just by simulation.

As an extreme case, the oscillator used by Straayer in 2008 to provide a time base for a time-to-digital converter is a 47-stage, penta-path ring oscillator [17]. Of course, it can be imagined how hard it is to come up with the best coupling configuration for such an oscillator using only qualitative analysis and simulation.

In all the above examples, the oscillation frequency of the MPRO does not just depend on the number of stages as in SPROs but rather on the coupling structure of the oscillator as well. In fact, if a designer tries to explore the design space by simulation, he will see that for some coupling structures, as the sizing ratios are varied, the oscillation frequency can experience discrete jumps accompanied by a change in the phase arrangement of the oscillator outputs. In some cases, the oscillator may just stop oscillating at all.

The reason for this phenomenon is that multipath oscillators have different possible modes of oscillation. Each of these modes is characterized by a different frequency, phase shifts, and phase noise versus power tradeoff. Without clear understanding of what determines the dominant mode, it is very possible that a designer will end up having an oscillator where the oscillation mode is only marginally stable; meaning that it depends on the oscillator initial conditions [17]. The problem becomes even more severe as the number of phases in the oscillator increases.

Factors that determine the dominant oscillation mode have been studied in [18][19]. However, the analysis in [18] is constrained to dual-path oscillators while that in [19] is constrained to even number of phases with cross coupling inverters.

In the next chapter, we introduce a general model for multipath ring oscillators with arbitrary coupling structures. We present a general analysis that explains the operation of a generic multipath ring oscillator. We show that all the previously presented designs are special cases of the general case we study. We explain how to design the oscillator for a certain number of phases and maximize its oscillation frequency and phase noise performance while guaranteeing the stability of the desired oscillation mode.

2.3. Multiphase Frequency Dividers

Frequency dividers are important building blocks in clock generators performing frequency multiplication and in low-jitter multiphase generators. The most widely used type of frequency dividers is the latch-based divider. These dividers are composed of latches or flip-flops as unit building blocks. The latches can be of any logic family like CMOS, true single-phase clock (TSPC), or current-mode logic (CML). To optimize the performance of these dividers, the only degree of freedom is optimizing the latch design. In [38] for example, all possible implementations of TSPC latches and flip-flops are explored using an exhaustive search to find the optimum flip-flop implementation. In [39], a modified CML latch circuit is proposed that can operate at speeds up to tens of GHz. This latch is used in [40] to design a 40 GHz divide-by-2 circuit. Inductive peaking can be viewed as a way of optimizing the latch design by partially tuning out its load capacitance using inductors [41].

Regenerative frequency dividers (RFDs), also known as Miller-type dividers [20], and injection-locked frequency dividers (ILFDs) have been used for frequency division at very high frequencies. Although both terms are sometimes used interchangeably [21], the most common convention is that regenerative dividers do not have a self-oscillation frequency in the absence of the input signal. In other words, the self-oscillation frequency of regenerative dividers is equal to zero. On the other hand, injection-locked dividers oscillate at a certain self-oscillation frequency if the input signal is not applied. In [22], the authors show that both types of dividers can be analyzed using the same model.

Both RFDs and ILFDs can be classified based on their core oscillator, injection method, and injection phases. The core oscillator can be either an *LC*-based oscillator [21][23] or a ring-

oscillator [24][27]. *LC*-based oscillators can operate at relatively higher frequencies but they suffer from a narrow locking range which makes them sensitive to PVT variations. In addition, they consume large areas due to the use of inductors. Ring oscillators, on the other hand, have lower frequencies but are more compact and have wider locking ranges reducing their sensitivity to PVT variations.

Signal injection can be achieved by two different methods. One method is by varying the transconductance of the amplifying transistors with the input signal. This is usually achieved by driving the tail bias-current of these transistors with the input and thus is referred to as tail injection [21][27]. Another method is by varying the load impedance, usually achieved by modulating the conductance of a load that is directly connected to the divider output and thus is called direct injection [23][24]. Fig. 2.8 shows an example of each of the 4 types of dividers mentioned.

Dividers can also be classified based on the number of injection phases. Single-phase injection means that only one phase is required at the input [25]. Similarly, the divider is said to have a differential-injection when two opposite phases are used at the input [23][24]. In general, multiphase injection can be used when M phases are used at the input (M=1, 2, 3, …) [26-28].

The idea of multiphase injection for frequency dividers has been introduced in [26]. The authors use a frequency domain model to derive the optimum phase shift between different injected signals to maximize the locking range. The analysis is applied to a 6-phase ring oscillator composed of 3 CML differential buffers and with tail injection at two stages with 120^{o} phase shift. In [27], the authors explain the concept of multiphase injection using a time-domain

model. They apply it on a 4-phase divide-by-2 and a 12-phase divide-by-6 both composed of CML cross-coupled latches and having 4 injection phases.

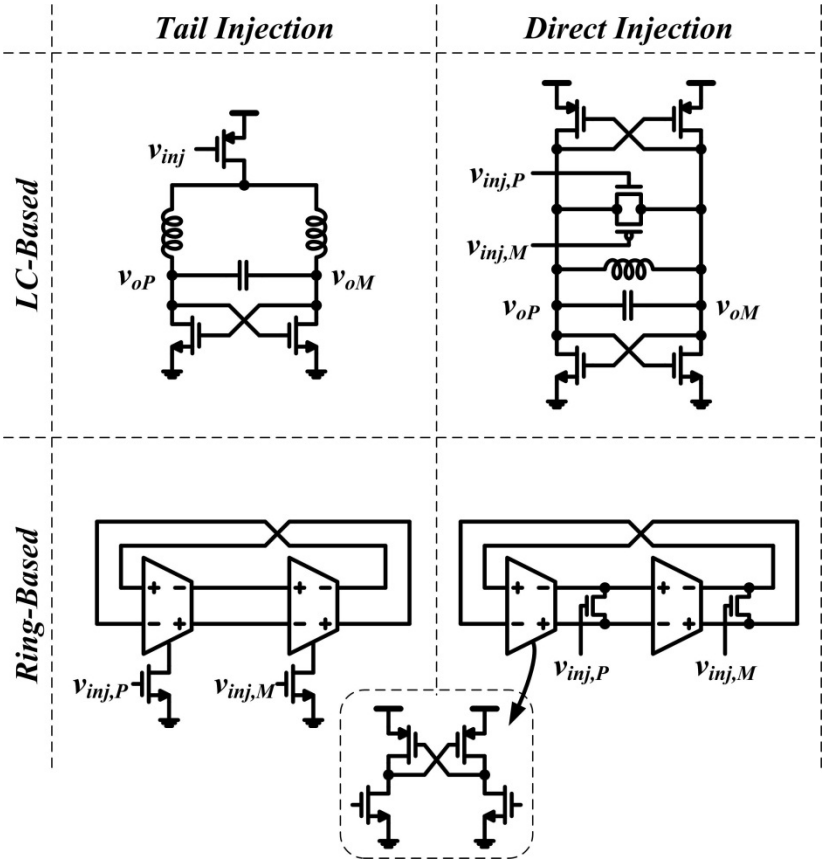


Fig. 2.8. Different types of injection-locked frequency dividers classified based on the core oscillator and the injection method.

The term, superharmonic injection-locked oscillator (SHIL-O), has been used in [29] to describe ILFDs. Superharmonic injection-locking is a phenomenon where an oscillating system can be locked in phase at steady state to a periodic input signal whose frequency is a superharmonic, or an integer multiple, of its own output frequency. In that sense, both RFDs and ILFDs can be considered SHIL-Os. The only difference between them is that RFDs use a core oscillator whose free-running frequency is equal to zero.

We propose in Chapter 4 of this dissertation a general model for superharmonic injection-locked multipath ring oscillators (SHIL-MPROs). The model is valid for both RFDs and ILFDs with either tail-injection or direct-injection and with any number of input injection phases. In our analysis, latch-based dividers are treated as a special case where the injection is large. We show that SHIL-MPROs have different mechanisms that limit the locking range and derive the mathematical expressions needed to optimize the locking range. We also derive a mathematical condition that gives the possible clocking configurations for correct injection phases. With multiple injection phases and multipath sizing factors, the design space of SHIL-MPROs can be very large. A design procedure that uses the model is presented to allow designers to quickly converge on a final design.

2.4. Serial Link Transmitters

A serializing transmitter is used as an application of the SHIL-MPRO design procedure and verification of the analysis. Fig. 2.9 shows a typical block diagram of a serializing transmitter [5-9]. The transmitter consists mainly of a serializer, a driver, and a clock generator. The serializer is a chain of multiplexers that combine a number of low-speed input data channels and produce a single high-speed output data stream to be transmitted over a certain communication channel. The driver converts the binary data into a signal format suitable for the channel. For the serializer to operate properly, clock signals at different frequencies are required to drive the different multiplexing stages. These clock signals are provided by a voltage-controlled oscillator and a chain of dividers that are controlled by a phase-locked loop.

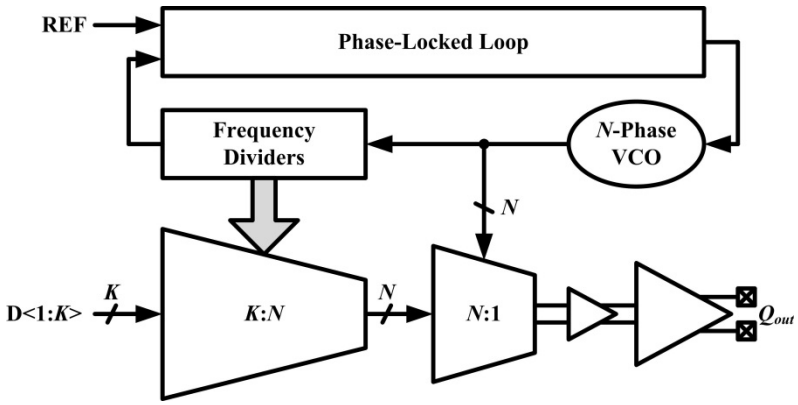


Fig. 2.9. Conceptual block-diagram of a serializing transmitter.

The range of output data rates where the transmitter can operate properly is limited by several factors. These factors include the circuit bandwidths, the oscillator tuning range, the locking range of the frequency dividers, and the timing constraints of the different serializer stages.

For multi-Gb/s transmitters, *LC* oscillators with a combination of coarse and fine tuning capacitors are typically used to generate the required high-speed clock at low phase noise and wide enough tuning range. To meet the speed requirements, designers usually use inductive peaking to extend the circuits bandwidths at the cost of the large area consumed by the inductors [42-44]. This bandwidth extension is usually applied to the final multiplexing stages in the data path and to the dividers in the clock network.

To explain how the timing constraints of a certain multiplexing stage can limit the operation range of the transmitter, Fig. 2.10(a) shows an *N*-to-1 multiplexer driven by an *N*-phase input clock signal of frequency f_o/N where f_o is the bit rate at the multiplexer output. This clock signal also samples, and if necessary, retimes, the *N* outputs of the preceding stage. Fig. 2.10(b) is a timing diagram that describes the operation. The signal D<1> is an output of the preceding multiplexer. Transitions in D<1> occur after a delay $t_{(C\text{-}Q)MUX}$ from the edge of the divided clock

signal CK_{DIV}<1>. This divided clock signal in turn has transitions that are delayed by t_{div} from the edge of the input clock signal CK_{in}<1>. The signal D<1> is sampled by CK_{in}<*i*> which is phase-shifted from CK_{in}<1> by $(2\pi)\times\theta$. In Fig. 2.10(a), θ can only take discrete values that are multiples of $1/N$. In general, if a buffering stage or variable delay is used between the input clock and the N-to-1 MUX, θ can be any positive real number. Depending on the number of phases at the output of the divider and the number of latches used in the retiming flip-flop, the same data phase can be sampled by more than one input clock phase. We assume the phase difference between the first and last clock edges sampling the same data phase is equal to $(2\pi)\times\varphi$.

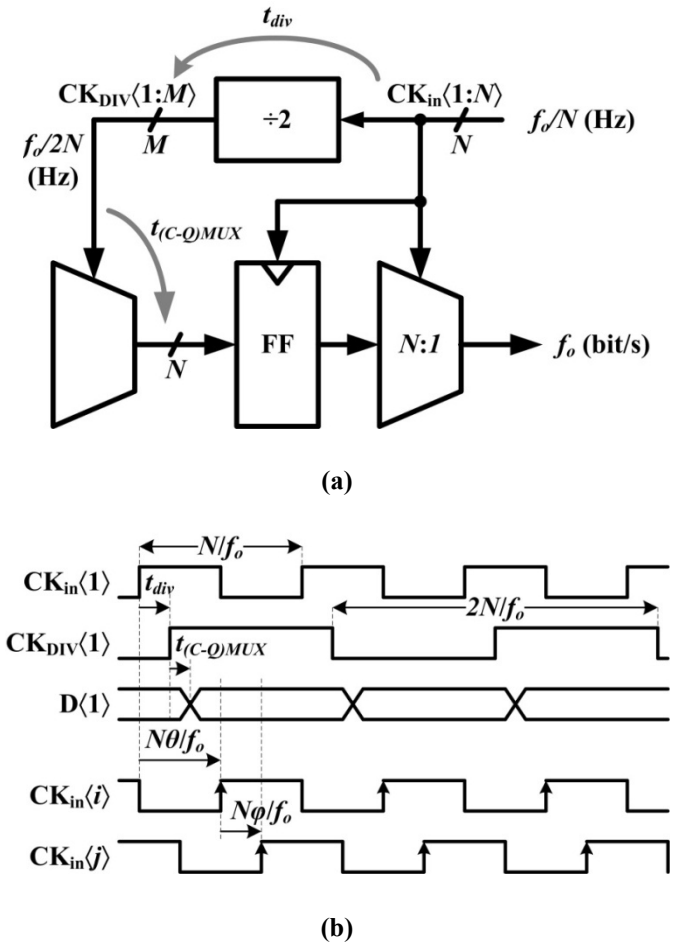


Fig. 2.10. Timing requirements in an *N*-to-1 multiplexer: (a) Block diagram. (b) Timing diagram.

For the setup time condition to be met, the delay between the triggering edge $CK_{in}\langle 1\rangle$ and the first sampling edge $CK_{in}\langle i\rangle$ has to be long enough to allow the data to switch before the edge of $CK_{in}\langle i\rangle$ by at least one setup-time (t_{su}). This delay sets an upper limit on the output bit rate as given by (2.3). On the other hand, for the hold time constraint to be met, the delay between the triggering edge $CK_{in}\langle 1\rangle$ and the last sampling edge $CK_{in}\langle j\rangle$ has to be short enough to allow at least one hold-time (t_h) before the next data transition. Assuming $t_h<t_{(C-Q)MUX}+t_{div}$, the hold time condition sets a lower limit on the allowed output bit rate as given by (2.4).

$$f_{\max} = \frac{N\theta}{t_{div} + t_{(C-Q)MUX} + t_{su}} \tag{2.3}$$

$$f_{\min} = \frac{N(\theta + \varphi - 1)}{t_{div} + t_{(C-Q)MUX} - t_h} \tag{2.4}$$

Fig. 2.11 shows the effect varying the phase shift θ and the order of the multiplexer on the valid bit rate window. In the figure, we assume φ=0 which can be achieved by retiming the sampled data before applying it to the multiplexer. As θ increases for a certain multiplexer, the maximum allowed bit rate increases but the overall window of allowed rates becomes narrower. The graph shows that a tradeoff exists between maximizing the output bit rate of the transmitter and its robustness where the narrow window can shift with PVT variations. When the order of the multiplexer (N) increases, this tradeoff between data rate and robustness becomes more relaxed due to the increase in the input clock period.

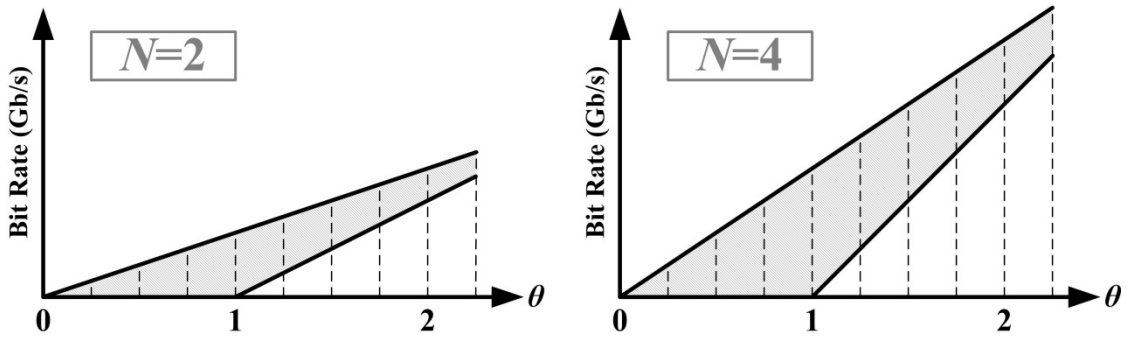


Fig. 2.11. Allowed bit rate window as a function of θ assuming $\varphi = 0$.

One technique for dealing with this delay skew problem is to insert a replica delay buffer between the input clock and the *N*:1 MUX [45]. Ideally, if the buffer delay matches the total delay of the divider and the preceding MUX, the timing conditions can be met independent on the bit rate. However, the replica buffer consumes extra power and occupies an additional area. Besides, it is usually hard to achieve good matching over all PVT corners [8].

Another technique for dealing with the delay skew problem is the insertion of a variable delay or a phase interpolator between the divided clock and the preceding MUX [7-8]. A feedback loop adjusts the value of θ so as to position the valid data rate window around the desired operation data rate. The drawback of this technique is the added design complexity in addition to the power consumption and area overhead. For example, the power overhead in [8] is 72mW which is slightly less than the total power consumption of our whole transmitter in the same 65nm CMOS technology. The area overhead is $0.88mm^2$ which is 73% of our total chip area.

Equations (2.3-2.4) and Fig. 2.11 show that as the order of the multiplexer (*N*) increases, the timing constrains become more relaxed due to the increased bit period at the input. In addition, as more phases are used for the input clock, the phase shift θ can be selected at design time with

a higher resolution allowing the optimum positioning of the nominal bit rate window such that the desired bit rates can fall within this window for all PVT corners.

Since the timing conditions have to be satisfied in every stage in the serializer, it is advantageous if the divided clocks also have multiple phases. This is because this allows more flexibility in setting the maximum and minimum allowed data rates for all stages. In Chapter 5, we show how multiple phases in the divided clock signals can also be useful in reducing the retiming elements to a minimum which leads to significant power and area savings.

CHAPTER 3

Multipath Ring Oscillators

This chapter presents the analysis of multipath ring oscillators. We first explain a general model that can represent any multipath ring oscillator. Then, we derive expressions for the oscillation frequency and amplitude and show how the frequency can be maximized taking mode stability into consideration. After that, we present the phase noise analysis.

3.1. Oscillator Modeling

3.1.1. General Form of the Multipath Ring Oscillator

Fig. 3.1 illustrates the general form of an MPRO. The oscillator consists of N stages where each stage consists of N inverting buffers connected together at their outputs. The input of each buffer is connected to one of the N different nodes of the oscillator to cover all possible coupling paths. The buffers of the main loop are all scaled by a sizing factor h_N with respect to a unit reference buffer of a given size. Buffers that are driven by signals skewed by one stage are sized by a factor h_{N-1}. Similarly, buffers driven by signals skewed by j stages are sized by h_{N-j}.

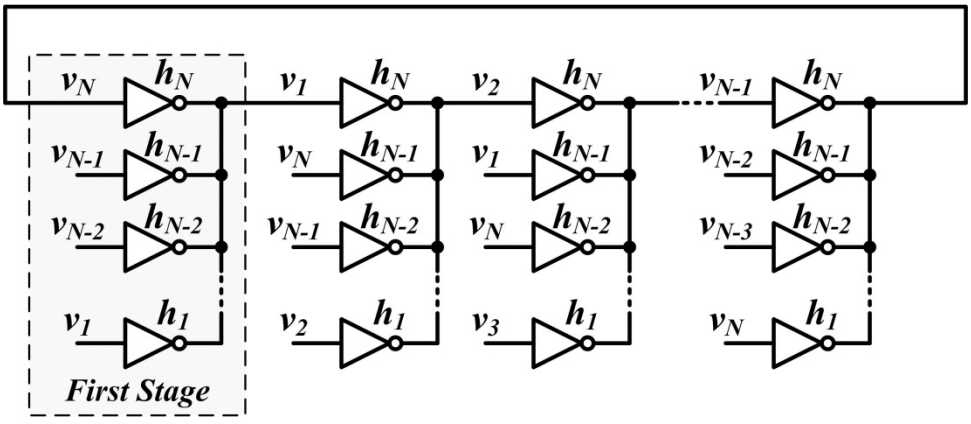


Fig. 3.1. General form of an MPRO having an arbitrary coupling structure.

This general form can be used to model any MPRO by selecting the appropriate values of the sizing factors, h_i. For example, an ordinary SPRO is a special case of the general form where $h_i=0 \ \forall \ i\neq N$. A dual-path ring oscillator has $h_i=0 \ \forall \ i\notin\{N,N-j\}$ where j is the skew of the second input and $0<j<N$. Cross coupling, usually used to achieve differential operation, can be modeled for an even numbered N by $h_{(N/2)+1}\neq 0$. The coupled oscillator [10] can also be treated as a special case. By using a 5×3 coupled oscillator as shown in Fig. 3.2(a) as an example, when numbering the nodes *diagonally* as shown in the figure, the oscillator can be visualized as a 15-stage dual-path oscillator with a skew of 2 as shown in Fig. 3.2(b).

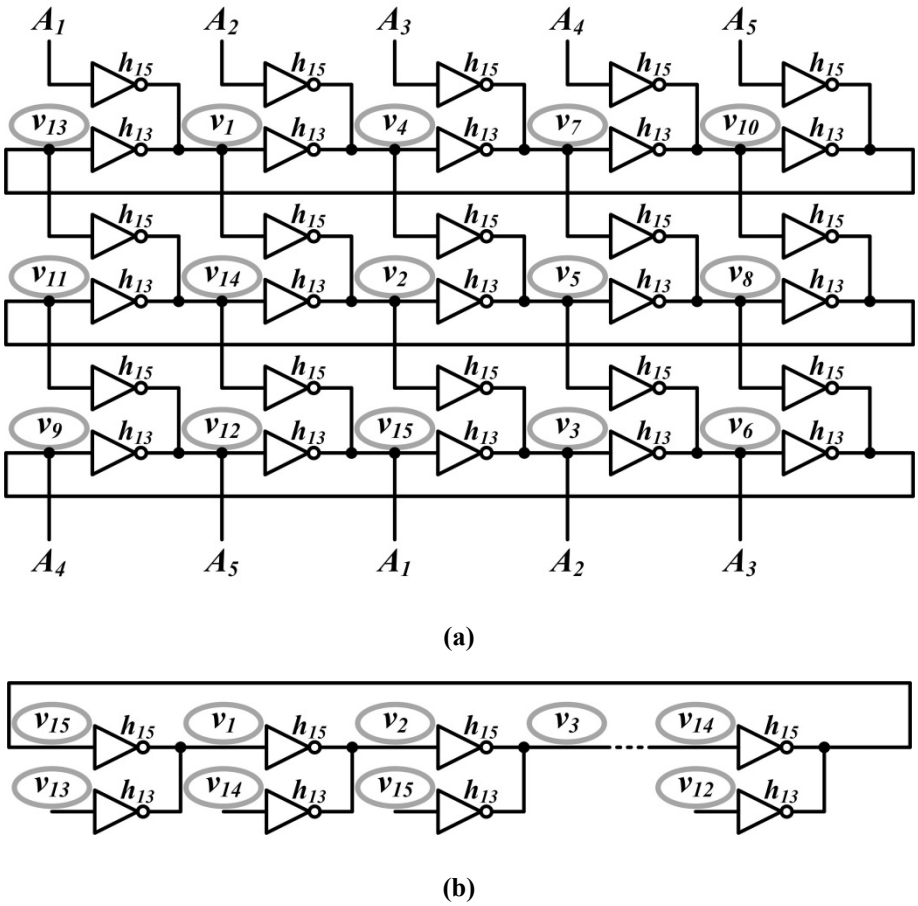


Fig. 3.2. An example using a 5×3 coupled-oscillator: (a) Coupled oscillator with its nodes numbered diagonally. The coupling inverters are scaled by h_{15} while the ring inverters are scaled by h_{13}. (b) Equivalent dual-path ring oscillator with a skew of 2.

Fig. 3.3 shows the circuit schematic of the unit inverter used in all the simulations in this chapter. All simulations are performed using a 65nm CMOS technology with a supply voltage of 1V. Transistors M1 and M4 are used as enable devices where their gates are always driven by V_{DD} for M1 and GND for M4. Transistors M2 and M3 are the main inverter devices. They have dimensions of (4μm/L) for M2 and (8μm/L) for M3 as shown in the figure. In different simulations, L takes values of 60nm, 100nm, 200nm, or 400nm. The driving strength of each inverter is determined by the number of units used which is indicated by h_i in Fig. 3.3. Unless otherwise stated, all the simulation results shown in this chapter are obtained using the periodic steady state (PSS) and the periodic noise (PNoise) simulators in Cadence-SpectreRF.

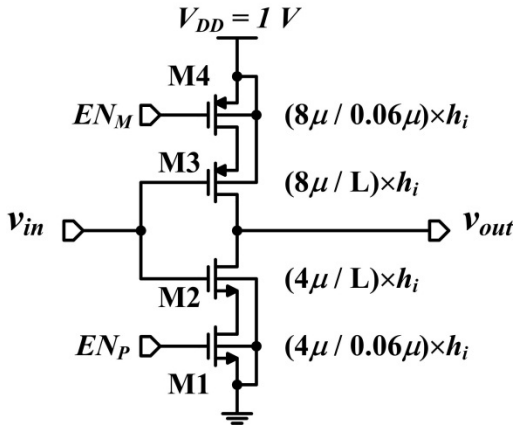


Fig. 3.3. Schematic diagram of the unit inverting buffer.

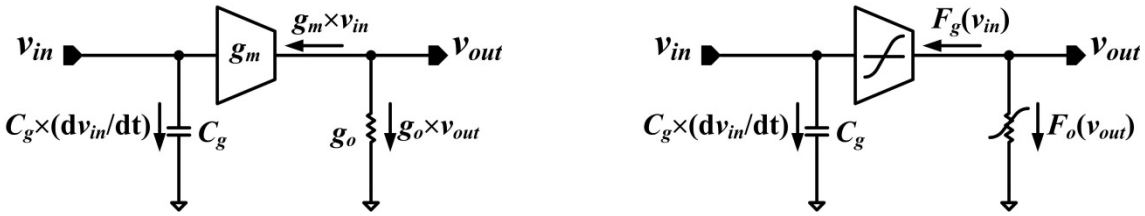
3.1.2. Linear Delay Stage Model

Fig. 3.4(a) shows the inverting buffer modeled as a linear transconductor. The input-output relationship of a single buffer scaled by h_i and driving the input capacitance of a similar buffer can be expressed as

$$h_i g_m v_{in}(t) + h_i g_o v_{out}(t) + h_i C_g \frac{dv_{out}(t)}{dt} = 0$$

$$\Rightarrow a_n v_{in}(t) + v_{out}(t) + \tau \frac{dv_{out}(t)}{dt} = 0 \tag{3.1}$$

where g_m is the transconductance, g_o is the output conductance, C_g is the buffer input capacitance which also acts as the load capacitance for the driving buffer, $a_n=g_m/g_o$ is the linear *dc* gain of the buffer and $\tau=C_g/g_o$ is a time constant. In practice, parasitic capacitance due to routing and any external loading can be absorbed into the capacitance, C_g.



(a) **(b)**

Fig. 3.4. Model of a single unit inverting buffer (a) Linear model (b) Nonlinear model.

A single stage of an MPRO consists of N buffers and is loaded with N buffers of similar sizing factors as shown in Fig. 3.1. Using the linear model, the output voltage of any stage can be expressed in terms of the N input voltages using a linear differential equation. Equation (3.2) expresses v_1, the output of the first stage in Fig. 3.1, in terms of the N inputs of the first stage.

$$\sum_{i=1}^{N} h_i g_m v_i(t) + \sum_{i=1}^{N} h_i g_o v_1(t) + \sum_{i=1}^{N} h_i C_g \frac{dv_1(t)}{dt} = 0 \tag{3.2}$$

Defining the fractional sizing factors and the total sizing factor as $x_i=h_i/H$ and $H = \sum_{i=1}^{N} h_i$, respectively, equation (3.2) can be simplified into (3.3) where $a_n=g_m/g_o$ and $\tau=C_g/g_o$ are the same *dc* gain and time constant defined in (3.1).

$$a_n \sum_{i=1}^{N} x_i v_i(t) + v_1(t) + \tau \frac{dv_1(t)}{dt} = 0 \tag{3.3}$$

3.1.3. Nonlinear Delay Stage Model

To model the nonlinear behavior of the inverter, we assume the transconductance and the output conductance to be nonlinear functions of the input and the output voltages, respectively. This nonlinear model is shown in Fig. 3.4(b). In this model, we assume the inverter input capacitance is linear. The output voltage of a stage can be expressed as a function of the N inputs using a nonlinear differential equation. Equation (3.4) shows the output of the first stage of the general MPRO in Fig. 3.1 as a function of the N inputs. When $F_g(v_i)=g_m v_i$ and $F_o(v_1)=g_o v_1$, this equation reduces to the linear case (3.3).

$$\sum_{i=1}^{N} x_i F_g\left(v_i(t)\right) + F_o\left(v_1(t)\right) + C_g \frac{dv_1(t)}{dt} = 0 \tag{3.4}$$

3.2. Oscillation Frequency and Amplitude

3.2.1. Oscillation Modes

In this section, we first use linear analysis to explain the different oscillation modes that can exist in an MPRO and determine which is dominant. Linear analysis also helps in understanding how we can size the different coupling paths of the MPRO and what limits its maximum oscillation frequency. Next, we use a simplified nonlinear analysis to find an expression for the oscillation amplitude and a more accurate expression for the oscillation frequency.

Due to the symmetry of the system in Fig. 3.1 and in the absence of mismatches, if the MPRO is to oscillate at a certain frequency, ω_n, the phase shift between each two successive nodes and

the amplitude of oscillation at each node in the oscillator will ideally be the same. Therefore, the oscillation waveform at the i^{th} node can be expressed as

$$v_i(t) = V_o \cos(\omega_n t - \Delta\varphi \times i) \tag{3.5}$$

where ω_n is the oscillation frequency and $\Delta\varphi = 2\pi n/N$ since the total phase shift around the loop should be multiples of 2π, N is the number of stages in the oscillator, and n can take values between 0 and N-1 representing the different possible modes of oscillation.

Using (3.5), equation (3.3) can be written as

$$a_n \sum_{i=1}^{N} x_i \cos\left(\omega_n t - \frac{2\pi n}{N} i\right) + \cos\left(\omega_n t - \frac{2\pi n}{N}\right) - \omega_n \tau \sin\left(\omega_n t - \frac{2\pi n}{N}\right) = 0 \tag{3.6}$$

By equating the $\cos(\omega_n t)$ and the $\sin(\omega_n t)$ terms of (3.6), we get expressions for the oscillation frequency of the n^{th} mode (3.7) and the minimum *dc* gain required for this mode to exist (3.8). We refer to this gain as the *mode gain*.

$$\omega_n \tau = \frac{\sum_{i=1}^{N} x_i \times \sin\left(\frac{2\pi n}{N}(i-1)\right)}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)} \tag{3.7}$$

$$a_n = \frac{1}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)} \tag{3.8}$$

In practice, the oscillator starts first from a linear mode of operation where all the buffers are indeed acting as linear transconductors. All oscillation modes that have mode gains, a_n, lower than the actual *dc* gain of the inverter, a_o, start to grow. As the oscillation amplitude grows, the effective gain of the inverter drops due to nonlinearity. Consequently, modes with higher mode

gain die out and only the mode that requires the minimum gain continues to oscillate and hence is the dominant mode. Therefore, for an MPRO with N stages, once we choose a certain value for the relative sizing vector $\overline{x}=[x_1\ x_2\ x_3\ \ldots\ x_N]^T \in \Re^N$, the index, n^*, of the dominant mode is given by (3.9). Note that this definition for the dominant mode is dependent only on the relative sizing vector, $\overline{x}$, of the MPRO and is valid for any buffer design used to build the actual oscillator.

$$n^* = \arg\min_{n=1,2,\ldots,N}\left[\frac{1}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)} \geq 0\right] = \arg\max_{n=1,2,\ldots,N}\left[-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)\right] \tag{3.9}$$

3.2.2. Oscillation Amplitude and Nonlinear Time Constant

The nonlinear nature of the buffer elements in the MPRO affects the oscillator in two ways. First, the nonlinearity determines the oscillation amplitude. Second, it can change the oscillation frequency since the effective output conductance is often dependent on the oscillation amplitude.

Equation (3.7) predicts the oscillation frequency normalized to a certain time constant. Depending on the unit inverting buffer used to implement the MPRO, this time constant may not be actually, constant. To explore the dependence of the time constant, τ, and the oscillation amplitude ,V_o, on the sizing vector, $\overline{x}$, we simplify equation (3.4) by solving it using a single tone harmonic balance (3.10). This assumption is later verified to be a good approximation when comparing the equations with simulation results.

$$I_g(V_o)\sum_{i=1}^{N} x_i \cos\left(\omega_n t - \frac{2\pi n}{N} i\right) + I_o(V_o)\cos\left(\omega_n t - \frac{2\pi n}{N}\right) - \omega_n C_g V_o \sin\left(\omega_n t - \frac{2\pi n}{N}\right) = 0 \tag{3.10}$$

In (3.10), V_o is the amplitude of the fundamental component of the voltage waveform, $I_g(V_o)$ and $I_o(V_o)$ are the fundamental components of the transconductor and the output conductance currents, respectively. Similar to the linear analysis, equation (3.10) can be decomposed into the following:

$$I_g\left(V_o\right)\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}\left(i-1\right)\right) + I_o\left(V_o\right) = 0 \tag{3.11}$$

$$I_g\left(V_o\right)\sum_{i=1}^{N} x_i \times \sin\left(\frac{2\pi n}{N}\left(i-1\right)\right) - \omega_n C_g V_o = 0 \tag{3.12}$$

Using the frequency and mode gain definitions in (3.7) and (3.8), we can reduce (3.11) and (3.12) for the dominant oscillation mode into:

$$I_g\left(V_o\right) = a_{n^*} \cdot I_o\left(V_o\right) \tag{3.13}$$

$$\omega_{n^*}\left[\frac{C_g V_o}{I_o\left(V_o\right)}\right] = \frac{\sum_{i=1}^{N} x_i \times \sin\left(\frac{2\pi n^*}{N}\left(i-1\right)\right)}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n^*}{N}\left(i-1\right)\right)} \tag{3.14}$$

Equation (3.13) shows that the oscillation amplitude of an MPRO depends only on the type of nonlinearity that the buffer exhibits and the value of the dominant-mode gain. Fig. 3.5 is an interpretation for (3.13). The figure shows arbitrary amplitude characteristics for an inverter. At small input amplitudes, the inverter acts as a weakly nonlinear amplifier that can be approximated by a third order nonlinearity coefficient. As the input amplitude increases, the output resembles a square-wave whose fundamental component is $(2/\pi)V_{dd}$. As the figure shows, the oscillation amplitude is determined by the amplitude that causes enough gain compression such that the effective dc gain of the inverter is exactly equal to the gain required to sustain the oscillation mode, i.e. the mode gain.

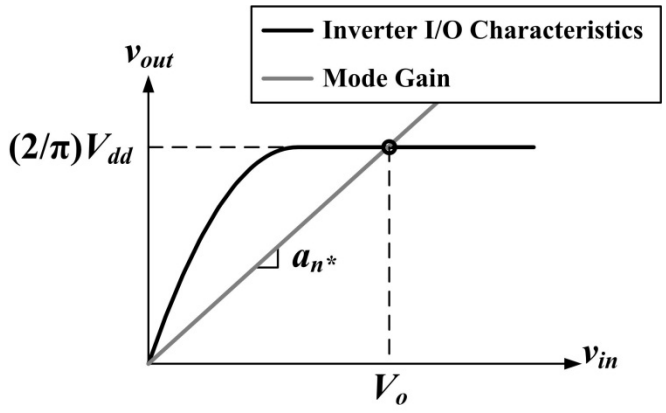


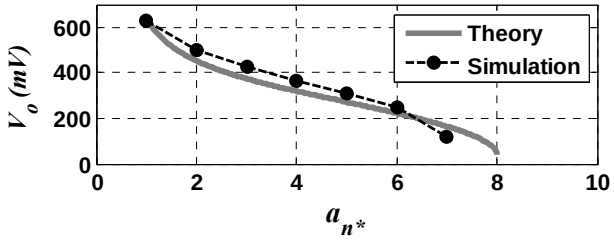
Fig. 3.5. Example of the amplitude characteristics of an inverter.

To find an accurate expression for the oscillation amplitude, the exact shape of the buffer nonlinearity must be known. In general, two limiting cases can be examined. The first case is when the mode gain is close to unity where the oscillation waveform is approximately a square-wave with a fundamental component $(2/\pi)V_{dd}$. In this case, the oscillation amplitude can be approximately given by $(V_o/V_{dd})= (2/\pi)\times(1/a_{n*})$. The other limiting case is when the mode gain is close to the small signal dc gain of the inverter, a_o, which is the maximum gain an inverter can provide. This case causes the oscillation amplitude to be very small and the inverter nonlinearity can be approximated using a third-order nonlinearity coefficient. This coefficient can be chosen to match the simulation results at small oscillation amplitudes.

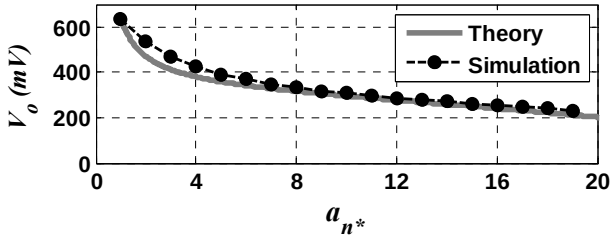
Equation (3.15) is an empirical expression for the oscillation amplitude. This expression is derived by taking the average of the two limiting cases discussed above. The third order nonlinearity coefficient is empirically chosen such that V_o is equal to $(2/\pi)V_{dd}$ when $a_{n*}=1$.

$$\frac{V_o}{V_{dd}} = \frac{1}{\pi}\cdot\left[\frac{1}{a_{n*}} + \sqrt{\frac{a_o - a_{n*}}{a_o - 1}}\right] \tag{3.15}$$

Fig. 3.6 shows the simulated oscillation amplitude as a function of the dominant mode gain together with equation (3.15). The values of the *dc* gain, a_o, used to plot equation (3.15) for different channel lengths are shown in Table 3.1. These values are obtained using *ac* simulation and will be used throughout the rest of this chapter. For each value of the mode gain, we use an MPRO similar to that in Fig. 3.1 with the unit inverter shown in Fig. 3.3 and with sizing factors as shown in Table 3.2. The way these sizing factors are derived is explained in the next subsection. To verify the validity of the expression for different channel lengths, each simulation is repeated using different channel lengths for the NMOS and the PMOS transistors of the inverter. As the figure shows, very good agreement between the empirical equation and the simulation results is observed.



(a)



(b)

Fig. 3.6. Fundamental component of the oscillation waveform as a function of the dominant mode gain. (a) L=60nm (b) L=200nm.

Table 3.1. Small-signal *dc*-gain and time-constant parameters of the unit inverter for different channel lengths

Channel Length (L)	60nm	100nm	200nm	400nm
Small-signal dc gain (a_o)	8	20	30	45
Time-constant (τ_o)	35ps	145ps	580ps	2800ps
Fanout-1 delay (τ_p)	10.2ps	18.4ps	50ps	166ps

To find an expression for the nonlinear time constant, we compare equations (3.14) and (3.7) to derive (3.16), the effective time constant. Equation (3.16) shows that the effective time constant is similar to the oscillation amplitude in that it only depends on the dominant mode gain and the buffer nonlinearity. This result implies that two MPROs with the same dominant mode gain but with different sizing factors and possibly, different number of stages would still have the same oscillation amplitude and effective time constant.

$$\tau = \frac{C_g V_o}{I_o\left(V_o\right)} = \tau\left(a_{n*}\right) \tag{3.16}$$

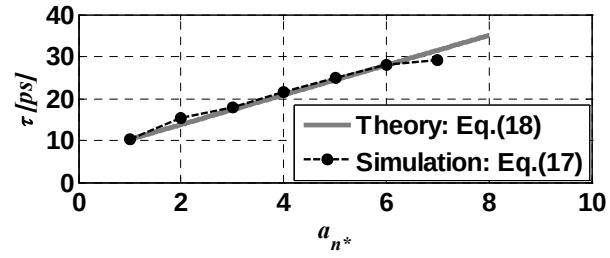
As we did for the oscillation amplitude, we first examine the two limiting cases when $a_{n*} \to 1$ and when $a_{n*} \to a_o$, the small signal *dc* gain of the buffer. These two cases represent the minimum and the maximum dominant mode gains that can exist. Obviously, a mode gain below unity would not satisfy the oscillation unity gain condition and an oscillator with a dominant mode gain greater than a_o would not oscillate.

For the case when $a_{n*} \to 1$, the equivalent time constant $\tau(a_{n*})$ approaches τ_p, the buffer's fanout-1 propagation delay. To explain this, we examine equations (3.7) and (3.8) with $x_N=1$ and N a large odd number. In this case, we see that $a_{n*} \to 1$ and $f_{n*} \to 1/(2N\tau)$ which is the familiar equation for the oscillation frequency of a long-chain SPRO having a delay per stage, τ_p.

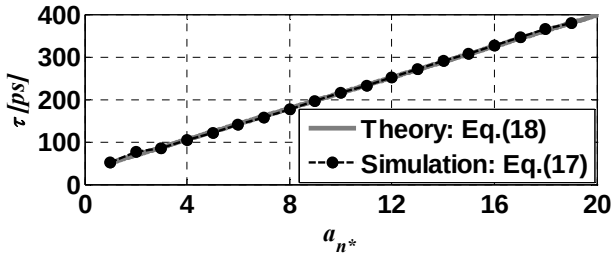
When $a_{n*} \rightarrow a_o$, the oscillation amplitude is infinitesimally small since any growth in amplitude will cause the gain to drop due to nonlinearity. Accordingly, the linear expression for the oscillation frequency becomes valid and the equivalent time constant is equal to the small signal time constant of the buffer, $\tau_o = C_g / g_o$.

Fig. 3.7 shows the simulated values of the effective time constant as a function of the mode gain for different channel lengths of the inverter. The plot is obtained by simulating different MPROs having the sizing factors shown in Table 3.2. For each MPRO, we compare the oscillation frequency obtained from simulation, f_{sim}, to the expression in (3.7) and find the value of the equivalent time constant, τ_{sim}, as shown in equation (3.17).

$$\tau_{sim} = \frac{1}{2\pi f_{sim}} \times \frac{\sum_{i=1}^{N} x_i \times \sin\left(\frac{2\pi n}{N}(i-1)\right)}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)} \tag{3.17}$$



(a)



(b)

Fig. 3.7. Effective time constant as a function of the dominant mode gain. (a) L=60nm (b) L=200nm.

As the figure shows, the effective time constant can be very well approximated using a linear interpolation between the two extreme cases of mode gain. Equation (3.18) shows the approximate expression for the effective time constant as a function of the dominant mode gain. The validity of this approximation is verified by repeating the simulation for different channel lengths as shown in Fig. 3.7. In all cases, we found a very good agreement between the linear interpolation and the simulated values of the time constant. The values for a_o, τ_o and τ_p used in Fig. 3.7 and throughout the rest of this chapter are shown in Table 3.1. These values were obtained using ac simulation for a_o. Values of τ_p are the fanout-1 propagation delay of the unit cell obtained by simulating a 19-stage SPRO. Finally, values of τ_o are those that best fit the curves in Fig. 3.7. These values were found to be very close to the actual small-signal time constant obtained from *ac* simulation.

$$\tau\left(a_{n^*}\right) \approx \tau_p + \left(\frac{\tau_o - \tau_p}{a_o - 1}\right) \cdot \left(a_{n^*} - 1\right) \tag{3.18}$$

3.2.3. Oscillation Frequency

Using equations (3.7), (3.8), and (3.18), an expression for the oscillation frequency can be derived (3.19). Equation (3.19) gives the oscillation frequency of the dominant mode of any MPRO having any arbitrary coupling structure and number of phases.

$$f_{n^*} = \frac{1}{2\pi} \frac{\left(a_o - 1\right) \cdot \sum_{i=1}^{N} x_i \sin\left(\frac{2\pi n^* \left(i-1\right)}{N}\right)}{\left(a_o \tau_p - \tau_o\right) \cdot \sum_{i=1}^{N} -x_i \cos\left(\frac{2\pi n^* \left(i-1\right)}{N}\right) + \left(\tau_o - \tau_p\right)} \tag{3.19}$$

To verify this general expression for the MPRO frequency, the frequency is calculated for different oscillator configurations and compared against circuit simulation results. We start with

the degenerate case of an SPRO. In this case, x_N=1 and all other fractional sizing factors are equal to zero. Equation (3.9) shows that the dominant oscillation mode for SPROs is given by n^*=ceil(N/2). For even N, n^*=N/2 and the oscillation frequency of the dominant mode is always equal to zero indicating the fact that even numbered SPROs latch and do not oscillate. For odd N, n^*=(N+1)/2 showing that the phase shift between every two successive nodes is $\pi+(\pi/N)$ which is a well-known result for SPROs. The oscillation frequency can be found from (3.19) and is expressed by (3.20) and compared to simulation in Fig. 3.8. The expression reduces to the familiar form $f_{SPRO}=1/(2N\tau_p)$ when N is a large odd integer.

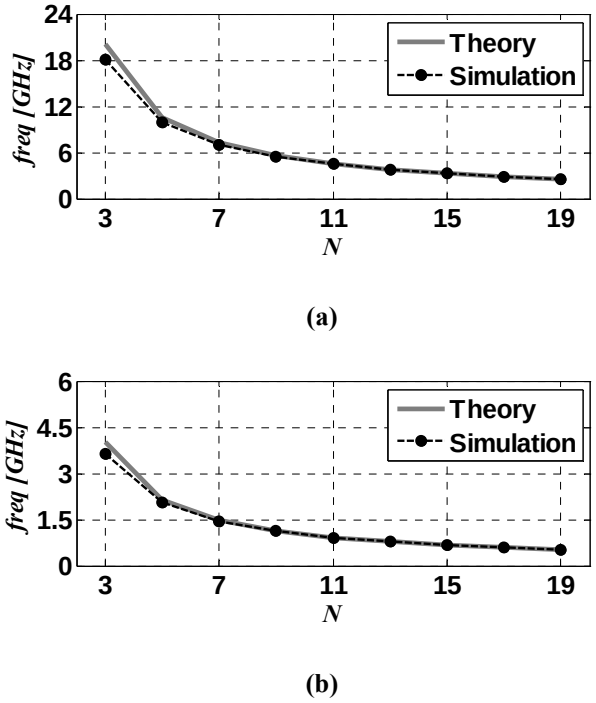
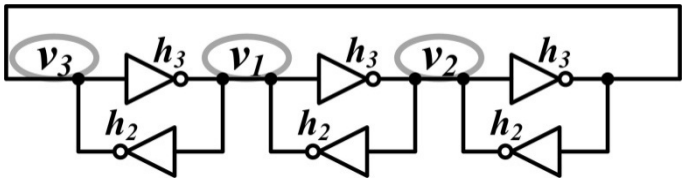


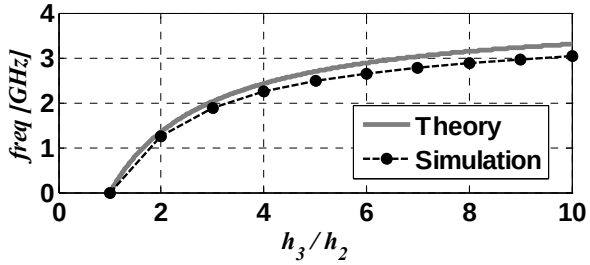
Fig. 3.8. Oscillation frequency of an SPRO for different numbers of stages. (a) L=60nm (b) L=200nm

Fig. 3.9 shows the comparison for the case of a 3-stage dual-path ring oscillator. Fig. 3.9(a) shows the schematic diagram of the oscillator. In this special case, the mode gain is equal to 2 and is independent on the sizing coefficients. Accordingly, the effective time constant is also independent on sizing. The oscillation frequency can be obtained from (3.19) and is plotted in

Fig. 3.9(b). The analytical results were found to match the simulation for all the simulated channel lengths. The figure only shows the results for a channel length of 200nm.



(a)

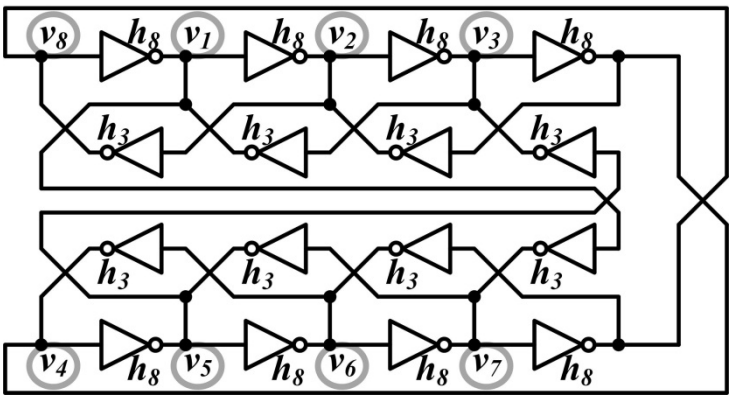


(b)

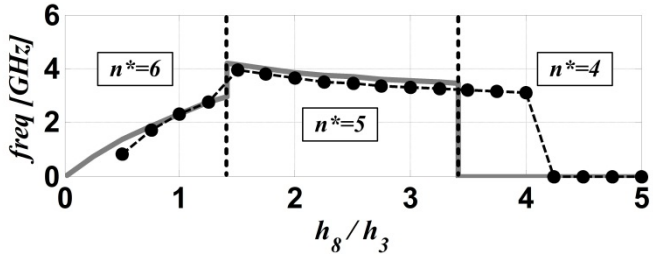
Fig. 3.9. Oscillation frequency of a 3-stage dual-path ring oscillator.
(a) Schematic diagram of the oscillator (b) Simulation results and analytical expression for L=200nm.

Fig. 3.10 and Fig. 3.11 show the comparison between equation (3.19) and the simulation results for two different 8-stage dual-path ring oscillators. The oscillator in Fig. 3.10(a) has a skew of 5 stages meaning that v_1 is driven by v_8 and v_3. Similarly, the oscillator in Fig. 3.11(a) has a skew of 3 stages. Fig. 3.10(b) and Fig. 3.11(b) show the simulation results and the analytical expression for the oscillation frequency. The figures also mark the different regions where different modes are dominant. These regions are found using equation (3.9). The boundaries between these regions are characterized by an abrupt change in frequency accompanied by a change in the output phase order when the sizing factors are changed. For this reason, if the MPRO is to be used as an oscillator that is desired to operate at a stable, well-defined oscillation mode, these boundaries must be avoided.

In both figures, a discrepancy between the simulation and the analytical prediction at the boundary between the modes n^*=5 and n^*=4 is observed. This discrepancy is due to the very small difference in mode gains at this region and the way these oscillators are simulated. This small difference in mode gain causes the possibility of exciting a non-dominant mode if the initial conditions of the oscillator are suitable for this. More about mode stability and dependence on initial conditions is discussed in section 3.3.5.

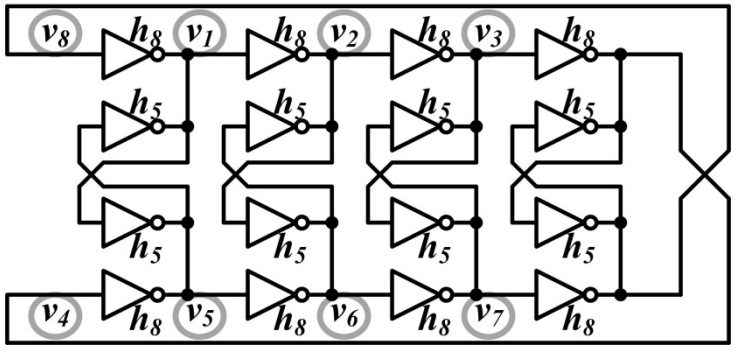


(a)

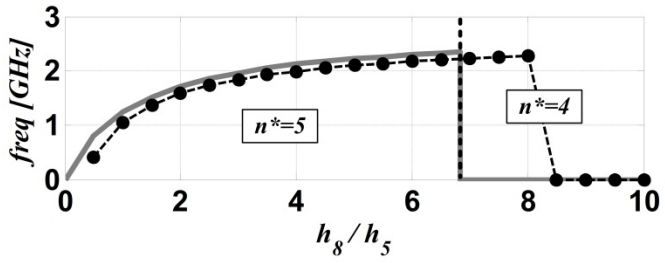


(b)

Fig. 3.10. Oscillation frequency of an 8-stage dual-path ring oscillator with a skew of 5 stages. (a) Schematic diagram of the oscillator (b) Simulation results (black dots) and analytical expression (gray curve) for L=200nm.



(a)



(b)

Fig. 3.11. Oscillation frequency of an 8-stage dual-path ring oscillator with a skew of 3 stages. (a) Schematic diagram of the oscillator (b) Simulation results (black dots) and analytical expression (gray curve) for L=200nm.

3.2.4. Maximum Oscillation Frequency

Using the derived analytical expression for oscillation frequency as a function of the fractional sizing vector, $\overline{x}$, we can find the value of $\overline{x}$ that maximizes the oscillation frequency for a given number of stages and certain constraints on the mode gain. This maximization is useful in determining whether a particular frequency is achievable. Furthermore, as shown in the next section, the design for maximum frequency allows us to design oscillators with lower phase noise.

We first define the two matrices *A* and *B* as given by (3.21) and (3.22) and then rewrite (3.7) and (3.8) in matrix notation as follows:

$$A=\begin{bmatrix} \alpha_{01} & \cdots & \alpha_{0N} \\ \vdots & \ddots & \vdots \\ \alpha_{(N-1)1} & \cdots & \alpha_{(N-1)N} \end{bmatrix};\ \alpha_{ni}=\sin\left(\frac{2\pi n}{N}(i-1)\right) \tag{3.21}$$

$$B=\begin{bmatrix} b_{01} & \cdots & b_{0N} \\ \vdots & \ddots & \vdots \\ b_{(N-1)1} & \cdots & b_{(N-1)N} \end{bmatrix};\ b_{ni}=-\cos\left(\frac{2\pi n}{N}(i-1)\right) \tag{3.22}$$

$$a_n=\frac{1}{B_n^T\bar{x}} \tag{3.23}$$

$$\omega_n\tau=\frac{A_n^T\bar{x}}{B_n^T\bar{x}} \tag{3.24}$$

where $\bar{x}=[x_1\ x_2\ x_3\ \ldots\ x_N]^{\mathrm{T}} \in \Re^{\mathrm{N}}$ is the fractional sizing vector and each of the row vectors $A_n{}^T$ and $B_n{}^T$ is the n^{th} row in the matrices A and B, respectively.

The goal is to maximize $\omega_n*\tau$ where the feasible region of the vector $\bar{x}$ in $\Re^{\mathrm{N}}$ can be expressed by a group of linear equations and linear inequalities. This region is defined by

$$\Psi=\left\{\bar{x}\in\Re^N:\bar{x}\geq 0,\bar{1}^T\bar{x}=1\right\} \tag{3.25}$$

where $\bar{1}^T = [1\ 1\ 1\ \ldots\ 1]^{\mathrm{T}}$. The first constraint requires $\bar{x}$ being positive while the second constraint follows from the definition of $\bar{x}$ summing to unity.

The algorithm used to solve this optimization problem can be summarized in the following steps:

1. For each mode n, where n and N do not have common factors (to guarantee N distinctive phases at the output), find the region of space Ψ_{n} where this mode is dominant. This can be achieved by adding two additional constraints to the feasible

region Ψ as shown in (3.26). The first inequality in (3.26) constrains the mode gain to be less than a certain maximum value, $a_{\max}$. This is important to guarantee certain minimum oscillation amplitude. The second inequality guarantees the mode gain of the mode n is less than that of all other modes. This allows us to maximize the frequency of each mode in the region where this mode is dominant. The parameter δ_m allows us to set a certain margin between the dominant mode gain and other modes to guarantee mode stability. This will be explained more in the next section.

$$\Psi_n = \left\{ \bar{x} \in \Psi : B_n^T \bar{x} > 1/a_{\max}, B_n^T \bar{x} \geq (1+\delta_m) B_m^T \bar{x};\ m \neq n \right\} \tag{3.26}$$

2. Find the maximum normalized oscillation frequency of each mode and the corresponding optimum sizing vector, $\bar{x}_n^*$, by solving the following optimization problem:

$$\begin{aligned} &\text{maximize} \quad A_n^T \bar{x} / B_n^T \bar{x} \\ &\text{subject to: } \bar{x} \in \Psi_n \end{aligned} \tag{3.27}$$

This problem is a linear fractional optimization problem. It can be solved accurately by iteration using a binary search algorithm. Each of the iterations in this algorithm is a linear programming feasibility problem that can be solved in MATLAB by methods such as the Simplex algorithm or interior point methods [46][47].

3. Find the absolute maximum frequency over all modes and the corresponding optimum sizing vector, $\bar{x}^*$.
4. Repeat the previous steps for MPRO's with different numbers of stages.

Fig. 3.12 shows the results obtained from running the above algorithm assuming $a_{\max}$ is infinite and δ_m= 0. These results represent the absolute maximum normalized frequency that can be obtained from an MPRO of a certain number of stages. The results show a linear increase in the maximum possible normalized oscillation frequency as the number of stages increases provided that the dc gain of the buffer sufficient to provide the required amplification. Table 3.2 shows optimum values of the sizing factors, h_i, and the corresponding mode gain for varying number of stages. Note that in this optimization and subsequent derivations, x_1 (an accordingly, h_1) is set to 0 since a diode connected transconductor mainly reduces the effective value of the time constant and thus can be absorbed in the parameter, τ.

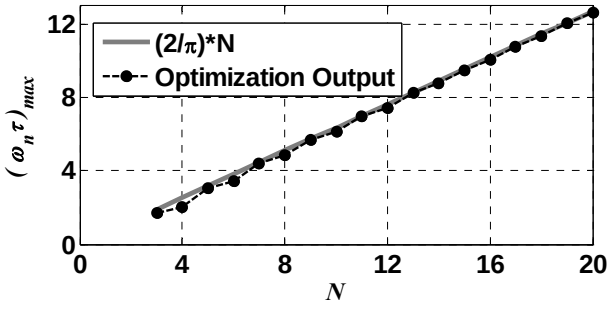


Fig. 3.12. Maximum normalized oscillation frequency.

It is interesting to note that the results in Table 3.2 are considerably systematic and can be easily deduced for higher values of N. Using (3.8) and the values in Table 3.2, the dominant mode gain for maximum frequency is given by $a_{n*}=N-1$ as can be seen in Table 3.2. From (3.7), it can be shown that $\omega_{n*}\tau$ approaches $(2/\pi)\times N$ as N increases.

Since the results in Fig. 3.12 and Table 3.2 were derived assuming δ_m= 0, these results cause the oscillator to oscillate at the boundary between different oscillation modes. In fact, it can be easily shown by substituting the values in Table 3.2 into (3.8) that for each of these MPROs, the

value of the mode gain is the same for all modes n= 1, 2, …, N-1. This means that the maximum oscillation frequency of the MPRO is achieved at the cost of the minimum possible mode stability. Accordingly, if the MPRO is to be used as an oscillator that has a stable well-defined oscillation mode, some back-off from this maximum frequency is needed to guarantee mode stability. However, the results obtained for the maximum frequency and the corresponding sizing factors are still important for two reasons. First, they serve as a benchmark to show the maximum achievable frequency under all circumstances. And second, they can still be used for driven MPROs like in injection-locked oscillators and frequency dividers where mode stability is guaranteed by the external driving signals.

Table 3.2. Optimum sizing factors for maximum oscillation frequency assuming unlimited dc gain and zero mode gain margins

N	a_n	h_2	h_3	h_4	h_5	h_6	h_7	h_8	h_9	h_{10}	h_{11}	h_{12}	h_{13}	h_{14}	h_{15}	h_{16}
3	2	0	1													
4	3	0	1	2												
5	4	0	0	1	1											
6	5	0	0	1	2	2										
7	6	0	0	0	1	1	1									
8	7	0	0	0	1	2	2	2								
9	8	0	0	0	0	1	1	1	1							
10	9	0	0	0	0	1	2	2	2	2						
11	10	0	0	0	0	0	1	1	1	1	1					
12	11	0	0	0	0	0	1	2	2	2	2	2				
13	12	0	0	0	0	0	0	1	1	1	1	1	1			
14	13	0	0	0	0	0	0	1	2	2	2	2	2	2		
15	14	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
16	15	0	0	0	0	0	0	0	1	2	2	2	2	2	2	2

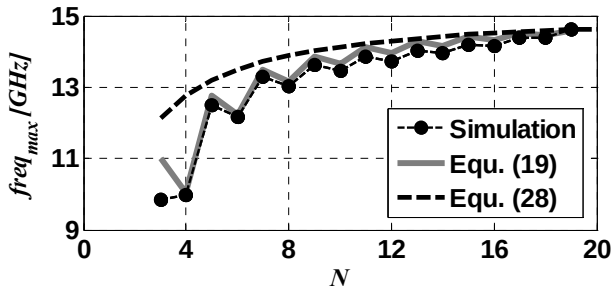
When the mode gain is limited by a certain finite a_{max}, the optimum values of h_i will be different from those shown in the Table 3.2 for N>(1+a_{max}). The new values can be obtained similarly by running the same algorithm as before and setting the appropriate value of the maximum gain. In this case, the maximum normalized oscillation frequency saturates approximately at $(2/\pi)\times(a_{max}+1)$ where a_{max} is the upper bound of the mode gain used in the

optimization problem. In general, if we use the upper bound shown in Fig. 3.12 for $(\omega_n\tau)_{\max}$, that is $(\omega_n\tau)_{\max} < (2/\pi)\times N$, together with (3.18), an approximate maximum limit on the oscillation frequency can be formulated as given by (3.28).

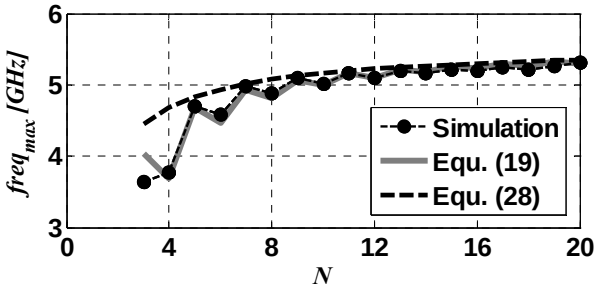
$$f_{\max}(N)=\begin{cases}\dfrac{1}{\pi^2}\dfrac{N(a_o-1)}{(a_o-1)\tau_p+(N-2)(\tau_o-\tau_p)}; & 3\le N\le a_{\max}+1\\[2ex] \dfrac{1}{\pi^2}\dfrac{(a_{\max}+1)(a_o-1)}{(a_o-1)\tau_p+(a_{\max}-1)(\tau_o-\tau_p)}; & N\ge a_{\max}+1\end{cases} \tag{3.28}$$

From this expression, we see that theoretically, the absolute maximum frequency of an MPRO can be achieved when $a_{\max}$ is set equal to a_o, the maximum available dc gain of the inverter. When this gain is high enough, the limit is equal to $(1/\pi^2)\times a_o/\tau_o = (1/\pi^2)\times g_m/C_g$ which is proportional to the cut-off frequency of the unit inverter used to build the oscillator.

Fig. 3.13 shows the actual maximum oscillation frequency obtained from circuit simulation together with the theoretical expression in (3.19) and the maximum limit in (3.28). The increase in the actual frequency is only sub-linear as the figure shows due to the increase of the effective time constant with mode gain as explained in the previous subsection. As the figure shows, as N increases, both equations (3.19) and (3.28) converge and they match the simulation results very closely. In these simulations, the initial state of the oscillator is adjusted such that the desired oscillation mode is excited. It should be noticed that for N=3, the maximum frequency is that of a 3-stage SPRO as indicated in Table 3.2.



(a)



(b)

Fig. 3.13. Simulated maximum oscillation frequency for different numbers of stages. (a) L=100nm (b) L=200nm.

3.2.5. Mode Stability

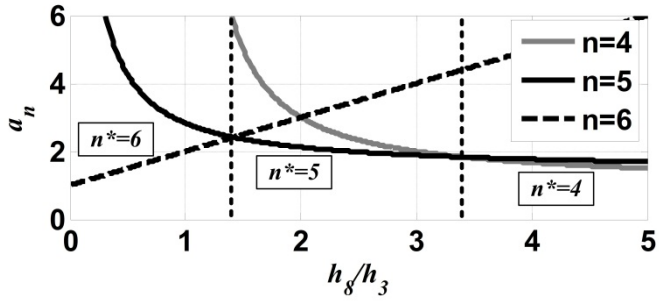
A common problem in MPRO design is the stability of the dominant oscillation mode. Mode stability refers to whether the MPRO always oscillates at the same mode regardless of the initial conditions of the oscillator. This problem is especially pronounced for MPROs with a large number of phases. This is due to the existence of many modes and the very small differences in the value of the mode gain of adjacent modes if the MPRO is not well designed.

Analyzing the problem of mode stability accurately requires an accurate nonlinear state-space analysis to identify the different regions of attraction for each of the oscillation modes in the *N*-dimensional state space of the oscillator [30]. Such accurate analysis is out of the scope of this work and cannot be made using the presented model. However, our model still provides

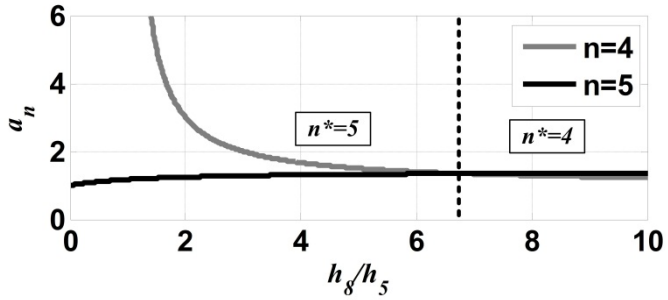
sufficient information for designing MPROs that are less sensitive to their initial conditions and that have a stable, well-defined oscillation mode regardless of their initial state.

As an example, we use the two 8-stage dual-path ring oscillators shown in Fig. 3.10 and Fig. 3.11 with coupling skew of 5 and 3, respectively. Fig. 3.14 shows the mode gain of the different possible modes of oscillation for the two oscillators as a function of the sizing factors. These curves can be obtained using equation (3.8) for different values of n. Modes that are not plotted in the figure are either degenerate or impossible (having negative mode gain). As the figure shows, for both oscillators, the difference in the values of mode gain for n=4 and n=5 is very small near the boundary between these two modes. In general, when the mode gain difference between two modes is small, the oscillator can operate in either one depending on initial conditions. Hence, designing an oscillator near this boundary is undesirable although the maximum oscillation frequency exists at this region.

Another example is shown in Fig. 3.15. The figure shows the mode-gain profile of two 47-stage MPROs. The first MPRO is designed using the design procedure explained in the previous section for maximum oscillation frequency at a maximum mode gain a_{max}=2. The oscillator has sizing factors, (h_{47},h_3)=(2,1), a dominant mode, n^*=31, a dominant mode gain, a_{n^*}=2, and a normalized oscillation frequency, $\omega_{n^*}\tau$=1.73. Fig. 3.15(a) plots the mode gain profile of this oscillator. The even symmetry in the figure directly follows from (3.8). Combined with the odd symmetry in equation (3.7), every two mirror image modes are actually degenerate, i.e. they are the same mode. As the figure shows, the mode gain margin between the dominant mode, n=31, and the adjacent modes is very small. This causes the actual oscillation mode to be sensitive to initial conditions.



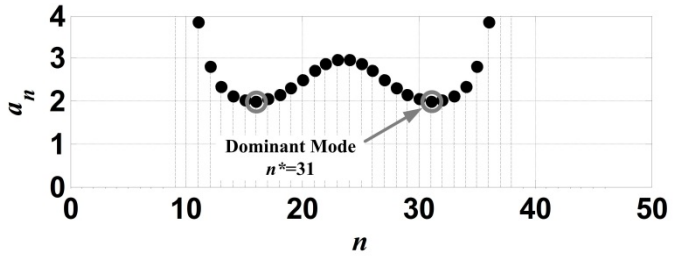
(a)



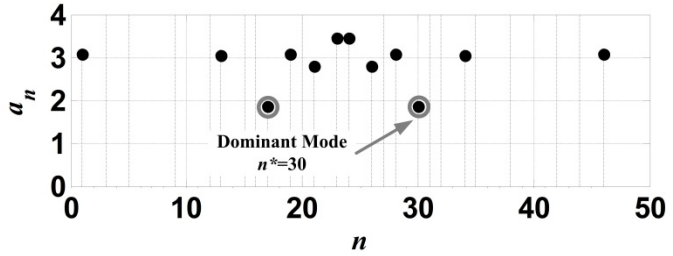
(b)

Fig. 3.14. Mode gain of the different possible oscillation modes of an 8-stage dual-path ring oscillator having (a) Skew=5 (b) Skew=3. The vertical dashed lines represent boundaries between different modes.

Fig. 15(b) shows the mode gain profile of a second MPRO. The sizing factors of the second oscillator are also obtained using the optimization algorithm with the mode gain margin, δ_m, set to 50% to allow for mode stability. After quantizing the sizing factors into integers, the second MPRO has a coupling configuration, (h_{47},h_{25},h_{22},h_{14},h_{11})=(3,5,4,5,2), a dominant oscillation mode, n*=30, a dominant mode gain, a_{n*}=1.84, and a normalized frequency, $\omega_{n*}\tau$=1.48. As Fig 15(b) shows, all the modes other than the dominant mode have at least 50% higher mode gain compared to the dominant mode.



(a)



(b)

Fig. 3.15. Mode gain profile of a 47-stage MPRO having a coupling configuration. (a) (h_{47},h_3)=(2,1) (b) (h_{47},h_{25},h_{22},h_{14},h_{11})=(3,5,4,5,2).

To verify the two MPROs for mode stability, both oscillators are simulated using the test-bench shown in Fig. 3.16. In this simulation, an exponentially decaying sinusoidal waveform is coupled to one node of the MPRO using a small coupling capacitor of 1fF. The coupling capacitor is small enough not to cause any significant loading or mismatch for the MPRO when oscillating at steady state. The excitation frequency, f_s, is varied and the steady-state oscillation frequency and oscillation mode are measured. For the first oscillator in Fig. 3.15(a), the final oscillation mode was found to be dependent on the excitation frequency. This is attributed to the small mode gain margin as explained before. For the second oscillator, we found the final oscillation mode to be always n*=30, independent on the excitation frequency.

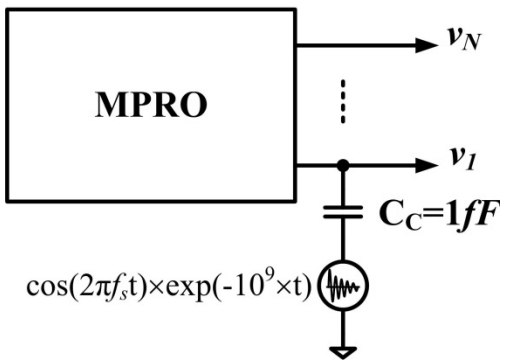


Fig. 3.16. MPRO simulation test-bench. The oscillator is excited using an exponentially decaying sinusoidal waveform of frequency f_s coupled to v_1 using a 1-fF capacitor.

In general, the design methodology presented in this section can be used to design any MPRO with any number of phases. The designer must verify the mode stability by simulating the oscillator using the different expected initial conditions. Improving the mode stability can be achieved by increasing the mode gain margin and this usually comes at the cost of reduced maximum frequency.

3.3. Phase Noise Analysis

The approach for analyzing phase noise follows a linear analysis similar to that in [31]. The MPRO is modeled as an unstable negative feedback system with the noise sources in the system acting as inputs. Fig. 3.17(a) shows the small signal model of the MPRO. Every single transconductor injects noise into the oscillator by an equivalent noise current source, $h_i \times \overline{i_n^2}$. To find the system transfer function, the loop can be opened at node v_1 as shown in Fig. 3.17(b) where all the noise sources injecting noise current at v_1 are lumped into one noise source, $H \times \overline{i_n^2}$ where H is the total sizing factor. The system is equivalent to the circuit in Fig. 3.17(c) where the output current from the equivalent transadmittance across v_1 is subtracted from the input noise

current. The error current is converted into a noise voltage by the impedance $Z(j\omega)/H$ seen at node v_1 to ground where $Z(j\omega)=1/(g_o+j\omega C_g)=r/(1+j\omega\tau)$.

Based on this model, and using Fig. 3.17(d), the open–loop gain, $G(j\omega)$, and the closed–loop transfer function, $T(j\omega)$, of the MPRO can be expressed in equations (3.29) and (3.30) respectively.

$$\begin{aligned} G(j\omega) &= \left[\frac{1}{H}\cdot Z(j\omega)\right]\cdot\left[H\cdot Y_m(j\omega)\right] \\ &= Z(j\omega)\cdot Y_m(j\omega) \end{aligned} \tag{3.29}$$

$$T(j\omega) = \frac{v_n}{i_{in}}(j\omega) = \frac{1}{H}\cdot\frac{Z(j\omega)}{1+G(j\omega)} \tag{3.30}$$

At the oscillation frequency, ω_n, linear analysis predicts an infinite closed-loop transfer function and an open-loop gain, $G(j\omega_n) = -1$. Using the first order Taylor series approximation for $G(j\omega)$ and assuming that $\Delta\omega << \omega_n$, we can approximate $T(j\omega_n+j\Delta\omega)$ as

$$T(j\omega_n + j\Delta\omega) \approx \frac{1}{H}\frac{Z(j\omega_n)}{\dfrac{d}{d\omega}\left[G(j\omega)\right]\Big|_{\omega=\omega_n}\cdot(\Delta\omega)} \tag{3.31}$$

The noise voltage at the node v_1 due to the noise current injected at this node can be expressed as

$$\overline{v_n^2}(j\omega_n + j\Delta\omega) = \frac{\overline{i_n^2}}{H}\left|\frac{Z(j\omega_n)}{\dfrac{d}{d\omega}\left[G(j\omega)\right]\Big|_{\omega=\omega_n}\cdot(\Delta\omega)}\right|^2 \tag{3.32}$$

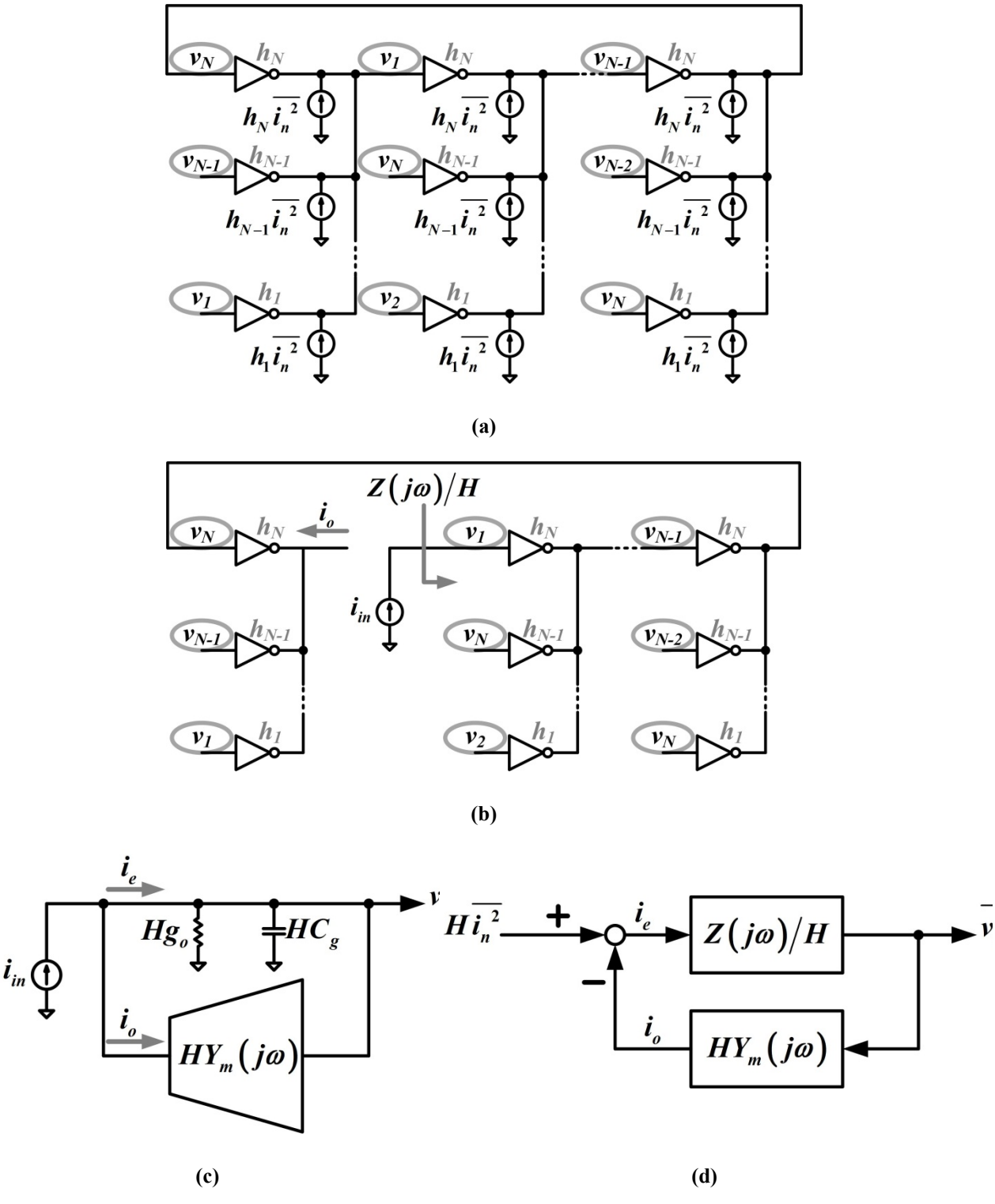


Fig. 3.17. Linear model used for noise analysis. (a) Schematic diagram for the MPRO in closed loop. (b) Schematic of the MPRO in open loop configuration. (c) Equivalent circuit of the MPRO. (d) Block diagram of the equivalent negative feedback system.

By using assumptions similar to [31][1], the expression for the single-sideband phase noise due to the noise sources from the N nodes is

$$\begin{aligned} L(\Delta\omega) &= \frac{1}{2}\cdot\frac{\overline{v_n^2}}{V_{rms}^2}\cdot N \\ &= \frac{\overline{i_n^2}\cdot r^2}{V_o^2}\cdot\frac{N}{H}\left|\frac{Z(j\omega_n)/r}{\omega_n\dfrac{d}{d\omega}\left[G(j\omega)\right]\Big|_{\omega=\omega_n}}\right|^2\cdot\left(\frac{\omega_n}{\Delta\omega}\right)^2 \end{aligned} \tag{3.33}$$

where the mean-squared voltage of the oscillation waveform is $V_{rms}^2=V_o^2/2$.

To find an expression for the oscillator figure of merit, the normalized power consumption, P_u, is defined as power consumed in mW by a single stage in the MPRO having a total sizing factor, H=1. With this definition, the total power consumption of the MPRO can be expressed as

$$P_{tot,mW} = N\cdot H\cdot P_u \tag{3.34}$$

Combining (3.33) and (3.34), the figure of merit of the MPRO is expressed in equation (3.35) where $I_o(V_o)$ is the fundamental component of the output conductance current as in (3.10) and the power is in mW.

$$\begin{aligned} FOM &= \left\{\frac{L(\Delta\omega)\times P_{tot,mW}}{(\omega_n/\Delta\omega)^2}\right\}^{-1} \\ &= \left[\frac{V_o^2}{\overline{i_n^2}\cdot r^2}\cdot\frac{1}{P_u}\right]\cdot\left\{\left|\frac{\omega_n\dfrac{d}{d\omega}\left[G(j\omega)\right]\Big|_{\omega=\omega_n}}{N\cdot Z(j\omega_n)/r}\right|^2\right\} \\ &= \left[\frac{I_o^2}{\overline{i_n^2}}\cdot\frac{1}{P_u}\right]\cdot F_{MPRO}(\bar{x}) \end{aligned} \tag{3.35}$$

[1] Assume that half of the power is causing phase noise while the other half is causing amplitude noise that is rejected by the nonlinear amplitude limiting mechanism of the oscillator. Also assume that the voltage gain between different nodes of the MPRO close to the oscillation frequency is approximately unity.

The first term of (3.35) is dependent on both the circuit design of the unit buffer and the MPRO coupling configuration. The coupling configuration determines the value of the dominant mode gain which in turn determines the value of the oscillation amplitude, V_o, the output conductance current, $I_o(V_o)$, and the equivalent noise current, $\overline{i_n^2}$ [32][33]. The normalized power dissipation, P_u, is also dependent on mode gain at low values of the mode gain where power is dominated by the switching power, $P_{u,sw}=V_{dd}(2V_o)C_gf$. Power is impacted not only through V_o but is also proportional to $(\omega_n\tau)$. At higher values of the dominant mode gain, the total power remains roughly constant since the inverting buffers behave as class-A amplifiers as the oscillation amplitude decreases.

The second term in (3.35), $F_{MPRO}(\bar{x})$, is only dependent on the coupling structure and not on the unit buffer design. This term represents the filtering or the frequency selectivity of the MPRO. In other words, it represents the effective quality factor of the oscillator. By optimizing this term, we can determine the best phase noise performance of an MPRO given a certain mode gain.

To derive an expression for $F_{MPRO}(\bar{x})$, we first derive an expression for the transadmittance, $Y_m(j\omega)$. From Fig. 3.17(b), the output current is given by

$$i_{out}(j\omega) = Hg_m\tilde{x}^T\bar{v}(j\omega) = HY_m(j\omega)v_1 \tag{3.36}$$

where $\tilde{x}=[x_2\ x_3\ \ldots\ x_N]^T$ and $\bar{v}=[v_2\ v_3\ \ldots\ v_N]^T$. We assume as before that $x_1=0$. Therefore, the open-loop gain of the MPRO can be expressed as

$$G(j\omega) = \frac{g_m/g_o}{1+j\omega\tau}\tilde{x}^T(\bar{v}/v_1) \tag{3.37}$$

To find the vector ($\bar{v}/v_1$), we apply *KCL* at the node v_k with $k\neq 1$. By defining the matrix X as shown in (3.38) and the vector $\tilde{x}_F=[x_N\ x_{N-1}\ \ldots\ x_2]^T$, we can express the vector ($\bar{v}/v_1$) as shown in (3.39). The open-loop gain can then be expressed by (3.40).

$$X=\begin{bmatrix} \dfrac{1+j\omega\tau}{g_m/g_o} & x_2 & \cdots & x_{N-1} \\ x_N & \dfrac{1+j\omega\tau}{g_m/g_o} & \cdots & x_{N-2} \\ \vdots & \vdots & \ddots & \vdots \\ x_3 & x_4 & \cdots & \dfrac{1+j\omega\tau}{g_m/g_o} \end{bmatrix} \tag{3.38}$$

$$\left(\bar{v}/v_1\right)=-X^{-1}\cdot\tilde{x}_F \tag{3.39}$$

$$G\left(j\omega\right)=-\left(\frac{g_m/g_o}{1+j\omega\tau}\right)\tilde{x}^T\cdot X^{-1}\cdot\tilde{x}_F \tag{3.40}$$

By differentiating (3.40) with respect to $j\omega\tau$ and using the fact that $G(j\omega_n)\approx$-1, the expression for $F_{MPRO(\bar{x})}$ can be written as (3.41). In this step, we use the effective transconductance and output conductance, not the small-signal ones. Thus g_m/g_o is equal to a_n.

$$F_{MPRO}\left(x\right)=\left(\frac{\omega_n\tau}{N}\right)^2\left|1+\tilde{x}^T\cdot {X_n}^{-1}\cdot {X_n}^{-1}\cdot\tilde{x}_F\right|^2 \tag{3.41}$$

From (3.40) and using the values of the normalized frequency and the mode gain in (3.6) and (3.7), $(1+j\omega\tau)/a_n$ can be expressed as a sum of complex exponentials as (3.42)

$$\tilde{x}^T\cdot {X_n}^{-1}\cdot\tilde{x}_F=-\tilde{x}^T\cdot C_n=-{C_{Fn}}^T\cdot\tilde{x}_F \tag{3.42}$$

where $C_n=[e^{-j\frac{2\pi n(2-1)}{N}}\ \ e^{-j\frac{2\pi n(3-1)}{N}}\ \ \cdots\ \ e^{-j\frac{2\pi n(N-1)}{N}}]^T$ and $C_{Fn}=[e^{-j\frac{2\pi n(N-1)}{N}}\ \ e^{-j\frac{2\pi n(N-2)}{N}}\ \ \cdots\ \ e^{-j\frac{2\pi n(2-1)}{N}}]^T$. Since all elements of $\tilde{x}$ and $\tilde{x}_F$ and all the real and imaginary components of X_n^{-1} are greater than or equal

to 0 and with at least one element greater than 0, then, $X_n^{-1} \cdot \tilde{x}_F = -C_n$ and $\tilde{x}^T \cdot X_n^{-1} = -C_{Fn}{}^T$ which means

$$F_{MPRO}(x) = \left(\frac{\omega_n \tau}{N}\right)^2 \left|1 + C_{Fn}{}^T \cdot C_n\right|^2 = (\omega_n \tau)^2 \tag{3.43}$$

Interestingly, the value of $F_{MPRO}(\bar{x})$ is equal to $(\omega_n \tau)^2$ hence reducing the expression for phase noise to (3.44) and the *FOM* to (3.45). Since the unit power consumption is proportional, at most, to $(\omega_n \tau)$ while $F_{MPRO}(\bar{x})=(\omega_n \tau)^2$, maximizing the normalized oscillation frequency using the algorithm explained in the previous section, also maximizes the *FOM* given a certain value of the dominant mode gain.

$$L(\Delta\omega) = \frac{\overline{i_n^2} \cdot r^2}{V_o^2} \cdot \frac{1}{HN} \cdot \frac{1}{(\omega_n \tau)^2} \cdot \left(\frac{\omega_n}{\Delta\omega}\right)^2 \tag{3.44}$$

$$FOM = \left(\frac{I_o{}^2}{\overline{i_n^2}} \cdot \frac{1}{P_u}\right) \cdot (\omega_n \tau)^2 \tag{3.45}$$

The numerical value for the *FOM* depends on how the different terms in (3.45), other than $(\omega_n \tau)$, vary as a function of the dominant mode gain. The analysis has been done for SPROs [34-37]. The resulting expressions for *FOM* from [34-37] vary depending on the assumptions but the final numerical values in all derivations predict an *FOM* in the vicinity of 170dB when the mode gain approaches unity[2].

In this work, we do not derive expressions for the different terms in (3.45). Although this is possible, we believe that these expressions are of limited practical importance. The more important conclusion in this paper is that for a certain value of the mode gain, maximizing the

[2] An SPRO with a large number of stages is the case when the mode gain approaches unity.

normalized frequency gives the best *FOM* and accordingly, the best phase noise versus power tradeoff.

Fig. 3.18 shows the simulated maximum *FOM* measured at a 10MHz offset frequency as a function of the dominant mode gain for different channel lengths. These results are obtained by simulating the MPROs in Table 3.2. The result for $a_n \approx 1$ is obtained using a 19-stage SPRO as an example of a long chain SPRO and it agrees with the predictions in [34-37]. The maximum FOM for $a_n=2$ is equal to that of a 3-stage SPRO as indicated in Table 3.2. In general, as the figure shows, as the dominant mode gain increases, the maximum *FOM* decreases due to the faster reduction in the first term in (3.45) compared to the possible increase in $(\omega_n \tau)$. Initially this reduction is relatively fast for a_n between 1 and 3, and then the *FOM* stays relatively constant until the mode gain approaches the small-signal dc gain of the unit inverter. At this point, the *FOM* decreases sharply due to the fast reduction in oscillation amplitude.

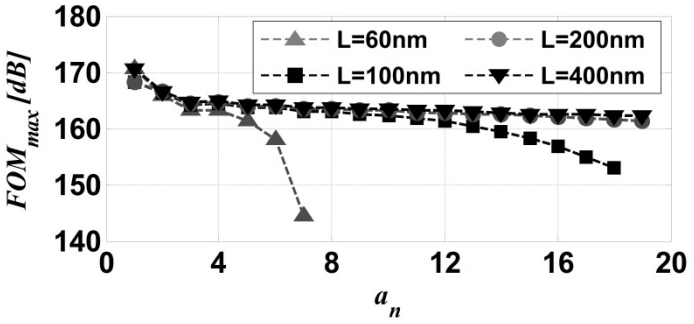


Fig. 3.18. Simulated maximum FOM as a function of the mode gain. Phase noise is measured at a 10-MHz offset frequency.

For applications requiring multiple clock phases, it is important to note that equation (3.45) does not directly depend on the number of phases of the MPRO. As long as the mode gain and the oscillation frequency stay constant, increasing the number of phases does not change the

FOM, theoretically. When the MPRO is sized correctly, the additional phases come at zero power cost.

Table 3.3 shows the coupling configurations for a number of MPROs having different number of phases spanning a range from 8 to 32. These coupling configurations have been obtained using the optimization algorithm in Section 3.3.4 where mode stability is also taken into consideration. The coupling configurations shown in the table are those obtained after quantizing the resulting sizing factors into integers to be suitable for practical implementation.

The simulation results shown in Table 3.3 are obtained using the same unit cell in Fig.3.3 with a channel length 200nm. As we can see from the table, although the number of phases spans 2 octaves, the *FOM* of all MPROs differs only by less than ±0.5dB and their oscillation frequency differs only by ±3%. The *FOM* stays roughly constant because all of the oscillators are designed to have approximately the same value for the dominant mode gain, a_{n*}, and the normalized oscillation frequency, ($\omega_n \tau$). If these MPROs are scaled such that all of them have the same total power consumption then all of them would have the same thermal phase noise. These results indicate that the oscillation frequency can be decoupled from the desired number of phases and the additional phases can theoretically be obtained at zero power cost.

In practice, however, for a given power consumption, the number of phases cannot be increased indefinitely. As the number of stages increases at the same total power, the driving capability of the MPRO is divided among a greater number of stages reducing the driving capability of each single phase. In addition, as the number of stages increases, the layout routing becomes more complex leading eventually to a need for increasing the total oscillator power in order to drive this increased loading.

Table 3.3. Coupling Configurations and Simulation Results for Unloaded MPROs Designed for Dominant Mode Gain ≈ 2 and Mode Gain Margin > 60% for Mode Stability.

N	*Coupling Configuration*	*Dominant Mode (n*) Eq (9)*	*Mode Gain (a_{n^*}) Eq (3.8)*	*Mode Gain Margin (δ_m) Eq (3.26)*	*Normalized Freq ($\omega_{n^*}\tau$) Eq (3.7)*	*Freq (GHz) Eq (3.19)*	*Freq. (GHz) [Sim.]*	*Pwr (mW) [Sim.]*	*FOM (dB) [Sim.]*
8	(h_8,h_5,h_3)=(4,1,3)	5	2.09	91%	1.52	3.46	3.31	9.55	165.4
9	(h_9,h_7,h_5)=(2,4,1)	5	1.89	163%	1.39	3.34	3.12	8.94	165.8
10	(h_{10},h_3)=(1,1)	7	1.79	123%	1.38	3.41	3.15	2.75	166.3
11	(h_{11}, h_8,h_3)=(4,1,2)	7	1.81	122%	1.37	3.36	3.12	10.65	166.1
12	(h_{12},h_{10},h_5)=(2,1,4)	7	1.88	86%	1.46	3.52	3.28	11.88	166.2
13	(h_{13},h_8,h_5,h_3)=(5,2,1,2)	8	1.93	128%	1.43	3.40	3.20	18.71	165.8
14	(h_{14},h_{11},h_3)=(3,1,2)	9	1.87	74%	1.47	3.55	3.29	11.83	166.2
15	(h_{15},h_{11},h_7)=(2,3,4)	11	1.82	70%	1.40	3.43	3.19	18.78	166.2
16	(h_{16},h_{13},h_6,h_3)=(1,2,1,4)	11	1.93	107%	1.48	3.52	3.30	18.44	166.0
32	(h_{32},h_{20},h_{15},h_{10},h_5)=(3,2,2,1,1)	19	1.83	64%	1.43	3.49	3.23	40.14	166.2

Based on the analysis we present in this paper, the design of a ring oscillator, given a certain unit buffer design, should proceed in the following steps. First, the required number of phases, the target oscillation frequency and the power budget should be specified. Second, the values of the parameters a_o, τ_o, and τ_p should be found by simulation for different channel lengths of the devices. Third, using the optimization algorithm explained in Section 3.3, the optimum sizing factors can be found. The constraint on maximum allowed mode gain must be decreased until the minimum possible mode gain is found. This is done by running the algorithm and comparing the oscillation frequency in (3.19) to the target frequency until the minimum mode gain is found. If the required number of phases is odd and the target frequency is less than or equal the frequency of an SPRO (3.20), the optimum design converges to an SPRO. Finally, the phase noise should be simulated. If the phase noise performance is limited by flicker noise, then the overall performance can be improved by using longer channel lengths for the devices at the cost of lower speed. To compensate for the reduced frequency, the previous step should be repeated where the optimum mode gain needs to be increased. In this way, the flicker noise performance is improved at the cost of thermal noise.

3.4. Conclusion

In this chapter, a general model for multipath ring oscillators having arbitrary coupling structures is presented. With multiple modes of oscillation possible in MPRO structures, we define the mode gain as the minimum buffer *dc* gain required to sustain a certain oscillation mode. The value of the mode gain is only a function of the sizing factors of the different coupling branches. The dominant mode is the oscillation mode with the lowest mode gain. We show that several properties of the oscillator like the oscillation amplitude, the effective time constant, the normalized power consumption and the effective noise factor are dependent on the oscillator sizing only through the mode gain. An algorithm is introduced to calculate the optimum sizing factors for the different coupling branches to achieve the maximum oscillation frequency and the best phase noise taking into consideration the stability of the oscillation mode. The results and methodology are verified by circuit simulation.

This chapter provides several guidelines for designing MPROs. The results of the optimization show a simple heuristic for sizing an MPRO for maximizing the output frequency. While frequency can be maximized by maximizing the mode gain of the dominant mode, a designer should not choose a target mode gain near the maximum. Backing off from the maximum avoids boundaries between modes, and improves an oscillator's figure of merit. Furthermore, the analysis indicates that for a given oscillation frequency and target mode gain, the number of output phases can be increased without penalizing the figure of merit.

In the next chapter, the MPRO analysis is extended for optimizing the design of multiphase frequency dividers. The divider is considered to be a further generalization of the multipath ring oscillator, namely, a superharmonic injection-locked multipath ring oscillator.

CHAPTER 4

Superharmonic Injection-Locked Multipath Ring Oscillators

In this chapter, we extend the analysis we presented in the previous chapter to include frequency dividers. We show that any latch-based divider can be modeled and analyzed as an injection-locked oscillator. The locking range of this oscillator is dependent on the oscillator structure and the injection strength. By deriving accurate expressions for the locking range, a design procedure can be deduced to maximize the maximum division frequency. If the divider is not required to operate at the maximum frequency, high-speed can be traded-off for power savings.

4.1. General Model

A superharmonic injection-locked MPRO (SHIL-MPRO) is an MPRO that is locked in phase at steady state to an input periodic signal with a frequency that is an integer multiple (i.e. a superharmonic) of the frequency of the MPRO itself [29]. Accordingly, a SHIL-MPRO is typically used as a frequency divider. In this section, we propose a general model for a SHIL-MPRO. This model can be used to find the optimal sizing factors and clocking configuration that maximize the locking frequency of the divider.

To explain our model, we begin first by a simple example of the divide-by-2 shown in Fig. 4.1(a). The divider consists of two latches driven by a differential clock input. Fig. 4.1(b) shows a CML implementation of the latch while Fig. 4.1(c) shows a possible CMOS implementation. In both implementations, the clock signal modulates the transconductance of the amplifying

transistors by modulating their bias current. For the CMOS implementation, the clock signal also modulates the output conductance of the inverters since it is dependent on the bias current.

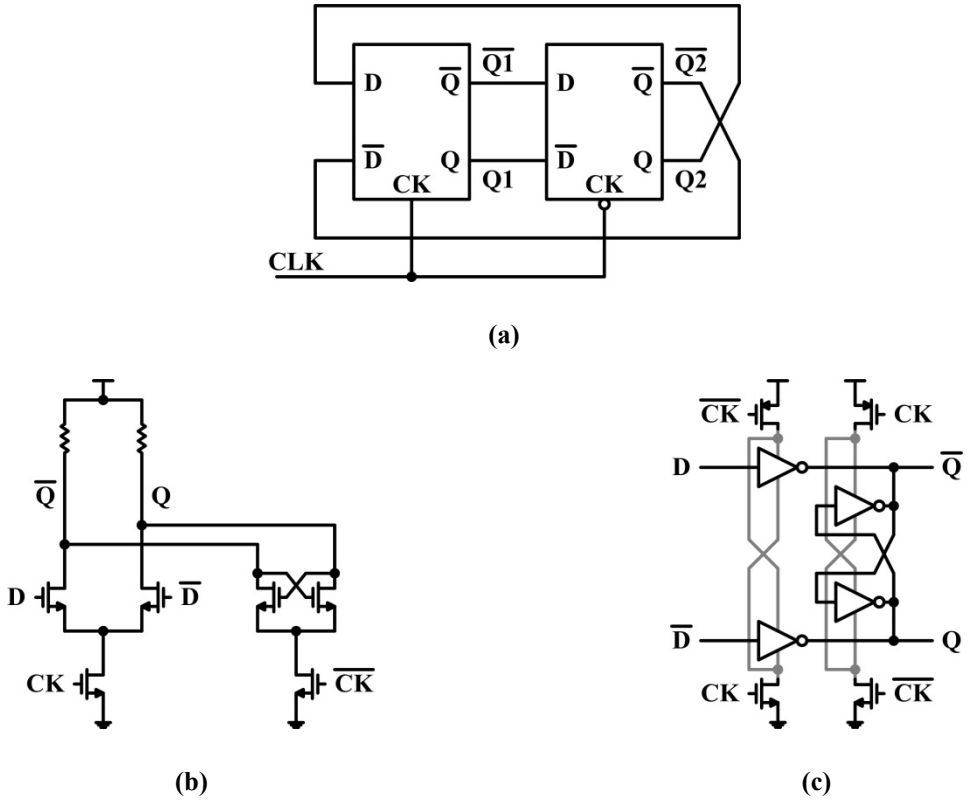


Fig. 4.1. Latch-based divide-by-2 (a) Divider schematic (b) CML latch implementation (c) CMOS latch implementation

As a result of this mixing effect, the output current of any of the transconductors forming the divider consists of many harmonic components. One component is a linear product due to the input of the transconductor. Other components are the different intermodulation products of the latch input with the clock signal. Fig. 4.2 shows an equivalent block diagram for the quadrature divider. The divider can be considered an injection-locked quad-phase MPRO. The injection currents are the result of mixing the MPRO outputs with the different input clock phases.

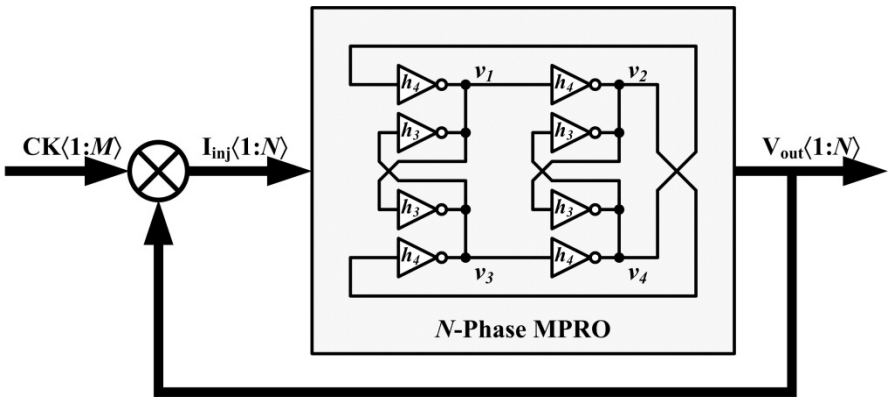


Fig. 4.2. Equivalent model of the quadrature divider.

A general model for an M-phase input, N-phase output SHIL-MPRO is shown in Fig. 4.3. The core oscillator is a general MPRO similar to that in Fig. 3.1. The parameters $\{h_i\}$ are sizing parameters with respect to a reference unit inverter. The parameters $\{\alpha_i\}$ take values 1 or 0 according to whether the i^{th} branch of inverters is driven by the clock or not, respectively. We assume in our analysis that a single-tone harmonic balance is accurate enough. Therefore, assuming the MPRO is locked at a frequency ω_o, the output voltages can be approximated by (4.1). The transconductance of the inverter driven by the node v_p and driving the node v_q is modulated by the clock signal $u_{(q,p)}(t)$ given by (4.2). We assume the input clock has a frequency ω_{in} and M distinct phases available. The clock phases distribution is determined by the parameters (m_1,m_2) which can take integer values between 0 and M-1. By varying the values of (m_1,m_2), all the possible uniform phase distributions can be modeled. Finally, the angle ψ is a phase shift that depends on the injection frequency. In this analysis, we only consider the case of tail injection. In general, direct injection can also be included by considering an additional set of clock inputs modulating the output conductance of the inverters.

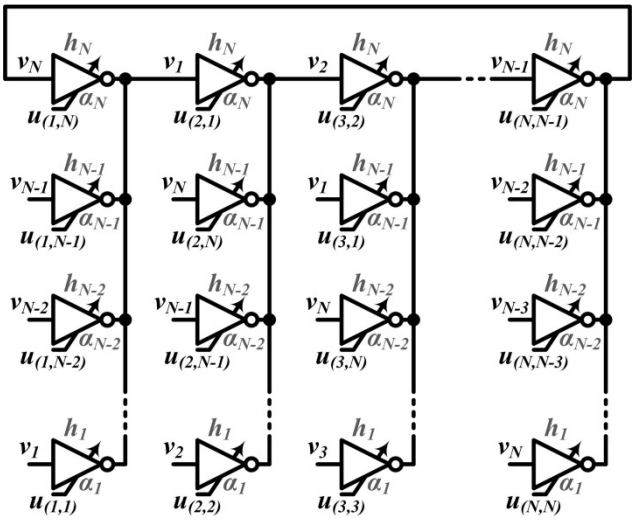


Fig. 4.3. General model of an *M*-phase input *N*-phase output SHIL-MPRO.

$$v_i(t) = V_o \cos\left(\omega_o t - \frac{2\pi n(i-1)}{N}\right) \tag{4.1}$$

$$u_{(q,p)}(t) = U_o \cos\left(\omega_{in} t - \frac{2\pi\left[m_1(q-1) + m_2(p-1)\right]}{M} + \psi\right) \tag{4.2}$$

The transconductance current of the inverter driven by v_p and driving v_q can be expressed by (4.3). We assume the transconductance can be modeled as a memoryless nonlinear time varying element. The first term in (4.3) represents the different components due to the transconductance nonlinearity. The second component is the time variation function caused by the input clock signal. This function is described by the coefficients $\alpha_{i,k}$. If the i^{th} branch is clocked (α_i=1), then $\alpha_{i,k}$ is equal to λ_k, the k^{th} Fourier coefficient of the time modulation function. If the i^{th} branch is not clocked (α_i=0), then $\alpha_{i,k}$ is equal to unity for k=1 and is zero for $k\neq$1.

$$\begin{aligned} i_{g(q,p)} = h_{p-q+1} &\times \left\{\sum_{k=1}^{\infty} g_{m,k} V_o \cos\left[k\omega_o t - k\frac{2\pi n(p-1)}{N}\right]\right\} \\ &\times \left\{\sum_{k=0}^{\infty} \alpha_{(p-q+1),k} \cos\left[k\omega_{in} t - k\frac{2\pi\left[m_1(q-1) + m_2(p-1)\right]}{M} + k\psi\right]\right\} \end{aligned} \tag{4.3}$$

From all the frequency components given by (4.3), we are only interested in the component at ω_o. To calculate this component, we assume that at lock, the input frequency is an integer multiple of the output frequency, that is $\omega_{in}=d\times\omega_o$. By using this assumption, the transconductance current component at ω_o can be calculated as shown in (4.4). The first component of this current is the linear g_m product. The second and third components are the injection current components due to upper side and lower side injection, respectively.

$$\begin{aligned} i_{g(q,p)}\big|_{\omega_o} &= \left(h_{p-q+1}\cdot\alpha_{p-q+1,0}\right) g_{m,1} V_o \cos\left[\omega_o t - \frac{2\pi n(p-1)}{N}\right] \\ &+ \frac{V_o}{2} h_{p-q+1} \sum_{k=1}^{\infty} \left(g_{m,(kd-1)}\cdot\alpha_{p-q+1,k}\right) \cos\left[\omega_o t + (kd-1)\frac{2\pi n(p-1)}{N} - k\frac{2\pi\left[m_1(q-1)+m_2(p-1)\right]}{M} + k\psi\right] \\ &+ \frac{V_o}{2} h_{p-q+1} \sum_{k=1}^{\infty} \left(g_{m,(kd+1)}\cdot\alpha_{p-q+1,k}\right) \cos\left[\omega_o t - (kd+1)\frac{2\pi n(p-1)}{N} + k\frac{2\pi\left[m_1(q-1)+m_2(p-1)\right]}{M} - k\psi\right] \end{aligned} \tag{4.4}$$

At any node v_q of the oscillator, the harmonic balance equation can be written as (4.5) where g_o and C_g are the output conductance and input capacitance of the unit inverter, respectively. The parameter $H=\sum_{i=1}^{N} h_i$ is defined similar to the MPRO case. Substituting from (4.1) and (4.4) into (4.5), the harmonic balance equation can be rewritten as shown in (4.6).

$$\sum_{i=1}^{N} i_{g(q,i+q-1)} + Hg_o v_q + HC_g \frac{dv_q}{dt} = 0 \tag{4.5}$$

$$\begin{aligned} &\sum_{i=0}^{N} h_i \alpha_{i,0} g_{m,1} V_o \cos\left[\omega_o t - \frac{2\pi n(q-1)}{N} - \frac{2\pi n(i-1)}{N}\right] + Hg_o V_o \cos\left[\omega_o t - \frac{2\pi n(q-1)}{N}\right] - HC_g\omega_o V_o \sin\left[\omega_o t - \frac{2\pi n(q-1)}{N}\right] \\ &+ \frac{V_o}{2}\sum_{i=1}^{N} h_i \sum_{k=1}^{\infty} g_{m,(kd-1)}\alpha_{i,k} \cos\left\{\omega_o t - \frac{2\pi n(q-1)}{N} - \frac{2\pi n(i-1)}{N} + k\left[2\pi\left(\frac{nd}{N}-\frac{m_2}{M}\right)(i-1) + 2\pi\left(\frac{nd}{N}-\frac{m_1+m_2}{M}\right)(q-1) + \psi\right]\right\} \\ &+ \frac{V_o}{2}\sum_{i=1}^{N} h_i \sum_{k=1}^{\infty} g_{m,(kd+1)}\alpha_{i,k} \cos\left\{\omega_o t - \frac{2\pi n(q-1)}{N} - \frac{2\pi n(i-1)}{N} - k\left[2\pi\left(\frac{nd}{N}-\frac{m_2}{M}\right)(i-1) + 2\pi\left(\frac{nd}{N}-\frac{m_1+m_2}{M}\right)(q-1) + \psi\right]\right\} \\ &= 0 \end{aligned} \tag{4.6}$$

By comparing the first line in (4.6) to equation (3.2), we see that it represents the behavior of the MPRO. The second and third lines of equation (4.6) represent the injection current. For the output of the SHIL-MPRO to have uniform phases, the gain and phase conditions of the oscillator at lock should be independent on the node where the harmonic balance is derived. From (4.6), we can see that this can only happen if the condition given by (4.7) is satisfied. This condition represents the allowed input clock phase distributions that can result in uniform output phases. For the oscillator outputs to have N distinct phases, the mode index n and the number of stages N should have no common factors. This condition implies that the minimum number of input phases, M, required to have uniform phases at the output throughout the whole locking range is equal to the number of output phases, N, divided by the division ratio, d, or $M \geq N/d$. Equation (3.7) thus serves as the mathematical formulation for the progressive injection phase condition that is argued qualitatively in [27].

$$\frac{m_1 + m_2}{M} = \frac{nd}{N} \tag{4.7}$$

To simplify the analysis, we consider only the lowest order intermodulation product and assume that all the other components of the injection current can be neglected. Using this assumption, (4.6) can be simplified to (4.8). The parameters $h_{R,i}$ H_R, $g_{R,o}$, and $C_{R,g}$ are equivalent to the same parameters without the subscript 'R' in the free running MPRO. These are given by $h_{R,i}=h_i \times \alpha_{i,0}$, $H_R = \sum_{i=0}^{N} h_i \alpha_{i,0}$, $g_{R,o}=g_o \times H/H_R$, and $C_{R,g}=C_g \times H/H_R$, respectively. The injection current amplitude is given by (4.9) where $\alpha_{i,1}= \alpha_i \times \lambda_1$ and λ_1 is the first Fourier coefficient of the time-domain modulation function.

$$\sum_{i=0}^{N} h_{R,i} g_{m,1} V_o \cos\left[\omega_o t - \frac{2\pi n(q-1)}{N} - \frac{2\pi n(i-1)}{N}\right]$$
$$+H_R g_{R,o} V_o \cos\left[\omega_o t - \frac{2\pi n(q-1)}{N}\right] - H_R C_{R,g} \omega_o V_o \sin\left[\omega_o t - \frac{2\pi n(q-1)}{N}\right] \quad (4.8)$$
$$= I_o \cos\left[\omega_o t - \frac{2\pi n(q-1)}{N} + \Psi\right]$$

$$I_o = \frac{\lambda_1}{2} H g_{m,(d-1)} V_o \left| \sum_{i=1}^{N} x_i \alpha_i \exp\left[j2\pi \left(\frac{m_1}{M} - \frac{n}{N} \right)(i-1) \right] \right| \quad (4.9)$$

Equation (4.8) describes the injection-locked MPRO (IL-MPRO) shown in Fig. 4.4. The unit inverter of this IL-MPRO has a transconductance $g_{m,1}$, an input capacitance $C_{R,g}$ and an output conductance $g_{R,o}$. The mode gain and the normalized free running frequency of the equivalent MPRO without injection are given by (4.10) and (4.11), respectively where $x_{R,i}=h_{R,i}/H_R$. The injection current at the i^{th} node of the IL-MPRO is given by (4.12) where I_o is expressed by (4.9). The substitution $\Psi=\tan^{-1}(\omega_{R,n}\tau)+\theta$ is made for convenience since it makes the arbitrary phase shift θ equal to zero when the locking frequency is equal to the free running frequency of the equivalent core oscillator.

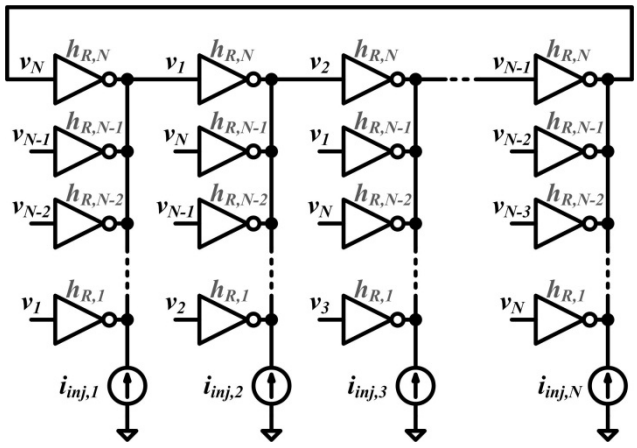


Fig. 4.4. Equivalent injection-locked MPRO model.

$$a_{R,n} = \frac{1}{-\sum_{i=1}^{N} x_{R,i} \cos\left[\frac{2\pi n(i-1)}{N}\right]} \tag{4.10}$$

$$\omega_{R,n}\tau = \frac{\sum_{i=1}^{N} x_{R,i} \sin\left[\frac{2\pi n(i-1)}{N}\right]}{-\sum_{i=1}^{N} x_{R,i} \cos\left[\frac{2\pi n(i-1)}{N}\right]} \tag{4.11}$$

$$i_{inj,i}(t) = I_o \cos\left(\omega_o t - \frac{2\pi n(i-1)}{N} + \tan^{-1}(\omega_{R,n}\tau) + \theta\right) \tag{4.12}$$

Equations (4.7)-(4.12) represent the mathematical model we use for the SHIL-MPRO analysis. We use this model in the next section to calculate the locking range of a SHIL-MPRO.

4.2. Locking Ranges

Fig. 4.5 shows a phasor diagram for an injection-locked MPRO at lock. The current I_g is the amplitude of the total transconductance current injected *into* a certain node v_q. This current is given by (4.13) where the negative sign in the first line indicates the current direction out of the transconductors. The total current injected into the oscillator node I_T can be decomposed into a resistive component $I_{T,R}$ that is in phase with the node voltage and an orthogonal capacitive component $I_{T,C}$. The total transconductance current I_g has a phase shift of $\tan^{-1}(\omega_{R,n}\tau)$ compared to the resistive current. For the oscillator to be locked at a frequency ω_o, the total current I_T must have a phase shift $\tan^{-1}(\omega_o\tau)$ with respect to the resistive current. The extra phase shift, $\varphi = \tan^{-1}(\omega_o\tau) - \tan^{-1}(\omega_{R,n}\tau)$, must be provided by the injection current. The angle θ is greater than or less than zero depending on whether the injection frequency is greater than or less than the free running frequency of the equivalent MPRO, respectively.

$$
\begin{aligned}
i_{g,q}(t) &= -\sum_{i=1}^{N} g_{m,1} V_o h_{R,i} \cos\left(\omega_o t - \frac{2\pi n(q-1)}{N} - \frac{2\pi n(i-1)}{N} \right) \\
&= \frac{H_R g_{m,1} V_o}{a_{R,n}} \sqrt{1+(\omega_{R,n}\tau)^2} \cos\left(\omega_o t - \frac{2\pi n(q-1)}{N} + \tan^{-1}(\omega_{R,n}\tau) \right) \\
&= I_g \cos\left(\omega_o t - \frac{2\pi n(q-1)}{N} + \tan^{-1}(\omega_{R,n}\tau) \right)
\end{aligned}
\tag{4.13}
$$

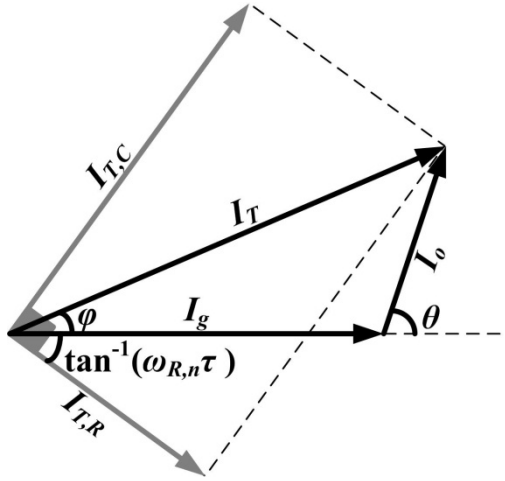


Fig. 4.5. Phasor diagram for an injection-locked MPRO at lock

The gain and phase conditions for locking can be derived from (4.8) by separating the $\cos[\omega_o t - 2\pi n(q-1)/N]$ and $\sin[\omega_o t - 2\pi n(q-1)/N]$ coefficients. Equation (4.14) gives the equivalent *dc* gain of the unit inverter at lock and (4.15) gives the phase condition from which the value of the angle θ can be calculated. The injection coefficient η is defined in (4.16) where the value of the injection current derived in (4.9) is used.

$$
a_n = \frac{a_{R,n}}{1+\eta\cos\left[\tan^{-1}(\omega_{R,n}\tau)+\theta\right]} \tag{4.14}
$$

$$
(\omega_o\tau) = \frac{(\omega_{R,n}\tau)+\eta\sin\left[\tan^{-1}(\omega_{R,n}\tau)+\theta\right]}{1+\eta\cos\left[\tan^{-1}(\omega_{R,n}\tau)+\theta\right]} \tag{4.15}
$$

$$\begin{aligned}\eta &= \frac{I_o}{I_g}\sqrt{1+\left(\omega_{R,n}\tau\right)^2} \\ &= \frac{a_{R,n}I_o}{H_R g_{m,1} V_o} \\ &= \frac{\lambda_1}{2}\times a_{R,n}\times\left(\frac{H}{H_R}\right)\times\left(\frac{g_{m,(d-1)}}{g_{m,1}}\right)\times\left|\sum_{i=1}^{N} x_i\alpha_i \exp\left[j2\pi\left(\frac{m_1}{M}-\frac{n}{N}\right)(i-1)\right]\right|\end{aligned} \tag{4.16}$$

In the remainder of this section, we derive expressions for the different possible limitations on the locking range.

4.2.1. Phase-Limited Locking Range

The first limitation on the locking range is due to the maximum phase shift $\pm\varphi_{\max}$ that can be caused by the injection current. This limitation defines the phase-limited locking range (PLLR) [22]. Fig. 4.6 shows the phasor diagram of the IL-MPRO at the edge of the PLLR. An expression of the maximum and minimum locking frequencies due to the PLLR can be derived from the figure trigonometry or by differentiating equation (4.15) with respect to θ. The PLLR expression is given by (4.17) where η is the injection coefficient defined in (4.16).

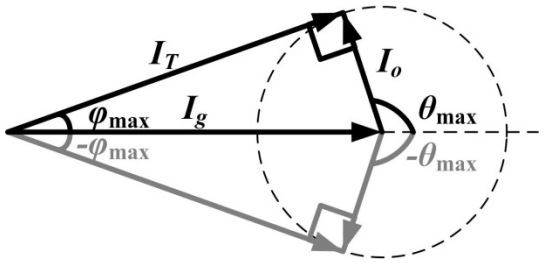


Fig. 4.6. Phasor diagram for an IL-MPRO at the edge of the phase-limited locking range.

$$\left(\omega_o\tau\right)_{PLLR(\max/\min)} = \frac{\left(\omega_{R,n}\tau\right)\pm\eta\sqrt{1-\eta^2+\left(\omega_{R,n}\tau\right)^2}}{1-\eta^2} \tag{4.17}$$

Fig. 4.7 is a plot of the PLLR expression in (4.17) as a function of the injection coefficient η for different values of the normalized free-running frequency ($\omega_{R,n}\tau$). As the figure shows, for

small values of η, the locking range is a narrow range around the oscillator free running frequency. As the injection strength increases, the locking range starts to increase. This behavior is characteristic for weak injection and is explained in various previous publications as in [22]. However, as Fig. 4.7 shows, as the injection strength increases, the lower end of the PLLR approaches zero while the upper end increases significantly until it tends to infinity when η approaches unity. In practice, no matter how strong the injection level is, the locking range can never tend to infinity which suggests the existence of additional limitations on the locking range of a divider.

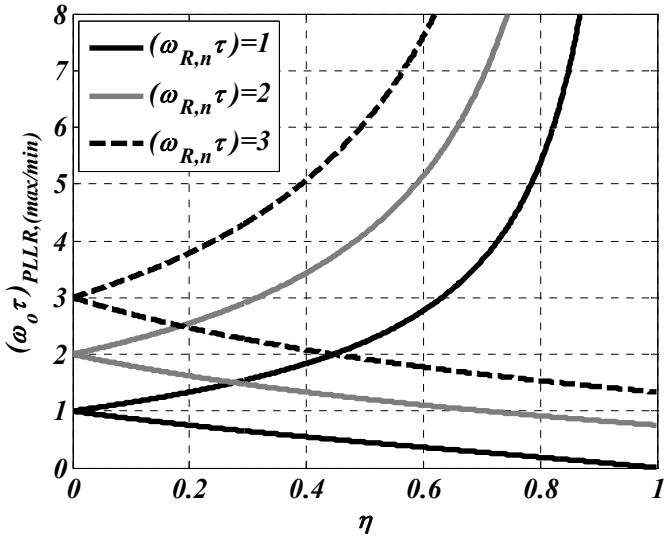


Fig. 4.7. Phase-limited locking range.

4.2.2. Gain-Limited Locking Range

The second limitation on the locking range arises from the gain condition in (4.14). For locking to occur, the available *dc* gain of the inverters of the equivalent MPRO must be greater than the value given by (4.14). Otherwise, the oscillator cannot be locked. This limitation defines the gain-limited locking range (GLLR). An expression for the GLLR can be derived from (4.14)

and (4.15) and is given by (4.18). The parameter $a_{\max}$ is the maximum allowed mode gain for the IL-MPRO at lock (4.14) while $a_{R,n}$ is the mode gain of the equivalent free running MPRO (4.10). For our argument in this subsection, $a_{\max}$ is the small signal *dc* gain of the inverters of the equivalent MPRO and is equal to $(H_R/H)\times a_o$ where a_o is the small signal *dc* gain of the actual inverters without switching.

$$\left(\omega_o\tau\right)_{GLLR/MLLR(\max)} = \left(\frac{a_{\max}}{a_{R,n}}\right)\left[\left(\omega_{R,n}\tau\right) + \sqrt{\eta^2 - \left(1 - \frac{a_{R,n}}{a_{\max}}\right)^2}\right] \tag{4.18}$$

For a certain value of $(a_{\max}/a_{R,n})$, the upper end of the locking range becomes gain-limited only when the injection coefficient, η, exceeds a certain threshold, η_g, given by (4.19). At this value, both the PLLR and the GLLR have the same upper bound. When η exceeds this value, the GLLR becomes the limit for the maximum locking frequency. The lower end of the locking range is always phase-limited as long as $a_{\max}\geq a_{R,n}$ which is the practical case of interest.

$$\eta_g = \sqrt{1 - \left(\frac{a_{R,n}}{a_{\max}}\right) + \frac{\left(\omega_{R,n}\tau\right)^2}{2} - \left(\omega_{R,n}\tau\right)\sqrt{\frac{\left(\omega_{R,n}\tau\right)^2}{4} + \left(\frac{a_{R,n}}{a_{\max}}\right)\left[1 - \left(\frac{a_{R,n}}{a_{\max}}\right)\right]}} \tag{4.19}$$

Fig. 4.8 shows a plot of the GLLR given by (4.18) for $(\omega_{R,n}\tau)$=2 and $(a_{\max}/a_{R,n})$= 1, 2, and 3. As the figure shows, for small values of η, the locking range is phase limited. When η exceeds the value of η_g, the maximum locking frequency becomes gain-limited. The limit increases when the maximum available gain increases.

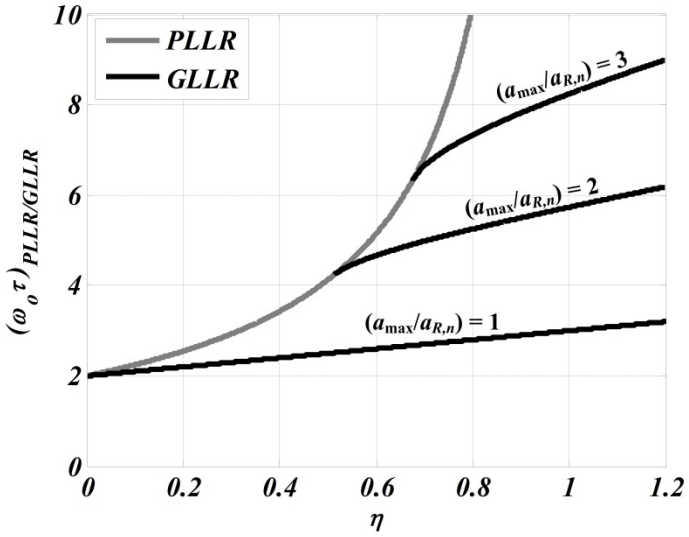


Fig. 4.8. Gain-limited locking range for an IL-MPRO with (ωR,nτ)=2 and (amax/aR,n) = 1, 2, and 3

4.2.3. Mode-Limited Locking Range

The third limitation on the locking range arises for the existence of other possible modes of oscillation for the MPRO. If the mode gain of the IL-MPRO (4.14) is higher than any of the mode gains of the equivalent free running oscillator (4.10), this oscillation mode is able to build up and the lock is lost. This limitation defines the mode-limited locking range (MLLR).

An expression for the MLLR is identical to that for GLLR if we define the maximum possible mode gain a_{max} as the minimum non-dominant mode gain. In general, equation (4.18) expresses both the GLLR and the MLLR when a_{max} is defined as given by (4.20).

$$a_{\max} = \min\left\{\left(\frac{H_g}{H}\right)\times a_o, \min_{\substack{l=0,1,\ldots,N-1 \\ l\neq n}}\left[a_{R,l} > 0\right]\right\} \tag{4.20}$$

4.2.4. Quadrature-Phase Divider Example

In this subsection, we compare our analysis with simulation. A simple quadrature-phase divide-by-2 is used in this example. In the simulations, we use the unit cell shown in Fig. 4.9. It consists of differential CMOS inverters switched at the common source nodes of both the NMOS and the PMOS transistors. The clock signal is assumed to be strong enough to turn off the current path when it is in *low* state. Accordingly, the time modulation function is assumed to be a 50% duty cycle square wave with an average λ_0=0.5 and a first harmonic component $\lambda_1=2/\pi$. When a certain cell is not clocked, this means that CK=V_{DD} at all times. The *dc* gain of the unswitched inverter for V_{DD}=1V in 65nm CMOS technology is equal to 8. The clock signal is a rail-to-rail square-wave with 10% rise and fall time. The simulated maximum division frequency shown in this section is for the unloaded divider which represents the absolute maximum frequency a divider can work at. The effect of loading is discussed in the next section.

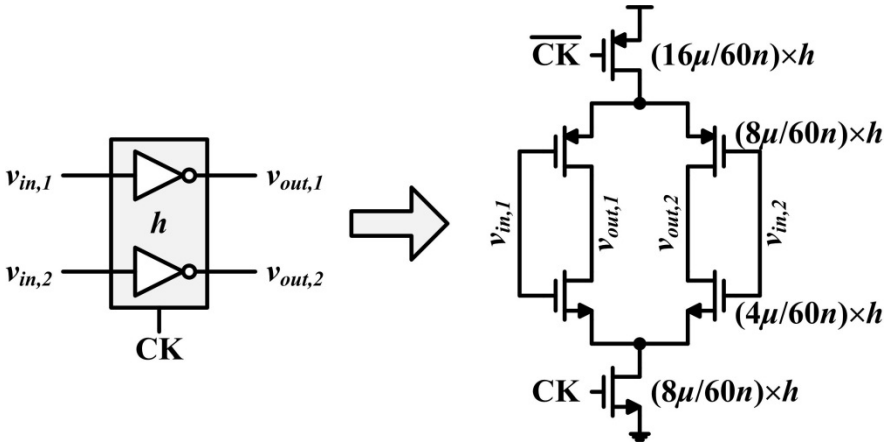


Fig. 4.9. Unit switched inverters used in simulation.

Fig. 4.10 shows the schematic of a quadrature phase (N=4) SHIL-MPRO. The sizing factors of the feed-forward and cross-coupling inverters are (h_4,h_3)=(h,1). The equivalent MPRO has two distinct oscillation modes, n=3 is the desired mode and n=2 is an undesired mode. Assuming

the maximum number of distinct input phases is M=4, the input clock phases must satisfy the condition (m_1+m_2)=6 (4.7).

Table 4.1 shows all the allowed clocking configurations that satisfy equation (4.7). The table also shows all the quantities needed to calculate the three locking ranges as a function of the sizing ratio, h.

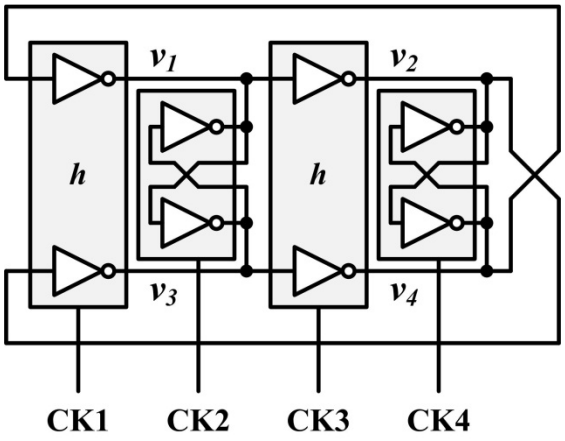


Fig. 4.10. Quadrature output divide-by-2.

Table 4.1. Possible clocking configurations for a quadrature-phase divide-by-2 shil-mpro

Index	(α_4,α_3)	m_1	CK1	CK2	CK3	CK4	$a_{R,3}$	$a_{R,2}$	$\omega_{R,3}\tau$	η	h_{GM}
1	(0,1)	X	V_{DD}	0º	V_{DD}	180º	$1+\frac{h}{\lambda_0}$	$\frac{h+\lambda_0}{h-\lambda_0}$	$\frac{h}{\lambda_0}$	$\frac{\lambda_1}{2\lambda_0}$	$\frac{\lambda_0 a_0+1}{a_0-1}=0.71$
2	(1,0)	X	0º	V_{DD}	180º	V_{DD}	$1+\lambda_0 h$	$\frac{h\lambda_0+1}{h\lambda_0-1}$	$\lambda_0 h$	$\frac{\lambda_1}{2}\cdot h$	$\frac{a_0+1}{\lambda_0 a_0-1}=3$
3	(1,1)	0	0º	180º	180º	0º	$1+h$	$\frac{h+1}{h-1}$	h	$\frac{\lambda_1}{2\lambda_0}\cdot\sqrt{h^2+1}$	$\frac{\lambda_0 a_0+1}{\lambda_0 a_0-1}=1.67$
4	(1,1)	1	0º	90º	180º	-90º	$1+h$	$\frac{h+1}{h-1}$	h	$\frac{\lambda_1}{2\lambda_0}\cdot\lvert h-1\rvert$	$\frac{\lambda_0 a_0+1}{\lambda_0 a_0-1}=1.67$
5	(1,1)	2	0º	0º	180º	180º	$1+h$	$\frac{h+1}{h-1}$	h	$\frac{\lambda_1}{2\lambda_0}\cdot\sqrt{h^2+1}$	$\frac{\lambda_0 a_0+1}{\lambda_0 a_0-1}=1.67$
6	(1,1)	3	0º	-90º	180º	90º	$1+h$	$\frac{h+1}{h-1}$	h	$\frac{\lambda_1}{2\lambda_0}\cdot(h+1)$	$\frac{\lambda_0 a_0+1}{\lambda_0 a_0-1}=1.67$

Fig. 4.11 shows the normalized maximum locking frequency $(\omega_o\tau)_{\max}$ for the 6 clocking configurations, calculated by substituting the values in Table 4.1 into (4.17–4.20), and the maximum locking input frequency obtained by simulation. For the six configurations, at small

values of h, the free running frequency, ($\omega_{R,3}\tau$), is small and thus the MPRO mode gain, $a_{R,n}$, and the IL-MPRO mode gain, a_n, are both smaller than the maximum available *dc* gain. This causes the locking range to be phase limited. As the value of h increases, the value of a_n at the edge of the PLLR exceeds the available *dc* gain. Accordingly, the locking range becomes gain limited. As h increases further, the value of the non-dominant mode gain, $a_{R,2}$, decreases below the available *dc* gain. This decrease in the non-dominant mode-gain casuses locking range to be mode limited. For a 4-phase SHIL-MPRO using this particular unit cell (a_o=8), the maximum locking frequency occurs at the intersection of the GLLR and the MLLR. The value of the sizing ratio that satisfies this condition, h_{GM}, is calculated for each clocking configuration in the last column in Table 4.1.

Fig. 4.11 shows that the optimum sizing ratio for maximizing the upper limit of the locking range can be predicted with good accuracy. Note that while the sizing factor of the maximum is accurate, the plot shows some discrepancy in the magnitude or shape of the curves. The discrepancy is expected because the normalizing time constant, τ, for an MPRO is a function of the mode-gain. Accordingly for a SHIL-MPRO, τ is a function of the sizing parameters and injection strength (4.14). Meanwhile, the theoretical calculation uses a constant τ for normalization.

When the SHIL-MPRO is sized to maximize the upper end of the locking range, (4.9) indicates that the equivalent injection current is large. Coupled with the low quality factor of ring oscillators, the oscillator has a locking range that extends down to low frequencies and is sufficient for most practical applications. A more detailed application of this model is presented in Section 4.4.

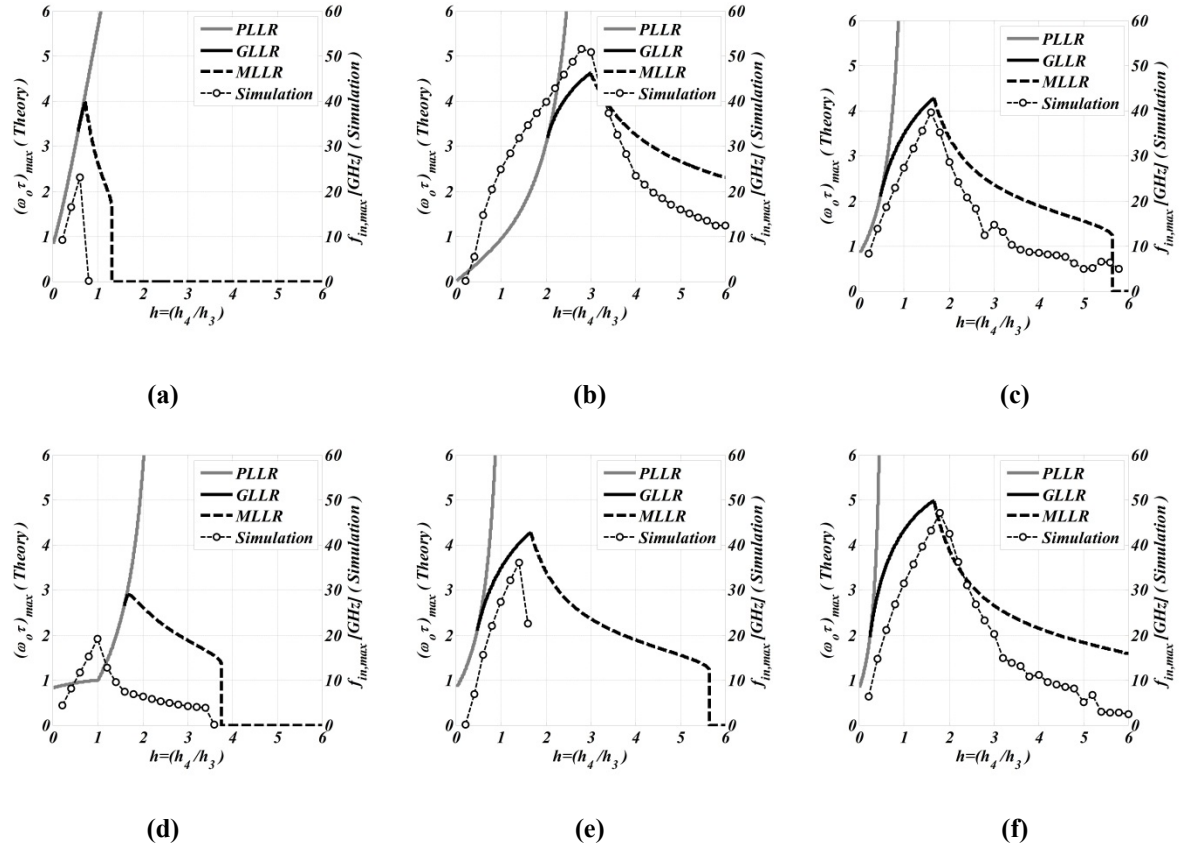


Fig. 4.11. Theoretical normalized maximum locking frequency and simulated maximum locking frequency for an unloaded quadrature divide-by-2. (a) to (f) refer to the six clocking configurations in Table 4.1 respectively

4.3. Power Consumption and Effect of Loading

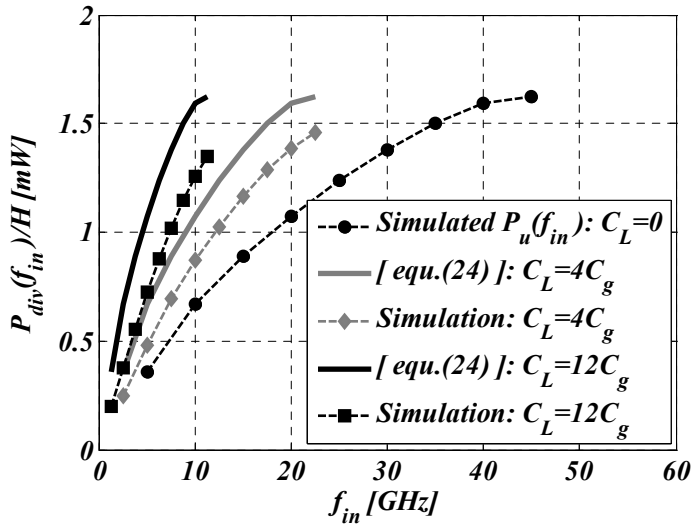
To study the effect of loading, we first consider an arbitrary unloaded SHIL-MPRO with a locking range between f_L and f_H and with sizing factors $\{h_i\}$ where $H = \sum_{i=1}^{N} h_i$. For a fixed supply voltage, the power consumption of this unloaded divider at lock is $P_d(f)$. The power is only a function of the injection frequency, $f_L \leq f \leq f_H$. The self-loading capacitance of this divider at each of its outputs is equal to HC_g where C_g is the equivalent input capacitance of the unit inverter as defined before. The exact form of the function $P_d(f)$ depends on the design of the unit inverter

and the divider architecture and is in general due to both the switching and the direct-path currents.

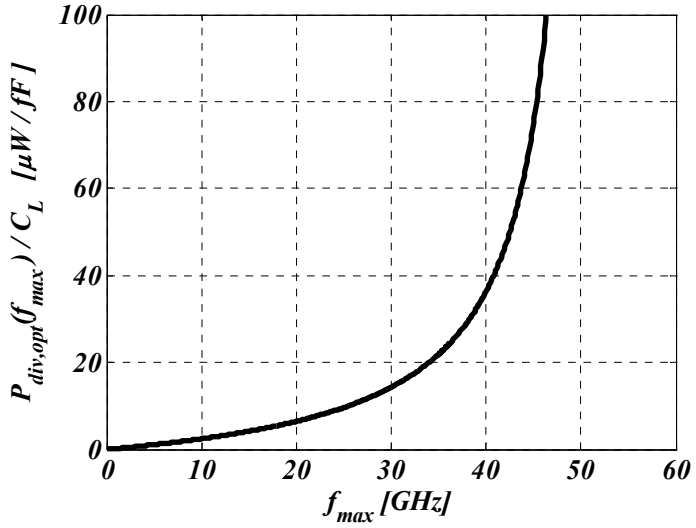
If the whole unloaded divider is scaled with a factor K_d, the power consumption of the scaled divider becomes $K_d P_d(f)$ where $f_L \le f \le f_H$. If the scaled divider outputs are uniformly loaded with a capacitance C_L at each node, the divider behavior as a function of frequency scales in the frequency axis by a factor $(K_d HC_g+C_L)/(K_d HC_g)$. Note that the RC ring-type ILO behavior is always dependent on the normalized variable ($\omega_o \tau$) rather than the absolute frequency. The power consumption of the loaded scaled divider can be expressed by (4.21). Fig. 4.12(a) shows an example for the frequency scaling due to loading. The figure shows the simulated power consumption of the quadrature divider of Fig. 4.10 as a function of the injection frequency for topology 2 in Table 4.1 which corresponds to Fig. 4.11(b). The divider uses the unit cell of Fig. 4.9 and has a sizing vector $(h_4,h_3) = (3,1)$.

$$P_{div}(f) = K_d \times P_d\left(\frac{K_d HC_g + C_L}{K_d HC_g} f\right) \text{; where } \frac{K_d HC_g}{K_d HC_g + C_L} f_L \le f \le \frac{K_d HC_g}{K_d HC_g + C_L} f_H \qquad (4.21)$$

To minimize power consumption, a divider must be scaled with the minimum scaling factor K_d that still achieves the desired maximum operation frequency $f_{max} \le f_H$. This optimal scaling factor and the corresponding power consumption can be expressed as (4.22) and (4.23) respectively. In (4.23), $P_u(f_H)$ is the power consumption of a unit unloaded divider with a total sizing factor H=1 at its maximum locking frequency f_H and is equal to $P_d(f_H)/H$. In practice, the frequency f_H should be chosen less than the actual maximum locking frequency by a factor large enough to guarantee the divider achieves the desired frequency over all PVT variations.



(a)



(b)

Fig. 4.12. Power consumption of a quadrature divider with sizing factors (h_4,h_3)=(3,1) and clocking configuration (α_4,α_3)=(1,0) (a) As a function of input frequency for different load capacitances (b) As a function of the maximum desired division frequency when the divider is scaled optimally.

$$K_{d,\min} = \frac{C_L}{HC_g}\frac{f_{\max}}{f_H - f_{\max}} \quad ; \; f_{\max} < f_H \tag{4.22}$$

$$P_{div,opt}(f_{\max}) = \left(\frac{f_{\max}}{f_H - f_{\max}}\right) \times \frac{P_d(f_H)}{HC_g} \times C_L = \left(\frac{f_{\max}}{f_H - f_{\max}}\right) \times \frac{P_u(f_H)}{C_g} \times C_L \quad (4.23)$$

Fig. 4.12(b) is a plot of equation (4.23) where C_g=160fF for our unit cell in Fig. 4.9. If the divider is always scaled for minimum power, the power consumption is always proportional to the load capacitance. At frequencies that are small compared to f_H, the power is proportional to the maximum desired input frequency. As the input frequency approaches the maximum injection frequency of the unloaded divider, f_H, the required power increases rapidly with frequency since the divider has to be scaled up in size to the limit where the external load becomes small enough compared to its self-loading capacitance.

The analysis, in this section, shows that maximizing the maximum locking frequency of the unloaded divider is useful even when a divider does not need to operate at such high locking frequency since the divider can then be scaled down in size and save power compared to an un-optimized design.

4.4. Design Procedure

The mathematical model we derived in equations (4.7) through (4.20) can be used in an optimization algorithm to find the optimum design. Fig. 4.13 shows a flow chart indicating the proposed design procedure. In step A, we set the required initial parameters like the number of input and output phases, the inverter *dc* gain, the range of sizing factors to search, and the characteristics of the time-domain modulation function. We use these parameters in step B to form the design space grid. This grid consists of all the possible sizing factors, oscillation modes, and clocking configurations. We limit the number of signal paths per stage to a maximum of 3

paths. In general, if the maximum frequency required cannot be achieved using 3-paths, then the maximum number of paths should be increased and the search should be repeated. However, it should be noted that in practice, as the number of paths increases, the layout design of the divider becomes more complicated and the benefit obtained from using more paths starts to diminish.

In step C, we exclude the undesired solutions from the grid before the actual computation of the maximum locking frequency. These solutions include those that contain any two branches, i and $i+N/2$ since they have opposite phases. We also exclude all the modes that do not lead to distinctive output phases. These are the modes that do not satisfy the condition $gcd(n,N)=1$ where $gcd()$ is the greatest common divisor of two integers. We finally exclude all the solutions that contain ambiguity in the output phases.

In step D, we use (4.16-4.20) to calculate the maximum locking frequency for all the remaining solutions in the design space. We sort these solutions in step E into three groups according to the number of clocked branches. We then sort the solutions in each group in descending order according to the maximum locking frequency. Finally in step F, we select the best solution and plot its maximum locking frequency as a function of the sizing factors and compare that to simulation. Since we do not have to examine all the possible combinations, the design time is reduced significantly.

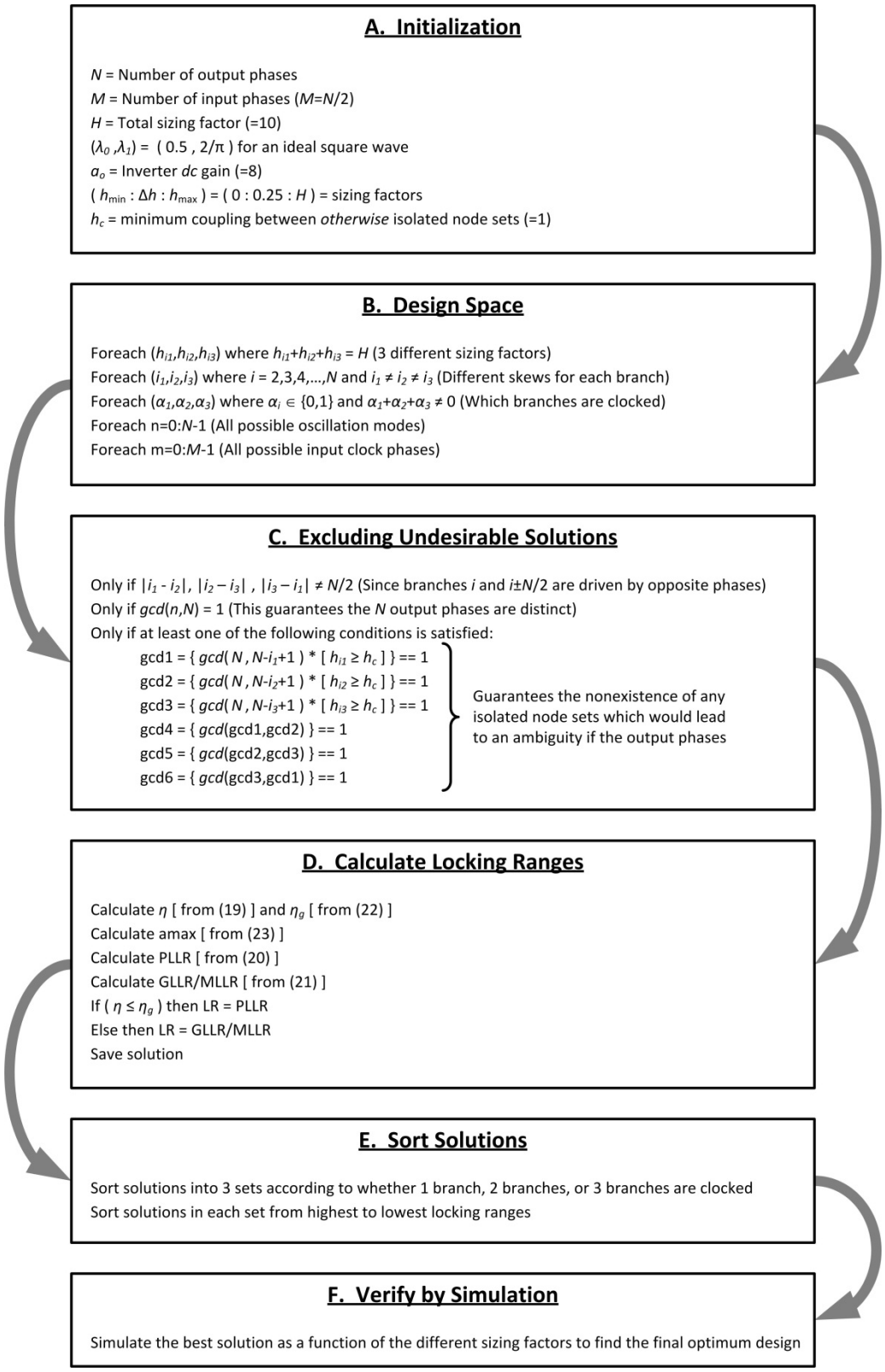


Fig. 4.13. Flow chart indicating the design procedure of a SHIL-MPRO divide-by-2.

4.5. Octal-Phase Divider

In this section, we apply our procedure to design a quadrature-phase input, octal-phase output divide-by-2. This divider is the first stage of a divider chain used to generate the clock signals required by a high speed serializing transmitter which is explained in the next chapter. The initial parameters for this design are N=8, M=4, in addition to the other parameters given in step A in Fig. 4.13. The design space formed in step B includes three different kinds of architectures as shown in Fig. 4.14. Each of these architectures can have different clocking configurations where we only show the one where one branch is clocked. The first architecture in Fig. 4.14(a) uses two separate differential-input quadrature-output dividers with a 90^o phase shift between their input clock phases. The advantage of this realization is that the maximum division frequency is equal to that of a quadrature divider. However, due to the symmetry of the divider, this architecture suffers from 180^o ambiguity in the phase relationship between the outputs of the two dividers. As part of step C, this ambiguity cannot be tolerated in most applications where the sampling phases have to be predictable and accordingly it is eliminated from consideration. In general, this condition can be identified whenever there exist isolated node sets in the divider.

Fig. 4.14(b) shows a second architecture where 4 cross-coupled latches are clocked with the quadrature input clock to produce 8 phases at half the input frequency. This approach does not suffer any phase ambiguity but our analysis, in addition to common practice, indicates that the maximum division frequency is roughly half that of a 2-latch-based quadrature divider.

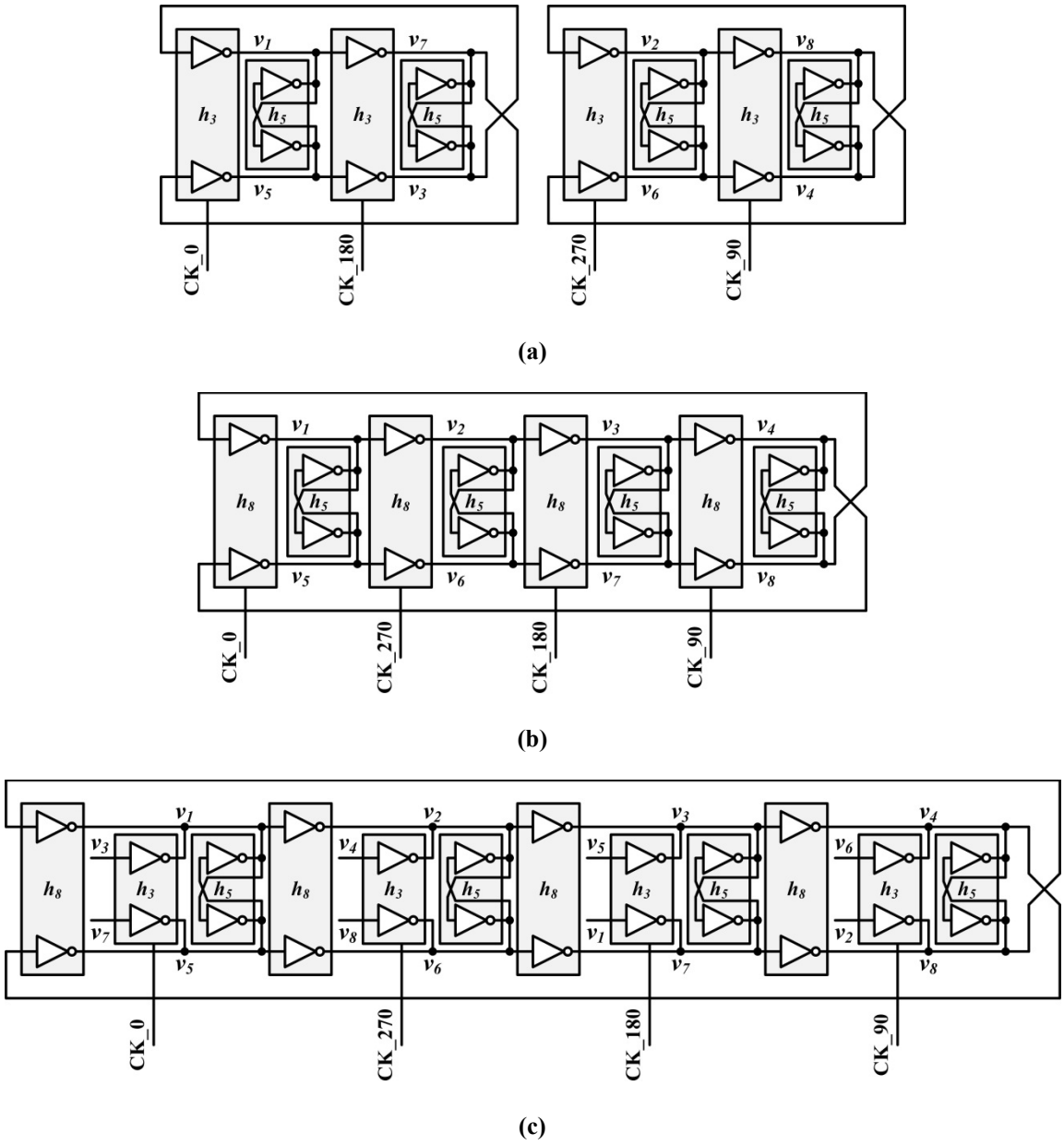


Fig. 4.14. Quadrature-phase input, octal-phase output divide-by-2 with three possible implementations as (a) Two separate differential-input quadrature-output dividers (b) Conventional 4 latches in a single loop and (c) Triple-path SHIL-MPRO.

Fig. 4.14(c) shows a third realization as a triple-path SHIL-MPRO. If the coupling structure and clocking configuration of this realization are optimized, the design can achieve a maximum division frequency that is equal to that of a quadrature divider. At the same time, since the design has no isolated node sets, it does not suffer any phase ambiguity. In fact, one can see that the

third realization is a general case that reduces to the first one if h_8=0 and to the second one if h_3=0. In general, a quad-path SHIL-MPRO can also be used and the maximum division frequency in that case can theoretically be even higher than a quadrature-divider. However, the increased layout complexity practically limits the performance improvement. Accordingly, a three-paths-per-stage architecture is chosen.

We used our model in the search algorithm to examine all the possible triple-path implementations and find the best coupling structure and clocking configuration (steps D and E). Fig. 4.15 shows the simulation results for the triple-path octal-phase SHIL-MPRO in Fig. 4.14(c) where only the branch, h_3, is clocked (α_8,α_5,α_3) = (0,0,1). The figure shows the simulated and theoretical maximum locking frequencies as a function of the sizing factor, h_3, for different values of h_8. The value of h_5 is given by $h_5=H-h_8-h_3$ where H is arbitrarily taken equal to 10. The figure shows that our model can predict the optimum design with very good accuracy. By comparing Fig. 4.15 and Fig. 4.11, we see that the maximum locking frequency for the octal-phase divider is approximately the same as that for the quadrature one. This shows that using SHIL-MPROs, the maximum locking frequency and the number of output phases can be decoupled which is the same conclusion we reached for MPROs.

For the first stage in our divider chain, we use a triple-path SHIL-MPRO with (h_8,h_5,h_3)=(2,2,6) and (α_8,α_5,α_3)=(0,0,1). We scaled the design so as to minimize the power consumption while still meeting the maximum frequency target at the worst PVT case.

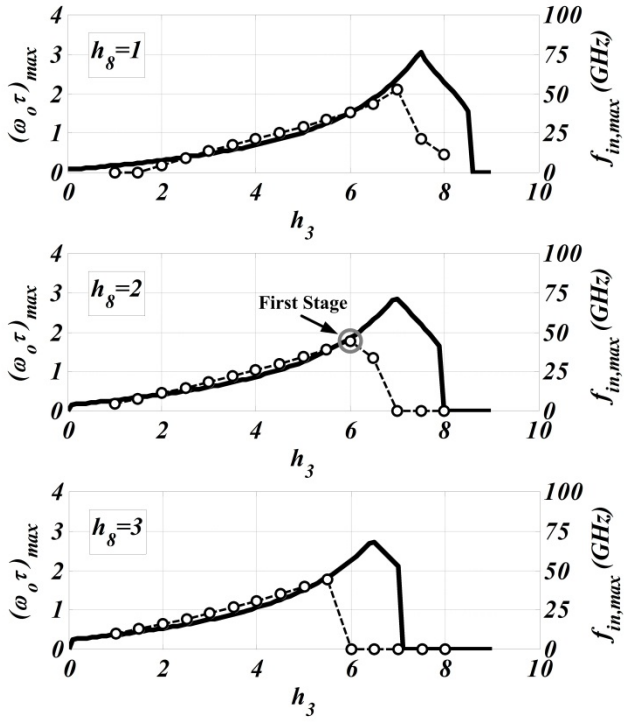


Fig. 4.15. Theoretical normalized (solid lines) and simulated (circles) maximum locking frequency for an unloaded triple-path octal-phase divide-by-2 for (α_8,α_5,α_3)=(0,0,1) and h_5=10-h_8-h_3

4.6. Hexadecimal-Phase Divider

The second stage in the divider chain used in our transmitter is an octal-phase-input, hexadecimal-phase output divide-by-2. Similar to the previous design, different implementations are possible. Using the same design procedure, we chose a triple-path SHIL-MPRO with (h_{16},h_9,h_7)=(2,2,6). Fig. 4.16 shows the clocking configuration and coupling structure.

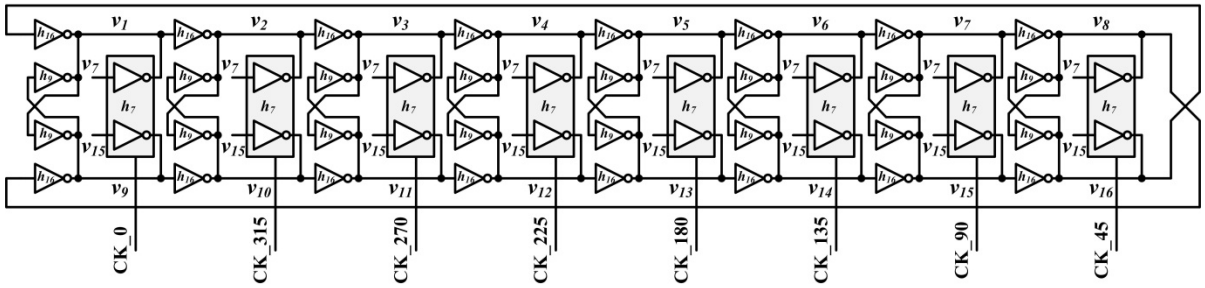


Fig. 4.16. Octal-phase input, hexadecimal-phase output divide-by-2 as a triple-path SHIL-MPRO

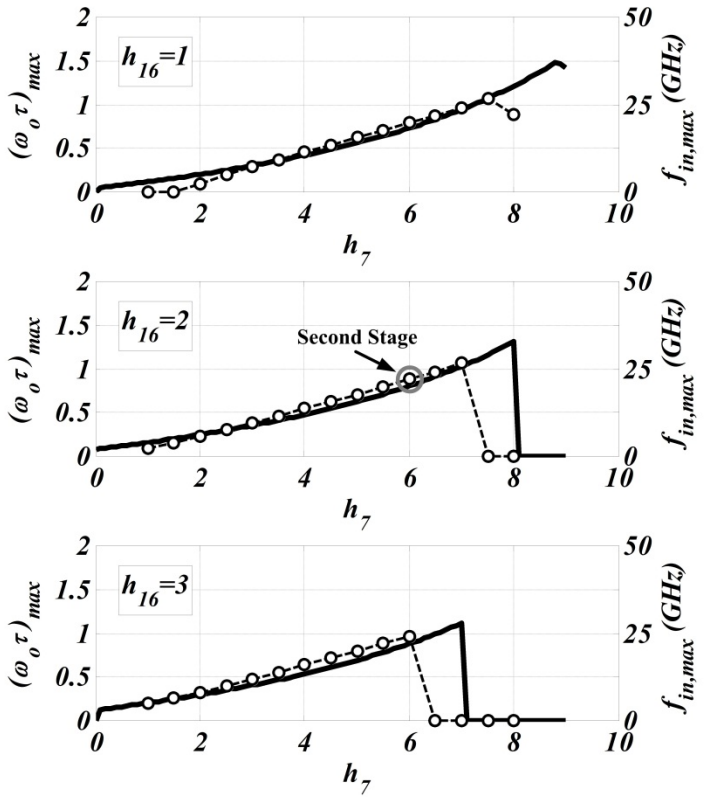


Fig. 4.17. Theoretical normalized (solid lines) and simulated (circles) maximum locking frequency for an unloaded triple-path hexadecimal-phase divide-by-2 for $(\alpha_{16},\alpha_9,\alpha_7)$=(0,0,1) and h_9=10-h_{16}-h_7

Fig. 4.17 shows that the simulation results for the selected architecture have good agreement with the analytical model. The maximum frequency of the 16-phase triple-path SHIL-MPRO is approximately half that of the 8-phase design. This is acceptable for our case since it does operate at half the frequency of the octal-phase divider. However, if a higher maximum speed is needed, 4 or more paths per stage should be used at the cost of a more complicated layout.

4.7. Conclusion

We propose in this chapter a comprehensive analysis and model for superharmonic injection-locked multipath ring oscillators. The analysis shows that SHIL-MPROs inherit the property of

MPROs such that one can increase the number of output phases without penalizing the maximum division frequency. We explain three different limitations that determine the maximum locking range of the frequency divider: phase (PLLR), gain (GLLR), and oscillation mode (MLLR). The PLLR corresponds to the maximum phase shift that an equivalent injection current can cause. The GLLR corresponds to the finite *dc* gain of the inverters forming the divider. And the MLLR corresponds to the existence of other non-dominant oscillation modes that at some point can become dominant and prevent the SHIL-MPRO from locking in the desired mode. We derive expressions for each of these three limitations on locking ranges as functions of the sizing factors and input clock distribution. These expressions can be used in a design procedure to find the optimum coupling structure and clocking configuration that maximizes the locking frequency of the divider. We also explain the effect of loading the divider with an external capacitive load and show that maximizing the locking frequency can be used to save power if the divider is then operated at a lower frequency. The design procedure can be used for a wide range of applications for any ring-oscillator based divider.

The next chapter describes the detail implementation of a serial link transmitter that uses the dividers presented in Section 4.5 and 4.6 to achieve low area and power for the data serialization.

CHAPTER 5

A 32-48 Gb/s Serial Link Transmitter

The ability to achieve frequency division with multiple phases at relatively high frequency is used to relax the timing requirements of the serializer hence allowing us to eliminate the need for any delay calibration loops. This chapter applies this idea to a serial-link transmitter. We first explain the system design of the transmitter in the first section and then give the details of the circuit design in Section 5.2.

5.1. Transmitter System Design

Fig. 5.1 shows a block diagram of a serializing transmitter. The data path consists of a 64-to-1 serializer followed by a two-stage driver. The sampling clock signals required for the different serializer stages are generated from a charge-pump phase-locked loop. An *LC*-VCO drives the final *N*:1 multiplexer with an *N*-phase clock at a frequency f_o/N where f_o is the final bit rate. The VCO clock is then divided by a chain of frequency-dividers to generate the lower frequency clock signals required by the 64:*N* multiplexing stages.

To minimize the chip area of the transmitter, the use of inductors has been restricted only to the VCO, the final multiplexing stage, and the following pre-driver and driver. All the other multiplexing stages in addition to the whole frequency-divider chain are to be designed in CMOS. In addition, to avoid the overhead added by delay-calibration loops or delay matching buffers, the serializer must have a wide enough operation range to guarantee the timing constraints are met for the desired data rate over all PVT corners.

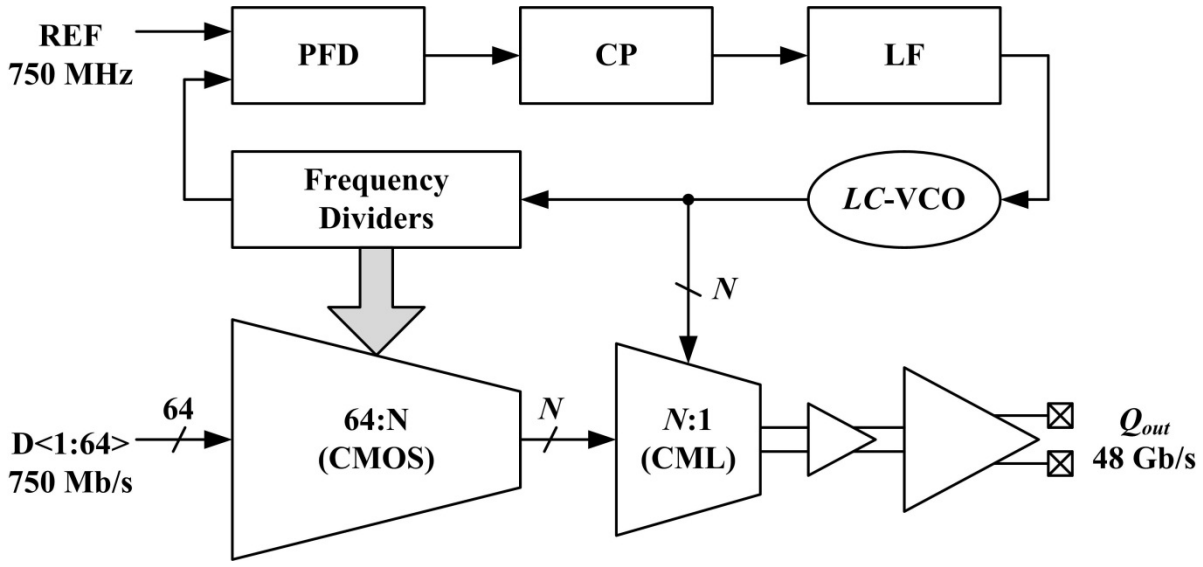


Fig. 5.1. Block-diagram of a 64-to-1 serializing transmitter.

In the following subsections, we explain the different architectural choices that we made to arrive at the proposed architecture.

5.1.1. Final Multiplexing Stage Order

As explained in Chapter 2, as the order of the final multiplexer (N) increases, the timing constraints at the final multiplexing stage become more relaxed. However, this has two drawbacks. First, higher order multiplexers suffer lower bandwidth which means higher power consumption to meet a certain target data rate. On the other hand, as N increases, the VCO output frequency decreases which lowers the power consumption requirements of the divider chain as explained in Chapter 4. Accordingly, to select the value of N that minimizes the total power consumption, this trade-off has to be analyzed. The second problem is that when N increases, the output signal becomes more sensitive to phase mismatches in the multiphase VCO. In addition, if an *LC*-VCO is used, the number of inductors in the VCO increases increasing the chip area.

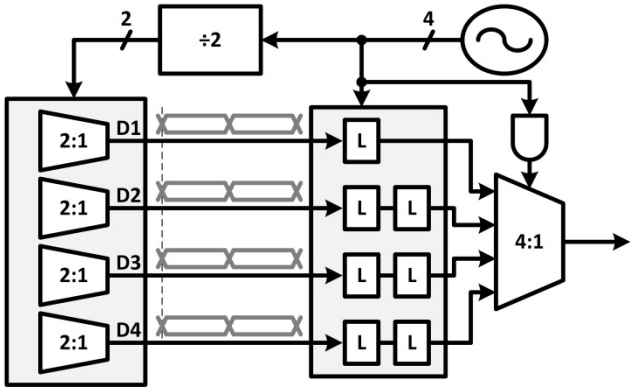
By investigating the power trade-off between the MUX and the clock dividers, we found that for the target data rate of ~40 Gb/s using 65-nm CMOS technology, a 4-to-1 MUX at the final stage is the best compromise. If a 2-to-1 MUX is used, the first divider has to be clocked by a ~20-GHz input clock which requires burning a lot of power if inductive peaking is to be avoided. On the other hand, if an 8-to-1 MUX is used, the power consumption required for the MUX to meet the bandwidth requirement becomes excessive. In addition, a 4-to-1 multiplexer was found to be a good compromise between relaxed timing constraints and phase-mismatch sensitivity.

5.1.2. Multiphase Sampling

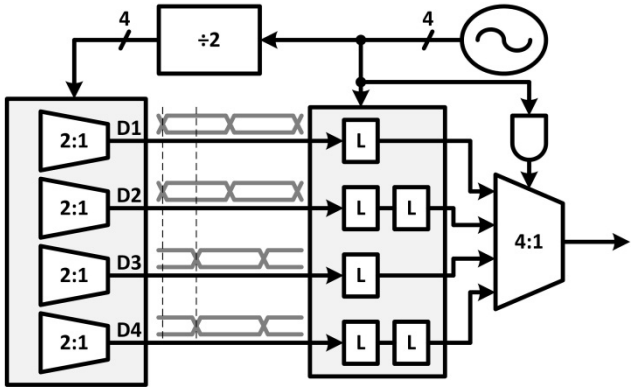
Another design trade-off is the number of phases in the divided clock signals. Fig. 5.2 shows the number of latches required to correctly retime the data input to the final 4:1 MUX. If the first divided clock has a differential phase, the 4 outputs of the preceding 8:4 stage will have transitions all at the same phase. Accordingly, the data has to be retimed before being applied to the 4:1 MUX. Fig. 5.2(a) shows a possible implementation where a minimum of 7 latches is required before the multiplexer. If the divided clock has a quadrature phase, the 4 data inputs will have 2 transition phases which relaxes the number of latches to a total of 6 latches as shown in Fig. 5.2(b). Finally, if the divided clock has 8 phases, the input data is already retimed and the number of latches required is reduces to 4 latches as shown in Fig. 5.2(c).

Fig. 5.2 shows that if we can generate 8 phases for the divided clock, power and area savings can be achieved by minimizing the required sampling elements at the input of the multiplexer. This approach can be applied to all stages of the serializer. In general, for any multiplexing stage, if the time resolution of the divided clock is equal to that of the input clock, the number of

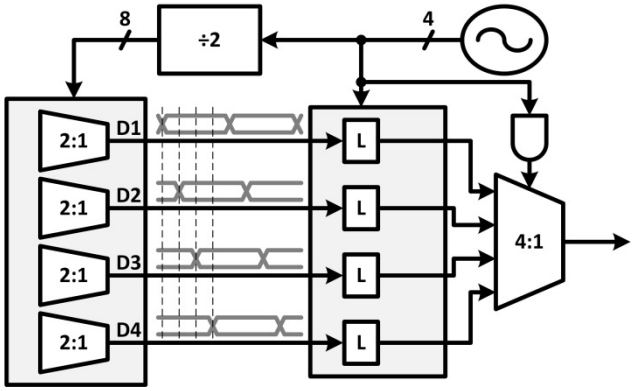
retiming elements can be minimized. Time resolution can be maintained if the number of phases of the divided clock is double that of the input clock.



(a)



(b)



(c)

Fig. 5.2. Required retiming elements at the input of the final 4-to-1 multiplexer when the divided clock has (a) Two phases. (b) Four phases. (c) Eight phases.

Based on the analysis in Chapter 4, multiphase dividers can be designed as superharmonic injection-locked multipath ring oscillators at no additional power cost.

5.1.3. Transmitter Architecture

Fig. 5.3 shows the proposed transmitter architecture. The transmitter consists of a 64:1 serializer followed by a two-stage driver. The final stage in the serializer is a 4:1 MUX that includes pulse generation and latching functionality. The required sampling clock signals are generated from a phase-locked loop. A quadrature phase *LC*-VCO generates 4 phases at 12 GHz that directly drive the final MUX and the first frequency divider. High speed, low power frequency dividers are realized as superharmonic injection-locked multipath ring oscillators. The dividers generate 8 phases at 6 GHz, 16 phases at 3 GHz, 8 phases at 1.5 GHz, and 16 phases at 750 MHz.

Since the number of phases at the output of each of the first and the second dividers is double the number of phases at their inputs, the number of latches at the input of the 8:4 MUX and the 4:1 MUX can be minimized to a single latch per input. This saves a considerable amount of power. In principle, it is possible to maintain the timing resolution for the whole divider chain. However, due to the increased layout complexity of multiphase dividers and the lower power of the low speed stages, the third divider is designed to have only 8 phases instead of 32. This increases the number of latches required at the input of the 16:8 MUX to 1.5 latches per input where the MUX itself is used as a latch. The final divider generates 16 phases at 750 MHz maintaining the timing resolution of the preceding clock and thus allowing the use of a single latch per stage for the 32:16 MUX. Since the timing constrains are relaxed at this low frequency,

we eliminate this latch. In effect, this means that the 32:16 MUX has an effective φ=0.5 since it is transparent to the input for half the clock period.

A 64-channel PRBS generator generates a pseudorandom sequence of length (2^7-1), (2^{15}-1), or (2^{31}-1) that is used as an input data source for the TX [48]. The PRBS generator can also be bypassed and a 2^{10}-bit arbitrary sequence can be used as the input data. The data source is driven by one of the 750 MHz clock phases and its output is retimed and applied to the input of the serializer.

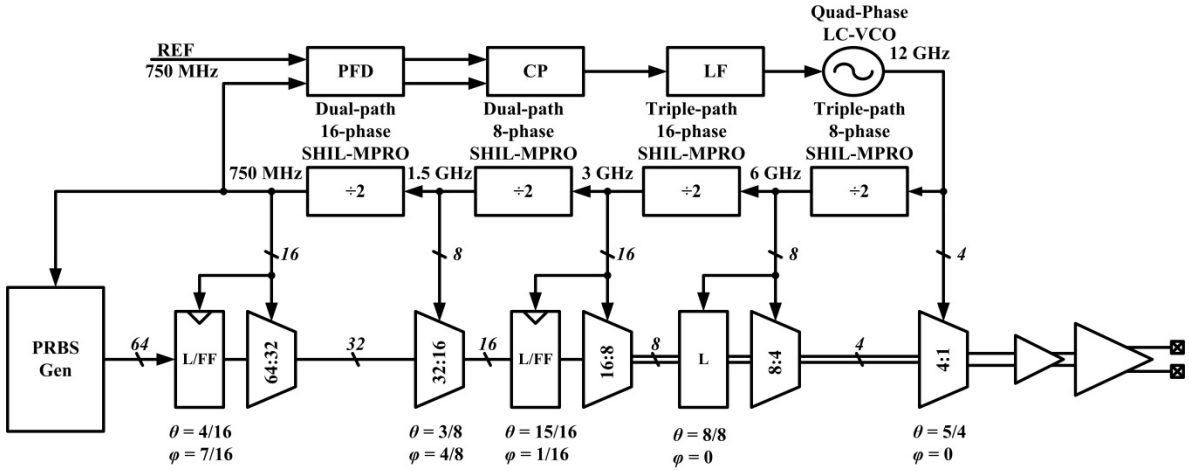


Fig. 5.3. Proposed transmitter architecture.

5.1.4. On-Chip Eye Monitor

To be able to measure the actual waveforms on the chip, we included an on-chip eye monitoring system. A 6-bit phase interpolator [60] and a simple 8-bit R-2R DAC provide variable time and voltage references for a high bandwidth comparator. The comparator subsamples the output of the transmitter at 1/64 of the final data rate. The output of the comparator is then compared in the control unit to one of the input channels of the transmitter and bit errors are counted in a 32-bit counter. The measurement is repeated for every input clock

phase and reference voltage and the results are stored in a scan chain that is read in real time using a logic analyzer.

Although the output is subsampled, the sampling aperture of the comparator has to be narrow enough to avoid filtering the measured signal. In fact, the bandwidth requirements of the comparator used here are the same as that that would be used in the receiver. The design of the comparator is discussed in Section 5.2.

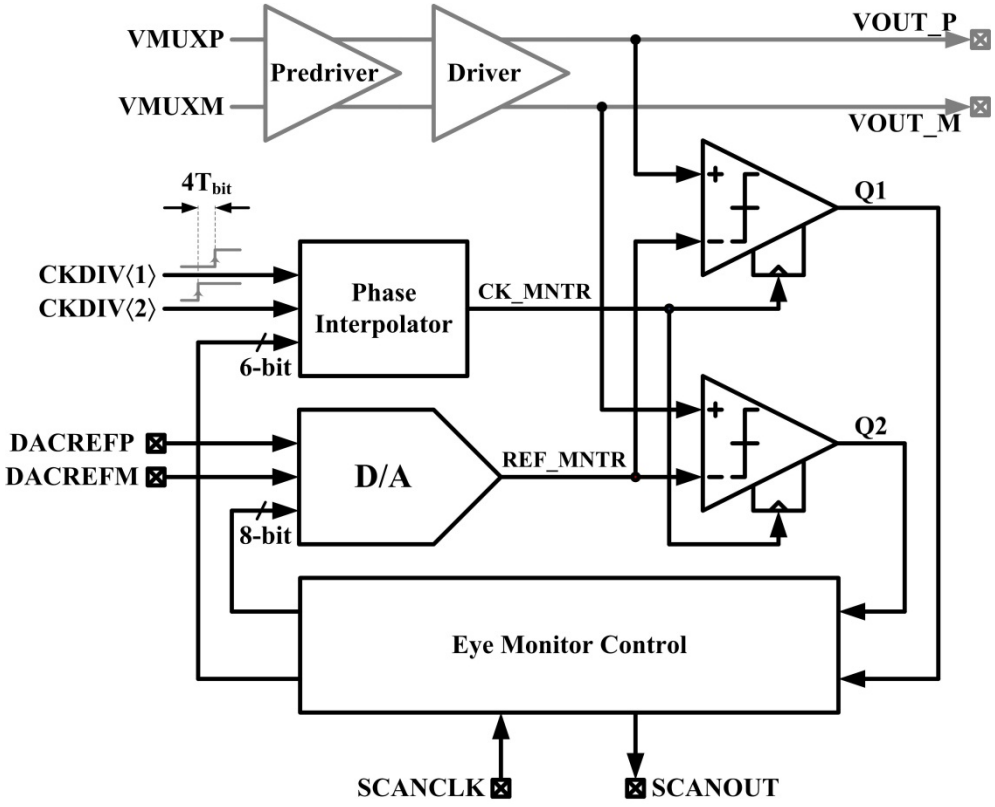


Fig. 5.4. On-chip eye monitoring system.

5.2. Circuit Details

This section explains the details of the different circuit blocks used in the transmitter. We begin with the building blocks of the phase-locked loop then we explain the design of the multiplexer and finally, the design of the comparator is discussed.

5.2.1. Quadrature *LC*-VCO

Fig. 5.5 shows the schematic of the 12-GHz quadrature *LC*-VCO. Using the same naming convention used for MPROs in Chapter 3, the cross-coupled inverters are sized by a scaling factor h_3 while the coupling inverters are sized by h_4. An expression for the oscillation frequency of the quadrature oscillator can be derived using a similar analysis to that of MPROs. In the Appendix, we derive an expression for the oscillation frequency of a general multiphase, multipath *LC* oscillator (MPLCO). This expression can be simplified as given by (5.1).

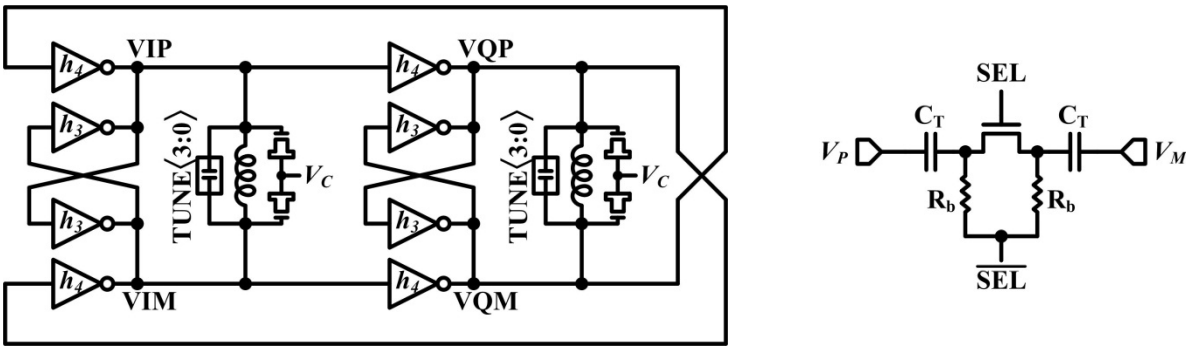


Fig. 5.5. Schematic diagram of the quadrature *LC*-VCO: (a) VCO. (b) Unit capacitor used for coarse tuning.

$$\omega_{osc} = \frac{\omega_R}{2} + \sqrt{\left(\frac{\omega_R}{2}\right)^2 + \omega_o{}^2} \tag{5.1}$$

In (5.1), ω_o is the resonance frequency of the equivalent tank circuit while ω_R is the oscillation frequency of the core ring oscillator that results if the equivalent inductance of the

tank circuit is eliminated. From the analysis in Chapter 3, As the coupling ratio (h_4/h_3) is increased, the value of ω_R increases causing the oscillation frequency to deviate more from resonance. This increase in the coupling ratio improves the quadrature phase accuracy at the cost of random phase noise degradation [49].

In practice, supply noise is a more serious source of jitter compared to the device noise. As the supply voltage increases, both components that determine the oscillator frequency, ω_R and ω_o, change in opposite directions. On one hand, the frequency of the core ring oscillator increases with the supply voltage due to the increased current drive of the inverters. On the other hand, the resonance frequency of the tank circuit decreases with supply voltage due to the increase in the value equivalent tank capacitance [39]. The variation in oscillation frequency due to supply variation can be calculated by differentiating (5.1) as given by (5.2). Since the first term due to the core ring oscillator is always positive while the second term that represents the tank resonance is always negative, a value of h_4/h_3 exists that causes the supply sensitivity to be nulled.

$$\frac{\partial \omega_{osc}}{\partial V_{dd}} = \frac{1}{2}\left(\frac{\omega_{osc}}{\omega_{osc} - (\omega_R/2)}\right) \times \left(\frac{\partial \omega_R}{\partial V_{dd}}\right) + \left(\frac{\omega_o}{\omega_{osc} - (\omega_R/2)}\right) \times \left(\frac{\partial \omega_o}{\partial V_{dd}}\right) \tag{5.2}$$

Fig. 5.6 shows simulation results for the supply sensitivity defined by (5.3) and the oscillator figure of merit (2.2). In addition to improving the phase accuracy, increasing the coupling ratio can improve the supply rejection by more than 20dB at the cost of ~4dB degradation in random phase noise for the same power consumption. In a typical mixed-signal chip environment, this leads to an overall improvement in the overall jitter. Accordingly, in our design, we use a coupling ratio h_4/h_3=1.

$$S_{VDD} = 20\log\left[\frac{(\Delta\omega_{osc}/\omega_{osc})}{(\Delta V_{dd}/V_{dd})}\right] \tag{5.3}$$

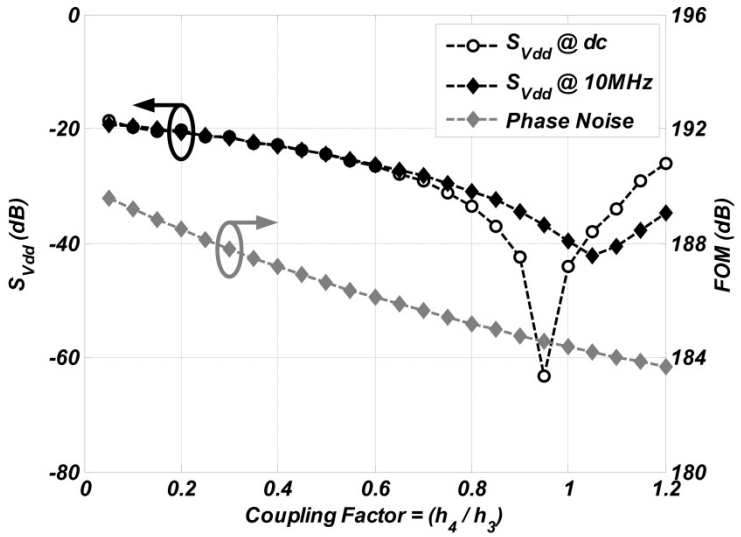


Fig. 5.6. Effect of varying the coupling ratio (h4/h3) on the supply voltage sensitivity and the oscillator figure of merit

5.2.2. Frequency-Divider Chain

The divider-chain consists of four stages. The first and second stages are explained in Sections 4.5 and 4.6, respectively. They are realized as octal-phase and hexadecimal-phase superharmonic injection locked triple-path ring oscillators. The first stage has a coupling configuration (h_8,h_5,h_3)=(2,2,6) and a clocking configuration (α_8,α_5,α_3)=(0,0,1) while the second stage has (h_{16},h_9,h_7)=(2,2,6) and (α_{16},α_9,α_7)=(0,0,1). These sizing ratios maximize the maximum locking frequency as explained in the previous chapter with only one clocked branch to simplify the layout design.

For the octal-phase divider in the third stage, we only used a conventional dual-path design as the one in Fig. 4.15(b). The reason for this choice is because at the third stage, the frequency is 4 times less compared to that at the first stage and the loading capacitance is also less due to the

fanout in the transmitter data path. Accordingly, the optimally scaled triple-path design would reach the limit of the minimum device size that we set and the dual-path design becomes more power efficient due to reduced self-loading. Similarly, for the final hexadecimal-phase divider, we used a dual-path design using 8 differential cross-coupled latches. The sizing ratios for the third and fourth stages are (h_8,h_5)=(3,1) and (h_{16},h_9)=(3,1), respectively. In both stages, only the feedforward inverters are clocked. That is (α_8,α_5)=(1,0) for the octal-phase divider and (α_{16},α_9)=(1,0) for the hexadecimal-phase one.

5.2.3. Phase/Frequency Detector

Fig. 5.7(a) shows the block diagram of a conventional tri-state phase/frequency detector (PFD) [51]. The flip-flop can be implemented as a TSPC-FF with an asynchronous reset signal as shown in Fig. 5.7(b). Since the D-input of the flip-flop is always equal to '1', node 'X' in Fig. 5.7(b) is always pulled down. Accordingly, both the first stage and the pull-down network of the second stage can be removed without affecting the functionality of the flip-flop when used in a PFD. Since the output has 0-to-1 transitions only when the reset input is activated, M6 in the third stage can also be removed. The flip-flop thus reduces tot eh simplified form in Fig. 5.7(c).

Fig. 5.7(d) shows the schematic of the proposed PFD. It consists of two simplified dynamic latches that require only a single phase for both the reference and divided clock inputs. Minimizing the number of stacked devices allows the PFD to have sharp output transitions. Simulations show fast rising/falling edges for frequencies up to more than 2 GHz.

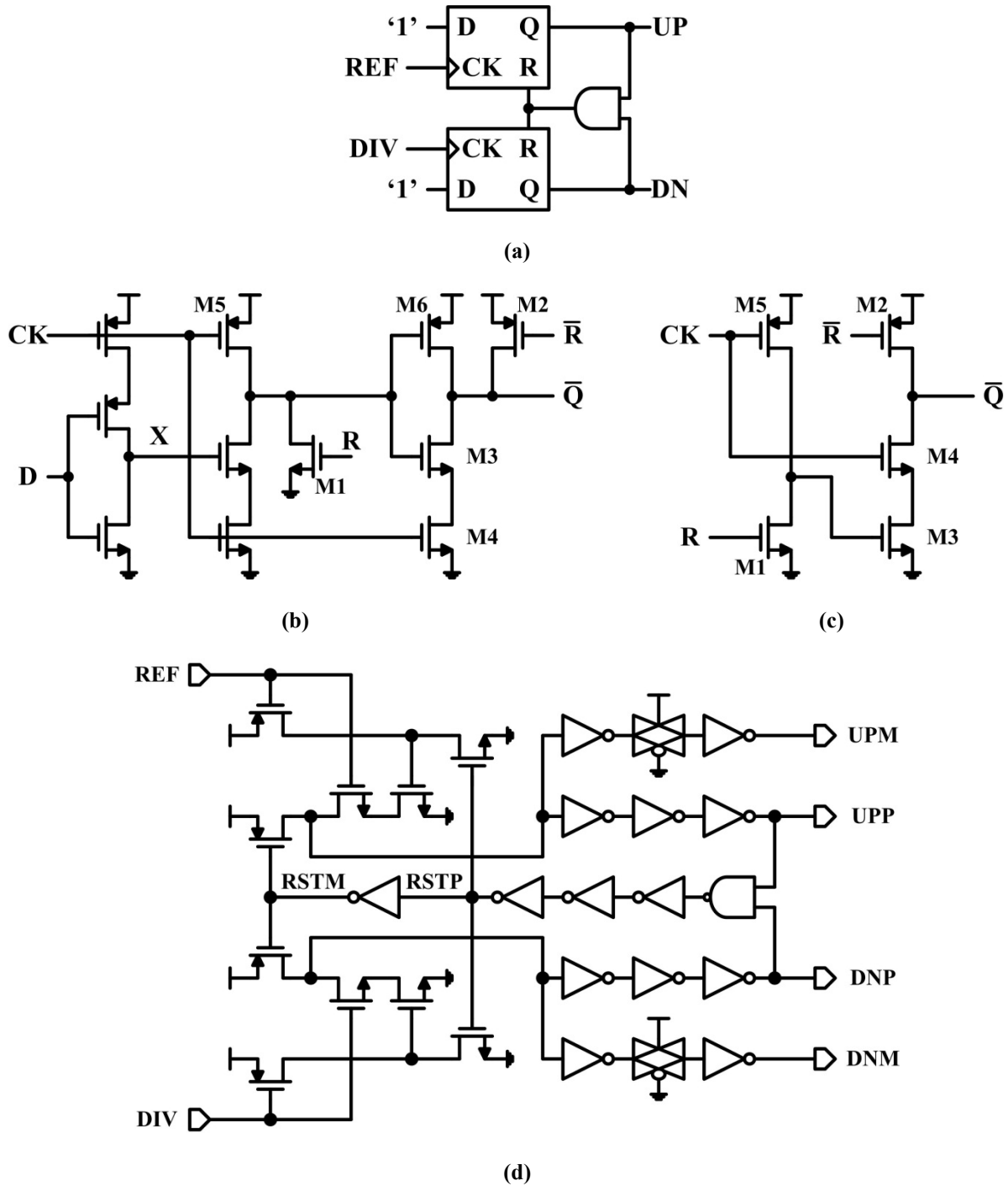


Fig. 5.7. Evolution of the proposed phase/frequency detector (a) Block diagram of a conventional PFD (b) TSPC flip-flop with an asynchronous reset (c) Simplified TSPC-FF assuming D=1 (d) Proposed PFD

5.2.4. Charge-Pump

Fig. 5.8 shows the schematic diagram of the charge pump. Dual current compensation [52] is used to achieve constant and matched UP/DN currents. In addition, current steering and OpAmp biasing of node X reduces the dynamic mismatch [53]. Since the loop filter capacitors are implemented using metal fringing capacitors, no leakage compensation is needed in the charge pump. Due to the small static and dynamic mismatch, the measured spur level is less than −74 dBc without any calibration.

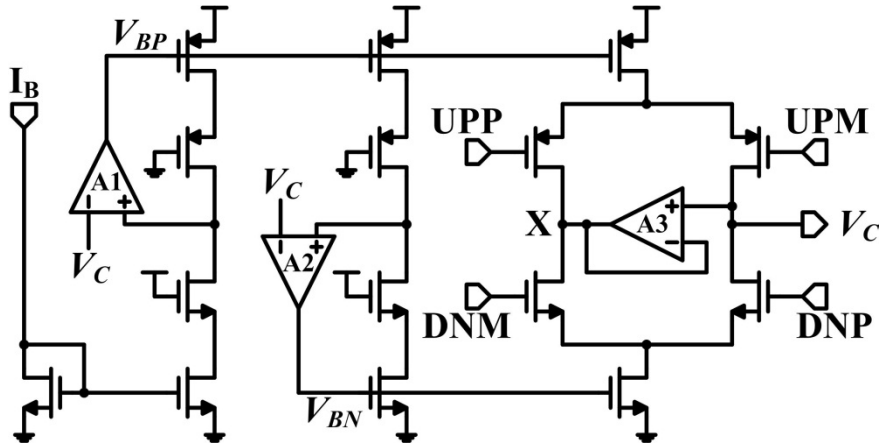


Fig. 5.8. Charge pump schematic

5.2.5. Multiplexer Design

The final stage in the serializer is a 4-to-1 multiplexer that operates up to 48 Gb/s. The MUX is clocked with a quadrature-phase 12 GHz clock generated directly from an *LC*-VCO. Fig. 5.9(a) shows a block diagram of the multiplexer. Each unit cell generates a 25% duty-cycle pulse by ANDing two adjacent clock phases. This pulse is used to connect one data input to the output as shown in Fig. 5.9(b). The outputs of the 4 unit cells are added in the current-domain and converted into a voltage by the output impedance of the multiplexer. Inductive shunt peaking is used to extend the bandwidth of the circuit.

Fig. 5.10 shows different possible methods to implement the multiplexer unit cell. In Fig. 5.10(a), a stack of 3 NMOS devices is used to perform the ANDing and the sampling operations in a single stage. This technique is used in [54] to implement a 10 Gb/s 4:1 MUX in 0.13μm CMOS technology. Although the number of internal nodes is minimal, the devices have to be large enough to provide the current drive needed to produce the desired swing. Scaling up the devices increases the capacitive loading of the VCO and the preceding latch which increases the overall power consumption.

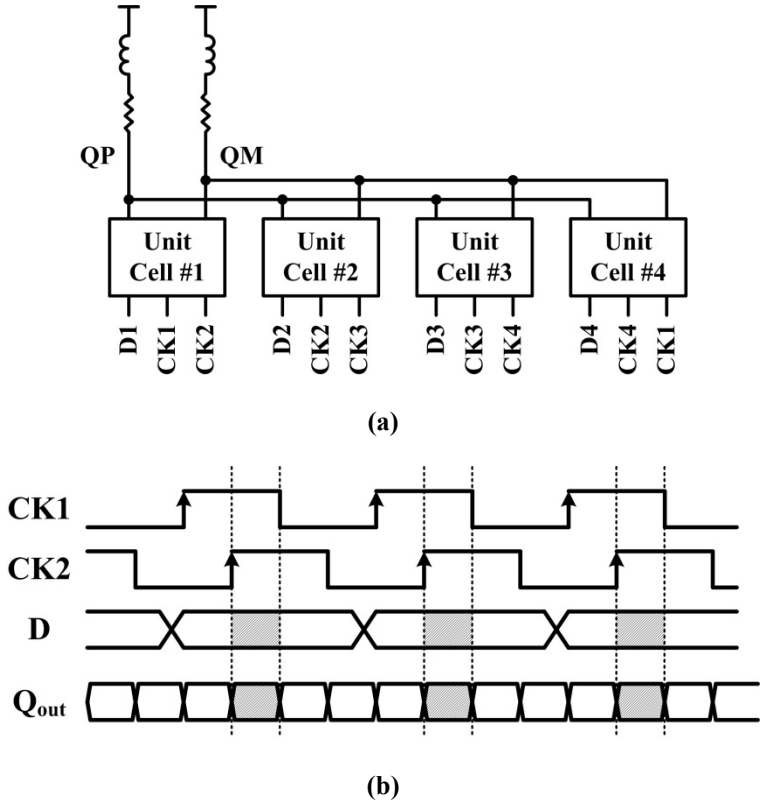


Fig. 5.9. Block diagram (a) and timing diagram (b) of a 4:1 multiplexer.

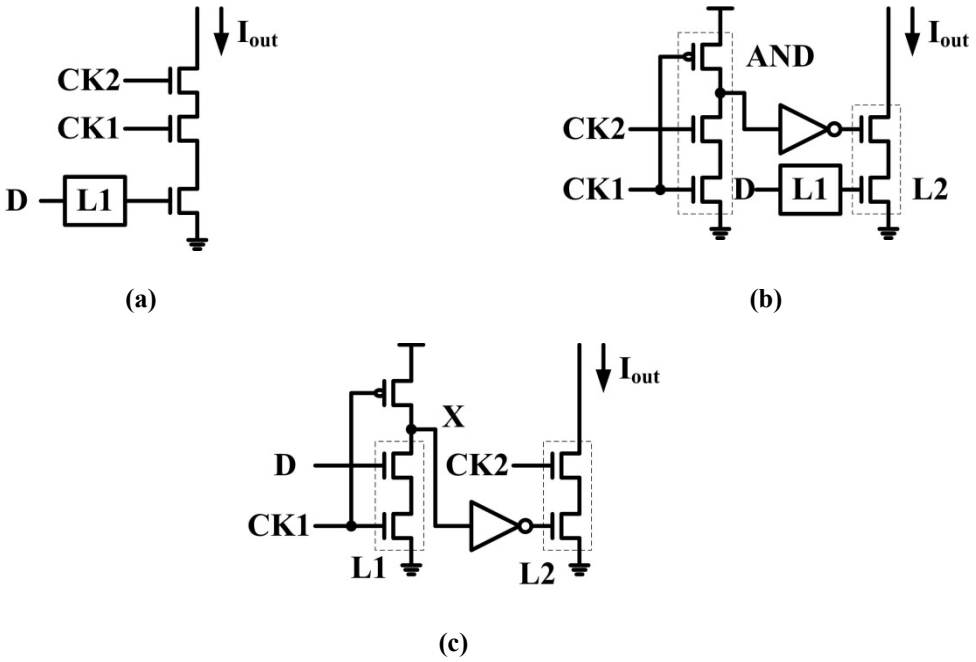


Fig. 5.10. Different possible implementations of the 4:1 MUX unit cell

To improve the current drive, a two-stage implementation can be used where pulse generation is achieved using a separate AND gate as shown in Fig. 5.10(b). Since the AND gate is directly driven by the sinusoidal VCO outputs, the output of the first NAND gate is not rail-to-rail and the inverter burns an excessive amount of power due to both the switching and the direct-path currents.

A modified two-stage implementation is shown in Fig. 5.10(c) [55]. Since the AND gate output duty-cycle is increased to 50% and its switching activity is reduced by a factor of 2, the power consumption can be reduced. In addition, the first stage now acts as a dynamic latch where node X is pre-charged every clock cycle and then conditionally discharged by the input data. Accordingly, no additional latches are required before the multiplexer.

The proposed implementation of the multiplexer unit cell is shown in Fig. 5.11(a). It is a modified version of the design in [55] where the input latch is realized in PMOS. At the rising

edge of CK1, L1 holds the sampled data input at the internal capacitance of node X which then propagates to the output as shown in Fig. 5.11(b). At the rising edge of CK2, node X is discharged causing the output current to turn off. Since node X is pre-discharged rather than pre-charged, the inverter is not needed and can be removed. The proposed design minimizes the number of internal nodes and the direct-path current.

Fig. 5.11(c) shows the schematic diagram of the proposed 4-to-1 multiplexer. It uses a differential version of the proposed unit cell. The transistor M1 is shared between the 4 branches to provide a higher current drive for the discharging branch. Since each clock phase drives both clock inputs in two different unit cells and each cell has a differential data input, the clock load is symmetric for all phases and no phase mismatch can result from load imbalance.

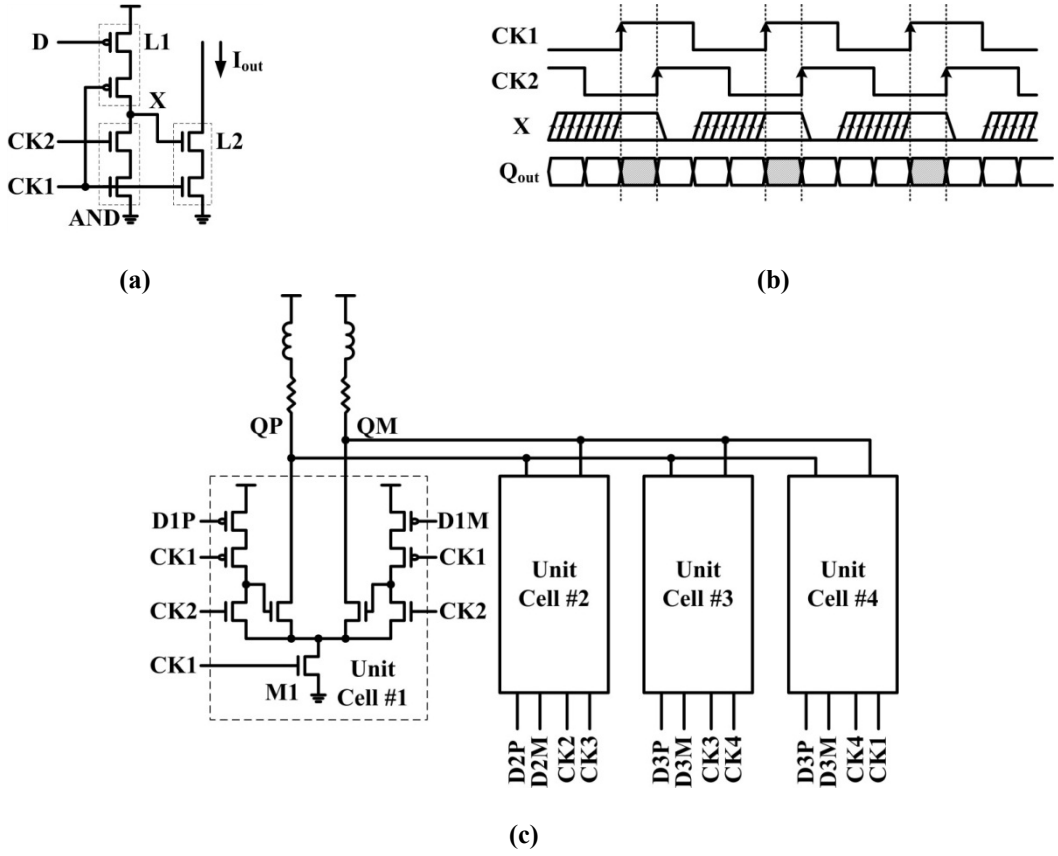


Fig. 5.11. Proposed 4-to-1 multiplexer (a) Unit cell (b) Timing diagram (c) Complete MUX

5.2.6. Comparator Design

The comparator is used in the on-chip eye-monitoring system to sample the output waveform of the transmitter. Accordingly, the sampling aperture of the comparator has to be narrow enough such that it does not introduce significant filtering for the measured waveform.

Fig. 5.12(a) shows the schematic of the proposed comparator design. The comparator uses both edges of the input differential clock to operate at double the input clock rate. During one of the two input clock phases, one channel uses negative feedback to extend the tracking bandwidth at the cost of the tracking gain. At the same time, the other channel uses positive feedback to achieve regeneration. The switching between tracking and regeneration is achieved by reversing the output polarity of the feedback stage as shown in Fig. 5.12(b). The design uses drain switching rather than source switching to minimize the transition time from tracking to regeneration which reduces the sampling aperture.

Fig. 5.13 shows the simulated sampling function of the comparator. The simulation is performed using the periodic steady-state (PSS) and the periodic *ac* (PAC) analyses in spectreRF as explained in [61]. The sampling instant is taken at the end of the regeneration period just before the clock transition. The simulation is done using a 10 GHz input clock which corresponds to a sampling rate of 20 GS/s. Fig. 5.13 shows that the sampling aperture is approximately 14 ps which is less the minimum desired bit period of 20 ps.

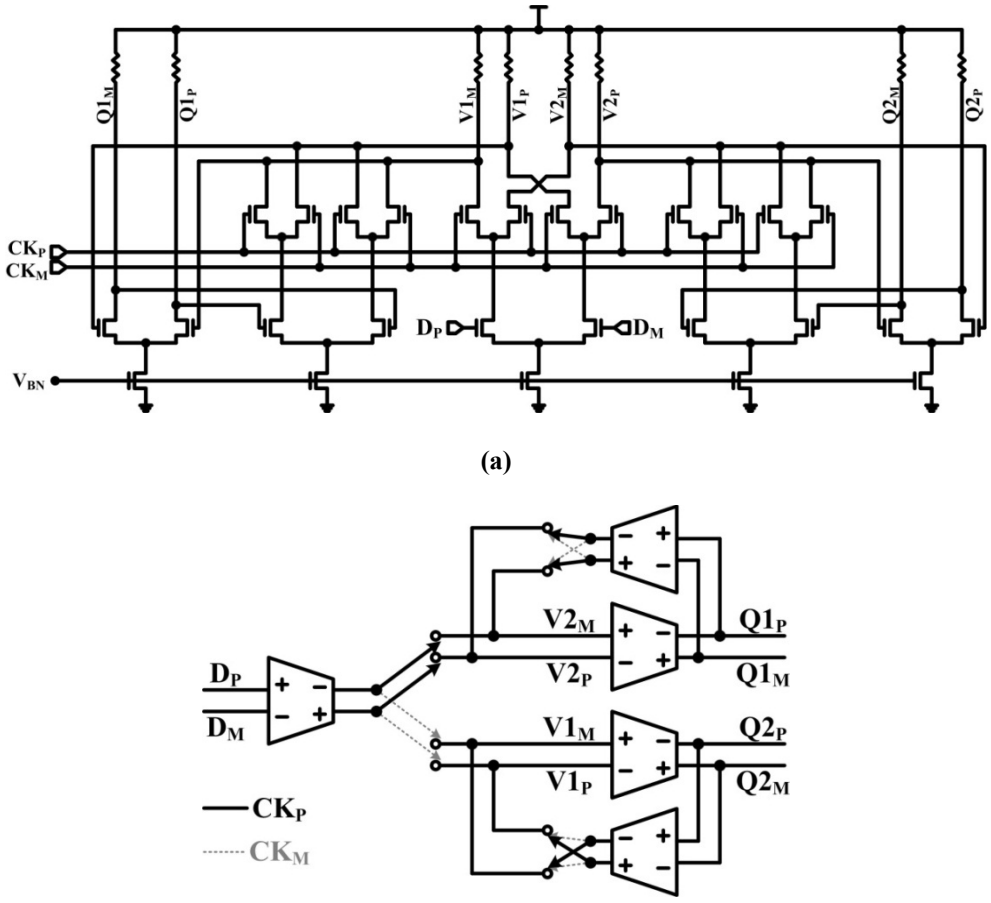


Fig. 5.12. Proposed drain-switched comparator: (a) Schematic diagram. (b) Equivalent block diagram.

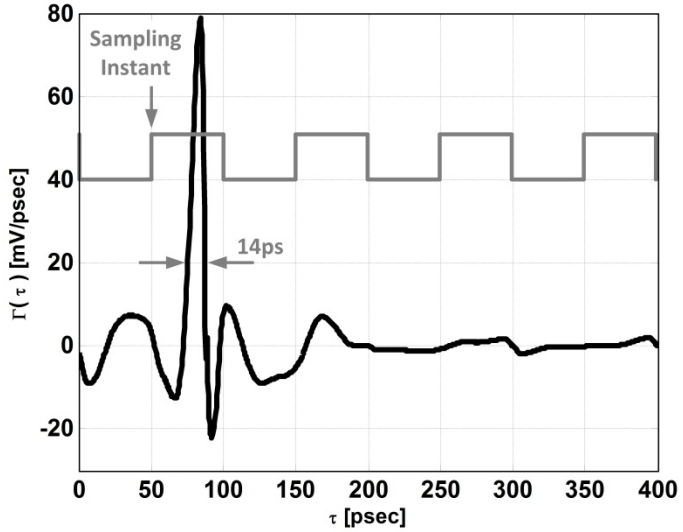


Fig. 5.13. Simulated sampling aperture of the comparator.

Fig. 5.14 shows the simulated sensitivity of the comparator. A '00110011' sequence is applied to the comparator input at double the clock rate. This causes a '0101' output at each of the comparator outputs. The time shift between the data transition and the clock edge is varied and each time, the minimum signal amplitude needed to obtain correct outputs is found. The minimum sensitivity occurs for a data-to-clock delay of ~30 ps which is equal to the delay of the comparator, as can be seen from Fig. 5.13, and is less than 3-mV.

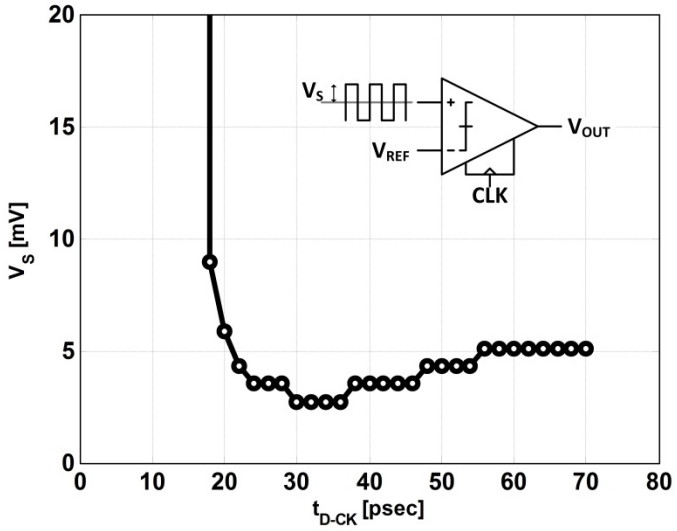


Fig. 5.13. Simulated sampling aperture of the comparator..

5.3. Conclusion

Serial link transmitters are systems that are inherently parallel and thus ones that can greatly benefit from multiphase clocking. In this chapter we showed how multiphase sampling can be used to optimize the operation bit-rate window such that the transmitter can operate for a wide range of bit rates. This leads to designing transmitters that are robust to PVT variations and eliminate the need for any delay matching buffers of delay calibration loops leading to a simpler, more compact, and lower power design.

Multiphase sampling can also allow the designer to minimize the number of sampling elements between the different serializer stages which are needed for resynchronization. If the timing resolution of the sampling clock is maintained between different stages, the required number of latches can be reduced by 43% which leads to significant improvement in power and chip area provided that phase generation can be achieved at no extra overhead. This is accordingly a direct application for the results of our analysis in Chapter 4.

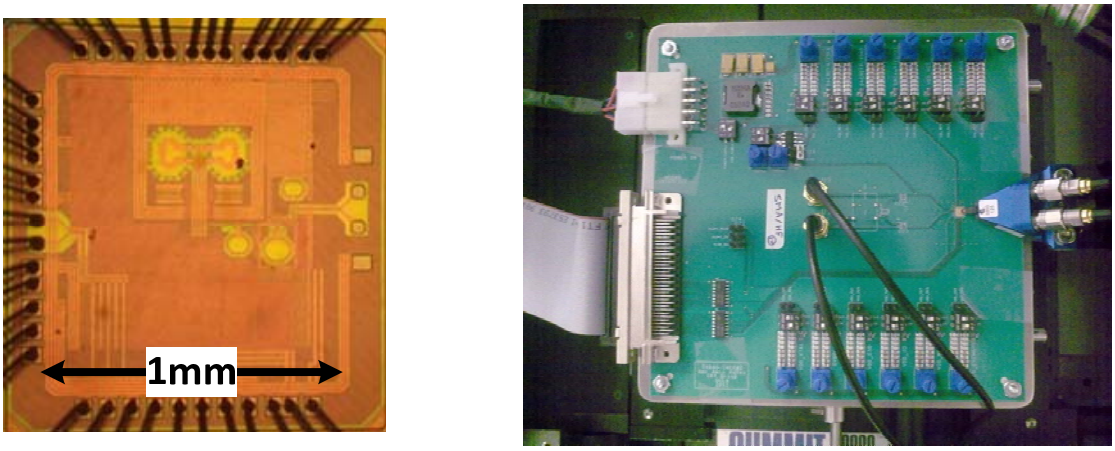
Various circuit techniques are proposed to improve the power efficiency and performance of the transmitter. An accurate quadrature-phase low supply sensitivity VCO design has been explained to minimize the deterministic jitter at the output of the transmitter. A novel PFD and an accurate charge pump reduce the reference spur level to less than -74 dBc which leads to negligible sinusoidal jitter at the output. A new 4-to-1 multiplexer design, that achieves the desired bandwidth requirements at low power, is proposed. And finally, a low sampling aperture comparator using drain-switching that is used in an on-chip eye monitoring system is explained.

In the next chapter, we show the measurement results of the fabricated transmitter chip.

CHAPTER 6

Experimental Results

The transmitter explained in the previous chapter is fabricated in 65-nm 1P9M CMOS technology and tested in a chip-on-board assembly. Fig. 6.1 shows the chip and the printed circuit board photographs. The chip occupies a total area of 1.2 mm^2. In this chapter, we explain the details of the testing setup and discuss the measurements results.



(a) **(b)**

Fig. 6.1. Chip photograph (a) and testing board (b)

6.1. Testing Setup

Fig. 6.2 shows a block diagram of the testing setup. The transmitter output is probed using a 50-GHz bandwidth GSSG cascade probe. The probe is either connected to a 20-GHz bandwidth subsampling scope or a 50-GHz bandwidth spectrum analyzer. An external signal generator generates a 750-MHz reference clock that is used both as a reference to the PLL and to trigger the scope. Different control bits are written into an on-chip scan chain using a pattern generator

and can be read out using a logic analyzer. The interface between the pattern generator, the logic analyzer, the chip and the PC is controlled by a National Instruments data acquisition (NI-DAQ) interface.

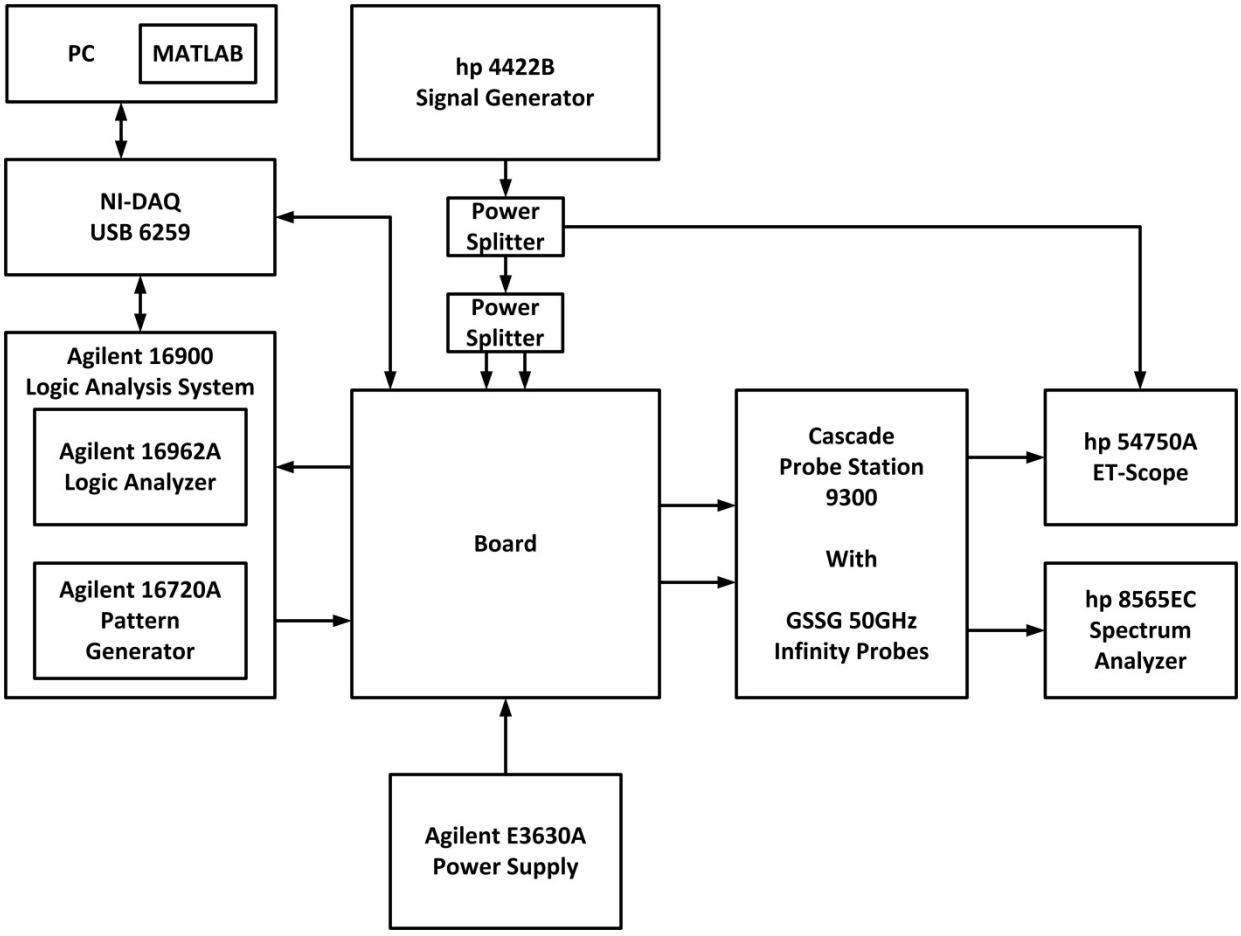


Fig. 6.2. Testing setup

6.2. Measurement Results

Fig. 6.3 shows the measured PLL output spectrum at 10.56-GHz output. To test the PLL, a '0011' sequence is applied to the serializer causing the final 4:1 MUX, the pre-driver, and the driver to act as a 3-stage clock buffer for the VCO output. The locking range of the PLL extends

from 7.9 GHz to 12.1 GHz limited only by the VCO tuning range. The worst reference spur level over the locking range of the PLL is −74 dBc for a carrier frequency of 10.56 GHz.

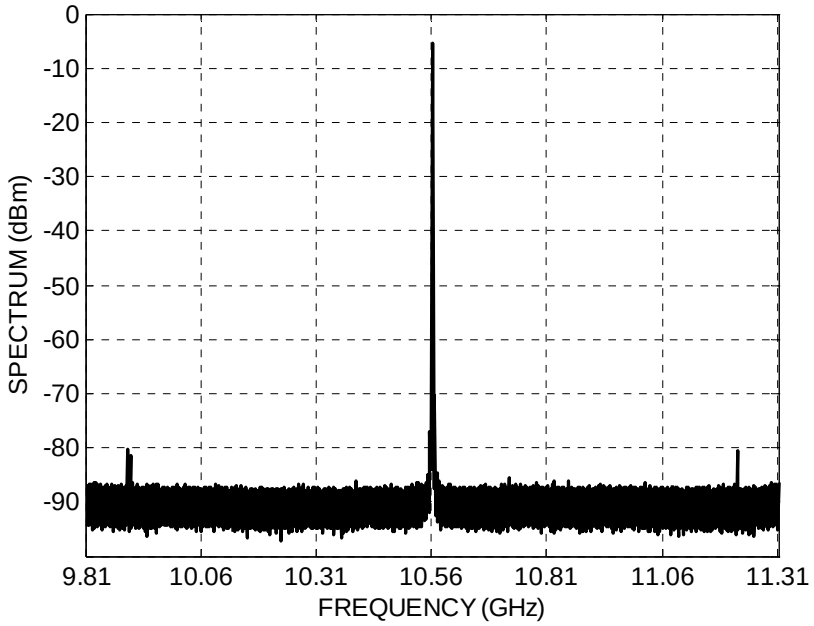


Fig. 6.3. Measured spectrum of the PLL output for a 10.56 GHz output carrier frequency

Fig. 6.4 shows the measured single side-band phase noise for a carrier frequency of 12.08 GHz near the upper end of the locking range. The out of band phase noise at 10 MHz offset is −127.5 dBc/Hz. The small bump around 1 MHz is due to some under-damping in the loop dynamics. The integrated phase noise from 100 Hz to 10 MHz is equal to 1.09 degree-rms which corresponds to 251 fsecrms random jitter. As one would expect from the very low spur level, the periodic jitter is very low.

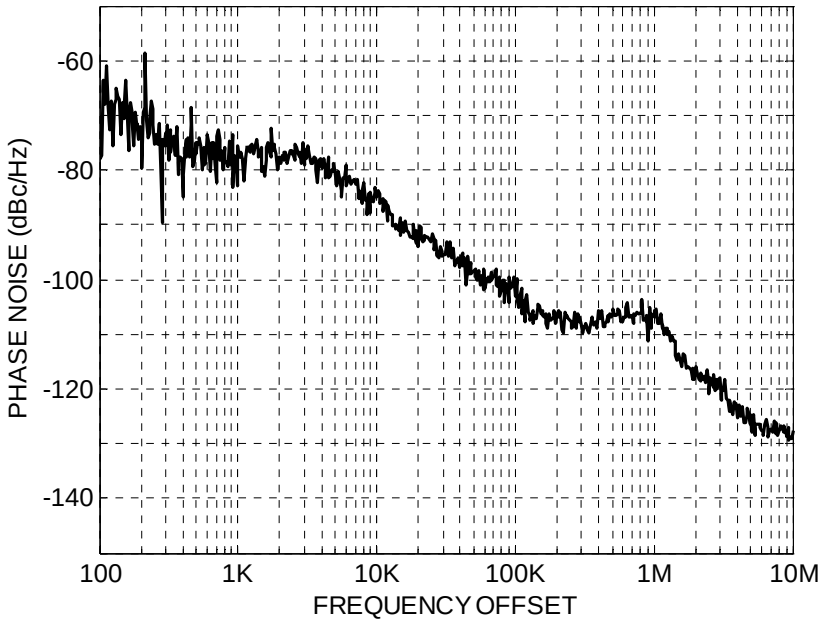


Fig. 6.4. Measured phase noise at 12.08 GHz carrier frequency

Such low jitter numbers are not measurable using our equipment. Fig. 6.5 shows the time domain measured jitter histogram. The measured jitter is less than 0.66 $psec_{rms}$ limited by the triggering jitter of the scope.

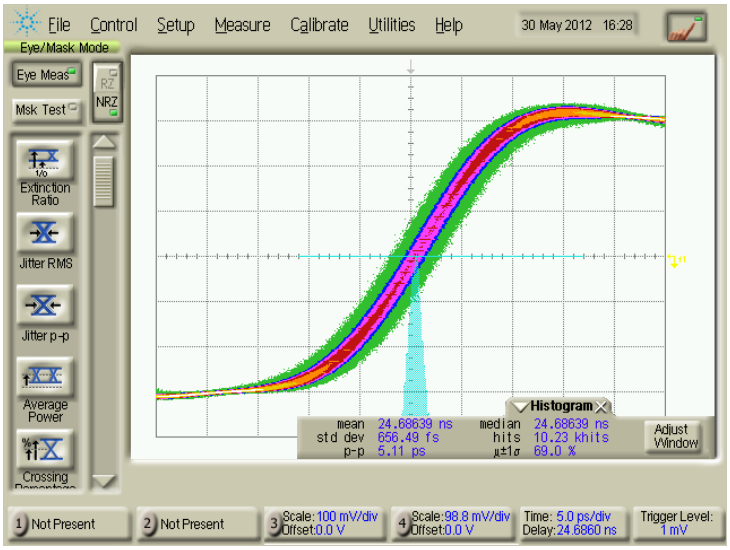


Fig. 6.5. Measured jitter for a 12.08 GHz carrier frequency.

The serializer operates properly over the whole locking range of the PLL. This range corresponds to data rates of 32-48 Gb/s. This wide operation range is due to the optimum choice of the sampling phases at all the multiplexing stages. Fig. 6.6 shows the measured single-ended eye-diagram at the output of the transmitter at 48 Gb/s while Fig. 6.7 shows the measured eye using the on-chip eye monitoring. The vertical eye opening measured on chip for the single-ended output is ~270 mV while that measured by the scope is ~150 mV. This difference is due to the attenuation caused by the probes, the 48" cables and the sampling front-end of the digital scope. This attenuation is estimated as ~7 dB at 24 GHz.

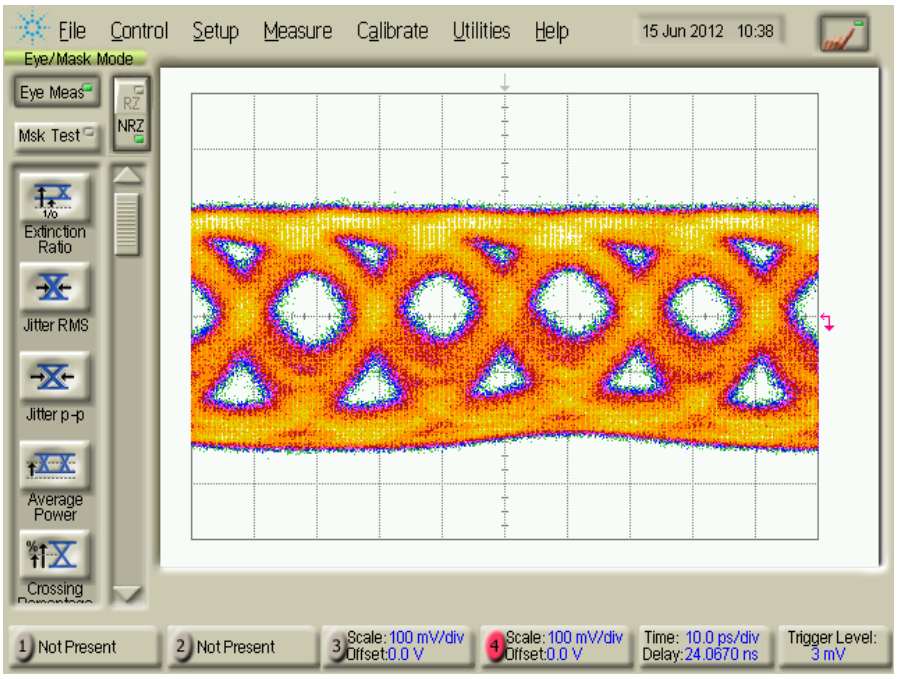


Fig. 6.6. Measured eye-diagram at 48 Gb/s using a ($2^{31}-1$) PRBS

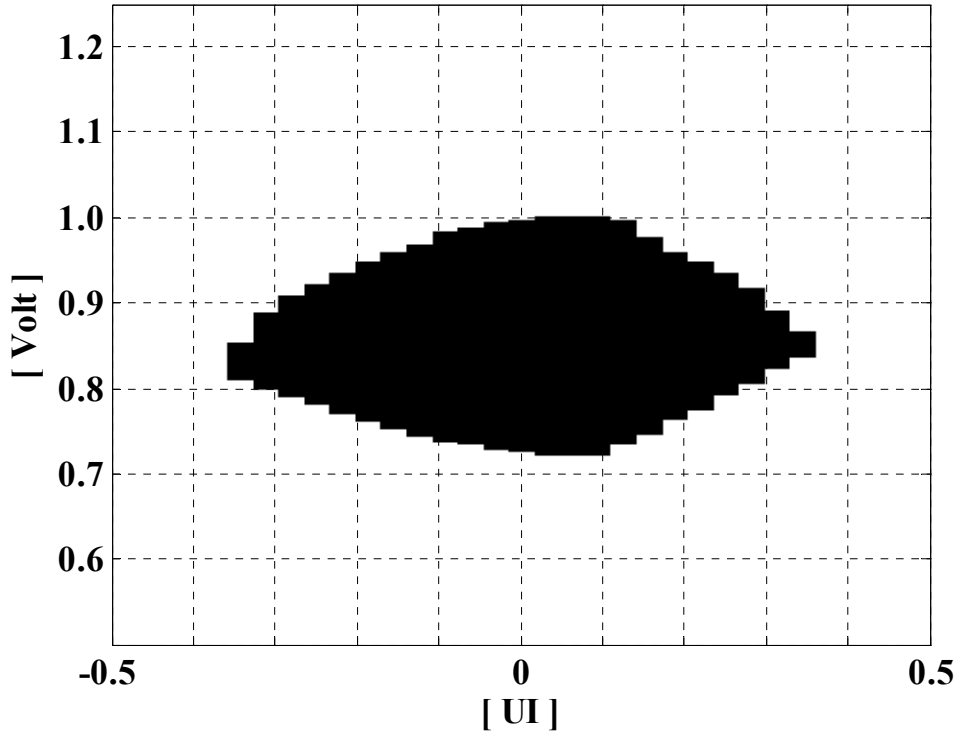


Fig. 6.7. Eye diagram measured using on-chip eye monitor.

The chip operates at data rates 31.68−48.4 Gb/s. It consumes a total power of 88 mW from a 1.2 V supply. Table 6.1 shows the power breakdown of the transmitter while Table 6.2 compares the achieved performance with other serializing transmitters operating at similar data rates. The use of high-speed power-optimized multiphase frequency dividers allows us to remove all forms of delay adjustment overhead that is used in other designs. In addition, it allows us to minimize the number of retiming latches in the data path and to realize the whole divider chain in CMOS without using any inductors. All of which leads to the significant power and area savings compared to previous work. These savings are achieved with a phase noise and jitter performance that is comparable with other approaches.

Table 6.1. Power breakdown for the transmitter chip.

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

Table 6.2. Performance Summary

Ref	[5]	[7]	[8]	This Work
Technology	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage [V]	1.45	1.1	1.2	1.2
Data Rates [Gb/s]	35.2−38.8	39.8−44.6	39.8−44.6	31.68−48.4
PLL Freq [GHz]	17.6−19.4	39.8−44.6	19.9−22.3	7.92−12.1
PN@10MHz (dBc/Hz)	-113.5	-108	-120	-127.5
Jitter [fsec$_{rms}$]	650	238	640	251
TX Area [mm^2]	3.74	5	4.6	1.2
TX Power [W]	1.56	0.76	0.86	<0.1

CHAPTER 7

Conclusion

We present in this dissertaion an accurate model and a comprehensive analysis that explain the operation of multipath ring oscillators [57] and frequency dividers [58]. We showed that using multipath coupling, the number of phases of a ring oscillator or a frequency divider can be increased arbitrarily while maintaining the oscillation or division frequency. In fact, by increasing the number of phases, it is possible to push the maximum operation frequency to higher values at the cost amplitude reduction or equivalently degraded phase noise. We show that the only limitation on the maximum operation frequency of a ring oscillator or a frequency divider is the cut-off frequency of the technology and not the number of phases needed at its output.

The mode stability problem which is characteristic of multipath ring structures is part of the analytical study. To help designers traverse the large design space, a design procedure based on a linear optimization algorithm is provided to allow a designer to quickly arrive at the optimum coupling structure that maximizes the oscillation frequency given a certain desired number of phases and phase noise performance. This optimum structure is chosen while considering mode stability.

The oscillator analysis is further extended to apply to frequency dividers. The locking range of superharmonic injection-locked multipath ring oscillators is studied under the condition of strong signal injection. We show that, unlike the previously studied weak injection scenario, the

actual locking rang of the divider is not actually phase limited. Instead, it is either limited by the maximum gain available in the circuit or by the existence of other non-dominant modes that can prevent the desired mode from being sustained.

Similar to our work on oscillator design, a design procedure that uses the derived mathematical model is proposed to help a designer to quickly arrive at the best divider design that maximizes the division frequency for a certain power budget.

The ability to generate multiple phases at high frequencies and with low power is useful in numerous applications. As an example, we showed how this can help design a high speed serial link transmitter allowing it to operate at wide range of data rates without the need for any delay adjustment overhead. As shown in out measurement results, the architecture also minimizes the number of high-speed latches which results in significant power savings in comparison with previously published results.

The analyses presented in this work can be extended to many of the applications mentioned in Chapter 1. One example is to design a complete clock network as one big coupled oscillator. The effect of different loads and routing parasitics can be taken into account and compensated for by proper adjustment of coupling strengths. Since the figure of merit an optimally designed multipath ring oscillator can be maintained regardless of the number of phases it has, this suggests that as the clock network grows in size, the resulting phase noise or jitter at any of its outputs can actually decrease. This conclusion is opposite to common wisdom which suggests that as more buffering elements are added, the jitter performance should degrade.

Another extension is to perform this coupling in clock networks and embed the frequency dividers. This extension is not unlike the clock divider approach described in this dissertation

except the feedback divider can be considered as part of the oscillator itself as opposed to an explicit element downstream from the oscillator. In addition to reducing jitter, inter-stage coupling allows the design of a clock network with accurate and well defined phase relationships between the different outputs.

Appendix

Oscillation Modes in Multipath *LC* Oscillators

Fig. A.1 shows the general form of a multipath *LC* oscillator (MPLCO). Similar to the MPRO, we assume all coupling paths exist. Each row of inverters is sized by a sizing factor, h_i, with respect to a certain reference inverter where i=1,2,3,…,N. The unit inverter has an equivalent input capacitance, C_g, an output conductance, g_o, and an equivalent transconductance, g_m. Unlike the MPRO, each of the output nodes of the MPLCO is loaded with an *LC* tank circuit having a capacitance, C_t, and an inductance, L. The finite quality factor of the inductance is modeled with a parallel conductance g_t=1/(QωL).

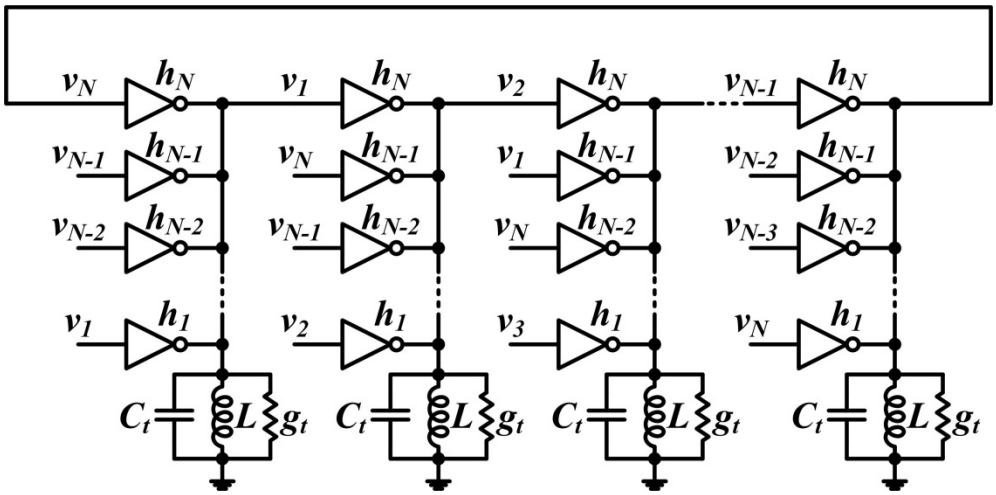


Fig. A.1. General form of a multipath *LC* oscillator.

The output voltage v_i can be expressed by (A.1) where V_o is the oscillation amplitude, ω_n is the oscillation frequency, and n=0,1,2,…,N-1 is the oscillation mode index. The gain and phase

oscillation conditions can be derived by applying KCL at any of the oscillator nodes similar to the MPRO analysis. Equation (A.2) shows the harmonic balance equation at node v_1.

$$v_i(t) = V_o \cos\left(\omega_n t - \frac{2\pi n(i-1)}{N}\right) \tag{A.1}$$

$$\begin{aligned} &\sum_{i=1}^{N} h_i g_m V_o \cos\left(\omega_n t - \frac{2\pi n(i-1)}{N}\right) + g_o\left[\frac{g_t}{g_o} + \sum_{i=1}^{N} h_i\right] V_o \cos(\omega_n t) \\ &-\omega_n Cg\left[\frac{Ct}{Cg} + \sum_{i=1}^{N} h_i\right] V_o \sin(\omega_n t) + \frac{1}{\omega_n L} V_o \sin(\omega_n t) = 0 \end{aligned} \tag{A.2}$$

By separating the coefficient of $\cos(\omega_n t)$, the gain condition can be derived and the mode gain can be expressed by (A.3) where $a_{R,n}$ is the mode gain of the core MPRO that results if the LC tanks are disconnected (3.8) and $H = \sum_{i=1}^{N} h_i$ is defined similar to the previous MPRO and SHIL-MPRO analyses. Equation (A.3) shows that the dc gain required from the inverters in the case of an MPLCO is slightly higher than that for an MRPO due to the loading caused by the finite quality factor of the tank circuit.

$$\begin{aligned} a_n &= \frac{1 + (g_t / H g_o)}{-\sum_{i=1}^{N} x_i \times \cos\left(\frac{2\pi n}{N}(i-1)\right)} \\ &= \left[1 + (g_t / H g_o)\right] a_{R,n} \end{aligned} \tag{A.3}$$

The phase condition can be derived by separating the coefficient of $\sin(\omega_n t)$ in (A.2). Due to the presence of the inductor, the phase condition is a quadratic equation of the oscillation frequency that has two solutions rather than just one as for an MPRO. The oscillation frequencies of the n^{th} mode can be expressed by (A.4) where $\omega_{R,n}$ is the oscillation frequency of the core MPRO if the tank circuits are disconnected, expressed by (3.7), and $\omega_o = [L(C_t + HC_g)]^{-1/2}$ is the

resonance frequency of the tank circuit loaded with the inverters. Equation (A.4) shows that if the core MPRO does not have a zero frequency, the oscillation frequency of the MPLCO can take one of two values that is either higher than or less than the resonance frequency. This each value of the mode index, *n*, corresponds to two oscillation modes. The first mode has a higher oscillation frequency than the resonance frequency where the tank load appears capacitive and thus we refer to it as the capacitive mode and we denote it with the subscript 'C'. The second mode has a lower frequency than resonance where the tank circuit appears inductive and thus we refer to it as the inductive mode and we denote it with the subscript 'L'.

$$\omega_{n(C/L)} = \left[\left(\frac{\omega_{R,n}}{2}\right)\times\frac{1+\left(g_t/Hg_o\right)}{1+\left(C_t/HC_g\right)}\right] \pm \sqrt{\left[\left(\frac{\omega_{R,n}}{2}\right)\times\frac{1+\left(g_t/Hg_o\right)}{1+\left(C_t/HC_g\right)}\right]^2 + {\omega_o}^2} \qquad \text{(A.4)}$$

The analysis in its current form does not show whether the capacitive or the inductive mode is dominant. This is due to the symmetry of the impedance of the tank load as a function of frequency. In practice, the finite quality factor of the inductor is more precisely modeled as a series resistance rather than a parallel conductance [56]. In this case, the equivalent parallel conductance of the tank circuit is lower at higher frequencies causing the mode gain of the capacitive mode to be lower than that of the inductive one and thus becomes more dominant.

If the quality factor of the tank circuit is limited by that of the capacitance rather than the inductance, the situation is reversed where the inductive mode becomes the dominant mode. This situation, however, is rare in practice and it can easily be avoided by good layout design.

In the special case of a cross coupled oscillator, the oscillation frequency of the core MPRO is equal to zero and (A.4) reduces to the resonance frequency.

References

[1] Anantha P. Chandrakasan, Samuel Sheng, and Robert Brodersen, "Low-Power CMOS Digital Design," *IEEE Journal of Solid-State Circuits*, vol. 27, no.4, pp. 473–484, Apr. 1992.

[2] Zhiyu Ru, Niels A. Moseley, Eric A. M. Klumperink, and Bram Nauta,"Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.

[3] David Murphy, Amr Hafez, Ahmad Mirzaei, Mohyee Mikhemar, Hooman Darabi, Mau-Chung Frank Chang, Asad Abidi, "A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure," International Solid-State Circuits Conference (ISSCC), pp. 74–75, Feb. 2012.

[4] Xiang Gao, Eric A. M. Klumperink, and Bram Nauta, "Advantages of Shift Registers Over DLLs for Flexible Low Jitter Multiphase Clock Generation," *IEEE Transactions on Circuits And Systems – II: Express Briefs*, vol. 55, no. 3, pp. 244–248, Mar. 2008.

[5] Jeong-Kyoum Kim, Jaeha Kim, Gyudong Kim, and Deog-Kyoon Jeong, "A Fully Integrated 0.13-μm CMOS 40-Gb/s Serial Link Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1510–1521, May 2009.

[6] Jaeha Kim, et al.,"A 20-GHz Phase-Locked Loop for 40-Gb/s Serializing Transmitter in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 899–908, Apr. 2006.

[7] Shunichi Kaeriyama et al., "A 40 Gb/s Multi-Data-Rate CMOS Transmitter and Reciever Chipset With SFI-5 Interface for Optical Transmission Systems," *IEEE Journal of Solid State Circuits*, vol. 44, no. 12, pp. 3568–3579, Dec. 2009.

[8] Kouichi Kanda, et al., "A Single-40 Gb/s Dual-20 Gb/s Serializer IC With SFI-5.2 Interface in 65 nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 44, no. 12, pp. 3580–3588, Dec. 2009.

[9] Nikola Nedovic, et al., “A 3 Watt 39.8-44.6 Gb/s Dual Mode SFI5.2 SerDes Chip Set in 65 nm CMOS,” *IEEE Journal of Solid State Circuits*, vol. 45, no. 10, pp. 2016–2029, Oct. 2010.

[10] John G. Maneatis and Mark A. Horowitz, “Precise delay generation using coupled oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1273–1282, Dec. 1993.

[11] S. J. Lee, B. Kim, and K. Lee, “A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme,” *IEEE Journal of Solid-State Circuits*, vol. 32, no. 2, pp. 289–291, Feb. 1997.

[12] Lizhong Sun and Tadeusz A. Kwasniewski, “A 1.25-GHz 0.35-m Monolithic CMOS PLL Based on a Multiphase Ring Oscillator,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 910–916, Jun. 2001.

[13] W. Yan and H. Luong, “A 900-MHz CMOS Low-Phase-Noise Voltage-Controlled Ring Oscillator,” *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 48, no. 2, pp. 216–221, Feb. 2001.

[14] Chan-Hong Park and Beomsup Kim, “A Low-Noise, 900-MHz VCO in 0.6-um CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 586–591, May 1999.

[15] T. Kan, G. Leung, and H. Luong, “A 2-V 1.8-GHz Fully Integrated CMOS Dual-Loop Frequency Synthesizer,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1012–1020, Aug. 2002.

[16] Yalcin Alper Eken, and John P. Uyemura, “A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18-m CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 36, no.1, pp. 230–233, Jan. 2004.

[17] Matthew Z. Straayer, and Michael H. Perrott, “A Multi-Path Gated Ring Oscillator TDC with First-Order Noise Shaping,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 230–233, Apr. 2009.

[18] Junfeng Xu, Shwetabh Verma, Thomas H. Lee, "Coupled Inverter Ring I/Q Oscillator for Low Power Frequency Synthesis," in Proc. IEEE Symp. VLSI Circuits, 2006, pp. 172–173.

[19] S. Mohan, W. Chan, D. Colleran, S. Greenwood, J. Gamble, and I. Kouznetsov, "Differential Ring Oscillators with Multipath Delay Stages," in Proc. IEEE 2005 Custom Integrated Circuit Conf., 2005, pp. 503–506.

[20] R. L. Miller, "Fractional-Frequency Generators Utilizing Regenerative Modulation," *Proc. I.R.E.*, pp. 446–457, Jul. 1939.

[21] Aminghasem Safarian, Seema Anand, and Payam Heydari, "On the Dynamics of Regenerative Frequency Dividers," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 53, No. 12, pp. 1413–1417, Dec. 2006.

[22] Shwetabh Verma, Hamid R. Rategh, and Thomas H. Lee, "A Unified Model for Injection-Locked Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 1015–1027, Jun. 2003.

[23] Marc Tiebout, "A CMOS Direct Injection-Locked Oscillator Topology as High-Frequency Low Power Frequency Divider," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1170–1174, Jul. 2004.

[24] Stefano Dal Toso, Andrea Bevilacqua, Marc Tiebout, Nicola Da Dalt, Andrea Gerosa, and Andrea Neviani, "An Integrated Divide-by-Two Direct Injection-Locking Frequency Divider for Bands S Through Ku," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 7, pp. 1686–1695, July 2010.

[25] Ken Yamamoto, Minoru Fujishima, "A 44-μW 4.3-GHz Injection-Locked Frequency Divider With 2.3-GHz Locking Range," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 671–677, Mar. 2005.

[26] Jun-Chau Chien, and Liang-Hung Lu, "Analysis and Design of Wideband Injection-Locked Ring Oscillators With Multiple-Input Injection," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1906–1915, Sep. 2007.

[27] Ahmad Mirzaei, Mohammad E. Heidari, Rahim Bagheri, and Asad A. Abidi, "Multi-Phase Injection Widens Lock Range of Ring-Oscillator-Based Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.

[28] Hui Zheng and Howard C. Luong, "A Double-Balanced Quadrature-Input Quadrature-Output Regenerative Frequency Divider for UWB Synthesizer Applications," *IEEE Transactions on Circuits and Systems–I: Regular Papers*, vol. 55, no. 9, pp. 2944–2951, Oct. 2008.

[29] Hamid R. Rategh, and Thomas H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[30] D. W. Jordan, and P. Smith, Nonlinear Ordinary Differential Equations, Oxford University Press, 2007.

[31] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.

[32] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[33] Alper Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: a unifying theory and numerical methods for characterization," *IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 47, no. 5, pp. 655–673, May 2000.

[34] J. A. McNeill, "Jitter in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 870–879, Jun. 1997.

[35] L. Dai, and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 49, no. 5, pp. 328–338, May 2002.

[36] R. Navid, T. H. Lee, and R. W. Dutton, "Minimum achievable phase noise of RC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 630–636, Mar. 2005.

[37] Asad. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[38] Zhiming Deng, and Ali M. Niknejad, "The Speed–Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2457–2465, Nov. 2010.

[39] Payam Heydari, and Ravindran Mohanavelu, "Design of Ultrahigh-Speed Low-Voltage CMOS CML Buffers and Latches," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 12, no. 10, pp. 1081–1093, Oct. 2004.

[40] Payam Heydari, and Ravindran Mohanavelu, "A 40-GHz Flip-Flop Based Frequency Dividers," *IEEE Transactions on Circuits and Systems–II: Express Briefs*, vol. 53, no. 12, pp. 1358–1362, Dec. 2006.

[41] Christian Kromer, George von Büren, Gion Sialm, Thomas Morf, Frank Ellinger, and Heinz Jäckel, "A 40-GHz Static Frequency Divider With Quadrature Outputs in 80-nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 10, pp. 564–566, Oct. 2006.

[42] Jaeha Kim, et al.,"Design Optimization of On-Chip Inductive Peaking Structures for 0.13-μm CMOS 40-Gb/s Transmitter Circuits," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 56, no. 12, pp. 2544–2555, Dec. 2009.

[43] Sudip Shekhar, Jeffrey S. Walling, and David Allstot, "Bandwidth Extention Techniques for CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.

[44] Jeffrey S. Walling, Sudip Shekhar, and David Allstot, "Wideband CMOS Amplifier Design: Time-Domain Considerations," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 55, no. 7, pp. 1781–1793, Aug. 2008.

[45] Hai Tao et al., "40–43-Gb/s OC-768 16:1 MUX/CMU Chipset With SFI-5 Compliance," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2169–2180, Dec. 2003.

[46] Dimitris Bertsimas, John N. Tsitsiklis, Introduction to Linear Optimization. Athena Scientific, 1997.

[47] Stephen Boyd, and Lieven Vandenburghe, Convex Optimization. Cambridge University Press, 2004.

[48] Ming-Shuan Chen, C.-K. Ken Yang, "A Low-Power Highly Multiplexed Parallel PRBS Generator", accepted for publication at *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2012.

[49] Ahmad Mirzaei, Mohammad E. Heidari, Rahim Bagheri, Saeed Cherazi, and Asad Abidi, "The Quadrature *LC* Oscillator: A Complete Portrait Based on Injection Locking," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.

[50] Emad Hegazi, and Asad A. Abidi, "Varactor Characteristics, Oscillator Tuning Curves, and AM-FM Conversion," *IEEE Journal of Solid State Circuits*, vol. 38, no. 6, pp. 1033-1039, Jun. 2003.

[51] Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.

[52] Dong-Keon Lee, Jeong-Kwang Lee, and Hang-Geun Jeong, "A dual Compensated Charge Pump With Reduced Current Mismatch," *Proceedings of the 4th WSEAS international conference on Circuits, systems, signal and telecommunications*, pp. 109–112, 2010.

[53] Woogeun Rhee, "Design of High Performance CMOS Charge Pumps in Phase-Locked Loops," *IEEE International Symposium on Circuits and Systems*, pp. 545–548, Jul. 1999.

[54] Patrick Chiang, William J. Dally, Ming-Ju Edward Lee, Ramesh Senthinathan, Yangjin Oh, and Mark A. Horowitz, "A 20-Gb/s 0.13-μm CMOS Serial Link Transmitter Using an *LC*-PLL to Directly Drive the Output Multiplexer," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 1004–1011, Apr. 2005.

[55] C.-K. Ken Yang and Mark A. Horowitz, "A 0.8-pm CMOS 2.5 Gb/s Oversampling Receiver and Transmitter for Serial Links," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 2015–2023, Dec. 1996.

[56] Sudip Shekhar, et al., "Strong Injection Locking in Low-Q *LC* Oscillators: Modeling and Application in a Forwarded-Clock I/O Receiver," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 56, no. 8, pp. 1818–1829, Aug. 2009.

[57] Amr A. Hafez, C.-K. Ken Yang, "Design and Optimization of Multipath Ring Oscillators," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 58, no. 10, Oct. 2011, pp. 2332-2345.

[58] Amr A. Hafez, C.-K. Ken Yang, "Analysis and Design of Superharmonic Injection-Locked Multipath Ring Oscillators," Submitted to *IEEE Transactions on Circuits and Systems—I: Regular Papers*.

[59] Amr A. Hafez, Ming-Shuan Chen, and C.-K. Ken Yang, "A Multi-Phase Multi-frequency Clock Generator Using Superharmonic Injection Locked Multipath Ring Oscillators as Frequency Dividers," Accepted in *IEEE Asian Solid State Circuits Conference (ASSCC)*, Nov. 2012.

[60] Ming-Shuan Chen, Amr A. Hafez, and C.-K. Ken Yang, "A 0.1-1.5 GHz 8-Bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection," Accepted in *IEEE Asian Solid State Circuits Conference (ASSCC)*, Nov. 2012.

[61] Jaeha Kim, Brian S. Leibowitz, Metha Jeeradit, "Impulse Sensitivity Function Analysis of Periodic Circuits," *IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 386–391, Nov 2008.