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**Integrated Microwave and Millimeter-Wave Phased-Array Designs  
in Silicon Technologies**

A dissertation submitted in partial satisfaction of the  
requirements for the degree Doctor of Philosophy  
in  
Electrical Engineering (Electronic Circuits and Systems)

by

Kwang-Jin Koh

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Professor Lawrence Larson

2008

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The dissertation of Kwang-Jin Koh is approved, and it is acceptable  
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Chair

University of California, San Diego

2008



*To my mother & my brother*

*in Heaven.*

*I wish I had to say I love them more often.*

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- Chapter 2 and 3 are based on the following papers:
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  - K.-J. Koh and G. M. Rebeiz, “6-18 GHz 5-Bit Active Phase Shifter,” *IEEE Trans. Microwave Theory Tech.*, (in review).
  - K.-J. Koh and G. M. Rebeiz, “A 0.13- $\mu\text{m}$  CMOS Digital Phase Shifter for K-band Phased Arrays,” *IEEE RFIC Symp. Dig.*, pp. 383-386, June 2007.
  
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  - K.-J. Koh and G. M. Rebeiz, “An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360-1371, June 2008.
  - K.-J. Koh and G. M. Rebeiz, “An Eight-Element 6 to 18 GHz SiGe BiCMOS RFIC Phased-array Receiver,” *Microwave Journal*, vol. 50, no. 5, pp. 270-274, May 2007.
  - K.-J. Koh and G. M. Rebeiz, “An X- and Ku-Band 8-Element Linear Phased Array Receiver,” *IEEE CICC Conf. Proc.*, pp. 761-764, Sept 2007.
  
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  - K.-J. Koh and G. M. Rebeiz, “A Q-Band Phased-Array Front-End with Integrated Wilkinson Couplers for Linear Power Combining,” *IEEE Bipolar Circuit and Tech. Meeting*, pp. 190-193, Oct. 2008.

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  - K.-J. Koh, J. W. May and G. M. Rebeiz, “A Millimeter-Wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE J. Solid-State Circuits*, (in review).
  - K.-J. Koh, J. W. May and G. M. Rebeiz, “A Q-Band (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE RFIC Symp. Dig.*, pp. 225-228, June 2008.

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- K.-J. Koh and G. M. Rebeiz, “An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360-1371, June 2008.
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- K.-J. Koh and G. M. Rebeiz, “An Eight-Element 6 to 18 GHz SiGe BiCMOS RFIC Phased-array Receiver,” *Microwave Journal*, vol. 50, no. 5, pp. 270-274, May 2007.
- K.-J. Koh, M.-Y. Park, C.-S. Kim and H.-K. Yu, “Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver,” *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871-884, June 2004.
- K.-J. Koh, J. W. May and G. M. Rebeiz, “A Millimeter-Wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE J. Solid-State Circuits*, (in review).
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K.-J. Koh and G. M. Rebeiz, "A 0.13- $\mu\text{m}$  CMOS Digital Phase Shifter for K-band Phased Arrays," *IEEE RFIC Symp. Dig.*, pp. 383-386, June 2007.

K.-J. Koh, M.-Y. Park and H.-K. Yu, "A Merged Structure of LNA & Sub-harmonic Mixer for Multi-band DCR Applications," *IEEE MTT Symp. Dig.*, vol. 1, pp. 246-247, June 2003.

Y.-S. Youn, J.-H. Jang, K.-J. Koh, Y.-J. Lee and H.-K. Yu, "A 2GHz 16dBm IIP3 Low Noise Amplifier in 0.25 $\mu\text{m}$  CMOS technology," *IEEE ISSCC Dig. Tech. Papers*, vol. 1, pp 452-453, 507, Feb. 2003.

#### FIELDS OF STUDY

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Studies in Electronic Circuits and Systems

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Studies in Communication Theory and Systems.

Professors Bhaskar Rao, Laurence Milstein and Rene Cruz

## ABSTRACT OF THE DISSERTATION

Integrated Microwave and Millimeter-Wave Phased-Array Designs in Silicon Technologies

by

Kwang-Jin Koh

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2008

Professor Gabriel M. Rebeiz, Chair

This research focuses on the design and analysis of on-chip phased-array receivers and transmitters in silicon technologies. Passive phase shifters have been widely used in conventional discrete implementations of phased-arrays which are based on transmit/receive modules in III-V technologies. However their large volume and high loss impose several challenging issues for on-chip integration. To leverage system optimizations of on-chip phased-arrays, active phase shifter architecture is primarily investigated in this dissertation. The active phase shifter utilizes a quadrature signal interpolation where the I/Q signals are added with appropriate amplitude and polarity to synthesize the required phase. The quadrature signal generator is a key element for accurate multi-bit phase states in the active phase shifter. To generate lossless wideband quadrature signals, a novel I/Q signal generator based on second-order L-C series resonance is developed. Active phase shifters with 4-bit and 5-bit control are then designed in 0.13- $\mu\text{m}$  and 0.18- $\mu\text{m}$  CMOS technologies and tested successfully for 6-26 GHz phased-arrays applications, featuring the smallest chip size ever reported at these frequencies with similar phase resolutions.

After successful demonstration of the active phase shifters, an eight-element phased-array receiver is developed in 0.18- $\mu\text{m}$  SiGe BiCMOS technology for X- and Ku-band satellite communications. The phased-array receiver adopts corporate-feed architecture implemented with active signal combiners. The phased-array receiver is rigorously characterized including channel-to-channel mismatches and signal coupling errors from different channels. The on-chip phased-array designs are then extended to millimeter-wave frequencies. A four-element phased-array receiver and a sixteen-element phased-array transmitter are designed using the SiGe BiCMOS technology and tested successfully for Q-band applications. Wilkinson couplers are compactly integrated for linear coherent signal combining in the Q-band phased-array receiver. Also

in the Q-band transmitter array, passive Tee-junction power dividers are integrated as a linear signal feed network. The power divider is based on a coaxial-type shielded transmission line utilizing three-dimensional metal stack, which leads to a compact corporate-feed network suitable for large on-chip arrays. The sixteen-element phased-array transmitter marks the highest integration of phased-array elements known to-date, proving a good scalability to a large array of the proposed phased-array architecture. Also, each phased-array design integrates all digital control units and presents the first demonstration of on-chip silicon phased-array at the corresponding design frequency, solving one of key barriers for low-cost and complex phased-arrays.

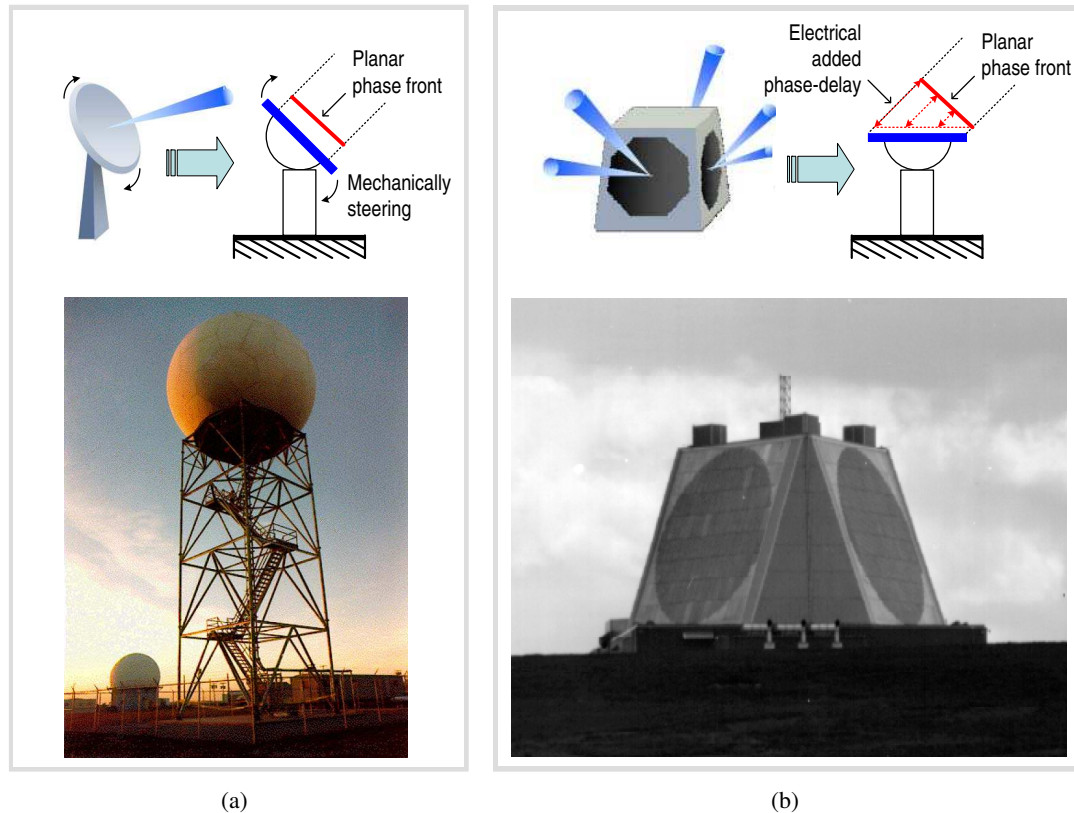
# 1

## Introduction

### 1.1 Motivation

#### 1.1.1 Background

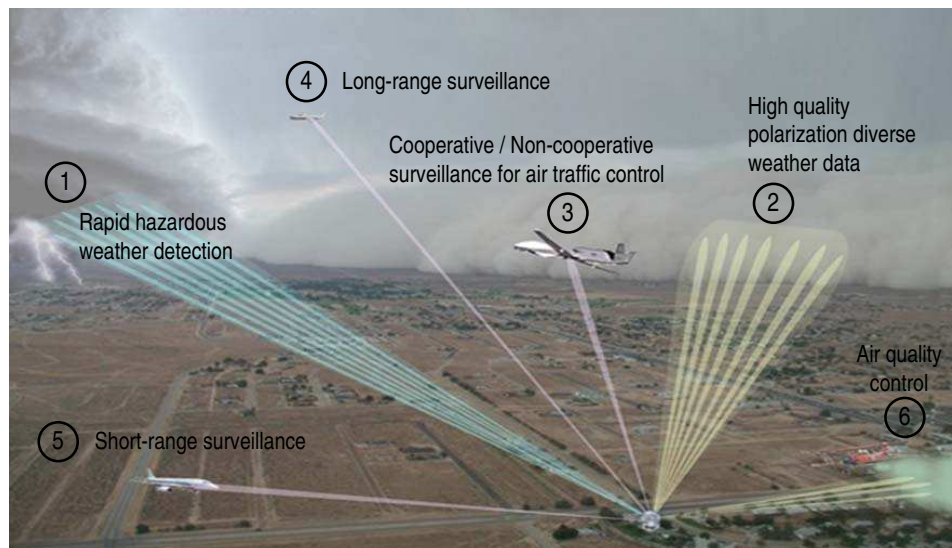
Array antennas, also called “smart antennas”, have been around for more than half a century [5–9]. They are groups of antennas which allow transmission or reception of an electromagnetic (EM) wave in a particular direction by constructive interference between the signals from individual antennas, while simultaneously blocking it to (or from) other directions by destructive signal interference, working as a spatial filter (see Appendix A). Also, by changing the signal amplitude in each antenna, the radiation pattern can be shaped, and this is labeled as “beam-forming” [8]. The controllability of the shaped-beam direction in antenna arrays, called “beam-steering”, allows that strong interferes from different directions can be placed in the nulls of a radiation pattern so as not to interfere with the desired signal, increasing spatial diversity [8]. Another fundamental merit of antenna arrays is to improve the signal-to-noise ratio (SNR), as compared to a single antenna element, by combining the signals coherently and noise incoherently from many different elements, hence increasing the channel capacity [8]. Depending on the beam steering method, there are two different antenna array systems: In the rotating reflector array shown in Figure 1.1(a), the antenna’s reflective surface is tilted mechanically to change the angle of beam center and the transmitted (or received) beam is shaped and steered by the antenna’s reflective surface [10, 11]. However, in a phased-array [Figure 1.1(b)], the beam forming and beam steering can be done by controlling the phase of the EM wave transmitted or received by each radiator relative to the phases of other radiators in the array. Typically electronic phase



**Figure 1.1:** Array antenna systems: (a) Mechanically steered, rotating reflector array and (b) electrically steered, fixed phased-array (excerpted from the presentation titled “*Update on New Technology for the Multi-Function Phased Array Radar (MPAR)*” by Office of the Federal Coordinator for Meteorology at 2007 *Multi-function Phased-Array Radar Symposium*).

shifters and attenuators are used to adjust the signal phase and amplitude in each antenna element, and analog-to-digital converters (ADCs) and digital signal processors (DSPs) are used for the computing necessary for the beam scanning [9, 12]. Due to the high-speed and high-precision control electronics, the beam forming and steering are much faster and accurate in phased-arrays than in reflector arrays where mechanical inertia limits the beam control speed. The high speed also enable for phased-arrays to move the beam nearly instantaneously in arbitrary directions, so multiple beams can be processed with the same phased-array unit [11].

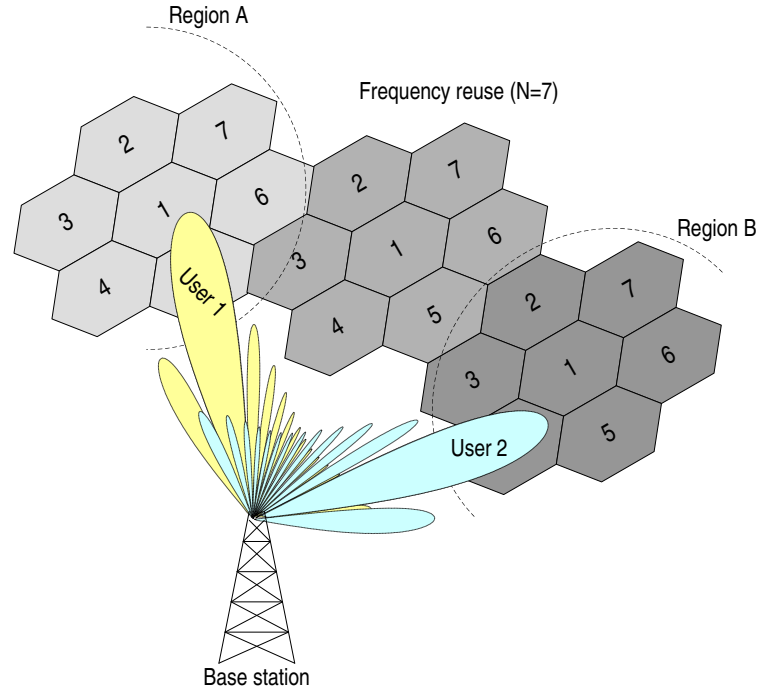
While the smart antenna has been active research subjects over past few decades, traditionally its application has been limited to military uses, such as surveillance, missile defense or target detection systems, because of the complexity of the control electronics and the cost



**Figure 1.2:** Phased-array applications in civilian sectors.

thereof. Recently with the constant efforts to reduce cost using advanced integrated circuit (IC) technology, the application area has been extended to civilian sectors. Typical examples for civilian use are shown in Figure 1.2 [11]. Rapid scan by phased-arrays can significantly improve lead time for severe weather; potentially improve modeled weather predictions; and increase warning times associated with extreme weather events ((1), (2)). The phased-arrays also can accomplish aircraft surveillance tasks much more quickly, flexibly, and at higher resolution, resulting in efficient air traffic controls ((3), (4), (5)). In addition, phased-arrays show significant potential to diagnose air quality at the scale needed to track airborne chemical, biological, radiological, and nuclear plumes ((6)). Since phased-arrays can process volumetric data with variable spatial and temporal resolutions in a micro- or nanosecond order, these functions can be incorporated into single phased-array unit called as “multi-function phased-array (MPAR)”.

Recently, phased-arrays are also coming into the spotlight for consumer-oriented mobile communications such as cellular telephones, Wi-Fi/WiMax wireless networking and internet access (IEEE 802.11 and IEEE 802.16 standards) [13–15]. Figure 1.3 shows one example for increase of spectral efficiency using phased-arrays in a conventional cell-based wireless communication environment. Since the highly directive beam pattern in phased-arrays allows interferer reduction/mitigation, increased number of users can share the same available sources such as frequency, time and codes [14]. Also, the directivity enables different users to reuse



**Figure 1.3:** Beamforming in conventional cellular wireless communication environment. The frequency reuse factor,  $N$ , can be increased by focusing energy in the desired direction, minimizing energy toward other directions and satisfying transmit power constraints.

the same sources, introducing a new multiple access scheme that exploits the space domain, called space-division multiplexing access (SDMA). Especially, the directivity of phased-arrays mitigates multi-path fading issue and focuses the EM energy toward the wanted users, lowering power requirement while increasing cover range and communication link quality. For the same reasons, phased-array can be an excellent candidate for millimeter-wave wireless communications to circumvent unfavorable propagation channel conditions at millimeter-wave frequencies [16]. The needs of phased-arrays for these commercial sectors are fueled by the exponential growth of the required signal bandwidth, precipitated by the global interest in wideband wireless applications. A low cost system with a small volume is a key factor for the commercial applications.

### 1.1.2 Dissertation Motive

Early phased-array electronics was developed with a hybrid-design concept where packaged transistors, stand-alone phase shifter, switches and passive components are assem-

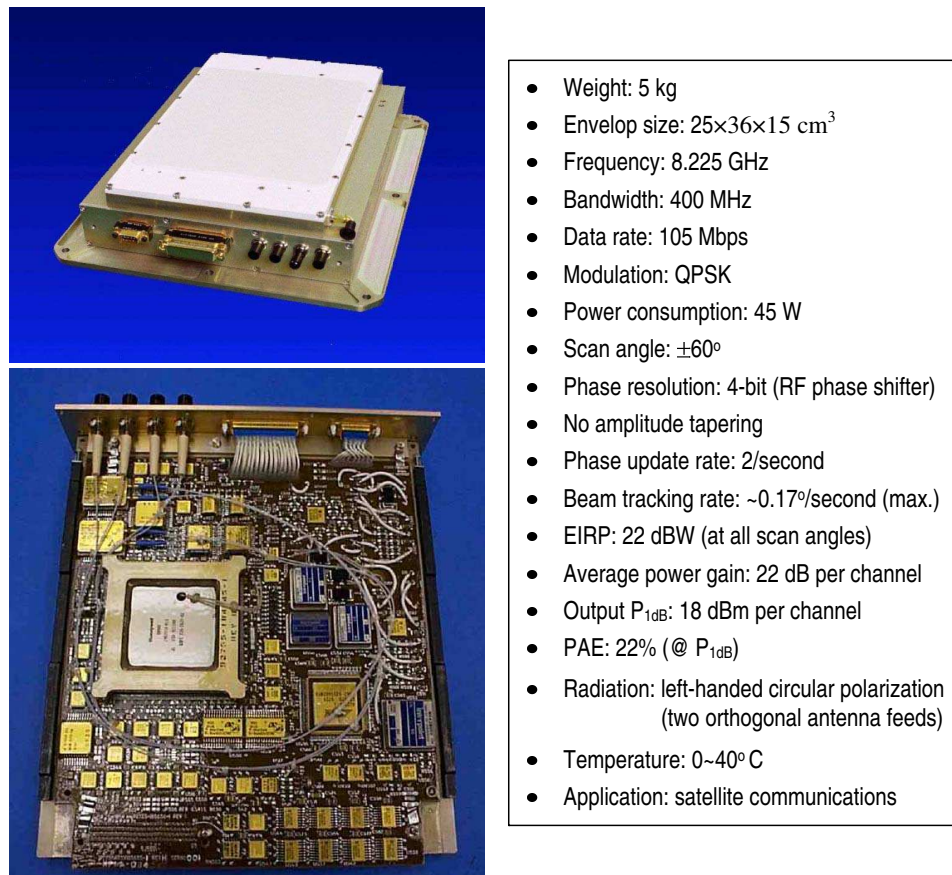
bled together on a ceramic board, resulting in high cost and large volume for civilian applications [1, 17]. Due to mature solid-state semiconductor and integrated circuit technologies, parts of the control electronics are now integrated in a monolithic form using III-V compound semiconductors (GaAs, GaN or InP). Typically analog parts are realized using III-V technologies and silicon-based DSPs are assembled together on a printed-circuit board, similar to a commercial PC motherboard construction (Figure 1.4). Most of conventional applications of phased-arrays in defense and science sectors need very high power and extremely low-noise operations in the transmitter and receiver, respectively, resulting in exclusive use of III-V solutions to date. Another important reason for the III-V implementation is that the phase shifter, which is the most essential electronic element for phased-arrays, has been realized using passive components such as inductors, microstrip lines, and switches implemented with FET or diode. The III-V technology provides high-Q passive components, and low-loss high-isolation switches, resulting in high performance passive phase shifters at the expense of cost and chip area. However, it is still common perception that the phased-arrays in III-V technologies are too expensive for commercial applications. Recent breakthrough in silicon technologies, SiGe and CMOS, provides high potential to replace the III-V chips and brings the opportunity to lower the cost of phased-arrays substantially from current level [18, 19]. Especially SiGe materials have demonstrated comparable performances to III-V materials for lower-power electronics up to millimeter-wave frequency ranges. By leveraging silicon technologies and adopting commercial IC process, highly reliable and low-cost phased-arrays can be fielded, and eventually silicon technologies will integrate all the phased-array control electronics including RF, analog and digital parts, into a single chip.

## 1.2 Dissertation Objective

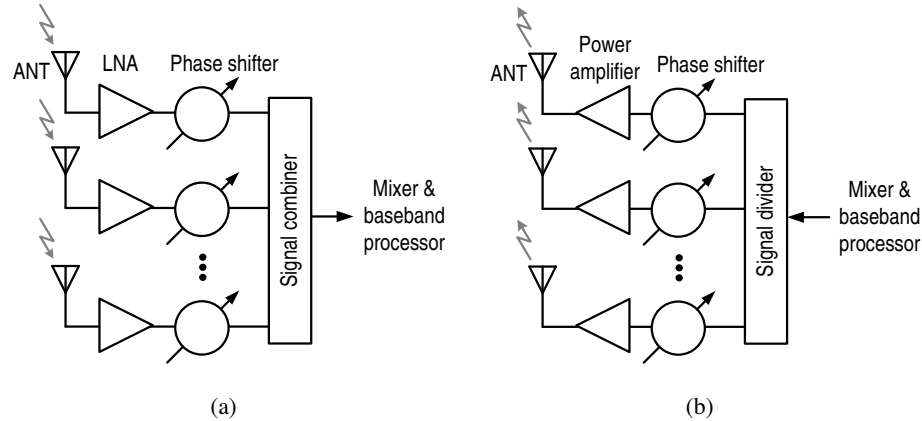
The main purpose of this dissertation is to develop phased-array transmitters and receivers using SiGe BiCMOS technology and to investigate technical difficulties of integrating phased-arrays on a silicon substrate. The goal is to demonstrate the possibility of silicon-based single-chip phased-array at RF, microwave and millimeter-wave frequency ranges. While the phase shifter is the most essential element in a phased-array, it is also a problematic building block when being integrated on a silicon chip. In conventional phased-arrays using III-V technologies, a low-loss phase shifter can be built using passive elements only, due to high-Q passive components and high-isolation (insulated) substrate. However, in silicon technology, the con-



ductive substrate causes significant loss for inductors and transistor switches, which results in a passive phase shifter with 10-20 dB loss depending on the operation frequency. In a system level perspective, the loss in the phase shifter causes several issues. First, in the receiver path, where the phase shifter is placed after the LNA [Figure 1.5(a)], the LNA should have very large gain to compensate the loss in the phase shifter and to result in a low system NF. In silicon technologies, especially in integrated designs, there is a complex trade-off between gain and noise figure, and linearity and power consumption. This means that the high loss in the phase shifter limits the overall dynamic range and also results in extra power consumption. Also, in the transmitter path



**Figure 1.4:** A 64-element (8×8) X-band Phased-array transmitter and its main features (developed by Boeing and presented at 2007 *Multi-function Phased-Array Radar Symposium*). The 64 elements, custom electronic components, analog and digital I/O devices are mounted in a printed wiring board, which distributes RF excitation, logic control signals, and power to each element. Each of the 64 elements contains three MMICs (a 4-bit RF phase shifter, a driver amplifier, and a dual power amplifier) in III-V technology, and an ASIC controller in silicon technology.

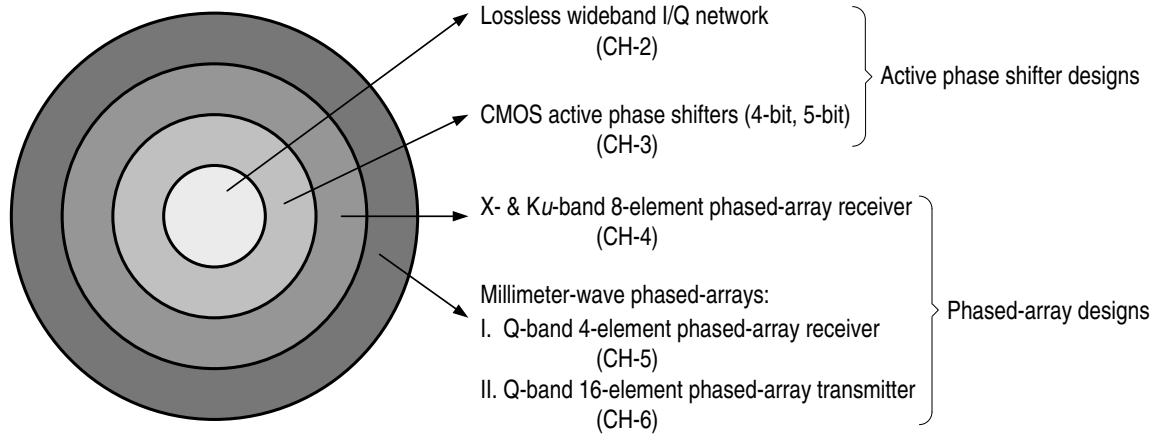


**Figure 1.5:** Simplified phased-array front-ends: (a) receiver front-end (b) transmitter front-end.

[Figure 1.5(b)], to compensate for the loss in the phase shifter, the power amplifier should be able to generate a larger output power, burning more DC current. High output power with decent efficiency is still very challenging in standard commercial silicon process. Another issue in conventional passive phase shifters is the size which tends to be too large for on-chip integration, resulting in a high cost factor. These difficulties present a fundamental issue for the integration of compact on-chip phased-arrays. To tackle these issues, substantial part of this dissertation is devoted to the development of a new phase shifter using an active approach which minimizes the chip size and loss with a constraint of low power consumption. A new lossless wideband quadrature signal generator is proposed and plays a key role in the successful operation of the active phase shifters. Signal combiners and dividers are also very important building blocks, since they can take substantial chip area and any error in these function blocks degrade output beam pattern. Therefore, various active and passive ways of signal combining and dividing techniques, suitable for integrated on-chip phased-arrays, are also investigated in this dissertation.

### 1.3 Dissertation Overview

Figure 1.6 presents the technical contents of this dissertation. First two chapters (Chapter 2 and Chapter 3) are dedicated to describe the active phase shifter designs at X-, Ku- and K-bands (6-26 GHz). The active phase shifter is based on the signal interpolation technique where two different in-phased (I) and quadrature-phased (Q) signals are added with different ampli-



**Figure 1.6:** Technical contents of the dissertation.

tudes to generate necessary output phase [20, 21]. The I/Q signal generator is a key element for accurate multi-bit phase states in the phase shifter, and a new wideband I/Q network is developed in Chapter 2. The proposed I/Q network utilizes a second-order L-C resonance to minimize loss and to extend the operation bandwidth, and Chapter 3 provides experimental verification of the I/Q network. Also, in Chapter 3, 4-bit (phase quantization level= $22.5^\circ$ ) and 5-bit (phase quantization level= $11.25^\circ$ ) active phase shifters adopting the new I/Q network are realized using  $0.13\text{-}\mu\text{m}$  and  $0.18\text{-}\mu\text{m}$  CMOS technologies. After successful demonstration of the active phase shifters, an eight-element phased-array receiver is developed in Chapter 4 for X- and Ku-band satellite communications. The phased-array receiver in Chapter 4 is based on the corporate-feed architecture implemented with active signal combiners, and realized in a  $0.18\text{-}\mu\text{m}$  SiGe BiCMOS technology. The phased-array design is extended to millimeter-wave frequencies in Chapter 5 and Chapter 6. In Chapter 5, four-element phased-array receiver is realized in the SiGe BiCMOS technology for Q-band applications (30-50 GHz). At millimeter frequencies, a Wilkinson combiner can be integrated on-chip for the signal combiner/divider function, and Chapter 5 also presents the successful implementation of a Wilkinson combiner for the phased-array receiver. As an effort to increase integration level, a sixteen-element phased-array transmitter is developed for Q-band applications in Chapter 6, marking the highest integration of phased-array elements known to-date. This high integration is due to the active phase shifter having very small form factor and also due to compact passive power dividers based on a coaxial-type shielded transmission line which is also detailed in Chapter 6. The dissertation is concluded in Chapter 7.

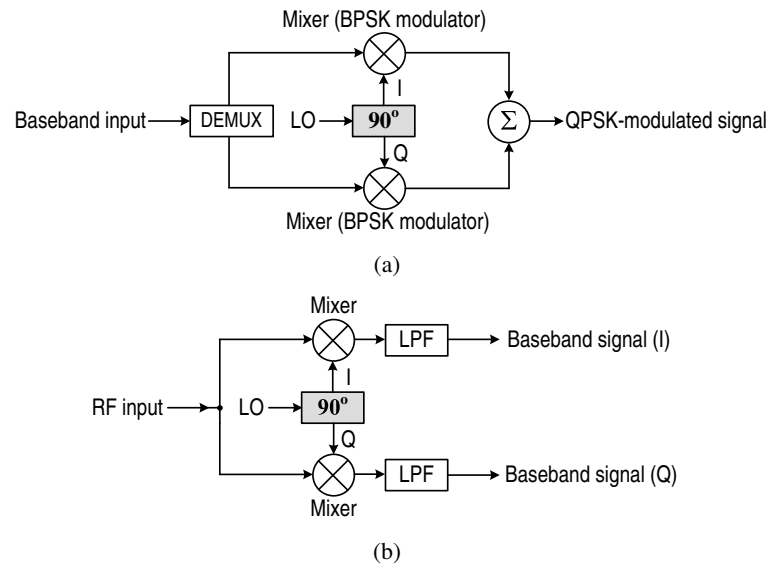
## 2

# L-C Resonance-Based Quadrature All-Pass Filter: Theory

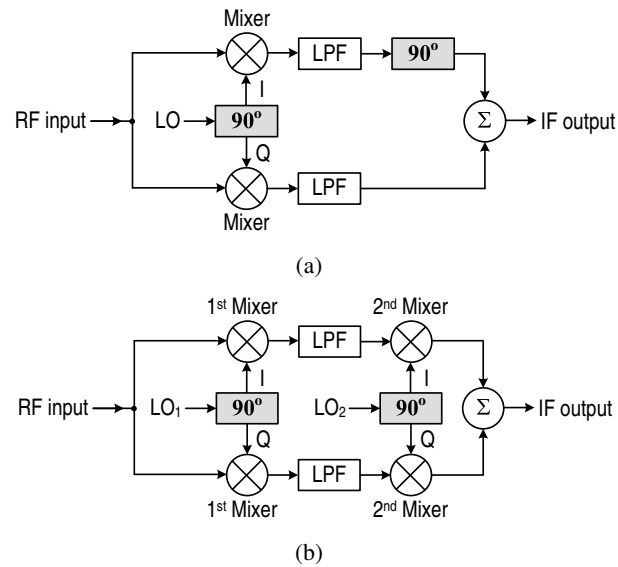
## 2.1 Introduction

An in-phased and quadrature-phased (I/Q) signals generator (or I/Q network) is a very versatile function block for many wireless communication systems [24, 25]. For instance, the  $90^\circ$  phase shifting is an essential function for quadrature phase-shift keying (QPSK) modulators or demodulators (Figure 2.1) [26, 27]. A quadrature phase shifter can also be used to differentiate image signals from the desired signal, and therefore, has been widely used for image rejection systems with complex mixers adopting Hartley or Weaver image-reject architecture (Figure 2.2) [28, 29]. Another useful application of  $90^\circ$  phase shifter is for agile polarization control of an electromagnetic wave [22], which is shown in Figure 2.3. If the phase of the vertical incident wave,  $E_V$  in Figure 2.3, is advanced by  $90^\circ$  compared with that of the horizontal incident wave,  $E_H$ , then the output signal after the combiner has *right-handed circular polarization* (RHCP), while the output signal will have *left-handed circular polarization* (LHCP) when the phase of  $E_V$  is lagged by  $90^\circ$  by the quadrature phase shifter. In general, thanks to the phase control by the  $90^\circ$  phase shifter, two independent RF signals can be transmitted at the same frequency with orthogonal linear or circular polarization, and this results in double the capacity of a communication system [30].

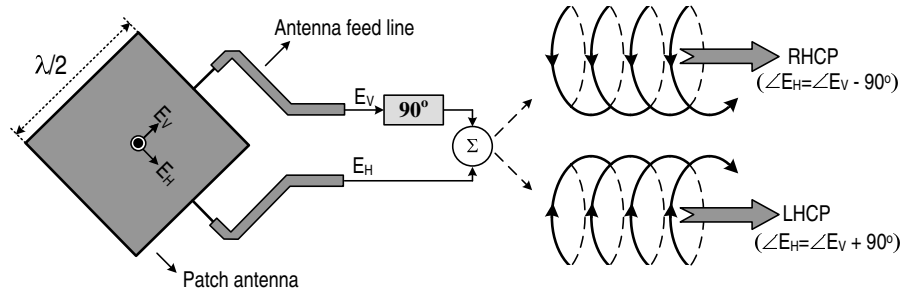
Another different use of the I/Q network is to develop a multiple-phased signal. As detailed in [31], as long as we have quadrature signals, called as *orthonormal basis* vectors,



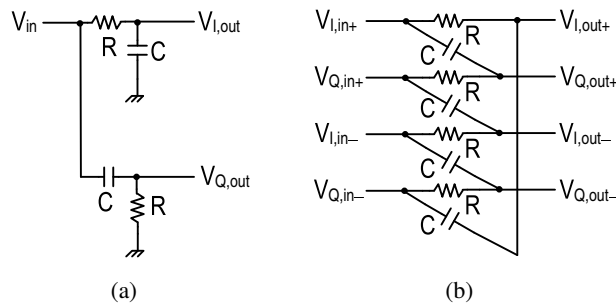
**Figure 2.1:** A simplified QPSK transceivers with  $90^\circ$  phase shifters in local-oscillator paths: (a) QPSK transmitter, (b) QPSK receiver.



**Figure 2.2:** Image rejection systems with complex mixers and  $90^\circ$  phase shifters: (a) Hartley image-reject receiver, (b) Weaver image-reject receiver.



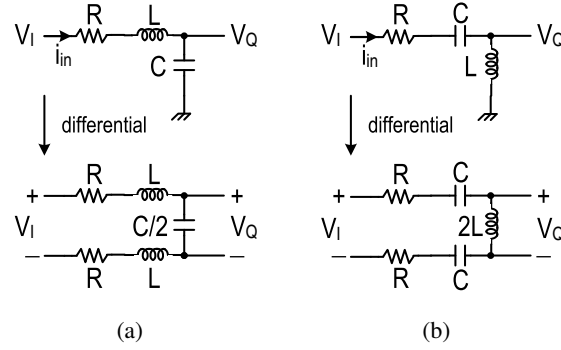
**Figure 2.3:** Wave polarization control using a  $90^\circ$  phase shifter in a circular-polarized antenna.



**Figure 2.4:** Typical R-C-based lumped passive quadrature networks: (a) RC-CR network, (b) R-C polyphase filter (one-stage).

any phase can be generated through a linear combination of the *orthonormal* vectors. If we define an *orthogonal basis* set as  $B = \{V_1, V_2\} = \{A\angle 0^\circ, A\angle 90^\circ\}$  then any signal  $V$  having the same frequency as that of the *basis* can be expressed as  $V = \alpha_1 V_1 + \alpha_2 V_2$ , where  $\alpha_i = \langle V_i, V \rangle / \langle V_i, V_i \rangle$  and  $\langle \cdot \rangle$  means the *Euclidean* inner product. The magnitude ( $|V|$ ) and phase ( $\angle \theta$ ) of  $V$  are  $|V| = A \sqrt{\alpha_1^2 + \alpha_2^2}$  and  $\angle \theta = \cos^{-1} \{ \alpha_1 / \sqrt{\alpha_1^2 + \alpha_2^2} \}$ , respectively, and therefore, the output phase can be controlled by changing the magnitude and polarity of the gain factors,  $\alpha_1$  and  $\alpha_2$ . Sometimes, this phasing technique is called “vector modulation” and will be detailed in the next chapter.

Usually the performance of communication systems adopting an I/Q network is dominated by the quadrature phase and amplitude accuracies of the I/Q network. The traditional RC-CR network has been widely used for narrowband quadrature signal generation [Figure 2.4(a)]. To extend the operation bandwidth, a multi-stage R-C polyphase filter of which a single stage is shown in Figure 2.4(b) has also been popular. However, although a polyphase filter provides a

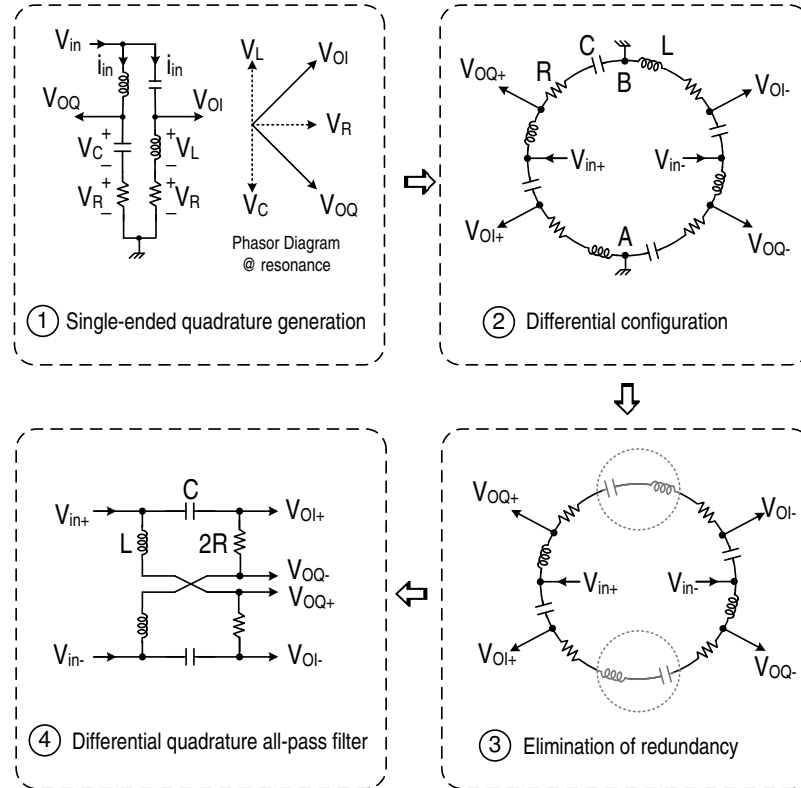


**Figure 2.5:** The L-C resonance-based quadrature networks: (a) low-pass form ( $V_Q$  is a low-pass of  $V_I$ ), (b) high-pass form ( $V_Q$  is a high-pass of  $V_I$ ).

solid way of quadrature generation and has been used in the LO or IF signal path where signal amplitude is large [28, 31, 32], its loss often prevents it from being used in the main RF signal paths. This is more true of multistage polyphase filters for wideband operations. To achieve high quadrature precision over wide bandwidth without sacrificing any signal loss, an L-C resonance based quadrature all-pass filter (QAF) is developed in this chapter [33].

## 2.2 Narrowband Lossless I/Q Network

Quadrature signals can be generated without any voltage loss by using an L-C resonance technique in passive circuits. Typical examples are shown in Figure 2.5, where  $R=\sqrt{(L/C)}$   $\{Q=\sqrt{(L/C)/R}=1\}$ , and L and C are resonated at a center frequency of  $\omega_o=1/\sqrt{(LC)}$ . When tapped on the top of capacitor [Figure 2.5(a)] or inductor [Figure 2.5(b)], the output signal [ $V_Q=1/j\omega Ci_{in}$  in Figure 2.5(a) and  $j\omega Li_{in}$  in Figure 2.5(b)] can be delayed or advanced by  $90^\circ$  with respect to the input signal ( $V_I=Ri_{in}$ ), without any voltage loss at  $\omega_o$ . However, in these R-L-C circuits, the phase of  $V_I$  undergoes a sharp transition near  $\omega_o$  due to the second-order resonance and this induces a quadrature phase error which grows quickly for any offset from  $\omega_o$ , limiting the operation bandwidth. The signal amplitude in the Q-path is also dependent on the low-pass and the high-pass characteristics in Figure 2.5(a) and Figure 2.5(b), respectively, causing I/Q amplitude error which also grows when the frequency deviates from  $\omega_o$ . The operation bandwidth can be increased with an all-pass form of the L-C resonance circuits, which is detailed in the following section.



**Figure 2.6:** Generation of the resonance-based second-order all-pass quadrature network. ①: single-ended I/Q network based on low-pass and high-pass topologies, ②: differential formation of ①, ③: elimination of redundancy by series resonance, and ④: the final form of differential all-pass filter.

## 2.3 Quadrature All-pass Filter (QAF)

### 2.3.1 Basic Operation: $Q=1$

Figure 2.6 shows a wideband lossless I/Q network design based on the second-order L-C resonance. As shown in step ①, the outputs of the single-ended I/Q network are tapped on the top of the two independent low-Q branches (instead of the high-Q branch of L and C as in the I/Q networks in Figure 2.5) to extend operation bandwidth at the expense of doubling the number of passive components, and the quadrature generation is based on the orthogonal phase splitting between  $V_{OI} (=j\omega Li_{in} + Ri_{in})$  and  $V_{OQ} (=1/j\omega Ci_{in} + Ri_{in})$  at resonance frequency in the series R-L-C resonators. The transfer function of the single-ended I/Q network is



$$\begin{bmatrix} V_{OI} \\ V_{OQ} \end{bmatrix} = V_{in} \times \begin{bmatrix} \frac{s \left( s + \frac{\omega_o}{Q} \right)}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \\ \frac{\frac{\omega_o}{Q} (s + Q\omega_o)}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \end{bmatrix}. \quad (2.1)$$

where  $\omega_o=1/\sqrt{LC}$ ,  $Q=\sqrt{L/C}/R$ , and  $s=j\omega$ . The benefits of this I/Q network are that it can guarantee  $90^\circ$  phase shift between I- and Q-paths for all  $\omega$  due to a zero at DC from the I-path transfer function, and it can achieve 3 dB voltage gain at resonance frequency when  $Q=1$ . The operating bandwidth is high due to the relatively low  $Q$ , albeit the I/Q output magnitudes are exact only at  $\omega=\omega_o$  as the quadrature relationships rely on the low-pass and high-pass characteristics. Even with these advantages, the single-ended I/Q network does not seem to be very attractive because the quadrature accuracy in the single-ended I/Q network is very sensitive to any parasitic loading capacitance, discussed further in this section.

Steps ② and ③ in Figure 2.6 show the transformation to a differential second-order all-pass configuration to increase the bandwidth and to make it less sensitive to loading effects. After building up the resonators differentially (step ②), opening nodes A and B from the ground replaces the ground with a virtual AC-ground, and eliminates the redundant series of L and C through series-resonance without causing any difference in the quadrature operation (step ③). The final form of the QAF (step ④) has a transfer function given by

$$\begin{bmatrix} V_{OI+} & V_{OI-} \\ V_{OQ+} & V_{OQ-} \end{bmatrix} = \begin{bmatrix} \frac{s^2 + \frac{2\omega_o}{Q} s}{s^2 + \frac{2\omega_o}{Q} s + \omega_o^2} & \frac{\omega_o^2}{s^2 + \frac{2\omega_o}{Q} s + \omega_o^2} \\ \frac{\frac{2\omega_o}{Q} s + \omega_o^2}{s^2 + \frac{2\omega_o}{Q} s + \omega_o^2} & \frac{s^2}{s^2 + \frac{2\omega_o}{Q} s + \omega_o^2} \end{bmatrix} \times \begin{bmatrix} V_{in+} & V_{in-} \\ V_{in-} & V_{in+} \end{bmatrix}. \quad (2.2)$$

As  $V_{in+}$  and  $V_{in-}$  constitutes a differential pair, the transfer function can be regarded as a linear superposition of the second-order low-pass and high-pass filters: i.e., while  $V_{OI+}$  shows high-pass characteristic in the view of  $V_{in+}$ , it also shows low-pass characteristics from the point of  $V_{in-}$ , and therefore, the linear combination of these characteristics leads to the all-pass operations. The I/Q transfer functions can be finalized as

$$\begin{bmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{bmatrix} = V_{in} \times \begin{bmatrix} \frac{s^2 + \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2} \\ \pm \frac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2} \\ \mp \frac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}s + \omega_o^2} \end{bmatrix} \quad (2.3)$$

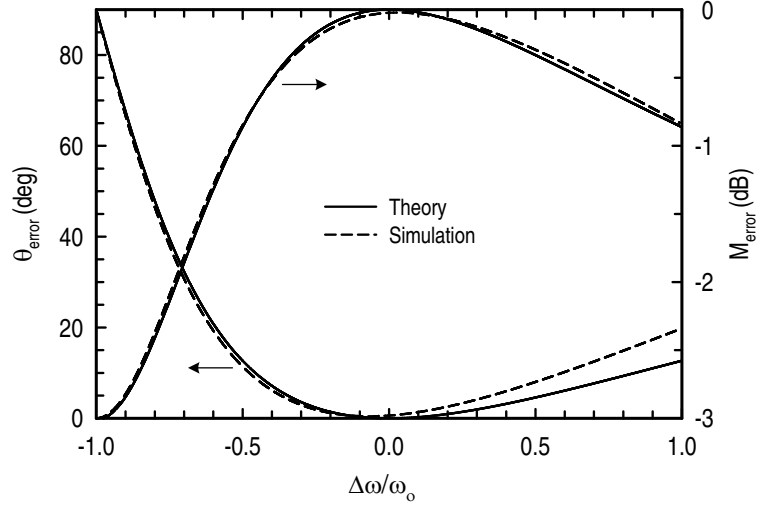
where  $V_{in}=V_{in+}=V_{in-}$ . The interesting point in (2.3), compared with (2.1), is that the Q is effectively divided by half and hence increasing the operation bandwidth, because of the elimination of a redundant series L-C during the differential implementation. Since both I- and Q-paths have the same characteristic function, the zeroes in (2.3) determine the phase difference between I- and Q-paths. The differential I/Q network shows  $|V_{OI\pm}|=|V_{OQ\pm}|$  for all  $\omega$  and generates exact  $90^\circ$  phase difference between the outputs at  $\omega=\omega_o$  which is the double-pole frequency of (2.3) when  $Q=\sqrt{(L/C)}/R=1$ . Actually, the QAF can generate any phase difference between the two outputs by changing the resistor value in Figure 2.6: i.e., in general, the replacement of R  $[=\sqrt{(L/C)}] \Omega$  with  $R \times \xi \Omega$  will generate  $2 \times \tan^{-1}(1/\xi)$  of phase difference between the output ports. When  $Q=1$  and  $\omega=\omega_o+\Delta\omega$ , where  $\Delta\omega$  is the frequency offset from the center frequency of  $\omega_o$ , (2.3) can be expanded as

$$\begin{bmatrix} V_{OI\pm} \\ V_{OQ\pm} \end{bmatrix} = V_{in} \times \frac{1}{\frac{\Delta\omega}{\omega_o} + \frac{1}{2} \left( \frac{\Delta\omega}{\omega_o} \right)^2 - j \left( 1 + \frac{\Delta\omega}{\omega_o} \right)} \times \begin{bmatrix} \pm \left\{ 1 + \frac{\Delta\omega}{\omega_o} + \frac{1}{2} \left( \frac{\Delta\omega}{\omega_o} \right)^2 - j \left( 1 + \frac{\Delta\omega}{\omega_o} \right) \right\} \\ \mp \left\{ 1 + \frac{\Delta\omega}{\omega_o} + \frac{1}{2} \left( \frac{\Delta\omega}{\omega_o} \right)^2 + j \left( 1 + \frac{\Delta\omega}{\omega_o} \right) \right\} \end{bmatrix}. \quad (2.4)$$

The phase error from the  $90^\circ$ -relationship between  $V_{OI\pm}$  and  $V_{OQ\pm}$  at  $\omega=\omega_o+\Delta\omega$ , defined as  $\theta_{error}=90^\circ-|\angle V_{OI\pm}-\angle V_{OQ\pm}|$ , can be expressed as

$$\theta_{error} = 90^\circ - 2 \times \tan^{-1} \left( \frac{1 + \frac{\Delta\omega}{\omega_o}}{1 + \frac{\Delta\omega}{\omega_o} + \frac{1}{2} \left( \frac{\Delta\omega}{\omega_o} \right)^2} \right) [\text{deg}]. \quad (2.5)$$

The circuit provides 3 dB voltage gain at  $\omega=\omega_o$  due to the resonance behavior of the QAF, and the gain error, defined as any deviation from the ideal value of 3 dB, i.e.,  $M_{error}=20 \times \log(V_{OI,OQ\pm}/V_{in})-3\text{dB}$ , can be given as

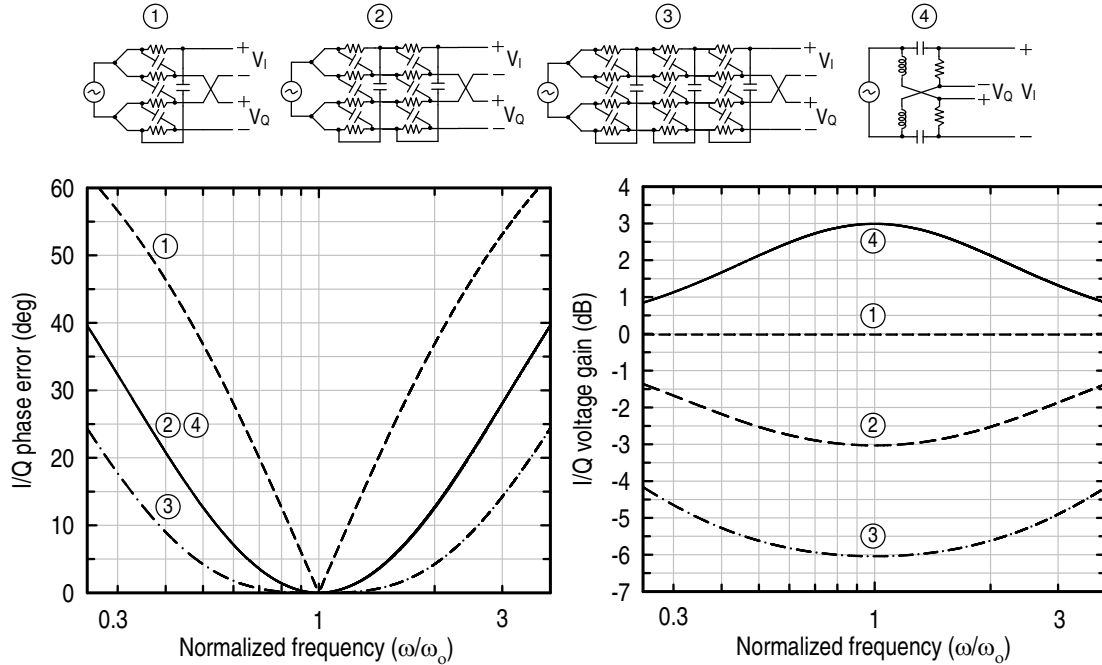


**Figure 2.7:**  $\theta_{error}$  in Eq. (2.5) and  $M_{error}$  in Eq. (2.6) versus the normalized offset frequency,  $\Delta\omega/\omega_o$ .  $L=639$  pH ( $Q=18$  @ 12 GHz,  $f_{SR}=50$  GHz),  $C=275$  fF and  $R=50$   $\Omega$  ( $f_o=12$  GHz).

$$M_{error} = 10 \times \log \left( \frac{1 + 2\frac{\Delta\omega}{\omega_o} + \frac{3}{2}\left(\frac{\Delta\omega}{\omega_o}\right)^2 + \frac{1}{2}\left(\frac{\Delta\omega}{\omega_o}\right)^3 + \frac{1}{8}\left(\frac{\Delta\omega}{\omega_o}\right)^4}{1 + 2\frac{\Delta\omega}{\omega_o} + 2\left(\frac{\Delta\omega}{\omega_o}\right)^2 + \left(\frac{\Delta\omega}{\omega_o}\right)^3 + \frac{1}{4}\left(\frac{\Delta\omega}{\omega_o}\right)^4} \right) \text{ [dB]}. \quad (2.6)$$

Since  $\theta_{error}$  and  $M_{error}$  depend on the higher-order terms of  $\Delta\omega/\omega_o$ , the error sensitivities to  $\Delta\omega$  are very small, resulting in wideband operation. Figure 2.7 presents the simulation results of  $\theta_{error}$  and  $M_{error}$  versus the normalized offset frequency  $\Delta\omega/\omega_o$ , and centered at  $\omega_o$ . The simulations were done by SPECTRE with process models,  $L=639$  pH ( $Q_{ind}=18.6$  @ 12 GHz and  $f_{SR}=50$  GHz),  $C=275$  fF,  $R=50$   $\Omega$  and  $f_o=12$  GHz, given by the IBM 0.13- $\mu\text{m}$  CMOS technology. Theoretically one can achieve less than  $5^\circ$  of  $\theta_{error}$  from -35% to about +50% variation of  $\Delta\omega$ , and  $|M_{error}|$  is less than 1 dB from -50% to over +100% variation of  $\Delta\omega$ . The theoretical values agree well with simulations. The discrepancy at high frequencies is due to the limited  $Q_{ind}$  of the given inductor.

It is noteworthy that the effective decrease of  $Q$  by half during the differential transformation of the QAF makes possible a real value of input impedance over a wider bandwidth and facilitates impedance matching. With input matched *differentially* to  $R$ , the input reflection coefficient ( $=\Gamma$ ) at  $\omega=\omega_o+\Delta\omega$  can be given as

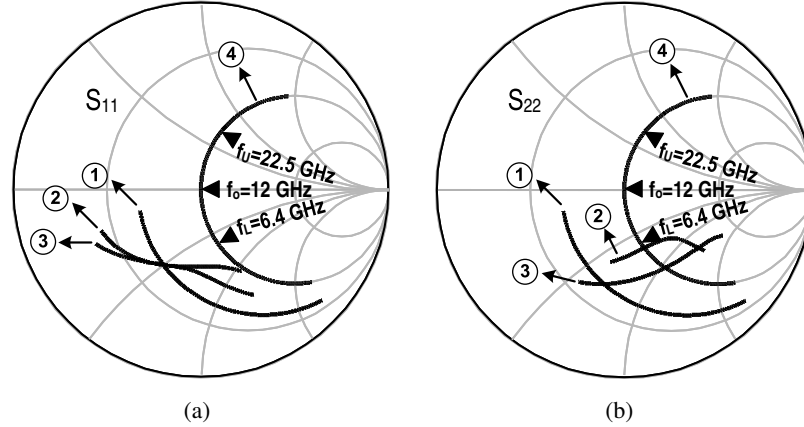


**Figure 2.8:** The performance comparison between QAF and R-C polyphase filters: quadrature phase error characteristics versus normalized frequency for the QAF and polyphase filters (*left*), and I/Q voltage gain characteristics at one of the I/Q outputs (*right*).  $R=50 \Omega$ ,  $C=265.26 \text{ fF}$ ,  $L=663.15 \text{ pH}$  and  $f_o=12 \text{ GHz}$ .

$$|\Gamma| = \left| \frac{R - Z_{in}}{R + Z_{in}} \right|, \quad Z_{in} = R \left\{ 1 + j \frac{Q}{2} \left( \left( 1 + \frac{\Delta\omega}{\omega_o} \right) - \left( 1 + \frac{\Delta\omega}{\omega_o} \right)^{-1} \right) \right\}. \quad (2.7)$$

Within  $-45\sim 80\%$  variation of  $\Delta\omega$ , (2.7) results in  $|\Gamma| < 0.3$ , corresponding to roughly below  $-10 \text{ dB}$  input return loss over more than  $100\%$  bandwidth.

Figure 2.8 shows a quadrature performance comparison between different polyphase filters and the QAF, when driven by ideal voltage source. For a fair comparison, the polyphase filters are also driven in an all-pass mode where the quadrature-phased differential input,  $V_{Q,in\pm}$ , is tied to the in-phased differential input,  $V_{I,in\pm}$  in Figure 2.4(b), resulting in equal I/Q amplitude for all  $\omega$  and quadrature phase splitting at the pole frequency ( $=1/RC$ ) [31]. The poles of each stage in the 2- and 3-stage polyphase filters are also set at the same value. The 3-stage polyphase filter shows the widest I/Q phase bandwidth at the expense of high loss. The I/Q phase error characteristic of the QAF is equivalent to that of the second-order polyphase filter but the QAF

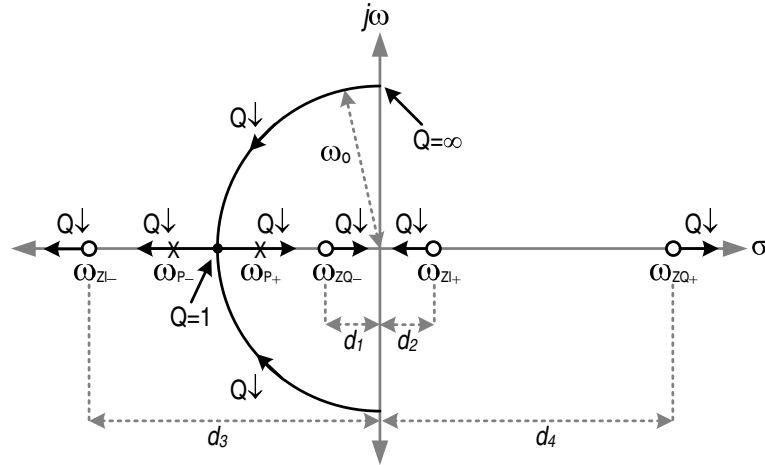


**Figure 2.9:** The input and output impedance characteristics of the I/Q networks shown in Figure 2.8: (a) input differential impedances, (b) output differential impedances for one of the I/Q outputs. Simulation frequency: 4.8–48 GHz ( $f_o=12$  GHz). For QAF,  $S_{11} < -10$  dB and  $S_{22} < -10$  dB at 6.4 GHz ( $0.53 \times f_o$ ) – 22.5 GHz ( $1.88 \times f_o$ ).

achieves 6 dB higher voltage gain than the second-order polyphase filter. The QAF can achieve more than 100% bandwidth with an I/Q phase error  $< 5^\circ$  and with  $> 2.6$  dB of voltage gain. Another major difference between the polyphase filters and the QAF is that the QAF provides a real input impedance over a wide bandwidth while the input impedance of the polyphase filter is capacitive, as mentioned. Figure 2.9 presents input and output impedance characteristics of the I/Q networks shown in Figure 2.8, and input and output return losses of the QAF are  $< -10$  dB over more than 240% bandwidth.

### 2.3.2 Bandwidth Extension: $Q < 1$

Figure 2.10 shows the pole-zero locus of the QAF as decreasing the  $Q$  in (2.3) and a slight lowering of the  $Q$  from 1 can split the double-pole into two separate negative real poles. The equations listed in (2.8) show the poles and zeroes of the transfer functions, where  $\omega_{P\pm}$  are the two left half-plane poles, and  $\omega_{ZI\pm}$  and  $\omega_{ZQ\pm}$  are the zeroes of the I- and Q-path transfer functions in (2.3), respectively. Regardless of  $Q$ , the zero locations are symmetric between the I- and Q-path transfer functions, which ensures equal I/Q amplitude for all  $\omega$ . For the quadrature phase splitting between I- and Q-path at a frequency of  $\omega_{IQ}$ , the difference of output phases contributed by each right half-plane zero of the transfer functions must be  $45^\circ$  at  $\omega=\omega_{IQ}$ . Another  $45^\circ$  contribution comes from the role of left half-plane zeroes at  $\omega=\omega_{IQ}$ . Equation (2.9) must



**Figure 2.10:** Pole-zero locus of the quadrature all-pass filter as decreasing  $Q$ . Regardless of  $Q$ , the zero locations are always symmetric between the I- and Q-paths ( $d_1=d_2$  and  $d_3=d_4$ ), resulting in equal I/Q amplitude for all  $\omega$ .

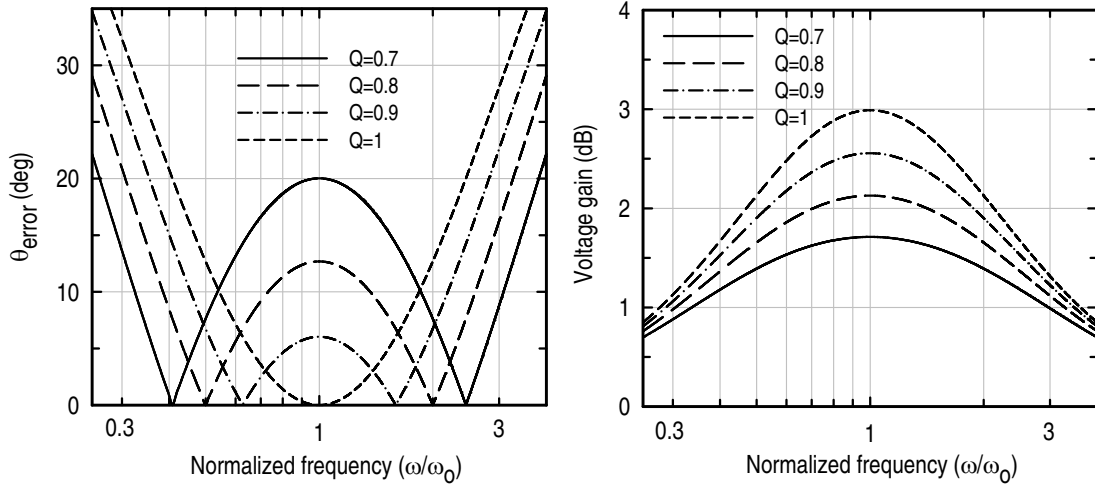
therefore be satisfied and the solutions are shown in (2.10).

$$\begin{pmatrix} \omega_{P\pm} = \left(-\frac{1}{Q} \pm \frac{1}{Q} \sqrt{1-Q^2}\right) \omega_o \\ \omega_{ZI\pm} = \left(-\frac{1}{Q} \pm \frac{1}{Q} \sqrt{1+Q^2}\right) \omega_o \\ \omega_{ZQ\pm} = \left(+\frac{1}{Q} \pm \frac{1}{Q} \sqrt{1+Q^2}\right) \omega_o \end{pmatrix}. \quad (2.8)$$

$$\tan^{-1} \underbrace{\left( \frac{\omega_{IQ}}{-\frac{\omega_o}{Q} + \frac{\omega_o}{Q} \sqrt{1+Q^2}} \right)}_{\text{output phase contribution from } \omega_{ZI+}} - \tan^{-1} \underbrace{\left( \frac{\omega_{IQ}}{+\frac{\omega_o}{Q} + \frac{\omega_o}{Q} \sqrt{1+Q^2}} \right)}_{\text{output phase contribution from } \omega_{ZQ+}} = 45^\circ. \quad (2.9)$$

$$\omega_{IQ} = \left( \frac{1}{Q} \pm \frac{1}{Q} \sqrt{1-Q^2} \right) \omega_o = -\omega_{P\pm}. \quad (2.10)$$

It is noted that if  $Q < 1$  in (2.3), which is possible by increasing  $R$  from the original value of  $\sqrt{L/C}$ , then one can obtain two frequencies where the QAF can generate exact  $90^\circ$  phase difference between the I/Q outputs, extending the operation bandwidth further, and these two frequencies are identical with the pole frequencies of the I- and Q-path transfer functions. When including  $Q$ , the  $\theta_{error}$  in (2.5) can be modified as



**Figure 2.11:** The characteristics of the quadrature all-pass filter: quadrature phase error versus normalized frequency with several values of  $Q$  (*left*), and voltage gain characteristics at each I- and Q-path of the QAF depending on the  $Q$  (*right*).

$$\theta_{error} = 90^\circ - 2 \times \tan^{-1} \left( \frac{\frac{2}{Q} \frac{\omega}{\omega_0}}{\left(\frac{\omega}{\omega_0}\right)^2 + 1} \right) \quad [\text{deg}] \quad (2.11)$$

where  $\omega/\omega_0$  is the normalized frequency. Figure 2.11 presents the QAF characteristics depending on  $Q$  versus the normalized frequency  $\omega/\omega_0$ . By decreasing  $Q$  from 1, one can get two frequency bands for the quadrature signal generation, which is a similar behavior to a two-stage polyphase filter having staggered poles to extend the operation band. By optimizing  $Q$ , hence by optimizing the  $R$  in the QAF, the I/Q signal bandwidth can be maximized with an acceptable I/Q error. For example, a 10% increase of  $R$  from the nominal value of  $\sqrt{(L/C)}$  corresponds to  $Q \simeq 0.91$ , and this generates  $< 5^\circ$  of  $\theta_{error}$  over  $0.55 \sim 1.85$  of  $\omega/\omega_0$ , achieving more than 200% bandwidth [Figure 2.11(*left*)]. The penalty in this bandwidth extension by the pole-splitting technique is a reduction of voltage gain which can be given as  $\sqrt{(1+Q^2)}$  at  $\omega_0$  [Figure 2.11(*right*)]. However, for practical applications with  $0.8 \leq Q \leq 1$ , the gain decrease is  $< 1$  dB from the ideal 3 dB voltage gain and this is acceptable for most cases.

### 2.3.3 Error Considerations

It is worthwhile to consider the quadrature errors caused by the loading effects on the QAF, which we have deliberately ignored for simplicity. Figure 2.12 addresses this prob-

lem conceptually in single-ended manner, where the parasitic loading capacitance ( $C_L$ ), mainly originating from the input gate capacitance of a transistor in the next stage, can modify the output impedances of  $Z_{OI}$  ( $R+j\omega L$ ) and  $Z_{OQ}$  ( $R+1/j\omega C$ ) differently. Intuitively,  $C_L$  will lower the loaded Q of a high-pass network,  $Z_{OI}$ , hence increasing the resistance and decreasing the inductance of  $Z_{OI}$ . Also,  $C_L$  will reduce the resistance and increase capacitance of the low-pass network,  $Z_{OQ}$ , hence increasing the loaded Q effectively. The by-products of these impedance modifications by  $C_L$  are the degradation of  $\Gamma$  and quadrature errors at the output. The phase and amplitude errors from this loading effect will be mainly dependent on the ratio of  $C_L/C$ , as given in (2.12) and (2.13), respectively, for the case of the single-ended I/Q network. The  $\Phi_{error}$  is defined in the same manner as  $\theta_{error}$  and  $A_{error}=|20\times\log(V_{OI}/V_{OQ})|$  at  $\omega=\omega_o$ .

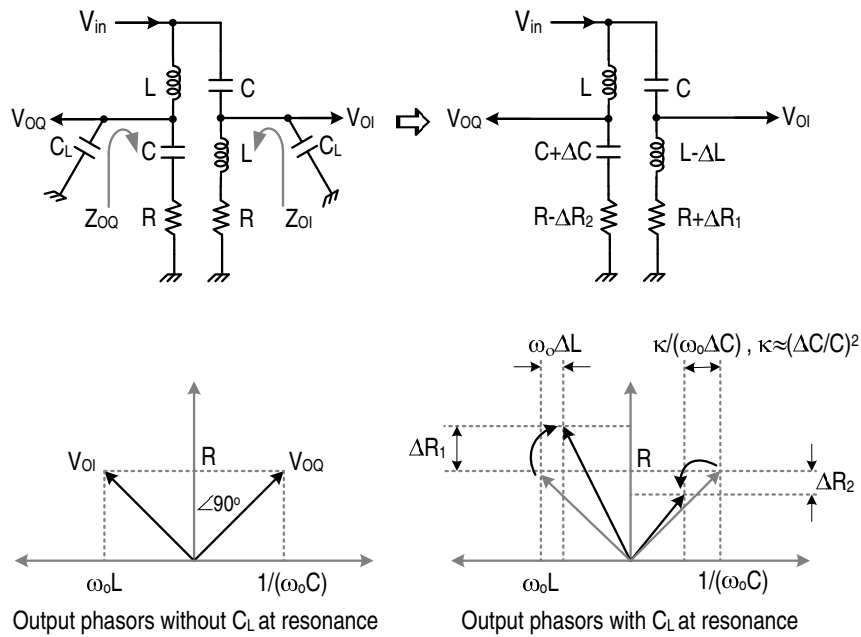
$$\Phi_{error} = 90^\circ - \left( \tan^{-1} \left( 1 - 2\frac{C_L}{C} \right) + \tan^{-1} \left( 1 + 2\frac{C_L}{C} \right) \right) \text{ [deg]}. \quad (2.12)$$

$$A_{error} = 10 \times \log \left( \frac{1 + 2\frac{C_L}{C} + 2\left(\frac{C_L}{C}\right)^2}{1 - 2\frac{C_L}{C} + 2\left(\frac{C_L}{C}\right)^2} \right) \text{ [dB]}. \quad (2.13)$$

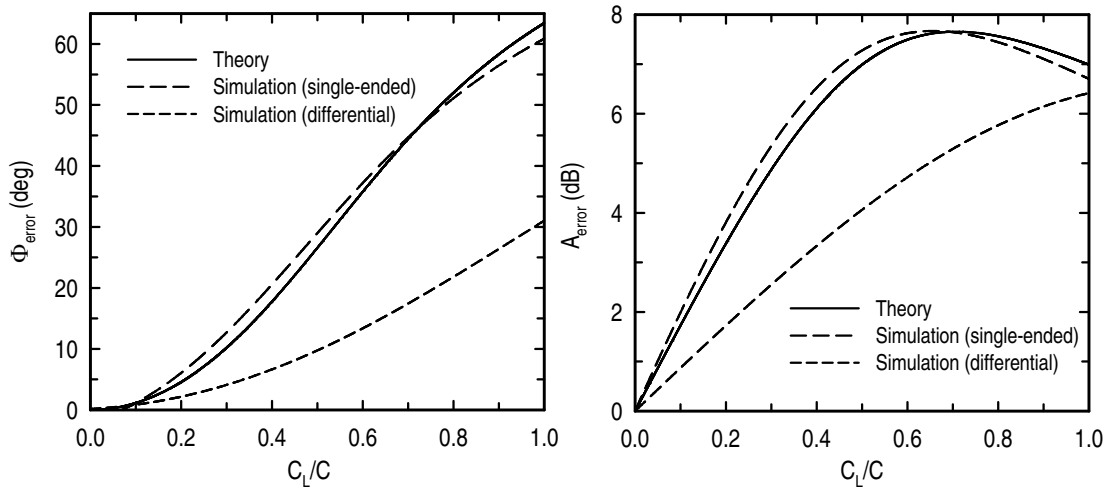
The all-pass mode differential configuration can suppress these errors because any output node impedance in Figure 2.6 is composed of low-pass and high-pass networks as mentioned, and provides counterbalances on the effect of  $C_L$ . Figure 2.13 shows the simulation results of the quadrature errors caused by  $C_L$  at  $f=f_o=12$  GHz for the single-ended and differential QAF, along with the theoretical values evaluated from (2.12) and (2.13). For the most practical range of  $C_L/C$  ( $\ll 1$ ), the differential I/Q network can reduce  $\Phi_{error}$  and  $A_{error}$  more than by half of that from the single-ended one.

As the capacitance of the QAF becomes smaller with increasing operating frequencies, the ratio  $C_L/C$  can go up to moderate values for high frequency applications, causing substantial errors. The lower impedance design of the QAF, where C can be increased while  $C_L$  kept constant hence diminishing  $C_L/C$ , can relieve this potential problem at the expense of more power consumption for driving the low impedance from the previous stage of the QAF. Another appropriate solution is to insert a unity gain buffer such as source follower or emitter follower after the QAF so that the loading capacitance  $C_L$  can be minimized. Figure 2.14 suggests another simple solution for the capacitive loading problem. The insertion of a series resistance  $R_s$  in the high-Q branches of C and L will reduce the network Q and its sensitivity to the loading





**Figure 2.12:** I/Q errors of the single-ended I/Q network due to capacitive loading.



**Figure 2.13:** Quadrature errors from the loading effect of  $C_L$  at  $f=f_0=12$  GHz: I/Q phase error (left), and I/Q amplitude error (right). All simulations were done by SPECTRE with foundry passive models given by IBM 0.13- $\mu$ m CMOS technology.  $L=639$  pH ( $Q_{ind}=18.6$  @ 12 GHz,  $f_{SR}=50$  GHz),  $C=275$  fF and  $R=48.2$   $\Omega$ .

capacitance. When including  $R_s$ , the I/Q transfer function of (2.3) is modified as (2.14), and  $R_s$  separates the negative real poles farther in Figure 2.10 through decreasing  $Q$  by  $(1+R_s/R)$ . The  $R_s$  does not disturb any zero location. Since the quadrature phase relation is set by the geometry of the zero positions, the I/Q phase characteristics of (2.14) are identical to those of (2.3).

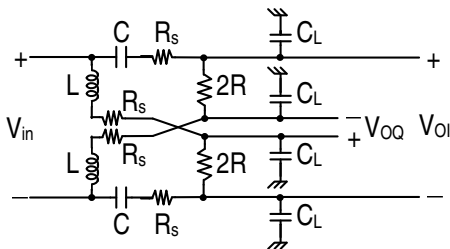
$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{in} \times \begin{bmatrix} \pm \frac{s^2 + \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}(1 + \frac{R_s}{R})s + \omega_o^2} \\ \mp \frac{s^2 - \frac{2\omega_o}{Q}s - \omega_o^2}{s^2 + \frac{2\omega_o}{Q}(1 + \frac{R_s}{R})s + \omega_o^2} \end{bmatrix} \quad (2.14)$$

Figure 2.15 shows simulated I/Q phase error (*left*) and I/Q magnitude mismatches (*right*) of the QAF with several values of  $R_s/R$  versus  $C_L/C$  at  $f_o=12$  GHz ( $R=50$   $\Omega$ ,  $C=265.26$  fF and  $L=663.15$  pH). The I/Q errors are suppressed with the increase of  $R_s$  and the QAF is perfectly insensitive to the parasitic capacitance when  $R_s=R$  at  $\omega_o$ . The penalty is loss as shown in Figure 2.16. The maximum loss to desensitize  $C_L$  perfectly at  $\omega_o$  is 3 dB when  $R_s=R$ . In reality, the choice of  $R_s$  depends on  $C_L/C$  which can be minimized with proper optimization of the QAF impedance and the loading transistor size. The added benefit of  $R_s$  is that it increases the QAF input impedance by  $(1+R_s/R)$  and relieves the loading on the previous stage.

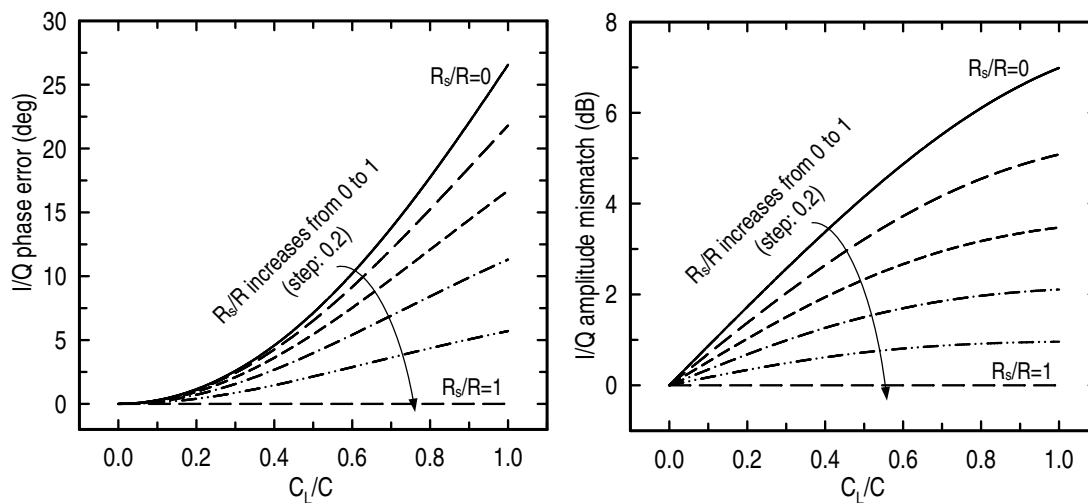
Finally, let us consider the quadrature errors due to R, L and C process variations in the QAF. To investigate the I/Q errors, the components are replaced by  $R+\Delta R_p$ ,  $L+\Delta L_p$  and  $C+\Delta C_p$  in Figure 2.6, and the quadrature phase error at  $\omega=\omega_o$  is given in (2.15).  $\Delta R_p$ ,  $\Delta L_p$  and  $\Delta C_p$  mean process deviations from the nominal values of R, L and C, respectively.

$$\begin{aligned} \theta_{\text{error}}|_{\Delta P} &= 90^\circ - 2 \times \tan^{-1} \left( \frac{2 \left(1 + \frac{\Delta C_p}{C}\right) \left(1 + \frac{\Delta R_p}{R}\right)}{1 + \left(1 + \frac{\Delta L_p}{L}\right) \left(1 + \frac{\Delta C_p}{C}\right)} \right) \\ &\simeq 90^\circ - 2 \times \tan^{-1} \left( \frac{1 + \frac{\Delta C_p}{C} + \frac{\Delta R_p}{R}}{1 + \frac{1}{2} \frac{\Delta L_p}{L} + \frac{1}{2} \frac{\Delta C_p}{C}} \right) \quad [\text{deg}]. \end{aligned} \quad (2.15)$$

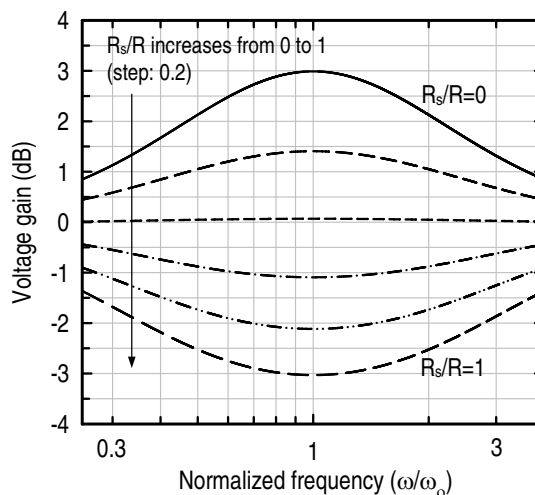
Considering the variations of  $|\Delta R_p/R| \leq 10\%$ ,  $|\Delta C_p/C| \leq 5\%$  and  $|\Delta L_p/L| \leq 5\%$  under the assumption of no loading capacitance, it is found that the I/Q phase error is  $|\theta_{\text{error},\Delta P}| < 10^\circ$  from (2.15) without any I/Q magnitude mismatch for all possible combinations of the process variations. When including about 20% of loading capacitance ( $C_L/C=0.2$ ), Monte-Carlo simulations



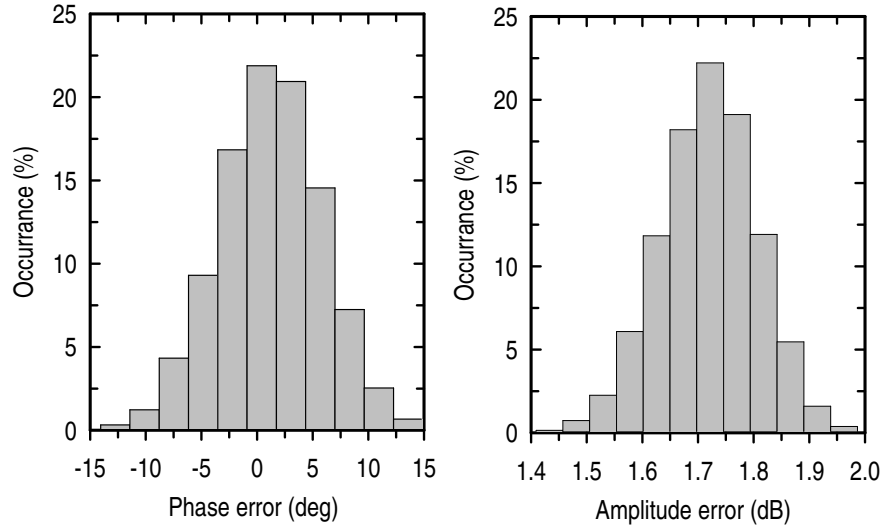
**Figure 2.14:** Reducing  $Q$  of the high- $Q$  branch of  $L$  and  $C$  by a insertion of  $R_s$  in the QAF to desensitize the loading capacitance  $C_L$ .



**Figure 2.15:** I/Q errors in the QAF under capacitive loading,  $C_L$ , with several values of  $R_s$  in Figure 2.14: I/Q phase errors (*left*), and I/Q amplitude mismatches (*right*).



**Figure 2.16:** Amplitude response of the QAF with the increase of  $R_s$  in Figure 2.14.



**Figure 2.17:** Monte-Carlo simulation results for I/Q errors in the QAF under process variations of R ( $\pm 10\%$ ), L ( $\pm 5\%$ ) and C ( $\pm 5\%$ ).  $C_L/C=0.2$ ,  $f_o=12$  GHz.

assuming Gaussian distributions of  $\Delta R_p/R=\pm 10\%$ ,  $\Delta C_p/C=\pm 5\%$  and  $\Delta L_p/L=\pm 5\%$  ( $L=663.15$  pH,  $C=265.26$  fF and  $2R=100$   $\Omega$  in Figure 2.6,  $f_o=12$  GHz), show about a maximum  $\pm 5^\circ$  of I/Q phase error within  $\pm 1\sigma$  statistical variations at the center frequency. The I/Q amplitude mismatch is  $1.7\pm 0.3$  dB for all statistical sample variations (Figure 2.17).

## 2.4 Conclusion

In this chapter, a new quadrature signal generator is proposed. The I/Q network utilizes a second-order L-C series resonance to generate I/Q signals, and its operation and performance are verified theoretically and in simulations using foundry process models. The fundamental benefit of this I/Q network, compared with conventional R-C-based quadrature generators, is that it can achieve maximum 3 dB of voltage gain with a wideband operation bandwidth. The proposed I/Q network is the essential building block when realizing phased-arrays in this thesis, and the performances are verified experimentally at various frequency bands in the following chapters.

## 2.5 Acknowledgements

This chapter is, in part, a reprint of:

- K.-J. Koh and G. M. Rebeiz, "0.13- $\mu\text{m}$  CMOS Phase shifters for X-, Ku- and K-Band Phased Arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.
- K.-J. Koh and G. M. Rebeiz, "6-18 GHz 5-Bit Active Phase Shifter," *IEEE Trans. Microwave Theory Tech.*, (in review).
- K.-J. Koh and G. M. Rebeiz, "A 0.13- $\mu\text{m}$  CMOS Digital Phase Shifter for K-band Phased Arrays," *IEEE RFIC Symp. Dig.*, pp. 383-386, June 2007.

I would like to thank my coauthor Prof. Gabriel M. Rebeiz.

# 3

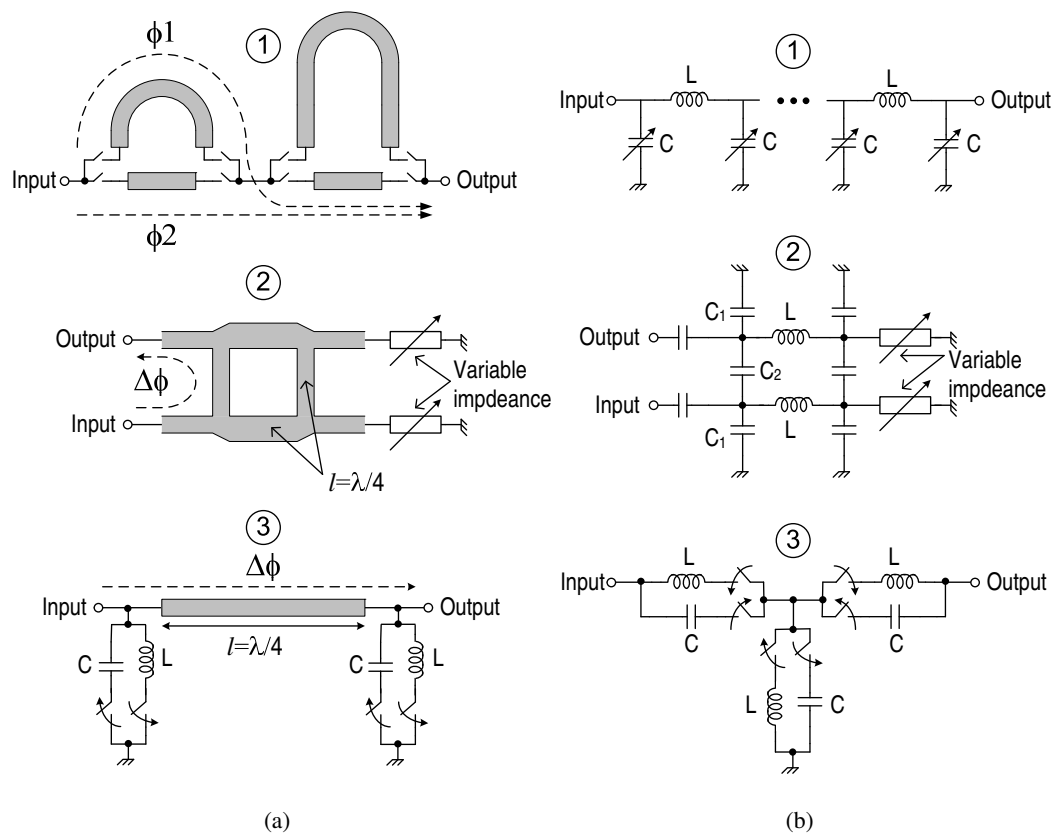
## Active Phase Shifter Designs in Silicon Technology

### 3.1 Introduction

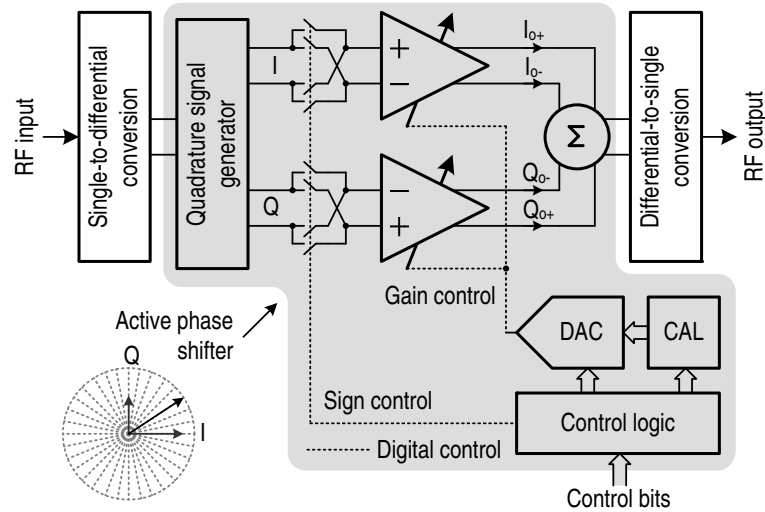
Electronic phase shifters, the most essential elements in the electronic beam-steering systems such as phased-array antennas, have been traditionally developed using switched transmission lines [34, 35] [Figure 3.1(a) ①], 90°-hybrid coupled-lines [36, 37] [Figure 3.1(a) ②], and periodic loaded-lines [38, 39] [Figure 3.1(a) ③]. However, even though these distributed approaches can achieve true time delay along the line sections, their physical sizes make them impractical for integration with multiple arrays in a commercial IC process, especially below K-band frequencies ( $\leq \sim 30$  GHz). The migrations from distributed networks to lumped-element configurations, such as synthetic transmission lines with varactors (and/or variable inductors) tuning [40, 41] [Figure 3.1(b) ①], lumped hybrid-couplers with reflection loads [42, 43] [Figure 3.1(b) ②] or the combined topologies of lumped low-pass filters and high-pass filters [44, 45] [Figure 3.1(b) ③], seem to reduce the physical dimensions of the phase shifters with reasonable performance achieved. However, for fine phase quantization levels over wide operation bandwidth, the size of the lumped passive networks grows dramatically, mainly for the various on-chip inductors used, and is not suitable for integrated phased array systems on a chip. Also, in most cases, the relationships between the control signal (voltage or current) and output phase of the lumped passive phase shifters are not linear, which makes the design of the control circuits to be quite complex [6]. The passive phase shifters by themselves achieve excellent linearity

without consuming any DC power, but their large insertion loss requires an amplifier to compensate the loss, typically more than two stages at high frequencies ( $\geq \sim 10$  GHz), which offsets the major merits of linearity and low power dissipation of the passive phase shifters.

Compared with passive designs, active phase shifters where differential phases can be obtained by the roles of transistors rather than passive networks, can achieve a high integration level with decent gain and accuracy along with a fine digital phase control under a constrained power budget [21, 46]. This chapter focuses on a compact 4-bit and 5-bit active phase shifter designs using the quadrature all-pass filter developed in the chapter 2.



**Figure 3.1:** Typical passive phase shifters: (a) transmission line approaches (①: switched transmission lines, ②:  $90^\circ$  branch-line hybrid coupler, and ③: periodic loaded line), (b) lumped element approaches (①: lumped synthetic transmission line, ②: lumped hybrid coupler, and ③: combination of lumped high-pass and low-pass topologies).



**Figure 3.2:** The active phase shifter architecture including balun blocks (single-to-differential and differential-to-single conversions) for a single-ended interface. The balun blocks are not necessary in fully differential integrated phased-arrays.

### 3.2 Active Phase Shifter Architecture

The phase shifter architecture presented in Figure 3.2 is pretty normal in active phase shifter designs, but implementation details on each function block are different for every case. Although sometimes called differently such as an endless phase shifter [46], a programmable phase shifter [21], a cartesian phase shifter [47] or a phase rotator [48], the underlying principle for all cases is to interpolate the phases of two orthogonal-phased input signals through adding the I/Q inputs for synthesizing the required phase. The different amplitude weights between the I- and Q-inputs result in different phases. Thus the basic function blocks of a typical active phase shifter are composed of a quadrature signal generator, an analog adder, and control circuits which set the different amplitude weights of I- and Q-inputs in the analog adder for the necessary phase bits.

The active phase shifter in Figure 3.2 is designed in differential mode, since a differential system provides more convenient way of  $360^\circ$  phase rotation than single-ended one. A differential input signal is split into quadrature phased I- and Q-vector signals using a quadrature signal generator. Two variable gain amplifiers (VGAs) consist a differential analog adder where the I/Q signals are added with with proper amplitude weights and polarities, giving an interpolated output signal with a synthetic phase of  $\angle \tan^{-1}(Q_{o\pm}/I_{o\pm})$  and magnitude of  $\sqrt{I_{o\pm}^2 + Q_{o\pm}^2}$ .

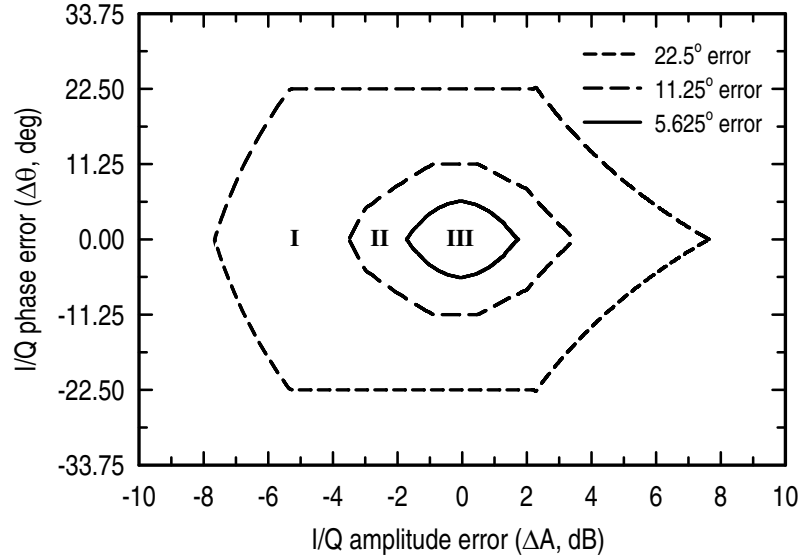


Since the output phase relies on the gain ratio between the I- and Q-paths, the output phase error resulting from the I/Q amplitude mismatch in the I/Q generator can be compensated by adjusting the I- and Q-path gains accordingly. This results in a robust design against process, supply voltage and temperature variations. To get multi-bit phase states, the different amplitude weights of each input of the adder can be accomplished through changing the gain of each VGA differently, and a digital-to-analog converter (DAC) is used to control the I/Q path gains digitally. In this architecture, the output phase resolution depends on the DAC resolution, and therefore, the active phase shifter can be fine-tuned by calibrating the DAC, which is done by the “CAL” in Figure 3.2. A CMOS logic encoder is implemented to synthesize the necessary control logic signals for the gain control in the DAC and for the sign control in the VGAs. The DAC is an indispensable element for fine digital phase controls in modern phased arrays. Increasing the phase quantization level needs more sophisticated gain control from a higher resolution DAC, but will not result in any significant increase of the phase shifter physical area. In this work, the DAC is designed to generate 4-bit phase states and the calibration path is used to achieve a 5-bit phase resolution.

Usually phase shifters are placed between stages in integrated phased-arrays and the single-to-differential and differential-to-single signal conversions are not inherent part of the active phase shifter. However, in stand-alone phase shifters, the baluns are preferable to be compatible with standard single-ended  $50\ \Omega$  input and output interfaces for measurement instruments.

### **3.3 Consideration of I/Q Accuracy of Quadrature Generator for the Phase Synthesis based on Signal Interpolation**

Phase synthesis based on the interpolation of two different vectors, called “vector modulator”, is a linear operation (i.e., *amplification* and *addition* of the reference vectors) and is independent of frequency, guaranteeing wideband operation. Actually, the two “basis” vectors do not need to be *orthonormal* as long as the amplitudes and polarities of the vectors can be controlled freely in a continuous way. However, This requires complex control to get accurate digitized multi-bit phase states [49]. Therefore, to avoid the control complexity phase shifters based on vector modulation adopt high precision quadrature networks, such as multistage polyphase filters or quadrature hybrid couplers [20, 21, 31, 47]. The fundamen-



**Figure 3.3:** The contour plot of I/Q errors (quadrature phase error,  $\Delta\theta$ , and amplitude mismatch,  $\Delta A$ ) in a quadrature network for guaranteeing 3-bit (region I,  $\theta_{error} < 360^\circ/2^4=22.5^\circ$ ), 4-bit (region II,  $\theta_{error} < 360^\circ/2^5=11.25^\circ$ ) and 5-bit (region III,  $\theta_{error} < 360^\circ/2^4=5.625^\circ$ ) accuracies in the interpolation-based phase shifter.

tal limitations of the phase accuracy and the operation bandwidth are given by those of the quadrature networks. To investigate the effect of the amplitude and phase errors in the quadrature network on the output phase accuracy, let's define a quadrature signal set as  $S_{IQ}=\{V_I, V_Q\}=\{A\angle 0^\circ, A\times\Delta A\angle(90+\Delta\theta)^\circ\}$ , where  $\Delta A$  and  $\Delta\theta$  are the I/Q amplitude mismatch and phase imbalance of the basis I/Q vectors  $V_I$  and  $V_Q$ , respectively. The linear combination of the reference vectors is  $V_{out}=G_I\times A\angle 0^\circ+G_Q\times A\times\Delta A\angle(90+\Delta\theta)^\circ$ , where  $G_I$  and  $G_Q$  are amplitude weights determined by the output phase  $\theta_{out}=\tan^{-1}(G_Q/G_I)$ . The phase error ( $\theta_{error}$ ) and amplitude error ( $M_{error}$ ) of the output signal are given by (3.1) and (3.2), respectively, with  $P_n=(G_Q/G_I)_n=\tan^{-1}(n\times 360^\circ/2^N)$  where  $N$ =number of phase bits; and  $n=0, 1, 2, \dots, 2^N-1$  ( $0 \leq P_n \leq \infty$ ,  $P_n=0$  for  $\theta_{out}=0^\circ$ ,  $P_n=1$  for  $\theta_{out}=45^\circ$  and  $P_n=\infty$  for  $\theta_{out}=90^\circ$ ).

$$\theta_{error}|_n = \tan^{-1}P_n - \tan^{-1}\left(P_n \times \frac{\Delta A \cos \Delta \theta}{(1 - P_n \Delta A \sin \Delta \theta)}\right) \quad (\text{deg}). \quad (3.1)$$

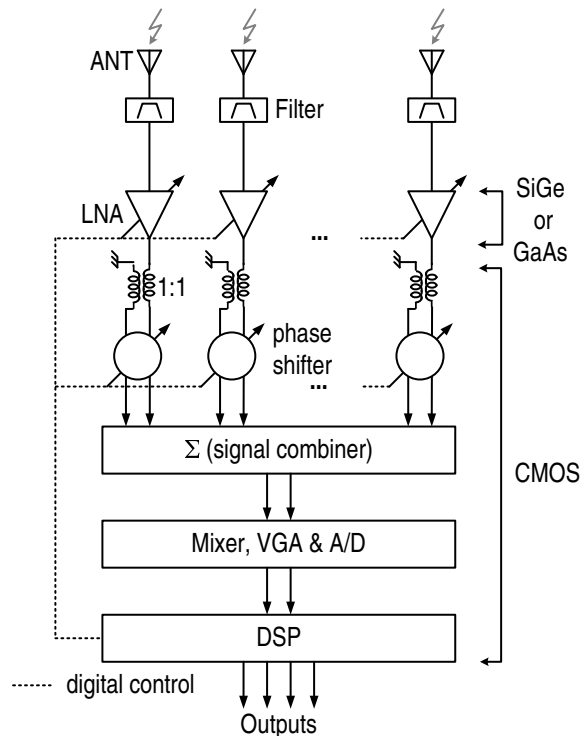
$$M_{error}|_n = 10 \log \left( \frac{1 + (P_n \Delta A)^2 - 2P_n \Delta A \sin \Delta \theta}{1 + P_n^2} \right) \quad (\text{dB}). \quad (3.2)$$

When  $P_n = \infty$  ( $+90^\circ$  phase bit),  $\theta_{error} = \Delta\theta$  and  $M_{error} = 20\log\Delta A$ , respectively, consistent with intuition ( $\tan^{-1}x \simeq \pi/2 - 1/x$ , if  $x \gg 1$ ).  $\theta_{error}$  should be  $< 360^\circ/2^{N+1}$  to avoid any phase overlap between different phase bits, guaranteeing  $N$ -bit phase resolution. Fig. 3.3 presents contour plots of  $\Delta A$  and  $\Delta\theta$  for several cases of  $\theta_{error}$ . To achieve 3-bit, 4-bit and 5-bit accuracies the I/Q errors should be inside of region I, II and III, respectively. To achieve 4-bit accuracy  $|\Delta\theta|$  should be less than  $10^\circ$  with  $|\Delta A| < 3$  dB approximately. For 5-bit phase accuracy, the  $|\Delta\theta|$  needs to be smaller than about  $5^\circ$  with maximum  $\pm 1.5$  dB of I/Q amplitude error in the quadrature network, which results in  $M_{error} < 2$  dB from (3.2).

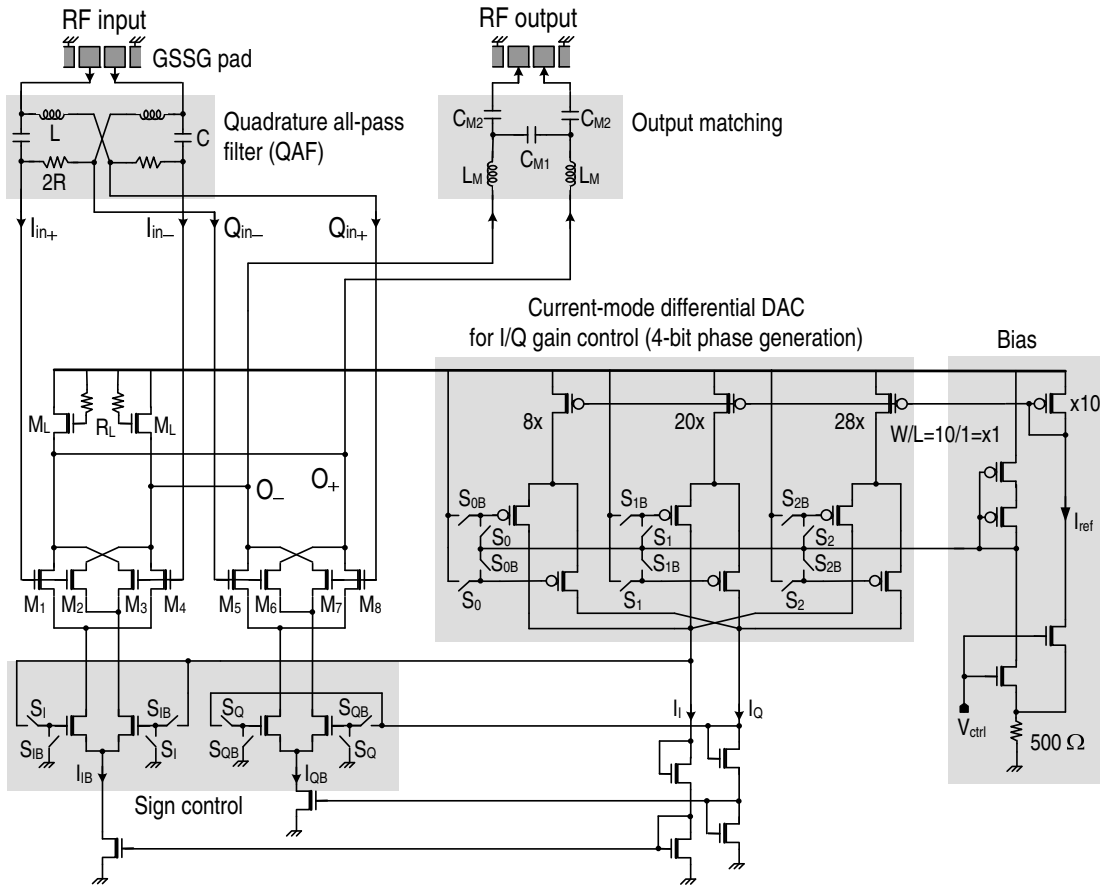
These are, however, rather theoretical considerations. The basic operation of the phase synthesis with a signal interpolation by adding two I/Q vectors is to chop the quadrature phase into a multiple of unity phase: i.e., the quadrature phase is divided into a multiple of  $360^\circ/2^N$  depending on the I/Q amplitude weights, rather than a real phase delay of a signal as in typical passive phase shifters. This means that the phase synthesis can guarantee output phase monotonicity as long as the I/Q amplitude weights,  $G_I$  and  $G_Q$ , are increased and/or decreased monotonically. This output phase monotonicity leads to stable  $N$ -bit phase resolution and accuracy without any phase overlap between the different phase states as long as  $|\theta_{error}| < 360^\circ/2^N$  (rather than  $360^\circ/2^{N+1}$ ), relaxing the I/Q accuracies for the finite phase resolution. In other words, as long as the phase monotonicity is ensured, the quadrature errors of the region I, II and III in Figure 3.3 will result in 4-bit, 5-bit and 6-bit accuracies, respectively. This monotonic output phase change is a fundamental merit of the interpolation-based active phase shifters over conventional passive phase shifter designs.

### 3.4 Design I: 4-Bit Active Phase Shifters in 0.13- $\mu\text{m}$ CMOS Technology

As a prototype implementation, two active phase shifters to be integrated on-chip with multiple phased-arrays for X-, Ku- and K-band (8-26 GHz) applications are designed in a 0.13- $\mu\text{m}$  RF CMOS technology ( $f_t \simeq 65\text{-}80$  GHz). The phase shifters in this section are designed under the system consideration shown in Figure 3.4. The phased-array adopts a single-ended SiGe or GaAs LNA having variable gain function, and the LNA sets the NF and gain of the RF part, required from the overall system perspective. The system includes transformer-based (1:1) on-chip baluns for differential signaling after the LNA. The active phase shifter shown in Figure 3.5 is fully differential and does not include DAC calibration path, “CAL” in Figure 3.2. The 4-bit differential phase shifter should provide about  $-5\sim 0$  dB of insertion loss and higher than  $-5$  dBm of input  $P_{1dB}$  level with less than 10 mW of power dissipation from a 1.5 V supply voltage. The input impedance of the phase shifter should be matched with the output impedance



**Figure 3.4:** Multiple antenna receiver for phased-array applications. A SiGe or GaAs LNA is used depending on the required system noise figure.



**Figure 3.5:** The schematic of 4-bit active phase shifter in 0.13- $\mu\text{m}$  CMOS technology.

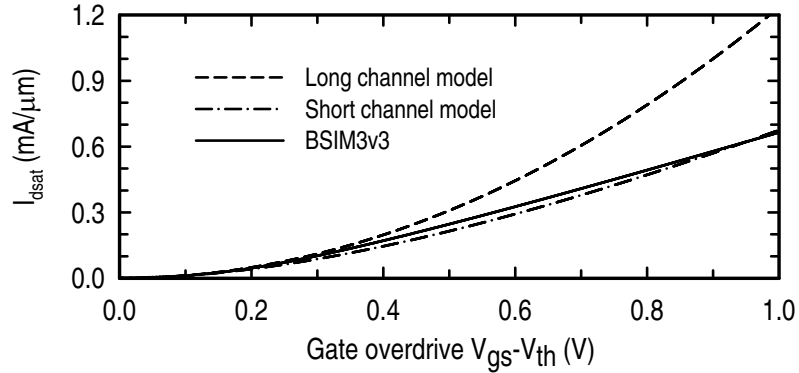
of the LNA ( $=50\ \Omega$ ). As the phase shifter will eventually be integrated on-chip with an active signal combiner network whose input impedance is capacitive ( $< 50\text{-}100\ \text{fF}$ , i.e., a gate input of following transistor), the output matching in the phase shifter is not necessary. However, the phase shifter should provide a digital interface to the DSP for 4-bit phase controls. The output matching circuits in Figure 3.5 is to provide differential  $100\ \Omega$  for measurement purpose only.

### 3.4.1 Circuit Design

**Quadrature All-pass Filter:** For the X- and Ku-band phase shifter, the QAF is designed with differential  $50\ \Omega$  ( $2R=100\ \Omega$  in Figure 3.5) for impedance matching with the previous stage. For  $f_o=12\ \text{GHz}$ , the final optimized values of L and C through SPECTRE simulations are  $L=698\ \text{pH}$  ( $Q_{ind}=18$  @ 12 GHz) and  $C=300\ \text{fF}$ . This takes into account about  $70\ \text{fF}$  of input GSSG pad capacitance and  $50\ \text{fF}$  of loading capacitance  $C_L$  which includes the input capaci-

tance of the following stage (a differential adder) and the parasitic layout capacitance. For the K-band phase shifter, the optimized passive component values are  $L=296$  pH ( $Q_{ind}=17.6$  @ 24 GHz),  $C=153.5$  fF and  $R=47.5$   $\Omega$  ( $2R=95$   $\Omega$  in Figure 3.5). The inductors are realized incorporating the parasitic layout inductance using the foundry models with full-wave electromagnetic simulations. With all the parasitic capacitances, Monte-Carlo simulations assuming Gaussian distributions of  $\Delta L_p/L$  ( $\pm 5\%$ ),  $\Delta C_p/C$  ( $\pm 5\%$ ) and  $\Delta R_p/R$  ( $\pm 10\%$ ), show about a maximum  $\pm 5^\circ$  of quadrature phase error within  $\pm 1\sigma$  statistical variations at 12 GHz. Within  $\pm 3\sigma$  variations, the maximum I/Q phase error is  $\pm 15^\circ$  and I/Q amplitude mismatch is  $1.2 \pm 0.3$  dB for the X- and Ku-band QAF. For the K-band design, the phase error distribution is  $-5^\circ \sim 13^\circ$  within  $\pm 1\sigma$  variations at  $f_o=24$  GHz. Within  $\pm 3\sigma$  variations, the phase error ranges from  $-15^\circ$  to  $+18^\circ$  and amplitude mismatch is  $2.3 \pm 0.6$  dB, which are just enough for distinguishing  $22.5^\circ$  of phase quantization levels.

**Analog Differential Adder (I/Q VGAs):** Two Gilbert-cells ( $M_{1-4}$  and  $M_{5-8}$ ) are merged at the output nodes,  $O_{\pm}$ , and constitute an analog differential adder. The  $V-I$  converted I- and Q-inputs from the QAF are added in the current domain at the output node of the adder, synthesizing the required phase. The size of the input transistors,  $M_{1-8}$  ( $W/L=40/0.12$ ), is optimized through SPECTRE simulations with respect of the linearity. The polarity of each I/Q inputs can be reversed by switching the tail current from one side to the other through turning on or off the tail NMOSs with switches  $S_I/S_{IB}$  and  $S_Q/S_{QB}$ . As the phase shifter is designed to be integrated with multiple arrays on-chip, the small form factor is a critical consideration, leading to the use of an active inductor load composed of  $M_L$  and  $R_L$ , instead of an on-chip spiral inductor. The equivalent output impedance from the active inductor load can be expressed as  $R_{eq} + j\omega L_{eq}$ , where  $R_{eq}=1/g_m$ ,  $L_{eq}=R_L \times (C_{gs} + C_{gd})/g_m$  [50]. The  $C_{gs}$  and  $C_{gd}$  are gate-source and gate-drain parasitic capacitances of the  $M_L$ , respectively, and  $g_m = \sqrt{\{\mu_{eff} C_{ox} W/L \times (I_{IB} + I_{QB})\}}$  is the transconductance of  $M_L$ .  $\mu_{eff}$  is the effective electron mobility and  $C_{ox}$  is the gate-oxide capacitance of NMOS, respectively. For measurement purposes only,  $L_M$ ,  $C_{M1}$  and  $C_{M2}$  constitute a wideband  $50$   $\Omega$  matching T-network (differentially  $100$   $\Omega$ ) of which maximum circuit node Q looking toward the  $50$   $\Omega$  load from the matching network is less than 1. The gain controls of the I- and Q-path of the adder for 4-bit phase resolution can be achieved by changing the bias current ratios between the two paths. Although the drain saturation current ( $I_{dsat}$ ) of a submicron CMOS varies more linearly with the gate overdriving of ( $V_{gs} - V_{th}$ ) rather than quadratically



**Figure 3.6:** Drain saturation current in 0.13- $\mu\text{m}$  NMOS versus gate overdriving expected from (3.3) and (3.4), along with the BSIM3v3 model given from the foundry.

as given in (3.3), the long channel quadratic  $I$ - $V$  model expressed in (3.4) still provides a good approximation for low-level gate overdriving [51].

$$I_{dsat} = C_{ox} W v_{sat} (V_{gs} - V_{th}) \frac{\sqrt{1 + 2\mu_{eff}(V_{gs} - V_{th})/(mv_{sat}L)} - 1}{\sqrt{1 + 2\mu_{eff}(V_{gs} - V_{th})/(mv_{sat}L)} + 1}. \quad (3.3)$$

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_{gs} - V_{th})^2}{2m}. \quad (3.4)$$

In (3.3) and (3.4),  $m$  is the body-effect coefficient given as 1.1-1.4 [51], and for the 0.13- $\mu\text{m}$  NMOS under considerations,  $v_{sat} = \mu_{eff} E_c$ ;  $\mu_{eff} = 270 \text{ cm}^2/\text{v}\cdot\text{s}$ ;  $E_c = 6 \times 10^4 \text{ V/cm}$ ;  $C_{ox} = 1.6 \text{ } \mu\text{F/cm}^2$ ;  $t_{ox} = 2.2 \text{ nm}$ ; and  $V_{th} = 0.36 \text{ V}$ . Figure 3.6 presents drain saturation currents calculated from the analytical models of (3.3) and (3.4), together with the simulation result which is expected from SPECTRE with 0.13- $\mu\text{m}$  NMOS model based on BSIM3v3 given from the foundry. Figure 3.6 shows that as long as the gate overdriving level is kept below about 0.5 V, which will be a usual case for low voltage small-signal applications, the conventional quadratic model still describes well the  $I$ - $V$  characteristic of the 0.13- $\mu\text{m}$  NMOS.

Viewed on the above discussions, the gain settings of the I- and Q-path of the adder for 4-bit phase resolution are based on the long channel model for simplicity and for better intuition. Due to the square-law gain dependency on bias current, the voltage gain ( $A_v$ ) at the phase shifter output is approximated as (3.5), and the output phase ( $\theta_{out}$ ) is determined by the I- and Q-paths bias current ratio given in (3.6).

**Table 3.1:** Logic Mapping Table for the Switch Controls

4-bit Input ABCD	Output Phase	Adder		I/Q-DAC			Control Logics
		S <sub>I</sub>	S <sub>Q</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	
0000	0°	+	x	+	+	+	S <sub>I</sub> =AB+ $\bar{A}\bar{B}$ S <sub>Q</sub> = $\bar{A}$
0001	22.5°	+	+	-	+	+	
0010	45°	+	+	-	-	+	
0011	67.5°	+	+	+	-	-	
0100	90°	x	+	-	-	-	S <sub>0</sub> = $\bar{B}CD+\bar{B}\bar{C}\bar{D}+B\bar{C}\bar{D}$ S <sub>I</sub> = $\bar{B}\bar{C}+BCD$
0101	112.5°	-	+	+	-	-	
0110	135°	-	+	-	-	+	
0111	157.5°	-	+	-	+	+	
1000	180°	-	x	+	+	+	S <sub>2</sub> = $\bar{C}\bar{D}+\bar{B}\bar{C}+BCD$ =S <sub>I</sub> + $\bar{C}\bar{D}$
1001	202.5°	-	-	-	+	+	
1010	225°	-	-	-	-	+	
1011	247.5°	-	-	+	-	-	
1100	270°	x	-	-	-	-	
1101	292.5°	+	-	+	-	-	
1110	315°	+	-	-	-	+	
1111	337.5°	+	-	-	+	+	

x=DON'T CARE, +=HIGH, -=LOW

$$A_v = 20 \log (\kappa \times \sqrt{I_{IB} + I_{QB}}) \quad (\text{dB}) \quad (3.5)$$

$$\text{where } \kappa = \sqrt{\mu_{eff} C_{ox} W/L} \times Z_{Load}.$$

$$\theta_{out} = \tan^{-1} \sqrt{\frac{I_{QB}}{I_{IB}}} \quad (\text{deg}). \quad (3.6)$$

In (3.5),  $W/L$  is the size of input NMOS  $M_{1-8}$  and  $Z_{Load}$  is the load impedance determined by the active inductor loads. For instance, a 6:1 ratio between  $I_{IB}$  and  $I_{QB}$  results in  $\sqrt{6}$ :1  $g_m$ -ratio between I- and Q-path of the adder leading to an output phase of  $\tan^{-1}(1/\sqrt{6}) \simeq 22.2^\circ$ , well matched with simulation results. This is only  $0.3^\circ$  error from the 4-bit resolution, indicating that the phase shifter can achieve a high accuracy by simple DC bias current controls.

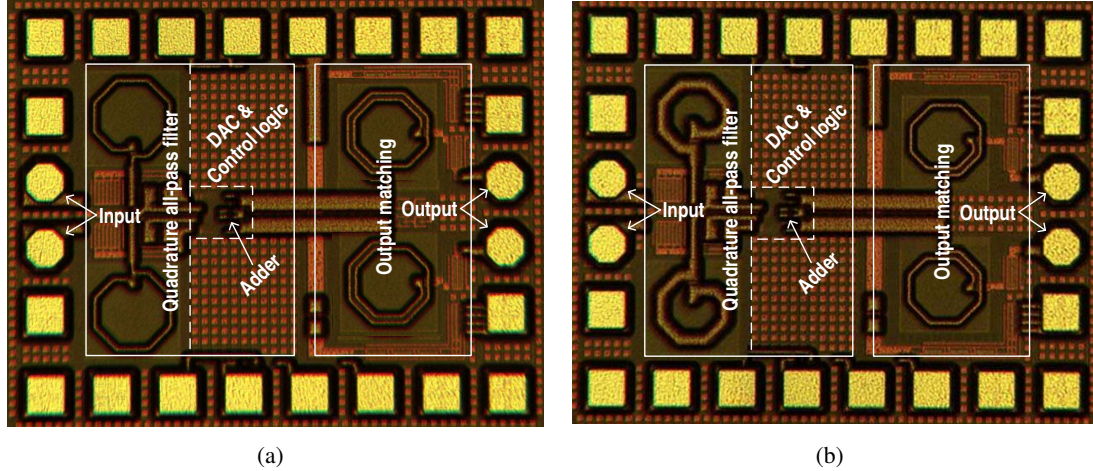
**4-Bit Phase Control:** A current mode differential DAC sets the bias current ratios of the I- and Q-paths of the adder by the cascode mirror in Figure 3.5. Table 3.1 shows the control logics for the PMOS switches,  $S_0$ ,  $S_1$  and  $S_2$  in the DAC, and NMOS switches,  $S_I$  and  $S_Q$  in the adder for 4-bit phase synthesis. ‘+’ means logically *high* (=on)-state and ‘-’ is logically *low* (=off)-state. The  $S_{nB}$ , where  $n=I, Q, 1, 2$  and  $3$ , is just the logic inversion of  $S_n$ . For  $0^\circ$ -state, by



setting  $S_I=S_0=S_1=S_2=high$ , all the DAC element currents are directed toward the I-path of the diode connected loads in the DAC, transferred to the only I-path of the adder with scaling up. In this case, switching status of  $S_Q/S_{QB}$  does not matter. Meanwhile, setting  $S_I=S_Q=S_1=S_2=high$  and  $S_0=low$  makes  $I_Q/I_I=I_{QB}/I_{IB}=1/6$  under the given scaling of the DAC current sources, resulting in  $22.5^\circ$  phase bit at the adder output. For  $45^\circ$ -bit, the binary status of all the switches shown in Table 3.1 makes an equal current ratio between the I- and Q-path in the DAC and in the adder. The differential architecture of the phase shifter makes  $0^\circ$ -,  $22.5^\circ$ - and  $45^\circ$ -bit to be fundamental bits, as the others can be obtained by switching the tail currents of these bits in the adder and/or in the DAC, which is clear in Table 3.1. For example, in Table 3.1 the  $67.5^\circ$ -bit is just the sign reversals of the switches,  $S_0$ ,  $S_1$ , and  $S_2$  of  $22.5^\circ$ -bit;  $0^\circ$ - and  $90^\circ$ -bit have also the same logic inversion relationships of the switches in the DAC; and etc. It should be emphasized that the logic and scaling of current sources of the DAC are set such that for all 4-bit phase states, the load current in the adder keeps constant value, i.e.,  $I_{IB}+I_{QB}=constant$  for all phase bits. This results in a constant impedance of the active inductor load, and the same amplitude response given in (3.5) for all phase states. So the phase can be changed with constant amplitude. To improve current matching, the DAC is designed with long channel CMOS ( $L=1 \mu m$ ). The control logics are implemented with static CMOS gates in AND-OR-INVERTER style.

For the X- and Ku-band phase shifter, the total bias current ( $=I_{IB}+I_{QB}$ ) in the differential adder is 5 mA from a 1.5 V supply voltage. This provides roughly  $R_{eq} \simeq 30 \Omega$  and  $L_{eq} \simeq 1.3$  nH ( $Q_{ind} \simeq 3.2$  @ 12 GHz) from the active inductor load with  $R_L=500 \Omega$  and  $W/L=100/0.12$  of  $M_L$ . In the SPECTRE simulations including I/O pad parasitics, the phase shifter shows  $-2\sim 0$  dB of differential voltage gain at 5-20 GHz. The peak gain variance is less than 2.4 dB and the worst case phase error at 12 GHz is  $< 5.2^\circ$  for all 4-bit phase states. The phase shifter achieves typically  $-4.7$  dBm of input  $P_{1dB}$  at 12 GHz. The  $S_{11}$  is  $< -10$  dB at 8-16.7 GHz and  $S_{22}$  is  $< -10$  dB at 6.7-16 GHz with  $L_M=691$  pH ( $Q_{ind}=18.5$  @ 12 GHz),  $C_{M1}=76.8$  fF and  $C_{M2}=535$  fF.

For the K-band phase shifter, with 7 mA of DC current in the adder, and with  $R_L=430 \Omega$  and  $W/L=50/0.12$  of  $M_L$  ( $R_{eq} \simeq 38 \Omega$  and  $L_{eq} \simeq 930$  pH), the differential voltage gain is  $-6\sim -2.5$  dB at 15-30 GHz in simulations. At 24 GHz, the peak gain error is  $< 3.5$  dB and the peak phase error is  $< 9.5^\circ$  for all phase bits. The input  $P_{1dB}$  at 24 GHz is  $-1.3$  dBm. The  $S_{11}$  is less than  $-10$  dB at 15-33 GHz and  $S_{22}$  is below  $-10$  dB at 15-28.2 GHz with  $L_M=364$  pH ( $Q_{ind}=17.2$



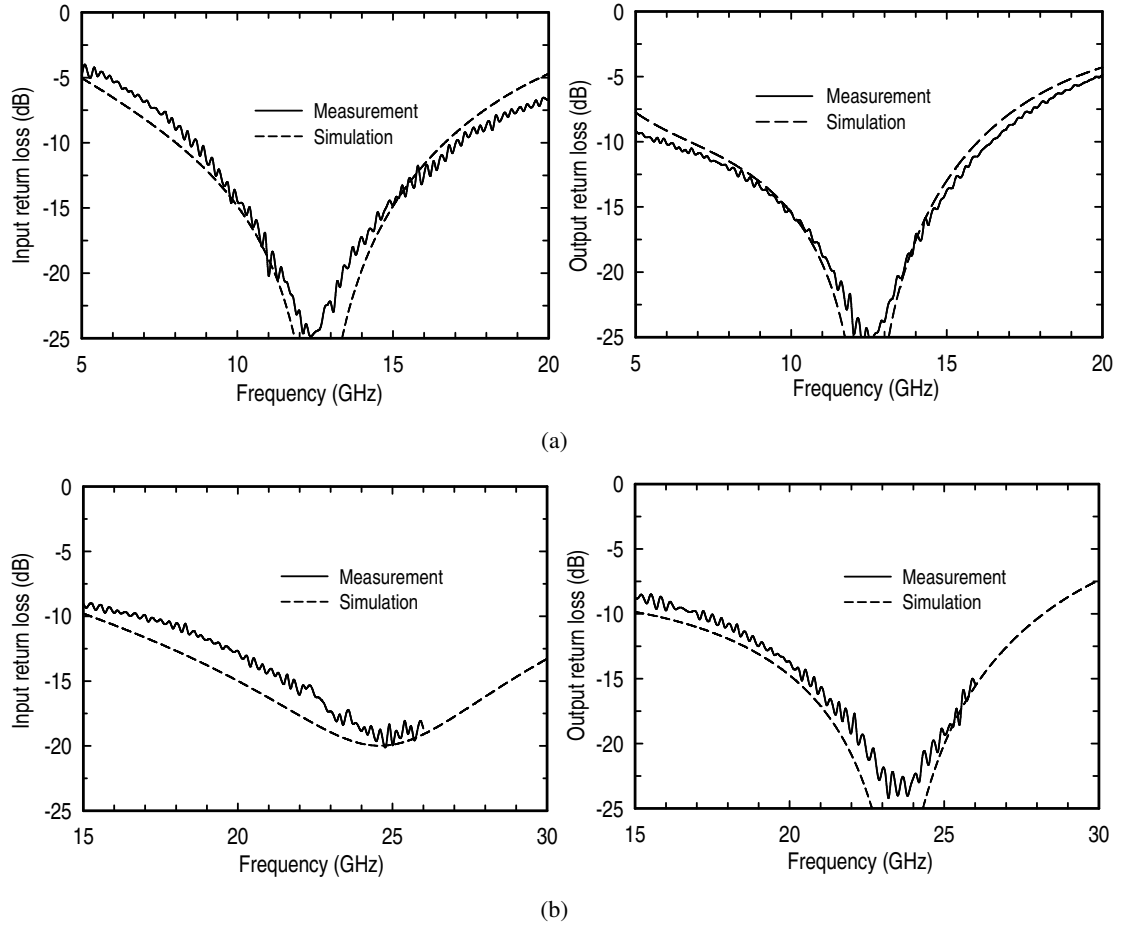
**Figure 3.7:** Chip microphotograph: (a) X- and Ku-band active phase shifter, (b)K-band active phase shifter. For both designs, the core size excluding output matching and pads is  $0.33 \times 0.43 \text{ mm}^2$ .

@ 24 GHz),  $C_{M1}=87.5 \text{ fF}$  and  $C_{M2}=535 \text{ fF}$  in the SPECTRE simulations.

### 3.4.2 Measured Results and Discussions

The active phase shifters are realized in IBM  $0.13\text{-}\mu\text{m}$  one-poly eight-metal (1P8M) CMOS technology. To improve signal balance, all the signal paths have symmetric layouts. The fabricated die microphotographs are shown in Figure 3.7. The core size excluding output matching networks for both phase shifters is  $0.33 \times 0.43 \text{ mm}^2$ , and the total size including all the pads and matching circuits is  $0.75 \times 0.6 \text{ mm}^2$ . The phase shifters are measured on-chip with external  $180^\circ$  hybrid couplers (Krytar, loss=0.5-1.5 dB, amplitude imbalance= $\pm 0.7$  dB, and phase imbalance= $\pm 12^\circ$  @ 5-26 GHz) for differential signal inputs and outputs. The balun loss is calibrated out with a standard differential SOLT calibration technique using a vector signal network analyzer (Agilent, PNA-E8364B).

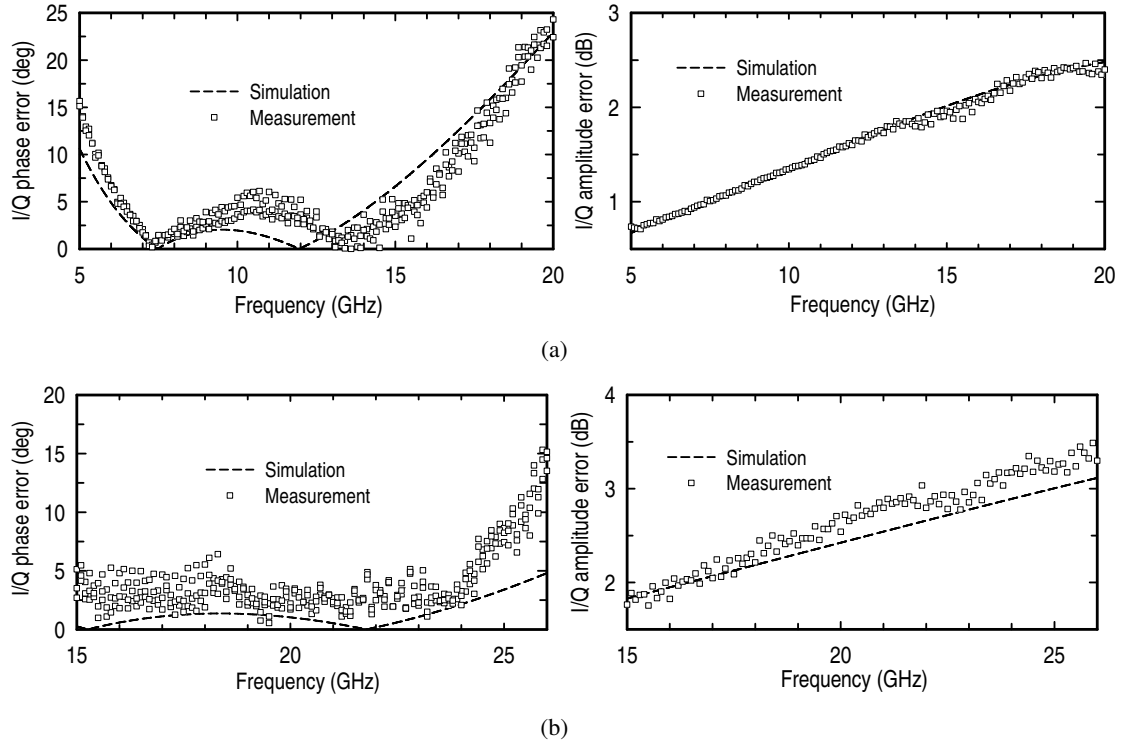
As the input reflection coefficient is dominantly set by the quadrature network, a changing phase at the adder does not disturb the  $S_{11}$  characteristic. The  $S_{22}$  characteristics also do not change for different phase settings, as the output load currents are same for all phase states, resulting in a constant output impedance from the active load as discussed. Figure 3.8 displays the typical measurement results of the input and output return losses, together with the simulation curves. For X- and Ku-band phase shifter, the  $S_{11}$ , converted into differential  $50 \Omega$



**Figure 3.8:** Measured input and output return losses of the active phase shifters: (a)  $S_{11}$  and  $S_{22}$  of X- and Ku-band phase shifter, (b)  $S_{11}$  and  $S_{22}$  of K-band phase shifter.

reference using ADS, is below -10 dB from 8.5 GHz to 17.2 GHz. In differential  $100 \Omega$  reference, the phase shifter shows less than -10 dB of  $S_{22}$  from 6.3 GHz to 16.5 GHz range. For the K-band phase shifter, the measured  $S_{11}$  is below -10 dB at 16.8-26 GHz and the  $S_{22}$  is less than -10 dB at 17-26 GHz. The external  $180^\circ$  hybrid couplers limit the maximum measurement frequency for the K-band case.

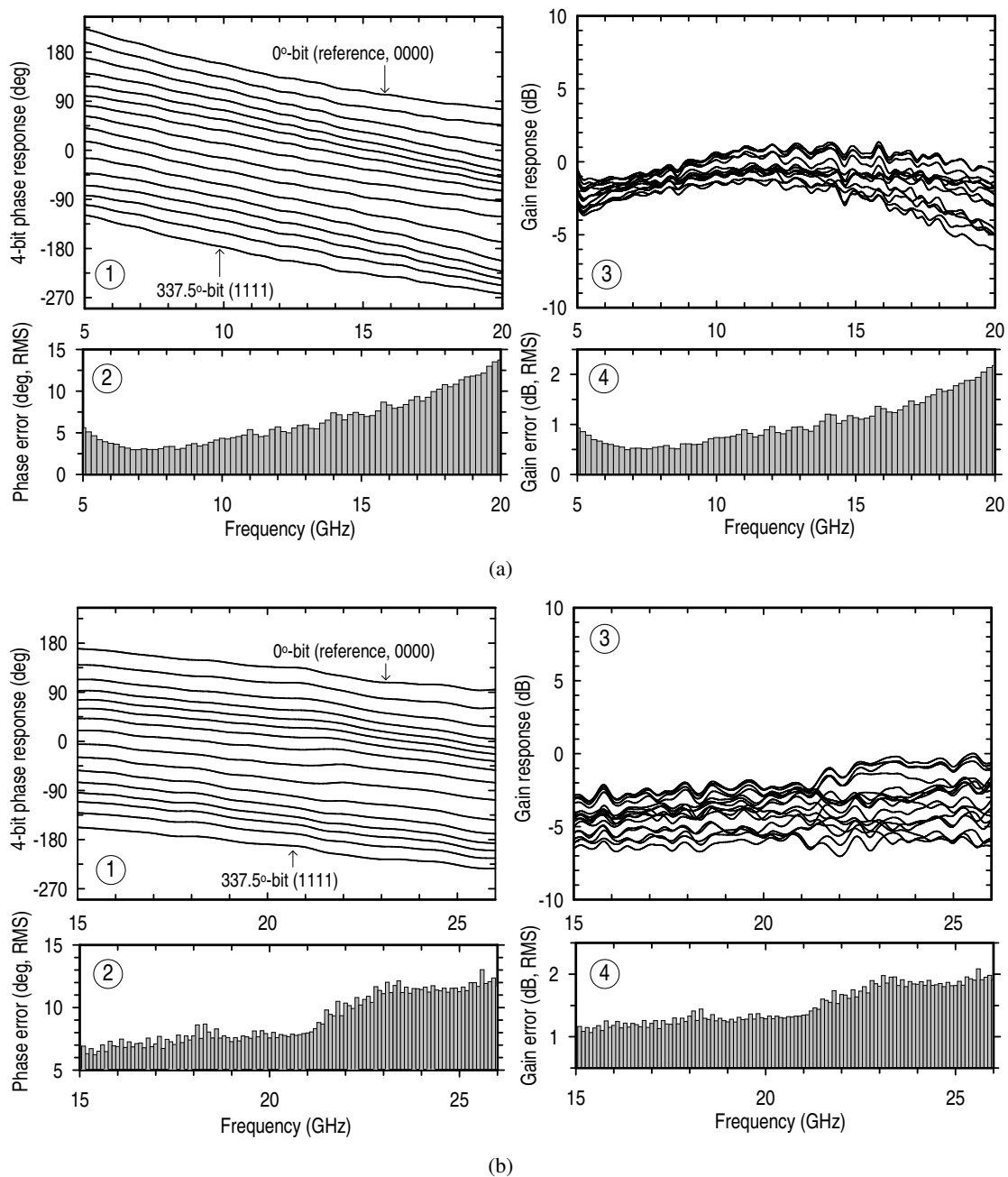
**QAF Characteristics:** The measurement of  $0^\circ$ -/ $180^\circ$ - and  $90^\circ$ -/ $270^\circ$ -bit at the final output of the phase shifters should reflect the QAF characteristics exactly (Figure 3.9). The dashed curves correspond to simulations with 50 fF loading capacitance. For the QAF of the X- and Ku-band phase shifter, the peak I/Q phase error is less than  $5.5^\circ$  and gain error is less than 1.5 dB at 12 GHz. The  $10^\circ$  phase error frequency range is from 5.5-17.5 GHz. The peak I/Q gain



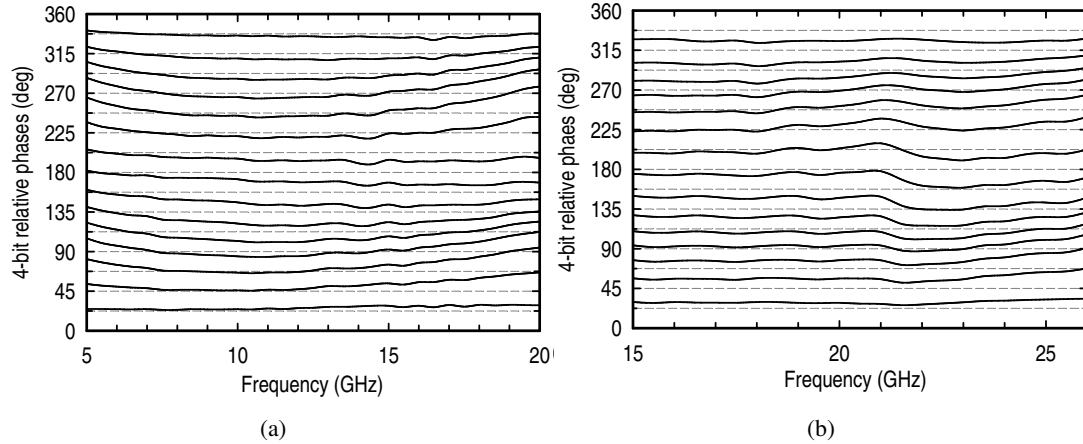
**Figure 3.9:** Quadrature error characteristics of the QAFs measured at the output of the adder: (a) I/Q phase and amplitude errors of the X- and Ku-band QAF, (b) I/Q phase and amplitude errors of the K-band QAF.

error at 5-20 GHz is less than 2.4 dB. For the K-band QAF, the quadrature phase error varies from  $2.7^\circ$  at 15 GHz to maximum  $15.2^\circ$  at 26 GHz. The I/Q amplitude error of the K-band QAF is 1.76-3.3 dB at 15-26 GHz.

**X- and Ku-band Phase Shifter:** For the X- and Ku-band phase shifter, Figure 3.10(a) shows the frequency responses of the unwrapped insertion phases and power gain according to the 4-bit digital input codes, measured from 5 GHz to 20 GHz. At 12 GHz, the measured peak-to-peak phase error is  $-8.5\sim 9.1^\circ$ . The peak-to-peak insertion gain is  $-1.5\sim 1.2$  dB for all phase state at 12 GHz, and the average differential gain ranges from -3 dB at 20 GHz to -0.2 dB at around 11-12 GHz [Figure 3.10(a)(3)]. The peak-to-peak gain variations are minimum 1.4 dB at 7 GHz and maximum 5.4 dB at 20 GHz. The major concern in phase shifter designs is the root-mean-square (RMS) value of the phase errors, and referenced to  $0^\circ$ -bit which results from a 0000 digital input code, the RMS value of phase errors can be defined as



**Figure 3.10:** Measured performances of the active phase shifters: (a) X- and Ku-band phase shifter (①: 4-bit phase response, ②: RMS phase error, ③: power gain and ④: RMS gain error), (b) K-band phase shifter (①: 4-bit phase response, ②: RMS phase error, ③: power gain and ④: RMS gain error).



**Figure 3.11:** Measured 4-bit relative phases referred to  $0^\circ$ -bit: (a) 4-bit relative phases of X- and Ku-band active phase shifter, (b) 4-bit relative phases of K-band active phase shifter. Grey dashed-lines are ideal 4-bit phases.

$$\theta_{\Delta,\text{rms}} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^N |\theta_{\Delta i}|^2} \quad (\text{deg}). \quad (3.7)$$

where  $N=16$  and  $\theta_{\Delta i}$  means the  $i$ th output phase error from the ideal phase value corresponding to the  $i$ th digital input sequence in Table 3.1. Similarly the rms gain error can be defined as

$$A_{\Delta,\text{rms}} = \sqrt{\frac{1}{N} \times \sum_{i=1}^N |A_{\Delta i}|^2} \quad (\text{dB}). \quad (3.8)$$

where  $A_{\Delta i}(\text{dB})=A_{vi}(\text{dB})-A_{ave}(\text{dB})$ . The  $A_{vi}$  is  $i$ th insertion gain in dB-scale corresponding to  $i$ th digital input order and  $A_{ave}$  is the average insertion gain in dB-scale also. The RMS values of phase error and gain error, calculated at each measured frequency, versus operating frequency are also shown in Figure 3.10(a) and 3.10(b), respectively. The phase shifter exhibits less than  $5^\circ$  RMS phase error from 5.3 GHz to about 12 GHz [Figure 3.10(a)(2)]. The  $10^\circ$  RMS error frequency range goes up to 18 GHz, achieving 5-bit accuracy across more than 100% bandwidth. The RMS gain error is less than 2.2 dB for 5-20 GHz [Figure 3.10(a)(4)]. The phase shifter achieves  $-5.4 \pm 1.3$  dBm of input  $P_{1dB}$  at 12 GHz for all 4-bit phase states with 5.8 mA of DC current consumption from a 1.5V supply voltage.

**K-band Phase Shifter:** Figure 3.10(b) shows the measured insertion phases and gain

**Table 3.2:** Performance Summary of the X- and Ku-band 4-bit CMOS Active Phase Shifter

Quantity	Results
Technology	0.13- $\mu$ m CMOS (1P8M)
Phase resolution	4-bit
Frequency band	6-18 GHz
Power consumption	8.7 mW ( $I_{DC}=5.8$ mA, $V_{DC}=1.5$ V)
Insertion gain (ave)	-2.1 ~ -0.2 dB (max @11 GHz, min @6 GHz)
Phase error (rms)	2.7 ~ 10° (max @18 GHz, min @7 GHz)
Gain error (rms)	0.5 ~ 1.7 dB (max @18 GHz, min @7 GHz)
Input $P_{1dB}$	-5.4 (+/- 1.3) dBm @ 12 GHz
Input return loss	< -10 dB @ 8.5-17.2 GHz
Output return loss	< -10 dB @ 6.3-16.5 GHz
Chip area	0.33 x 0.43 mm <sup>2</sup> (core), 0.75 x 0.6 mm <sup>2</sup> (including pads)

**Table 3.3:** Performance Summary of the K-band 4-bit CMOS Active Phase Shifter

Quantity	Results
Technology	0.13- $\mu$ m CMOS (1P8M)
Phase resolution	4-bit
Frequency band	15-26 GHz
Power consumption	11.7 mW ( $I_{DC}=7.8$ mA, $V_{DC}=1.5$ V)
Insertion gain (ave)	-4.6 ~ -3 dB (max @24.6 GHz, min @15 GHz)
Phase error (rms)	6.5 ~ 13° (max @25.6 GHz, min @15 GHz)
Gain error (rms)	1.1 ~ 2.1 dB (max @25.6 GHz, min @15 GHz)
Input $P_{1dB}$	-0.8 (+/- 1.1) dBm @ 24 GHz
Input return loss	< -10 dB @ 16.8-26 GHz
Output return loss	< -10 dB @ 17-26 GHz
Chip area	0.33 x 0.43 mm <sup>2</sup> (core), 0.75 x 0.6 mm <sup>2</sup> (including pads)

characteristics with 4-bit digital input codes of the K-band phase shifter. The RMS phase error is 6.5-13° at 15-26 GHz [Figure 3.10(b)(②)]. The average insertion loss varies from -4.6 dB at 15 GHz to -3 dB at around 24.5-26 GHz, and the peak-to-peak gain variations are minimum 3.3 dB at 15.4 GHz and maximum 6.3 dB at 25.6 GHz [Figure 3.10(b)(③)]. The RMS gain error is less than about 2.1 dB from 15 GHz to 26 GHz [Figure 3.10(b)(④)]. As shown in the RMS error characteristics in Figure 3.10(a) and 3.10(b), the RMS phase errors versus frequency have strong correlations with the RMS gain error patterns versus frequency. This is a typical characteristic of the proposed phase shifter, because the output phase in the phase shifter is set by the gain factors of I- and Q- input of the adder, any gain error indicates the scale of the phase error. The measured

input  $P_{1dB}$  is  $-0.8 \pm 1.1$  dBm for all phase states at 24 GHz. The total current consumption is 7.8 mA from a 1.5 V supply voltage.

Finally, the  $0^\circ$ -bit response is subtracted from all the measured 4-bit phase responses and the results show nearly constant 4-bit phase shift versus frequency for each phase shifter (Figure 3.11). Grey dashed-lines are ideal 4-bit phases. It is seen that the phase imbalance of the external  $180^\circ$ -hybrid coupler causes significant phase error at  $\sim 14$ -16 GHz (for K- and Ku-band phase shifter) and at  $\sim 21$ -24 GHz, respectively, which will be improved with an accurate integrated balun and be shown in the next section. The active phase shifters also show 4-bit phase resolution at the measurement band edges, which implies that albeit the phase accuracy is dependent on the accuracy of the I/Q network, the phase shifter guarantees the output phase monotonicity versus input digital control sequences, one of the fundamental merits the active phase shifters over passive designs. All the measured results are summarized in Table 3.2 and Table 3.3.



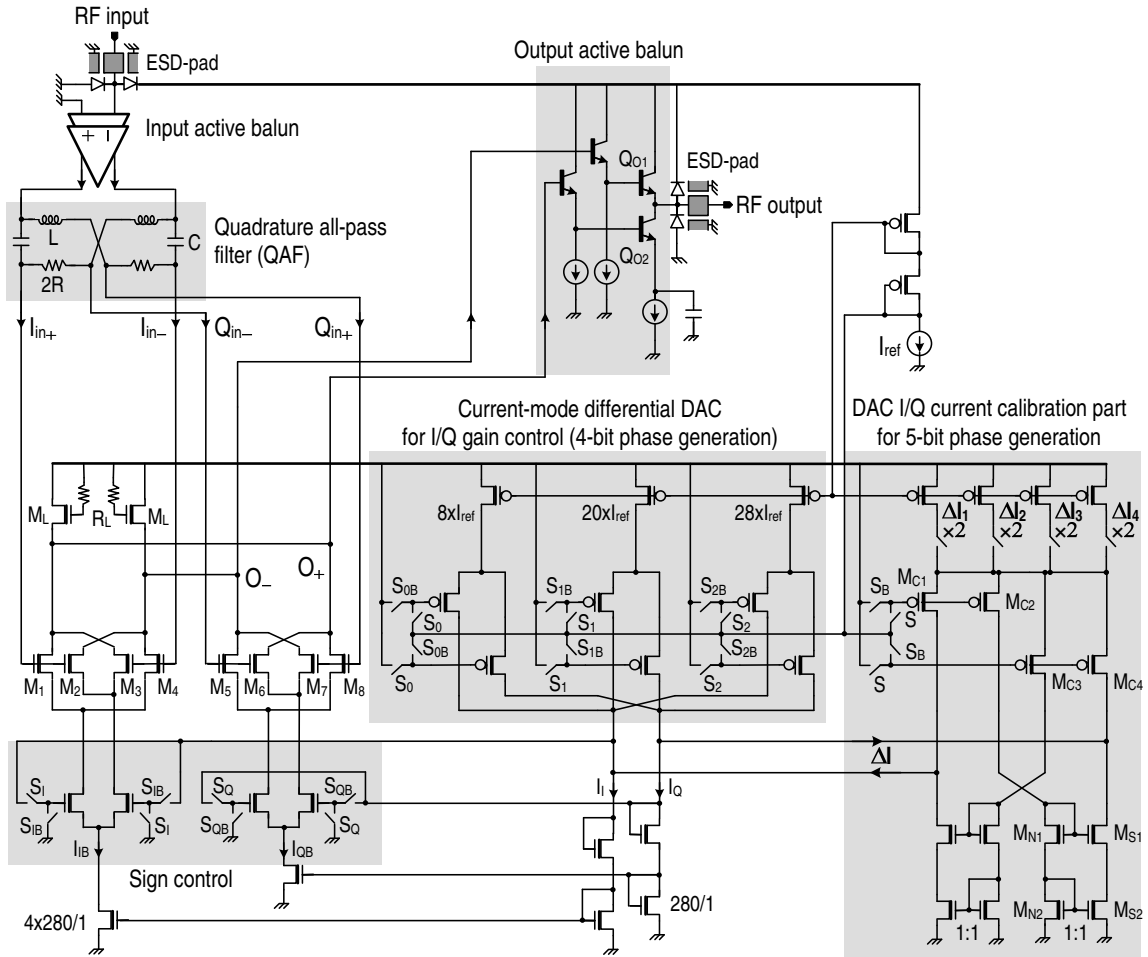
### 3.5 Design II: 5-Bit Active Phase Shifters in 0.18- $\mu\text{m}$ CMOS Technology

This section focuses on the optimization of the QAF and DAC current control scheme by including a calibration path (called “CAL” in Figure 3.2) so that the active phase shifter proposed in the previous section can generate 5-bit phase states at 6–18 GHz for high resolution phased-arrays. This optimization also enables to calibrate phase error caused by chip implementation errors such as process variations, resulting in more stable operation. The phase shifter shown in Figure 3.12 includes active baluns (rather than passive balun) designed in a SiGe HBT technology at the input and output stages so that they can provide a wideband (6-18 GHz) single-to-differential and differential-to-single signal conversions at the expense of power consumption and linearity degradation at those active baluns. The input 2-stage active balun is realized using differential amplifiers by grounding one of the differential inputs, and provides 33.5 dB voltage gain, 3.5-4 dB NF and -30 dBm IIP<sub>3</sub> with  $\sim$ 13 mA of DC current consumption at 10-14 GHz, which will be detailed in the next chapter. The differential phase and magnitude errors are negligible at 6-18 GHz. The core phase shifter circuits shown in Figure 3.12 are designed using 0.18- $\mu\text{m}$  CMOS built in the Jazz SiGe120 technology, and the design details are followings.

#### 3.5.1 Circuit Design

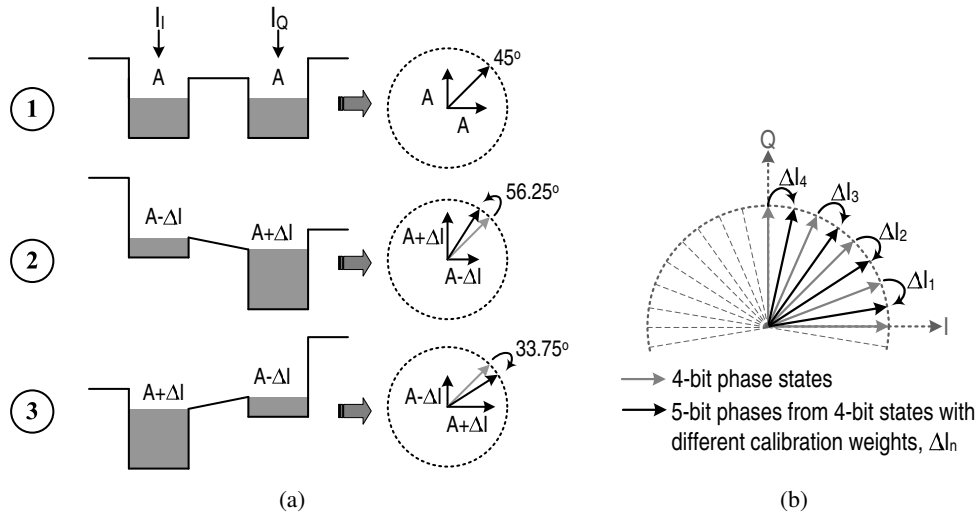
**Quadrature All-pass Filter:** Compared with the previous designs, the characteristic impedance of QAF [ $=\sqrt{L/C}$ ] is scaled down to  $\sim$ 24.4  $\Omega$  with a resonance at 12 GHz to increase the quadrature accuracy under a finite capacitive loading: L=324.2 pH and C=542.8 fF.  $\sqrt{L/C}$ =24.4  $\Omega$ . The nominal value of 2R is 50  $\Omega$ . These result in Q=0.97, and generates two pole frequencies, given as  $\omega_{p1,2}=1/Q \times (1 \pm \sqrt{1-Q^2}) \times \omega_o$  in Chapter 2, of 9.6 GHz and 14.8 GHz, where the QAF shows exact 90° phase difference between the outputs. The estimated loading capacitance is  $C_L=50\sim 80$  fF but since  $C_L/C$  is very small (roughly  $< 0.13$ ) the I/Q errors caused by the  $C_L$  are negligible. SPECTRE simulations show that the I/Q phase error is  $\Delta\theta < 3^\circ$  at 7-15.5 GHz with an I/Q amplitude error of  $\Delta A < 1.5$  dB. For 6-18 GHz,  $\Delta\theta < 9^\circ$  and  $\Delta A < 1.8$  dB, both peak error values.

**Analog Differential Adder (I/Q VGAs):** To maximize linearity, while minimizing the loading effect on the QAF, a small sizing (W/L=20/0.18) with a large gate-overdriving of  $V_{gs}-V_{th}\simeq 0.5$  V is chosen for the input transistors ( $M_{1-8}$ ) of the adder. This results in a maximum



**Figure 3.12:** The schematic of 5-bit active phase shifter. The phase shifter cores composed of QAF, I/Q VGAs, DAC and calibration part are designed using 0.18- $\mu\text{m}$  CMOS technology.

of  $\pm 250$  mV of differential input swing for less than  $\pm 50\%$  variation of drain bias current from its quiescent point. The simulated input  $P_{1dB}$  and  $IIP_3$  in the adder are 2.4 dBm and 15.5 dBm, respectively, for 200  $\Omega$  of load impedance at 12 GHz with with  $0^\circ$ -bit phase setting and a bias current of 2.5 mA. The gain is  $A_v = -2 \pm 0.5$  dB with an active load consist of  $M_L$  ( $W/L=20/0.18$ ) and  $R_L$  (600  $\Omega$ ) which gives about  $95 + j28.5$   $\Omega$  impedance at 12 GHz. The NF of the active phase shifter is dependent on the input transistor size and bias current. With input transistor size of  $W/L=20/0.18$ , NF is  $\sim 15$  dB at 12 GHz from the matched source impedance of 25  $\Omega$  for a bias current of 2.5 mA. However, if the input transistor size in the adder is increased from 20/0.18 to 80/0.18, the NF becomes 9.4 dB for a bias current of 10 mA. The NF variations over 6-18 GHz



**Figure 3.13:** I/Q DAC current calibration for 5-bit phases: (a) phase splitting from  $45^\circ$  (①) to  $56.25^\circ$  (②) or  $33.75^\circ$  (③) by readjusting current  $\Delta$ , (b) 5-bit phase generation from 4-bit phase states.

is  $\leq 0.6$  dB from the NF at 12 GHz in the phase shifter. For good current matching,  $L=1 \mu\text{m}$  of gate length is chosen for the tail NMOS and the cascode mirror faithfully transfers the control DC currents ( $I_I$  and  $I_Q$ ) from DAC to the I- and Q-path VGAs ( $I_{IB}$  and  $I_{QB}$ ).

**5-Bit Phase Control:** The switch control scheme for 4-bit phase generation is set such that  $I_I+I_Q=\text{constant}$  for all phase states for a constant amplitude response at the output. For 5-bit phase generation from the 4-bit phase states, this design includes additional I/Q current calibration path in the DAC. The current calibration is done as follows: When  $M_{C1,2}$  are selected (and  $M_{C3,4}$  are deselected) by switching  $S=\text{on}$  and  $S_B=\text{off}$ , a small calibration current of  $\Delta I$  is added to  $I_I$ , and the  $M_{N1,2}$  senses the same amount of  $\Delta I$  and mirror it to the current sink of  $M_{S1,2}$  which subtracts the  $\Delta I$  from  $I_Q$ . This results in  $\theta_{out,cal}=\tan^{-1}[\sqrt{\{(I_Q-\Delta I)/(I_I+\Delta I)\}}]$  decreasing the output phase from the original value of  $\theta_{out}$ . The switch  $S$  in Figure 3.12 decides the direction of the calibration current  $\Delta I$ , i.e., when  $S=\text{off}$  and  $S_B=\text{on}$  the direction of  $\Delta I$  is reversed, increasing the output phase. Still the total control current of  $I_I+I_Q$  is *constant* and therefore the output amplitude does not change after calibration. Figure 3.13(a) illustrates the generation of  $56.25^\circ$  ( $5 \times 11.25^\circ$ ) or  $33.75^\circ$  ( $3 \times 11.25^\circ$ ) phase state from  $45^\circ$  phase bit, i.e., by switching  $S_0=S_1=S_2B=\text{on}$  ( $S_{0B}=S_{1B}=S_2=\text{off}$ ),  $I_I=I_Q=28 \times I_{ref}$  resulting in  $45^\circ$  phase state (①) in Figure 3.13(a),  $A=28 \times I_{ref}$ ). By setting  $\Delta I=10.7 \times I_{ref}$  and transferring it from I-path to Q-path (② in Figure 3.13(a)) or vice-versa (③ in Figure 3.13(a)), the output phase will increase to

56.25° or decrease to 33.75°.

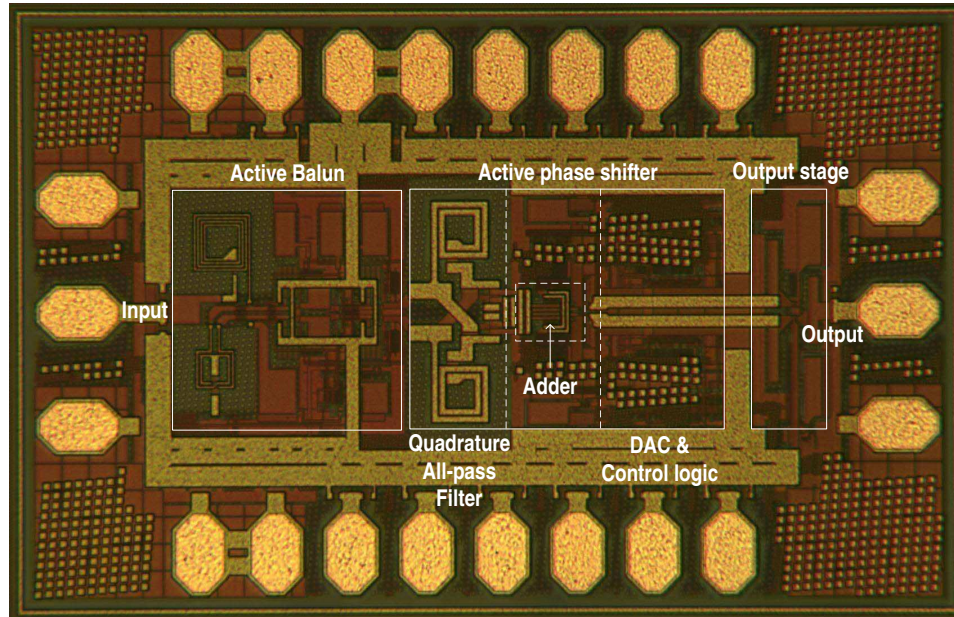
Figure 3.13(b) shows a way to generate 5-bit phase states by staggering 11.25° from 4-bit phases in the first quadrant phase space. The phases in the first quadrant space form fundamental phase states and four different calibration weights of  $\Delta I$  are necessary to generate another four phases from the original 4-bit states. Therefore, the sizes of the four current sources in the calibration path are set as  $\Delta I_1=6 \times I_{ref}$ ,  $\Delta I_2=11 \times I_{ref}$ ,  $\Delta I_3=10 \times I_{ref}$  and  $\Delta I_4=3 \times I_{ref}$  ( $I_{ref}=11 \mu\text{A}$ ). The phases in the other quadrant spaces can be generated by polarity manipulation through switching the tail current in the DAC and/or VGAs. The mismatches in the DAC current sources can be minimized with long channel CMOS with large size. In this design, the current source PMOSs therefore are designed with a gate length of  $L=1 \mu\text{m}$ . The calibration path can also be used to compensate for phase error which originates from quadrature mismatches (amplitude error and phase error) in the I/Q network.

The final differential-to-single-ended conversion stage is a Class-A push-pull amplifier which is a modification of the conventional totem-pole output stage [52]. It is composed of an emitter-follower providing wideband output matching and a common emitter stage having a unity gain, and effectively combines the differential inputs in an in-phase fashion at 6-18 GHz. The simulated  $S_{22}$  is  $< -12$  dB at 6-18 GHz. The RF input and output pads are protected using dual-diode ESD cells (HBM rating: 3 kV, 2 A).

### 3.5.2 Measured Results and Discussions

The active phase shifters are realized in Jazz 0.18- $\mu\text{m}$  CMOS technology (1P6M) built in SiGe120 BiCMOS technology (SiGe HBT  $f_t \simeq 150$  GHz). The overall chip size including all pads is  $1.2 \times 0.75 \text{ mm}^2$  and the phase shifter core including QAF, I/Q VGAs and digital control part takes only a very small area of  $0.45 \times 0.35 \text{ mm}^2$  (Figure 3.14). The IC is measured on-chip after standard short-open-load-through (SOLT) calibration with a vector network analyzer (Agilent, E8364B). The overall current consumption is 18.7 mA (active balun: 13 mA, phase shifter: 3 mA, emitter-follower buffer and output balun stage: 2.7 mA) from a 3.3 V supply voltage.

Figure 3.15 presents the measured input and output matching characteristics. For all 5-bit phase states,  $S_{11}$  is  $< -10$  dB from 11.2 GHz to 15.2 GHz, and  $S_{22}$  is  $< -12$  dB at 6–18 GHz. It is seen that a phase change in the phase shifter causes a slight disturbance in  $S_{22}$ . This is

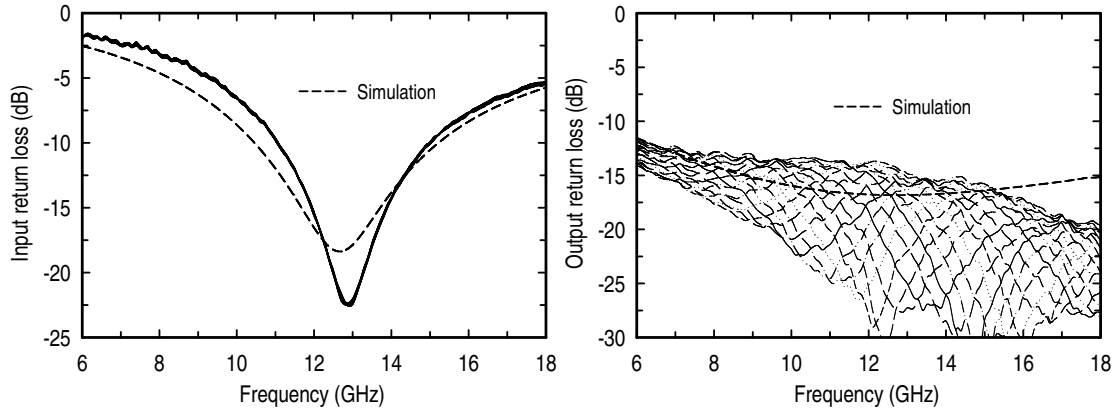


**Figure 3.14:** Chip photograph of the 5-bit active phase shifter including input and output active baluns (phase shifter area= $0.45 \times 0.35 \text{ mm}^2$ , overall area= $1.2 \times 0.75 \text{ mm}^2$  including baluns and pads).

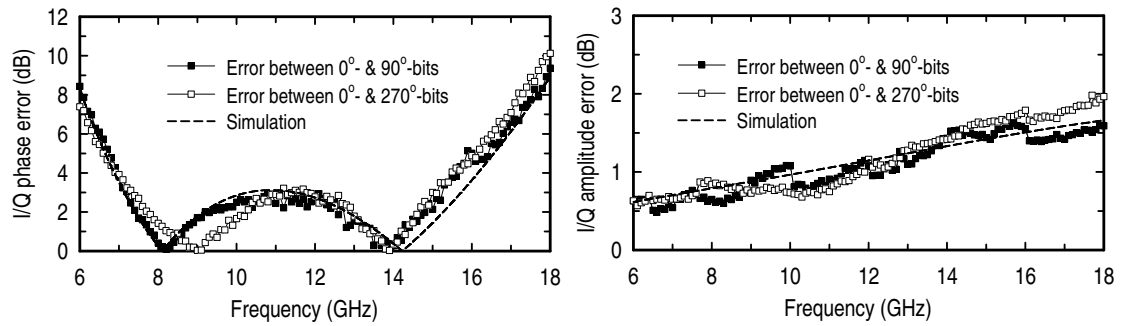
because the output impedance of the emitter follower,  $Q_{O1}$  in Figure 3.12, is slightly modulated by the load current change in the adder. The measured reverse isolation ( $S_{12}$ ) is below -38 dB at 6-18 GHz.

The I/Q errors of the QAF are measured by comparing the phases of the measured S-parameters of  $0^\circ$ -,  $90^\circ$ -,  $180^\circ$ - and  $270^\circ$ -bits. The measured I/Q amplitude mismatch is  $< 2$  dB at 6–18 GHz, and the quadrature phase error is  $< 3^\circ$  from 7.2 GHz to 15.2 GHz and is  $< 10^\circ$  at 6–18 GHz (Figure 3.16). The SPECTRE simulation includes 70 fF of loading capacitance, and compared with the results in Figure 3.9, the quadrature accuracy is substantially improved with the low impedance design of the QAF.

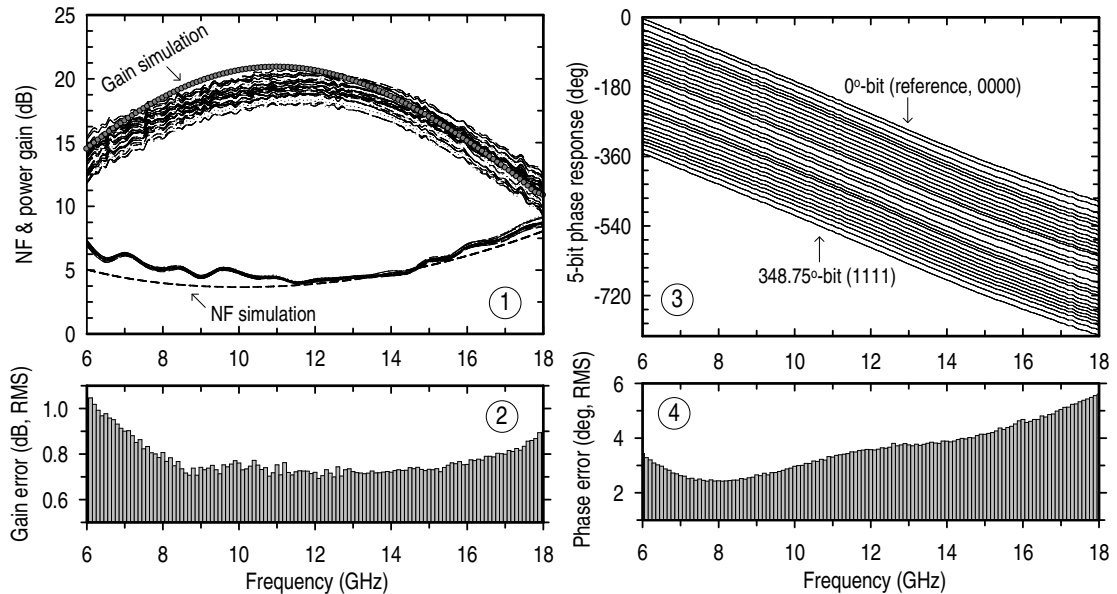
The measured average power gain ( $S_{21}$ ) is 16.5–19.5 dB at 7.5–15.2 GHz (peak average gain=19.5 dB @12 GHz), which is dominated by the active balun (Figure 3.17①). NF is measured using Y-factor method with a spectrum analyzer (Agilent, E4448) and a noise source (Agilent, 346C ENR=15.61 dB @12 GHz). The average NF ranges from 4 dB at 11.5 GHz to 8.8 dB at 18 GHz, and is nearly independent of the phase states (Figure 3.17①). The peak-to-peak gain variation is  $\leq \pm 1.5$  dB, and the RMS gain variation is  $< 1.1$  dB from the average value at 6–18 GHz for all 5-bit phase states (Figure 3.17②). The main sources of the gain error



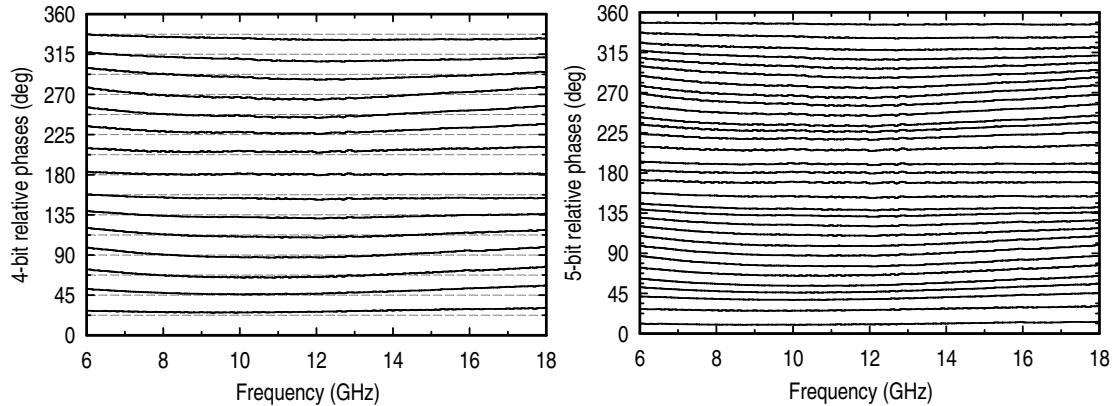
**Figure 3.15:** Measured input and output matching characteristics (4-bit states are shown for clarity purpose).



**Figure 3.16:** Measured I/Q phase error and amplitude error.



**Figure 3.17:** Measured performances of the 5-bit active phase shifters. ①: power gain and NF, ②: RMS gain error, ③: 5-bit phase response and ④: RMS phase error.



**Figure 3.18:** Measured relative phases, referred to  $0^\circ$ -bit, of the 5-bit active phase shifter: 4-bit relative phases without DAC current calibration (*left*), and 5-bit relative phases with DAC current calibration (*right*). Grey dashed-lines are ideal 4-bit phases.

for different phase states are the I/Q amplitude error in the QAF and the DAC current source mismatch together with the input transistor mismatch in the I/Q VGAs.

Figure Figure 3.17③ shows the measured 5-bit phase responses from 6 GHz to 18 GHz, and the phase shifter shows less than  $3^\circ$  of RMS error from 6.4 GHz to 10.2 GHz, and at 6–18 GHz the RMS error is  $< 5.6^\circ$  achieving better than 5-bit accuracy over 6-18 GHz (Figure 3.17④). The 4-bit relative phases without DAC calibration [Figure 3.18 (*left*)] show much better accuracy compared with the results in Figure 3.11, due to the precise input balun and QAF operations. Figure 3.18 (*right*) shows relative 5-bit phase states with the DAC current calibration, and highlights the merit of the active phase shifter: i.e., the phase shifter can achieve nearly ideal constant phase shift over very wideband and the phase resolution can be extended by a simple DC current readjustment without consuming additional chip area. The measured performance of the 5-bit phase shifter is summarized in Table 3.4.

### 3.6 Conclusion

In this section, 4-bit and 5-bit active phase shifters are developed using  $0.13\text{-}\mu\text{m}$  CMOS and  $0.18\text{-}\mu\text{m}$  CMOS technology, respectively, for integrated phased-array applications. The fundamental operation of the active phase shifters is to interpolate the phases of the quadrature input signals by adding two I/Q inputs with appropriate I/Q gains. The resonance-based quadrature all-pass filters minimize loss and increase the operation bandwidth with excellent

**Table 3.4:** Performance Summary of the 5-bit Active Phase Shifter

Quantity	Results
Technology	0.18- $\mu$ m CMOS (1P6M)
Phase resolution	5-bit
Frequency band	6-18 GHz
Power consumption	61.7 mW ( $I_{DC}=18.7$ mA, $V_{DC}=3.3$ V) (*9.9 mW ( $I_{DC}=3$ mA, $V_{DC}=3.3$ V))
Insertion gain (ave)	16.5-19.5 dB @ 7.5-15.2 GHz (*-3 ~ 0 dB @ 7.5-15.2 GHz)
Phase error (rms)	< 5.6° @ 6-18 GHz
Gain error (rms)	< 1.1 dB @ 6-18 GHz
NF	4 ~ 5.7 dB @ 7.5-15.2 GHz (*14.5 ~ 16.5 dB @ 7.5-15.2 GHz)
Input return loss**	$\leq$ -10 dB @ 11.2-15.2 GHz
Output return loss	$\leq$ -12 dB @ 6-18 GHz
Chip area	0.45 $\times$ 0.35 mm <sup>2</sup> (core), 1.2 $\times$ 0.75 mm <sup>2</sup> (overall)

\*Estimation for the active phase shifter only, excluding input and output active baluns.

\*\* Input return loss is limited by the input active balun.

signal precision in the phase shifters. The measured phase shifter performances are very wide-band and well matched with theory and simulations from SPECTRE. In the proposed phase shifter architecture, the output phase resolution can be extended using a higher resolution DAC, and the DAC current calibration path can be used to correct any phase error caused by QAF errors or manufacturing errors such as process variations. All of these functions can be implemented with very small size, because the area consuming elements are only two inductors. As the phase accuracy are dominated by the transistor matching in the DAC and current silicon-based integrated circuit technology can provide an excellent transistor matching, the proposed phase shifters are excellent candidates for high resolution and low-cost integrated phased-array systems. The following chapter focuses on the phased-array designs using the 0.18- $\mu$ m CMOS active phase shifter developed in this chapter.

### 3.7 Acknowledgements

This chapter is, in part, a reprint of:



- K.-J. Koh and G. M. Rebeiz, "0.13- $\mu\text{m}$  CMOS Phase shifters for X-, Ku- and K-Band Phased Arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.
- K.-J. Koh and G. M. Rebeiz, "6-18 GHz 5-Bit Active Phase Shifter," *IEEE Trans. Microwave Theory Tech.*, (in review).
- K.-J. Koh and G. M. Rebeiz, "A 0.13- $\mu\text{m}$  CMOS Digital Phase Shifter for K-band Phased Arrays," *IEEE RFIC Symp. Dig.*, pp. 383-386, June 2007.

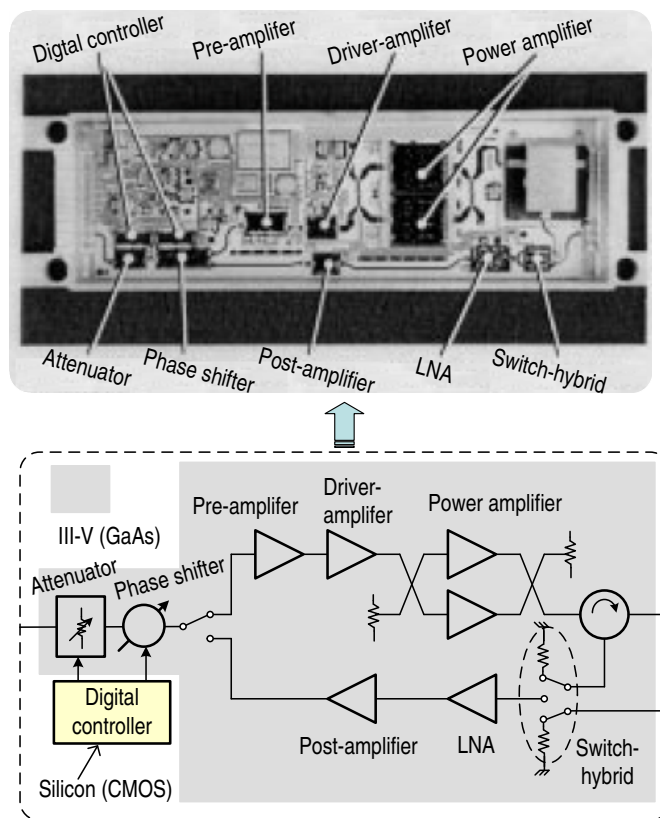
I would like to thank my coauthor Prof. Gabriel M. Rebeiz.

# 4

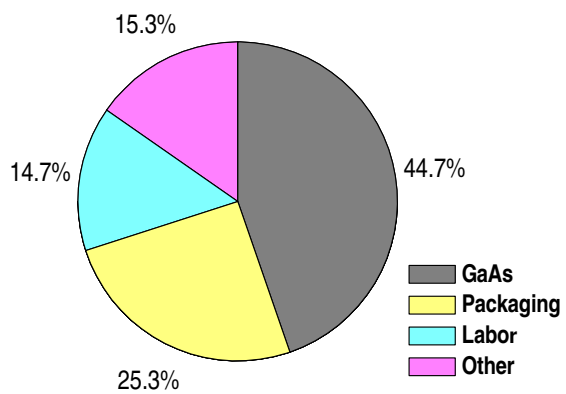
## **RF/Microwave Phased-Array Design: X-/Ku-Band 8-Element Phased-Array Receiver in 0.18- $\mu\text{m}$ SiGe BiCMOS Technology**

### **4.1 Introduction**

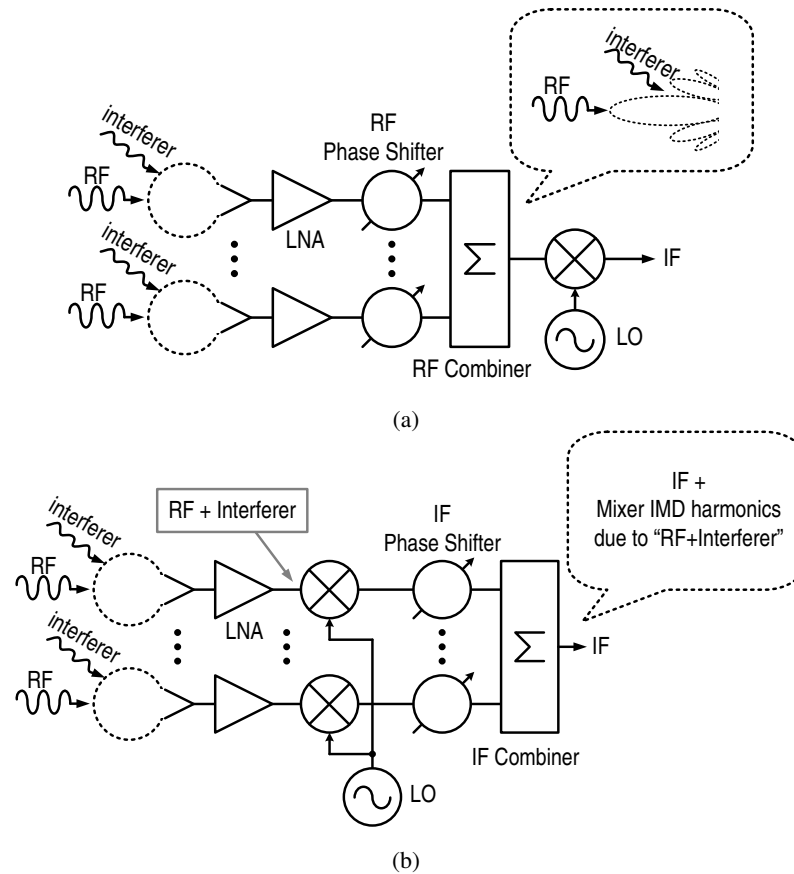
While phased-arrays have been widely used in defense and science applications, their commercial applications have been very limited due to their high cost and large size. The high cost and volume are mainly due to the discrete implementations of the phased arrays based on transmit/receive (T/R) modules. Typical T/R module implementation is shown in Figure 4.1 where III-V front-end MMICs (GaAs) were assembled together with silicon-based digital control chipsets [1, 53]. Within these T/R modules, the III-V MMICs and assembly/packaging are the most significant cost elements, taking about 70 % of overall cost as is shown in Figure 4.2 [2]. Therefore, the integration of high capability RF blocks with baseband and digital processors on a silicon chip will drastically reduce the cost and size of phased arrays, which is the main object of this chapter. A SiGe BiCMOS process can be an excellent candidate for this purpose, and can provide high-performance SiGe HBT for RF and analog processes and dense CMOS for digital circuit designs [18, 19].



**Figure 4.1:** Typical Transmit/receive module and its RF block diagram [1].



**Figure 4.2:** Typical X-band T/R module cost elements [2].



**Figure 4.3:** Analog beam-forming systems: (a) phased-array based on RF phase shifters, (b) phased-array based on LO phase shifting in the mixer.

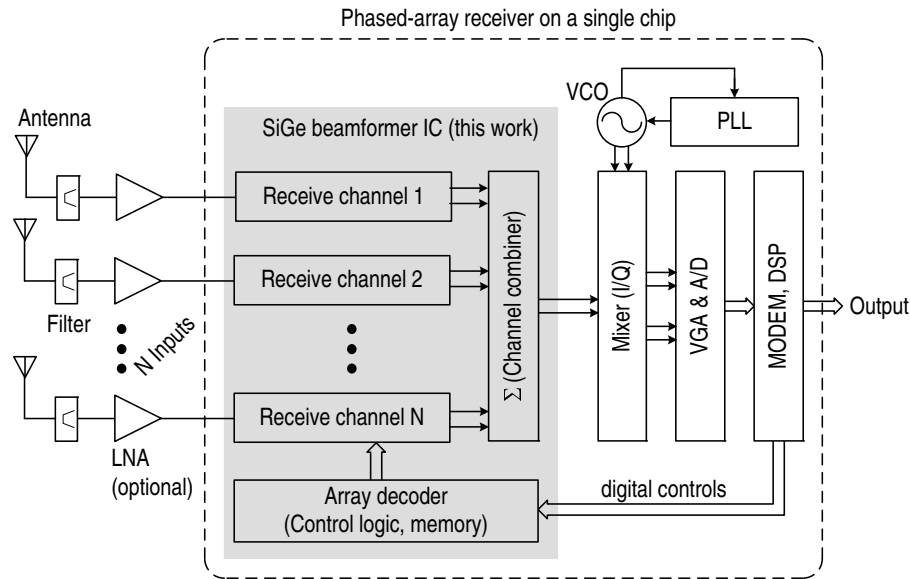
In the architectural view of phased-arrays, phase shifting in the RF domain for each array element has been dominant ever since they were developed [54]. Recently phased-array based on IF phase shifting architecture was realized at 94 GHz in [55] and LO phase shifting phased-array which had been proposed in concept in 1986 [56] was realized in [57]. The fundamental merit of the RF phase shifting architecture over the LO or IF phase shifting ones, as shown in Figure 4.3(a), is that the output signal after the RF combiner has a high pattern directivity and can substantially reject an interferer before the following receiver units, maximizing the value of the phased arrays as a spatial filter. On the other hand, in LO or IF phase shifting methods (figure 4.3(b)), a mixer is connected to a low directivity antenna and is subjected to interference from all directions, thus generating intermodulation products which can propagate throughout the array. Another advantage of the RF phase shifting architecture is the elimination of an LO distribution network and this results in a much simpler system architecture and layout

especially for large arrays with 64-1000 elements. Also, in satellite or defense-based applications, the required LO phase noise is very low, for example,  $<-155$  dBc/Hz at 10 kHz offset for X-band radar systems and  $<-123$  dBc/Hz at 1 MHz offset for 11-13 GHz direct broadcast satellite systems over a temperature variation of  $-50^{\circ}\text{C}\sim 100^{\circ}\text{C}$ . This can only be achieved using an external oscillator such as a dielectric resonator oscillator and removes the advantage of integrated silicon-based oscillators. It is for these reasons that current phased-array systems are still developed with RF phase shifters in the main industries [58, 59].

A major issue in RF phase shifting architecture is the design of the RF phase shifter. Traditional phase shifters based on passive networks occupy a large space on wafer. Therefore, for the integrated phased arrays especially for X- and Ku-band applications, where a small form factor is required, the active phase shifter design proposed in the previous chapter is more appropriate. In this work, an RF phase shifting beamformer (called the *All-RF* architecture) integrated with all the digital control circuitry is designed in a standard  $0.18\text{-}\mu\text{m}$  SiGe BiCMOS technology. The application areas are in miniature phased-arrays for mobile satellite systems, and for defense systems such as radars and large bandwidth telecommunication links covering the X- and Ku-band frequency range [60]. The operational bandwidth of these systems is between 50 MHz (medium data rate systems) to 3 GHz (high data rate systems and low probability of intercept radars).

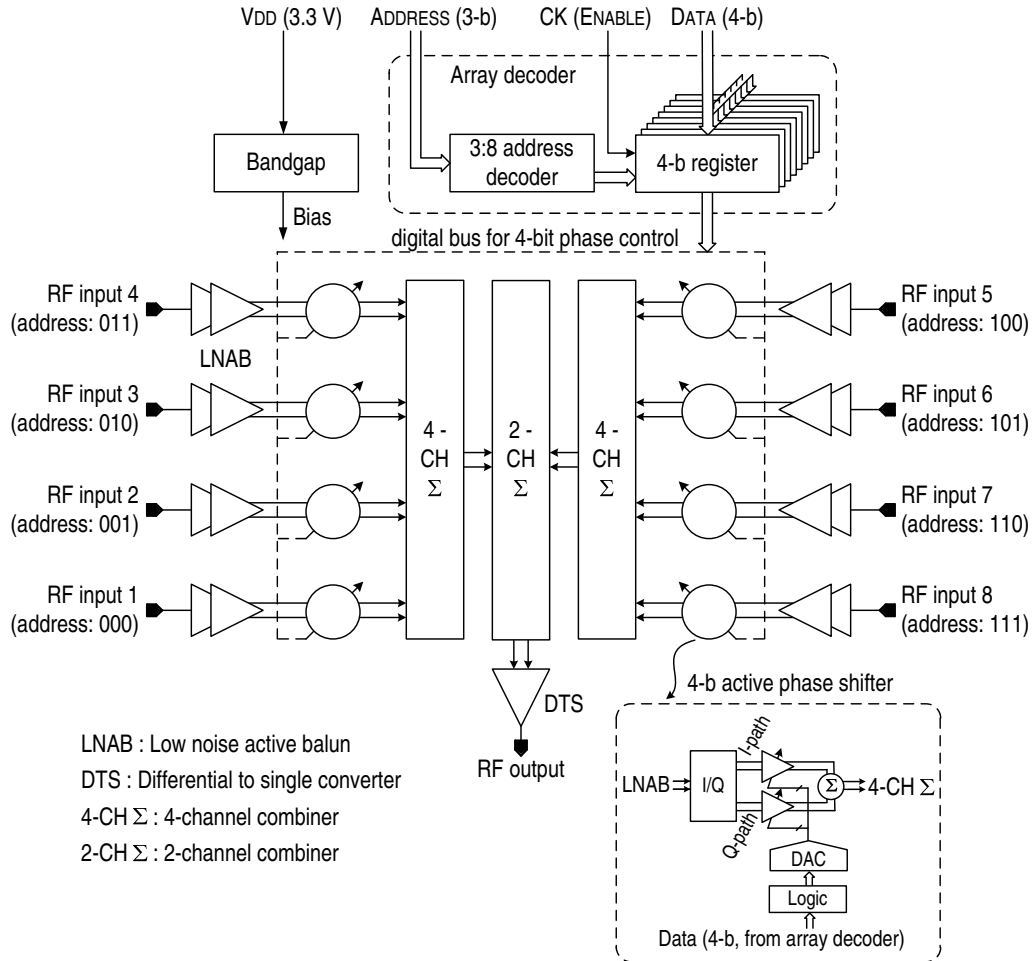
## 4.2 On-Chip Phased Array Architecture

Figure 4.4 presents a phased-array receiver with all the front-end elements, baseband and back-end digital processors on a single SiGe BiCMOS chip. The RF signals from the different antenna elements (followed by external filters) form the inputs to the RF phased array network. This work focuses on the beamforming network, the essential part of the phased-array receiver, composed of eight array elements, channel combiners and an array digital decoder controller. After the RF channel combiner, the signal can be handled using standard wireless communication system building blocks. Integration of single-end LNAs between the antennas and the silicon chip is optional depending on the minimum required sensitivity of the system. Figure 4.5 shows the specific functional blocks of the beamforming receiver. Every array element is composed of a low-noise active balun (LNAB) for differential RF signal processing and the differential 4-bit active phase shifter realized using I/Q signal interpolation, proposed in the



**Figure 4.4:** A phased-array receiver system completely integrated on a single silicon chip.

previous chapter. Each phase shifter can be controlled independently using digital inputs from an array decoder which is composed of a 3-to-8 address decoder and 4-bit register cells (8x) for memory. A 4-bit digital data sequence, which sets the phase to each phase shifter, is loaded to a phase shifter by an enabling clock signal and an address decoder output corresponding to the address of each element. The coherent combining of the RF signals from the eight antenna channels is done in two steps. First, the addition of four individual signals is done in the 4-channel combiners (4-CH  $\Sigma$ ), and then 2-channel combiner (2-CH  $\Sigma$ ) adds the outputs of the 4-channel combiners together, emulating the conventional corporate-feeds but in an active approach [7]. The corporate-feed approach ensures equal electrical distance between any of the input ports to the output port, and results in easy phase calibration at the sub-array level. Finally a differential-to-single converter (DTS) transforms the balanced signal into a single-ended one, and provides a wideband  $50 \Omega$  matching impedance for the measurement instrumentation. All the bias currents are referred to an internal bandgap reference. In the *All-RF* phased-array architecture, while the phase shifter and channel combiners constitute essential parts and should show good linearity, the balun blocks (LNAB and DTS) are dispensable in fully differential phased-array systems. However, in this work, these balun blocks are included for single-ended RF measurements and are based on active circuits for wideband balun operations, at the expense of power consumption and linearity degradation at the active baluns. In case that the system linearity is a major



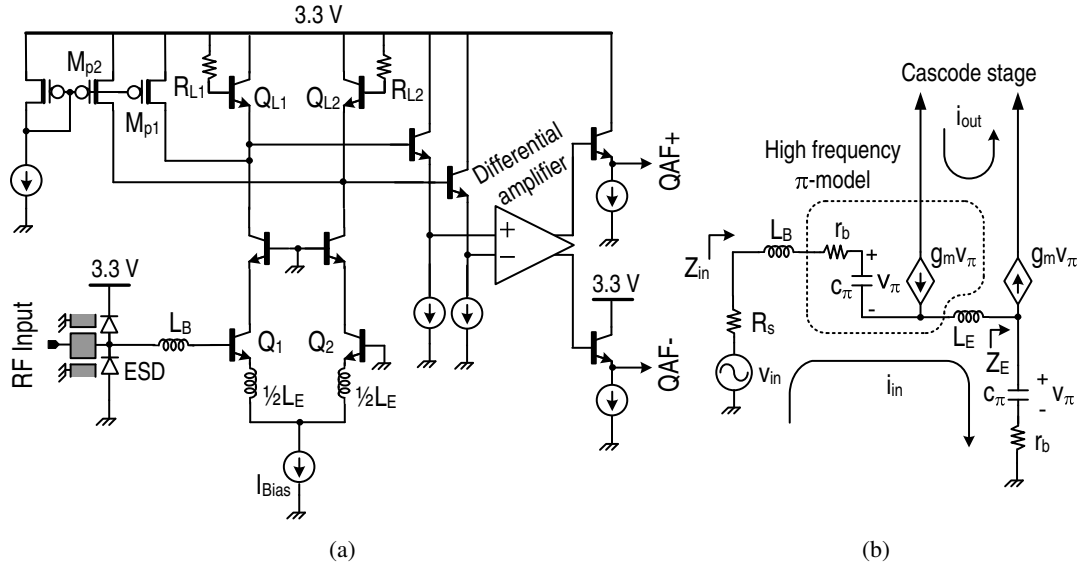
**Figure 4.5:** Functional block of the beamforming network.

concern, the LNAB can be replaced by an integrated passive balun or can be removed entirely if the phased-array chip is preceded by a differential LNA. The DTS can also be removed if a differential mixer/receiver is placed after the array.

## 4.3 Building Block Designs

### 4.3.1 Low-Noise Active Balun (LNAB)

The essential functions of the two-stage active balun shown in Figure 4.6 are low-noise signal amplification, input impedance ( $50 \Omega$ ) matching and wideband single-to-differential conversion for providing a differential signal to the quadrature all-pass filter in the active phase shifter. The emitter-coupled first stage amplifier provides these functions and the second stage differential amplifier contributes additional common-mode rejection. The output emitter-



**Figure 4.6:** (a) Low-noise active balun (LNAB). The second stage is AC-coupled with the first stage. (b) Input transconductor of the LNAB in small-signal models.

follower drives the following I/Q network. To save area, while still obtaining tuned gain characteristics, active inductor loads composed of  $Q_{L1-4}$  and  $R_{L1-4}$  are used. With the same biasing of  $Q_{L1,2}$  as that of the input transistors,  $Q_{1,2}$ , the noise contributions from the internal shot noise sources of  $Q_{L1,2}$  can be significant. The PMOS current sources,  $M_{P1,2}$ , steer most of the bias current provided by the tail current source from  $Q_{L1,2}$  and thus minimize the noise contribution from  $Q_{L1,2}$ . Typically with the same current biasing, the drain current noise in PMOS ( $\langle i_{n,PMOS} \rangle^2 = 4kT\gamma g_{m,PMOS}$ ) is much less than the collector shot noise current in BJT ( $\langle i_{n,BJT} \rangle^2 = 2qI_{C,BJT}$ ) under the operating condition of  $4V_T\gamma \ll V_{gs} - V_{th}$ , where  $g_{m,PMOS}$  is a transconductance in PMOS;  $I_{C,BJT}$  is a collector bias current;  $V_T (=kT/q)$  is the thermal voltage;  $\gamma$  is the drain current thermal noise coefficient in PMOS; and  $V_{gs} - V_{th}$  is the gate over-driving voltage in PMOS.

Figure 4.6(b) shows the input transconductor cell of the LNAB for impedance matching and gain considerations, where the source impedance  $R_s$  is  $50 \Omega$ .  $r_b$  is the base ohmic resistance in the small signal HBT  $\pi$ -model which is simplified for the frequency range of interest. Under the normal operating frequency ranges of  $\omega$  ( $\ll \omega_T \simeq g_m/C_\pi$ ), the impedance looking into the emitter terminal of  $Q_2$  ( $Z_E$  in Figure 4.6(b)) can be simplified as  $1/g_m$  ( $=V_T/I_C$ , where  $V_T = kT/q$  and  $I_C$  is the collector bias current), leading to an effective emitter-degeneration of  $Z_E = j\omega L_E + 1/g_m$  for the input transistor  $Q_1$ . Therefore, the overall input impedance ( $Z_{in}$ ) in-



cluding matching elements can be expressed as (4.1) at the frequency range of  $\omega_T/\beta_{DC} \ll \omega \ll \omega_T$  ( $\beta_{DC}=g_m r_\pi$  is the collector-base DC current gain). Intuitively, additional degeneration by the  $1/g_m$  from the emitter-coupled stage effectively reduces  $C_\pi$  of  $Q_1$  by half, compared with the typical common-emitter HBT LNAs with inductive degeneration [61, 62].

$$Z_{in} \approx j\omega(L_B + L_E) + \frac{2}{j\omega C_\pi} + \left( \omega_T L_E + \frac{1}{g_m} + r_b \right). \quad (4.1)$$

$L_B$  and  $L_E$  cancel  $C_\pi$  at  $\omega_o = \sqrt{2/(L_B + L_E)C_\pi}$ , and the real term in (4.1) can be used for 50  $\Omega$ -matching. The presence of the ESD diodes does not disturb the matching characteristic since its impedance ( $\sim j330 \Omega$  @ 12 GHz) can be absorbed with a small increment of  $L_B$  from the designed value. The overall loaded-Q of the input matching network at resonance is given in (4.2). The collector-base AC current gain ( $\beta_{AC}$ ) is defined as (4.3), and the overall transconductance ( $G_m$ ) under the matched condition is expressed as (4.4) which is basically the base side conductance reflected to the collector port by being multiplied with  $\beta_{AC}$ .

$$Q_{input} = \frac{\omega_o(L_B + L_E)}{2R_s} = \frac{1}{R_s \omega_o C_\pi}. \quad (4.2)$$

$$\beta_{AC} = \frac{i_{out}}{i_{in}} = \frac{\beta_{DC}}{1 + j\omega r_\pi C_\pi} \approx \frac{g_m r_\pi}{j\omega r_\pi C_\pi} = -j \frac{\omega_T}{\omega}. \quad (4.3)$$

$$\begin{aligned} G_m &= \frac{i_{out}}{V_{in}} = \frac{i_{out}}{2R_s \times i_{in}} = \frac{\beta_{AC}}{2R_s} = -j \left( \frac{\omega_T}{\omega} \right) \left( \frac{1}{2R_s} \right) \\ &= -j \left( g_m \times \frac{1}{2} Q_{input} \right) \quad @ \omega = \omega_o. \end{aligned} \quad (4.4)$$

The overall differential voltage gain in the first stage of the LNAB is given as (4.5), where  $R_{eq}$  and  $L_{eq}$  are the equivalent series resistance and inductance of the active inductor. In (4.5),  $C_{\pi,Q1}$  and  $C_{\pi,QL}$  are base-emitter capacitances of  $Q_1$  and  $Q_{L1}$ , respectively, and  $g_{m,QL} = I_{C,QL}/V_T$  where  $I_{C,QL}$  is the bias current of  $Q_{L1,2}$ .  $I_{C,Q1}$  is the bias current of the input transistors. For matching bandwidth,  $Q_{input}$  should be a relatively small value, and therefore the gain can be set by optimizing the bias current ratio of  $I_{C,Q1}/I_{C,QL}$  and sizing the active inductors.

$$\begin{aligned}
A_{v,1st-stage} &\approx \underbrace{-j \left( \frac{\omega_T}{\omega} \right) \left( \frac{1}{2R_s} \right)}_{G_m} \underbrace{\left( \frac{1}{g_{m,QL}} + j\omega \frac{R_{L1}C_{\pi,QL}}{g_{m,QL}} \right)}_{Z_L = R_{eq} + j\omega L_{eq}} \times 2 \\
&= \left( -jQ_{input} + \frac{R_{L1}}{R_s} \frac{C_{\pi,QL}}{C_{\pi,Q1}} \right) \times \frac{I_{C,Q1}}{I_{C,QL}} \quad @ \omega = \omega_o.
\end{aligned} \tag{4.5}$$

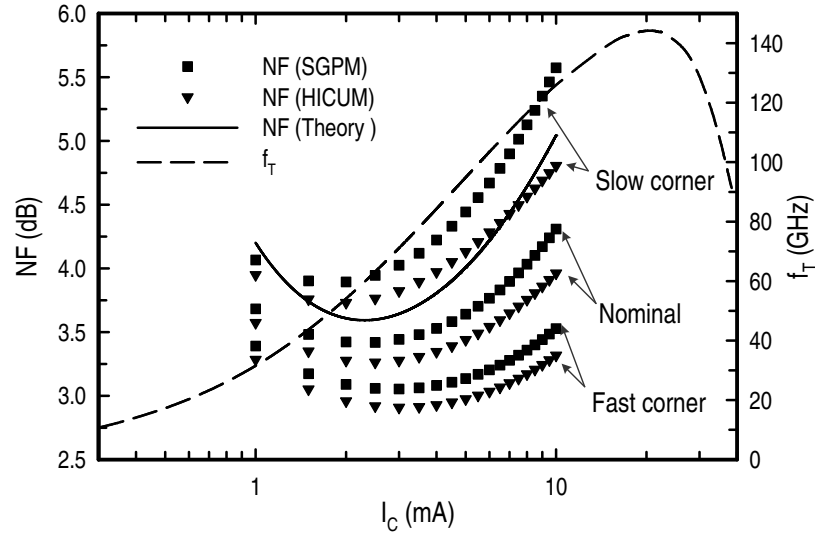
The  $NF_{min}$  of the SiGe HBT in the Jazz 0.18- $\mu\text{m}$  SiGe BiCMOS process is well described in [63] and given as (4.6), where  $r_e$  is emitter ohmic resistance and  $n$  is the collector current ideal factor.

$$NF_{min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2I_C}{V_T} (r_e + r_b) \left( \frac{1}{\beta_{DC}} + \left( \frac{\omega}{\omega_T} \right)^2 \right) + \frac{n^2}{\beta_{DC}}}. \tag{4.6}$$

Since  $r_b \gg r_e$ , it is important to minimize  $r_b$  for a lower  $NF_{min}$ , which can be possible by increasing the emitter length ( $l_e$ ) of  $Q_{1,2}$  ( $W_e=0.2 \mu\text{m}$ ) up to a point where the  $Q_{1,2}$  can still achieve a reasonable  $\omega_T$ . Therefore,  $l_e=20.32 \mu\text{m}$  ( $r_b \simeq 16 \Omega$ ) is chosen from SPECTRE simulations based on Spice Gummel-Poon Model (SPGM) and High-Current Model (HICUM) of the HBT [64]. Although the achievable  $NF_{min}$  at 12 GHz from (4.6) is around 1.3-1.5 dB with  $I_C=2-3 \text{ mA}$ , it is not possible to get this value under 50- $\Omega$  matching. The internal noise sources from the emitter-coupled stage of  $Q_2$  also contribute to the output noise significantly, leading to a higher NF than that of a standard differential HBT LNA with inductive degeneration. A rigorous NF analysis using the 1<sup>st</sup>-order small signal model shown in Figure 4.6 with identification of all the noise sources is presented in the Appendix B, and shows that the LNAB NF can be given as

$$\begin{aligned}
NF &= 1 + (1 + \delta_z^2) \frac{r_b}{R_S} + (1 + \eta_z^2) \frac{V_T}{2R_S I_C} + \left( \frac{\omega_T}{\omega_o} \right)^2 \frac{4V_T}{R_S \beta_{DC} I_C} \\
&\quad + \left( \frac{\omega_o}{\omega_T} \right)^2 (1 + \eta_z^2) \frac{I_C}{2R_S V_T} \left( R_S + r_b + \frac{V_T}{I_C} \right)^2.
\end{aligned} \tag{4.7}$$

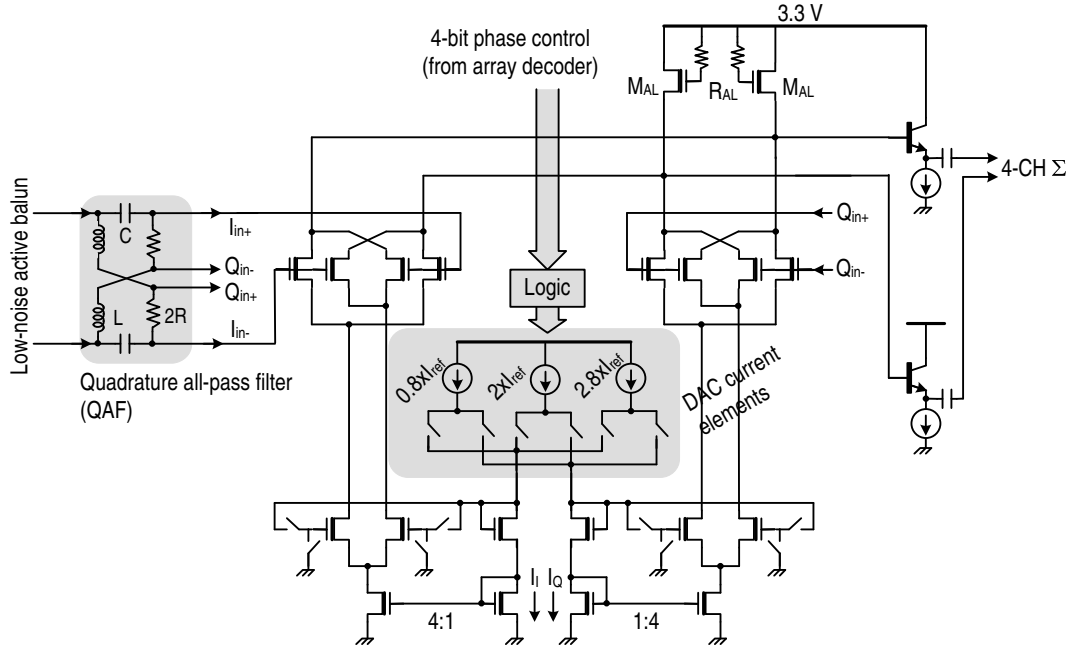
where  $\delta_z$  and  $\eta_z$  are constants addressing the NF contributions from the  $r_b$  and the collector shot noise of  $Q_2$ , respectively. Both of  $\delta_z$  and  $\eta_z$  are less than or equal to 1 depending on the



**Figure 4.7:** SPECTRE simulation results of  $NF$  and  $f_T$  versus  $I_C$  for the LNAB, together with theoretical estimation of  $NF$  from (4.7) at 12 GHz ( $A_E=0.2 \times 20.32 \mu\text{m}^2$ ).

operation frequency (See Appendix B). The noise contribution from the base shot noise current of  $Q_2$  is negligible because most of the base noise current will be directed to ground. Noise figure simulations were done with SPECTRE for several cases of process corner models with SGPM and HICUM under a  $50 \Omega$  input matched condition:  $L_B=1.44$  nH,  $L_E=125$  pH,  $C_{\pi,Q1}=180$  fF,  $\omega_T=414.7$  Grps,  $g_{m,Q1,2}=100.7$  m $\Omega$ ,  $\beta_{DC}=112.5$  and  $Q_{input}=1.36$ . Figure 4.7 shows the  $NF$  simulation results at 12 GHz versus collector bias current, along with the theoretical value from (4.7) where  $\delta_z$  and  $\eta_z$  are approximated as 1 and 0.5, respectively, for the frequency range of 10-15 GHz. The simulated  $f_T$  of  $Q_{1,2}$  is also shown together in Figure 4.7. The SGPM results in a slightly higher  $NF$  than HICUM, and there is about 1 dB of  $NF$  variations between process corners at the optimum bias points. Within these variations, (4.7) provides reasonable  $NF$  estimations, and the achievable minimum  $NF$  from (4.7) and SPECTRE with nominal process model is around 3.5 dB with  $I_C=2.7$  mA. The ESD diodes, cascoding stage and active load with  $I_{C,QL}=0.2$  mA increase this  $NF$  further by 0.2-0.3 dB in the simulations. The net  $NF$  improvement by the PMOS current sources  $M_{P1,2}$  is around 3.8-4 dB at 10-12 GHz.

The simulated  $S_{11}$  is  $< -10$  dB from 10.7 GHz to 15.8 GHz. With the optimized values of  $R_{L1}=400 \Omega$ ,  $C_{p,QL}=22$  fF ( $l_e$  of  $Q_{L1,2} = 1.4 \mu\text{m}$ ) and  $I_{C,Q1}/I_{C,QL}=13.5$ , the differential voltage gain in the first stage from (4.5) is 27 dB at 12 GHz, consistent with SPECTRE simulations. The second stage gives additional 6.5 dB gain with a bias current of 2.5 mA. The output impedance



**Figure 4.8:** 4-bit differential active phase shifter based on I/Q signal interpolation.

of the emitter-follower driving the next I/Q network is about  $13 \Omega$  with 2 mA of bias current per path. The overall  $IIP_3$  of the LNAB is around -30 dBm for a voltage gain of 33.5 dB at 12 GHz in SPECTRE simulations.

### 4.3.2 4-Bit Differential Active Phase Shifter

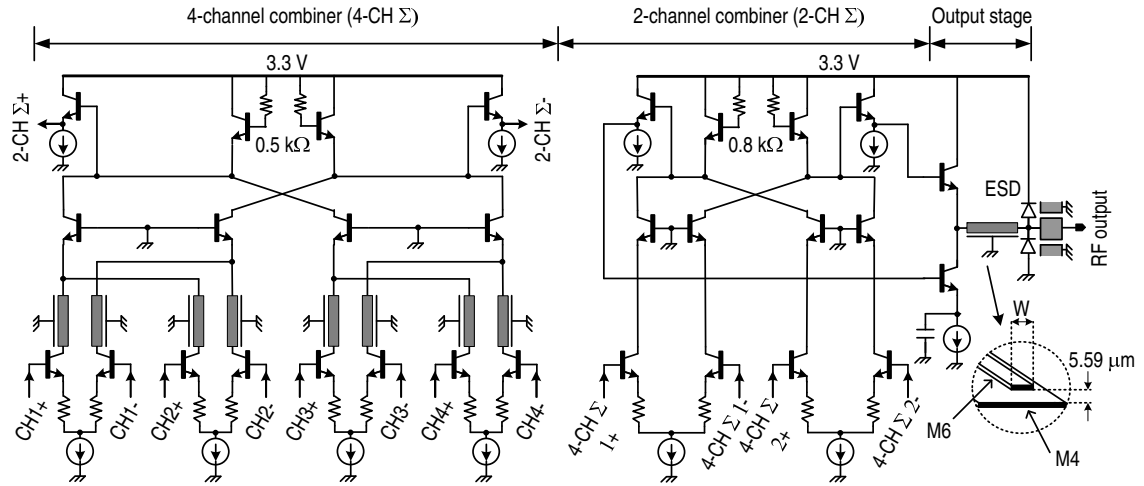
The integrated RF active phase shifter shown in Figure 4.8 is an essential building block for the 8-element phased-array. The  $2^{nd}$ -order quadrature all-pass filter provides a wide-band differential I/Q signal with maximum 3 dB voltage gain. An important issue of the QAF for high frequency applications ( $> 10$  GHz) is parasitic loading effect causing I/Q errors. The lower impedance design of the filter alleviates this, and therefore a filter impedance of  $25 \Omega$  is chosen with a resonance at 12 GHz:  $R=25 \Omega$  ( $2R=50 \Omega$  in Figure 4.8),  $L=324.2$  pH ( $Q_{peak}=15.5$  @ 29.3 GHz) and  $C=542.8$  fF. However, the low impedance of QAF loads the LNAB, and there is about 6 dB loss for the output emitter-follower of the LNAB to drive the QAF. The driving loss can be minimized using a low-impedance driver such as totempole driver [52], which will be shown in the following chapters. With 70 fF of loading capacitance from the input transistors of the adder, a conservative estimation including layout parasitic capacitances, a Monte-Carlo simulation assuming  $\Delta R/R=\pm 10\%$ ,  $\Delta C/C=\pm 5\%$  and  $\Delta L/L=\pm 5\%$  at 12 GHz, shows less than

$\pm 5^\circ$  of I/Q phase error distribution within  $1\sigma$  statistical variations, and the  $2\sigma$  and  $3\sigma$  values of I/Q phase errors are  $< \pm 10^\circ$  and  $< \pm 15^\circ$ , respectively. I/Q amplitude error distributions are less than 0.8 dB for all statistical sample variations at 12 GHz. The adder is realized with 0.18- $\mu\text{m}$  NMOS for better linearity. Another important reason for this choice is to change phases with constant amplitude, i.e., the square-root gain dependency on bias current in NMOS enables a phase change with constant amplitude as long as  $(I_I+I_Q)$  is constant, even though the ratio of  $I_Q/I_I$  is different for each 4-bit phase state, as discussed in Chapter-3. It is worthwhile to mention that since the output phase is set by the ratio of  $I_Q/I_I$  rather than the absolute values of the  $I_Q$  and  $I_I$ , and the ratio  $I_Q/I_I$  can linearly track the process, supply voltage and temperature (PVT) variations to the first order, the output phase accuracy can be fairly constant over the PVT variations. The input transistors are biased at  $V_{gs}-V_{th} \simeq 0.5$  V with sizing of  $W/L=20/0.18$  and bias current of 2.5 mA, which results in an  $\text{IIP}_3$  of  $\sim 15.5$  dBm at 12 GHz. The simulated gain is  $-1.5\sim -2.5$  dB with an active load consist of  $M_{AL}$  ( $W/L=20/0.18$ ) and  $R_{AL}$  ( $600 \Omega$ ). The cumulative differential voltage gain per channel including LNAB and phase shifter is about 27 dB at 12 GHz in simulations, and the NF and  $\text{IIP}_3$  of LNAB dominate the overall channel performance. The DAC and logic are designed for 4-bit phase control capability, excluding the calibration path in Figure 3.12 in Chapter-3, and are implemented using 0.36- $\mu\text{m}$  CMOS to be compatible with 3.3 V supply voltage.

### 4.3.3 Differential Channel Combiners and Output Stage

The coherent RF signal combining of the individual signals is an important part of practical phased arrays since any phase imbalance and amplitude error between each path of the combiner network can degrade the array factor. In traditional phased array systems, the RF combiner is realized using passive components such as Tee-junction splitter/combiner or Wilkinson splitter/combiner, which will be shown in the next chapter. However, these passive networks are not practical for on-chip combining due to their large size at 6-18 GHz. Therefore, the combiners are realized with active adder amplifiers in this design (Figure 4.9). The signal combining can be very wideband in these active combiners at the expense of power consumption. The isolations between different channels also can be better due to the unilateral behavior of active circuits, but they suffer from linearity issue.

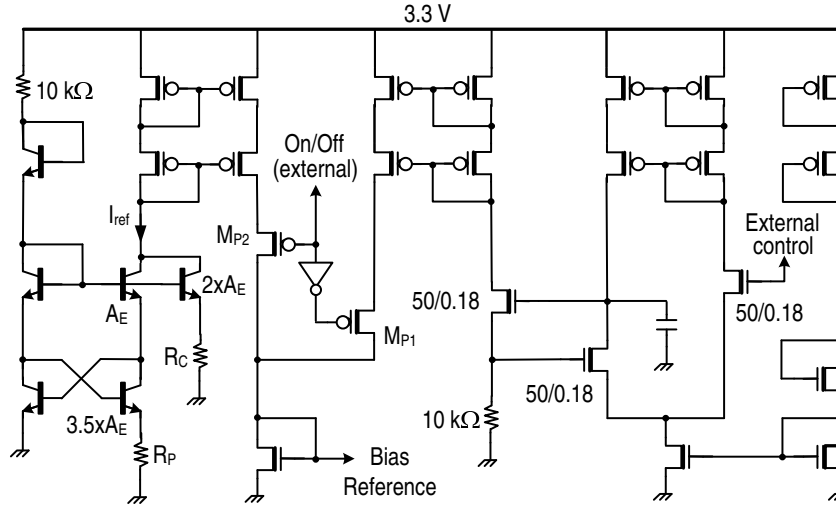
In the 4-CH  $\Sigma$ , the differential input transconductors are distributed at the output of



**Figure 4.9:** Channel combiners and output balun stage.

each array element in layout, and the combining of the 4 channels is done in binary fashion. First, the differential outputs from every two elements are added in the current domain at the emitter nodes of the cascoding stages, after guided by a differential microstrip line (DM-line). The DM-line is realized with top metal (Metal 6, sheet resistance=10.5 m $\Omega$ , thickness=2.81  $\mu\text{m}$ ) as a signal line and Metal 4 (sheet resistance=10.5 m $\Omega$ , thickness=0.62  $\mu\text{m}$ ) as a ground plane. These two metal layers are separated by SiO<sub>2</sub> layer ( $\epsilon_r=4.15$ , thickness=5.6  $\mu\text{m}$ ). The DM-line impedance is matched with the emitter resistance (12  $\Omega$ ) of the cascoding transistors to provide stable combining of the RF currents in terms of load reflections and node parasitics. Then, the combined signals at the first level are added together at the output nodes. The cascoding stage provides excellent isolation between *Channel-1&2* and *Channel-3&4*. The degeneration resistance is 100  $\Omega$  and increases the linear input range. The bias current in the 4-CH  $\Sigma$  is 3.2 mA per each differential path. The standalone 2-CH  $\Sigma$  adds the two outputs from the 4-CH  $\Sigma$ s, providing yet another isolation stage between the summed channels (Figure 4.9). The bias current in each differential path in the 2-CH  $\Sigma$  is 4 mA and 125  $\Omega$  of emitter-degeneration is used. The active loads are optimized for a peak gain at 11-13 GHz with an overall 3-dB gain bandwidth of 8-15 GHz, and the overall voltage gain in the 8-channel combiner (4-CH  $\Sigma$ +2-CH  $\Sigma$ ) is about +1 dB at 12 GHz with an IIP<sub>3</sub> of +1.5 dBm in SPECTRE simulations.

The NPN-based Class-A push-pull amplifier is used for output balun stage (DTS) and an internal microstrip line (M-line) guides the output signal to the output port. The M-line width, W in Figure 4.9, is tapered from 20  $\mu\text{m}$  ( $Z_o \simeq 30 \Omega$ ) to 9.5  $\mu\text{m}$  ( $Z_o \simeq 50 \Omega$ ) to minimize



**Figure 4.10:** Details of the bias circuits for the 8-element phased-array.

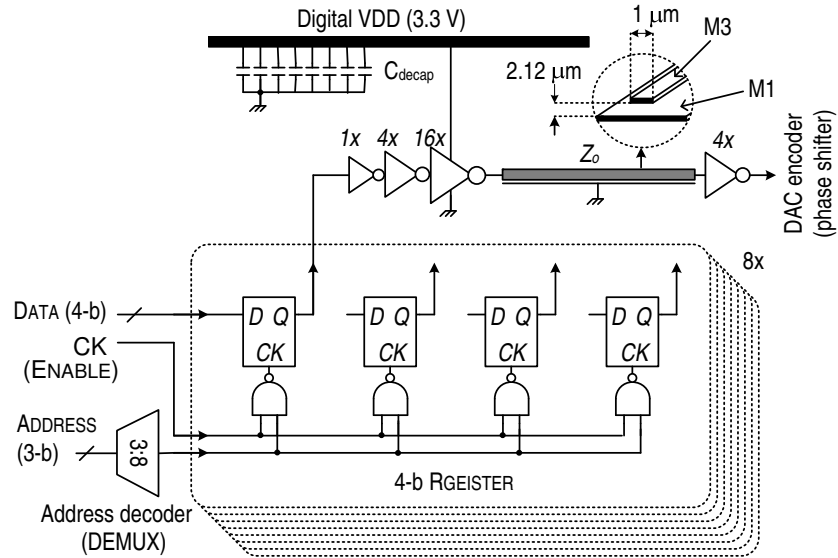
the impedance discontinuity between the balun stage and the output port.

#### 4.3.4 Biasing

The total bias current is referenced to a bandgap current generated by a bias circuit shown in Figure 4.10. With the indicated emitter area ratios,  $R_P$  ( $=1.5 \text{ k}\Omega$ ) and  $R_C$  ( $=10 \text{ k}\Omega$ ) generate PTAT current and CTAT current, respectively, and combining these two results in a bandgap reference current ( $I_{ref}=110 \text{ }\mu\text{A}$ ) [65]. The temperature sensitivity ( $=|1/I_{ref} \times \partial I_{ref}/\partial T|$ ) of the  $I_{ref}$  is less than 23 ppm/ $^\circ\text{C}$  at the temperature variation of 0~100 $^\circ\text{C}$  in SPECTRE simulation ( $\partial V_{BE}/\partial T \simeq -1.5 \text{ mV}/^\circ\text{K}$ ). The bias circuit also includes an external control path, by turning  $M_{P1}$  on and  $M_{P2}$  off, for adjusting the bias current in case external LNAs precede the array, where a low power operation is preferable to noise or gain performance.

#### 4.3.5 Digital Controls

The control logic in the array decoder is designed with 0.36- $\mu\text{m}$  CMOS (FO4 delay  $\simeq 150 \text{ ps}$ ) to be compatible with a 3.3 V supply voltage. Figure 4.11 shows a simplified diagram of the digital control paths. The output from an address decoder (3:8 DEMUX) together with an enabling clock signal load a 4-bit data stream, setting one of 4-bit phases to an array element, into a register allocated by an address determined by the DEMUX. The 4-bit register ( $8\times$ ) is composed of level-triggered D-flip-flops. A buffer driver uploads the data to a DAC encoder of the array element having the same address. M-lines are used as the control bus



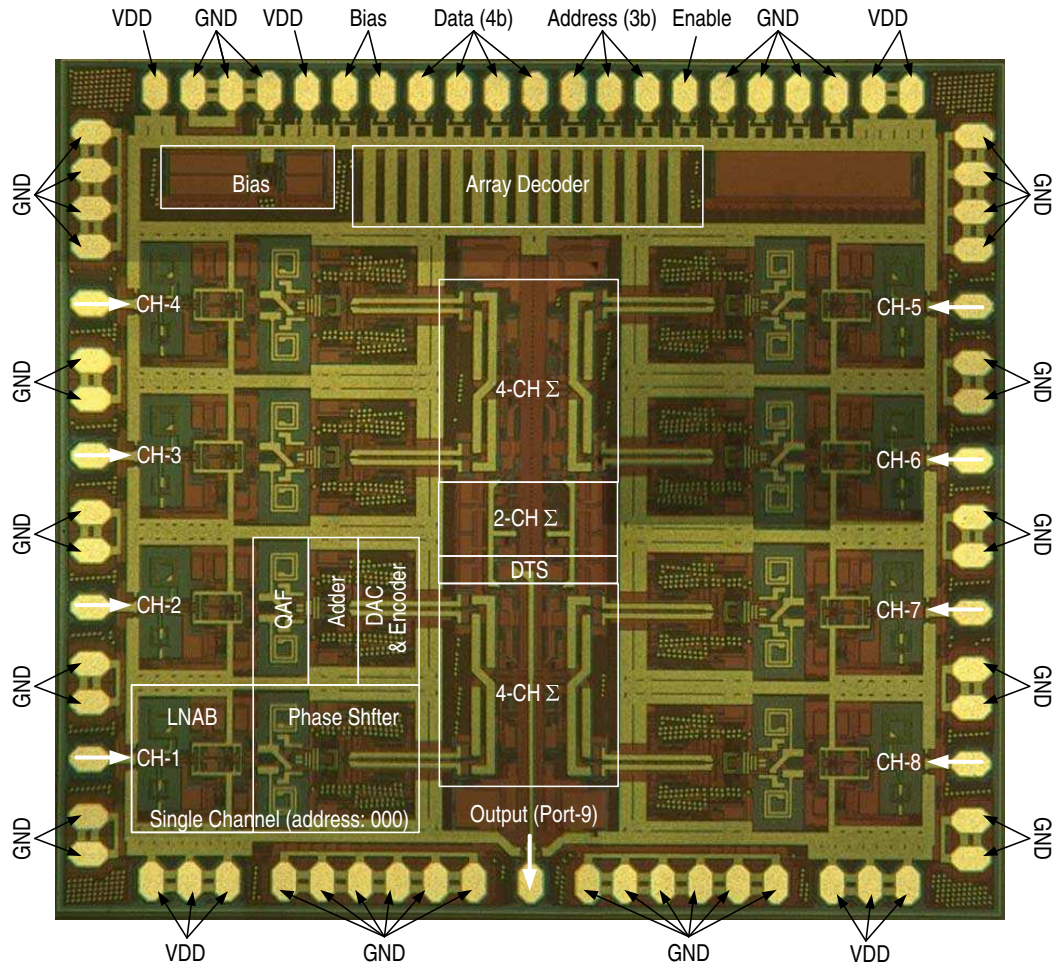
**Figure 4.11:** Simplified illustration of the digital control paths.

distribution networks and are terminated by another inverter buffer driving the DAC encoder. The interconnection M-line is realized with Metal 3 (sheet resistance=82 m $\Omega$ /, thickness=0.51  $\mu$ m) for signals and Metal 1 for ground plane, and its characteristic impedance [ $Z_o=\sqrt{(L/C)}$ ] is 85  $\Omega$ . The inductance effect of the transmission line is minimal as the pull-up and pull-down resistances ( $> 1$  k $\Omega$ ) of the buffer are much larger than  $Z_o$ . The longest transmission line length is around 2  $\mu$ m and the estimated Elmore Delay of the aluminum line is 33 psec ( $R_{line}=165$   $\Omega$  and  $C_{line}=465$  fF), which is much less than the FO4 delay. Therefore, the gate switching delays determine the overall path delay. The critical path delay including the interconnection line and DAC encoder is less than 50 ns, resulting in maximum control clock frequency of 20 MHz.

### 4.3.6 ESD Protection

All I/O pads including RF pads are protected using dual-diode ESD cells. The ESD diodes are constructed from MOS S/D junctions with a reverse breakdown of 8-10 V. Both diodes in the RF pads can survive up to about 1.6 kV and 1.1 A of positive polarity HBM (Human Body Model). The overall parasitic capacitance from the ESD diodes at the RF pads is about 40 fF per channel. The ESD diodes on the digital I/O pads are sized to be tolerant up to 3 kV (2 A) of HBM rating.





**Figure 4.12:** Chip microphotograph of the 8-element phased-array receiver ( $2.2 \times 2.45 \text{ mm}^2$ ).

#### 4.4 Measured Results And Discussions

The phased array receiver is realized in a  $0.18 \mu\text{m}$  one-poly six-metal (1P6M) BiCMOS process (Jazz SiGe120). Figure 4.12 shows the chip microphotograph of the phased array and overall chip size is  $2.2 \times 2.45 \text{ mm}^2$ . A near perfect corporate-feed layout was done on the 8-element receiver, and the electrical distances between the output port (*Port-9*) and every other channel are virtually identical. The channels are isolated using metallic barriers, composed of a series of via stacks from the substrate to metal 5 and tied to ground planes (M1 or M4) so as to minimize the parasitic interactions between the channels. The top metal, M6, is used for analog-VDD which is capacitively coupled to the metallic barriers for added isolation. The 4-CH  $\Sigma$ s are laid out in a perfectly symmetrical fashion with input differential lines from each channel.

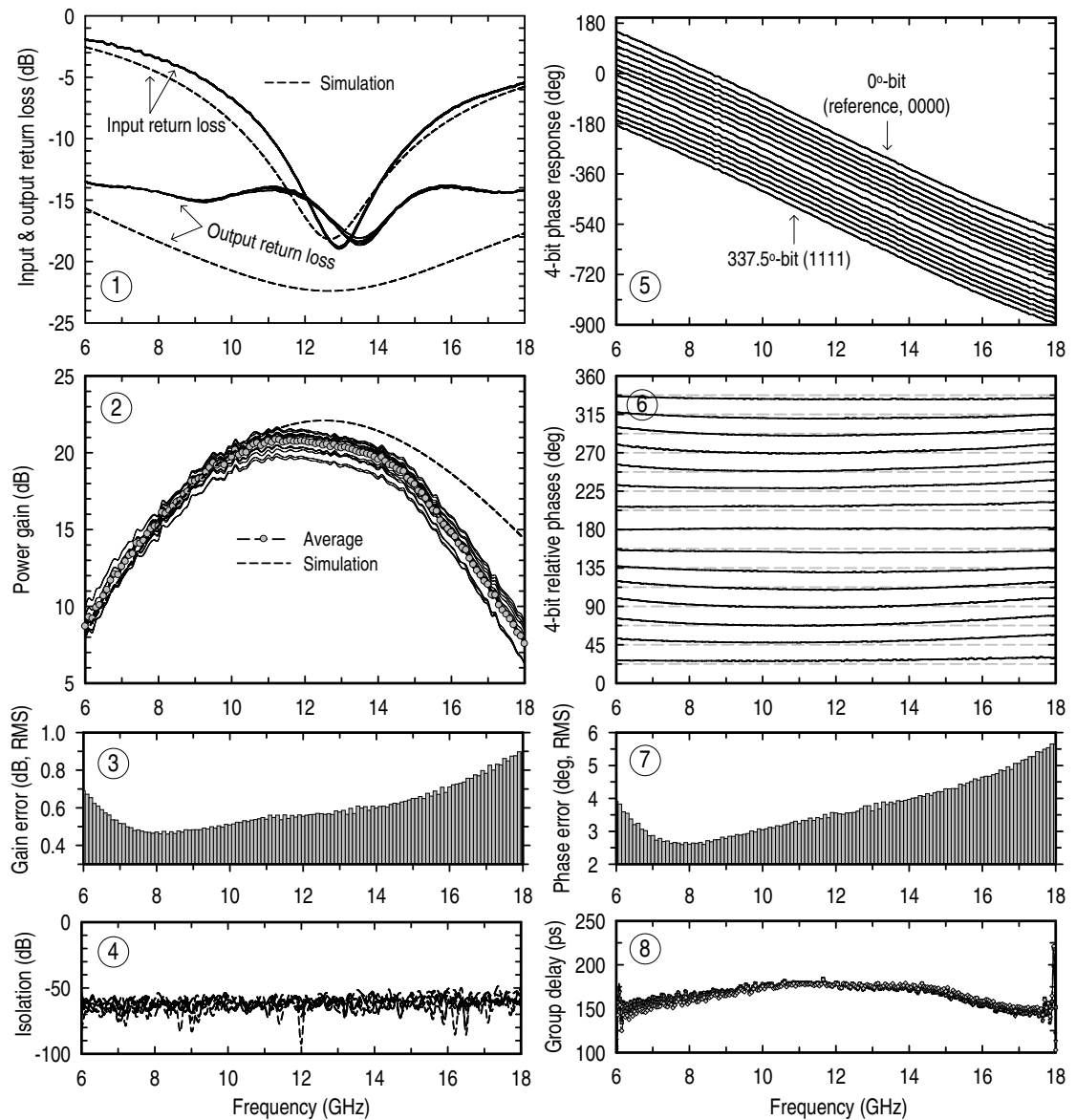
The final 2-CH  $\Sigma$  also has a symmetrical layout, and the output of the DTS (output balun) is in a microstrip mode which is tightly coupled to the M4 ground plane. Analog-VDD and Digital-VDD are separated on-chip to isolate the digital switching noise from the analog paths, and large on-chip decoupling capacitors are used in the supply lines and in the DC bias paths.

The array receiver was measured on-chip after a standard SOLT calibration with a vector signal network analyzer (Agilent, PNA-E8364B). The measurements are done without any calibration or trimming. The only control inputs applied to the chip are supply voltages (analog and digital), address bits (3-bit), data bits (4-bit) and enabling clock signals. The phased array consumes 170 mA with the internal bandgap reference from a 3.3 V supply voltage (561 mW total and 70.1 mW per channel). It is seen that the 8 elements (LNABs + phase shifters) account for 83% ( $\simeq 17.6$  mA per element) of the DC current consumption and 16% of the DC current is consumed in the combiners (4-CH  $\Sigma$ s+2-CH  $\Sigma$ ) and DTS.

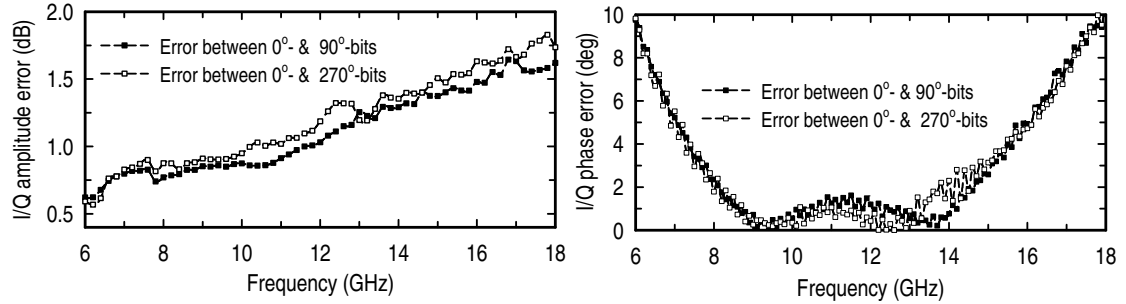
#### 4.4.1 Single Path: Matching, Gain, Phase, Isolation and QAF Characterizations

Figure 4.13 presents the measured single path (*Channel-1*) characteristics with the internal bandgap biasing for all 4-bit phase states. The input return loss ( $S_{11}$ ) is  $< -10$  dB from 11 to 15 GHz, and output return loss ( $S_{99}$ ) is  $< -13.5$  dB at 6-18 GHz (Figure 4.13 ①). A phase change in the phase shifter does not alter  $S_{nn}$  ( $n=1-9$ ) due to the high isolation provided by the LNAB and the active combiners. Simulations done in ADS with the measured  $S_{11}$  incorporating a bondwire inductance of 0.5 nH at the input port show an  $S_{11} < -10$  dB from 10 to 18 GHz. This inductance is inevitable when mounting the chip with 8 external antenna elements. In general, an off-chip interstage matching network can be designed between the antenna/amplifier and the SiGe chip to provide wideband matching at any frequency. The measured average power gain ( $S_{91}$ ) is 18-21 dB at 9-15 GHz with a 50  $\Omega$  load (average gain=20.8 dB @ 12 GHz, Figure 4.13 ②). It should be pointed out that the actual differential voltage gain per channel is 6 dB larger than the measured values, since the output DTS, inserted for 50  $\Omega$  measurements only, induces a 6 dB voltage loss for impedance matching. The measured RMS gain error with a reference of the average power gain is less than 0.9 dB for all 4-bit phase states at 6-18 GHz (Figure 4.13 ③). The isolation ( $S_{n9}$ ,  $n=1-8$ ) between the output and input ports is better than -60 dB at 6-18 GHz (Figure 4.13 ④).

The measured phase responses excited by the 4-bit digital data inputs show very linear



**Figure 4.13:** The measured single channel (*Channel-1*) characteristics for all 4-bit phase states with internal bandgap biasing ( $I_{bias}=170$  mA). ①: input ( $S_{11}$ ) and output ( $S_{99}$ ) matchings, ②: power gain ( $S_{91}$ ), ③: RMS gain error, ④: output-to-input isolation, ⑤: 4-bit phase responses, ⑥: 4-bit relative phases, ⑦: RMS phase error (from the ideal 4-bit phases) and ⑧: averaged group delays for 4-bit phase states.



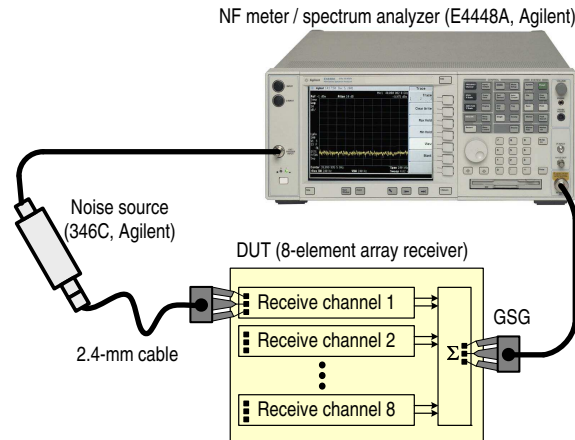
**Figure 4.14:** Measured I/Q amplitude error (*left*) and I/Q phase error (*right*) of the QAF.

phases at 6-18 GHz (Figure 4.13 ⑤). The measured 4-bit relative phases (Figure 4.13 ⑥), referenced to the measured 0°-bit phase state, highlights the fundamental merit and the limitation of the active phase shifter together: i.e., the active phase shifter can achieve nearly ideal constant phase shift over very wide frequency and is therefore not a true time delay (TTD) circuit. However, for an 8- or even a 16-element array, a constant phase shift is acceptable at the element level, and a TTD circuit is placed at the sub-array level for systems requiring  $> 20\%$  fractional bandwidth [9]. The measured RMS phase error from the ideal 4-bit phase states is  $< 3^\circ$  at 6.8-10 GHz and  $< 5.7^\circ$  at 6-18 GHz, achieving more than 5-bit accuracy (Figure 4.13 ⑦). The group delay for all 16 phase states is  $162.5 \pm 12.5$  ps at 6-18 GHz (Figure 4.13 ⑧).

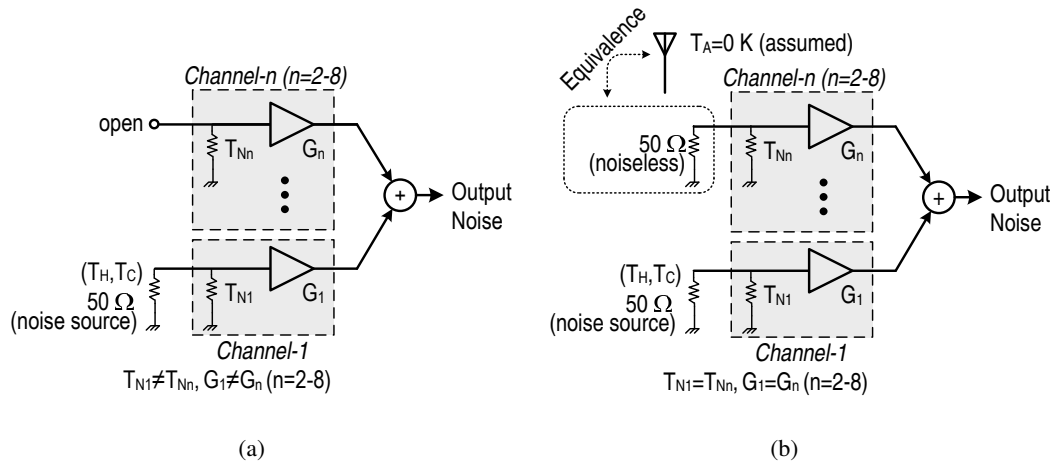
The QAF is characterized by comparisons of phase and gain of the measured 0°-, 90°- and 270°-bit S-parameters. The QAF shows excellent quadrature performance over 6-18 GHz, enough to generate 4-bit phase resolution without any calibration. The quadrature phase error is  $< 2^\circ$  at 8-14.7 GHz, and is  $< 10^\circ$  at 6-18 GHz [Figure 4.14 (*right*)]. The I/Q amplitude error is  $< 1.8$  dB at 6-18 GHz [Figure 4.14 (*left*)]. The process variations of passive components  $Q$  [ $=\sqrt{\{(L/C)/R\}}$ ] of the QAF, resulting in slightly better I/Q phase characteristic than the result in Figure 3.16 in Chapter 3.

#### 4.4.2 Single Path: NF Characterization

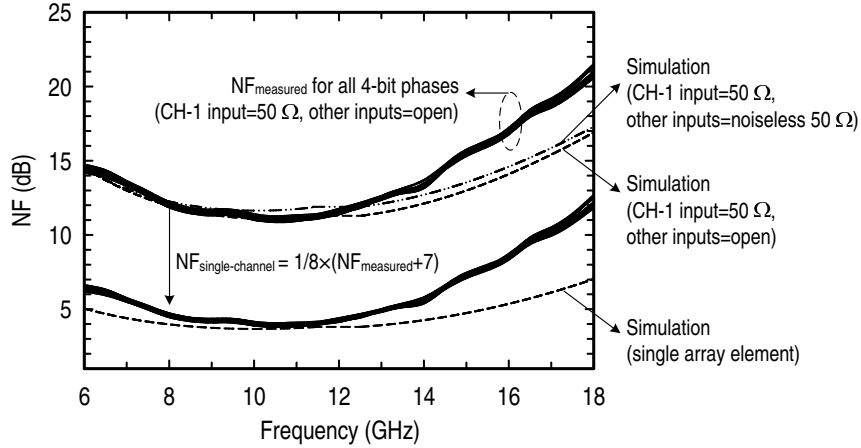
The NF is measured using the Y-factor method, given as  $NF = ENR / (Y - 1)$  where ENR is the excess noise ratio of a noise source, with a spectrum analyzer (Agilent, E4448) and a noise source (Agilent 346C, ENR=14.5-15.6 dB @ 6-18 GHz). Actually the characterization of the NF for a single channel is not straightforward, and the measured NF from the set-up shown in Figure 4.15 includes the noise from all the 8 channels, resulting in an Y-factor given in (4.8)



**Figure 4.15:** NF measurement set-up in a phased-array NF characterization.



**Figure 4.16:** NF simulation set-up for characterizing single-path NF: (a) input of *Channel-1*=50  $\Omega$  (noise source) and the other inputs=open (emulation of the measurement in Figure 4.15), (b) input of *Channel-1*=50  $\Omega$  (noise source) and the other inputs=50  $\Omega$  (noiseless). The noiseless 50  $\Omega$  simulates an antenna temperature of 0 K.



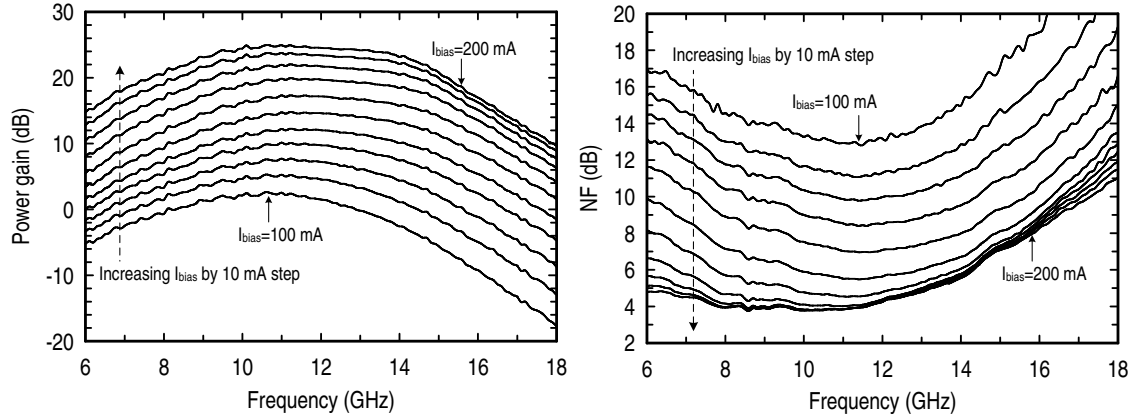
**Figure 4.17:** NF measurement set-up in a phased-array NF characterization.

where  $T_H$  and  $T_C$  are the hot and cold noise temperatures provided by the noise source, and  $T_{Nn}$  and  $G_n$  are the noise temperature and power gain of *Channel-n* ( $n=1-8$ ), respectively.

$$Y = \frac{(T_H + T_{N1})G_1 + \sum_{n=2}^8 T_{Nn}G_n}{(T_C + T_{N1})G_1 + \sum_{n=2}^8 T_{Nn}G_n} = \frac{(T_H + T_{N1})G_1 + 7T_{N2}G_2}{(T_C + T_{N1})G_1 + 7T_{N2}G_2} \quad (4.8)$$

In (4.8), it is assumed that the noise temperatures and power gains among *Channel-2* through *Channel-8* are identical. However  $T_{N1}$  and  $G_1$  are different from  $T_{Nn}$  and  $G_n$  ( $n=2-8$ ), respectively, since the input of *Channel-1* is terminated with  $50 \Omega$  while the others are left open-circuited during the measurements. In order to study the effect of the open-circuit at the inputs on *Channel-n* ( $n=2-8$ ), SPECTRE noise simulations (from the input of *Channel-1* to the final output of the array receiver) were done for two cases: 1) The input of *Channel-1*= $50 \Omega$  (noise source) and the inputs of *Channel-n*=open ( $n=2-8$ ) [Figure 4.16(a)], and 2) the input of *Channel-1*= $50 \Omega$  (noise source) and the inputs of *Channel-n*= $50 \Omega$  (noiseless,  $n=2-8$ ) [Figure 4.16(b)]. The noiseless  $50 \Omega$  simulates an antenna temperature of 0 K. Figure 4.17 presents the measured and simulated results. The simulations are similar for the two cases and the maximum difference is  $< 0.5$  dB at 6-18 GHz. This validates the approximation of  $T_{N1} \simeq T_{Nn}$  and  $G_1 \simeq G_n$  ( $n=2-8$ ) within about 0.5 dB of error boundary, and therefore the noise figure per single channel can be estimated as

$$NF_{\text{single-channel}} \simeq \frac{1}{8} \times (NF_{\text{measured}} + 7). \quad (4.9)$$



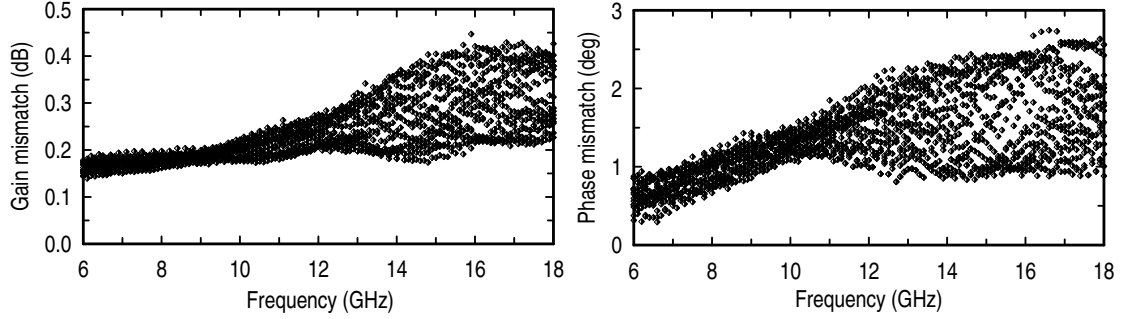
**Figure 4.18:** Measured power gain (*left*) and NF (*right*) with bias current control from *Channel-1* ( $I_{bias}=100 \sim 200$  mA).

This is shown in Figure 4.17 where the NF simulation for a single array element is also presented. The average NF over all phase states is  $< 5$  dB at 8-13 GHz with a minimum of 3.92 dB at 10.5 GHz, which agrees well with simulations validating the analysis given in the Appendix B.

#### 4.4.3 Single Path: Gain & NF versus Bias Current

The overall gain can be adjusted by switching to the external bias control, and Figure 4.18 show the gain and NF variations, respectively, with different bias currents for *Channel-1* with  $0^\circ$ -bit phase setting (data=0000). At 12 GHz, the power gain varies from 1.5 dB to 24.5 dB with increasing bias current and the NF varies from 4.2 dB to 13.2 dB. The achievable minimum NF is 3.8 dB at 10-11 GHz with  $I_{bias}=180$  mA. The measured  $S_{11}$  versus bias current is very close to that of Figure 4.13 (Ⓐ), and  $S_{99}$  is  $< -10$  dB at 6-18 GHz for  $100 \text{ mA} \leq I_{bias} \leq 200$  mA.

The measured  $IIP_3$  with  $I_{bias}=170$  mA at 12 GHz is -31 dBm and varies from -18 to -33 dBm with  $I_{bias}=100$ -200 mA. These are acceptable for satellite systems whose  $IIP_3$  requirements are typically  $-40 \sim -28$  dBm according to gain variations, since they have protected frequency bands and very directive antennas. The  $IIP_3$  is limited by the two-stage LNAB with a large voltage gain, and not by the phase shifter or combiners, and therefore can be improved substantially by replacing the LNAB with a passive balun or a single-stage differential LNA (for a fully differential design).



**Figure 4.19:** Measured mismatches among the eight channels: RMS gain mismatch (*right*), and RMS phase mismatch (*left*).

#### 4.4.4 8-Element Array: Channel Mismatch Characterizations

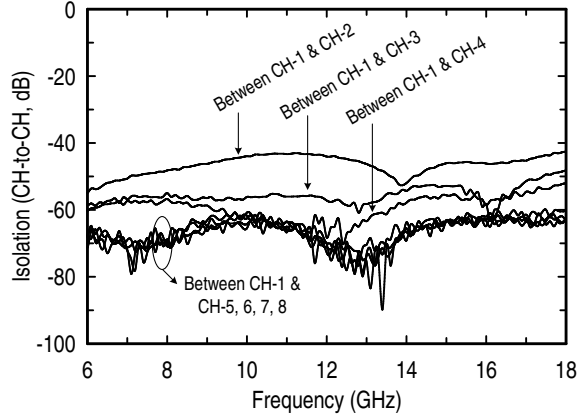
Two-port  $S$ -parameters (6-18 GHz) were measured between  $Channel-n$  ( $n=1-8$ ) and the output port for the 4-bit phase settings on each channel, resulting in  $8$  (channels)  $\times$   $16$  (phase states) =  $128$  two-port  $S$ -parameters, to fully characterize the array receiver. The measurement were done with an internal bias of  $I_{bias}=170$  mA. The measured input and output reflection coefficients,  $S_{nn}$  ( $n=1-9$ ), are all identical to Figure 4.13 (ⓐ). The mismatch between the channels can be parameterized with an RMS phase mismatch [ $\phi_{mismatch,k-bit}$  in (4.10)] and an RMS gain mismatch [ $G_{mismatch,k-bit}$  in (4.11)] by comparing the  $S$ -parameters,  $S_{9n}$  ( $n=1-8$ ), for the same phase setting of the different channels. The 4-bit phase response and gain response of  $Channel-1$  are set as the reference values, and  $k=22.5^\circ \times n$  ( $n=0-15$ ) in (4.10) and (4.11). In other words, the RMS gain and phase differences between  $Channel-1$  and  $Channel-n$  ( $n=2-8$ ) are plotted for every phase state in Figure 4.19.

$$\phi_{mismatch,k-bit} = \sqrt{\frac{1}{7} \times \sum_{n=2}^8 |\phi_{Channel-1,k-bit} - \phi_{Channel-n,k-bit}|^2} \text{ (deg)}. \quad (4.10)$$

$$G_{mismatch,k-bit} = \sqrt{\frac{1}{7} \times \sum_{n=2}^8 |G_{Channel-1,k-bit} - G_{Channel-n,k-bit}|^2} \text{ (dB)}. \quad (4.11)$$

The RMS gain mismatch is less than 0.4 dB for all eight channels at 6-18 GHz [Figure 4.19(*left*)], and the maximum RMS phase mismatch among the eight channels is  $2.7^\circ$ , much smaller than  $22.5^\circ$  of the 4-bit phase quantization level [Figure 4.19(*right*)]. The gain and phase mismatches





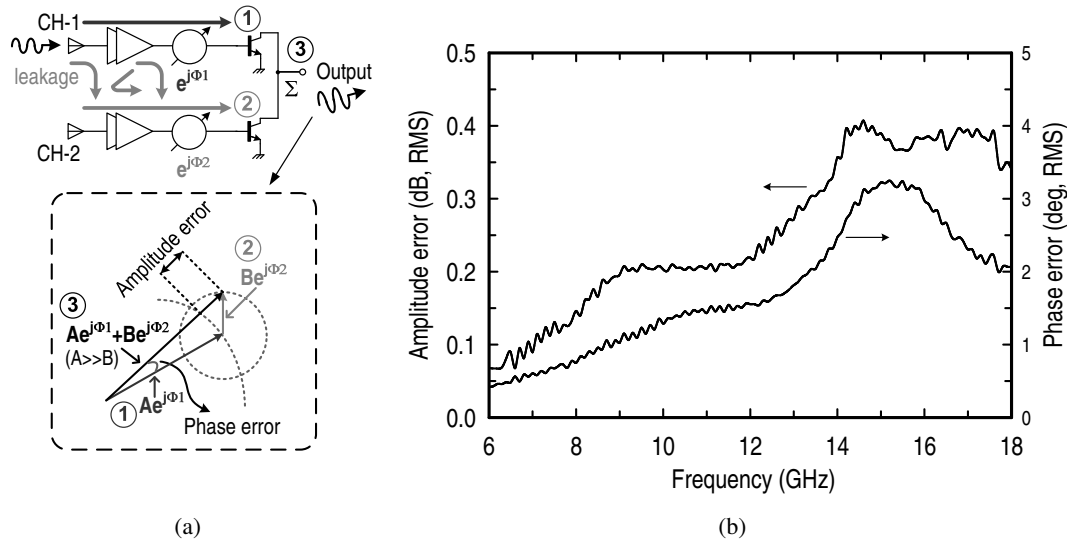
**Figure 4.20:** channel-to-channel isolations measured between input ports.

among the eight channels are truly negligible due to the integrated design and the symmetrical corporate power combiners. It is important to note that the mismatches in Figure 4.19 also include system-level measurement uncertainties such as CPW probe placement errors for all eight channels, cable stability and room temperature effects.

#### 4.4.5 8-Element Array: Coupling Characterizations

The isolation ( $S_{nm}$ ,  $n$  and  $m=1-8$  and  $n \neq m$ ) between different channels was also measured. A worst case isolation among the eight channels occurs between *Channel- $n$*  and *Channel- $(n+1)$* , where  $n=1, 3, 5$  and  $7$ . The reason is that in the first-level of signal combining shown in Figure 4.9, these two channels share the collector nodes after an internal DM-line and therefore, the base-collector capacitances of the input transistors provide a leakage path between the adjacent channels. The measured worst case isolation between the channels is around  $-43$  dB at  $18$  GHz (Figure 4.20). The other channel combinations show approximately below  $-50$  dB of isolation at  $6-18$  GHz.

A realistic and important coupling problem in every phased array is described in Figure 4.21(a). In this case, any leakage from *Channel-2* will undergo a different phase delay of  $\Phi_2$  (compared with the phase delay of  $\Phi_1$  in *Channel-1*) and add to *Channel-1* in the combiner. The leakage signal ( $Be_{j\Phi_2}$ ) therefore causes amplitude and phase errors in the true output signal ( $Ae_{j\Phi_1}$ ) from *Channel-1*. This coupling can be serious between adjacent channels on a silicon chip due to the conductive substrate. To investigate the added error due to this coupling, the phase state of *Channel-1* is set to  $0^\circ$  and the phase of *Channel-2* is varied over all

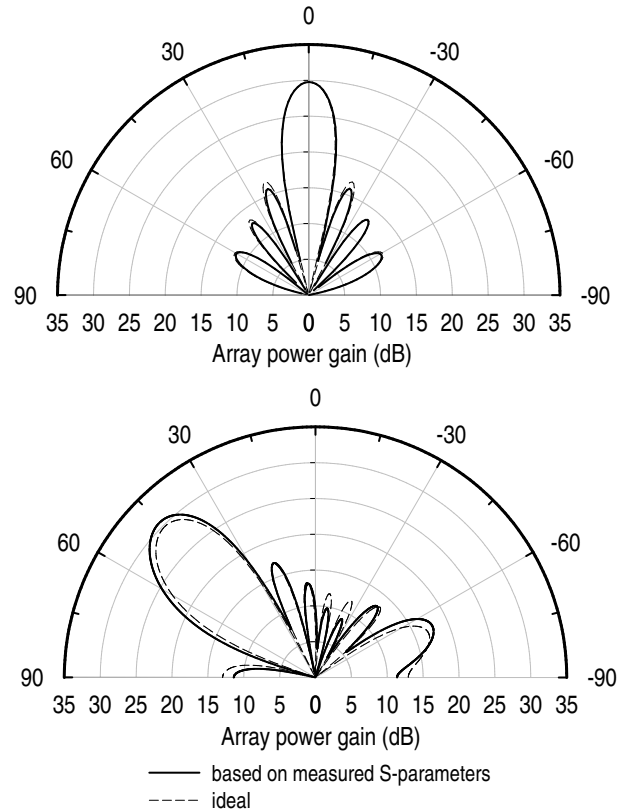


**Figure 4.21:** On-chip coupling characterization: (a) simplified coupling model from *Channel-1* to *Channel-2* along the signal path and signal errors of *Channel-1* due to the coupling; (b) measured amplitude and phase errors of the output signal from *Channel-1* due to the coupling. All the channel gains are set as  $20 \pm 1$  dB at 12 GHz.

4-bit cases and the gain and phase variations of  $S_{91}$  is recorded. During this measurement the input port of *Channel-2* is left open-circuited (not connected to  $50 \Omega$ ), which results in the worst coupling case. Figure 4.21(b) shows the measured amplitude and phase errors with a setting of  $20 \pm 1$  dB power gain at 12 GHz for all channels. The RMS gain error is  $\leq 0.4$  dB and RMS phase error is  $\leq 3^\circ$  at 6-18 GHz which are small enough to be negligible. This is due to the differential signaling and the high isolation in the layout.

#### 4.4.6 8-Element Array: Beam Pattern Characterizations

The phased array patterns (*Array Factor* [22]) were constructed in ADS at 12 GHz using the measured 4-bit  $S$ -parameter sets of all the eight channels (Figure 4.22). The measurement assumes a standard linear array with isotropic radiators and a uniform array spacing of  $d = \lambda/2$ . The ideal pattern assumes the same amplitude response as that of the measured  $0^\circ$ -bit for all ideal phase states. For a scan angle of  $0^\circ$ , the array receiver provides 29.8 dB of power gain (9 dB: array factor directivity, 20.8 dB: element power gain); the first sidelobe is below -13.8 dB at  $22^\circ$  from broadside; the 3-dB beamwidth is  $12.8^\circ$ ; and the null-to-null beamwidth is about  $30^\circ$  [Figure 4.22(upper)]. These agree well with the ideal case. The  $45^\circ$  scan angle from broadside



**Figure 4.22:** Array beam scanning characteristics: broadside scan (*upper*) and 45° scan angle (*lower*) at 12 GHz.

can be obtained by applying a progressive phase shift of  $127.3^\circ (=360^\circ/\lambda \times d \times \sin 45^\circ)$  per element for the ideal case and also by applying digitized phase shifts to the nearest measured 4-bit phase states. Again, the results are very close to the ideal case due to the very low RMS gain and phase errors between all the eight different channels [Figure 4.22(*lower*)]. The measured results are summarized in Table 4.1.

## 4.5 Conclusions

An 8-element linear phased array receiver is designed in a standard 0.18- $\mu\text{m}$  SiGe BiCMOS technology and successfully tested on-chip for X- and Ku-band applications. The design is based on the *All-RF* architecture with very broadband active phase shifters (6-18 GHz). Measurement done on all 8 channels show very low RMS phase and gain errors over 4-bit phase states both in single channel and also between the eight different channels due to the corporate-feed architecture. The demonstrated performance with an IIP<sub>3</sub> of -18 to -33 dBm is suitable

**Table 4.1:** Performance Summary of the 8-element phased-array receiver

Quantity	Results
Technology	0.18- $\mu$ m SiGe CMOS (Jazz SiGe 120, 1P6M)
Frequency band	6-18 GHz
Supply voltage	3.3 V
Current consumption	$I_{\text{bias}}=100 \sim 200$ mA (external control) $I_{\text{bias}}=170$ mA (with internal bandgap reference)
Single path (Array element)	
Phase resolution	4-bit (accuracy > 5-bit)
Input return loss	< -10 dB @ 11-15 GHz
Output return loss	< -10 dB @ 6-18 GHz
Power gain (ave, @50- $\Omega$ load)	1.5 dB (@ min. $I_{\text{bias}}$ ) ~ 24.5 dB (@max. $I_{\text{bias}}$ ) @ 12 GHz
Noise figure (ave)	4.2 dB (@ max. gain) ~ 13.2 dB (@min. gain) @ 12 GHz
Isolation (output-to-input)	< -60 dB @ 6-18 GHz
Phase error (rms)	< 5.7° @ 6-18 GHz
Gain error (rms)	< 0.9 dB @ 6-18 GHz
Group delay	162.5 $\pm$ 12.5 ps @ 6-18 GHz
IIP <sub>3</sub>	-18 dBm (@ min. gain) ~ -33 dBm (@max. gain) @ 12 GHz
Area	0.8 $\times$ 0.35 mm <sup>2</sup> (not including combiners)
Phased-array receiver	
Phase mismatch (rms)	< 2.7° @ 6-18 GHz (between all channels)
Amplitude mismatch (rms)	< 0.4 dB @ 6-18 GHz (between all channels)
Isolation (channel-to-channel)	< -43 dB @ 6-18 GHz (between all channels)
Array factor directivity	9 dB (8-elements)
Area	2.2 $\times$ 2.45 mm <sup>2</sup>

for satellite systems, and can be substantially improved in a fully differential system with the replacement of the two-stage low-noise active balun with a single-stage LNA or a passive balun preceded by an external LNA. The 8-element array can operate instantaneously at any center frequency with a wide bandwidth (3 to 6 GHz, depending on the center frequency) given primarily by the 3-dB gain variation in the 6-18 GHz. With the integration of all the digital control circuitry and ESD protections, this is the first demonstration of a phased array IC realization on a silicon chip based on the RF phase shifting architecture, thus solving one of the key barriers to complex phased array fabrication.

## 4.6 Acknowledgements

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- K.-J. Koh and G. M. Rebeiz, "An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1360-1371, June 2008.
- K.-J. Koh and G. M. Rebeiz, "An Eight-Element 6 to 18 GHz SiGe BiCMOS RFIC Phased-array Receiver," *Microwave Journal*, vol. 50, no. 5, pp. 270-274, May 2007.
- K.-J. Koh and G. M. Rebeiz, "An X- and Ku-Band 8-Element Linear Phased Array Receiver," *IEEE CICC Conf. Proc.*, pp. 761-764, Sept 2007.

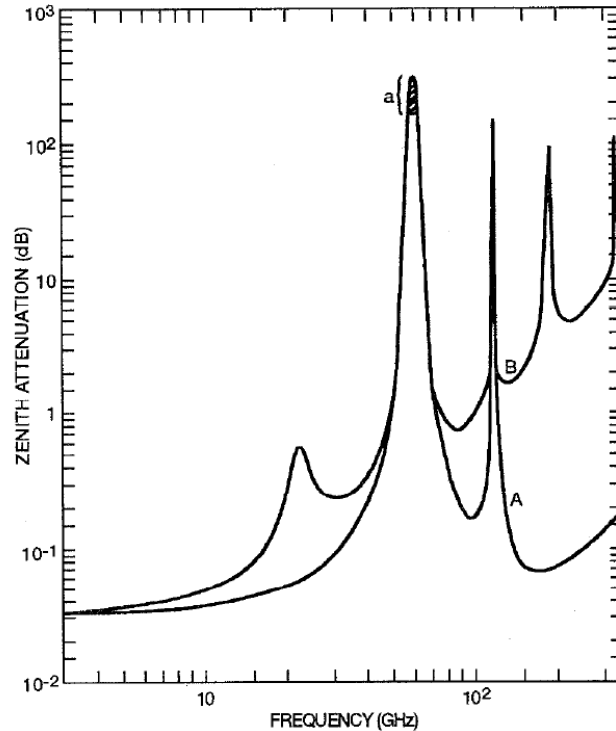
I would like to thank my coauthor Prof. Gabriel M. Rebeiz.

# 5

## **Millimeter-wave Phased-Array Design: I. Q-Band 4-Element Phased-Array Receiver in 0.18- $\mu\text{m}$ SiGe BiCMOS Technology**

### **5.1 Introduction**

Recently millimeter-wave ( $f > 30$  GHz) wireless communications have been gaining a lot of interest for high data-rate communication links [66, 67]. However, the wireless propagation channel environments are challenging at millimeter-wave frequencies: 1. the free path loss ( $L=16\pi^2R^2f^2/c^2$ ,  $R$ =distance,  $c$ =the speed of light) can be significant [68]; 2. the atmospheric attenuation due to the gaseous absorption and rain attenuation can be severe (Figure 5.1, [3]); 3. the fading also can be a serious problem at millimeter-wave frequencies [68]. These effects increase the channel noise temperature and limit the channel capacity [3, 68, 69]. Phased-arrays are an attractive solution to compensate for these propagation impairments, since a highly directive antenna improves the signal-to-noise ratio, hence channel capacity, significantly [16]. In this chapter, a Q-band (30-50 GHz) 4-element phased-array front-end receiver is demonstrated. The phased-array receiver is designed with an *All-RF* architecture where phase shifting and signal combining are done at RF level. The chip can be used as a stand-alone chip or as a sub-array for

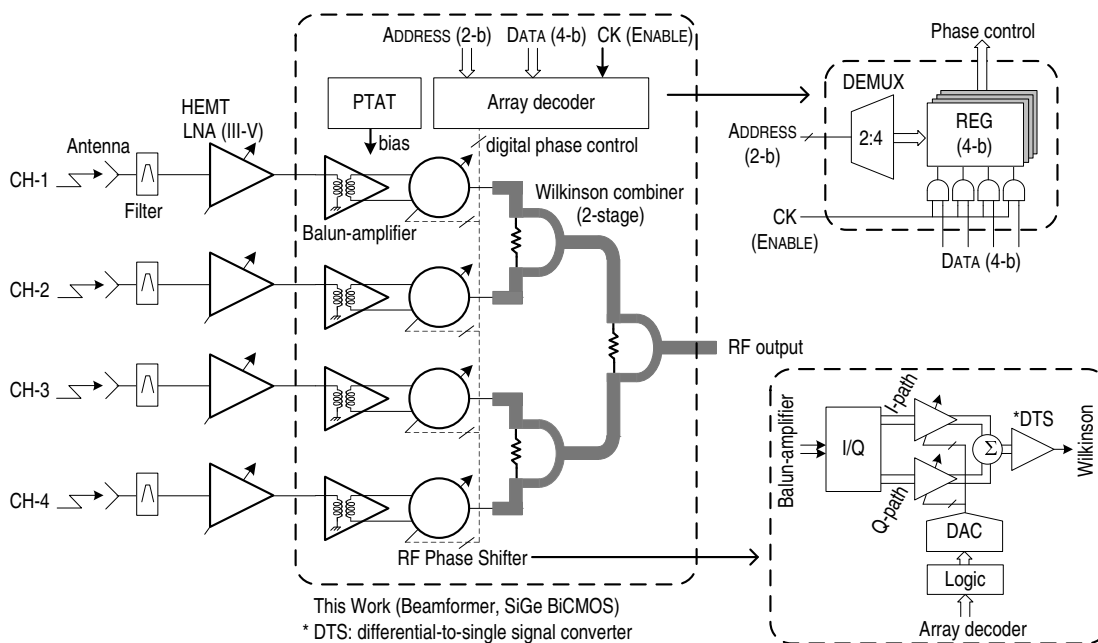


**Figure 5.1:** Total zenith attenuation due to gases, as a function of frequency (a=range of values. Curve A: dry atmosphere. Curve B: exponential water-vapor atmosphere of  $7.5 \text{ g/m}^3$  at ground level. Scale height=2 km.) [3].

large phased-arrays. Specifically the frequency band in this demonstration is optimized for the satellite systems operating at 36 to 46 GHz for high data-rate communications, or for defense applications such as high resolution radars [3]. Compared with the phased-array receiver in previous chapter, this design adopts passive signal combining method using on-chip Wilkinson couplers and results in excellent performance.

## 5.2 Phased-Array Architecture

Figure 5.2 presents the block diagram of the Q-band phased-array receiver. External filters and HEMT LNAs (GaAs or InP,  $\text{NF}=1.5\text{-}2 \text{ dB}$  and power gain= $10\text{-}16 \text{ dB @ } 40 \text{ GHz}$ ) precede the silicon beamforming network and the LNA sets the overall system noise figure. This work is focused on the 4-element silicon beamforming network, and a single channel is composed of an active balun and a 4-bit RF active phase shifter. The active balun provides broadband impedance matching ( $50 \Omega$ ) for the external LNA and wideband single-to-differential signal conversion for the differential phase shifter. The RF active phase shifter is realized using



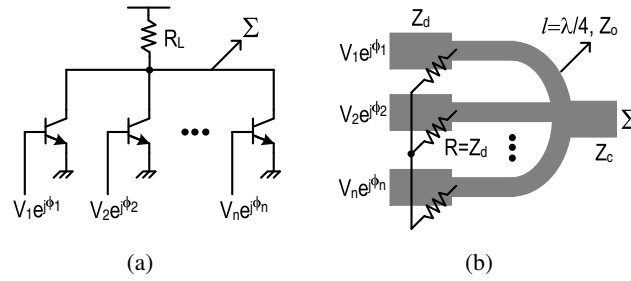
**Figure 5.2:** Functional block diagram of the Q-band phased-array front-end receiver. This study concentrates on the design of the silicon beamforming network.

a signal interpolation technique where quadrature signals are added with appropriate amplitudes to obtain the required phase. The output stage of the phase shifter is a differential-to-single signal conversion stage (DTS) and drives the Wilkinson power combining networks with a  $50 \Omega$  impedance.

In most phased-arrays, the power combining networks should be able to handle large signal levels, requiring good linearity. Wilkinson couplers are excellent candidates in terms of power handling capability and are integrated for the coherent signal combining. The Wilkinson combiners are cascaded in a corporate-feed (or binary) fashion and provide an easy way of phase calibration at the sub-array level. The phase of each phase shifter can be set independently using a 4-bit digital data input, and a digital array decoder is used to access each phase shifter. The array decoder is composed of 4-bit registers ( $\times 4$ ) for memory and 2-to-4 address decoder (DEMUX) for allocating an address to each register. The 4-bit data input is loaded to a register by a corresponding DEMUX output and by an enabling clock signal, and finally uploaded to the logic encoder of the phase shifter having the same address. The logic encoder synthesizes control logic for a digital-to-analog converter (DAC) to change the gains in each of the I- and Q-paths of the phase shifter so as to obtain the 4-bit phase response.

In this system, the linearity of the phased-array is limited by the small-signal nonlin-





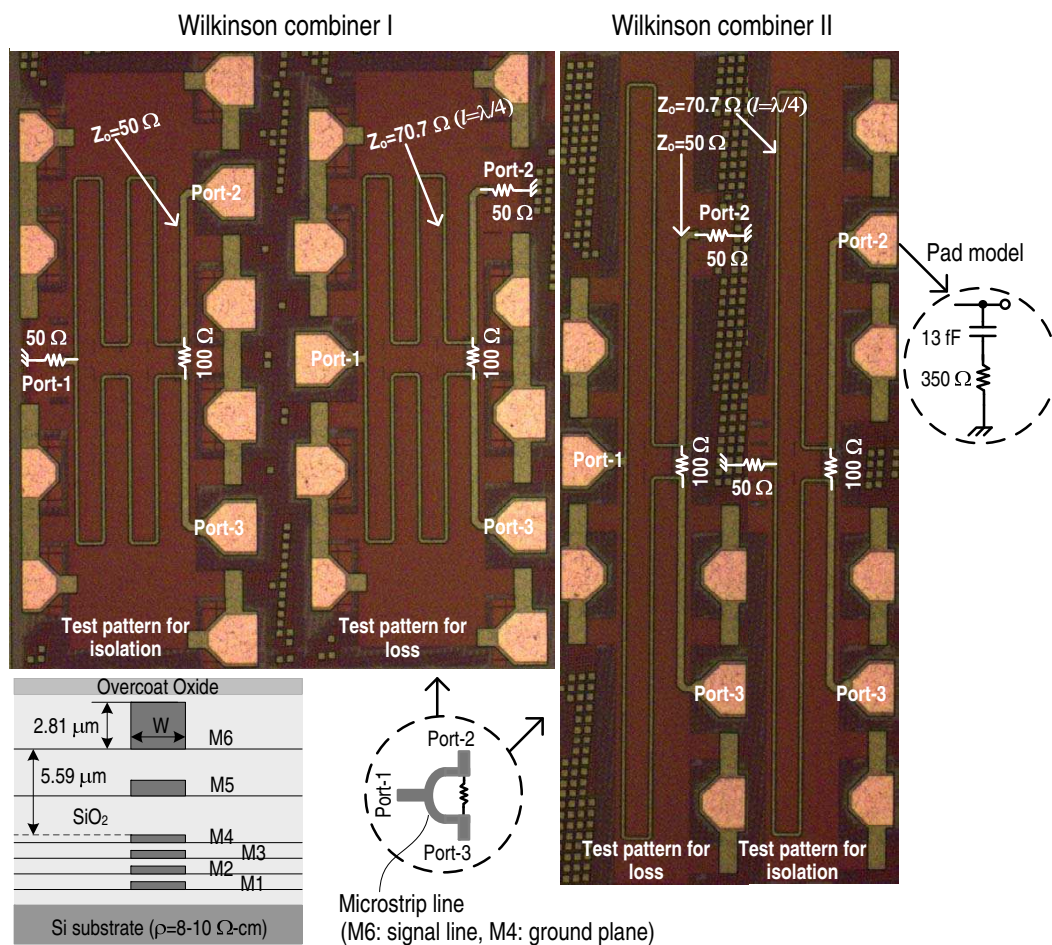
**Figure 5.3:** Signal combiners: (a) active combining, (b) passive combining ( $n$ -way Wilkinson coupler [4]).

earity of each array element, even if scaled to a large array ( $> 32$  elements), while in the active combining approach, the large signal nonlinearity in the combiner will have a detrimental effect on the overall dynamic range. Usually, the small-signal nonlinearity can be improved better (by a tradeoff with gain, noise figure or power consumption under an overall system budget) than the harmonic distortion arising from the large signal nonlinearity in typical active combiner circuits.

### 5.3 Integrated Wilkinson Couplers

A coherent signal addition in the combiner is an important part of phased-arrays, since any amplitude and phase imbalance in the combiner will degrade the array factor. There are two ways of signal combining (Figure 5.3), and for the peak phased-array angle, the phase shifters align the phases at the combiner's input ports (i.e.,  $\phi_1 = \phi_2 = \dots = \phi_n$  in Figure 5.3) although the amplitudes ( $V_1, V_2, \dots, V_n$ ) can be different depending on the aperture taper distribution on the phased-array. In the active approach, the input signals are added in current domain as shown in Figure 5.3(a) or in the voltage domain using an active transformer-based voltage summer [70]. However for these cases, a nonlinear voltage-to-current conversion is involved through a FET (BJT or MOS), and this will limit the linearity for large signal applications. Typical attempts to increase linearity such as emitter degeneration or lowering load impedance will end up with increased DC current to achieve an equivalent signal gain (or to minimize loss) in the active combiners. This DC dissipation depends on the required overall output signal level and can be substantial in large arrays with 16-256 elements.

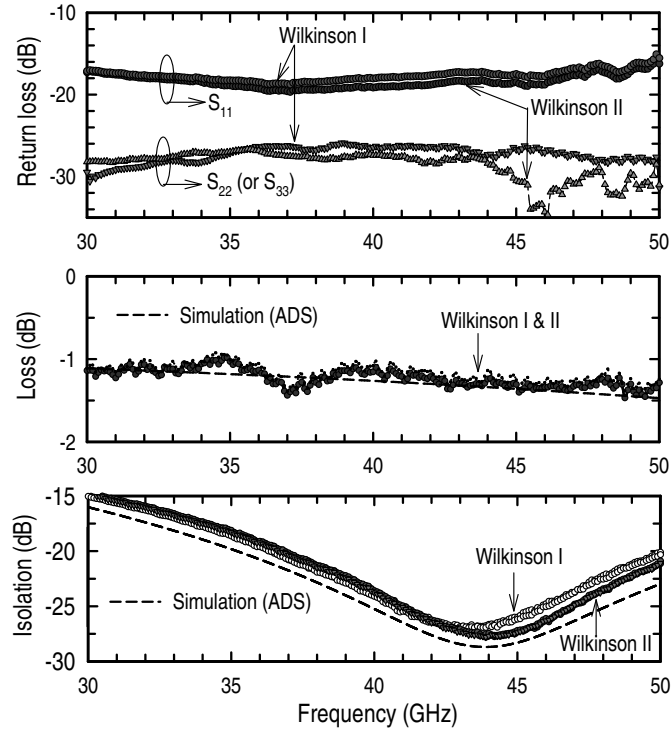
On the other hand, the Wilkinson coupler in Figure 5.3(b) where  $Z_o = \{(Z_c \times Z_d)^{1/2}\}$ , adds the inputs in a coherent way without any loss under matched conditions [4].  $Z_c$ ,  $Z_d$  and  $Z_o$  are the characteristic impedance of the transmission lines in Figure 5.3(b), and for lower loading



**Figure 5.4:** Test patterns of the integrated Wilkinson power combiners and metal stacks of Jazz SiGe120 process (1P6M). The core areas without pads are  $153 \times 494 \mu\text{m}^2$  for the Wilkinson I and  $80 \times 998 \mu\text{m}^2$  for the Wilkinson II, respectively.

to the previous stage, the characteristic impedance can be scaled up. The Wilkinson coupler is passive and is free from linearity issues without any power consumption, resulting in an ideal combiner for large arrays. The  $\lambda/4$ -transmission-line section can be replaced with a lumped L-C line at low frequencies to save area. However, at millimeter-wave frequencies, the quarter-wave line can be compactly integrated in a meandering fashion.

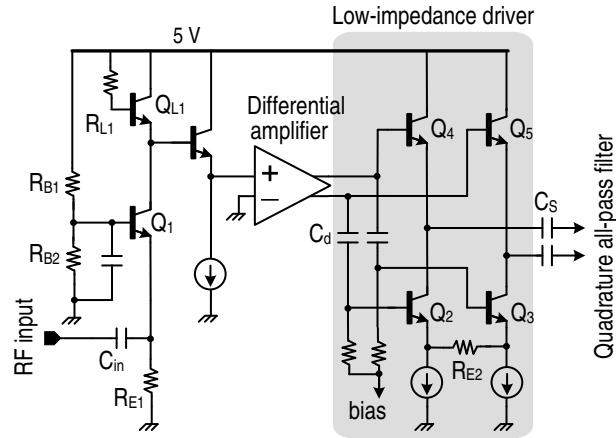
Figure 5.4 presents two different Wilkinson coupler topologies. The Wilkinson I combines the outputs from any two individual channels and the two different outputs form the combiners are finally added in the Wilkinson combier II. To be characterized with a standard two-port RF measurement, each coupler has two different test patterns: i.e., for measuring isolation between port-2 and port-3, port-1 is terminated with on-chip  $50 \Omega$ , and for loss measurement



**Figure 5.5:** Measured characteristics of the Wilkinson combiners. The simulations and measurement include the ground-signal-ground (GSG) pad parasitics.

between port-1 and port-3, port-2 is also terminated with on-chip  $50\ \Omega$ . The Wilkinson combiners are implemented with TEM-mode transmission lines in a standard  $0.18\text{-}\mu\text{m}$  SiGe BiCMOS process (Jazz SiGe120, 1P6M) and the corresponding metal stacks are also shown in Figure 5.4. The top metal (M6, thickness= $2.81\ \mu\text{m}$  and sheet resistance = $10.5\ \text{m}\Omega/\square$ ) is used for the signal line and the ground plane is implemented with M4 (thickness= $0.62\ \mu\text{m}$  and sheet resistance= $66\ \text{m}\Omega/\square$ ). The layouts keep perfect symmetry, and the core sizes excluding pads are  $153\times 494\ \mu\text{m}^2$  and  $80\times 998\ \mu\text{m}^2$  for the Wilkinson combiner I and II, respectively. For both designs, the port impedance is  $50\ \Omega$ , resulting in a characteristic impedance of  $70.7\ \Omega$  for the quarter-wavelength sections ( $l=\lambda/4=1045\ \mu\text{m}$ ,  $W=4.06\ \mu\text{m}$  @  $44\ \text{GHz}$ ,  $\text{SiO}_2\ \epsilon_r=4.2$ ). The isolation resistor of  $100\ \Omega$  is realized with a TiN metal resistor having a statistical variation of  $\pm 14\%$  for  $3\sigma$  corner models (sheet resistance= $24.5\ \Omega/\square$ ). The output of each port is routed to the pads using a  $50\text{-}\Omega$  transmission line ( $W=9.22\ \mu\text{m}$ ).

Figure 5.5 shows the measured and simulated (using Agilent ADS)  $S$ -parameters of the Wilkinson couplers. For both designs, the measured  $S_{11}$  is  $< -15\ \text{dB}$  and  $S_{22}$  (and  $S_{33}$ ) is  $< -26\ \text{dB}$  at 30-50 GHz. The intrinsic transmission loss, which is  $S_{13}$  (or  $S_{31}$ ) subtracted by  $-3\ \text{dB}$ ,



**Figure 5.6:** Q-band balun amplifier with a low-impedance output driver.

is 1-1.4 dB at 30-50 GHz and matches well with simulations. The results include the transition loss from the pad parasitics which can be modeled as a shunt capacitor ( $C=13$  fF) in series with a resistor ( $R=350 \Omega$ ). The pad model is estimated based on the library model given by the process foundry. The estimated transition loss in ADS is 0.25-0.4 dB per pad at 30-50 GHz. Therefore, the expected loss between port-1 and port-2 (or port-3) inside the phased-array chip is about 0.5-0.6 dB per Wilkinson stage at Q-band. The isolation ( $S_{23}$  or  $S_{32}$ ) between port-2 and port-3 is  $< -15$  dB at 30-50 GHz and  $< -20$  dB at 36.8-50 GHz for both designs, and matches well with ADS simulations.

## 5.4 Active Circuit Design

### 5.4.1 Balun Amplifier

Figure 5.6 presents the balun amplifier. The first common-base stage provides broadband  $50\text{-}\Omega$  match for the preceding external LNA. The balun function is realized in the second stage using a differential amplifier with one of the differential inputs grounded. The resistors  $R_{B1}$  ( $2.46 \text{ k}\Omega$ ),  $R_{B2}$  ( $2.46 \text{ k}\Omega$ ) and  $R_{E1}$  ( $750 \Omega$ ) set a 2.1 mA of bias current for the common-base stage and the emitter length ( $l_e$ ) of the input transistor  $Q_1$  is  $l_e=9.04 \mu\text{m}$  (width= $0.2 \mu\text{m}$ ). With  $C_{in}=0.2$  pF, the input return loss is less than -10 dB at 35-50 GHz in SPECTRE simulations. The balun amplifier adopts an active inductor load composed of  $Q_{L1}$  ( $l_e=1.52 \mu\text{m}$ ) and  $R_{L1}$  ( $100 \mu$ ) to minimize chip area while achieving a tuned gain characteristic with a 3-dB gain bandwidth of 37-47 GHz [50]. The equivalent inductance from the active inductor load is 186.5 pH and the

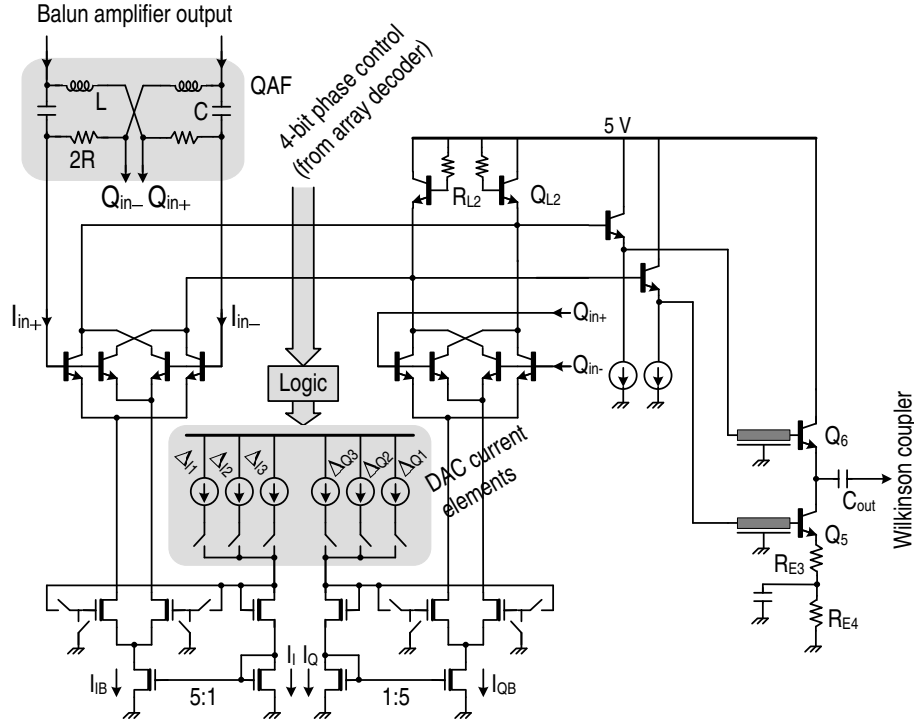
parasitic series resistance is roughly  $22.8 \Omega$  at 40 GHz. A 8.2 mA of bias current is dedicated to the second stage of a standard differential amplifier which also has an active inductor load for gain shaping and a resistive degeneration for better linearity.

The output stage utilizes the totem-pole technique [52] and drives the quadrature all-pass filter (QAF) having an input impedance of  $\sim 32 \Omega$  (differential). When driving a low impedance load, a standard CE amplifier or emitter-follower usually suffers from the limited current sourcing or sinking to (and from) the load, resulting in signal nonlinearity. In the output driver, the transistors  $Q_{2,3}$  ( $l_e=3.4 \mu\text{m}$ ) and  $Q_{4,5}$  ( $l_e=3.4 \mu\text{m}$ ) operate in a push-pull manner and improve the current driving to the heavy load: i.e., when the  $Q_2$  pulls the load down by sinking current  $\Delta I$ ,  $Q_4$  also senses the input signal with opposite polarity and pulls another  $\Delta I$  approximately from the load. As a consequence, the net current pulled from the load is doubled and so is the voltage gain. The  $Q_{3,4}$  taps the RF signal through AC-coupling ( $C_d=0.5 \text{ pF}$ ) and  $R_{E2}=25 \Omega$  is chosen for better  $3^{\text{rd}}$ -order linearity.  $C_s$  (50 fF) are DC blocking capacitor, and also resonates out the parasitic active inductance caused by the emitter followers,  $Q_{4,5}$ , maximizing the voltage transfer to the load at the design frequencies.

The balun amplifier shows a peak gain of 12 dB and a minimum NF of 11-11.5 dB at 39-42 GHz. The NF can be improved to 7-8 dB with the use of a low-noise common emitter topology employing inductive degeneration for the matching in the first stage and by replacing the active inductors with passive inductors at the expense of chip area. The  $IIP_3$  for the balun amplifier is around -14 dBm at 39-40 GHz with a differential  $32\text{-}\Omega$  load in SPECTRE simulation.

#### 5.4.2 4-Bit Active Phase Shifter

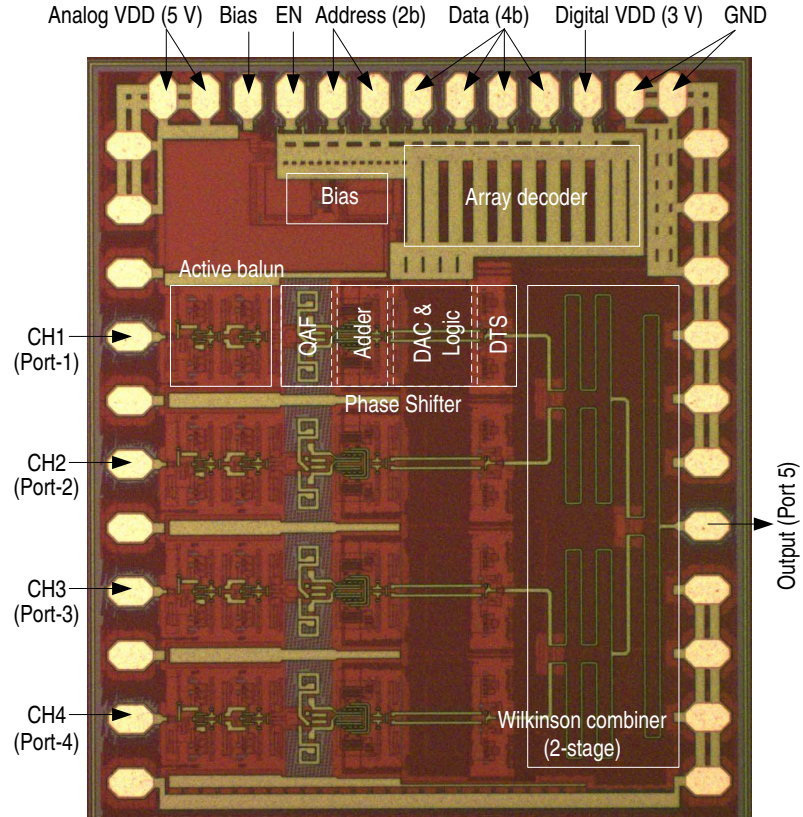
The integrated Q-band 4-bit active phase shifter is shown in Figure 5.7. The quadrature all-pass filter is designed with a low impedance of  $\sqrt{L/C}=27 \Omega$  ( $L=93.4 \text{ pH}$ ,  $C=125.4 \text{ fF}$  and  $2R=62.5 \Omega$ ), and this results in  $< 5^\circ$  of I/Q phase error at 37-48 GHz under a loading capacitance of  $C_L=70 \text{ fF}$ . The  $C_L$  includes the base input capacitance from the adder and the parasitic layout capacitance. Especially, the passive values of the QAF are optimized to get accurate I/Q phase centered at 42-43 GHz, using SPECTRE simulation under the loading capacitance [see Figure 5.10 (*right*)]. The QAF exhibits  $\leq 3^\circ$  of I/Q phase error at 36.8-48 GHz. The output phase error originating from any I/Q amplitude mismatch in the quadrature all-pass filter can be effectively suppressed by optimizing the I/Q amplitude weights accordingly (in other words, by adjusting



**Figure 5.7:** Q-band 4-bit active phase shifter. The input is differential and output is single-ended.

the DAC currents according to the I/Q amplitude mismatch from the I/Q network). For this, independent current cells  $\Delta_{I1-3}$  and  $\Delta_{Q1-3}$  are allocated for each I- and Q-path, respectively, in the DAC, and the size of each current element is optimized using SPECTRE simulations to achieve 4-bit phase accuracy with less than  $\pm 1.5$  dB of gain variations for all 4-bit phase states.

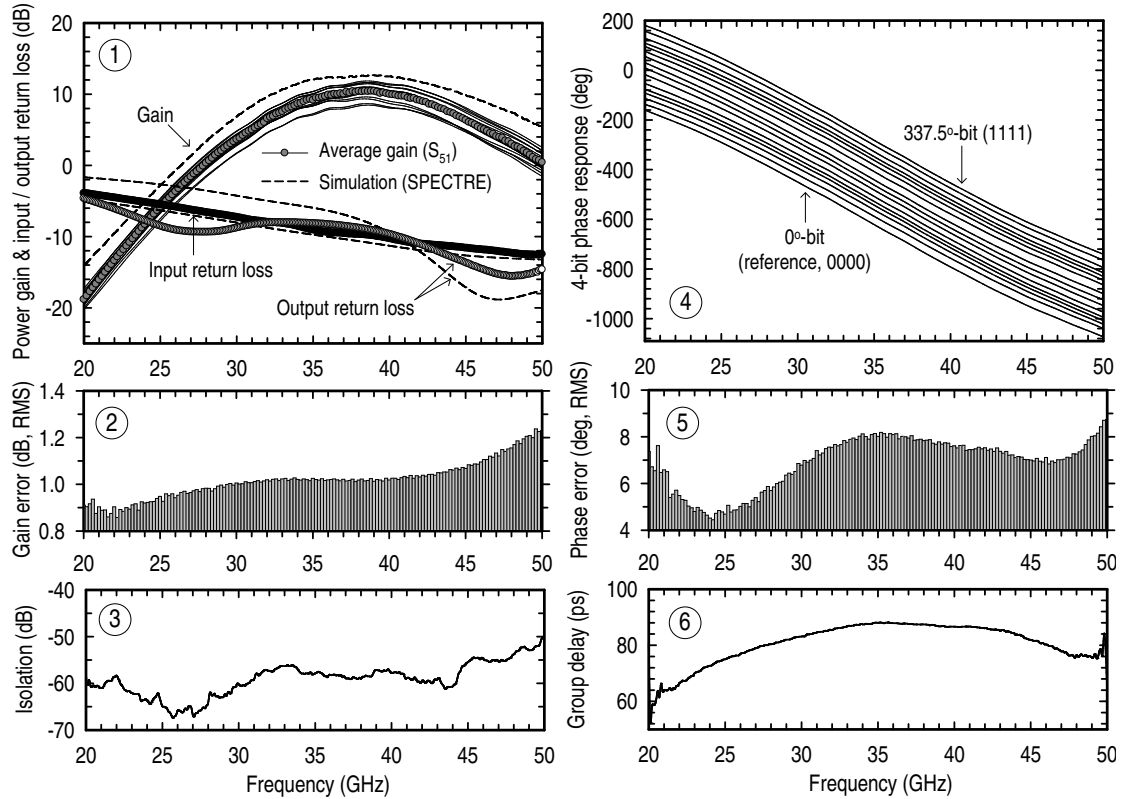
Theoretically, the bias current ratio of  $I_I:I_Q=1:\sqrt{6}$  results in the minimum phase step of  $22.5^\circ$ -bit because of the linear gain dependency on bias current in bipolar transistors ( $g_m=I_{bias}/V_T$ ). However, in reality, the different bias currents modulate the base-emitter diffusion capacitances ( $C_{diff} \propto g_m \propto I_{bias}$ ) of the input NPN transistors in the I- and Q-paths differently, and this capacitance variation causes non-negligible phase error from the required value. Therefore, an optimization is done to set the DAC current elements for the different phase shifts. It is worthwhile to note that in CMOS the gate-source capacitance is fixed as  $2/3C_{ox} \times W \times L$  in the first order as long as the transistor operates in saturation mode and the sizing of DAC elements is quite predictable as is shown in the previous chapters. The emitter length of the input transistors constituting the Gilbert-cells is  $3.4 \mu\text{m}$ . To achieve a wide 3-dB gain bandwidth, the gain characteristic in the phase shifter is staggered from that of the balun amplifier, i.e., the ac-



**Figure 5.8:** Q-band phased-array receiver front-end (area= $1.4 \times 1.7 \text{ mm}^2$  including pads).

tive load composed of  $Q_{L2}$  ( $l_e=1.6 \text{ }\mu\text{m}$ ) and  $R_{L2}$  ( $100 \text{ }\Omega$ ) is optimized for peak gain of 2.5 dB at 34-36 GHz with a 3-dB gain bandwidth of 30-40 GHz. Actually, the phase shifter core including the quadrature all-pass filter and I/Q VGAs provides a 7.5 dB of voltage gain, but the output stage loses about 5 dB for the  $50\text{-}\Omega$  matching. This results in a 14.5 dB of peak gain at 37-40 GHz with a 3-dB bandwidth of 33-46 GHz for the cascade of active balun and phase shifter.

A class-A NPN push-pull stage is used for single-ended signal conversion and drives the following Wilkinson coupler ( $50 \text{ }\Omega$ ). The  $C_{out}$  ( $75.4 \text{ fF}$ ) absorbs a finite parasitic active inductance caused by the emitter-follower  $Q_6$  ( $l_e=3.4 \text{ }\mu\text{m}$ ) and improves the impedance matching. The  $R_{E3}$  ( $35 \text{ }\Omega$ ) and  $R_{E4}$  ( $100 \text{ }\Omega$ ) are used for biasing and the  $R_{E3}$  also increases the linearity of the common-emitter  $Q_5$  ( $l_e=3.4 \text{ }\mu\text{m}$ ). The simulated  $IIP_3$  is about 6 dBm for the phase shifter core with  $0^\circ$ -bit phase setting and a  $200 \text{ }\Omega$  of differential loading impedance. The output stage shows a 9.5 dBm of  $IIP_3$  with a  $50 \text{ }\Omega$  loading around 39-40 GHz. The current consumption in the phase shifter is 10.5 mA from a 5 V supply voltage (phase shifter core: 8 mA, output push-pull stage: 2.5 mA). The overall cascade  $IIP_3$  of balun amplifier and phase shifter is  $-16 \pm 1.5 \text{ dBm}$  at



**Figure 5.9:** The measured single channel (*Channel-1*) characteristics for all 4-bit phase states. ①: input and output matching, and power gain, ②: RMS gain error, ③: output-to-input isolation, ④: 4-bit phase responses, ⑤: RMS phase error (from ideal 4-bit phases) and ⑥: averaged group delays for 0°-bit phase states.

39 GHz in SPECTRE simulations for all 4-bit phase states. The simulated noise figure for the phase shifter is 19-19.5 dB, and the cascaded NF for the active balun and phase shifter is 12.7-13 dB at 37.5-44 GHz. The interconnection transmission lines are in microstrip or grounded coplanar-stripline modes and are characterized as S-parameter sets using full electro-magnetic simulations with SONNET [71]. The digital logic is implemented with 0.36  $\mu\text{m}$  CMOS and is compatible with a 3.3 V of digital supply voltage.

## 5.5 Measured Results And Discussions

The phased-array front-end receiver is realized in a 0.18  $\mu\text{m}$  SiGe BiCMOS technology (Jazz SiGe120, SiGe HBT  $f_t=150$  GHz). Figure 5.8 shows the chip microphotograph and the overall chip size is  $1.4 \times 1.7$  mm<sup>2</sup>. A ground plane (via stack from substrate to top metal) is inserted between each channel and increases the channel-to-channel isolation. The beamformer

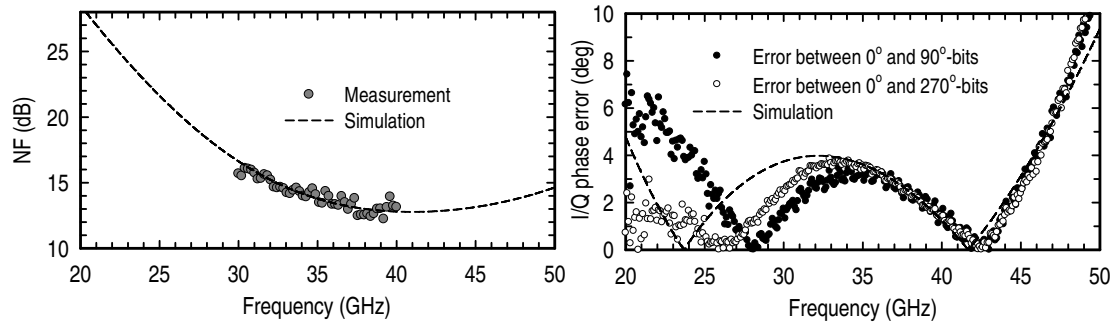


is measured on chip after a standard SOLT calibration with a vector network analyzer (Agilent, PNA-E8364B). The chip consumes 118 mA (29 mA per array element) from a 5 V analog supply voltage.

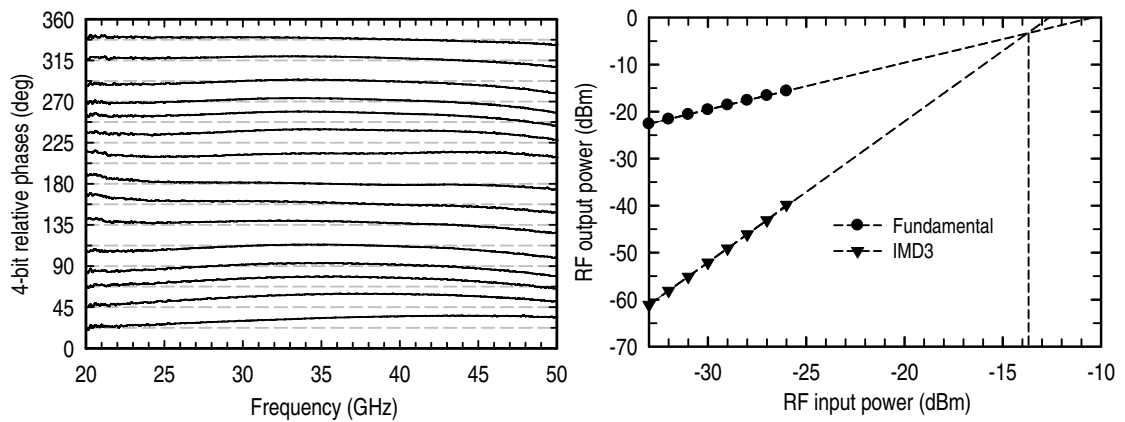
### 5.5.1 Single Channel Characterization

Figure 5.9 presents the measured single path (from Channel-1 to Port-5) characteristics of the array. The input and output return loss ( $S_{11}$  and  $S_{55}$ ) are  $\leq -10$  dB at 40-50 GHz and  $\leq -8$  dB at 32-50 GHz, and are independent of the phase state (Figure 5.9 ①). The output return loss is dominated by the output impedance of the phase shifter since the Wilkinson combiners are pure passive circuits. The power gain ( $S_{51}$ ) is shown for all 16 phase states and the average gain per channel is 10.4 dB at 38.5 GHz with a 3-dB gain bandwidth of 32.8-44 GHz (Figure 5.9 ①). The measured gain is about 2.5-3 dB lower than the simulated gain at 30-45 GHz, presumably due to device models and process deviations of the SiGe HBT combined with layout parasitics. The actual measured  $S_{51}$  is 4.4 dB and this includes the 6 dB loss in the two-stage Wilkinson combiner since each port of the Wilkinson combiner is terminated with 50  $\Omega$ . The RMS gain error from the average value is  $\leq 1.2$  dB at 20-50 GHz for all 4-bit phase states (Figure 5.9 ②). The measured output-to-input isolation ( $S_{15}$ ) is  $< -50$  dB up to 50 GHz (Figure 5.9 ③). The active phase shifter shows a linear 4-bit phase response over very wideband (Figure 5.9 ④) and the RMS phase error from the ideal 4-bit phase state is  $\leq 8.7^\circ$ , achieving 5-bit accuracy at 20-50 GHz (Figure 5.9 ⑤). The calculated group delay from the measured phase response is  $85 \pm 3$  ps at 30-45 GHz for  $0^\circ$ -bit phase state, and other phase settings show nearly same group delay (Figure 5.9 ⑥).

The NF is characterized using single-element test pattern not including Wilkinson stages, and the NF is 12.5-14 dB at 37.5-40 GHz with  $0^\circ$ -bit phase setting, which agrees well with SPECTRE simulation [Figure 5.10 (*left*)]. The NF is nearly independent of the phase state due to the gain stage of the balun amplifier. The higher NF is mainly due to the active inductor loads where internal shot noise sources of NPN HBTs degrade the output noise as indicated in the previous chapter. To minimize the noise, the active loads should be placed by spiral inductors in practical systems at the cost of chip area as mentioned in the design section. The measured I/Q phase characteristics of the QAF agree well with the SPECTRE simulation, and the I/Q error is  $\leq 3^\circ$  at 36.6-45.6 GHz [Figure 5.10 (*right*)]. The measured relative phase states shows the 4-bit



**Figure 5.10:** Measured NF from single channel test pattern (*left*), and I/Q phase imbalance in the QAF (*right*).

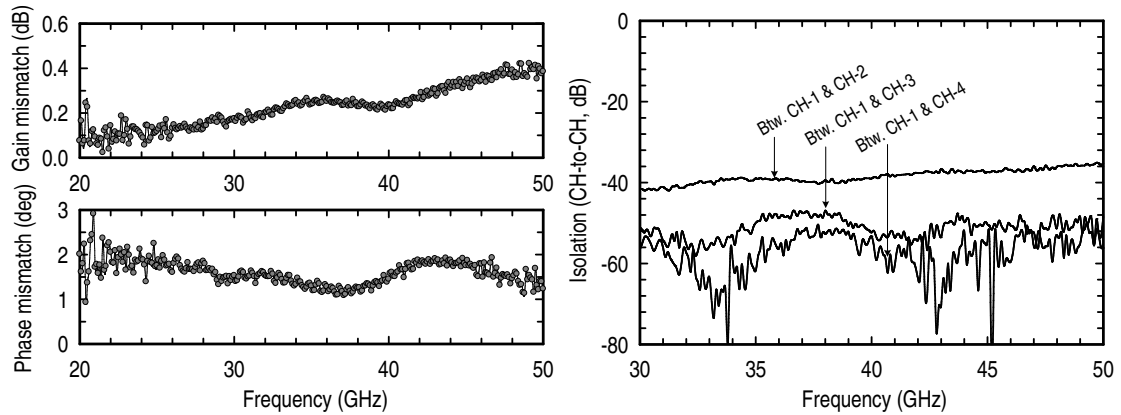


**Figure 5.11:** The measured 4-bit relative phase states (*left*), and two-tone linearity test result at 38.5 GHz with 0° phase setting (*right*).

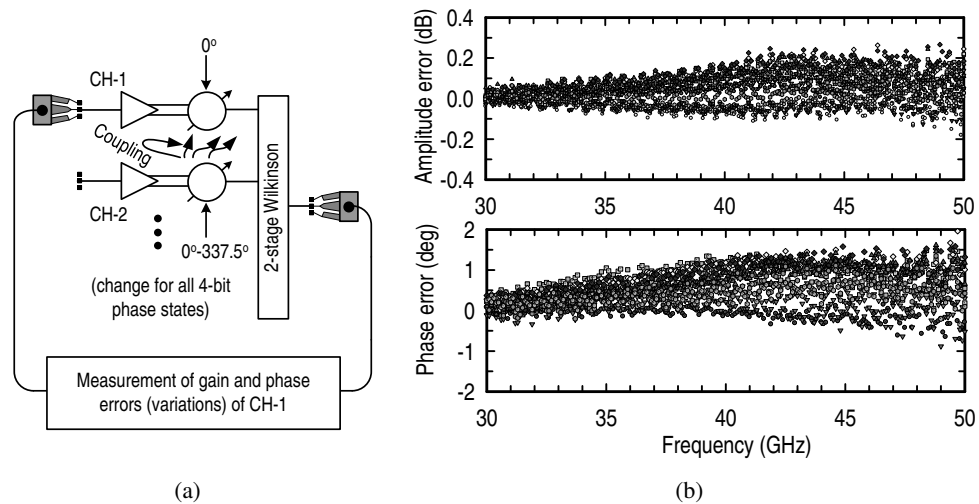
phase shifting is almost constant over 20-50 GHz [Figure 5.11 (*left*)]. The constant phase shift over very wideband is a fundamental aspect of the active phase shifter approach since the phase interpolation process (adding two orthogonal vectors) is basically independent of the operating frequency, as discussed in Chapter-3. The measured IIP<sub>3</sub> with the 0°-bit phase setting is -13.8 dBm and its variation is  $\pm 1.5$  dBm at 38.5 GHz for all 4-bit phase states [Figure 5.11 (*right*)].

## 5.5.2 Array Characterization

The mismatches (gain and phase mismatches) between the array elements are measured by comparing the 0°-bit (reference) S-parameters of all the 4 channels ( $S_{51}$ ,  $S_{52}$ ,  $S_{53}$  and  $S_{54}$ ). The phased-array shows a  $\leq 0.4$  dB of RMS gain variation and a  $\leq 2^\circ$  of RMS phase mismatch between the channels at 30-50 GHz [Figure 5.12 (*left*)]. This includes the variation between the different phase shifters and any amplitude and phase imbalance in the 2-stage



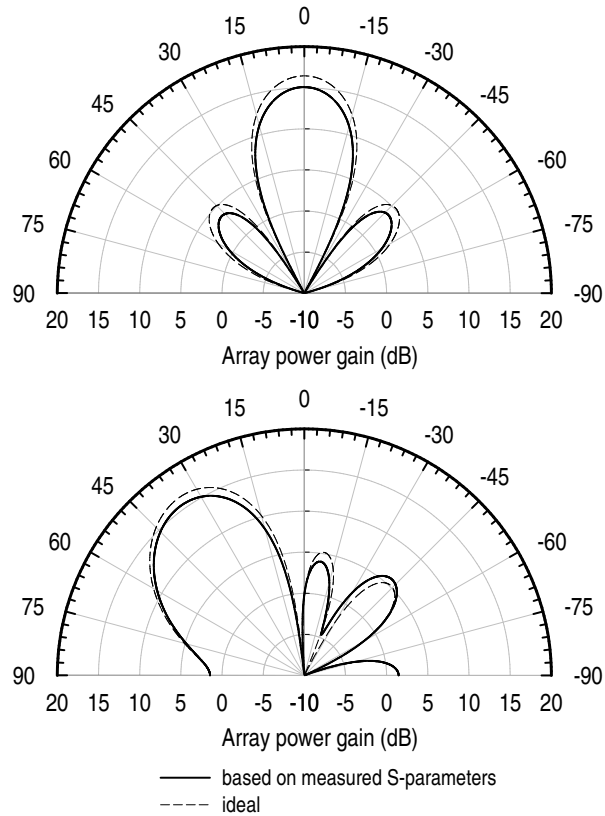
**Figure 5.12:** Measured channel-to-channel RMS mismatches (*left*), and measured channel-to-channel isolations (*right*).



**Figure 5.13:** Coupling characterization: (a) coupling test setup, (b) the measured peak-to-peak amplitude error (*upper*), and peak-to-peak phase error (*lower*).

Wilkinson combiner. A -35 dB measured worst case channel-to-channel isolation occurs between adjacent channels at 30-50 GHz [Figure 5.12 (*right*)].

Figure 5.13(a) shows the test set-up for measuring the errors due to the on-chip coupling in this study: the phase state of *Channel-1* is set as 0°-bit; the phase state of *Channel-2* is varied for all 16 phases; and the phase and amplitude variations of  $S_{51}$  are measured at the same time. Note that the input port impedance at *Channel-2* is set as an open circuit (not loaded with 50  $\Omega$ ) and this results in maximum voltage coupling at *Channel-2* and a worst-case condition for coupling [49]. The measured peak-to-peak phase error and peak-to-peak amplitude variation in  $S_{51}$  are  $-1 \sim 2^\circ$  and  $-0.2 \sim 0.3$  dB, respectively, at 30-50 GHz for all phase variations of *Channel-2*



**Figure 5.14:** Array beam scanning characteristics: broadside scan (*upper*) and 35° scan angle (*lower*) at 44 GHz.

(Figure 5.13(b)). The low coupling error is the result of combined efforts of symmetric differential design and high isolation layout by surrounding a ground plane around each array element, together with relatively high resistive substrate in the SiGe technology ( $\rho=8\sim 10 \Omega/\text{cm}$ ).

The phased-array pattern were constructed in ADS at 38.5 GHz using the measured 4-bit S-parameter sets of all the 4 channels under an assumption of standard linear array with uniform illumination (Figure 5.14). The 35° scan angle from broadside is obtained by applying a progressive phase shift of 103.2° ( $=360^\circ/\lambda \times d \times \sin 35^\circ$ ) per element for the ideal case and by applying digitized phase shifts to the nearest 4-bit phase states. The result is very close to the ideal case due to the low RMS gain error and phase mismatch between the 4 channels. The measured results are summarized in Table 5.1.

**Table 5.1:** Performance Summary of the Q-band 4-element phased-array receiver

Quantity	Results
Technology	0.18- $\mu\text{m}$ SiGe BiCMOS (Jazz SiGe120, 1P6M)
Frequency band	Q-Band (3-dB BW: 32.8-44 GHz)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	118 mA (29 mA per channel)
Chip area	1.4 $\times$ 1.7 mm <sup>2</sup>
Single Path Characteristics	
Input return loss	$\leq -8$ dB @ 32-50 GHz, $\leq -10$ dB @ 40-50 GHz
Output return loss	$\leq -8$ dB @ 32-50 GHz, $\leq -10$ dB @ 40-50 GHz
Channel power gain (ave)	10.4 dB @ 38.5 GHz
Phase resolution	4-bit
Gain error	$\leq 1.2$ dB (rms) @ 30-50 GHz
Phase error	$\leq 8.7^\circ$ (rms) @ 30-50 GHz
Input IP <sub>3</sub>	-13.8 dBm @ 38.5 GHz
NF	*12.4 dB @ 38.5 GHz
Group delay	85 $\pm$ 3 ps @ 30-45 GHz
Isolation (output-to-input)	$\leq -50$ dB @ 30-50 GHz
Array Characteristics	
Phase mismatch (rms)	$\leq 2^\circ$ @ 30-50 GHz (between all channels)
Amplitude mismatch (rms)	$\leq 0.4$ dB @ 30-50 GHz (between all channels)
Isolation (channel-to-channel)	$\leq -35$ dB @ 30-50 GHz (between all channels)
Array factor directivity	6 dB (4 elements)

## 5.6 Conclusions

In this chapter, a 4-element phased-array receiver is successfully demonstrated for Q-band applications. The phased-array is based on the *All-RF* architecture with 4-bit RF active phase shifters in a corporate-feed approach, and implemented using 0.18- $\mu\text{m}$  SiGe BiCMOS technology. In this design, Wilkinson couplers are compactly integrated in a meandering fashion using transmission-lines for the signal combiner. The measured loss of the Wilkinson couplers are very small ( $< 1$  dB) at 30-50 GHz, and impedance matching bandwidth is also pretty wide, leading to an excellent candidate for millimeter-wave phased-arrays. Also, in this chapter, the quadrature all-pass filter was successfully implemented at Q-band, and shows very accurate quadrature performance, validating its usefulness for millimeter-wave applications. The active phase shifter using the QAF shows very linear constant phase shift over 20-50 GHz with 5-bit phase accuracy. Measurement done on all 4 channels shows very low RMS phase and gain errors over the 4-bit phase states both in a single channel and also between the 4 different channels. These results suggest that the proposed phased-array architecture using active phase shifter can

be competitive for millimeter-wave applications. Since the area consumption of the active phase shifter is very small, it can provide high integration level of array element, and the next chapter shows a successful integration of 16 array elements on a single silicon chip at Q-band.

## 5.7 Acknowledgements

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- K.-J. Koh and G. M. Rebeiz, “A Q-Band 4-Element Phased-Array Front-End Receiver with Integrated Wilkinson Power Combiners in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 9, pp. 2046-2053, Sept. 2008.
- K.-J. Koh and G. M. Rebeiz, “A Q-Band Phased-Array Front-End with Integrated Wilkinson Couplers for Linear Power Combining,” *IEEE Bipolar Circuit and Tech. Meeting*, pp. 190-193, Oct. 2008.

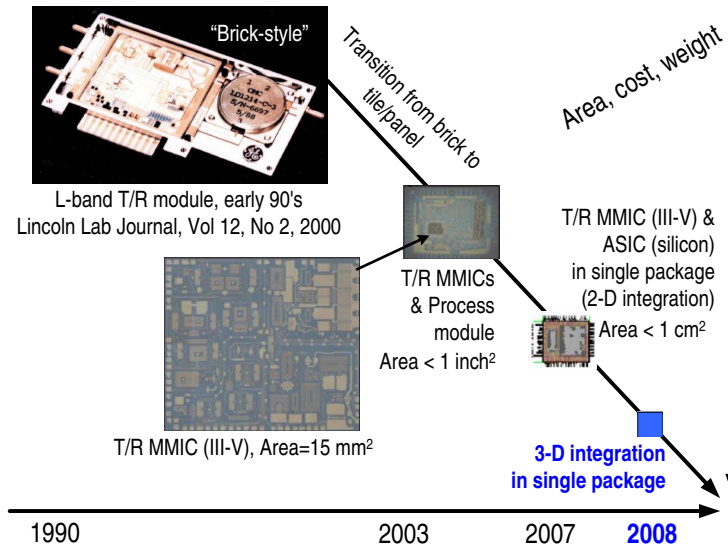
I would like to thank my coauthor Prof. Gabriel M. Rebeiz.

# 6

## **Millimeter-wave Phased-Array Design: II. Q-Band 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$ SiGe BiCMOS Technology**

### **6.1 Introduction**

Phased-array electronics have been developed with similar trend to commercial wireless telecommunication electronics. Figure 6.1 presents the evolution of phased-array electronics. Since monolithic circuits had not yet sufficiently matured, they had been realized with hybrid brick-style designs until early 1990s, where discrete packaged transistors, diode phase-shifters, switches and passive component were attached to a common ceramic substrate [17]. Recent brilliant advance in IC technology enabled for the phased-arrays to transit from the brick-style to tile-based integration, and typically III-V T/R MMICs were assembled with silicon-based process modules on a board level. To reduce system volume and cost further, in these days, the T/R MMICs are attempted to be integrated two-dimensionally with the control silicon ASIC in a single package [1, 2]. For the next generation of T/R modules, three-dimensional (3-D) integration of the T/R MMICs and control ASICs in a single chip will drastically reduce the size, cost and weight of the phased-array antenna module [72].



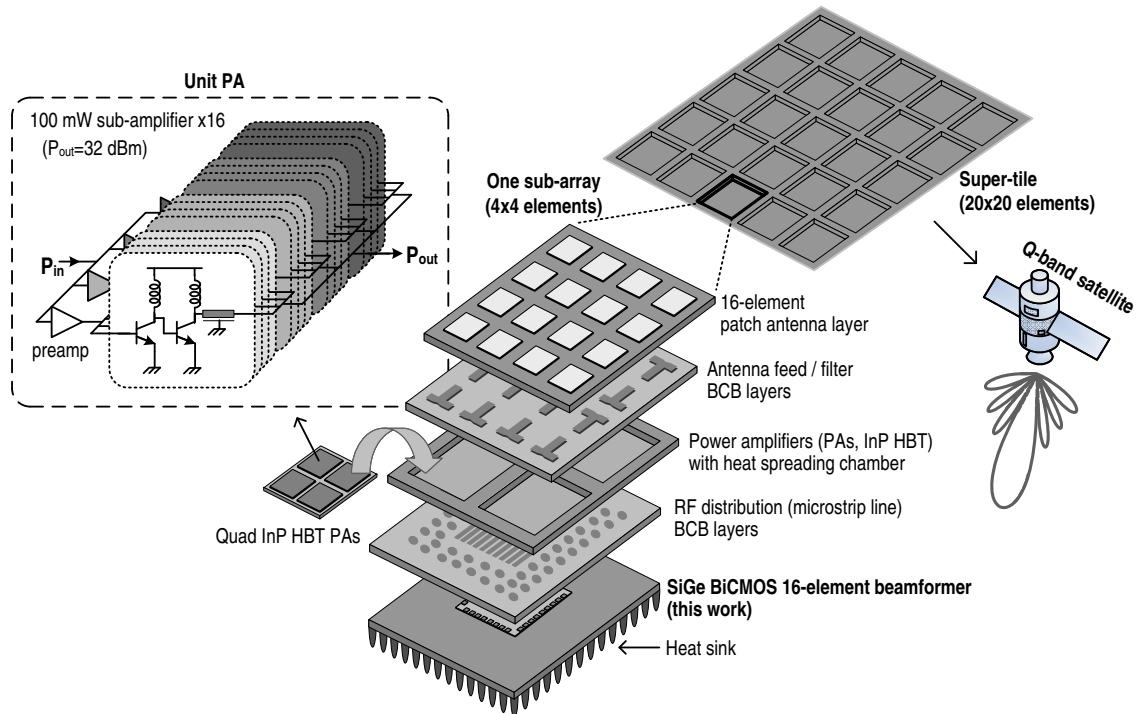
**Figure 6.1:** A technical direction for integrating phased-array electronics (excerpted from the presentation titled “*Reducing Cost, Size, & Mass of Radar components*” by COBHAM Defense Electronic Systems at 2007 *Multi-function Phased-Array Radar symposium*).

In this chapter, the die-scale (or wafer-scale) 3-D integration of millimeter-wave phased-array system is proposed in the next section, and 16-element phased-array transmitter (except for power amplifiers) is realized in a SiGe BiCMOS technology for Q-band satellite communications. In the architectural view, good scalability to large array is very important to increase integration level. In terms of scalability, phased-arrays based on the *All-RF* architecture and using RF phase shifters [73, 74] have a simple system architecture and results in a relatively straightforward extension to large array implementation. On the other hand, the mixer-based approach in [56] and [57], and the IF phase shifting scheme in [55] requires the same number of frequency conversion units as the number of array elements, requiring a complicated LO distribution network and limiting the scalability to large arrays. The 16-array transmitter is designed with 4-bit RF active phase shifters and the signal frequency band is 43-45 GHz, centered at the satellite communication frequency 44 GHz (bandwidth: 2 GHz, 4.5%).

## 6.2 Phased-Array System in 3-D Integration in a Single Package

Figure 6.2 illustrates the tile-based array construction, where the 16-element sub-array (called a “tile”) is assembled into the array (called a “super-tile”) in a layered tile configuration





**Figure 6.2:** A tile-based array architecture. One super-tile is composed of  $5 \times 5$  tiles (sub-arrays) and each tile contains 16 elements ( $4 \times 4$ ). Multi-layer integration allows the optimization of each layer in terms of thermal, mechanical and electrical performances.

and thus making a  $20 \times 20$  array [12, 75, 76]. Each tile utilizes batch-fabricated three-dimensional silicon micromachining technology [77] to integrate 16 patch antennas, 16 InP power amplifiers and SiGe BiCMOS beamforming transmitter in a multi-layered single package. The layer-level heterogeneous integration allows for choosing optimum process technologies for each functional layer and known-good-dies are stacked, resulting in high performance system in terms of yield and cost. A brief description of each functional layer is listed below.

A patch antenna with a micromachined air cavity provides high isolation (between each antenna element) and high efficiency (around 80-85 % at 44 GHz) with more than 10% bandwidth [77]. In the second layer, microstrip lines and slots are used for feeding the antenna, and a planar filter is also integrated as a part of the antenna feed. The required output power from the power amplifier (PA) is 1.5 W (for a  $50 \Omega$  load) with 30 % of PAE and 30 dB of power gain at 44 GHz, which is very challenging for silicon technology. Therefore, an InP double heterojunction bipolar transistor (D-HBT [75]) technology having high breakdown voltage of 9-10 V is chosen for the PA, and quad PAs are integrated together on a single die for easy assembly on a micromachined heat-spreading chamber as shown in Figure 6.2. Each PA is composed of

16 closely packed sub-amplifiers having a 20 dBm of maximum output power per unit sub-amplifier, and the overall parallel-combined output power is 32 dBm per PA. For maximum output power, high current density in the HBT is inevitable, leading to about 3.5 kW/cm<sup>2</sup> of localized dissipation power density in the InP HBT cell at the PAs. Therefore, a careful thermal management is essential to prevent the thermal hazard. In Figure 6.2, the micromachined cellular cavity chambers provide an excellent thermal conductivity and spread heat, and thermal vias (heat pipes having the matched thermal expansion coefficient of 1 W/cm<sup>2</sup>-K) are used to drain the thermal vapor to the bottom heat sink. These maintain below 150°C of junction temperature in the HBTs. The various transmission lines with an order of  $\lambda/4$  are involved in the PA for impedance matching and power combining network. To minimize the transmission line loss, low dielectric BCB layers ( $\epsilon_r=2.7$ ,  $\tan \delta=0.002$ ) are chosen for interconnects and this results in about 0.4 dB/ $\lambda$  of attenuation at 44 GHz [78]. Finally, the SiGe BiCMOS beamformer (16-element transmitter IC), the main focus in this chapter, allows the precision 4-bit digital phase control for the 16 patch antenna elements. The maximum saturated output power required per element from the beamformer is -3~0 dBm which is enough to drive the InP PA module.

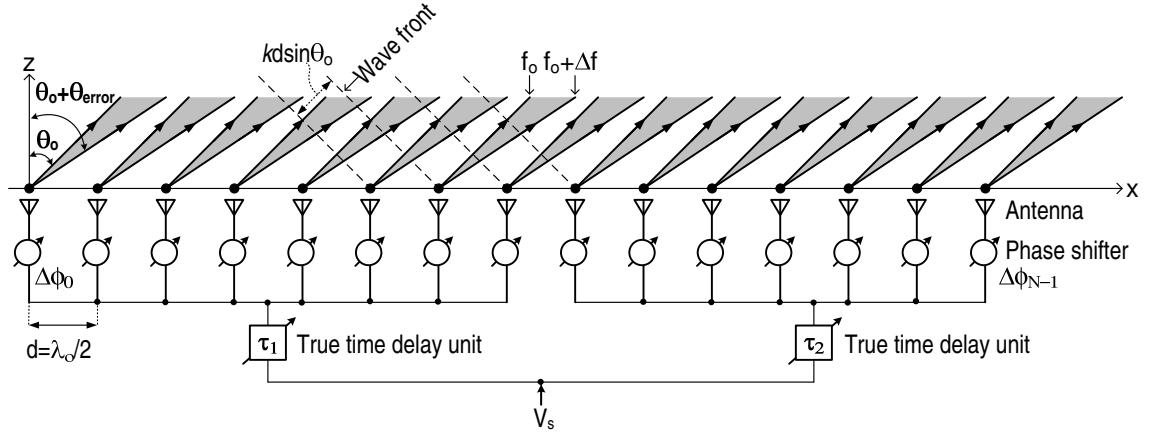
### 6.3 Bandwidth Limitations in Large On-Chip Phased-Arrays (Revisited)

While larger phased-arrays can provide better sensitivity and selectivity of a signal at the spatial domain, they usually suffer from bandwidth limitation and there exists a maximum allowable bandwidth for a given array size. To investigate this, let's consider the 16-element phased-array shown in Figure 6.3, with an inter-element spacing of  $d=0.5\lambda_o$  at the center frequency ( $f_o$ ).  $\lambda_o (=c/f_o, c=light\ speed)$  is the signal wavelength, and  $\theta_o$  is the beam steering angle. The input signal,  $V_s$  given in (6.1), has a finite frequency allocation of  $f_o \pm \Delta f$  (bandwidth,  $f_{BW}=2\Delta f$ ), and the phase delay  $\Delta\phi_n$  per element is given in (6.2).

$$V_s = A \sin 2\pi (f_o + \Delta f) t = A \sin 2\pi f_o \left( 1 + \frac{\Delta f}{f_o} \right) t. \quad (6.1)$$

$$\Delta\phi_n = n2\pi f_o \left( 1 + \frac{\Delta f}{f_o} \right) \Delta\tau = nkd \sin \theta_o \left( 1 + \frac{\Delta f}{f_o} \right) \quad (6.2)$$

where  $n=0, 1, 2, \dots, N-1$  ( $N=16$ , total number of array elements),  $k=2\pi/\lambda_o$ , and  $\Delta\tau=d\sin\theta_o/c$  is the time-delay difference between two adjacent elements. The phase distribution ( $\Delta\phi_0, \Delta\phi_1,$



**Figure 6.3:** 16-element phased-array with a combination of phase shifters at the element level and true time delay (TTD) units at the sub-array level for wideband operation ( $N=16$ ).

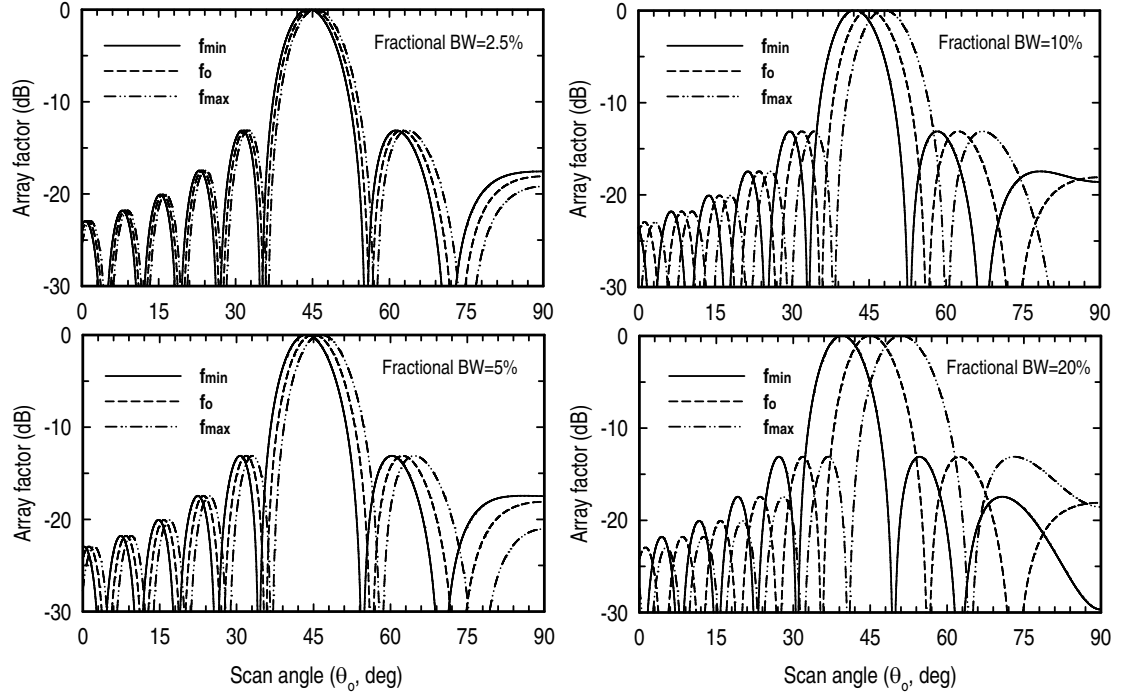
...,  $\Delta\phi_{N-1}$ ) must be linear over the entire array both in frequency and in space domain to ensure perfect true-time-delay (TTD) operation of the phased-array. This guarantees that the output signals from all the array elements are in phase (or congruent in time) in the  $\theta_o$  direction [7,9,23]. However, due to on-chip area limitation, the phase shift is not only constant versus frequency but also covers only 0-360° [33, 74]. The phase shifting value per element is therefore chosen at  $f_o$  and is given in (6.3). This results in a phase quantization error,  $\Delta\phi_{error,n}$  which is expressed as (6.4), at  $f_o \pm \Delta f$  across the array.

$$\Delta\phi_{o,n} = |nkd \sin \theta_o - \text{modulus}(2\pi)|. \quad (6.3)$$

$$\begin{aligned} \Delta\phi_{error,n} &= |\Delta\phi_n - \Delta\phi_{o,n}| \\ &= \left| nkd \sin \theta_o \frac{\Delta f}{f_o} - \text{modulus}(2\pi) \right|. \end{aligned} \quad (6.4)$$

The  $\Delta\phi_{error,n}$  causes a beam pointing error versus frequency,  $\theta_{error}$  in Figure 6.3, where the beam points in slightly different directions at different frequencies (see [7] for more details). References [9] and [8] suggest that the  $\theta_{error}$  should be less than half of the 3-dB beamwidth, and this results in the maximum allowable bandwidth for a given array size as expressed in (6.5) where  $Nd$  is the total length ( $L$ ) of the array.

$$\frac{f_{BW}}{f_o} \leq 0.886 \frac{\lambda_o}{Nd \sin \theta_o}. \quad (6.5)$$



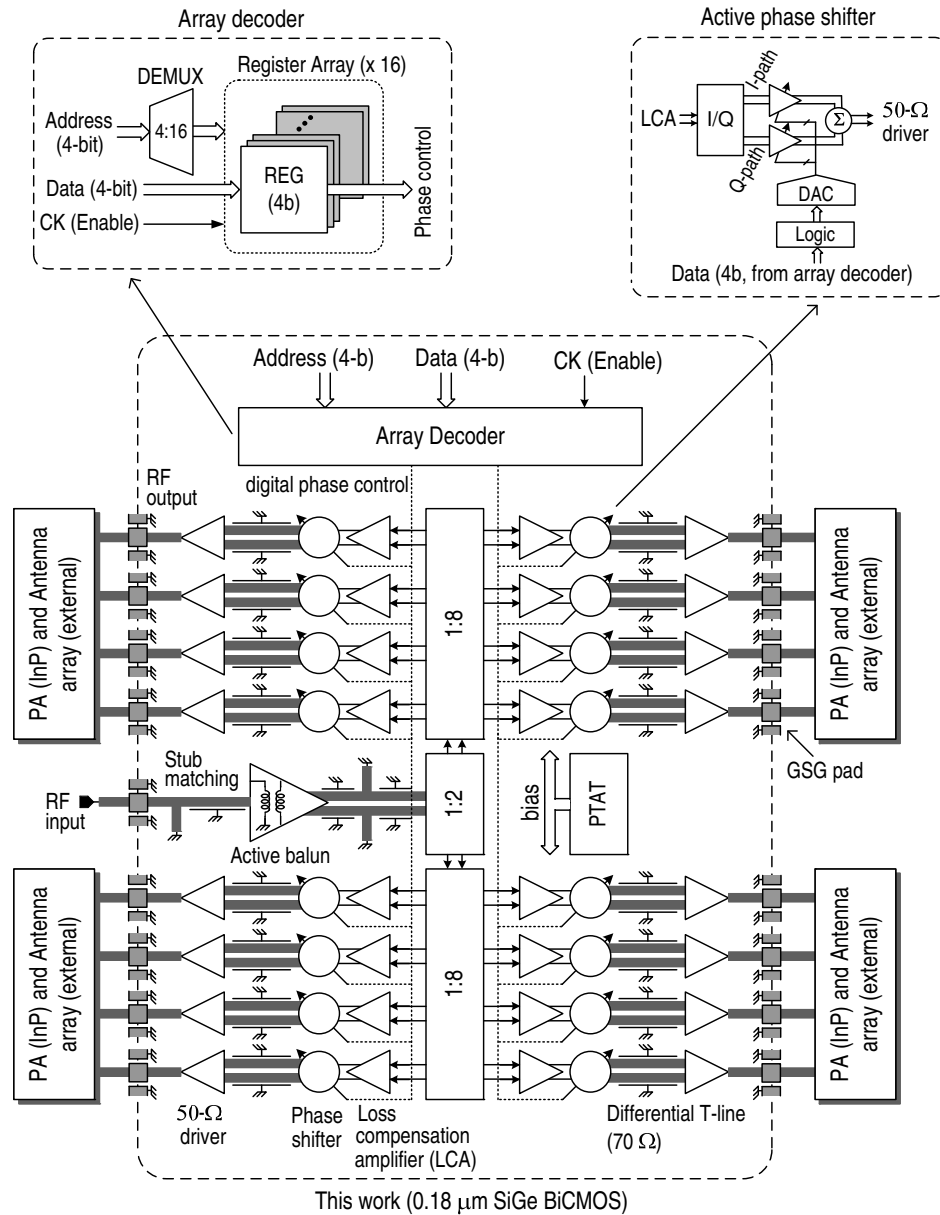
**Figure 6.4:** Array factors for a 16-element linear phased-array for different fractional bandwidths (scan angle= $45^\circ$ ).

It is seen that if the array does not scan ( $\theta_0=0^\circ$ ), then an infinite bandwidth can be tolerated. However, for a phased-array with a length  $L$  and  $\theta_0$  scan angle, the 3-dB bandwidth is proportional to  $1/(L\sin\theta_0)$  for constant  $0-360^\circ$  phase shifters.

Figure 6.4 presents the array factor for a uniformly-fed linear 16-element array scanned to  $\theta_0=45^\circ$  ( $\Delta\phi_{o,n}=n\pi\sin\theta_0\simeq n\times 127.3^\circ$ ) and a fractional bandwidth ( $f_{BW}/f_0$ ) of 2.5%, 5%, 10% and 20% [23]. The beams are squinted especially at the upper and lower bandwidth frequencies ( $f_{min}$  and  $f_{max}$ ) due to the non-optimal phase delays: for example, for a 10% fractional bandwidth system, the main beam from the 16-element array is diverted by  $\theta_{error}\simeq \pm 3^\circ$  from  $45^\circ$  at the band edges, and results in 1.13 dB of pattern loss at the  $45^\circ$  scan angle for  $f_{min}$  and  $f_{max}$ . The  $f_{BW}$  is proportional to  $1/N$ , and an 8- or 4-element array can tolerate 2 or 4 times larger bandwidth than a 16-element array. Therefore, one can conclude from Figure 6.4 that on-chip phased-arrays with  $0-360^\circ$  phase shifters can drive  $4\times 4$  or even  $8\times 8$  elements with virtually no penalty for a system with up to 10% bandwidth.

As a final note, TTD units are imperative at the sub-array level to cover more than 10% bandwidth for  $8\times 8$  arrays (Figure 6.3). In this case, the TDD units must result in a phase

difference of  $8 \times \Delta\phi$  (center-to-center at the 8-element level,  $\Delta\phi$ =phase difference between adjacent elements). These TTD units are based on switched transmission lines in low dielectric constant substrates and are quite large due to the large required phase shift [79]. However, only one of them is needed for every  $8 \times 8$  elements [9].



**Figure 6.5:** The functional block of the 16-element phased-array beamformer in 0.18- $\mu\text{m}$  SiGe BiCMOS technology.

## 6.4 16-Element Phased-Array Transmitter Architecture

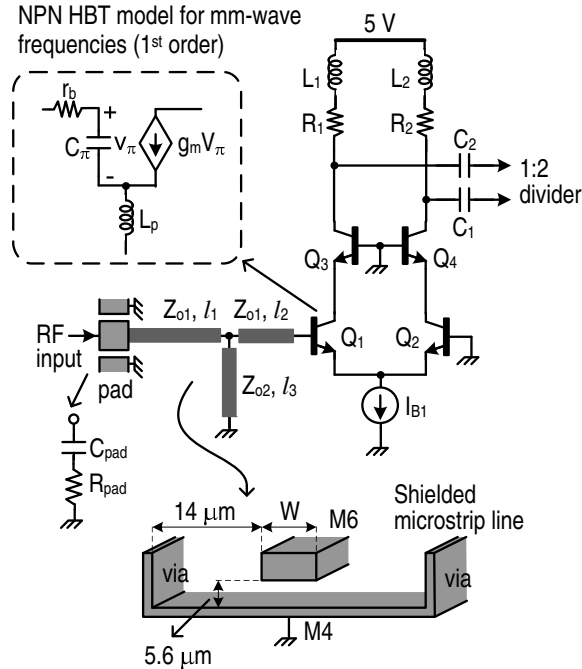
Figure 6.5 presents the functional blocks of the 16-element phased-array transmitter based on the corporate-feed approach with active RF phase shifters. The RF input signal is transformed into a balanced signal using an active balun, and the input and output of the balun amplifier are matched to  $50\ \Omega$  with inductive transmission line stubs. The 1:16 signal divider constitutes the core part of the corporate-feed network, and is realized using a combination of active (1:2) and passive (1:8) designs for a compromise between loss, linearity and power consumption. To minimize area, the 1:8 passive dividers are realized with perfectly shielded differential transmission lines (similar to a coaxial line configuration) which are detailed in the next section.

After the dividers, each array element is composed of a loss-compensation amplifier (LCA), a 4-bit phase shifter and a  $50\text{-}\Omega$  driver. The LCA compensates for the 9 dB of power division loss from the 1:8 passive divider and drives an I/Q network inside the phase shifter. The active phase shifter is based on a phase interpolation technique where differential I/Q signals are added with appropriate weights to generate necessary phase, and a DAC controls the amplitude weights for 4-bit phase quantization [33]. The phase shifters are controlled independently using 4-bit digital data input from an array decoder. The array decoder is composed of a 4-to-16 address decoder and 4-bit register cells ( $\times 16$ ) are used to access each array element [74]. Finally a  $50\text{-}\Omega$  driver converts the differential signal into a single-ended one and drives the transmission lines in the BCB layer with wideband  $50\ \Omega$  matching (see Figure 6.2). The transmitter chip is followed by high-efficiency external InP PAs and microstrip antennas built using interconnection BCB layers.

## 6.5 Functional Block Design

### 6.5.1 Active Balun Amplifier

A differential system is more robust to parasitic coupling than a single-ended one for high frequency applications. In this design, the balun function is realized using a standard differential amplifier with emitter coupling by grounding one of the differential inputs (Figure 6.6). At millimeter-wave frequencies ( $> 30$  GHz), a small parasitic layout inductance can cause a moderate reactive impedance. For instance, when a line length,  $l$ , is much shorter than the



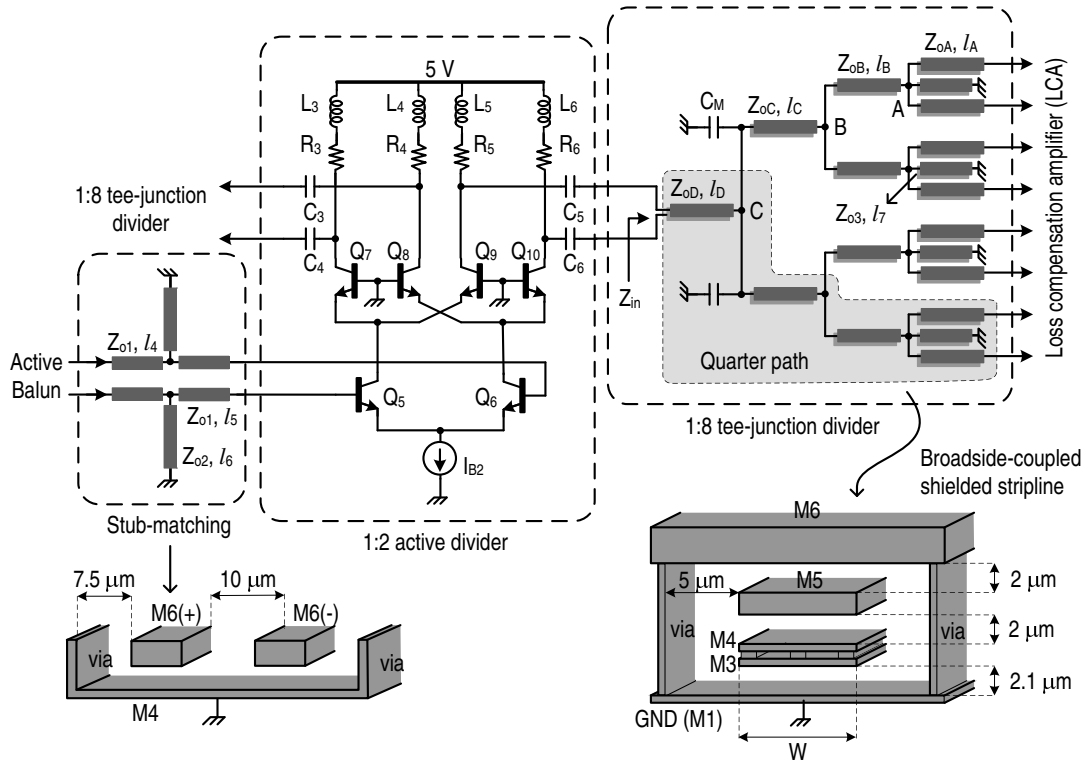
**Figure 6.6:** The active balun amplifier, microstrip line structure (not to scale) and small signal NPN HBT model which includes an inductance,  $L_p$ , to account for parasitic layout inductance for this work.

wave length,  $\lambda$ , the line inductance can be approximated by (6.6) where  $Z_o$  is the characteristic impedance of the line. Typical values of  $Z_o=100 \Omega$  and  $l=100 \mu\text{m}$  ( $\approx \lambda/42$  at 44 GHz,  $\text{SiO}_2$   $\epsilon_r=4.2$ ) results in  $L \approx 68 \text{ pH}$  corresponding to  $j19 \Omega$  at 44 GHz, which is comparable to the  $1/g_m$  of an HBT biased at  $> 1 \text{ mA}$ . When present at the emitter side, this parasitic reactance lowers the gain and increases linearity a bit.

$$L = \frac{Z_o \tan(\beta l)}{\omega} \approx \frac{Z_o \beta l}{\omega} = \frac{Z_o \sqrt{\epsilon_r}}{c} l, \text{ where } \beta = \frac{2\pi}{\lambda}. \quad (6.6)$$

To account for the parasitic layout inductance, the 1<sup>st</sup>-order small-signal model includes an inductor,  $L_p$  in Fig. 6.6, and this inductance is extracted from full-wave electro-magnetic (EM) simulations using Sonnet [71].

The input port is matched to  $50 \Omega$  at 39-60 GHz ( $S_{11} < -10 \text{ dB}$ ) using short transmission lines ( $Z_{o1}=50 \Omega$ ,  $l_1=390 \mu\text{m}$  and  $l_2=230 \mu\text{m}$ ) and a grounded inductive matching stub ( $Z_{o2}=75 \Omega$ ,  $l_3=380 \mu\text{m}$ ,  $L_{eff}=190 \text{ pH}$ ,  $Q=13.2$  @ 45 GHz). The transmission lines and inductive stubs are realized using shielded microstrip-mode lines. Typical line widths,  $W$  in Figure 6.6, are  $8 \mu\text{m}$  and  $4 \mu\text{m}$  for the  $50 \Omega$  and  $75 \Omega$  lines, respectively. The input transistors ( $Q_{1,2}$ ) are biased



**Figure 6.7:** The 1:2 active divider, differential microstrip line structure (not to scale), 1:8 passive tee-junction dividers (only one is shown) and broadside-coupled stripline structure (scaled, M5 thickness:  $1.6 \mu\text{m}$ , thickness of M4 and M3 with vias:  $1.9 \mu\text{m}$ ).

with  $2.5 \text{ mA}$  ( $I_{B1}=5 \text{ mA}$ ) to achieve a peak  $f_t$  of  $150 \text{ GHz}$ . The emitter lengths ( $l_E$ ) of  $Q_{1,2}$  and  $Q_{3,4}$  are  $5.1 \mu\text{m}$  and  $3.4 \mu\text{m}$ , respectively (emitter width= $0.2 \mu\text{m}$ ). The output is matched to  $100 \Omega$  differentially with  $L_{1,2}=200 \text{ pH}$  ( $Q=16$  @  $45 \text{ GHz}$ ) and  $C_{1,2}=33.6 \text{ fF}$ , and  $R_{1,2}=25 \Omega$  of series resistance is used for lowering  $Q$  and extending gain bandwidth. All the RF pads are modeled as S-parameters using EM simulation (nominal model:  $C_{pad}=30.8 \text{ fF}$  and  $R_{pad}=260 \Omega$ ). The voltage gain from the single-ended input to the differential output is  $6 \text{ dB}$  at  $45 \text{ GHz}$  and the 3-dB gain bandwidth is  $30\text{-}57 \text{ GHz}$  in SPECTRE simulation. The differential gain mismatch is  $2 \text{ dB}$  and the phase imbalance is  $2.7\text{-}4.4^\circ$  at  $40\text{-}50 \text{ GHz}$ .

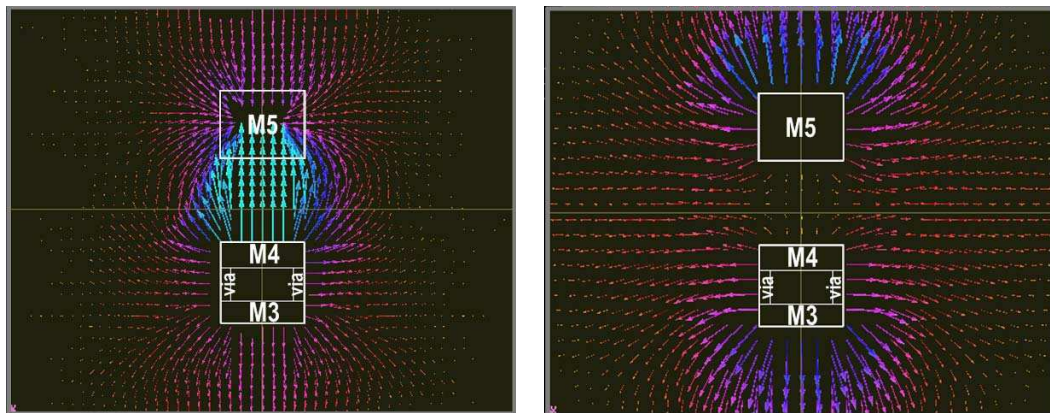
### 6.5.2 Corporate-Feed Network

Fig. 6.7 presents details of the 1:16 signal feed network composed of a 1:2 active divider and two 1:8 passive tee-junction dividers.

*Active 1:2 Divider:* The active divider provides additional common-mode rejection, correcting the differential errors from the active balun. The RF input signal is divided into two

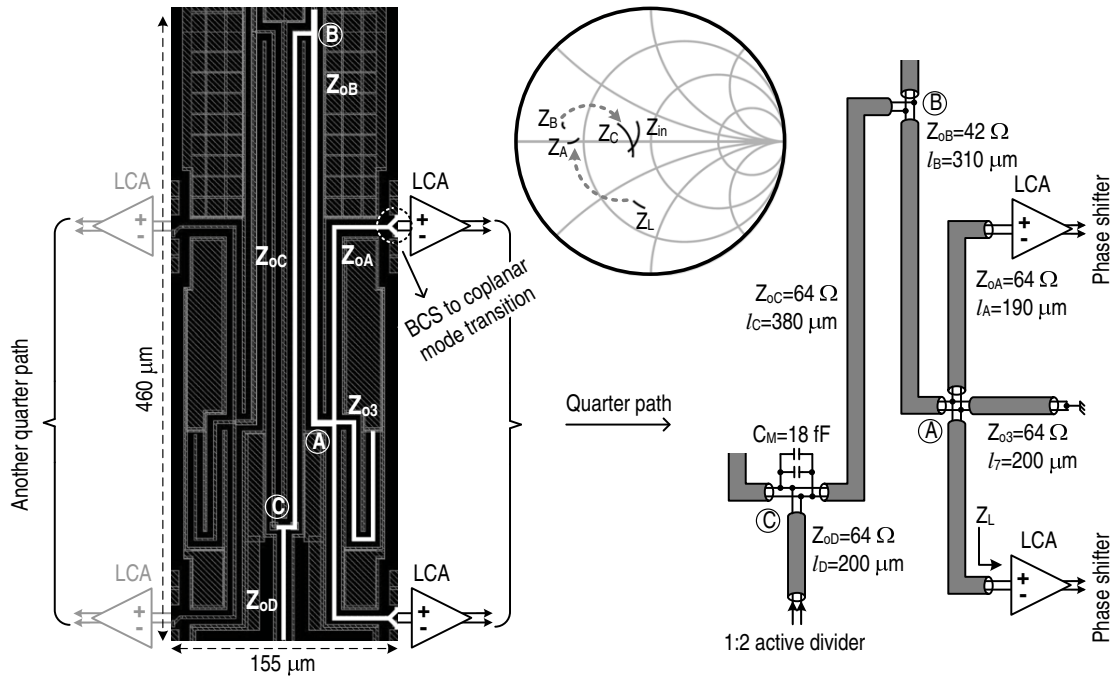


in the current domain at the cascode nodes ( $l_E$  of  $Q_{7-10}=3.4 \mu\text{m}$ ). The input of  $Q_{5,6}$  ( $l_E=10.7 \mu\text{m}$ ) is matched to differential  $100 \Omega$  using shielded microstrip-mode differential transmission lines ( $l_4=300 \mu\text{m}$  and  $l_5=98 \mu\text{m}$ ) and inductive stubs ( $l_6=300 \mu\text{m}$ ,  $L_{eff}=145 \text{ pH}$ ,  $Q=14.1 @ 45 \text{ GHz}$ ). Typical line width for the differential line is  $7 \mu\text{m}$  for a differential mode  $50 \Omega$ . To simplify the design of the passive dividers, the output of the active divider is also matched to  $100 \Omega$  differentially with  $L_{3-6}=200 \text{ pH}$  ( $Q=16 @ 45 \text{ GHz}$ ) and  $C_{3-6}=29 \text{ fF}$ . A  $R_{3-6}=15 \Omega$  increases the match bandwidth. The voltage gain of the active divider is  $12 \text{ dB}$  at  $45 \text{ GHz}$  for  $I_{B2}=15 \text{ mA}$  and the  $3\text{-dB}$  gain bandwidth is  $38.5\text{-}52.3 \text{ GHz}$ . All the layout parasitics are extracted as S-parameters using Sonnet and included in the SPECTRE simulations.



**Figure 6.8:** Electrical field distributions of the BCS-line from 3-D EM simulation (HFSS): differential mode (left) and common mode(right) field distributions.  $W=2 \mu\text{m}$  was chosen for the simulation.

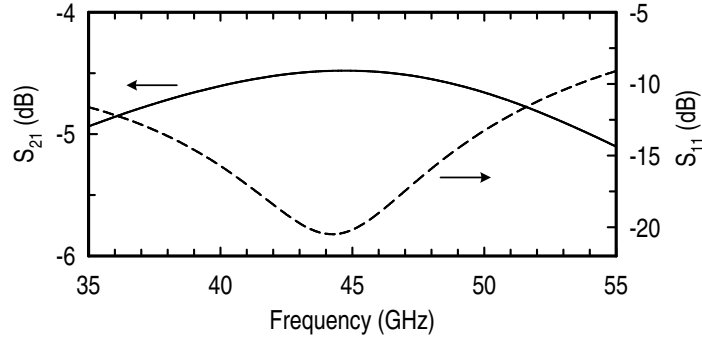
*Passive 1:8 Tee-Junction Dividers:* The passive dividers in Figure 6.7 utilizes the 3-dimensional metal stack structure to realize compact and tightly coupled differential transmission lines, called broadside-coupled shielded striplines (BCS-lines) [80,81]. Theoretical analysis and measured performance of the BCS-lines are presented in [81]. The M5 thickness is  $1.6 \mu\text{m}$  in the BCS-line structure in Figure 6.7, and to minimize geometrical asymmetry, M3 and M4 are connected together with via resulting in an equivalent thickness of  $1.9 \mu\text{m}$ . A distance of  $5 \mu\text{m}$  between the signal lines and the shielding via was found to be adequate using EM simulations, resulting in a total BCS-line width of  $15 \mu\text{m}$  (for  $W=3 \mu\text{m}$  in Figure 6.7) and this is much less horizontal space than typical coplanar waveguide (CPW) lines. Figure 6.8 presents the simulated electrical field distributions from HFSS [82] at  $45 \text{ GHz}$ . The differential-mode excitation exhibits tight coupling between the signal lines, while the common-mode field distribution



**Figure 6.9:** The layout of the quarter path shown in Figure 6.7 and its detailed description (all impedances are odd-mode impedances). The frequency range of the impedances in the Smith chart ( $Z_o=100 \Omega$ ) is 40-50 GHz.

shows negligible coupling between the differential signal lines. The line impedance can be set by the line width  $W$ . Typical differential mode characteristic impedances are  $42\text{--}64 \Omega$  for  $W=2\text{--}4 \mu\text{m}$ , and the measured loss is about  $3\text{--}3.5 \text{ dB}/0.5 \text{ mm}$  for a  $64 \Omega$  line at  $45 \text{ GHz}$  and is due to finite ohmic resistance of the signal lines [81]. The fundamental merit of the BCS structure is that the shielded ground plane surrounding the differential signal lines allows excellent line-to-line isolation in a very compact structure. This makes possible to integrate the  $1:8$  tee-junction divider in a small area (see Figure 6.13).

The layout details of the passive divider are presented in Figure 6.9 where only a quarter path is illustrated for simplicity. The Smith chart shows impedances at the junction points of the divider. The loading impedance ( $Z_L$ ) from the LCA input is  $Z_L=55\text{--}j65 \Omega$  at  $45 \text{ GHz}$ . The capacitive reactance of  $Z_L$  is tuned out using a BCS-line ( $Z_{oA}=64 \Omega$ ,  $l_A=190 \mu\text{m}$ ) in parallel with an inductive stub ( $L_{eff}=260 \text{ pH}$  @  $45 \text{ GHz}$ ,  $Z_{o3}=64 \Omega$ ,  $l_7=200 \mu\text{m}$ ). With two of these BCS-lines in parallel, the odd-mode characteristic impedances at node A is  $Z_A \approx 40 \Omega$  ( $Z_{oB}=42 \Omega$ ,  $l_B=310 \mu\text{m}$ ). The impedance seen at node B, then, is  $Z_B \approx 20 \Omega$ , and is matched to  $Z_C \approx 71 \Omega$  at node C using a BCS-line ( $Z_{oC}=64 \Omega$ ,  $l_C=380 \mu\text{m}$ ) followed by a shunt capacitor ( $C_M=18$

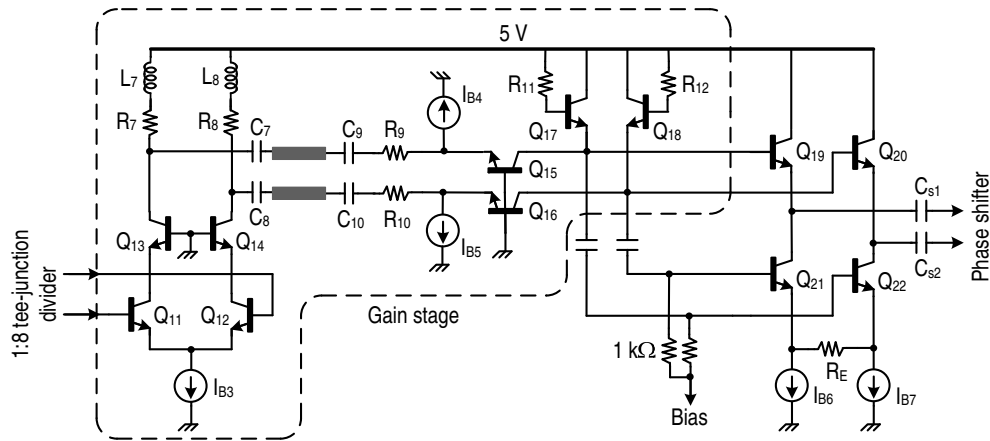


**Figure 6.10:** The simulated  $S_{21}$  and input reflection coefficient ( $S_{11}$ ) of the passive 1:8 tee-junction divider. Input port impedance= $100 \Omega$  and output load impedance= $55-j65 \Omega$  at 45 GHz. The  $S_{21}$  does not include the 9 dB 1:8 splitter loss. (Port-1: input port, Port-2: one of the 8 output ports).

fF). After another BCS-line section of  $Z_{oD}=64 \Omega$  and  $l_D=200 \mu\text{m}$ , the final input impedance is  $Z_{in}=83 \Omega$  at 45 GHz and this results in less than -15 dB input return loss at 39-49 GHz for a  $100 \Omega$  source impedance (Fig. 6.10). The output return loss is  $\leq -10$  dB at 30-53 GHz for the load impedance of  $Z_L$ . The estimated power loss in the 1:8 passive divider is 4.5-4.8 dB per path above the ideal 9 dB power split loss at 40-50 GHz (Figure 6.10). The entire passive 1:8 divider occupies an area of only  $0.15 \times 1.05 \text{ mm}^2$ .

### 6.5.3 Array Element Design

*Loss Compensation Amplifier (LCA):* The LCA compensates the power loss from the passive power dividers (Figure 6.11). The inductively-loaded common-emitter (CE) stage provides a peak voltage gain of 9 dB at 46 GHz with a DC current of  $I_{B3}=10 \text{ mA}$  ( $l_E$  of  $Q_{11,12}=8 \mu\text{m}$  and  $l_E$  of  $Q_{13,14}=5.3 \mu\text{m}$ ), and the common-base (CB) stage contributes another 3 dB gain for  $I_{B4}=I_{B5}=2 \text{ mA}$  ( $l_E$  of  $Q_{15,16}=3.4 \mu\text{m}$ ). A low impedance is better for stable operation under finite node parasitics at high frequencies. Therefore, the CE and CB interstage impedance is chosen to be  $50 \Omega$  (differentially  $100 \Omega$ ):  $L_{7,8}=200 \text{ pH}$ ,  $C_{7,8}=33.6 \text{ fF}$ ,  $R_{7,8}=12.5 \Omega$ ,  $C_{9,10}=100 \text{ fF}$  and  $R_{9,10}=12 \Omega$ . The size of the active inductor loads composed of  $Q_{17,18}$  ( $l_E=3.4 \mu\text{m}$ ) and  $R_{11,12}$  ( $124 \Omega$ ) are optimized to have a peak gain at around 40-41 GHz, resulting in a 36.5-49 GHz of 3-dB gain bandwidth in the gain stage. The output LCA stage is a low-impedance driver and designed with the same manner as in Figure 5.6 in Chapter-5. The emitter length of  $Q_{19-22}$  is  $l_E=3.4 \mu\text{m}$ . An  $R_E=25 \Omega$  is chosen for better 3<sup>rd</sup>-order linearity.  $C_d$  (0.5 pF) and  $C_{s1,2}$  (50 fF)

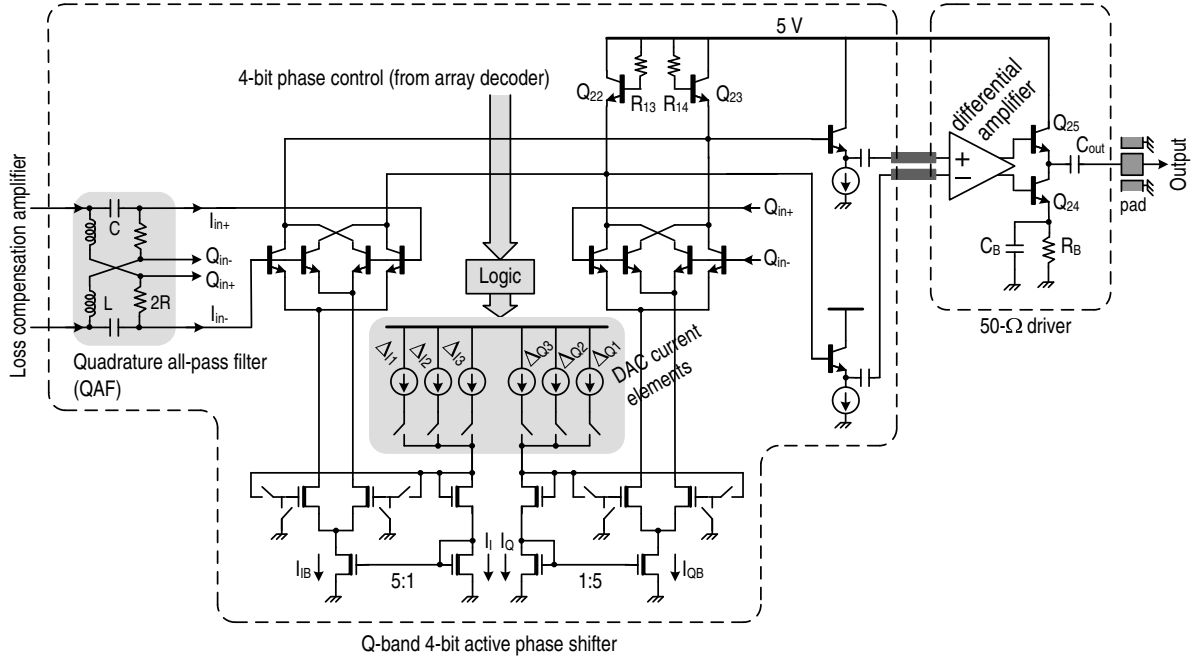


**Figure 6.11:** The loss compensation amplifier (LCA) composed of gain stage (common emitter and common base stage) and an output low-impedance driver for the following phase shifter.

are DC blocking capacitors and  $C_{s1,2}$  also resonates out the parasitic active inductance caused by the emitter followers,  $Q_{19,20}$ . The output driver consumes 6 mA of DC current ( $I_{B6}=I_{B7}=3$  mA) with unity voltage gain for a  $32 \Omega$  load.

*4-Bit Active Phase Shifter:* The active phase shifter is realized in the same manner as in Figure 5.7 in Chapter 5 (Figure 6.12). A low impedance of  $\sqrt{L/C}=27 \Omega$  is chosen for QAF to increase the I/Q phase accuracy under about 70 fF of loading capacitance ( $L=93.4$  pH,  $C=125.4$  fF and  $2R=62.5 \Omega$ ), resulting in  $\leq 3^\circ$  of I/Q phase error at 37-48 GHz in the QAF. Two separate current-scaled DACs are integrated and control  $I_{IB}$  and  $I_{QB}$  independently, which enables to optimize the I- and Q-path gain according to the I/Q amplitude mismatch in the QAF. The sizes of DAC current sources ( $\Delta_{I1-3}$  and  $\Delta_{Q1-3}$ ) are optimized using SPECTRE to achieve 4-bit phase accuracy with less than  $\pm 1.5$  gain variations for all 4-bit phase states. The current consumption in the phase shifter including the buffer is 8 mA, and the size of the active inductor composed of  $Q_{22,23}$  ( $I_E=3.4 \mu\text{m}$ ) and  $R_{13,14}$  ( $125 \Omega$ ) is set to have a 2-3 dB voltage gain at 39-46 GHz.

*50- $\Omega$  Driver:* The 50- $\Omega$  driver in Figure 6.12 compensates about 3 dB of line loss to the external InP PA. A standard differential amplifier with resistive emitter-degeneration is first used and provides 3-4 dB voltage gain at 39-53 GHz for a bias current of 10 mA [83]. The NPN-based push-pull output stage ( $Q_{24,25}$ ,  $I_E=3.4 \mu\text{m}$ ) converts the differential input to a single-ended one and drives the external 50  $\Omega$  transmission line at the expense of 6 dB loss for impedance matching [74]. A 3 mA of bias current sets the matching impedance and the output



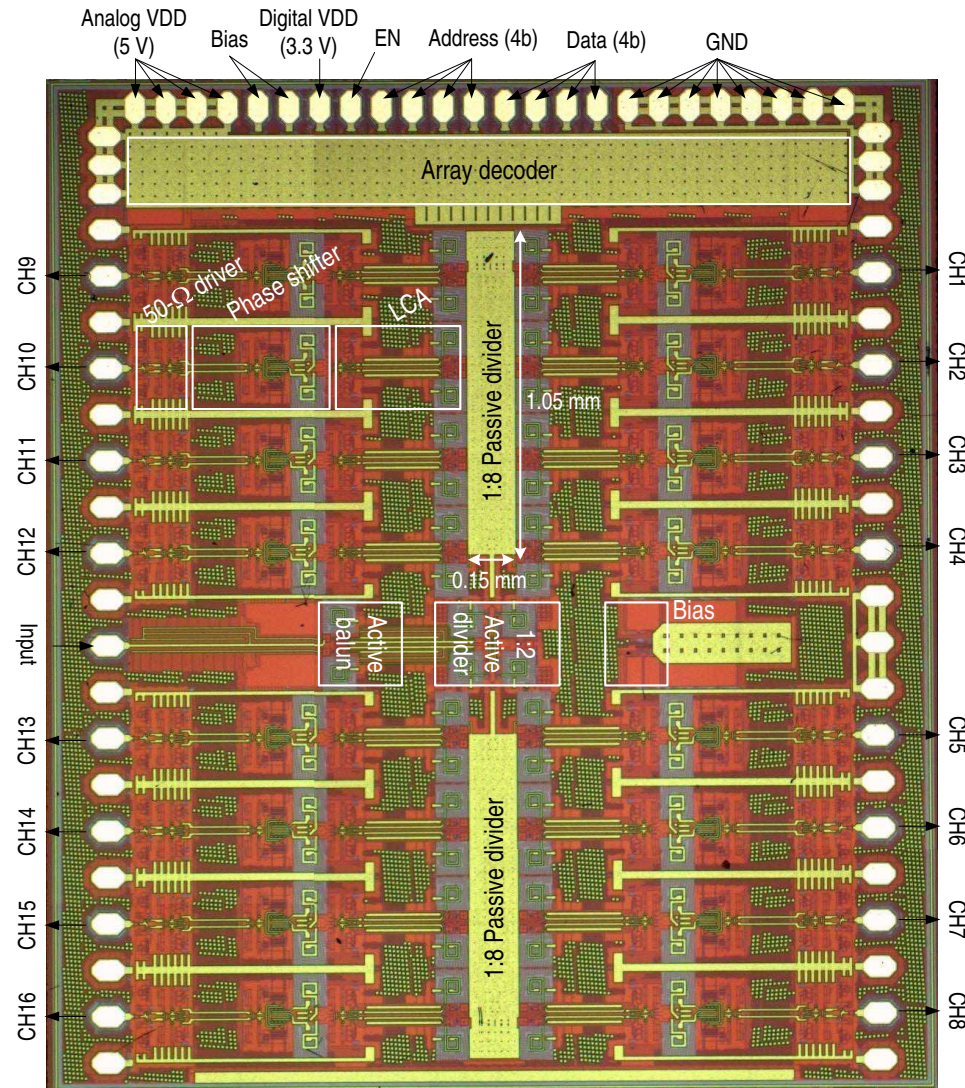
**Figure 6.12:** The active 4-bit RF phase shifter and 50- $\Omega$  output driver.

return loss is  $\leq -10$  dB @ 36-53.5 GHz in simulation including the pad parasitics.  $R_B$  (50  $\Omega$ ) and  $C_B$  (100 fF) are used for biasing and AC bypassing, respectively. The output DC blocking capacitor ( $C_{out}=60$  fF) is also used for compensating a finite active inductance caused by  $Q_{25}$  at the design frequencies.

## 6.6 Measured Results And Discussion

The phased-array transmitter is realized in a 0.18  $\mu\text{m}$  SiGe BiCMOS process (1P6M, SiGe HBT  $f_t \simeq 150$  GHz) and the chip microphotograph is shown in Figure 6.13. The overall chip size is  $2.6 \times 3.2$  mm<sup>2</sup>. The electrical distances between the input port and all output channels are virtually identical due to the corporate-feed layout. A ground barrier (grounded via stack from substrate to top metal) is placed between channels to reduce parasitic substrate coupling among adjacent channels. The total current consumption is 720 mA (which is referenced to an internal PTAT source) from a 5 V supply voltage, and agrees well with simulation. Several DC pads are tied together for the supply and ground pads to satisfy the current density requirement. The DC current is divided as 5 mA for the active balun, 15 mA for the 1:2 active divider and 44 mA ( $\times 16$ ) for each array element. The digital logic uses a 3.3 V of separate supply voltage. The



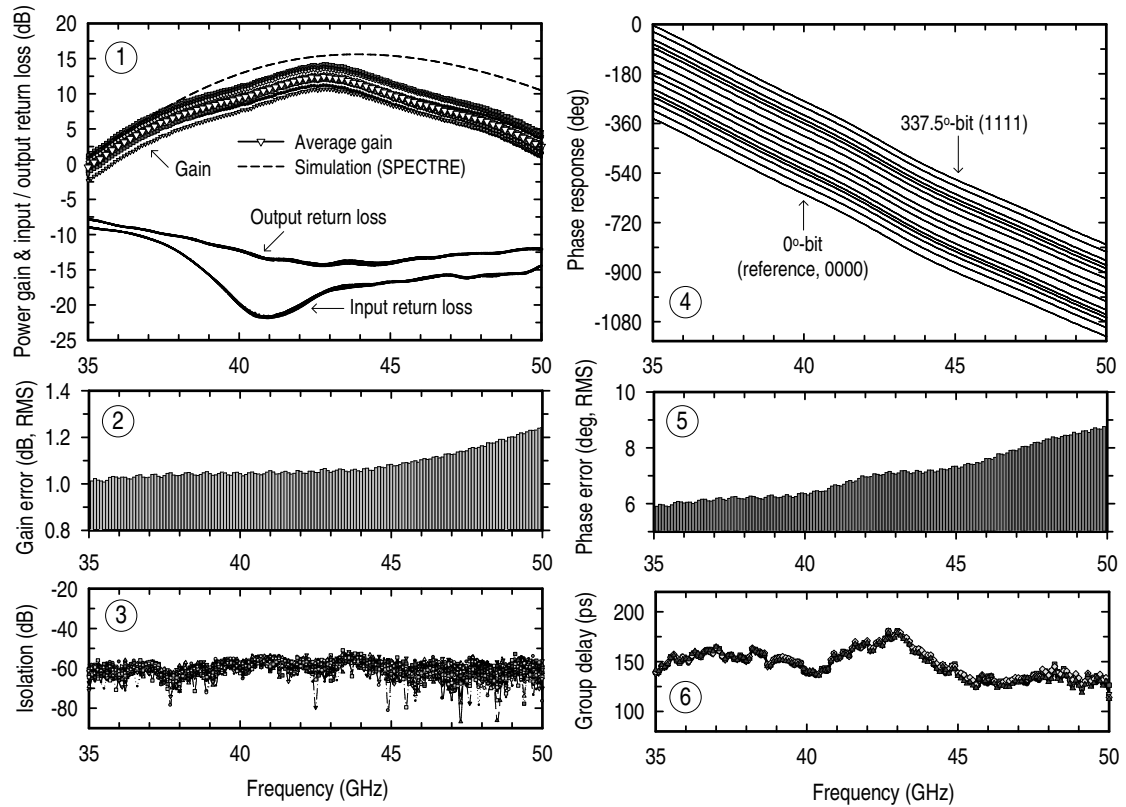


**Figure 6.13:** Chip photograph of the 16-element phased-array transmitter (area= $2.6 \times 3.2 \text{ mm}^2$ ).

transmitter was measured on-chip after a standard SOLT calibration to the probe tips using a vector signal network analyzer (Agilent, PNA-E8364B).

### 6.6.1 Single Channel Characterization

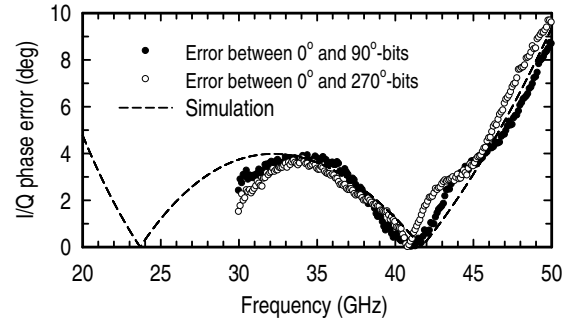
Figure 6.14 presents the measured S-parameters for all 4-bit phase states of a single path (*Channel-1*) in the 16-element array. The measured average power gain is 12.5 dB at 42.5 GHz and the 3-dB gain bandwidth is 39.9-45.6 GHz (Figure 6.14 ①). The discrepancy from simulations above 45 GHz could be due to the inaccurate HBT model at these frequencies together with process variations and errors in the parasitic estimation using EM simulations. The



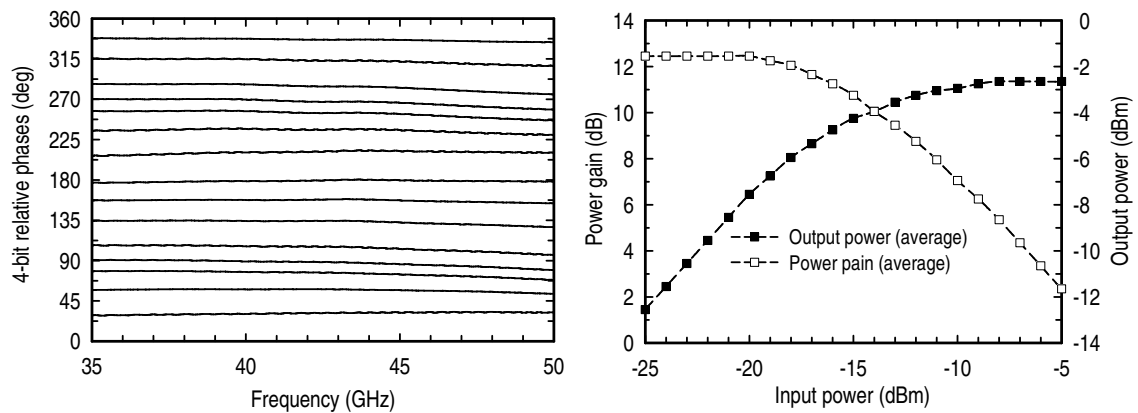
**Figure 6.14:** The measured single channel (*Channel-1*) characteristics for all 4-bit phase states. ①: input and output matching, and power gain, ②: RMS gain error, ③: output-to-input isolation, ④: 4-bit phase responses, ⑤: RMS phase error (from ideal 4-bit phases) and ⑥: averaged group delays for 0°, 22.5°, 45°, 67.5° and 90°-bit phase states.

peak-to-peak gain variation for all 4-bit phase states is about 3 dB at 40-45 GHz, and the RMS gain variation (error) is < 1.3 dB up to 50 GHz (Figure 6.14 ②). The measured input return loss is < -10 dB at 36.6-50 GHz, and output return loss is < -10 dB at 37.6-50 GHz. The isolation from output to input is below -55 dB at 30-50 GHz (Figure 6.14 ③).

The 4-bit phase response is measured from 35-50 GHz using the digital control from array decoder without any calibration (Figure 6.14 ④). The measured RMS phase error from the ideal 4-bit phase states (with a reference to the measured 0°-bit phase) is < 8.8° up to 50 GHz and much less than the 4-bit phase quantization level of 22.5° (Figure 6.14 ⑤). The wideband characteristic is an inherent nature of the active phase shifter, since the phase interpolation technique is a linear process independent of the operating frequency, and the bandwidth is mainly limited by the I/Q network. The group delay is measured by a derivative of the measured phase



**Figure 6.15:** The measured I/Q phase imbalance in the QAF. The simulation was done using SPECTRE with foundry passive models (estimated loading capacitance  $\approx 50\text{-}80$  fF).

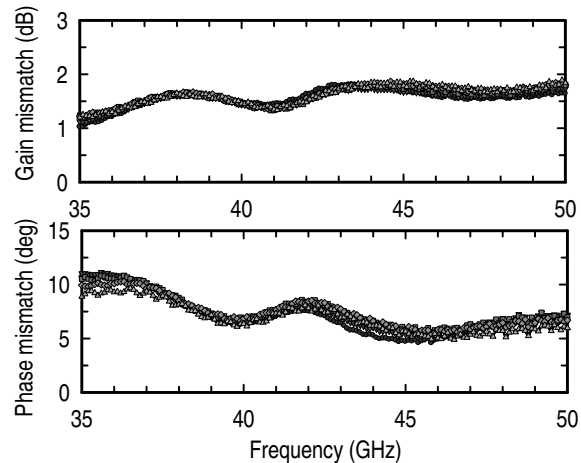


**Figure 6.16:** The measured 4-bit relative phase states (*left*), and output power per channel at 42.5 GHz versus RF input power (*right*).

responses and averaged by 5-point moving average with 100 MHz step. The group delay is 150 ps at 44 GHz and its variation at 40-45 GHz is  $\pm 20$  ps (Figure 6.14 ⑥).

The I/Q phase accuracy of the QAF is measured indirectly by comparing the phases of the  $0^\circ$ ,  $90^\circ$  and  $270^\circ$ -bit settings at the outputs. The I/Q phase error is  $\leq 5^\circ$  at 30-46.5 GHz (Figure 6.15). The  $0^\circ$ -bit phase response is subtracted from all the measured 4-bit phase responses and the phase shifters show a constant wideband relative 4-bit phase states [Figure 6.16 (*left*)]. The output  $P_{1dB}$ , which is measured at the peak gain frequency of 42.5 GHz, is  $-5 \pm 1.5$  dBm and the maximum output power is  $-2.5 \pm 1.5$  dBm for all 4-bit phase states [Figure 6.16 (*right*)]. A  $P_{1dB}$  analysis of the individual stage in the phased-array transmitter indicates that the output  $P_{1dB}$  is limited by the current at the output stage.

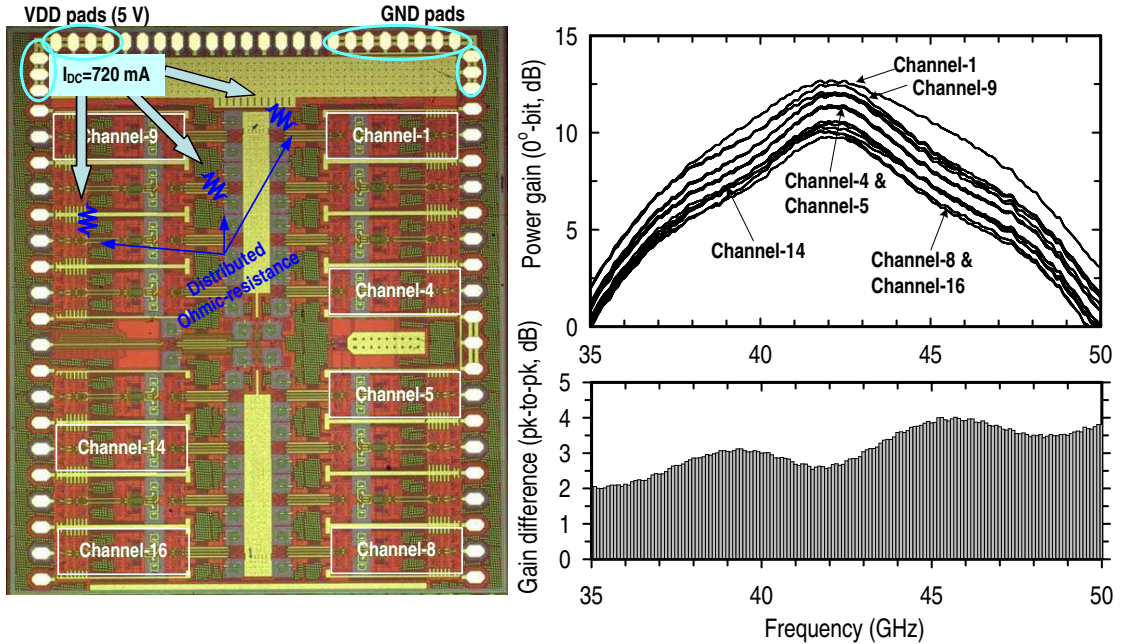




**Figure 6.17:** The measured channel-to-channel RMS gain and phase mismatches between the 16 channels for 5 different phase states ( $0^\circ$ ,  $22.5^\circ$ ,  $45^\circ$ ,  $67.5^\circ$  and  $90^\circ$ -bit phase states).

## 6.6.2 Array Characterization

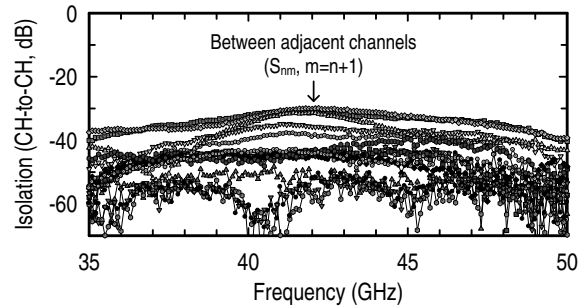
*Channel-to-Channel Mismatches:* The output impedance matching of all the other channels is nearly identical to *Channel-1*. The gain and phase mismatches between the 16 different channels are measured by comparing the gain and phase response of the  $0^\circ$ ,  $22.5^\circ$ ,  $45^\circ$ ,  $67.5^\circ$  and  $90^\circ$ -bit S-parameters of all the 16 channels. Other phase settings follow similar mismatches. The measured raw RMS gain mismatch is  $\leq 1.8$  dB and the RMS phase mismatch is  $\leq 7^\circ$  at 40-50 GHz (Figure 6.17). Compared with the result of the receiver in Chapter 5, the transmitter array shows larger channel mismatches. It is reasoned that in the transmitter, a large bias current of 720 mA is supplied from a chip corner (Figure 6.18(left)), and as the DC current passing by each array element, it causes ohmic voltage drop across the arrays due to distributed parasitic resistances inside the chip. This induces supply voltage and ground resistance variations between different channels, resulting in gain and phase variations among the array elements. Actually, it is measured that the power gains of channel-1 & -9 (upper parts of the chip in Figure 6.18(left)) are higher than those of channel-8 and channel-16 (lower parts of the chip in Figure 6.18(left)), presumably due to the higher supply voltage and lower ground resistance in the upper parts than in the lower parts of the transmitter (see Figure 6.18(right)). The peak-to-peak amplitude variation among the channels is  $\sim 4$  dB at 35-50 GHz (Figure 6.18(right)). It is worthwhile to mention that the measurement of the channel-to-channel mismatches include the



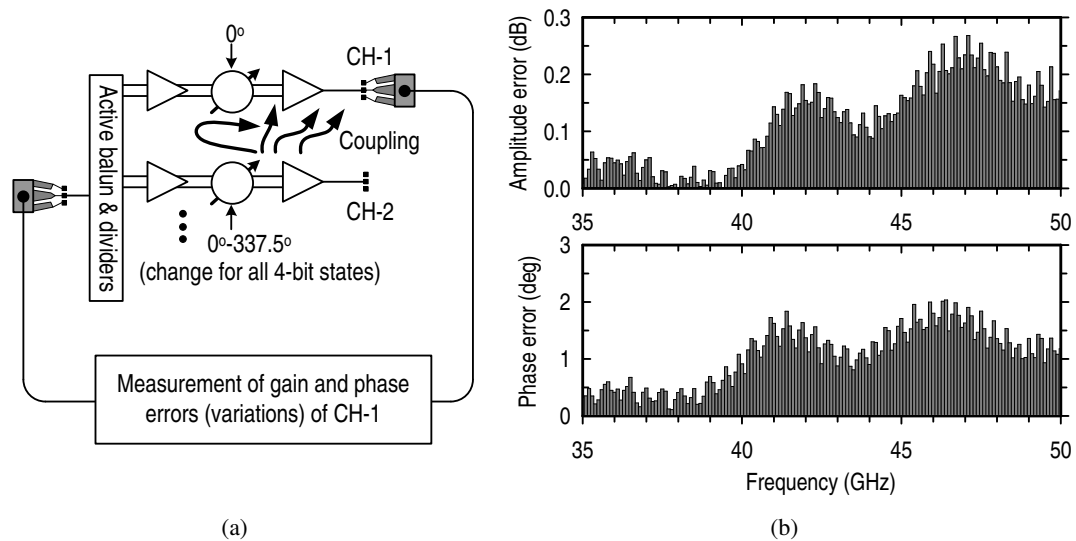
**Figure 6.18:** Gain mismatch between different channels due to on-chip supply voltage and ground resistance variations: supplying bias current from a corner of the 16-element array chip (left), and measured power gain (with  $0^\circ$ -bit phase setting) for all different channels and peak-to-peak gain difference among the channels (right).

mismatches in 1:8 passive dividers. The measured mismatches also include the systematic measurement uncertainties such as cable stability and CPW probe placement errors which could not be calibrated. It is observed that a  $\pm 0.3$  dB error in the power gain S-parameter measurements depending on different probe placements.

*Coupling between Channels:* In integrated silicon phased-arrays, the substrate coupling between the channels is a major concern due to the conductive substrate [49, 74, 84]. Compared with an RF CMOS technology where the substrate resistivity ( $\rho$ ) is 1-2  $\Omega/\text{cm}$ , the SiGe BiCMOS process provides a relatively high resistivity substrate with  $\rho=8-10\ \Omega/\text{cm}$ . This, together with differential signaling and careful isolation consideration in the layout, helps reduce the coupling between channels. A worst case port-to-port coupling (isolation) of -30 dB is measured at 41-43 GHz between adjacent channels and the isolation between the other channel combinations is  $< -40$  dB up to 50 GHz (Figure 6.19). As detailed in [74] and [49], the parasitic coupling interactions between channels induce output signal errors. To investigate the errors, *Channel-1* is set at the  $0^\circ$ -bit state and *Channel-2* is changed for all 4-bit phase states while mea-



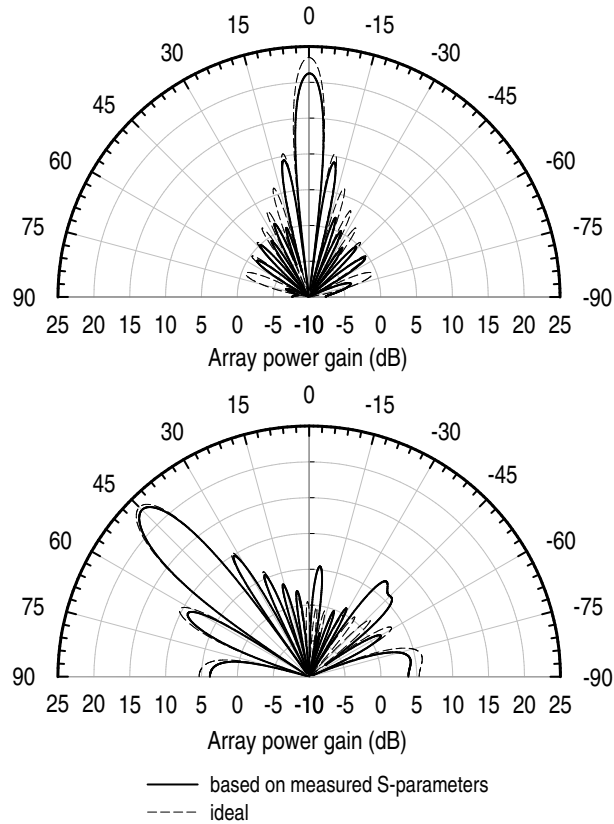
**Figure 6.19:** The measured isolation between channel to channel. The worst case occurs between adjacent channels ( $n=1-15$ ).



**Figure 6.20:** Coupling characterization: (a) coupling test setup, (b) the measured output signal errors (amplitude error and phase error).

asuring the gain and phase errors of the *Channel-1* at the same time (Figure 6.20(a)). The output port of *Channel-2* is left in open-circuit for a worst-case test condition [49]. The measured peak gain and phase errors are  $< 0.3$  dB and  $< 2^\circ$  at 35-50 GHz, respectively (Figure 6.20(b)).

*Array Patterns:* Figure 6.21 presents two cases of synthesized beam patterns (with an assumption of standard linear array with isotropic radiators and  $\lambda/2$  spacing between the elements) in ADS at 44 GHz using the measured 256 two-port S-parameters (16 channels  $\times$  16 S-parameters). In the ideal case, the phase on each element is changed continuously with an assumption of the same power gain of 11.5 dB for all of the 16 elements (11.5 dB is the measured average power gain at 44 GHz). In the measurement case the phase is digi-



**Figure 6.21:** Array beam scanning characteristics: broadside scan (*upper*) and 45° scan angle (*lower*) at 44 GHz.

tized to the nearest measured 4-bit phase states and the corresponding measured amplitude is used. For broadside scanning [Figure 6.21 (*upper*)], both results shows 6.4° of 3-dB beamwidth ( $=\sin^{-1}(0.891 \times 2/N)$ ,  $N=16$ ) and 14.3° of first null-to-null bandwidth ( $=2 \times \sin^{-1}(2/N)$ ,  $N=16$ ). For the 45° scan [Figure 6.21 (*lower*)], the sidelobes at -6° and -45° directions are a little bit larger than the ideal case due to the finite quantized phase states, but are still negligible compared with the main lobe power gain. The measured results are summarized in Table 6.1.

## 6.7 Conclusion

A millimeter-wave phased-array transmitter is developed with 4-bit RF phase shifters for Q-band (40-45 GHz) satellite communication applications. The 16 array elements and the digital control units are integrated in a chip area of  $2.6 \times 3.2 \text{ mm}^2$ , achieving the highest integration of millimeter-wave phased-array elements to-date. This high integration is due to the active phase shifter having very small size ( $0.43 \times 0.27 \text{ mm}^2$ ) and the compact passive dividers based

**Table 6.1:** Performance Summary of the Q-band 16-element phased-array transmitter

Quantity	Results
Technology	0.18 $\mu$ m SiGe BiCMOS (Jazz SiGe120, 1P6M)
Frequency band	Q-Band (40-45 GHz)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	720 mA
Chip area	2.6x3.2 mm <sup>2</sup>
Single Path Characteristics	
Input return loss	$\leq -10$ dB @ 36.6-50 GHz
Output return loss	$\leq -10$ dB @ 37.6-50 GHz
Channel power gain (ave)	12.5 dB @ 42.5 GHz (3-dB BW: 40-45 GHz)
Phase resolution	4-bit
Gain error	$< 1.3$ dB (RMS) @ 35-50 GHz
Phase error	$< 8.8^\circ$ (RMS) @ 35-50 GHz
Output P <sub>1dB</sub>	$-5 \pm 1.5$ dBm @ 42.5 GHz
Maximum output power (P <sub>sat</sub> )	$-2.5 \pm 1.5$ dBm @ 42.5 GHz
Isolation (output-to-input)	$\leq -55$ dB @ 35-50 GHz
Array Characteristics	
Phase mismatch (RMS)	$\leq 7^\circ$ @ 40-50 GHz (between all channels)
Amplitude mismatch (RMS)	$\leq 1.8$ dB @ 40-50 GHz (between all channels)
Isolation (CH-to-CH)	$\leq -30$ dB @ 35-50 GHz
Array factor directivity	12 dB (16 elements)

on the 3-dimensional broadside-coupled transmission line. The proposed coaxial-type shielded transmission line structure allows dense integration of differential lines, and is an enabling technology for highly integrated millimeter-wave systems. The phase shifter shows  $< 8.8^\circ$  of RMS phase error from the ideal 4-bit phase states at 35-50 GHz. The matching between the 16 different channels is very good: RMS gain variation is  $< 1.8$  dB and RMS phase variation is  $< 7^\circ$  at 35-50 GHz with no on-chip calibration. The parasitic coupling between the channels is negligible up to 50 GHz. All of these lead an excellent agreement between the ideal beam pattern and the synthesized beam pattern based on measure S-parameters. While the phased-array transmitter is designed as a subarray to be integrated in a  $20 \times 20$  large array, it also can be used as stand-alone array, and the simple *All-RF* architecture enables this design to be extended to 60 GHz or 77 GHz for low cost millimeter-wave phased-arrays.

## 6.8 Acknowledgements

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- K.-J. Koh, J. W. May and G. M. Rebeiz, “A Millimeter-Wave (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE J. Solid-State Circuits*, (in review).
- K.-J. Koh, J. W. May and G. M. Rebeiz, “A Q-Band (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18- $\mu\text{m}$  SiGe BiCMOS Technology,” *IEEE RFIC Symp. Dig.*, pp. 225-228, June 2008.

I would like to thank my coauthors Mr. Jason W. May and Prof. Gabriel M. Rebeiz.

# 7

## Conclusion

### 7.1 Summary of Work

This dissertation demonstrates silicon-based on-chip phased-array front-end designs, mainly focusing on the beam-forming networks composed of phase shifters and combiners/dividers. The phased-arrays adopt a corporate-feed architecture using RF active phase shifters which utilize an I/Q signal interpolation to synthesize required phase. To generate the I/Q signal in the active phase shifter, a new quadrature all-pass filter is proposed and its performances are verified theoretically and experimentally in the dissertation. The novelty of the quadrature all-pass filter is that, although being composed of all passive components, it can generate very wideband quadrature signals with 3 dB of voltage gain by utilizing the second-order L-C resonance, resolving the malignant loss problem in conventional R-C based quadrature networks. Typically the I/Q network can achieve more than 100% bandwidth with an I/Q phase error  $< 5^\circ$  and with  $> 2.6$  dB of voltage gain. Thanks to the lossless wideband I/Q network and the active signal interpolation approach, the active phase shifters show very wideband multi-bit phase states with minimum loss and high accuracy. In the proposed phase shifter architecture, the output phase error originated from the quadrature errors of the I/Q network can be calibrated using a higher resolution DAC, and therefore, the phase accuracy is mainly limited by the matching between the DAC current sources. Since recent silicon-based integrated circuit technologies can provide an excellent transistor matching, the proposed phase shifter architecture is suitable particularly for on-chip silicon phased-arrays for high resolution and low-cost applications. This is verified experimentally through various phased-array designs using the active phase shifter

at microwave and millimeter-wave frequency bands. The measured results of the phased-arrays agree well with circuit simulations done by SPECTRE and ADS using foundry process models, showing a good manufacturing reliability and reproducibility. The dissertation also demonstrates that the phased-array design technique adopting the active phase shifter can have a good scalability to a large array by developing successfully sixteen-element phased-array transmitter at Q-band. Namely, compared with LO- or IF-phase shifting architectures, the phased-array architecture with RF (active) phase shifters enables the construction of large arrays with less system complexity, since it is not involved with frequency conversion units and associated LO distribution, solving one of key barriers to complex phased-array fabrication. The followings summarize performances of the active phase shifters and phased-arrays presented in this dissertation.

**I. 4-Bit Active Phase Shifters:** Two 4-bit active phase shifters integrated with all digital control circuitry in 0.13- $\mu\text{m}$  RF CMOS technology are developed for X- and Ku-band (8-18 GHz), and K-band (18-26 GHz) phased arrays, respectively. Both phase shifters can change phases with less than  $\sim 2$  dB of RMS amplitude imbalance through an associated DAC control. For the X- and Ku-band phase shifter, the RMS phase error is  $< 10^\circ$  over the entire 5-18 GHz range. The average insertion loss is  $-3\sim-0.2$  dB at 5-20 GHz with  $I_{DC}=5.8$  mA ( $V_{DC}=1.5$  V). The input  $P_{1dB}$  for all 4-bit phase states is typically  $-5.4\pm 1.3$  dBm at 12 GHz in the X- and Ku-band phase shifter. The K-band phase shifter exhibits  $6.5\sim 13^\circ$  of RMS phase error at 15-26 GHz. The average insertion loss is  $-4.6\sim-3$  dB at 15-26 GHz with  $I_{DC}=7.8$  mA from  $V_{DC}=1.5$  V. The input  $P_{1dB}$  of the K-band phase shifter is  $-0.8\pm 1.1$  dBm at 24 GHz. For both phase shifters, the core size excluding all the pads and the output  $50\ \Omega$  matching circuits, inserted for measurement purpose only, is very small,  $0.33\times 0.43\ \text{mm}^2$ .

**II. 5-Bit Active Phase Shifter:** A fundamental benefit of the active phase shifter is that it can increase phase resolution with simple DC current readjustment in the control DAC without additional chip area consumption. This is shown well in the 5-bit phase shifter design using 0.18- $\mu\text{m}$  CMOS technology for 6-18 GHz applications. In this design, an integrated current-mode DAC controls the I/Q amplitudes monotonically to get 4-bit phase states and the DAC current is finely calibrated to achieve 5-bit phase resolution. All the I/O pads including RF input and output pads are ESD-protected. The phase shifter shows 19.5 dB



of power gain with  $< 1.1$  dB of RMS gain variation for all 5-bit phase states at 12 GHz, and the 3-dB gain bandwidth is 7.5-15.2 GHz. The measured RMS phase error is  $< 3^\circ$  at 6.4-10.2 GHz and  $< 5.6^\circ$  at 6-18 GHz achieving more than 5-bit accuracy. Within the 3-dB gain bandwidth the NF ranges from 4 to 5.7 dB and the NF variation is within  $\pm 0.12$  dB for all phase states. The total current consumption is 18.7 mA (phase shifter core:  $\sim 3$  mA) from a 3.3 V supply voltage and overall chip size is  $1.2 \times 0.75$  mm<sup>2</sup> (phase shifter core:  $0.45 \times 0.35$  mm<sup>2</sup>).

**III. X- and Ku-Band 8-Element Phased-Array Receiver:** The eight-element phased-array receiver realized in a standard 0.18- $\mu$ m SiGe BiCMOS technology shows 1.5~24.5 dB of power gain per channel from a 50  $\Omega$  load at 12 GHz with  $I_{DC}=100$ -200 mA, depending on the bias current control ( $V_{DC}=3.3$  V), and the associated NF ranges from 4.2 dB (@ max. gain) to 13.2 dB (@ min. gain). The RMS gain error is  $< 0.9$  dB and the RMS phase error is  $< 6^\circ$  at 6-18 GHz for all 4-bit phase states. The measured group delay is  $162.5 \pm 12.5$  ps for all phase states at 6-18 GHz. The RMS phase mismatch and RMS gain mismatch among the eight channels are  $< 2.7^\circ$  and 0.4 dB, respectively, for all 16 phase states, over 6-18 GHz. The eight-element array can operate instantaneously at any center frequency and with a wide bandwidth (3 GHz to 6 GHz, depending on the center frequency) given primarily by the 3-dB gain variation in the 6-18 GHz range. The chip size is  $2.2 \times 2.45$  mm<sup>2</sup> including all pads and CMOS control electronics.

**IV. Q-Band 4-Element Phased-Array Receiver:** The four-element phased-array front-end receiver is implemented in the 0.18- $\mu$ m SiGe BiCMOS technology for Q-band (30-50 GHz) applications and uses the corporate-feed approach with on-chip Wilkinson power combiners. Typical loss of the on-chip Wilkinson couplers is  $\leq 0.6$  dB up to 50 GHz. The phased-array receiver shows a power gain of 10.4 dB with an IIP<sub>3</sub> of -13.8 dBm per element at 38.5 GHz and a 3-dB gain bandwidth of 32.8-44 GHz. The RMS gain and phase errors are  $\leq 1.2$  dB and  $\leq 8.7^\circ$  for all 4-bit phase states at 30-50 GHz. The beamformer also results in  $\leq 0.4$  dB of RMS gain mismatch and  $\leq 2^\circ$  of RMS phase mismatch between the four channels. The channel-to-channel isolation is better than -35 dB at 30-50 GHz. The chip consumes 118 mA from a 5 V supply voltage and overall chip size is  $1.4 \times 1.7$  mm<sup>2</sup> including all pads.

**V. Q-Band 16-Element Phased-Array Transmitter:** Sixteen array elements are integrated in the Q-band phased-array transmitter, the highest integration level to-date, using the 0.18- $\mu\text{m}$  SiGe BiCMOS technology. In the transmitter array a 1:2 active divider and two 1:8 passive tee-junction dividers constitute the corporate-feed network, and 3-dimensional perfectly-shield transmission-lines are used for the passive divider to minimize area. The phased-array transmitter results in a 12.5 dB of average power gain per channel at 42.5 GHz with a 3-dB gain bandwidth of 39.9-45.6 GHz. The RMS gain variation is  $< 1.3$  dB and the RMS phase variation is  $< 8.8^\circ$  for all 4-bit phase states at 35-50 GHz. The measured input and output return losses are  $< -10$  dB at 36.6-50 GHz, and  $< -10$  dB at 37.6-50 GHz, respectively. The measured peak-to-peak group delay variation is  $\pm 20$  ps at 40-45 GHz. The output  $P_{1dB}$  is  $-5 \pm 1.5$  dBm and the maximum saturated output power is  $-2.5 \pm 1.5$  dBm per channel at 42.5 GHz. The transmitter shows  $< 1.8$  dB of RMS gain mismatch and  $< 7^\circ$  of RMS phase mismatch between the 16 different channels over all phase states. These channel-to-channel mismatches are primarily limited by power supply drop across the chip. A -30 dB worst-case port-to-port coupling is measured between adjacent channels at 30-50 GHz, and the measured RMS gain and phase disturbances due to the inter-channel coupling are  $< 0.15$  dB and  $< 1^\circ$ , respectively, at 35-50 GHz. The chip consumes 720 mA from a 5 V supply voltage and the chip size is  $2.6 \pm 3.2$  mm<sup>2</sup>.

## 7.2 Summary of Accomplishment

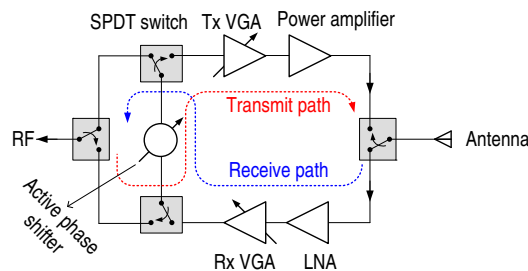
The consistent theme for all parts of this dissertation is the development of integrated phased-array transceivers using the RF phase shifters, while maintaining the corporate-feed architecture so as to increase backward compatibility with existing phased-array systems. In effect, this is the first realization of on-chip silicon phased-arrays with the RF phase shifting scheme. In particular, the quadrature all-pass filter is first proposed and leads to an architectural breakthrough in the phase shifter design which is suitable for integrated phased-arrays by relaxing design trade-off. Upon the completion of the phase shifter development, the phased-array transmitter and receivers are designed, fabricated and characterized successfully at various frequency bands using a SiGe BiCMOS technology, and each design ranks the first demonstration of silicon phased-array at the corresponding design frequency. The summary of accomplishment in this study follows.

- Developed a new quadrature all-pass filter (QAF) for a wideband I/Q signal generation with maximum 3 dB of voltage gain;
- Verified the QAF operation both in theory and experiment at various frequency bands;
- Validated the superiority of the QAF to conventional R-C based I/Q networks by a comparison between the QAF and R-C polyphase filters;
- Studied the I/Q errors of the QAF under various process variations and parasitic loading effect, and proposed modifications of the QAF to improve the I/Q accuracy under the loading effect, extending the application area up to millimeter-wave frequency ranges;
- Performed a detailed analysis of quadrature accuracy requirement for active phase shifter design which utilizes an I/Q signal interpolation to generate the required phase;
- Developed 4-bit and 5-bit active phase shifters using the QAF in 0.13- $\mu\text{m}$  and 0.18- $\mu\text{m}$  CMOS technologies for X-, Ku- and K-bands applications (6-26 GHz), featuring the smallest chip size ever reported at these frequencies with similar phase resolutions, and achieving very wideband accurate phase shifts which can not be obtained using lumped passive phase shifters;
- Developed X- and Ku-band 8-element phased array receiver with RF active phase shifters in 0.18- $\mu\text{m}$  SiGe BiCMOS technology, integrating all digital control units and bias reference, proving the feasibility silicon-based on-chip phased-arrays with the RF phase shifter for the first time;
- Developed Q-band 4-element phased array receiver with RF active phase shifters for the first time in 0.18- $\mu\text{m}$  SiGe BiCMOS technology, validating the QAF and active phase shifter performance at millimeter-wave frequencies;
- Developed and integrated on-chip Wilkinson couplers successfully on a silicon substrate for coherent linear signal combining and dividing in the phased-array applications, especially for millimeter-wave applications;
- Developed Q-band 16-element phased array transmitter with RF phase shifters in 0.18- $\mu\text{m}$  SiGe BiCMOS technology, a landmark as the highest integration of phased-array element down to date, proving a good scalability to a large array of the proposed phased-array architecture adopting the active phase shifters;
- Conducted various coupling studies between different channels in each phased-array, and characterized experimentally the output signal errors caused by on-chip coupling.

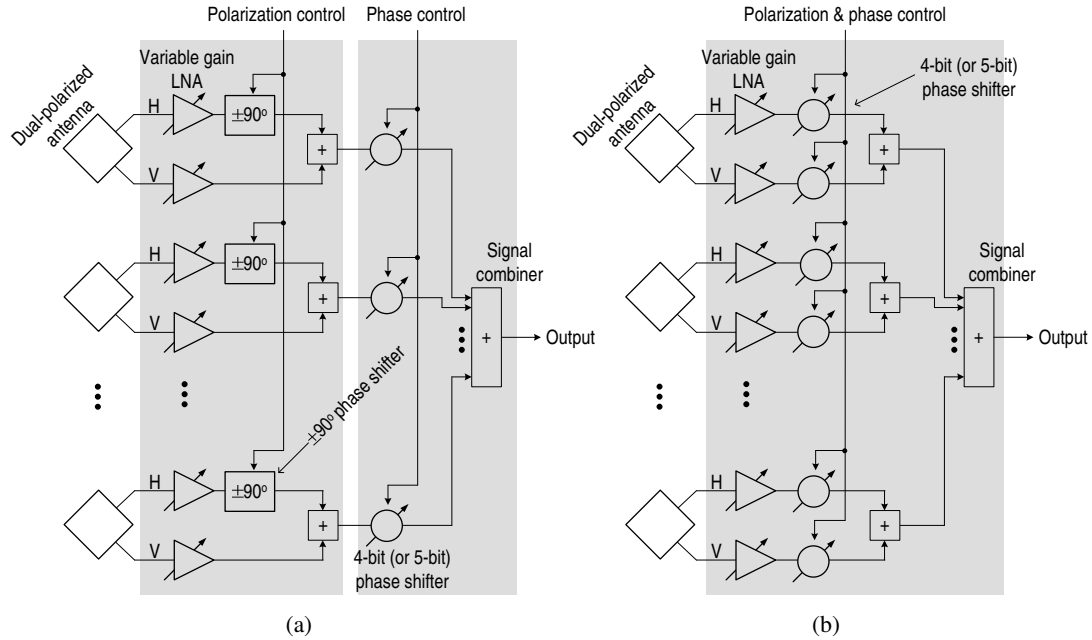
### 7.3 Future Work

Opportunities of future work involves the increase of integration levels of both array element numbers and function blocks. Thanks to the compact phase shifters, simple corporate-feed array architecture and its good scalability to a large array, larger number of array elements (32 or even 64 array elements) can be integrated with same architecture, demonstrating the possibility of on-chip large arrays in silicon technology. At the same time, intensive studies on low-noise and high-power silicon amplifiers should be conducted and these amplifiers need to be integrated on the phased-arrays to have a practical meaning of the on-chip silicon phased-arrays for low-cost applications. Particularly, the phased-array design technology need to migrate from the SiGe BiCMOS to a CMOS technology to further reduce cost. This is possible Considering the device performances of current nano-scale CMOS technology. Future CMOS phased-array can have practical uses in the commercial bands depending on the phased-array applications.

The active phase shifter can also be used to realize a bidirectional T/R module in conventional ways, which is shown simply in Figure 7.1 for example. While two independent VGAs are inserted in transmit and receive paths for amplitude tapering, the VGA function can be shared by placing single VGA before the active phase shifter. Since the active phase shifter developed in this work is differential, the T/R module need to be fully differential, otherwise there should be a balun in each transmitter and receiver path. Although the active phase shifter itself is not bidirectional, the T/R module can be bidirectional by switching the single-pole-double-through (SPDT) switches properly. To be a practical system, the performance of the SPDT switches is very important, i.e., to minimize the transmitter leakage to receiver path and to minimize the NF degradation by the switches in the receiver path, the SPDT switches need to



**Figure 7.1:** Bidirectional T/R module realization using the active phase shifter developed in the dissertation.

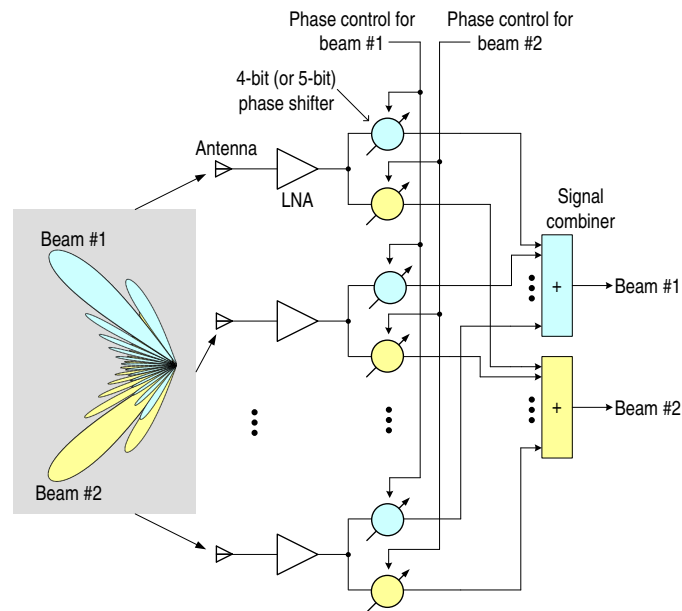


**Figure 7.2:** Polarization controllable phased-array receivers, (a) with  $\pm 90^\circ$  phase shifter for polarization control and 4-bit (or 5-bit) phase shifter for phased-array control, (b) with 4-bit (or 5-bit) phase shifter for both horizontal and vertical paths for both polarization (any polarization) and phased-array controls.

have both high isolation and low loss. In silicon technologies, it is still challenging to implement high performance passive switch, especially at high frequencies. The active phase shifter also may need to be optimized to satisfy noise and linearity specifications simultaneously required from the both transmit and receive paths.

Also, the phased-arrays developed in the dissertation can be readily extended to multi-function phased-arrays. Special interests are in polarization-agile phased-arrays (Figure 7.2) and multi-beam phased-arrays (Figure 7.3).

**Polarization-agile phased-array:** Typically the polarization control function can be built in the phased-arrays in two ways. In Figure 7.2(a), the  $\pm 90^\circ$  phase shifter delays (or advances) the horizontally incident signal with respect to the phase of the vertically excited signal depending on RHCP or LHCP, and the quadrature all-pass filter developed in Chapter-2 can be an excellent candidate for this function. In Figure 7.2(b), two independent phase shifters can be controlled such that the phase difference between the two phase shifters can be either  $+90^\circ$  or  $-90^\circ$  for all digitized phase states, depending on the polarization of in-



**Figure 7.3:** Dual-beam phased-array receiver. The polarization controllable function can be built in the dual-beam system by combining the idea in Figure 7.2.

coming signal. The phase shifters and active or passive signal combiners developed in this dissertation can be reused or modified with little effort for different operation frequencies.

**Multi-beam phased-array:** Since the integrated active phase shifter occupies very small space, multiple active phase shifters can be integrated with relatively small area consumption and controlled independently to process multiple beams at the same time. Figure 7.3 shows a two-beam phased-array receiver for example. While the phase shifters and signal combiners and dividers can be developed in the same manner as in the dissertation, the isolation between the paths for beam 1 and 2 needs to be high so as not to interfere with each other. Therefore, a careful study and characterization of coupling between different channels needs to be conducted for a successful realization of the multi-beam phased-arrays especially in CMOS technology due to the conductive substrate in silicon.

## Appendix A

# Phased-array in view of sampled-data system (review)

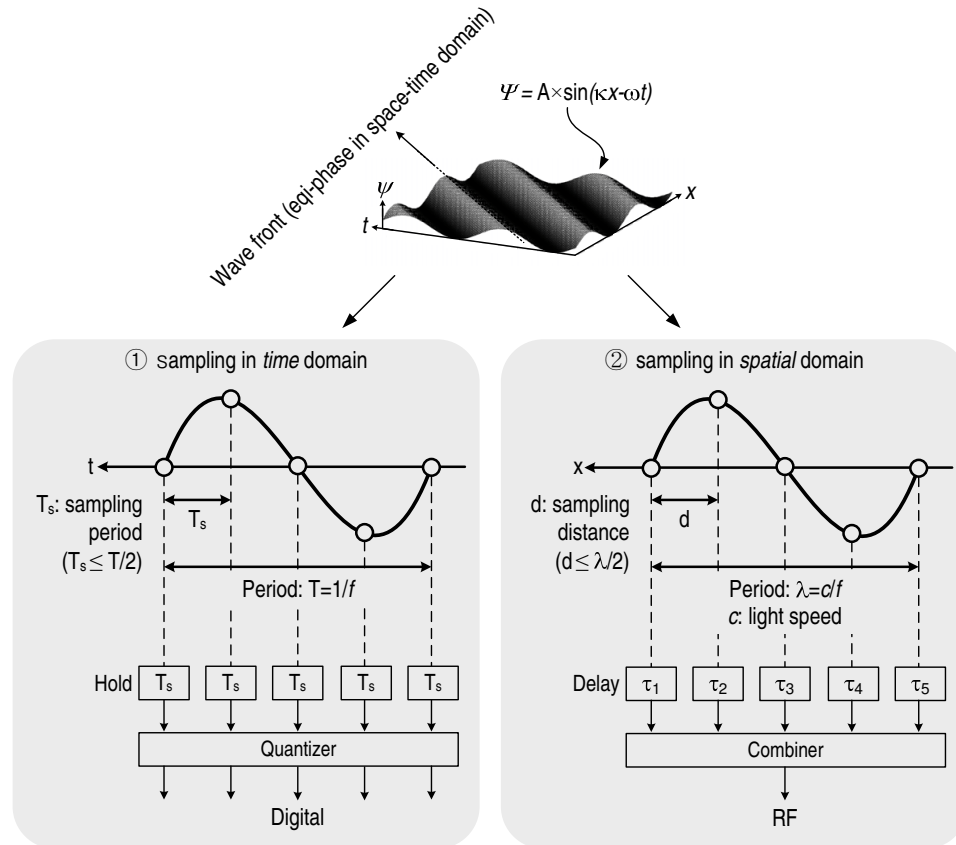
### A.1 Time-Domain Sampling & Spatial Domain Sampling

In this appendix, the phased-array system is introduced in the respect of a sampled-data system, which will help to understand phased-array as a spatial filter.

In wireless communications, the EM-wave, simply expressed as (A.1) for example, is a basic quantity to be processed and has both of time varying and spatially varying information. In (A.1),  $k$  ( $=2\pi/\lambda$ ) is the wave number meaning the rate of phase change per unit distance in space-time domain, and corresponds to the angular frequency  $\omega$  ( $=2\pi f$ ) which is the rate of phase change per unit time in angular frequency-time domain.

$$\psi = A \times \sin(kx - \omega t). \quad (\text{A.1})$$

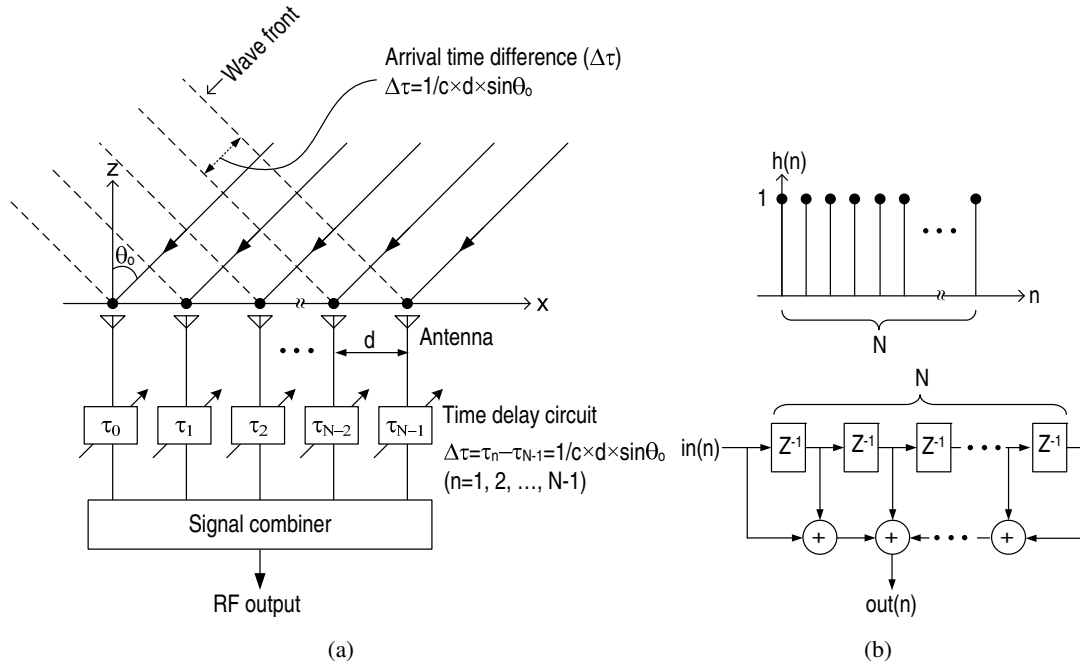
In conventional wireless communication systems using single omni-directional antenna, the antenna can not differentiate the spatially varying information. Thus, the information carried on the EM-wave can only be processed in time-domain after being sampled and quantized using an ADC after a series of RF and analog signal processes. However, if we use an array of antennas, then the wave-front of the propagating EM signal will hit each antenna at different time slot. Since the wave-front carries same information in space-time domain, the information simultaneously collected by each antenna will be different in the antenna array when the interval of each antenna is properly selected. Therefore, the antenna array can be regarded as a sampling system at spatial domain, and there is an analogy between time-domain sampling performed by an ADC and spatial domain sampling executed by an antenna array, which is shown in Figure A.1.



**Figure A.1:** Sampled data systems: sampling at frequency-time domain as in ADC and sampling at space-time domain as in antenna array.

The sampling distance ( $d$ ) at spatial domain, which is the distance between adjacent antennas in the antenna array, corresponds to the sampling period,  $T_s$ , in time-domain sampling. The inherent nature of the time-domain sampling is the repetition of information by the sampling period, called “aliasing”, and to avoid the aliasing,  $T_s$  has to be less than half of the signal period (Nyquist rate). By the same principle, the sampling distance,  $d$ , needs to be smaller than half of the signal wavelength to avoid “grating lobe” which is a different name of the aliasing in phased-array terminology [22, 23]. Since the propagating wave hits the antennas consecutively in the antenna array, the information gathered by each antenna has difference only in phase. Therefore, by delaying each sampled signal by appropriate sequential time step ( $\tau_{1-5}$ ), all the signals fetched by the array antennas can be combined with in-phase. The conventional time-domain sampling systems need hold time ( $T_s$ ) to quantize and digitize the sampled data. Eventually the coherently combined RF signal in the antenna array will undergo the time-domain





**Figure A.2:** True time-delay (TTD) antenna array and FIR filter: (a) antenna array with TTD circuit at each antenna element ( $d$ =array spacing and  $\theta_o$ =scan angle), (b) FIR filter as an analogy to the TTD array. The one clock delay ( $Z^{-1}$ ) in FIR filter corresponds to one unit time delay of  $\Delta\tau=d/c \times \sin\theta_o$ .

sampling process to extract information.

### A.2 Antenna Array as a FIR Filter at Space-Time Domain

Figure A.2(a) shows an example of antenna array composed of  $N$  antenna elements. If the incident angle of the EM wave to each array antenna is  $\theta_o$ , then the arrival time difference between any two adjacent antennas,  $\Delta\tau=\tau_n-\tau_{n-1}$  where  $n=1, 2, 3, \dots, N-1$ , is  $\Delta\tau=d/c \times \sin\theta_o$  ( $c$ =light speed). This causes phase differences between the incoming signals on each antenna. For all the received signals to be in-phase, each antenna input has to be delayed monotonically by  $\Delta\tau$  using true time-delay (TTD) circuits, i.e.,  $\tau_0=0, \tau_1=\Delta\tau, \tau_2=2\Delta\tau, \dots, \tau_{N-1}=(N-1)\Delta\tau$ . Finally the signal combiner adds all the received signals coherently, boosting the signal power by a factor of  $N^2$ . Therefore, the basic operations of the antenna array system are to sample the signal using a series of antennas in space domain, to delay the sampled signals consecutively by a time step of  $\Delta\tau$ , and finally to add the received signals in phase. Actually this is the

same function as in the finite impulse response (FIR) filter shown in Figure A.2(b). The one clock delay ( $Z^{-1}$ ) in FIR filter corresponds to the one unit time-delay of  $\Delta\tau$  in antenna array. As a result, the array factor of the antenna array shown in Figure A.2(a) can be given as (A.2) which is exactly the same transfer function of the FIR filter presented in Figure A.2(b) with the replacement of  $\varphi$  ( $=k \times d \times \cos\theta_o$ ) with  $\omega$  [8, 23].

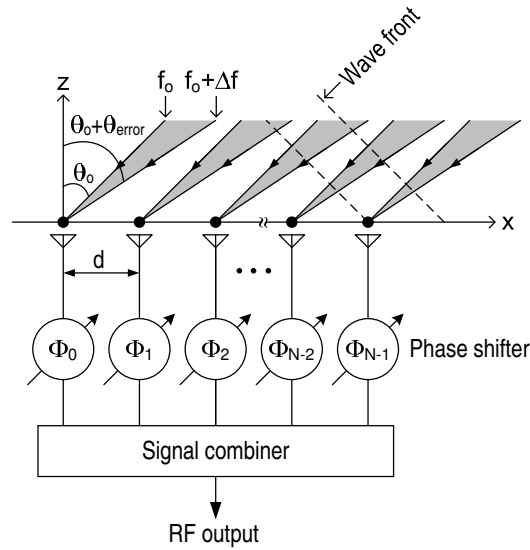
$$\begin{aligned} AF &= \sum_{n=0}^{N-1} e^{-jnkd \cos\theta_o} = e^{-j(N-1)\frac{kd \cos\theta_o}{2}} \frac{\sin\left(N\frac{kd \cos\theta_o}{2}\right)}{\sin\left(\frac{kd \cos\theta_o}{2}\right)} \\ &= e^{-j(N-1)\frac{\varphi}{2}} \frac{\sin\left(N\frac{\varphi}{2}\right)}{\sin\left(\frac{\varphi}{2}\right)} \end{aligned} \quad (\text{A.2})$$

where  $-kd \leq \varphi \leq kd$  and the phase term merely represents the phase shift of the array phase center relative to the origin. Therefore, the antenna array system can be regarded as a FIR filter, filtering the signal at space-time domain, and the increase of the antenna element number will narrower the beamwidth, just like that the passband becomes narrower as increasing the number of filter tap in the FIR filter. The 3-dB beamwidth (half-power beamwidth, HPBW), a measure of the selectivity at spatial domain, is defined to be the point where the  $|AF|$  is lowered by 3 dB from its maximum and is approximated as (A.3) in standard linear array with uniform illumination.

$$\varphi_{3dB} \simeq 0.886 \times \frac{2\pi}{N}, \quad (\text{for } N > 10) \quad (\text{A.3})$$

### A.3 Phased Array vs TTD Array

Although TTD arrays can achieve very wideband beamforming function, TTD circuits are too bulky to be realized in integrated circuit technologies and controlling the true time delay at each element level is also quite complex. Figure A.3 presents phased-array where TTD circuits are replaced by phase shifters for compactness and simple control. To discuss further, let's define an input signal having a finite bandwidth of  $2 \times \Delta f$  as (A.4) where  $A_o$  is amplitude,  $f_o$  is a center frequency and  $\Delta f$  is frequency deviation from the center frequency.



**Figure A.3:** Phased array where phase shifters adjust the phase of incoming signals at each antenna.

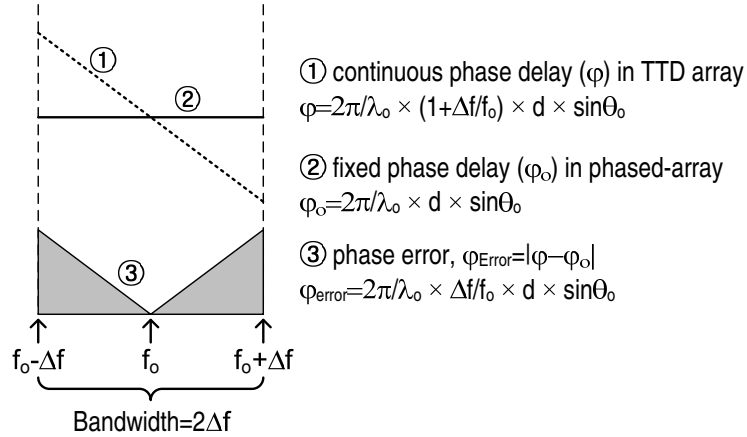
$$V_s = A_o \times \sin 2\pi (f_o + \Delta f) t = A_o \times \sin 2\pi f_o \left( 1 + \frac{\Delta f}{f_o} \right) t. \quad (\text{A.4})$$

As discussed, in TTD array the time-delay difference ( $\Delta\tau$ ) between any two adjacent elements results in a phase delay ( $\varphi$ ) given as (A.5) between adjacent elements.

$$\begin{aligned} \varphi &= 2\pi f_o \left( 1 + \frac{\Delta f}{f_o} \right) \times \Delta\tau = \frac{2\pi}{\lambda_o} \left( 1 + \frac{\Delta f}{f_o} \right) \times d \times \sin \theta_o \\ &= k \times d \times \sin \theta_o. \end{aligned} \quad (\text{A.5})$$

The  $\varphi$  is a linear monotonically decreasing function of  $\Delta f$  resulting in a coincidence of signals in time ( $\varphi$  is a lagging phase and has negative value). Therefore there is no pointing error in TTD array, i.e., all the signal components having different frequencies of  $f_o + \Delta f$  point the same direction of  $\theta_o$ .

However, in phased-array, all the signals are in phase only at the center frequency of  $f_o$ . Since the phase shifters emulate the time delay at just one frequency ( $f_o$ ), a fixed phase delay across the signal bandwidth will generate finite phase delay error for each frequency component except for the center frequency. Figure A.4 shows phase delays between adjacent elements and ① represents the phase delay ( $\varphi$ ) for TTD array case which is monotonic decreasing function



**Figure A.4:** Phase error for different frequency components due to the finite phase quantization in the phased array.

of  $\Delta f$  as expressed in (A.5). ② is a fixed phase delay of  $\varphi_o$  for the phase-array case and is set for the beamsteering direction of  $\theta_o$  at  $f_o$  ( $\Delta f = 0$  in (A.5)). Therefore the net phase error of ③ in the phased-array from the TTD case is  $\varphi_{error} = |\varphi - \varphi_o|$  which is given in (A.6). The  $\varphi_{error}$  will increase linearly as the frequency deviates from the center frequency, and can be a maximum at the band edges.

$$\varphi_{error} = \frac{2\pi}{\lambda_o} \times \frac{\Delta f}{f_o} \times d \times \sin\theta_o. \quad (\text{A.6})$$

The  $\varphi_{error}$  causes different scan angle errors ( $\theta_{error}$  in Figure A.3) for different frequency components, and the net result for the band-limited signal is pointing error called *beam squint* [9]. This is inevitable for the phased-array since the continuous phase delay in TTD array is quantized to a fixed phase delay in phase scanning case. To be insensitive to the scanning error caused by the phase quantization error, the  $\varphi_{error}$  should be less than half of the  $\varphi_{3dB}$  in (A.3), and this results in the bandwidth constraint given as

$$\frac{2\Delta f}{f_o} \leq 0.886 \times \frac{\lambda_o}{N \times d} \times \frac{1}{\sin\theta_o}. \quad (\text{A.7})$$

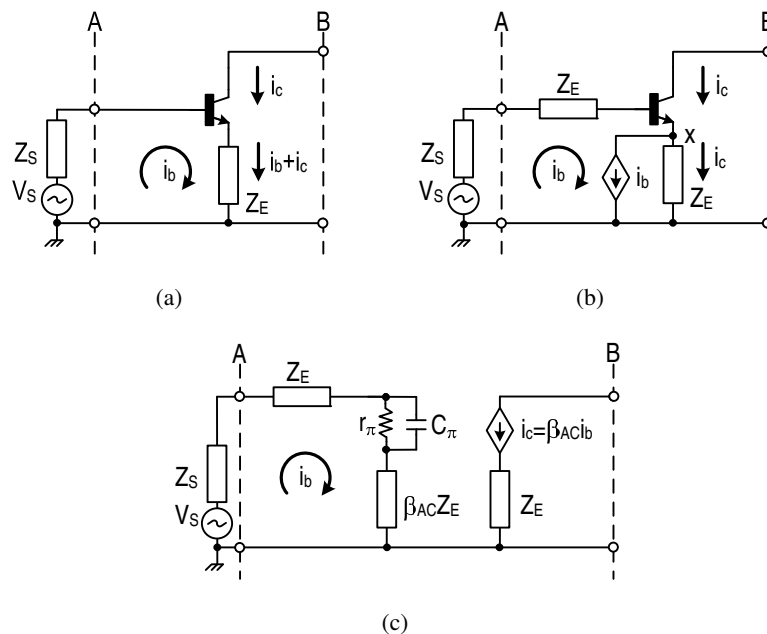
There is a trade-off between beam scanning range ( $\theta_o$ ) and allowable signal bandwidth ( $\Delta f$ ), and the bandwidth also trades off with the array size  $N$ . In case of 16-element standard linear array,

$\Delta f/f_o$  is about  $\pm 3.2\%$  for  $\theta_o = \pm 60^\circ$  of beam scan range, which is just enough for covering the frequency range of  $44 \pm 1$  GHz at the sub-array level required in this work, which is detailed in Chapter 6.

## Appendix B

# Noise analysis of the low-noise active balun in Chapter 4

In this appendix, details of the NF analysis for the low-noise active balun designed in Chapter-4 are provided. Figure B.1 illustrates a useful concept of base current isolation from the emitter branch, which simplifies the noise analysis under an emitter-degeneration  $Z_E$  that is assumed to be a noiseless passive element. The base current can be isolated from the emitter loop by inserting a dependent current source whose magnitude is exactly the same as base current ( $i_b$ )



**Figure B.1:** Equivalence with base current isolation: (a) common-emitter with  $Z_E$  degeneration, (b) base current isolation from emitter branch, (c) small signal equivalence of (b).

between the emitter and ground [Figure B.1(b)]. To address the series feedback caused by  $i_b$  and  $Z_E$  in the emitter terminal, the  $Z_E$  is inserted in the base branch in Figure B.1(b), resulting in identical input/output impedances and input/output currents between Figure B.1(a) and B.1(b). Therefore, the two circuits are equivalent, and by reflecting  $Z_E$  of the emitter branch in Figure B.1(b) into the base loop, the collector loop can be separated from the base loop [Figure B.1(c)]. The output current is given as

$$i_C = \frac{V_S}{Z_E + \left( \frac{r_\pi // \frac{1}{j\omega C_\pi}}{\beta_{AC}} + \frac{Z_S + Z_E}{\beta_{AC}} \right)} = \frac{V_S}{Z_E + \left( \frac{1}{g_m} + \frac{Z_S + Z_E}{\beta_{AC}} \right)} \quad (\text{B.1})$$

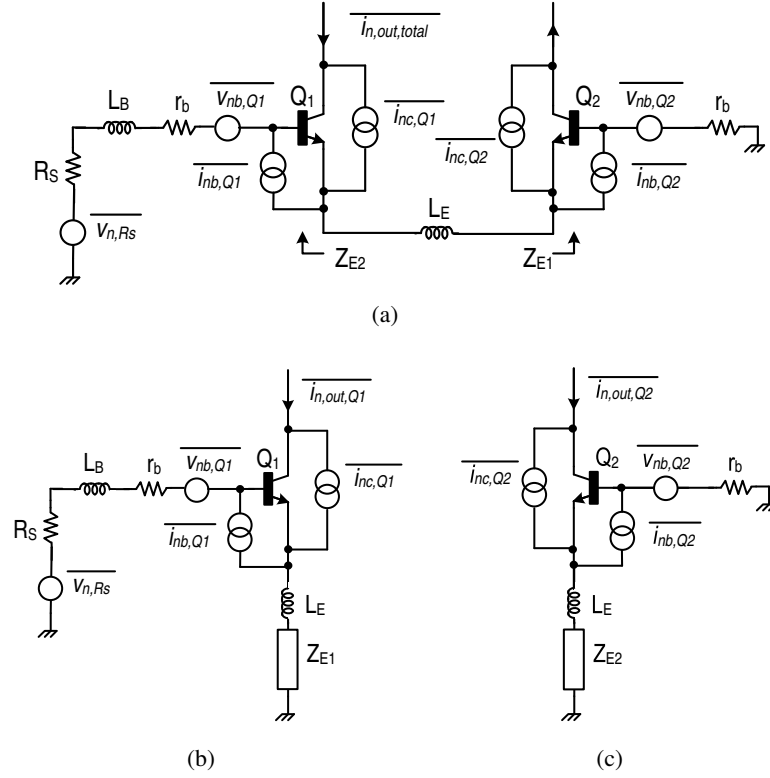
where the denominator is the transimpedance of whole network and the terms inside the parenthesis in the denominator are the overall base side impedances reflected into node x in Figure B.1(b).

Figure B.2(a) identifies all the noise sources in the transconductor of the LNAB shown in Figure 4.6(a), and can be decomposed into Figure B.2(b) and Figure B.2(c). Figure B.2(b) shows the output noise current ( $\langle i_{n,out,Q1} \rangle$ ) contribution from the noise sources of  $Q_1$  and source resistance,  $R_s$ , and Figure B.2(c) shows the output noise current ( $\langle i_{n,out,Q2} \rangle$ ) resulting from the noise sources of  $Q_2$  where  $Z_{E2} \simeq 1/g_m + (R_s + r_b + j\omega L_B)/(1 + \beta_{AC})$ .  $\langle v_{nb,Q1} \rangle$  and  $\langle v_{nb,Q2} \rangle$  are noise voltages from the base ohmic resistances of  $Q_1$  and  $Q_2$ , respectively.  $\langle i_{nc,Q1} \rangle$ ,  $\langle i_{nc,Q2} \rangle$ ,  $\langle i_{nb,Q1} \rangle$  and  $\langle i_{nb,Q2} \rangle$  are the internal shot noise currents.  $\langle v_{n,R_s} \rangle (=4kTR_s\Delta f)$  is the noise voltage from  $R_s$ . Assuming that all the noise sources are uncorrelated; base ohmic resistances in the  $Q_1$  and  $Q_2$  are same; and  $Q_1$  and  $Q_2$  are biased with same current, then  $\langle v_{nb,Q1}^2 \rangle = \langle v_{nb,Q2}^2 \rangle = 4kTr_b\Delta f$ ,  $\langle i_{nc,Q1}^2 \rangle = \langle i_{nc,Q2}^2 \rangle = 2qI_c\Delta f$  and  $\langle i_{nb,Q1}^2 \rangle = \langle i_{nb,Q2}^2 \rangle = 2qI_b\Delta f$ , where  $I_c$  and  $I_b$  are the collector and base bias currents, respectively.

The overall NF can be represented as (B.2) where  $\langle i_{n,out,total}^2 \rangle$  is the total output noise current and  $\langle i_{n,out,R_s}^2 \rangle$  is the output noise current due to the  $R_s$  only.

$$NF = \frac{\langle i_{n,out,total}^2 \rangle}{\langle i_{n,out,R_s}^2 \rangle} = \frac{\langle i_{n,out,Q1}^2 \rangle + \langle i_{n,out,Q2}^2 \rangle}{\langle i_{n,out,R_s}^2 \rangle}. \quad (\text{B.2})$$

In Figure B.2(b), it is straightforward to calculate the output noise currents by  $\langle v_{n,R_s}^2 \rangle$ ,



**Figure B.2:** Noise sources of the main LNA transconductor: (a) noise source identification, (b) output noise current from the noise sources of  $Q_1$ , (c) output noise current from the noise sources of  $Q_2$ .

$\langle v_{nb,Q1}^2 \rangle$  and  $\langle i_{nb,Q1}^2 \rangle$  if we apply the equivalence shown in Figure B.2 and substitute  $Z_S$  and  $Z_E$  in (B.1) with  $Z_S = R_S + r_b + j\omega L_B$  and  $Z_E = j\omega L_E + Z_{E1}$ , respectively. Equations (B.3)-(B.6) present the output noise currents from the corresponding noise sources in Figure B.2(b).

$$\langle i_{n,out,Rs}^2 \rangle = \frac{\langle v_{n,Rs}^2 \rangle}{|Z_{T1}|^2},$$

where  $Z_{T1} = (Z_{E1} + j\omega L_E)$  (B.3)

$$+ \left( \frac{1}{g_m} + \frac{1}{\beta_{AC}} (R_S + r_b + j\omega (L_B + L_E) + Z_{E1}) \right).$$

$$\langle i_{n,out,r_b}^2 \rangle = \frac{\langle v_{nb,Q1}^2 \rangle}{|Z_{T1}|^2}. \quad (B.4)$$

$$\langle i_{n,out,I_b}^2 \rangle = \frac{\langle v_{th,I_b}^2 \rangle}{|Z_{T1}|^2}$$

$$= \frac{1}{|Z_{T1}|^2} \times |R_S + r_b + j\omega (L_B + L_E) + Z_{E1}|^2 \times \langle i_{nb,Q1}^2 \rangle. \quad (B.5)$$



$$\langle i_{n,out,IC}^2 \rangle = \frac{\left| \frac{1}{g_m} + \frac{1}{\beta_{AC}} (R_S + r_b + j\omega (L_B + L_E) + Z_{E1}) \right|^2}{|Z_{T1}|^2} \times \langle i_{nc,Q1}^2 \rangle. \quad (\text{B.6})$$

$Z_{T1}$  is the overall transimpedance in Figure B.2(b), and  $\langle v_{th,Ib} \rangle$  in (B.5) is a Thevenin noise voltage caused by  $\langle i_{nb,Q1} \rangle$  in the base loop. In (B.6), the output noise current due to  $\langle i_{nc,Q1} \rangle$  is the result of a current division between the degeneration impedance and the impedance reflected from base loop into the emitter node under the equivalence shown in Figure B.1. Thus, the total output noise current from Figure B.2(b) is

$$\langle i_{n,out,Q1}^2 \rangle = \langle i_{n,out,Rs}^2 \rangle + \langle i_{n,out,r_b}^2 \rangle + \langle i_{n,out,I_b}^2 \rangle + \langle i_{n,out,IC}^2 \rangle. \quad (\text{B.7})$$

After applying the same procedure to Figure B.2(c), we get the final NF equation given as (B.8).

$$\begin{aligned} NF = 1 + & \left( 1 + \left| \frac{Z_{T1}}{Z_{T2}} \right|^2 \right) \frac{\langle v_{nb,Q1}^2 \rangle}{\langle v_{n,Rs}^2 \rangle} \\ & + \left( \frac{|R_s + r_b + j\omega (L_B + L_E) + Z_{E1}|^2}{\left| \frac{Z_{T1}}{Z_{T2}} \right|^2 |r_b + j\omega L_E + Z_{E2}|^2} \right) \frac{\langle i_{nb,Q1}^2 \rangle}{\langle v_{n,Rs}^2 \rangle} \\ & + \left( \frac{\left| \frac{1}{g_m} + \frac{1}{\beta_{AC}} (R_s + r_b + j\omega (L_B + L_E) + Z_{E1}) \right|^2}{\left| \frac{Z_{T1}}{Z_{T2}} \right|^2 \left| \frac{1}{g_m} + \frac{1}{\beta_{AC}} (r_b + j\omega L_E + Z_{E2}) \right|^2} \right) \frac{\langle i_{nc,Q1}^2 \rangle}{\langle v_{n,Rs}^2 \rangle} \end{aligned} \quad (\text{B.8})$$

$$\text{where } Z_{T2} = (Z_{E2} + j\omega L_E) + \left( \frac{1}{g_m} + \frac{1}{\beta_{AC}} (r_b + j\omega L_E + Z_{E2}) \right).$$

$Z_{T2}$  is the effective overall transimpedance in Figure B.2(c), corresponding to  $Z_{T1}$  in Figure B.2(b). Apparently, in (B.8), if  $Z_{E1}=0$  and  $Z_{T2}=\infty$  (implying no DC current in  $Q_2$ ), then the NF can be reduced to that of a conventional inductively degenerated LNA, found in [61, 62]. The noise contribution from  $Q_2$  in the LNAB is coupled through the transimpedance ratio of  $|Z_{T1}/Z_{T2}|$  which is typically  $\leq 1$  depending on the operating frequency.

To simplify the NF further, several parameters are defined in (B.9)-(B.12).  $|Z_{T1}/Z_{T2}|$  ( $=\delta_z$ ) also indicates the noise contribution from the  $r_b$  of  $Q_2$ .  $\chi_z$  and  $\eta_z$  are the output noise

contribution factors by the base shot noise current and collector shot noise current of  $Q_2$ , respectively. After substitutions of  $\langle v_{nb,Q1}^2 \rangle / \langle v_{n,Rs}^2 \rangle = r_b / R_s$ ,  $\langle i_{nc,Q1}^2 \rangle / \langle v_{n,Rs}^2 \rangle = I_C / (2\beta_{DC} V_T R_s)$  and  $\langle i_{nc,Q1}^2 \rangle / \langle v_{n,Rs}^2 \rangle = I_C / (2V_T R_s)$ , the NF can be given as (B.12) under the case that an input impedance is matched with  $R_s$  at  $\omega = \omega_o$ .

$$\delta_z = \left| \frac{Z_{T1}}{Z_{T2}} \right|. \quad (\text{B.9})$$

$$\chi_z = \frac{\left| \left( \frac{Z_{T1}}{Z_{T2}} \right) (r_b + j\omega L_E + Z_{E2}) \right|}{\left| R_s + r_b + j\omega (L_B + L_E) + Z_{E1} \right|}. \quad (\text{B.10})$$

$$\eta_z = \frac{\left| \left( \frac{Z_{T1}}{Z_{T2}} \right) \left( \frac{1}{g_m} + \frac{1}{\beta_{AC}} (r_b + j\omega L_E + Z_{E2}) \right) \right|}{\left| \frac{1}{g_m} + \frac{1}{\beta_{AC}} (R_s + r_b + j\omega (L_B + L_E) + Z_{E1}) \right|}. \quad (\text{B.11})$$

$$\begin{aligned} \text{NF} = & 1 + (1 + \delta_z^2) \frac{r_b}{R_s} + (1 + \chi_z^2) \left( R_s + r_b + \frac{V_T}{I_C} \right)^2 \frac{I_C}{2\beta_{DC} V_T R_s} + (1 + \eta_z^2) \frac{V_T}{2R_s I_C} \\ & + \left( \frac{\omega_T}{\omega_o} \right)^2 (1 + \chi_z^2) \frac{4V_T}{R_s \beta_{DC} I_C} \\ & + \left( \frac{\omega_o}{\omega_T} \right)^2 (1 + \eta_z^2) \frac{I_C}{2R_s V_T} \left( R_s + r_b + \frac{V_T}{I_C} \right)^2. \end{aligned} \quad (\text{B.12})$$

Intuitively, with a reasonably small value of  $r_b$ , the base shot noise current of  $Q_2$  can be negligible, as it will sink into the ground through  $r_b$ . This is clear in (B.10) where  $\chi_z \ll 1$  with a normal choice of passive values at the frequency of interest.  $\delta_z$  can be approximated as  $\delta_z \simeq 1$  up to very high frequency range, meaning that the output noise contribution from the base thermal noise of  $Q_2$  can be equivalent to that from  $Q_1$ . The output noise contribution from the collector shot noise current of  $Q_2$ , which is expressed as  $\eta_z$ , depends on the operation frequency. At low frequencies where  $\beta_{AC}$  is still very large,  $\eta_z \simeq 1$ . However, when  $\beta_{AC}$  decreases with increasing frequency,  $\eta_z$  decreases from 1 since some portion of collector shot noise current of  $Q_2$  can circulate by itself in  $Q_2$ , and does not contribute to the output noise. These considerations make it possible to approximate the NF as (4.7) in Chapter 4.

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