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Two-Dimensional Molybdenum Disulfide Field-Effect Transistors and Its Related Heterostructures

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Materials Science and Engineering

by

Yu Chai

June 2016

Dissertation Committee:
Dr. Cengiz S. Ozkan, Chairperson
Dr. Mihrimah Ozkan
Dr. Roger Lake
Dr. Sandeep Kumar

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The Dissertation of Yu Chai is approved:

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Committee Chairperson

University of California, Riverside

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ABSTRACT OF THE DISSERTATION

Two-Dimensional Molybdenum Disulfide Field-Effect Transistors and Its Related Heterostructures

by

Yu Chai

Doctor of Philosophy, Graduate Program in Materials Science and Engineering
University of California, Riverside, June 2016
Dr. Cengiz S. Ozkan, Chairperson

From the standpoint of mainstream IC manufacturing, newly introduced two-dimensional (2D) semiconducting transition metal dichalcogenides (TMDs), represented by molybdenum disulfide (MoS_2), may turn out to be the game changer in the relay of MOSFET downscaling process. However, Schottky barrier formed at metal-semiconductor interface makes MoS_2 transistors operate way below their capability. In the first part of this study, by depositing two kinds of contact metal combinations on the same MoS_2 sample, the effect of Schottky and Ohmic contacts on the extrinsic field-effect mobility has been studied. The result indicates that non-optimal contacts can become the "bottleneck' that hinders carrier transport, making transistors operate way below their intrinsic performance limit. A highly transparent M-S interface should be regarded as a prerequisite for stabilizing transistors in deep triode region and further mobility extraction. In the second part, a "passivation first, metallization second" technique is developed for fabricating edge contacts to MoS_2 in two heterostructures -

$Al_2O_3/MoS_2/SiO_2$ and h-BN/MoS_2/h-BN. Electrostatic gating effect has been characterized through the configuration of back-gated FETs. A plasma etching step with volatile product, and subsequent smooth side wall profiles are found related to more efficient Ohmic-like channel conduction. This technique is applicable to both exfoliated and synthesized TMDs, and it presents a useful route for preserving the pristine quality of 2D semiconductor from material preparation to device characterization. In the end, strain is exerted to MoS_2 channel by depositing a silicon nitride stress capping layer that covers the entire transistor. Current on/off ratio and other transistor performance metrics are measured as the transistor evolves from back-gate, to top-gate and finally, strain-gate configurations. A 58% increase in electron mobility and 46 % increase in on-current magnitude are observed in strain-gated, compared with top-gated transistors. This is the first study that directly links the strain effect to device performance of MoS_2 top-gated transistors.

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Chapter 1 Introduction

1.1 The crystal structure of MoS_2

The isolation of graphene from graphite by mechanical exfoliation in 2004 [1] showed an important fact: two-dimensional crystals can exist in a free-standing form. Graphene is the most well-known two-dimensional (2D) electronic material mainly because of its extremely large carrier mobility >100 000 cm^2/Vs [2]. Since then, research on 2D materials has expanded rapidly.

The key figures in the family of 2D material contain: graphene, a highly conductive semi-metal; hexagonal boron nitride (h-BN), an atomic flat insulator [3]; transition metal dichalcogenides (TMDCs), with the common formula MX_2, where M stands for transition metal (M = Mo, W, Nb, Ta, Ti) and X for Se, S or Te, displaying a rich variety of physical properties. Depending on the metal and the chalcogen involved, their electrical properties span the range from semiconducting to superconducting. The picture of future 2D nanoelectronics is complete.

MoS_2 has a lamellar structure much like graphite, with a molybdenum layer sandwiched between two sulfur layers. The inter-layer distance is ~6.5Å.There are two types of bonds, strong Mo-S covalent bond within the basal plane and very weak S-S Van der Waal force in between the planes with no dangling bonds on the surface. The mineral MoS_2, named molybdenite, was first reported by Linus Pauling in 1923, by means of spectral and Laue photographs [4]. The structure contains two MoS_2 in a hexagonal unit cell having a = 3.15 Å and c = 12.30 Å. Each sulfur atom is equidistant from three

molybdenum atoms, and each molybdenum atom is surrounded by six equidistant sulfur atoms, at the corners of a small triangular prism. MoS_2 has three polymorphs, 2H, 3R and 1T. 2H and 3R share the same trigonal prismatic metallic coordination. In 1T, the coordination becomes octahedral. For the case of monolayer MoS_2, there are only two polymorphs, 1H and 1T (Figure 1.1)

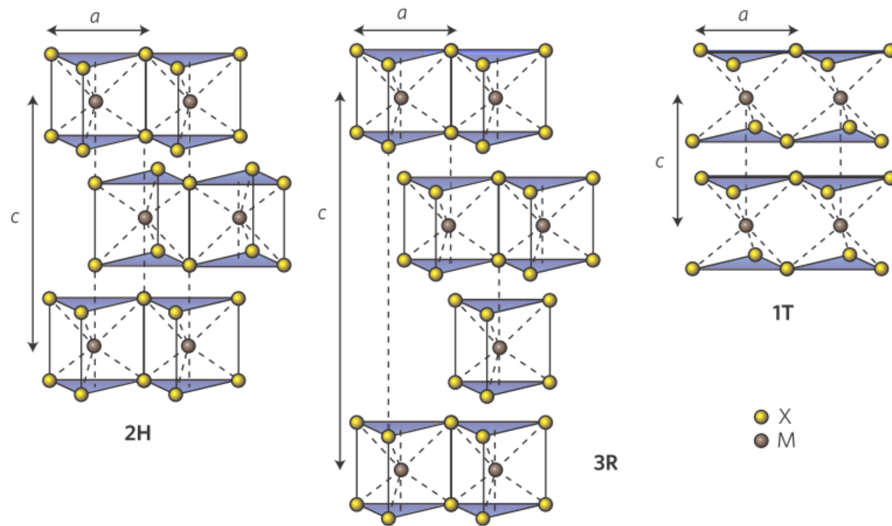
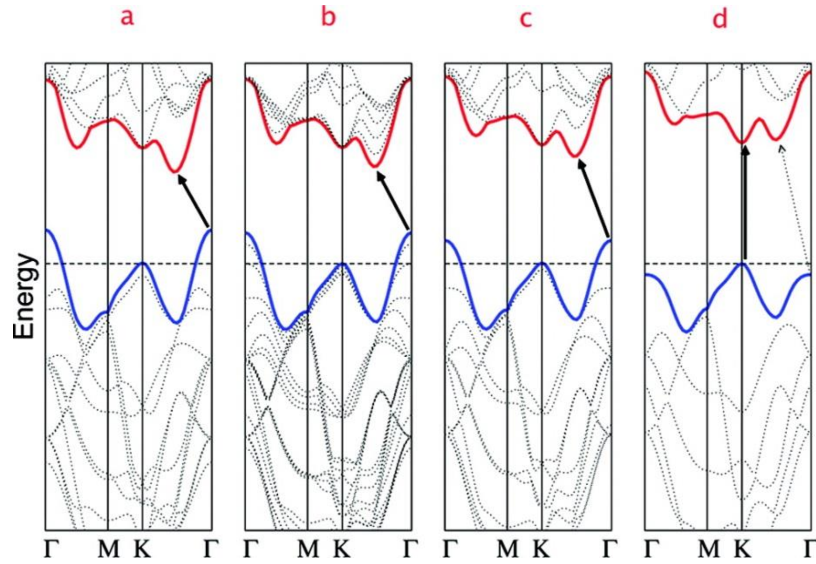


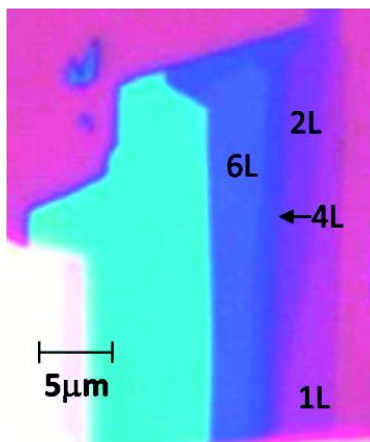
Figure 1.1 The three polymorphs of MoS_2 [5].

1.2 Thickness dependent band structure and related applications

The semiconducting nature of TMDCs has spurred a lot of interest in the mainstream semiconductor industry. Molybedenum Disulfide (MoS_2), one of the most-studied TMDC, has been seen as a candidate material that can replace silicon's leading position. What distinguishes MoS_2 from graphene is the presence of an intrinsic moderate bandgap. In transistors and logic circuits application, the bandgap of the channel material is a major factor determining the electrical conductivity of a solid; more importantly, it

can ensure negligible leakage current when the transistors are switched off for low static power consumption.





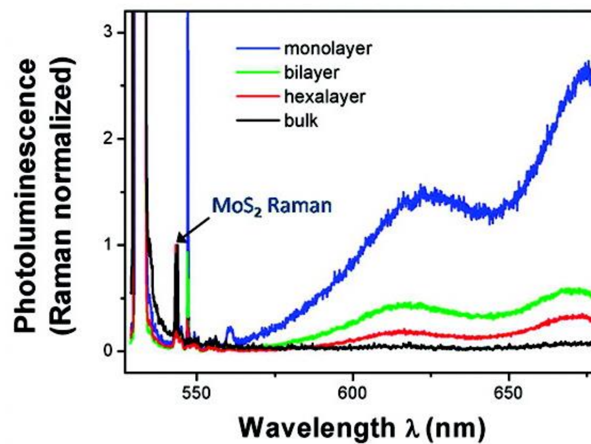


Figure 1.2 (Upper) calculated band structures of (a-d) bulk, quadrilayer, bilayer and monolayer MoS_2; (lower) an exfoliated MoS_2 flake on Si/SiO_2 substrate and its thickness-dependent photoluminescence spectra [7].

Research has shown that the bandgap of bulk MoS_2 is similar to that of silicon, naturally indirect with a value of 1.2 eV. The indirect band gap energy increases as the

crystal thickness is reduced. When a monolayer is reached, the indirect bandgap energy becomes larger than that for a direct transition at K point, therefore, monolayer MoS_2 changes to a direct bandgap semiconductor (single-layer MoS_2 shows a direct bandgap of 1.8 eV; bilayer MoS_2 exhibits an indirect bandgap of 1.3 eV) [6]. This improvement over quantum efficiency has been observed in photoluminescence measurement on mechanical exfoliated MoS_2 samples [7]. The change in the band structure with layer number is due to quantum confinement and the resulting change in hybridization between p_z orbitals on S atoms and d orbitals on Mo atoms [8].

Due to the presence of a sizable direct bandgap and the high efficiency in generating electron and hole pairs, MoS_2 has been found a novel semiconductor for optoelectronics, exemplary applications include photo-transistors [9] and solar cells [10]. Because of its ultra-thin nature, MoS_2 is also considered a favored candidate for flexible electronics [11]. For digital logic devices in literature, as a proof-of-concept, MoS_2 has been used in circuit-level design and fabrication [12], but the electrical performance of each individual MOSFET still needs to be precisely controlled.

1.3 MoS_2 and the short channel effect

An important advantage of these atomically thin 2D semiconductors is their superior resistance to short channel effects at the scaling limit. The Short Channel Effect (SCE) becomes prominent as transistors' gate length is kept on being scaled down nowadays. This effect mainly manifests in roll-off of the threshold voltage (V_T), that is, V_T is lower for a transistor with shorter gate length. This undesirable effect is further

exacerbated by high values of V_{DS}. The fluctuation of transistor characteristics like V_T on the same chip forces the circuit design to become conservative and the full advantage of short channel transistor cannot be utilized. The characteristic length of short channel transistors with planar structure is [13],

$$\lambda = \sqrt{\frac{\varepsilon_S}{\varepsilon_{OX}} t_S t_{OX}}$$

Where λ is the characteristic length, ε_S and ε_{OX} are the permittivity of semiconductor and gate oxide, and t_S and t_{OX} are the thickness of semiconductor channel and gate oxide. The characteristic length allows us to quantify the degree of the SCE for a given device geometry. In this regard, nano-layer MoS_2 shows superior immunity to SCE due to its natural ultrathin body and low dielectric constant. Research has shown that it is possible to have the characteristic length reduced to only 2 nm [13], which is far beyond the ITRS's projection. Because of the highly reactive surface of silicon, it is very complicated to make an atomically thin film. As a result the thinnest usable layers of silicon used in computer chips have been around 2 nm thick [14]. Monolayer MoS_2 with < 1 nm thickness, by contrast, allows chips to be made much smaller.

1.4 The exfoliation of MoS_2 crystals and the thickness determination

Mechanical cleavage produces single-crystal flakes of high purity and cleanliness that are suitable for fundamental characterization. MoS_2 flake with few-nanometer thickness can be obtained from standard mechanical exfoliation using Scotch tape just like the sample preparation procedure for graphene [15]. By folding and unfolding the

sticky side of the tape several times, the original bulky flake with a metallic luster gradually becomes invisible. Though this has been proved as a simple way of obtaining high quality single layer, the yield of monolayer crystals is low and often, large amounts of tape residue remain on the substrate surface. Under an optical microscope, the MoS_2 thin flakes show a variety of colors that are dependent on the flake's thickness. The contrast between the isolated layers and the underlying SiO_2 substrate is due to a phase shift induced by changes in the optical path and material opacity [16].

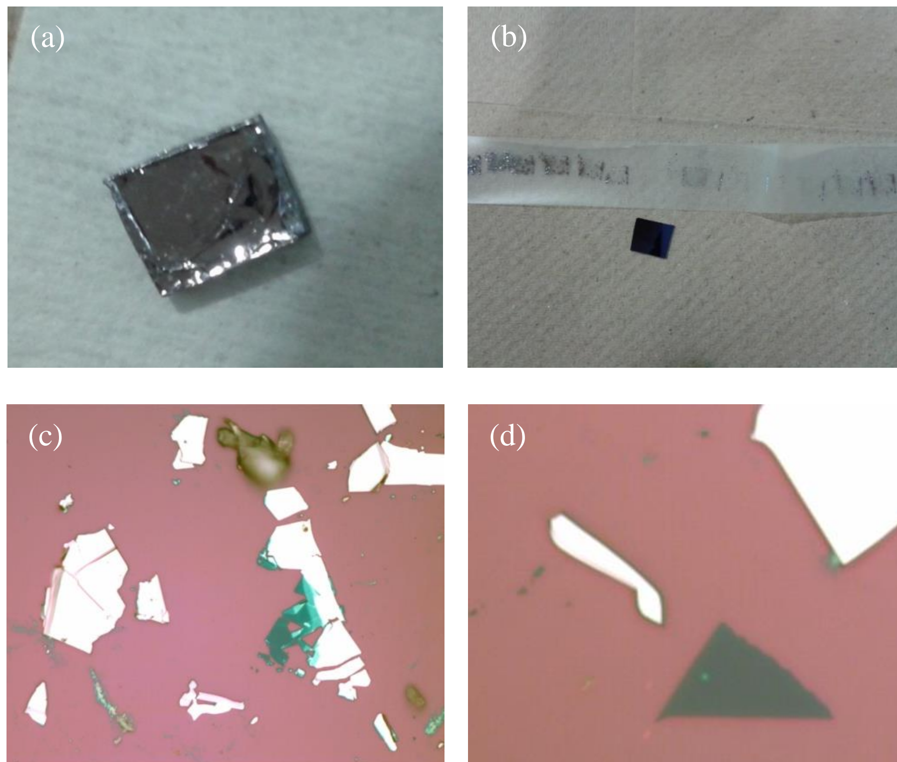
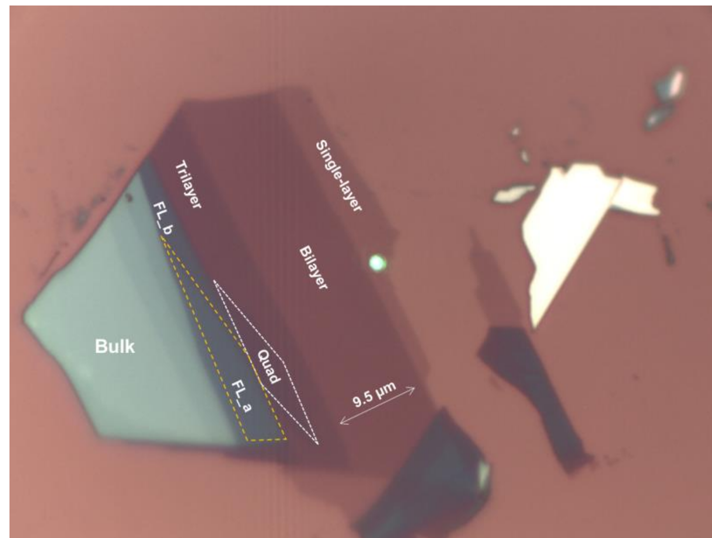


Figure 1.3 (a) MoS_2 bulk crystal with an edge length of ~ 1 cm; (b) after folding and unfolding the tape for a few times, the tape is to be pressed onto a SiO_2 substrate; (c, d) traces of the original crystal are left on the substrate after removing the tape. The greenish area (or bluish, depends on the light source) corresponds to nm-thick MoS_2.

Raman spectroscopy is frequently applied to determine the number of layers in as-exfoliated MoS_2 samples. In the high frequency region of a Raman spectrum, for monolayer MoS_2, the spacing between E_{2g}^{1} and A_{1g} is 19 cm^{-1}. This number increases to 22 cm^{-1} for bi-layer MoS_2 [17]. It has also been proposed to read the low frequency region for thickness measurement [18]. Here, the shear mode peak E_{2g}^{2} is used as an indicator. This peak is totally absent in monolayer MoS_2, then appears close to 20 cm^{-1} for bi-layer, further shifts to almost 30 cm^{-1} for tri-layer, then centered at 30 cm^{-1} for quad-layer. The location of E_{2g}^{2} and the spacing between the high frequency modes need to be cross-checked to confirm the number of layers in any MoS_2 sample. An exfoliated MoS_2 sample in Figure 1.4 shows a variety of thickness. No E_{2g}^{2} peak was found at the labeled single-layer area. The peak appears close to 20 cm^{-1} for the bi-layer region, shifts to almost 30 cm^{-1} for tri-layer and then centered at about 30 cm^{-1} for quad-layer. Both the low- and high-frequency regions in the measured Raman spectrum conform to the literature.



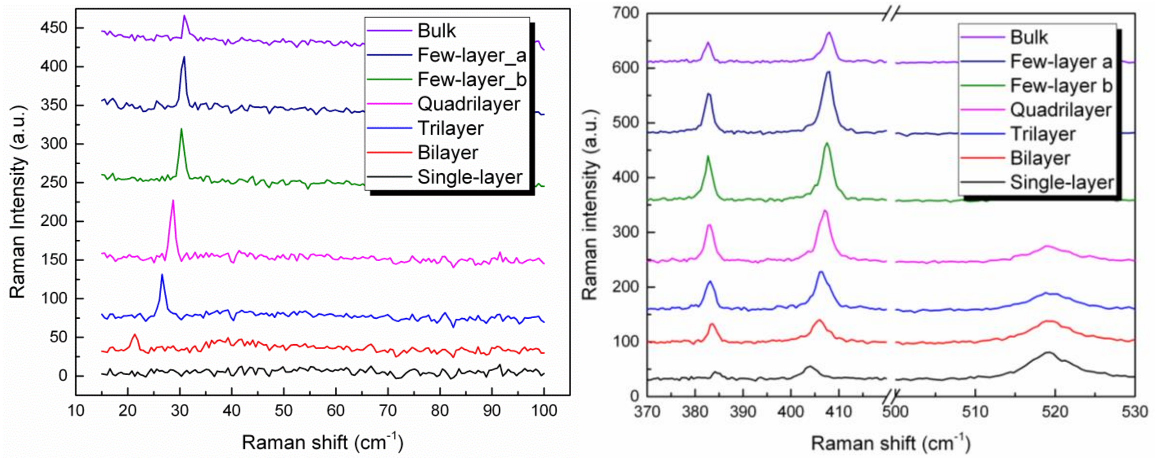


Figure 1.4 (Upper) a tiered MoS_2 sample on Si/SiO_2 substrate; (lower) low and high frequency thickness-dependent Raman spectra.

1.5 2D heterostructure assembly

1.5.1 The 2D material alignment and transfer tool

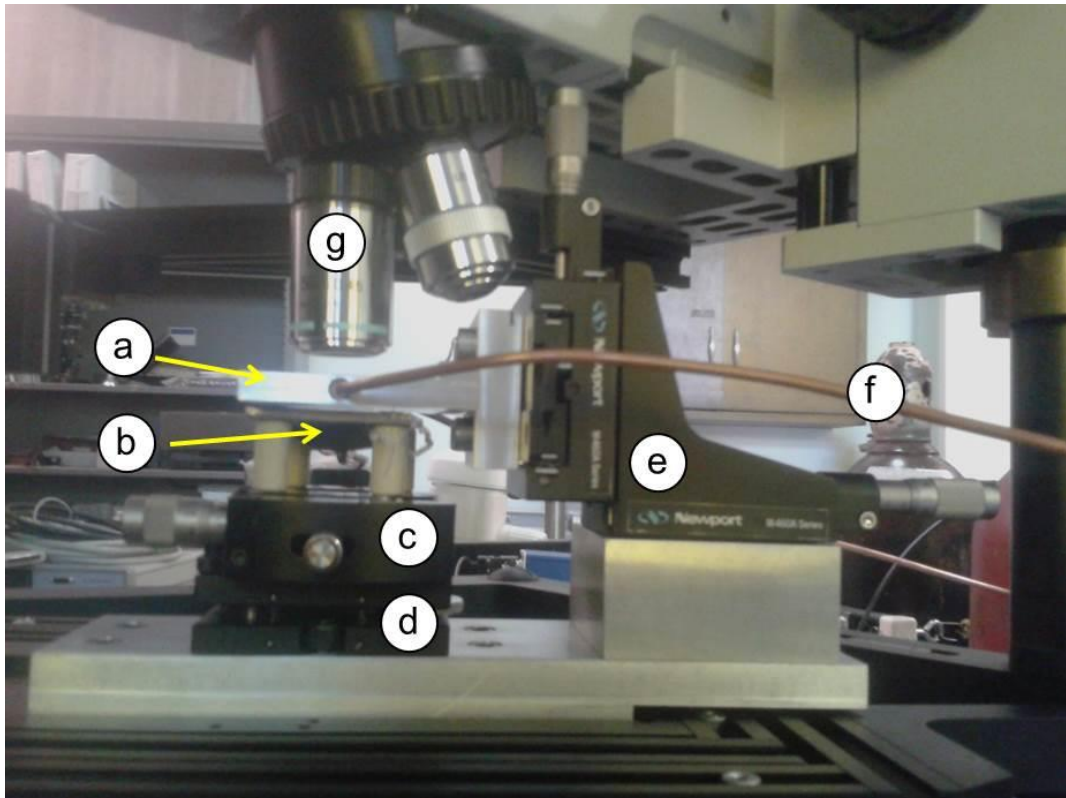


Figure 1.5 (a) upper sample stage; (b) lower sample stage with heating filament at the back; (c) rotational stage; (d) tilt stage; (e) XYZ stage with micrometers for moving the upper sample stage; (f) copper tube connected to a vacuum pump (g) microscope objectives (8x for coarse, 50x for fine focusing)

A dual fluorescence microscope is modified for using as the 2D material alignment and transfer purpose. Figure 1.5 shows the objective lenses of the upper part of the microscope and the mechanical device, attached onto the original sample stage of the dual microscope for precise sample alignment. The aluminum plate serves as the upper sample stage. The invar plate, which has a low coefficient of thermal expansion to reduce drift during transfer, is the lower sample stage with a heating filament coil sealed at the backside. It is designed so that the lower sample stage can be heated up during material transfer, which would help improve the adhesion of the transferred 2D material onto the substrate, though the majority of the transfer was carried out at room temperature. The central hole of the lower stage is connected to a vacuum pump through copper wires, so does the upper sample stage. The rotational and tilt stages are for leveling the upper and lower sample stages, so that the two are in exact parallel position. The XYZ stage with micrometers attached to the ends is for moving the aluminum plate at the point of sample alignment. The movement of the invar plate, together with the entire mechanical device, is however controlled by the two screws attached to the original microscope sample stage.

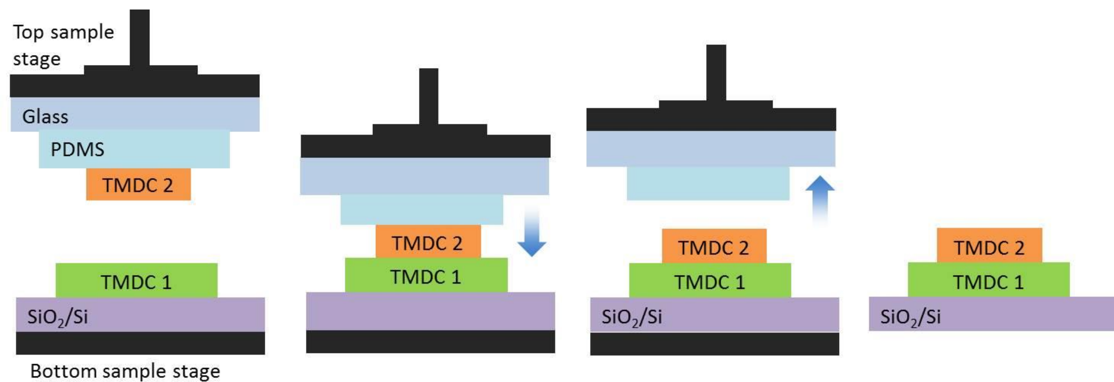


Figure 1.6 (left to right) an illustration of the solvent-free 2D material transfer procedure

A solvent-free all-dry transfer procedure has been applied to assemble 2D heterostructures [19]. As shown in Figure 1.6, one type of TMDC material is firstly exfoliated onto a Si/SiO_2 substrate. A second type is separately exfoliated onto a PDMS film, which was earlier affixed onto a glass slide. By checking through the microscope of the transfer tool, TMDC 2 is moved to the desired location and aligned with TMDC 1. Then the two samples are brought into contact as the top sample stage is gradually moved downward. Because of the van der waals force induced in between the two TMDC samples, the stack would remain on the main SiO_2 substrate even the top sample stage begins to move upward. Eventually, the stack is totally released from the PDMS film and ready to be retrieved from the bottom sample stage. As no solvent is involved in the whole transfer procedure, this technique ensures the cleanliness of the 2D material interface, which is critical for obtaining functional electronic devices.

1.5.2 MoS_2/h-BN heterostructure assembly standard operating procedure

1. Turn on the light source that leads to the upper part of the dual microscope. A light spot will appear on the lower sample stage (the invar plate). To prepare the transfer device for maximizing the room of movement, turn the two screws attached at the sides of the black sample stage, till the light spot overlaps the vacuum point of the invar plate. Then turn the micrometers to adjust the position of the upper sample stage, till the light spot is almost centered in its square opening.

2. Apply the mechanical exfoliation method to prepare h-BN on SiO_2 substrate. h-BN flakes in few nanometers usually show different shades of blue. The thinner it gets, the lighter the blue will become. Clean a piece of glass slide use acetone and IPA and blow-dry with N_2, leaving as few particles as possible. Cut a piece of the PDMS-based gel film (~ $1cm^2$), remove its protective layers, and gently lay the gel-film in the middle area of the glass slide. Try to get as few air bubbles trapped as possible. Then apply the mechanical exfoliation of MoS_2 directly onto the gel-film. An example of a MoS_2 flake left onto the gel-film is shown in Figure 1.7b. Few-layer MoS_2 usually has a dim color (light brown) on this transparent stamp.

3. Put the h-BN/SiO_2 sample onto the lower sample stage, use 8x objective lens to locate its position, use a tweezer to push the sample to the middle of the field of view, and then double-check its location under 50x. Turn on the vacuum pump so

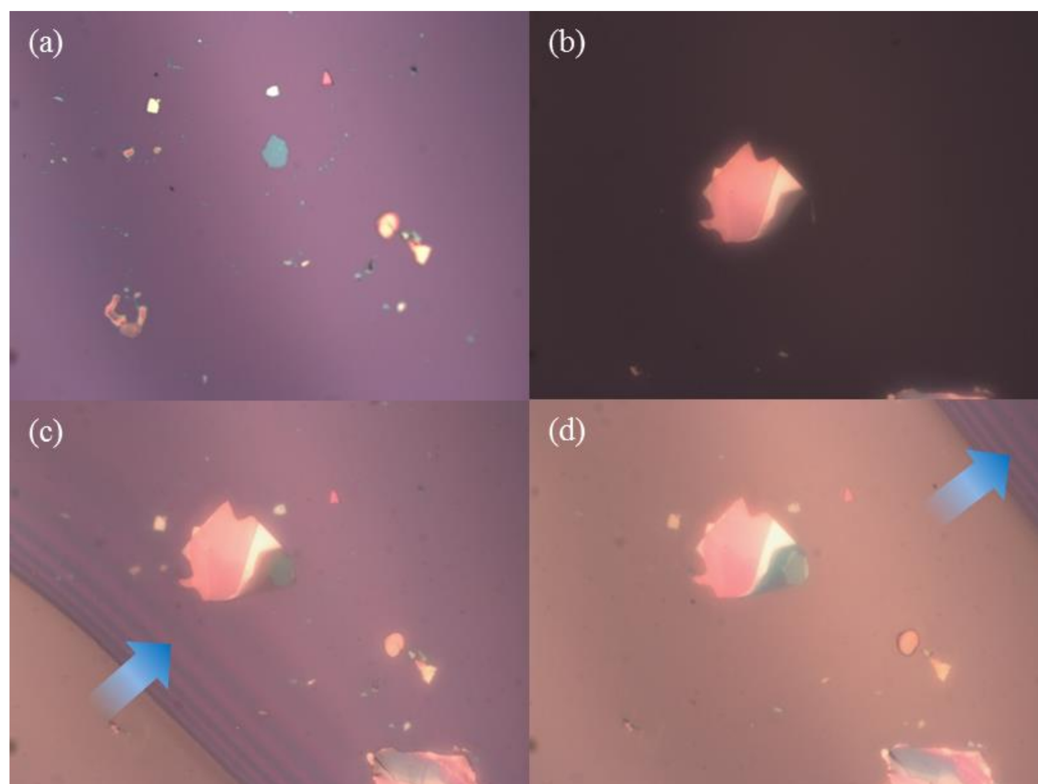
that the location of h-BN is secured. Next, insert the glass slide with the targeted MoS_2 into the mechanical device and attach it to the vacuum chuck of the upper sample stage (the gel-film is facing down). Center the MoS_2 flake in the field of view under 8x, then double-check at 50x.

4. Move down the upper stage till there is about 3 to 5 mm spacing between the SiO_2 substrate and the gel-film. Adjust the position of the objective lenses, now the two flakes can be seen on the same computer screen though at different lengths of focus. Adjust the position of the MoS_2 by turning the XYZ micrometers till it is aligned with the h-BN flake at the bottom. Then move down the upper stage further. Adjust the alignment further. Repeat the above steps carefully till both the h-BN and MoS_2 flakes come into focus. At this point the upper and lower stages are extremely close, and no spacing can be seen by visual inspection from a side view.

5. Move down the upper stage further, now the upper and lower stages are in contact. In Figure 1.7c, the light brown indicates the area where the gel-film is already in contact with the SiO_2 surface. The rest purple color indicates the area that the contact has not happened. Turning the z-axis micrometer to lower the upper stage further, you will see the boundary line that separating the two areas is gradually sweeping over the 2D stack (the blue arrow points the direction of movement). Once it has passed the stack for some distance like in Figure 1.7d,

loosen the z-axis micrometer a little to slowly move the upper stage in the reverse direction. In the second sweep across the 2D stack, make the motion of the boundary line as slow as possible, this is to prevent the stack from being separated again (Figure 1.7e, f).

6. After the gel-film is completely detached from the SiO_2 surface, raise the upper sample stage further apart from the bottom stage. Figure 1.7g shows how the stack looks like after the transfer but still seen through the gel-film. Now, hold the glass slide with hands and close the vacuum valve to the upper stage only. Take out the glass slide. Turn off the pump. Now the 2D stack is ready to be retrieved as shown in Figure 1.7h.



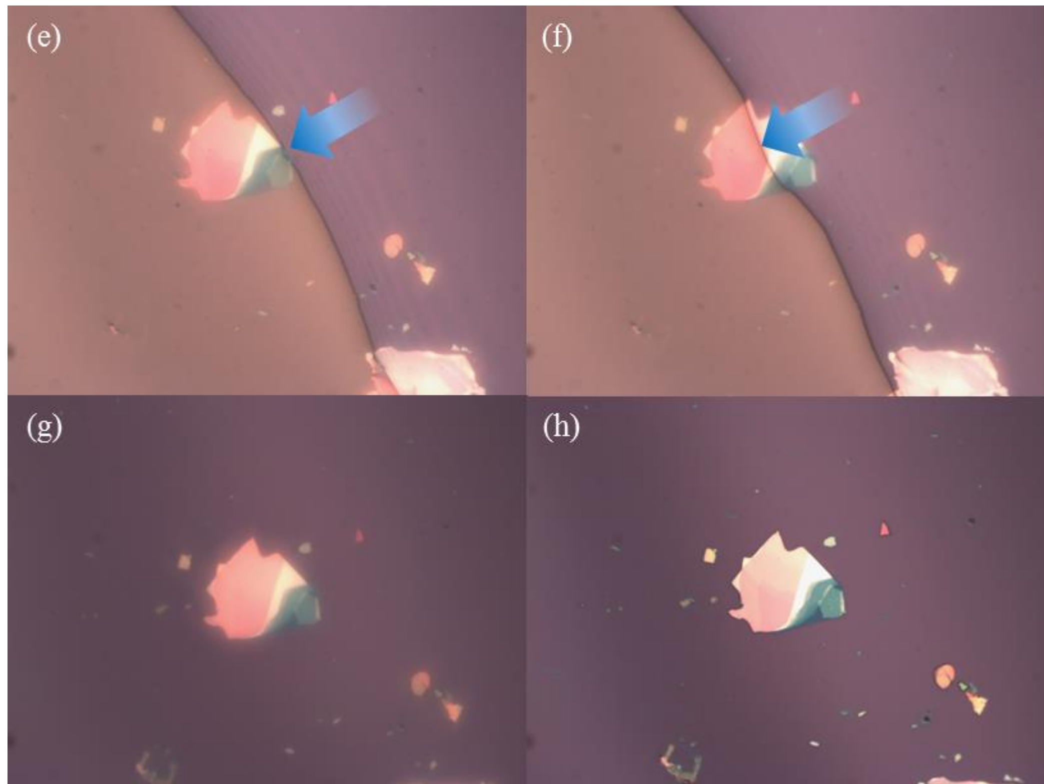


Figure 1.7 the solvent-free transfer procedure for assembling MoS_2/h-BN heterostructure (a) h-BN exfoliated on Si/SiO_2; (b) MoS_2 exfoliated onto PDMS-based gel-film (c - f) the motion of the boundary line separating the area where the contact has occurred and where it has not; (g) the 2D stack after transfer, seen through the gel-film; (h) the 2D stack after the gel-film and the glass slide are taken out of the transfer tool .

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Chapter 2 Electrical Characterization of the "Bottleneck" Effect in MoS_2 Field-effect Transistors

2.1 The prospect of MoS_2 UTB MOSFET

From the standpoint of mainstream IC manufacturing, newly introduced two-dimensional (2D) semiconducting transition metal dichalcogenides (TMDs), represented by molybdenum disulfide (MoS_2), may turn out to be the game changer in the relay of MOSFET downscaling process. Field-effect transistors (FET) made on atomically-thin MoS_2 flakes strike a notable resemblance to ultra-thin-body (UTB) MOSFET, in which the largely reduced Si body thickness minimizes the drain-to-channel capacitance, making the transistor less susceptible to "V_t roll-off" in gate length scaling [1]. Compared with silicon, MoS_2 FET can be regarded as a more cost-effective solution to silicon UTB device. Given the natural fully-terminated surface, processing steps to be developed for eliminating the dangling bonds can be circumvented. Besides, high quality and large area synthesis of the material from single- to few-layer has also been demonstrated in industry-compatible techniques such as chemical vapor deposition (CVD) [2–6] , most recently, metal-organic CVD [7, 8]. However, the carrier transport property of MoS_2, which determines the frequency response of a device, is still highly controversial.

2.2 Frequently cited performance metrics of MoS_2 FET

In order to realize high performance MoS_2 MOSFETs, three major issues needs to be completely addressed: one, how to achieve a low-resistivity metal-semiconductor junction; two, how to achieve high-quality interface between 2D crystal and dielectric; and three, device performance at scaled dimensions [9]. The first two questions need to be solved at device preparation so that the intrinsic characteristics of MoS_2 can be derived. Most commonly applied metrics for assessing the switching behavior of MoS_2 FET are:

- Field-effect mobility (μ_{FE})

$$\mu_{FE} = \frac{L}{WC_{ox}V_{DS}} g_m, \ \ (g_m = \frac{dI_D}{dV_G}, C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{d_{ox}})$$

Mobility describes carrier transport in low electric fields for micro-meter long channel. The above equation may underestimate the true channel field-effect mobility due to contact resistance [10]. 4-point probe measurement technique can eliminate the effect of contact resistance, in which case, V_{DS} represents the inner probe voltage drop, and L designates the channel length between the inner voltage probes.

- Current On/Off ratio (I_{ON}/I_{OFF})

Measured in the log plot of the transfer curve, a high current On/Off ratio is required for low static power dissipation as in Si MOSFET.

- Sub-threshold swing (SS)

$$SS = \frac{dV_g}{d(\log G)} = \left[1 + \frac{(C_S + C_{it})}{C_{ox}}\right]\frac{kT}{q}ln10$$

C_S is the capacitance in the MoS_2 conducting channel. $C_{it} = qD_{it}$, refers to the capacitance owing to the interface traps of density D_{it}. The minimum sub-threshold swing for ideal MOSFET = $\frac{kT}{q}ln10$ = 60 mV/dec [11].

2.3 Factors affecting the field-effect mobility of MoS_2

The field-effect mobility of MoS_2 is found dependent on both intrinsic and extrinsic factors: firstly, the number of layers [12]; secondly, the MoS_2-dielectric interface, encompassing the substrate effect [13-15], over-layer dielectric passivation [16-18] and the ambience for measurement [19, 20]; thirdly, the metal-semiconductor (M-S) interface at the contact region [12, 21]. Contrary to popular perception, contacts often play a more crucial role in nanoscale electronics than the semiconducting material itself. Sizeable Schottky barriers at the metal/semiconductor interface limit the current output of the FETs which leads to largely underestimated values for the mobility of the charge carriers. The importance of having ohmic contacts lies in that the contacts must be able to supply the necessary device current, and the voltage drop across the contact should be small compared to the voltage drops across the active device regions, so that the electrical performance is not degraded by device fabrication issues. Also, higher contact transparency reduces the required bias voltages for operation. Therefore, Schottky barrier

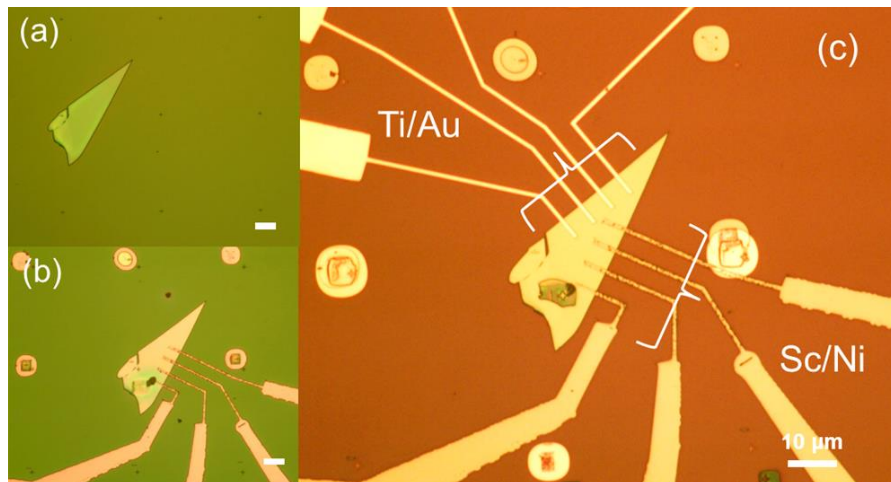
at both the source and drain electrodes is identified as the key debilitating factor, namely, the "Bottleneck" to achieve exceptional device performance.

There are two ways of making an Ohmic contact, one, heavily dope the contact region of the semiconductor; two, reduce the Schottky barrier height through adjusting the work function of the contact metal. The former has been realized, though indirectly through ionic liquid-gating technique [22-24]. For the latter, Schottky model defines the barrier to the flow of electrons from metal to semiconductor $\phi_B = \phi_m - \chi_s$, if excluding any contamination or defect induced surface states [25]. MoS_2 crystals have an electron affinity approximately about 4.0 eV [26]. High work function metal such as titanium ($\phi_m = 4.3$ eV) and gold ($\phi_m = 5.1$ eV) will result a barrier height of ~0.3 eV and 1.1 eV at M-S interface. Efficient carrier injection through Ohmic contact has been demonstrated in the case of scandium ($\phi_m = 3.5$ eV) since theoretically no barrier exists in the conduction band [12]. Experimental result has also shown that on a 20-layer exfoliated MoS_2 flake, mobility obtained from 2-probe measurement is considerably smaller by a factor of ~ 3, than the value from 4-probe measurement [27].

To establish a platform for comparing MoS_2 grown by different methods, it is necessary to understand how the nature of M-S junction affects the extraction of carrier mobility. Accordingly, we are able to judge whether the extracted mobility value truly reflects the intrinsic property of the material. Here, we utilize two exemplary contact metal combinations to create both Ohmic and Schottky junctions on the same MoS_2 sample, and characterize the discrepancy in transistor DC characteristics.

2.4 Experimental method

Pristine MoS_2 flakes were obtained through conventional Scotch-tape based mechanical exfoliation using bulk crystal. A degenerately boron-doped (0.001~0.005 Ω·cm) silicon substrate, with 285 nm SiO_2 capping layer, serves as the global back gate and gate dielectric. To mitigate the substrate effect, multilayer flakes in uniform color were chosen for device fabrication. Moreover, uniform color indicates the same number of layers across the entire sample area, negligible contamination and mechanical damage.



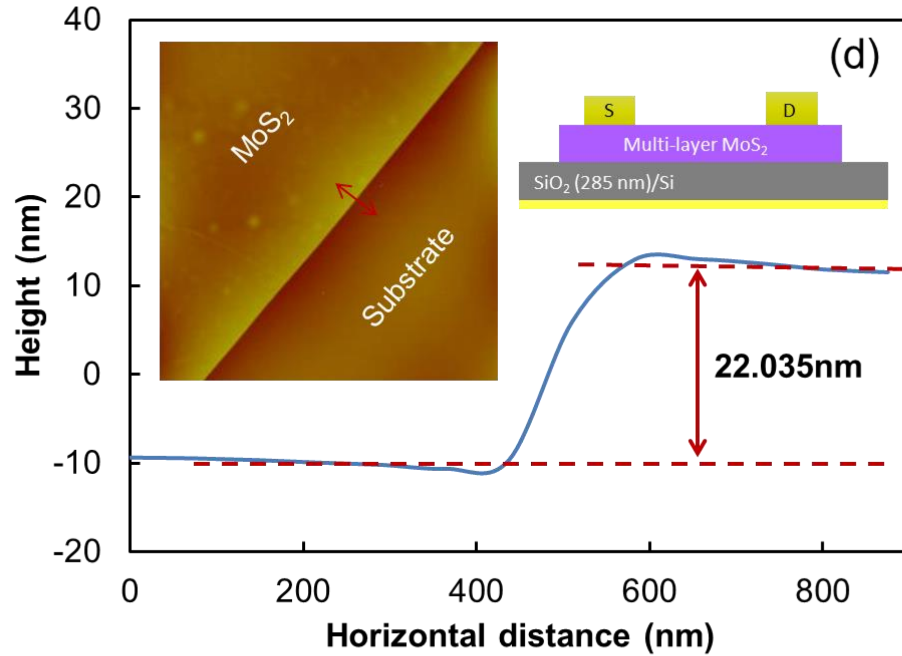


Figure 2.1 (a-c) fabrication steps and optical micrographs of a MoS_2 flake with contrasting metals as the surface contacts. (d) AFM height profile taken at the edge of the sample and FET schematic.

Figure 2.1 shows the optical image of the MoS_2 FETs. Through electron beam lithography and e-beam evaporation, two sets of FET with similar dimensions were fabricated on the same MoS_2 flake: Sc/Ni (60/40 nm) and Ti/Au (10/100 nm). Here, the top nickel layer protects the scandium from oxidation. The aspect ratios (W/L) of the channel area are: 6.4/4.7 μm and 5.8/4.8 μm for Sc/Ni- and Ti/Au-contacted FETs respectively (in short, Sc-FET and Ti-FET). All the electrodes, designed with a width of 1 μm, are arranged in-line with equal spacing. The sample thickness measured by atomic force microscopy (AFM) is ~ 22 nm, approximately 34 layers. A second Ti/Au contact was deposited at the backside of the substrate to finish the back-gated FET structure. No annealing was executed after lift-off. The device was characterized in a shielded probe

station connected to an Agilent 4155C semiconductor parameter analyzer. The entire measurement was carried out at room temperature in air.

2.5 Two-probe measurement

The transistor output profile I_D vs. V_{DS} was measured first to test the channel conduction. As shown in Figure 2.2, the output curves are symmetrical about the origin for both sets of device, implying that the source and drain electrodes were working properly and interchangeable. Under the same sweeping range of V_{DS}, clear rectification behavior is observed in the output plot of Ti - FETs, which tells the existence of a sizable Schottky barrier at Ti-MoS_2 interface. The current increases almost exponentially after a turn-on voltage (V_{on}) of ~1V, corresponding to ~ 2×10^3 V/cm inside the channel. K. Lee *et al.* [26] reported almost the same V_{on} in their transistor fabricated on a liquid-exfoliated MoS_2 sample. In their device, the channel was in direct contact with 10 nm chromium adhesion layer, which is also a high work function metal. In contrast, Sc - FET gives much more linear output profiles as shown in Figure 2.2a. The current density measured at the same drain bias is increased by ~10 times. The small bending may originate from some surface states at the M-S interface, though the real cause behind is not known yet. At this point, our experimental result confirms carrier injection from metal to MoS_2 is more efficient when Schottky barrier height ("Bottleneck") is largely reduced by utilizing a low work function metal.

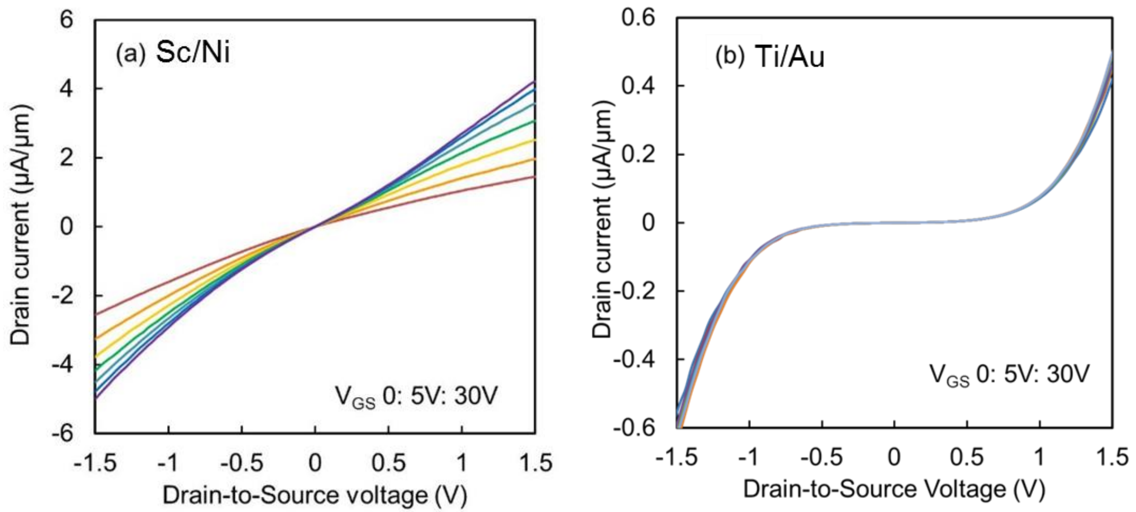


Figure 2.2 I_D vs. V_{DS} measured at different back-gate voltages from transistors contacted by (a) Sc/Ni (b) Ti/Au. Each of the above output characteristic was obtained at a constant V_{GS}, increasing from 0V to 30V in a step of 5V.

Next, two representative transfer plots, one from each set of the FETs, are shown in Figure 2.3. V_{DS} was set extremely small to capture the initiation of carrier transport across the Schottky barrier. With scandium contact, distinctive unipolar gate transfer characteristic can be observed at a drain bias as small as 5 mV. For Ti-FET, the boundary between On/off states is rather indefinite. Transfer curves measured at V_{DS} = 100 mV are added to highlight the contrast in current density. At the same back-gate voltage (e.g. V_{GS} = 20V), the gap in current density between these two groups of FET reaches nearly 500 times.

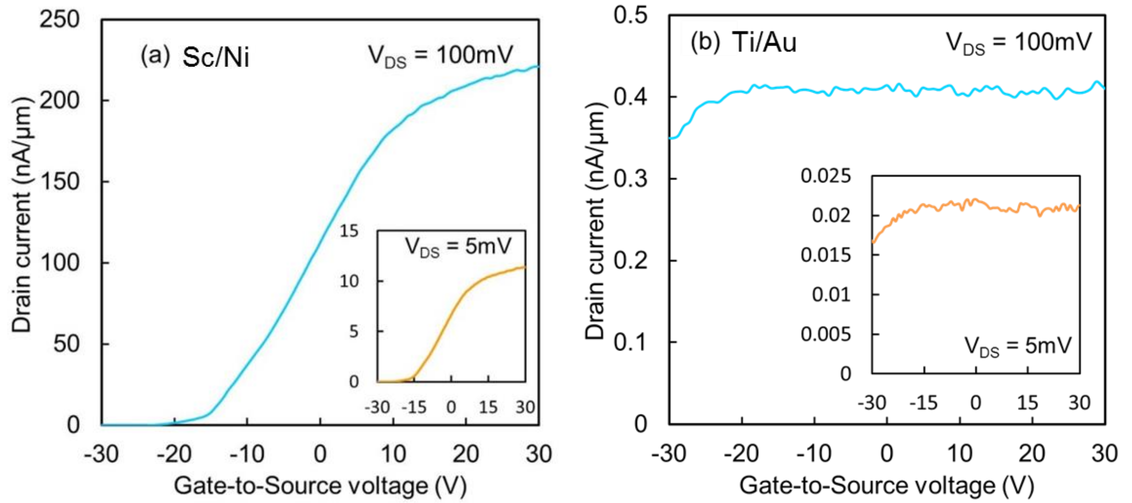
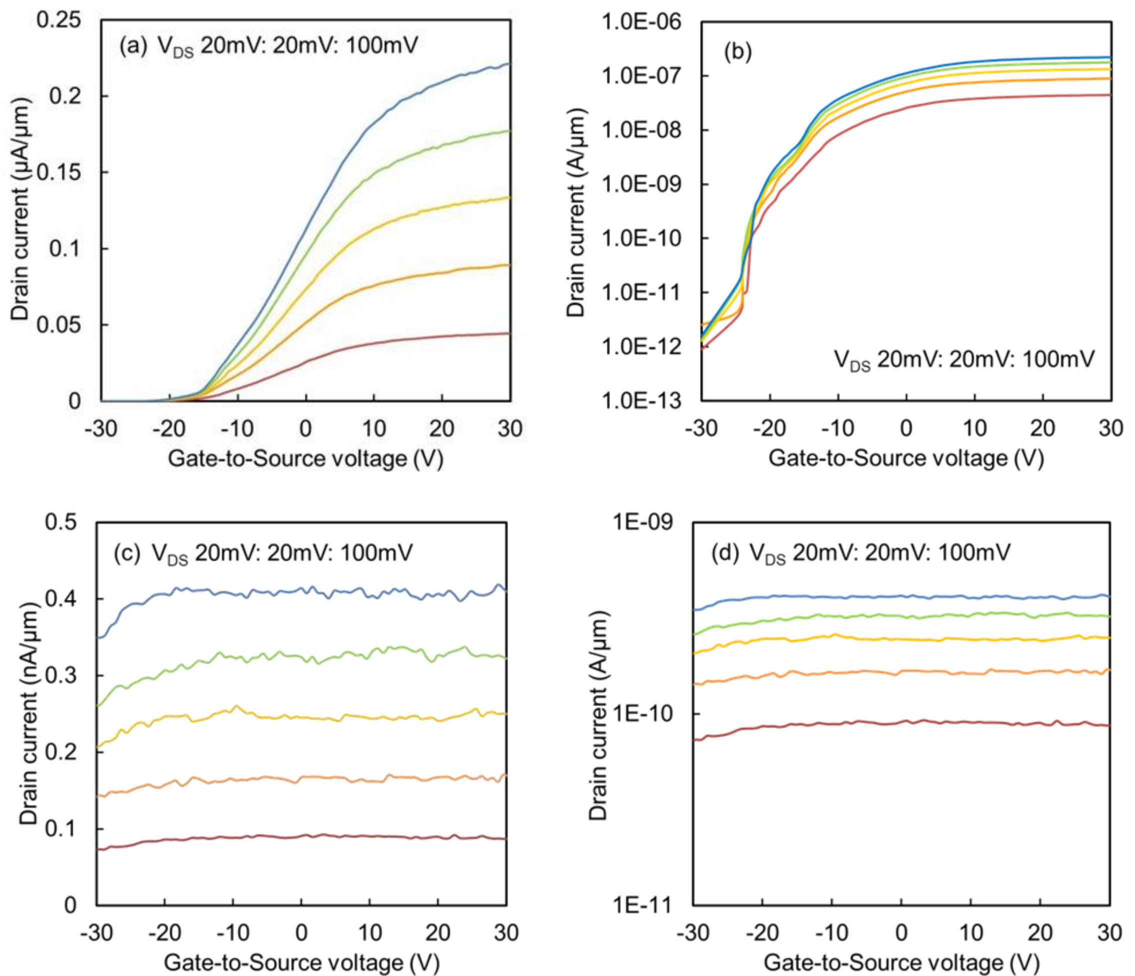


Figure 2.3 I_D vs. V_{GS} measured at two representative drain-to-source voltages, 100 mV and 5 mV, from transistors contacted by (a) Sc/Ni (b) Ti/Au. The axis labeling of the inset figure is the same as that of the main figure.

The full palette of gate transfer characteristic is shown in Figure 2.4. In all our devices, the upswing of the current at positive gate voltages clearly signals n-type conduction behavior, owing to accumulation of electrons [28]. Figure 2.4a and b are obtained from Sc - FET. The On-state current is reaching 200 nm/µm at V_{DS} = 100mV, and the current On/Off ratio is ~ 10^4 to 10^5 for a V_{DS} range from 20mV ~ 100mV. The threshold voltage obtained through linear extrapolation method [29] is -14V±0.5 for all the drain biasing conditions in Figure 2.4a, and it does not change noticeably with V_{DS}. From that, the carrier concentration at zero gate voltage $n_{2D} = C_{ox}(V_{GS} - V_{th})/q$ is 1.05×10^{12} cm^{-2}.

Figure 2.4c and d are from Ti-FET. Given the same biasing condition as those for Sc - FET, the "On" and "Off" states could not be distinguished. Because of the considerable Schottky barrier, the Ti-FETs have to be biased beyond the 1V so as to

produce identifiable switching characteristics (Figure 2.4e and f). In Figure 2.4f, we observe clearly the decay of current On/Off ratio: when V_{DS} is set at 2V, the On/Off ratio is about 100 times. The value is reduced to only ~ 10 times, when V_{DS} drops to 1V, and much smaller than 10, when V_{DS} is further reduced to 200 mV. The subthreshold swing is relatively large for both FET groups. The minimum is approximately 6V/dec at V_{DS} = 100mV. Thinning the gate oxide is one solution for sharpening the subthreshold swing [1]. All FETs operate in depletion-mode as the drain current is sizable at zero gate voltage.



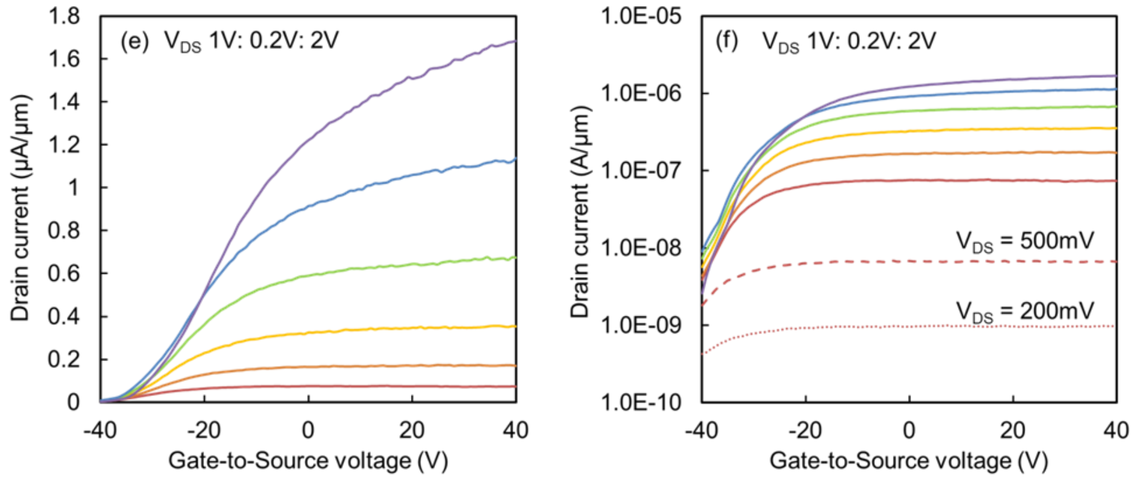


Figure 2.4 I_D vs. V_{GS} measured at different drain-to-source voltages. Transfer characteristics of transistors with Sc/Ni contacts are plotted in (a) linear scale (b) log scale; that of transistor with Ti/Au contacts are plotted in (c) linear scale (d) log scale. For the former, V_{DS} was set less than 100mV to stabilize the transistor in linear operating region, for the latter, the minimum V_{DS} that produces a clear switching behavior was found ~ 1V, due to a turn-on voltage of 1V observed in the rectified output current (e, f).

Multiple data points of the field-effect mobility were collected to capture the trend. Each mobility value was obtained firstly by fitting to each transfer curve and then calculated by applying the following equation:

$$\mu_{FE} = \frac{L_{DS}}{W C_{ox} V_{DS}} \left(\frac{dI_D}{dV_{GS}}\right)$$

where $C_{ox} = 1.2 \times 10^{-8}$ F/cm^2 is the capacitance per unit area of the 285 nm-thick SiO_2 dielectric layer. L_{DS} emphasizes that at 2-probe measurement the channel length is the entire distance between source and drain. Note that the maximum value of the slope dI_D/dV_{GS} was used in the calculation. Figure 2.5a shows mobility extracted from Sc-FETs is nearly constant at 35.4 ± 2.5 cm^2/Vs with respect to V_{DS}, whereas, those from Ti-FET fluctuate around an average value of only ~0.09 cm^2/Vs. When V_{DS} is increased

further, the mobility trend becomes regulated, increasing with the drain voltage up to 9.4 cm^2/Vs at V_{DS} = 2V.

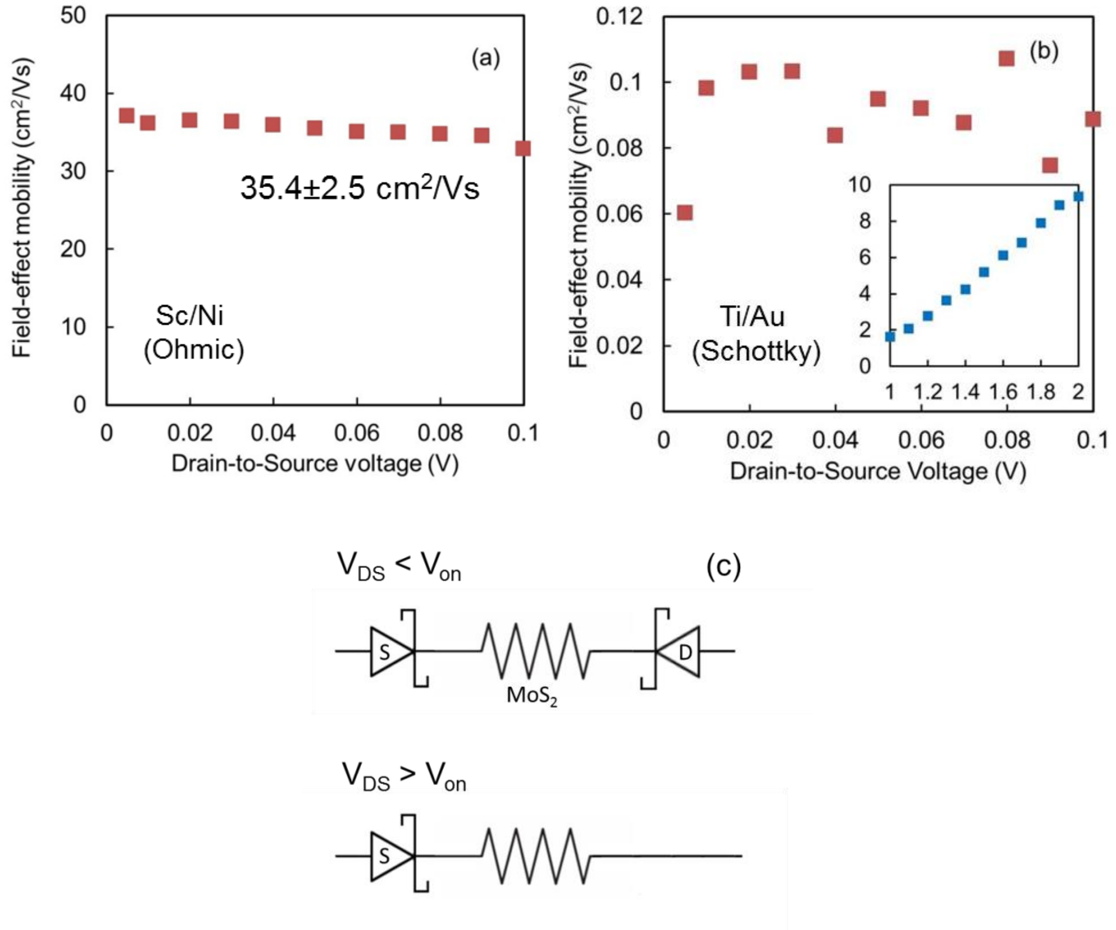


Figure 2.5 Extracted values of field-effect mobility at multiple drain biasing condition from FETs (a) with Sc/Ni contact (b) with Ti/Au contact. Inset: mobility values extracted from extended range of V_{DS}. (c) A circuit model of the top contact structure illustrating the "Bottleneck" formed at metal/2D semiconductor interface. The forward-biased junction at high V_{DS} explains the change of the trend of the mobility values – from disordered to monotonic.

The turning point shown in Figure 2.5b coincides with the turn-on voltage of Schottky barrier estimated from the output plots, implying that the "Bottlenecks" was in action (Figure 2.5c): when $V_{DS} < V_{on}$, the channel conduction is dominated by the back-

to-back connected Schottky diodes. And the current obtained is mainly contributed by thermionic emission process. When $V_{DS} > V_{on}$, one of the Schottky diode is now in forward bias, the effective barrier height in MoS_2 drops by qV_{MS}, where V_{MS} is the applied voltage. Electron flowing from the semiconductor into the metal thus gets boosted by a factor $\exp(qV_{MS}/kT)$ [25]. Furthermore, the reverse-biased junction will be loaded with the most of the potential drop. Thermally assisted tunneling current through the triangular Schottky barrier will be enhanced as the barrier width now becomes narrower for electrons to pass through. The "M-S-M" model was earlier employed at explaining the contact barrier observed in FET fabricated on liquid-exfoliated MoS_2 [26] and CdS nanowire [30].

2.6 Four-probe measurement

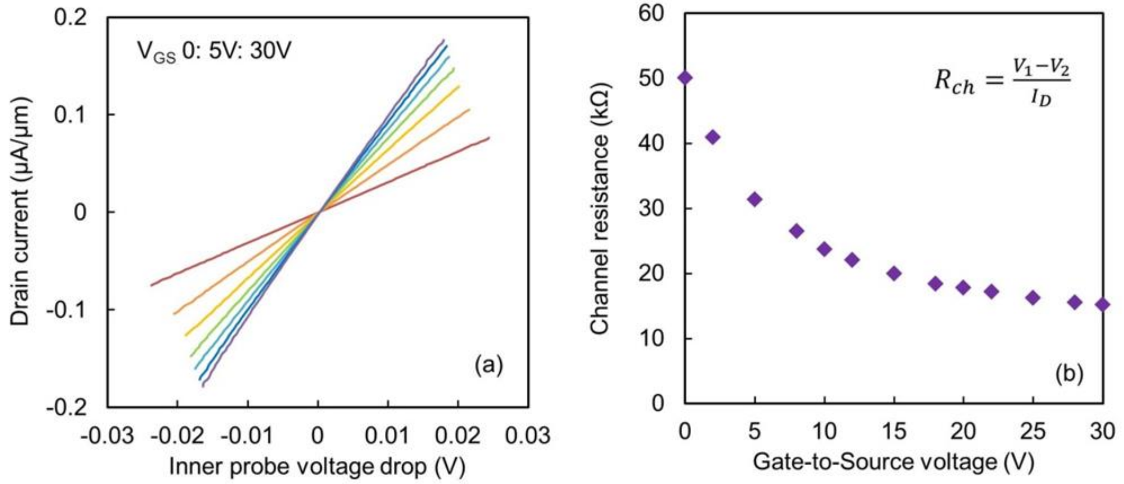
To probe the intrinsic mobility of the MoS_2 flake, we proceeded to gated 4-probe technique [31] which allows conductivity measurements with screened-out disturbances from contact resistance. Of the four scandium electrodes, the outer two serve as the stimulus probes, and the inner two are the voltage monitor probes. As shown in Figure 2.6a, the I_D - V_{DS} curves from 4-probe measurement become completely linear comparing with the 2-probe measurement results in Figure 2.1a. Thus, the channel resistance (R_{ch}) can be accurately determined by inverting the slope of the I_D - V_{DS} plot. A clear descending trend of R_{ch} with respect to V_{GS} confirms that the pristine MoS_2 sample is n-type. The non-linearity is probably associated with the gate-dependent interlayer

resistance in a multi-layer two-dimensional system: different numbers of interlayer resistors are involved at different back-gate bias conditions [32].

The measured channel conductance (G) is computed as $G = I_D/(V_1 - V_2)$. Figure 2.6c shows that all the conductance curves measured at different drain voltages almost overlapped with each other, from which, the intrinsic mobility is extracted by [33]:

$$\mu_{FE} = \frac{L_{in}}{W C_{ox}} \left(\frac{dG}{dV_{GS}} \right)$$

Where L_{in} is the distance between the inner voltage probes. We observe not only a steady trend, but also a ~ 4-fold increase of the mobility to 140.6 ± 1.2 cm^2/Vs. The stability and improved magnitude of the mobility manifests the intrinsic property of the MoS_2 sample.



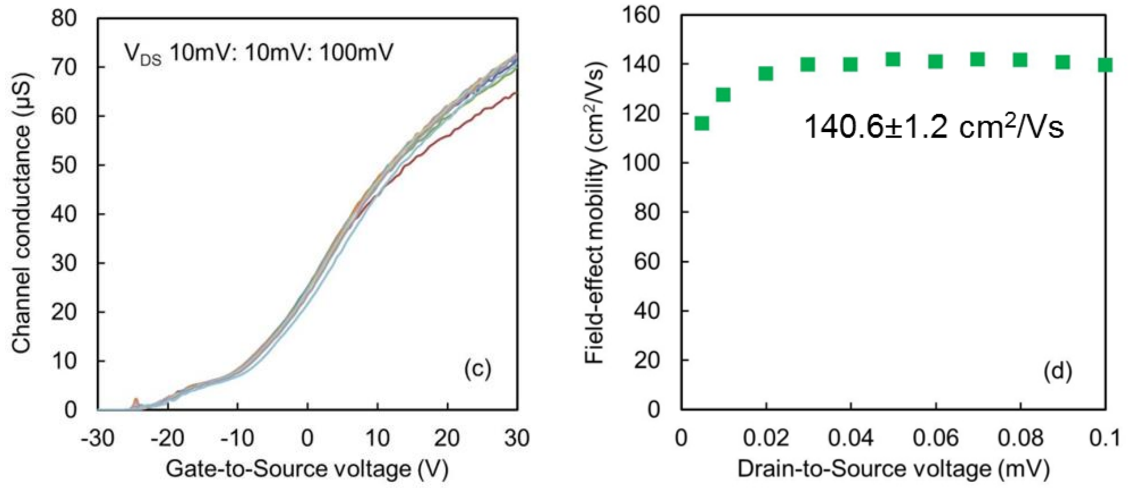


Figure 2.6 Electrical characteristics by gated 4-probe measurement on transistors with Sc/Ni contact. (a) Output profile at different back-gate voltages. (b) Channel resistance extracted from the inverse of the slope of the output curves. (c) Channel conductance vs. gate voltage when different V_{DS} is applied at the outer two electrodes. (d) Field-effect mobility extracted from (c).

Transmission line method (TLM) is applied to estimate the contact resistance of the Sc-FETs. As shown in the inset of Figure 2.7, electrode No. 1 is designated as the reference, then FETs with different channel length can be obtained between electrode pair 12, 13 and 14. The total channel resistance, calculated by inverting the slope of the I_D - V_{DS} plot, follows the relationship [29]:

$$R_T = \frac{R_S}{W} L + 2R_C$$

From the slope and the y-intercept, the total contact resistance from a single M-S junction is approximately is 57.6 kΩ (~ 0.37 MΩ · μm) and the sheet resistance of the MoS_2 channel is 31.9 kΩ/□.

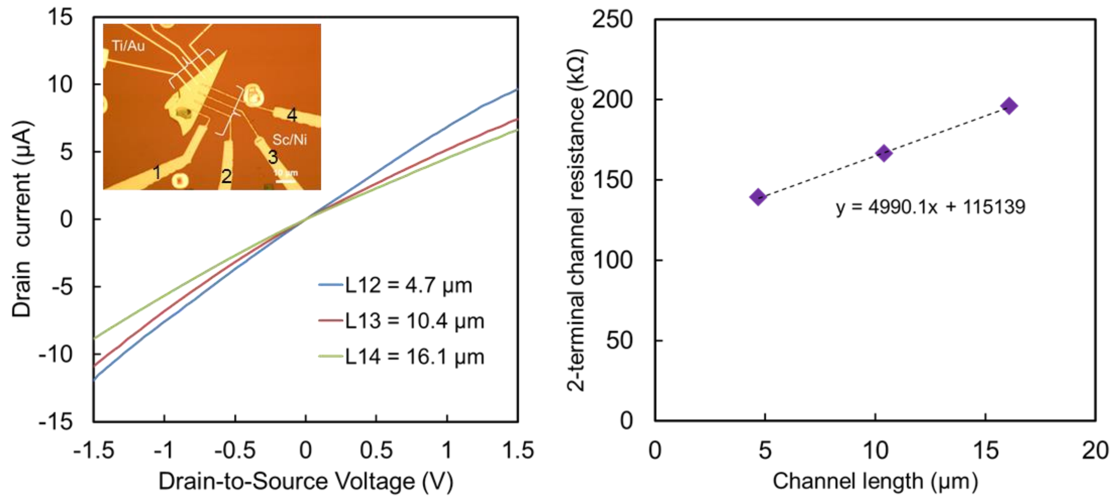


Figure 2.7 (left) I-V measurement coupling electrode pair 12, 13 and 14; (right) the 2-terminal channel resistance at different channel length for extracting contact resistance

For scandium contacted FETs alone, we notice a significant improvement in carrier mobility when switching from 2-probe to 4-probe measurement (Table 2.1). This implies that there are other factors at M-S interface that contribute to the total contact resistance, apart from the impedance of Schottky barrier.

Contact metal & measurement technique	Field-effect mobility (cm^2/Vs)
Ti (2-probe)	0.09 ± 0.017
Sc (2-probe)	35.4 ± 2.5
Sc (4-probe)	140.6 ± 1.2

Table 2.1 A summary of the extracted mobility values

Firstly, it is necessary to point out that a Schottky barrier height of ~30 meV [12] still exists even in the case of scandium due to Fermi level pinning to the conduction

band of MoS_2; Secondly, in this back-gated FET structure, the source/drain electrodes are only contacting the surface layer of the MoS_2 sample, however, electro-static control from the back gate is stronger in the lower layers [32], in this regard, current spreading resistance (R_{sp}) in multi-layer MoS_2 may also become considerable.

2.7 Conclusion

From a device point-of-view, we have seen drastic difference in carrier mobility brought by different contact metal combinations. This indicates that non-optimal contacts can become the “bottleneck’ that hinders carrier transport, making transistors operate way below their intrinsic performance limit. A highly transparent M-S interface should be regarded as a prerequisite for stabilizing transistors in deep triode region and further mobility extraction. Because of its scarcity, scandium may not be the best choice for industrial implementation. Novel contact technique, such as edge contact, in combination with continuously improved material synthesis technique, would ultimately form the solid foundation for 2D semiconductor in future nanoelectronic devices.

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Chapter 3 Making One-dimensional Electrical Contacts to MoS_2-based Heterostructures through Plasma etching

3.1 Challenges brought by surface electrical contacts

"Surface contact", as frequently applied in MoS_2 FETs [1–3], means that the electrode metal is deposited on the very top layer of the 2D material. However, this type of contact structure exhibits several limitations. The first one is the phenomenon of Fermi-level pinning [4], meaning that the carrier injection is always constrained, though, to different extent, by the Schottky barrier formed at metal-semiconductor (M-S) interface. Low work function metal such as Sc [4], Al [5]and Ag [6] have been proved producing superior transistor performance than conventional high work function metal (like Ni and Au); the second limitation originates from the inherent surface defects found on natural MoS_2 crystal. High density of sulfur rich/deficient sites on a freshly exfoliated MoS_2 crystal render localized p- or n- type conduction and variation of the electronic properties from sample to sample [7]. In the case of surface contacts, this type of structural defects would be buried under electrodes in permanence. Thirdly, the thinning of MoS_2 nanosheet is possible in air due to its oxidation to form more insulating MoO_3 ($E_g > 2.7$ eV) [8, 9], inevitably hampering carrier transport and also making it very difficult to reproduce the same transistor performance.

Given the aforementioned limitations of surface contact, one-dimensional edge contacts can be highly advantageous compared to surface contacts in terms of electron injection efficiency [10]. The concept of edge contact was firstly applied to h-

BN/graphene/h-BN heterostructure [11], in which the contact resistance is reduced to as low as 100 Ω•μm and becomes independent of temperature. Etched-graphene has also been effectively used as an intermedium between electrode metal and TMD transistor channel for lowering the contact resistance [12, 13]. DFT calculations [14] on TMDs have shown that metallic states at the edge of MoS_2 can be viewed as one-dimensional conducting wires. Besides, edge contact ensures the connection of the electrode metal to all the layers of a TMD sample, hence current spreading resistance is expected to be largely reduced [15]. The conversion of 2H semiconducting to 1T metallic phase under contact region has also proved to be an effective way for generating Ohmic-like carrier transport across the M-S interface [16]. In essence, the phase-engineered contact structure resembles edge contacts, because the inlet for electron flow is constrained to the boundary line, from which the two phases are separated.

Here, as a proof of concept, we firstly present a new technique for fabricating edge contacts to a multi-layer MoS_2 sample encapsulated under Al_2O_3. Next, a solvent-free material transfer procedure is employed to sandwich single-layer MoS_2 in between two h-BN flakes, and edge contacts are made to this 3-level 2D material stack. In both types of heterostructure, the sites for edge contacts were initially opened by plasma etching and then filled with metal through evaporation. Distinguished from the graphene-mediated edge-contacts [12] in literature, in this study, the exposed edges of MoS_2 are in direct contact with metal. From the perspective of industrial implementation, the requirement of simultaneously having clean MoS_2-graphene and graphene (edge) - metal interfaces [13], can be made into one processing step by adapting MoS_2 (edge) – metal

contact structure. The devices in this paper were further characterized through back-gated FET configuration.

3.2 Experimental method

3.2.1 Fabrication of edge contacts on $Al_2O_3/MoS_2/SiO_2$ heterostructure

Figure 3.1 illustrates the procedure for burying MoS_2 under Al_2O_3 prior to device fabrication. Pristine MoS_2 flakes were obtained through conventional Scotch-tape based mechanical exfoliation using bulk crystal. A degenerately boron-doped (0.001~0.005 Ω•cm) silicon substrate with 285 nm SiO_2 capping layer, served as the global back gate and gate dielectric. Right after the exfoliation step, the MoS_2 sample on SiO_2/Si substrate was coated with 20 nm Al_2O_3 using ALD (Cambridge Nanotech Savannah 100) for full isolation from oxygen and any potential solvent contamination in fab. E-beam lithography (EBL) with MMA/PMMA bi-layer resist was further performed to define the electrode pattern. CF_4 Plasma etching (100 W/2 min, STS Reactive Ion Etcher) engraves the developed patterns into the Al_2O_3 film and exposes the edge of the MoS_2. Next, contact metals 40 nm scandium, followed by 20 nm nickel was evaporated (Temescal BJD 1800 system) to fill the trench. The edge contact structure was completed after the extra metal was removed by lift-off. A second Ti/Au contact (10/100 nm) was deposited at the backside of the wafer substrate to finish the back-gated FET configuration. No annealing was executed.

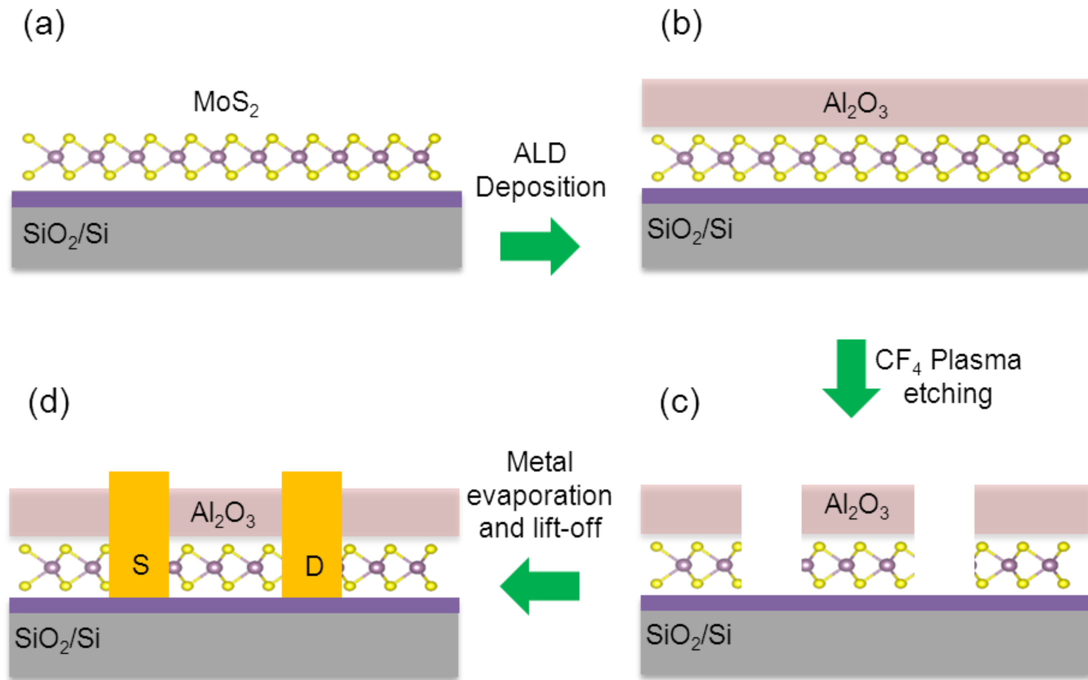

Figure 3.1 Schematic illustration of the fabrication procedure for creating edge contacts on MoS_2 with Al_2O_3 cover-layer.

"The passivation first, metallisation second" technique is applicable to both exfoliated and CVD synthesized 2D materials. A 7 nm MoS_2 flake identified through optical microscopy and Raman spectroscopy is chosen for device fabrication (Figure 3.2). It is very important to have sufficient metal fill up the contact trench to ensure the continuity between metal and the atoms at the exposed edge of MoS_2.

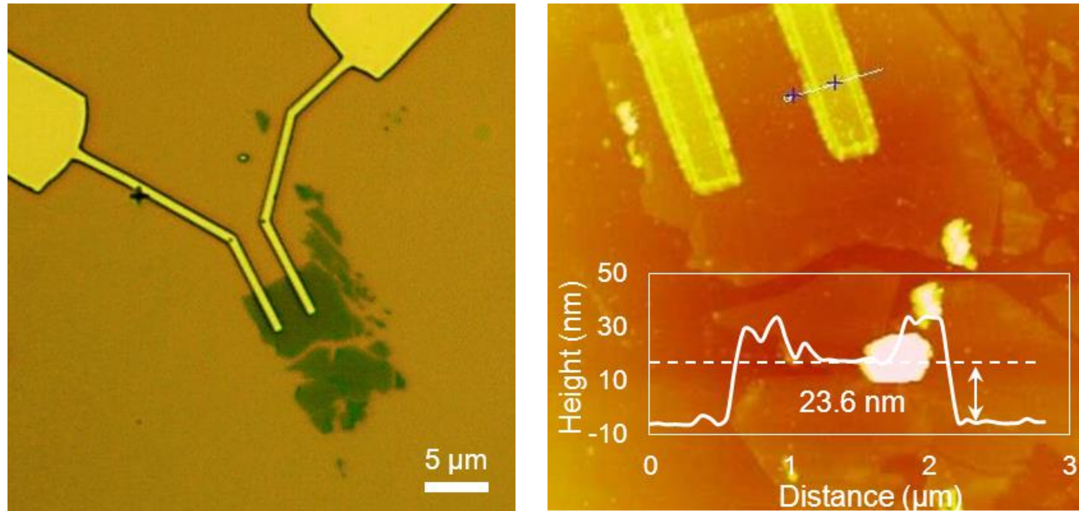

Figure 3.2 (left) an optical image of the edge contacts made on $Al_2O_3/MoS_2/SiO_2$ heterostructure; (right) AFM sectioning across the electrode shows an extra 23.6 nm of metal protruding out of the surface after trench fill-in.

3.2.2 Fabrication of edge contacts on h-BN/MoS_2/h-BN heterostructure

We applied similar dry transfer procedure [17] to assemble the 3-level stack (Figure 3.3). For the first step, h-BN powder (Momentive PT110) is exfoliated and pressed onto SiO_2/Si wafer using adhesive tape. A bulky h-BN flake (60 nm) was chosen as the under-layer, this is to mitigate the substrate effect that is due to surface states of the SiO_2 gate insulator [18]; Separately, MoS_2 is directly exfoliated onto a viscoelastic stamp affixed to a microscope glass slide. Fainter-coloured regions representing the thinnest flakes are located, confirmed later by Raman spectra after transfer (Figure 3.4). A micro-manipulator positions the MoS_2 flake over the h-BN under-layer, and then brings the two flakes into contact. Because MoS_2 adheres more strongly to h-BN than the stamp, the two-level stack remains on the wafer surface when the stamp is peeled off. The above procedure was repeated to transfer the top h-BN cover flake (21 nm). SF_6 plasma

generated by ICP (75 W/1 min, Oxford Plasmalab 100/180) etched through the stack of h-BN and MoS_2 to open the sites for edge contacts. The total thickness of the edge electrode Sc/Ni (60/40 nm) was increased to accommodate the thickness of the h-BN substrate for a complete trench fill-in.

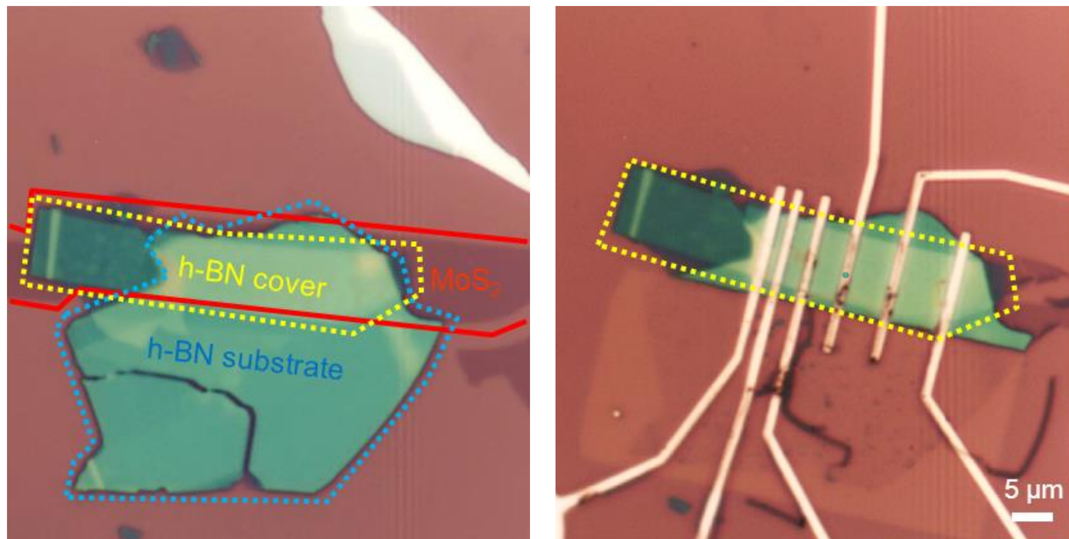

Figure 3.3 Optical images of the assembled h-BN/MoS_2/h-BN 3-level heterostructure before (left) and after (right) shaping by plasma etching.

3.2.3 Characterization

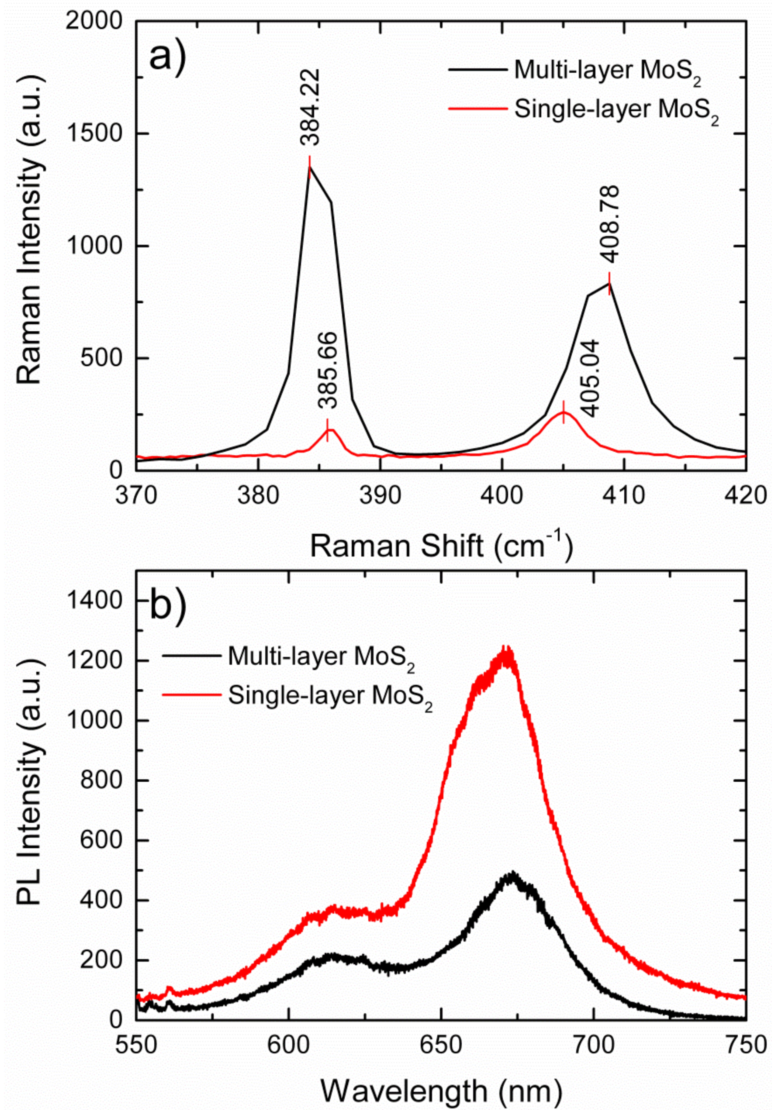

Figure 3.4 Raman and photoluminescence spectra of a 7 nm (11 layers) and a monolayer MoS_2 samples discussed in this chapter.

Raman and photoluminescence spectra were acquired under ambient conditions with a Horiba LabRAM HR spectrometer equipped with a 523 nm laser supply and an 1800 lines/mm grating. A 100x objective was used for focusing the laser to an

approximately 1 μm spot onto the sample. The laser power is < 1 mW to prevent sample heating. The Raman spectrum of the transferred MoS_2 shows the difference in the Raman shift between the in-plane E_{2g} (385.66 cm^{-1}) and out-of-plane A_{1g} (405.04 cm^{-1}) modes is 19.4 cm^{-1}, corresponding to monolayer MoS_2 [19]. The FETs was characterized in a shielded probe station connected to an Agilent 4155C semiconductor parameter analyser. The entire measurement was carried out at room temperature in air. Topography and thickness measurement were obtained with tapping mode atomic force microscopy (Multimode, Veeco).

3.3 Device performance of edge-contacted MoS_2 FETs

For the multi-layer back-gated MoS_2 FET (W/L = 4.7/2.4 μm) in Figure 3.2, after depositing 60 nm contact metal, AFM sectioning across the electrodes shows an extra 23.6 nm protruding out of the surface. Edge spikes ~ 10 nm high also appeared on the top surface of the electrodes, which is probably due to polymer re-deposition in the CF_4 etching step [20]. The surface of the electrodes can be considerably cleaned by an extra O_2 descum step, proving the carbon-rich nature of the re-deposited material (see Section 3.4). The transistor output profile I_D -V_{DS} was measured first to test channel conduction. As shown in Figure 3.5a, the output curves are symmetrical about the origin, implying that the edge contacts were functioning equivalently. Clear current rectification due to Schottky barrier is also observed, as the current increases exponentially after a turn-on voltage (V_{ON}) of ~ 0.3V, corresponding to 1.25×10^3 V/cm inside the transistor channel. The full palette of n-type depletion gate transfer curves are shown in Figure 3.5b. The

gate voltage ranging from -40 V to 40 V was swept with a constant $V_{DS} < 1V$. The On-state current density (I_{ON}/W) reaches 128 nA/μm at V_{DS} = 1V. Threshold voltage (V_{th}) obtained through linear extrapolation method [21] varies from -20 to 1 V at the set of drain biasing condition in Figure 3.5b.

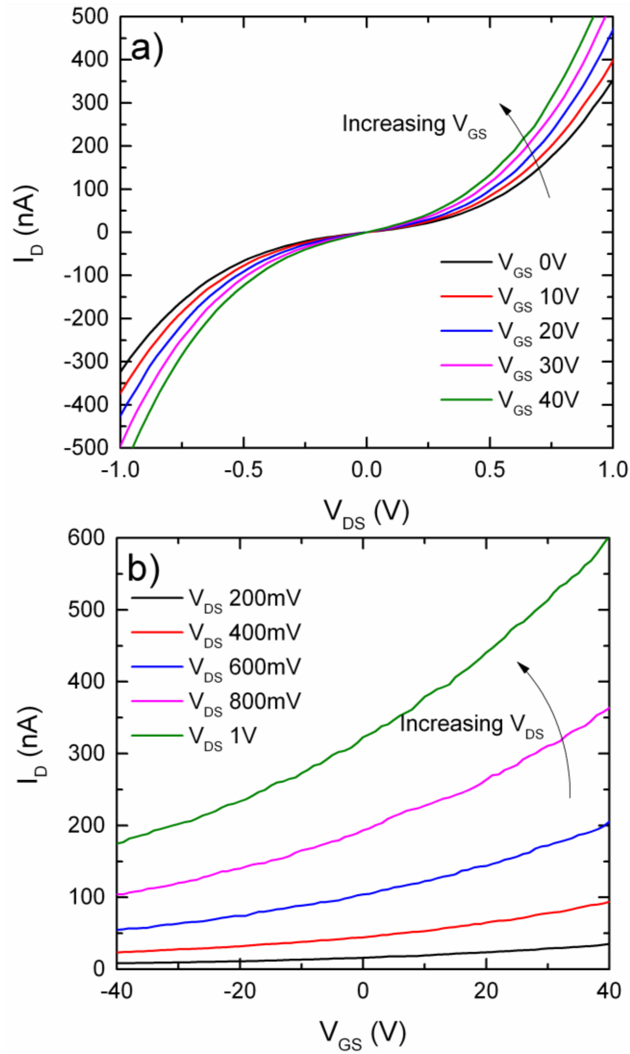

Figure 3.5 (a) output and (b) gate transfer characteristics of the $Al_2O_3/MoS_2/SiO_2$ back-gated FET with edge contacts.

The corresponding carrier concentration at V_{GS} = 40V, calculated using $n_{2D} = C_{ox}(V_{GS} - V_{th})/q$ is ~ 3 to 4 × 10^{12} cm^{-2}. Generally the subthreshold swing $SS = dV_{GS}/d(\log I_D)$ is relatively large, we believe it can be improved by thinning the gate oxide and optimizing the thickness of the Al_2O_3 encapsulation layer.

Alternatively, edge contacts can be fabricated to MoS_2 sandwiched in between h-BN. h-BN is a superior 2D insulator with a large bandgap of 6 eV, a dielectric constant of 3 - 4 and breakdown voltage ~ 0.7 V/nm, comparing favourably to those of SiO_2 [22]. The representative device performance (W/L = 6.5/1.8 μm) is shown in Figure 3.6, and summarized in Table 3.1. Comparing with the aforementioned multi-layer MoS_2 FET, most importantly, we observed Ohmic-like conduction in the output curves under non-zero gate voltage. A further SF_6 etching profile test on a multi-layer h-BN flake reveals a clean post-processing sample surface and smooth side walls, because of the formation of volatile etch product BF_3 [23] (see Section 3.5). For the gating characteristics, I_{ON} measured at the same drain bias is increased by 3 times. The device gives good current On/off ratio (10^4 ~ 10^5) and sub-threshold swing (~ 2 V).

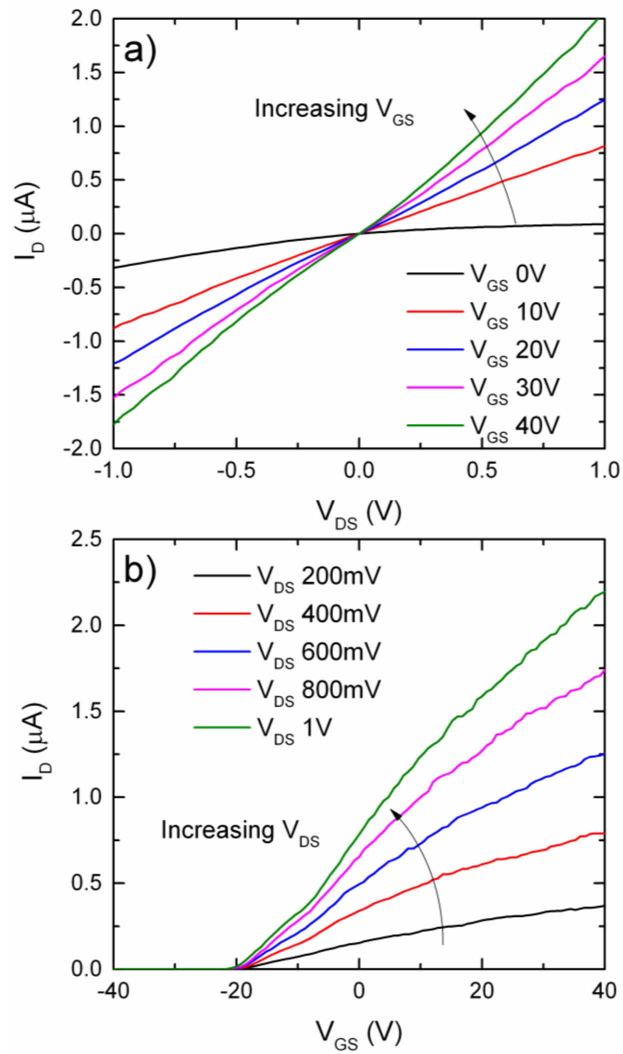

Figure 3.6 (a) output and (b) gate transfer characteristics of the h-BN/MoS_2/h-BN back-gated FET with edge contacts.

Type of heterostructure	Channel Material	ON current density* [nA/μm]	ON/OFF current ratio	Threshold voltage (V)	Sub-threshold swing [V]	Field-effect mobility** (cm^2/Vs)	Type of M-S junction observed
$Al_2O_3/MoS_2/SiO_2$	7nm (~11 L)	128	10	1 (V_{DS} = 200 mV) -20 (V_{DS} = 1 V)	> 20	4.2	Schottky
h-BN/MoS_2/h-BN	Monolayer	338	10^4~10^5	-20 (V_{DS} = 200 mV) -15.5 (V_{DS} = 1 V)	2	1.1	Ohmic

*At V_{DS} = 1 V, V_{GS} = 40 V
**At V_{DS} = 1 V

Table 3.1 Summary of device performance of MoS_2 FETs fabricated with edge contacts

Based on the electrical characterization data, we observed two contrasting output plots, corresponding to Schottky (Figure 3.5a) and Ohmic junction (Figure 3.6a). The data allows us to study how the different M-S interface affects the extraction of field-effect mobility under different drain bias. The mobility values were obtained firstly by curve fitting to each I_D - V_{GS} curve and then calculated by applying the following equation [24]:

$$\mu_{FE} = g_m \cdot \frac{L}{W} \cdot \frac{1}{C_{ox}} \cdot \frac{1}{V_{DS}}$$

where C_{OX} = 1.2×10^{-8} F/cm^2 is the capacitance per unit area of the 285 nm-thick SiO_2 gate dielectric. Note that the maximum value of the transconductance $g_m = dI_D/dV_{GS}$ was used in the calculation.

With Schottky barriers at the S/D electrodes, the mobility is clearly modulated by the drain voltage, increasing from ~ 2 to 9 cm^2/Vs, as V_{DS} is swept from 100 mV to 2V (Figure 3.7a). However, in the same operating window, the mobility extracted from the FET with ohmic junction stays fairly constant (1.1 ± 0.1 cm^2/Vs) (Figure 3.7b). This

observation, again, verifies the “Bottleneck effect” of Schottky barrier at metal and MoS_2 interface we discussed in Chapter 2. The increasing trend of mobility in Figure 3.7a actually complies to the effect of continuously narrowed Schottky barrier with drain bias. For an Ohmic-junction, the linearity of transconductance g_m is also found an indicator of the transparency of metal-MoS_2 junction (Figure 3.7c, d).

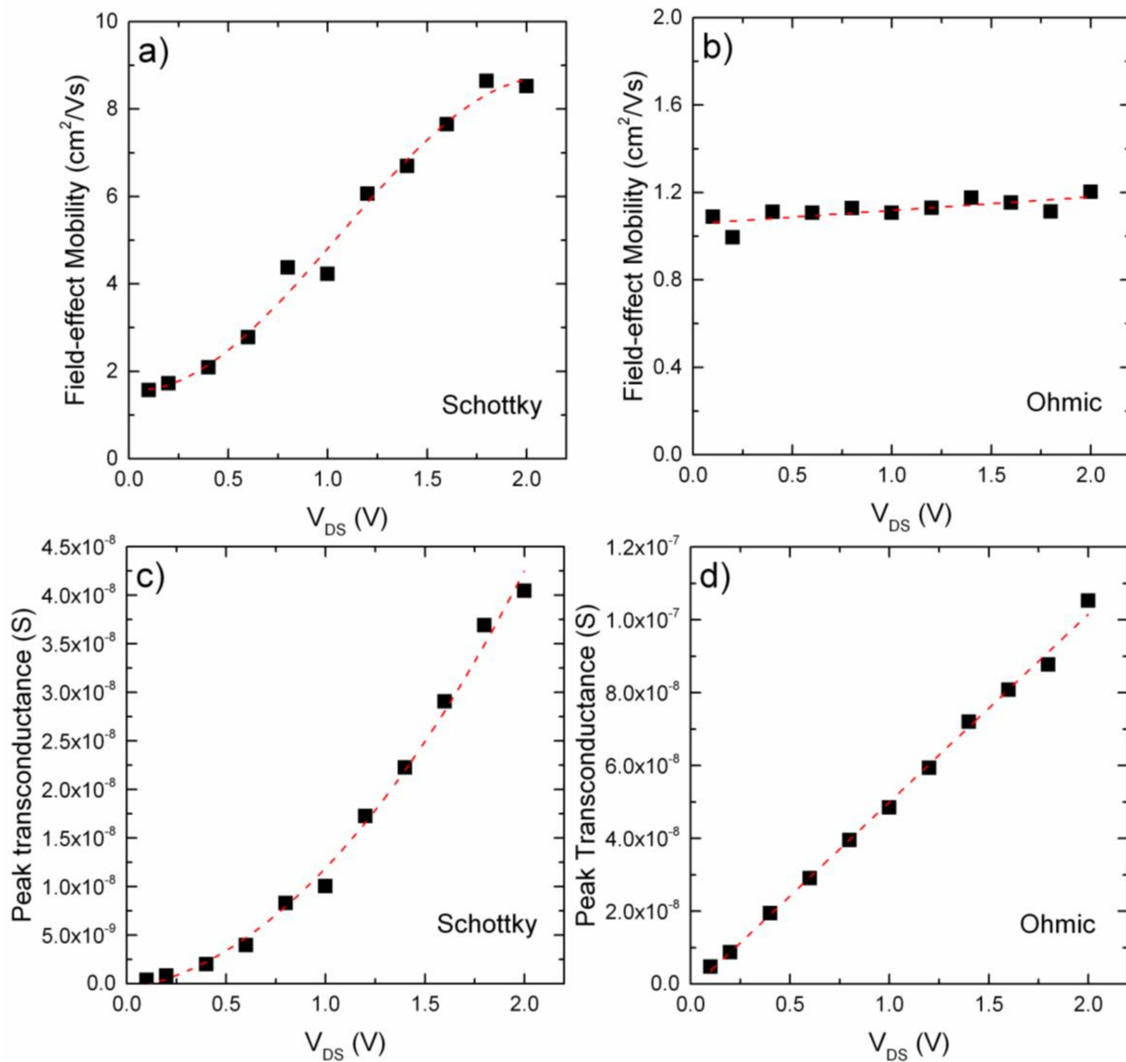

Figure 3.7 Extracted maxium transconductance (g_m) and field-effect mobilities at different V_{DS} from the two FETs with: (a) & (c) Schottky junction ($Al_2O_3/MoS_2/SiO_2$); (b) & (d) Ohmic junction (h-BN/MoS_2/h-BN). The fitted dash line is a guide for eyes.

3.4 CF_4 plasma etching profile test on $Al_2O_3/MoS_2/SiO_2$

A multi-layer MoS_2 flake, exfoliated on oxidized Si wafer, was used as the dummy sample for testing the edge profile of CF_4 etching. The test sample was firstly encapsulated by 20 nm Al_2O_3, then, through e-beam lithography and dry etching (the same process recipe as given in the main text), the heterostructure was defined into a beam (Figure 3.8).

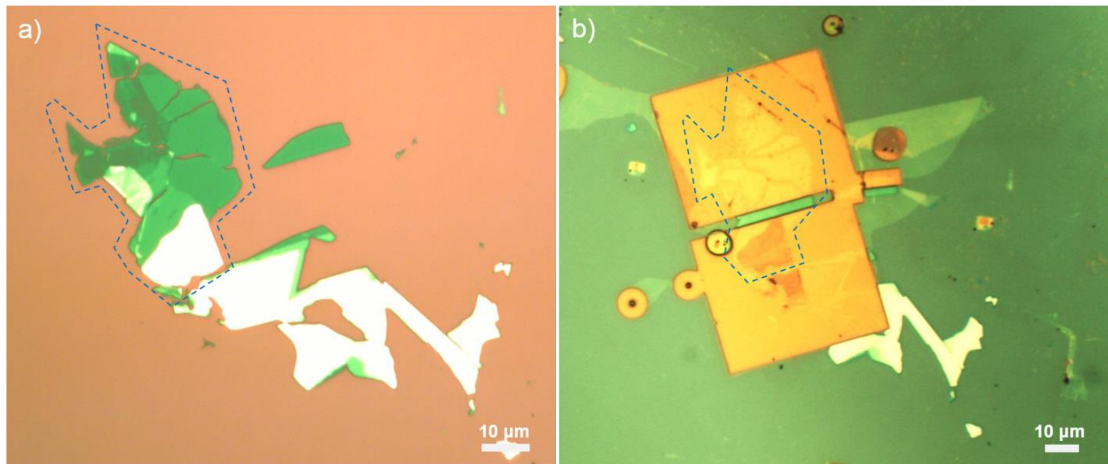

Figure 3.8 (a) as-exfoliated multi-layer MoS_2 flake (b) after Al_2O_3 encapsulation, the irregular flake is shaped into a beam, the rest are etched away by CF_4 plasma.

Right after the CF_4 plasma etching step, AFM sectioning across the $Al_2O_3/MoS_2/SiO_2$ beam shows edge spikes as high as 215.4 nm formed on the top surface at both sides of the beam. It is inferred that the spikes were due to carbon re-deposition during the etching process. After an initial 45s O_2 plasma descum step, the height of the edge spike was reduced to 33.3nm. After a second 45s O_2 plasma descum step, the edge spike was further shortened to 12.9 nm. The efficient removal of the plasma debris indicates its carbon-rich nature (Figure 3.9).

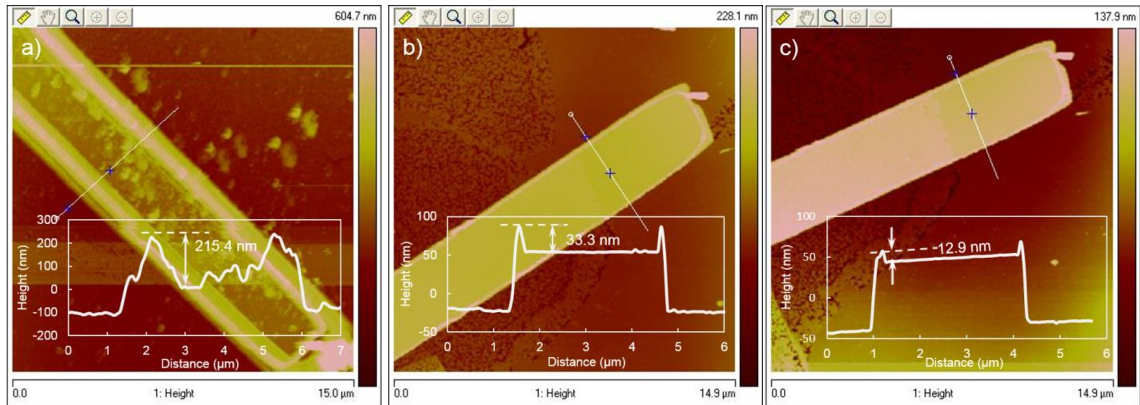

Figure 3.9 AFM section image of the $Al_2O_3/MoS_2/SiO_2$ beam (a) right after CF_4 plasma etching (b) after an initial 45s O_2 plasma descum step (c) after a second 45s O_2 plasma descum step.

3.5 SF_6 plasma etching profile test on h-BN/MoS_2/h-BN

A multi-layer h-BN flake, exfoliated on oxidized Si wafer, was used as the dummy sample for testing the edge profile of SF_6 etching. Through e-beam lithography and SF_6 etching, the h-BN was engraved with grooves of different width (Figure 3.10). AFM sectioning across the grooves shows smooth edge profiles, in contrast to the carbon-rich debris discussed in Section 3.4.

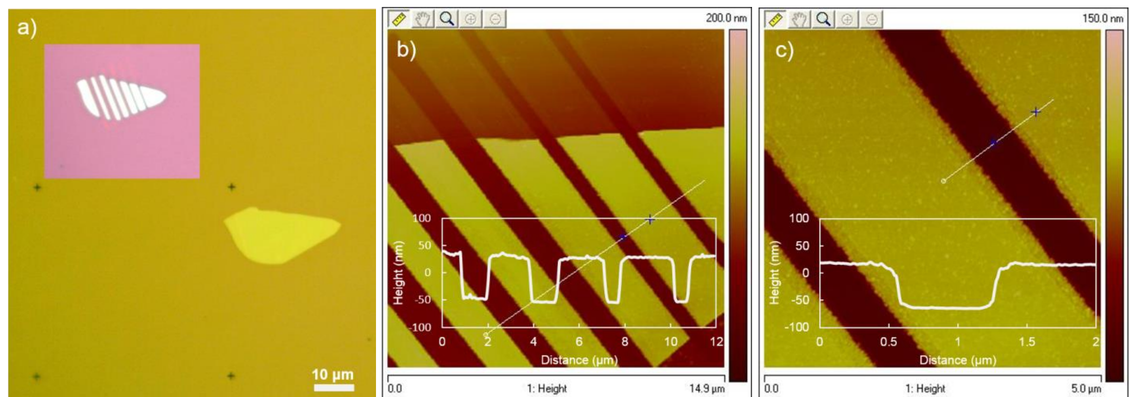

Figure 3.10 (a) a multi-layer h-BN flake, exfoliated on oxidized Si wafer (b) AFM section image across the grooves shows smooth edge profiles (c) an enlarged section image shows the side walls of one of the grooves.

3.6 Conclusion

We demonstrate a new fabrication procedure for total encapsulation of MoS_2 from environment prior to fab process and detailed steps for creating edge contacts to two types of MoS_2-based heterostructures: $Al_2O_3/MoS_2/SiO_2$ and h-BN/MoS_2/h-BN. Valid electrostatic gating effect has been characterized through the configuration of back-gated FET. A plasma etching step with volatile product, and subsequent smooth side wall profiles are found related to more efficient Ohmic-like channel conduction. Our process is applicable to other 2D material too, both exfoliated and synthesized crystal. We have also seen drastic difference in carrier mobility trend brought by the two exemplary M-S junctions. Detailed examination of the carrier transport mechanism across the edge contacts would be enabled by low-temperature electrical characterization in next stage.

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Chapter 4 Strain-gated MoS_2 Field-effect Transistors with Edge Contacts

4.1 Strain-gated Si MOSFET

Strain is a critical ingredient in modern transistor scaling. In the beginning of the millennium, carrier mobility degradation due to the large vertical electric field was identified as a key scaling problem. For Intel process technologies, the electron mobility has decreased from 400 to 120 cm^2/Vs when the industry migrated from 0.80 μm to 0.13 μm technology node [1]. As defined by Drude's equation, the carrier mobility is positively proportional to the ratio of mean scattering time τ and the effective mass of carrier m^*. Strain engineering has proven an effective route for mobility enhancement by modifying the aforementioned two parameters [2]. Theoretical studies show that strain breaks the symmetry of the energy-band structure and results in band splitting. The reduced interband /intervalley scattering and particularly, the effective masses, give rises to enhanced carrier transport in the strained-silicon layer [3]. For transistors with sub-100 nm gate length, strained silicon increased the saturated MOSFETs drive currents by 10 - 20 % and mobility by > 50%, and later ramped into high volume manufacturing on high performance microprocessors in the 90 nm logic technology [4].

The electron and hole mobility of silicon responds differently to externally applied stress. Longitudinal tensile stress along transistor channel improves electron mobility but degrades hole mobility [3, 5, 6]. To accommodate the different requirement, low-cost and highly manufacturable processing steps for strain induction were developed.

p-MOSFET features a compressively strained SiGe film embedded in the source and drain regions [7] (Figure 4.1). The mismatch in the SiGe to Si lattice causes the channel to be under a uniaxial compressive strain, leading to significantly improved hole mobility [8]. 17% germanium concentration is used which has a lattice spacing ~1% larger than Si [1]. For n-MOSFET, a post-salicide tensile silicon nitride capping layer was deposited on top of the transistor gate, wrapping both the gate and source drain area [7]. As a tensile stressor inside the nitride film tends to shrink, the stressor on the source and drain pulls apart the ends of the transistor channel and mainly produce a longitudinal tensile strain in the n-MOSFET channel [2] (Figure 4.2).

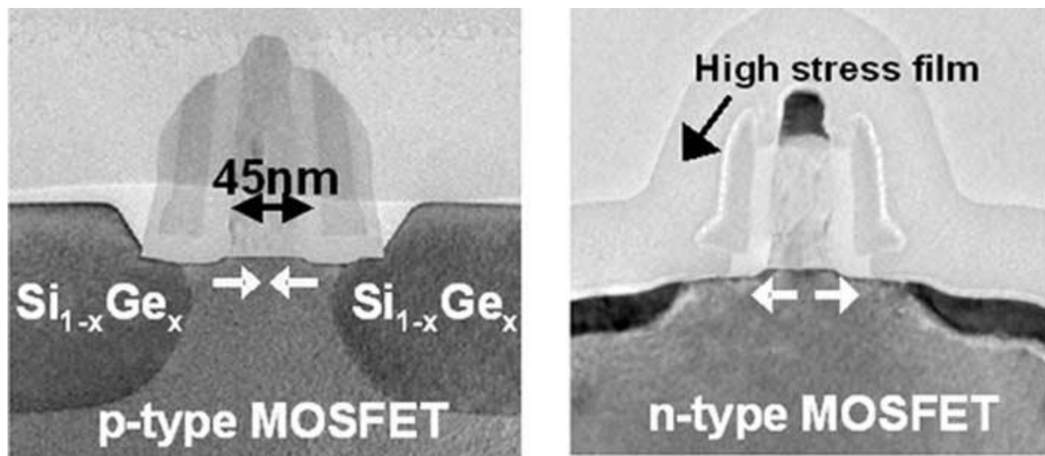


Figure 4.1 TEM micrographs of 45-nm p-type and n-type MOSFETs [9]

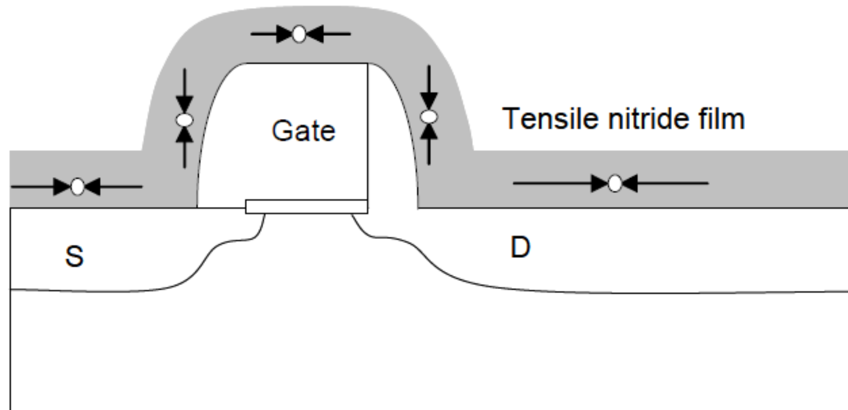


Figure 4.2 a tensile stressor tends to shrink. The stressor on the source and drain pulls apart the ends of the channel and produce a tensile strain σ_{xx} in the silicon [2].

4.2 The prospect of strain engineering in MoS_2 transistors

For three-dimensional semiconductor, the ultimate strain is limited by both bulk defects and surface imperfections [10]. Transition metal dichalcogenides (TMDs) material can circumvent the constraint for three reasons: one, negligible bulk defects because of a thickness of only a few atomic planes; two, strong in-plane covalent bond and weak van der Waals bond in between the layers, minimizing the potential dislocations in the out-of-plane direction for either homogenous sample or artificially assembled 2D heterostructures; three, a fully-terminated surface, eliminating processing steps that usually target at the passivation of the dangling bonds. The outstanding flexibility of 2D material has been proved experimentally: a breaking strain up to 11% for MoS_2 [11], an elastic strain of up to 25% for graphene [12], whereas bulk silicon can be strained only 1.2% before breaking [10].

Theoretical studies have shown that when an external tensile stress is applied, the electronic structure of monolayer MoS_2 undergoes a series of variations: first, a direct-to-indirect band gap transition when the lattice constant is just slightly lengthened; second, a more drastic semiconductor-to-metal transition when the lattice constant is increased by more than ~ 9.8% [13]. Especially, the tensile strain reduces the gap energy and effective masses while the compressive strain enhances them [13, 14]. In an imaginary solar funnel photovoltaic device made with single-layer MoS_2, the bandgap can be tuned to absorb a broad range of the solar spectrum from 2.0 eV to 1.1 eV as the biaxial tensile strain increases from 0% to 9% [15].

Most of experimental demonstration of the strain effect on MoS_2 employs standard three-point or four-point bending apparatus together with micro-Raman facilities. Ultra-thin MoS_2 samples are firstly exfoliated and clamped onto a bendable material such as PDMS [16], polycarbonate [17], PET [18] and PMMA cantilever [19]. Photoluminescence spectra are recorded at the moment when a mechanical strain is exerted. Similar findings have been reported: a red shift of photoluminescence energy and decreased peak intensity under uniaxial tensile strain, conform to the direct-to-indirect transition of the optical band gap as predicated by theoretical studies. The observation can be qualitatively understood as a result of reduced orbital overlap and hybridization due to weakened atomic bonds [19]. On the contrary, a blue shift of the photoluminescence peak and an increase of the emission intensity have been reported for biaxial compressive strain exerted to tri-layer MoS_2 through a piezoelectric substrate [20], which strengthens our understanding of the strain effect on atomically thin MoS_2.

The influence of mechanical strain on MoS_2 FETs can also be characterized through bending test. Tsai et al. introduced uniaxial strain along the longitudinal direction of the MoS_2 channel by firstly transferring synthesized tri-layer MoS_2 onto a flexible substrate and then taping the sample on a rigid cylindrical surface. Back-gated flexible MoS_2 transistor were measured in the flat state and the stretched state (strain = 0.07%). Of note is that a shift of the transfer curve toward lower back-gate voltages and an electron current increase is observed under strain [21]. Lee et al. fabricated highly flexible and transparent MoS_2 FETs built on hBN dielectric and graphene gate electrodes. However, the device performance was virtually unchanged with applied uniaxial strains up to 1.5% [22]. Different from the aforementioned two literature, biaxial tensile stress were earlier applied to AlGaN/GaN heterostrucure field-effect transistors through Si_3N_4 passivation, device performance shows an increase of the maximum drain current and transconductance, while this is mainly a manifestation of the increased sheet carrier density confined at the hetero-interface, due to the increased piezoelectric polarization in the strained AlGaN layer [23].

Though MoS_2 exhibits a comparable bandgap to Si, its carrier mobility is too low for logic devices. The room temperature carrier mobility in single- and few-layer MoS_2 FETs fabricated on SiO_2/Si substrates was found to be typically in the range of 0.1~10 $cm^2 V^{-1}s^{-1}$ [24, 25], without effort on optimizing the MoS_2/ dielectric interface [26-28] or contact engineering [29, 30].

In this chapter, we bring the concept of "strain-gate" into the realm of 2D semiconductors. Strain is exerted to MoS_2 channel by depositing a silicon nitride stress capping layer that covers the entire top-gated FET. To enhance the field-effect mobility, uniaxial tensile strain along the transistor channel is favored to be generated in order to reduce the band gap and electron effective mass. Current on/off ratio and other transistor performance metrics are measured as the transistor evolves from back-gate, to top-gate and finally, strain-gate configurations. This is the first study that directly links the strain effect to device performance of MoS_2 top-gated transistors. The nitride stress liner method is a permanent solution for strain exertion without relying on external instrument, besides, it is also a low-cost, highly manufacturable technique for improving transistor performance, highly beneficial for the ultimate goal of industrial application of TMD transistors.

4.3 Experimental methods

4.3.1 Bi-layer MoS_2 sample preparation

The bi-layer MoS_2 sample for spectroscopic study was exfoliated on a PDMS-based gel-film first, and then transferred onto a pre-cleaned oxidized Si substrate through a solvent-free micro-manipulation procedure as explained in Section 1.5. This additional exfoliation step on gel-film largely improved the yield of mono- and bi-layer MoS_2 to ~ 100%. The produced samples are usually in area of a few μm^2, feasible for multiple transistor fabrication. A second bi-layer MoS_2 sample sent on for strain-gate fabrication was prepared following the conventional method depicted in Section 1.4.

4.3.2 MoS_2 transistors fabrication

- Plasma enhanced chemical vapor deposition (PECVD) for depositing the nitride stress capping layer: Plasmatherm Unaxis 790, deposition pressure 900 mTorr, power 25 W, 2% SiN_4 200 sccm, NH_3 4 sccm, N_2 900 sccm, deposition time 10 mins at 120 °C, film thickness 125 nm
- Reactive ion etching (RIE) for generating He plasma and creating edge contacts: STS Reactive Ion Etcher Dielectric System, flow rate 50 sccm, 75 W, 20 s
- Atomic layer deposition (ALD) for HfO_2 top-gate dielectric: Cambridge Nanotech Savannah 100, 250 cycles at 120 °C, film thickness 30 nm
- Metal evaporation: Temescal BJD 1800 system, aluminum seed (2 nm, 0.1Å/s), source drain electrodes (Sc/Ni, 50/30 nm), back-gate electrode (Ti/Au, 10/100 nm), top-gate electrode (Ti/Au, 10/60 nm)
- Rapid thermal annealing (RTA) : RTP-600S system, 200 °C, Ar, 1 hr

A degenerately boron-doped (0.001~0.005 Ω•cm) silicon substrate with 285 nm SiO_2 capping layer, served as the global back gate and gate dielectric. Spectroscopic and electrical characterization instrument are the same as the information presented in Section 3.2.3.

4.4 Raman and PL characterization

First, we validate the approach of strain exertion through the deposition of a nitride stress capping layer using PECVD. The detection of the strain effect

experimentally can be done by observing the phonon modes of the material using Raman spectroscopy. Changes to the optical band gap can be extracted through photoluminescence spectroscopy. As shown in Figure 4.3a, a bi-layer MoS_2 sample was transferred onto a Si/SiO_2 substrate, and divided into three regions. The spectra of each region were recorded both before and after the nitride deposition. This is to minimize potential disturbances that can result from different pristine bi-layer samples. AFM height measurement at the edge of the nitride film shows a total thickness of 125 nm (Figure 4.3 c and d).

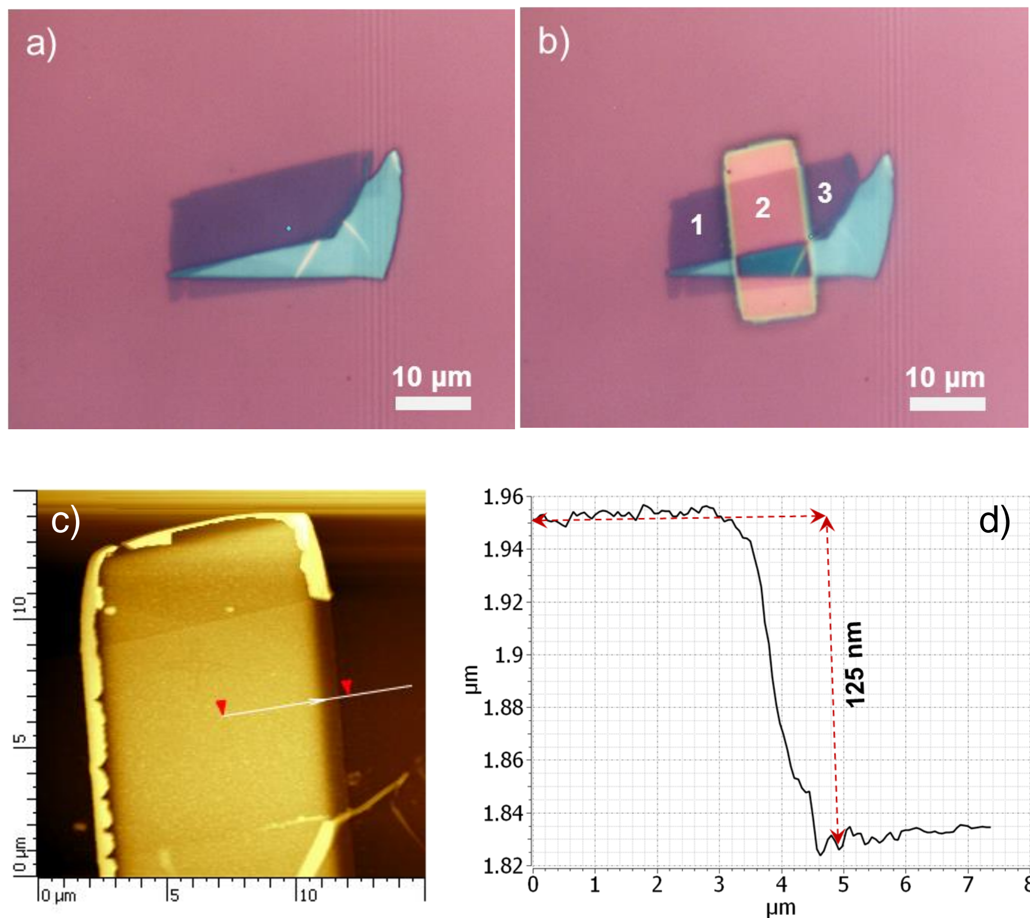


Figure 4.3 (a) a bi-layer MoS_2 transferred onto Si/SiO_2 substrate (b) after the patterning and deposition of silicon nitride (c, d) AFM section profile at the edge of the nitride film.

At all three spots, PL spectra show the two prominent emission peaks at 670 and 627 nm, corresponding to the two resonances known as A1 and B1 excitons [31], and the Raman spectra show the wavenumber difference between the E^1_{2g} and A_{1g} peak is 22 cm^{-1} [32]. Therefore, we confirm the bi-layer thickness and the homogeneity of the sample. Out of the three spots, only spot 2 is covered by silicon nitride. Two findings can be extracted from Figure 4.4b: one, there is about 14 nm shift of the entire luminescence spectra towards longer wavelength, and it is estimated to be 38 meV by using $E = 1240/\lambda$; two, about 40 % decrease of the emission intensity. Both findings indicate a reduced bandgap possibly due to the tensile strain from the nitride capping layer. Difference in thermal expansion coefficient between MoS_2 and silicon nitride could be another source of strain exertion [33], as the PECVD deposition of the nitride layer occurs at 120 °C, and a tensile strain can be induced in the MoS_2 flake during the subsequent cooling of the sample to room temperature. Spot 2's Raman spectra in Figure 4.4e shows a red shift of the A_{1g} peak ($\Delta\omega \approx 1.5$ cm^{-1}), given the fact that the referential peak of silicon remains at 520.7 cm^{-1} before and after the nitride deposition. This peak shift could be due to an extra strain in the out-of-plane direction, in the next stage, we are going to use simulation to find out the cause behind. No peak shift was detected in the PL or Raman spectra of the other two spots.

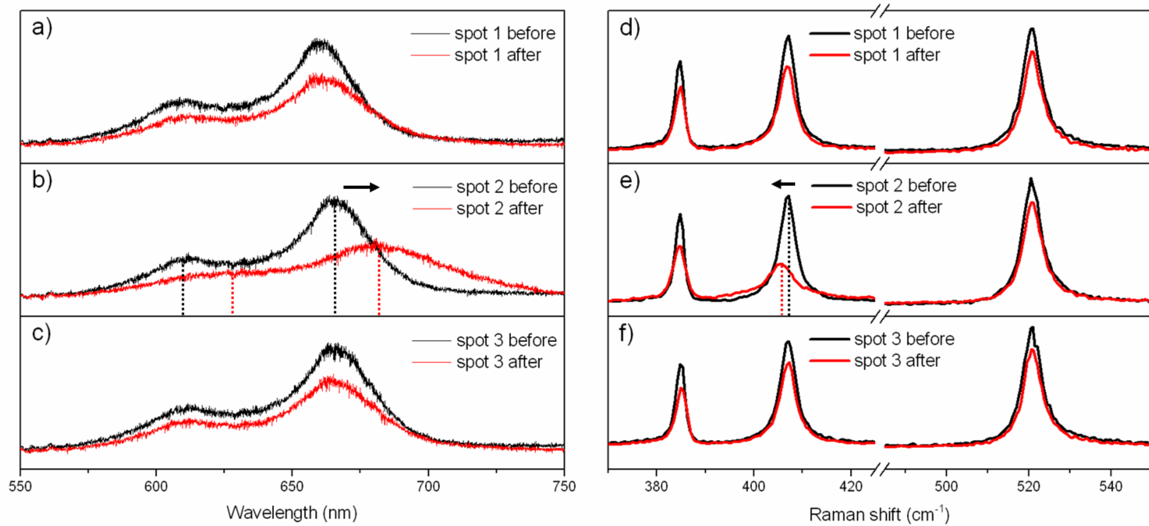


Figure 4.4 Raman and PL characterization of the MoS_2 covered by silicon nitride

4.5 Electrical characterization

Figure 4.5 illustrates the flow of fabrication process for the complete strain-gated MoS_2 transistor. The main stages for electrical characterization are denoted as back-gate (BG), top-gate (TG) and strain-gate (SG). Electrical data obtained from each cycle are put into comparison. The key challenge for achieving the strain-gate in the final stage is about having robust MoS_2 FET with good electrical contacts to survive multiple clean room processing and electrical measurement cycles.

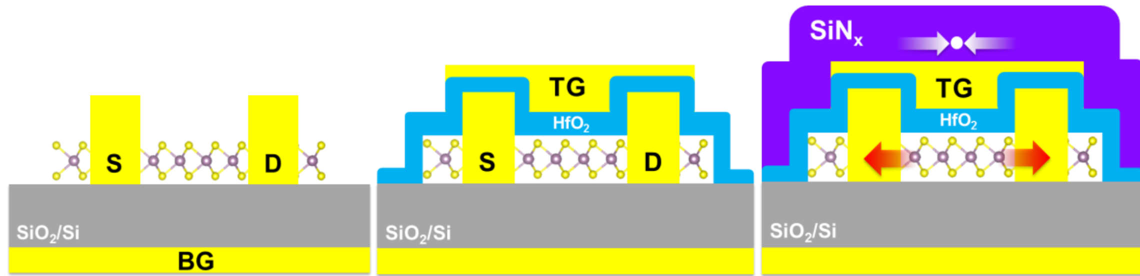


Figure 4.5 (from left to right) the evolution of the MoS_2 FET structure from back-gate to strain-gate.

In the beginning, a bi-layer MoS_2 was directly exfoliated onto a Si/SiO_2 substrate. The thickness is confirmed by the low wavenumber Raman peak (slightly larger than 20 cm^{-1}) [34], and the difference between the E^1_{2g} and A_{1g} peak, as shown in Figure 4.6. After the first e-beam lithography step, the sites for source drain contacts were etched by helium plasma (Figure 4.7a, b). Instead of using SF_6, the physical bombardment from helium plasma can prevent potential oxidation of the exposed MoS_2 atoms. From our experience, the yield of working FET is significantly improved with edge contacts, compared with surface contacts. The edge contacts are completed after metal evaporation (Sc/Ni, 50/30 nm) and lift-off (Figure 4.7c). Next we move on to top-gate FET structure. The top-gate dielectric comprised of an AlO_x/HfO_2 stack. The AlO_x was formed by e-beam evaporation of 2 nm aluminum seeds, followed by its natural oxidation in air overnight [35]. The 30 nm HfO_2 was formed using atomic layer deposition (Figure 4.7d). The top-gate electrode was Ti/Au, 10/60 nm (Figure 4.7e). After TG electrical measurement, the device was further sent on for SiN_x stress liner deposition by PECVD. The recipe is the same as the one in Section 4.4, which ensures the same amount of stress provided by the nitride film. As shown in Figure 4.7f, the entire MoS_2 flake, including

the bulky area, are sealed underneath this nitride layer. The thickness of the SiN_x film is 125 nm.

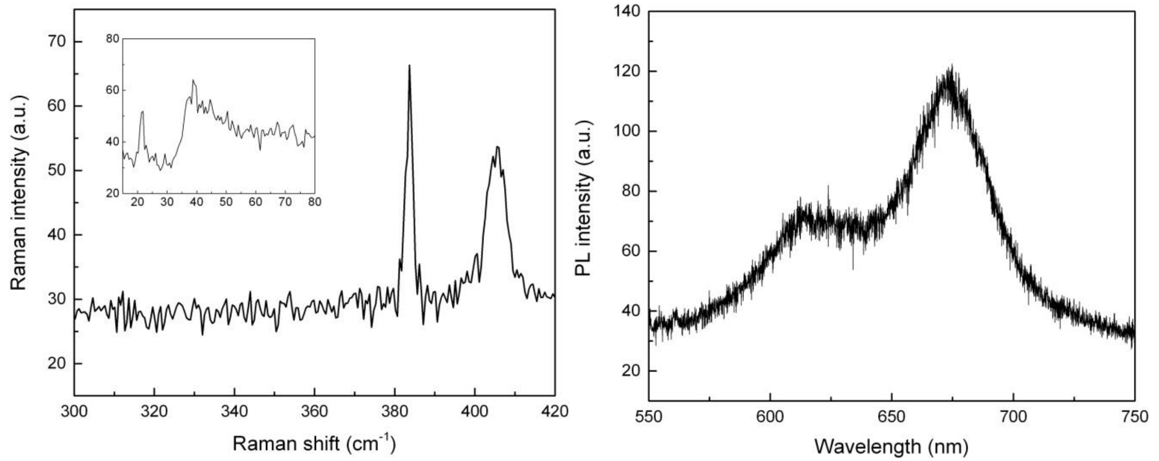
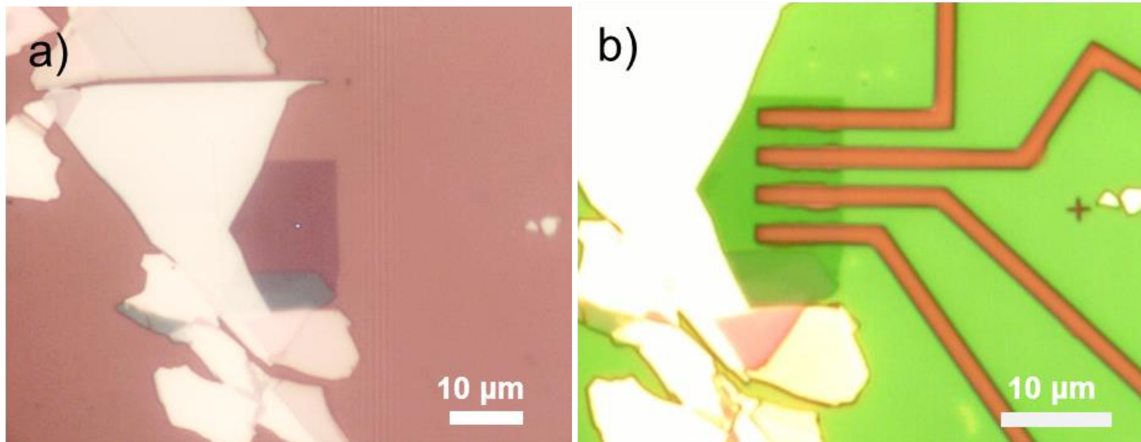


Figure 4.6 The Raman and PL spectra of the bi-layer MoS_2 sample selected for device fabrication



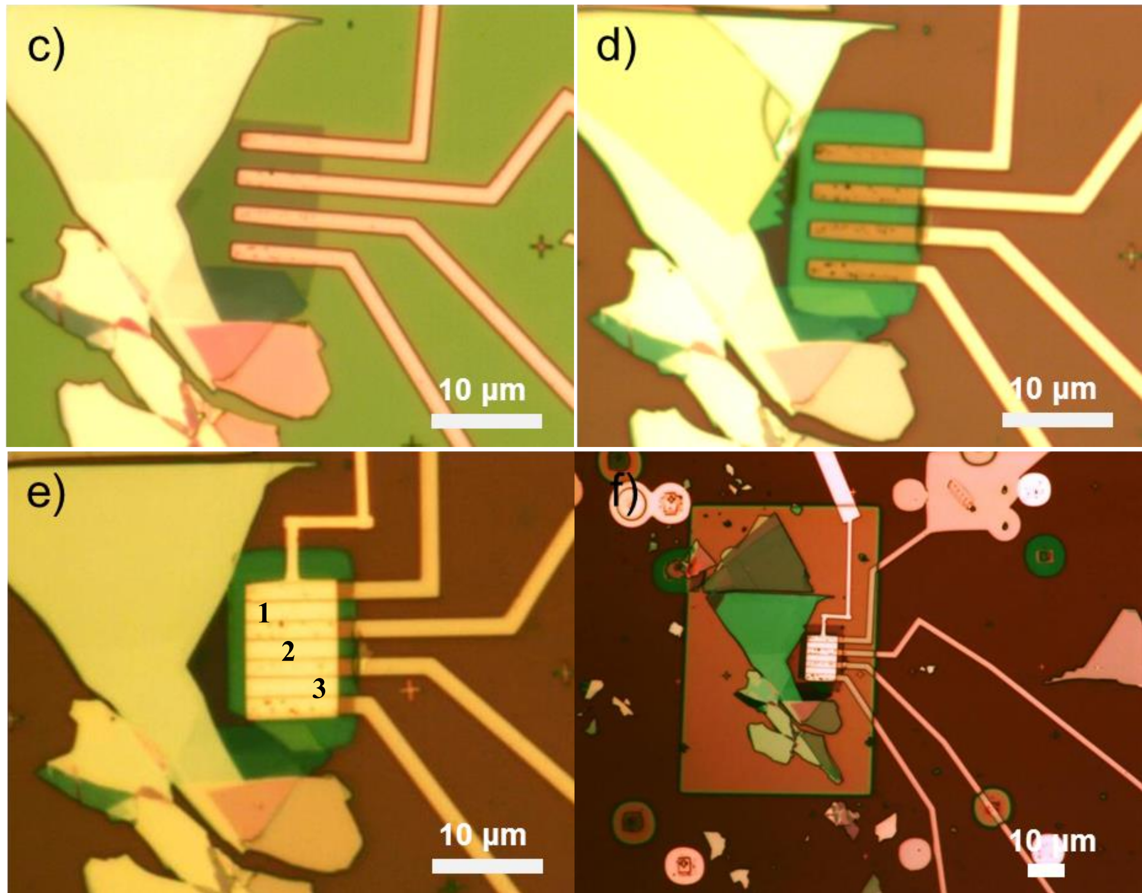


Figure 4.7 The process flow for device fabrication (a) optical imaging (b) open edge contacts by helium plasma (c) edge contact metal Sc/Ni evaporation (d) 30 nm HfO_2 ALD deposition (with 2 nm Al seed) (e) top-gate metal Ti/Au deposition (f) 125 nm SiN_x PECVD deposition at 120°C

In total, three field-effect transistors that have experienced the back-gate, top-gate and strain-gate stages are fabricated on this bi-layer MoS_2, as labeled on Figure 4.7e. To test whether all three are functioning, the output and transfer characteristics were taken at the time when the back-gate configuration was completed. Figure 4.8a shows the I_D - V_{DS} plot, in which V_{BG} is set to zero, and V_{DS} sweeps from -1 to 1V, and Figure 4.8b gives the complementary I_D - V_{GS} plot, in which V_{DS} is fixed at 1V, while the V_{BG} sweeps from -40 to 40V. The effective modulation of the drain current by the voltages across the edge

contacts tells that all three FETs give valid output and gate transfer characteristics, though some discrepancy is still observed. To make a fair comparison across the three stages of fabrication, from this point on, the discussion is focused on the electrical performance of transistor No.2.

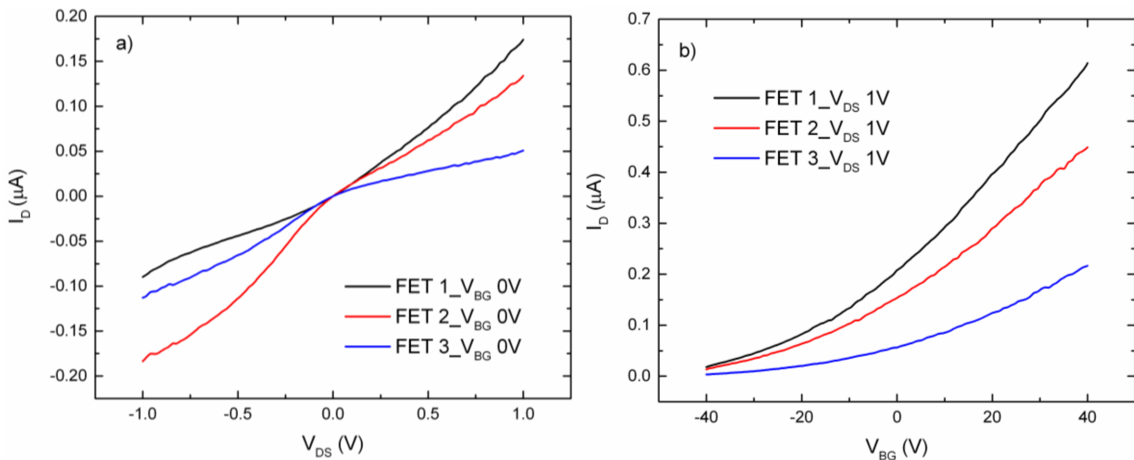


Figure 4.8 I-V repeatability tests on the three transistors after the back-gate FET configuration is completed

The full electrical characteristics of transistor No. 2 are given in Figure 4.9, and the legends and the name of the gate voltage tell which process it corresponds to. The first row is for output plots, in which V_{DS} sweeps from -1 to 1V. The inset of Figure 4.9a enlarges the area close to the origin. Within the range of -200 to 200 mV, I_D changes almost linearly with V_{DS}, indicating an Ohmic junction. Of note is that the top-gate voltage was set to 10 times smaller than that for back-gate, this is because of a much thinner top-gate dielectric and the enhanced over 60 times capacitance per unit area. As

shown in the following equation, here we use 30 nm thick HfO_2 with a theoretical relative permittivity of ε_r = 25, and 285 nm thick SiO_2 with ε_r = 3.9.

$$C_{Hfo2}/C_{Sio2} = \frac{\varepsilon_{Hfo2}}{d_{Hfo2}} \Big/ \frac{\varepsilon_{Sio2}}{d_{Sio2}} = \frac{25}{30\ nm} \Big/ \frac{3.9}{285\ nm} \approx 61$$

The second row is for gate transfer plots, with the linear scale on the left in black color and the log scale on the right in blue. The curve with filled markers corresponds to a V_{DS} of 1V; those with empty markers have V_{DS} of 100 mV. We notice three important findings across all three transfer plots, one, the drain current increases significantly at positive gate voltage, indicating n-type FET; two, a sharp contrast on current on/off ratio when we switch from back-gate to top-gate; three, the most importantly, the continued improved drain current magnitude from back-gate to strain-gate. This proves that the deposition of the nitride stress liner indeed enhances the transistor's electrical performance.

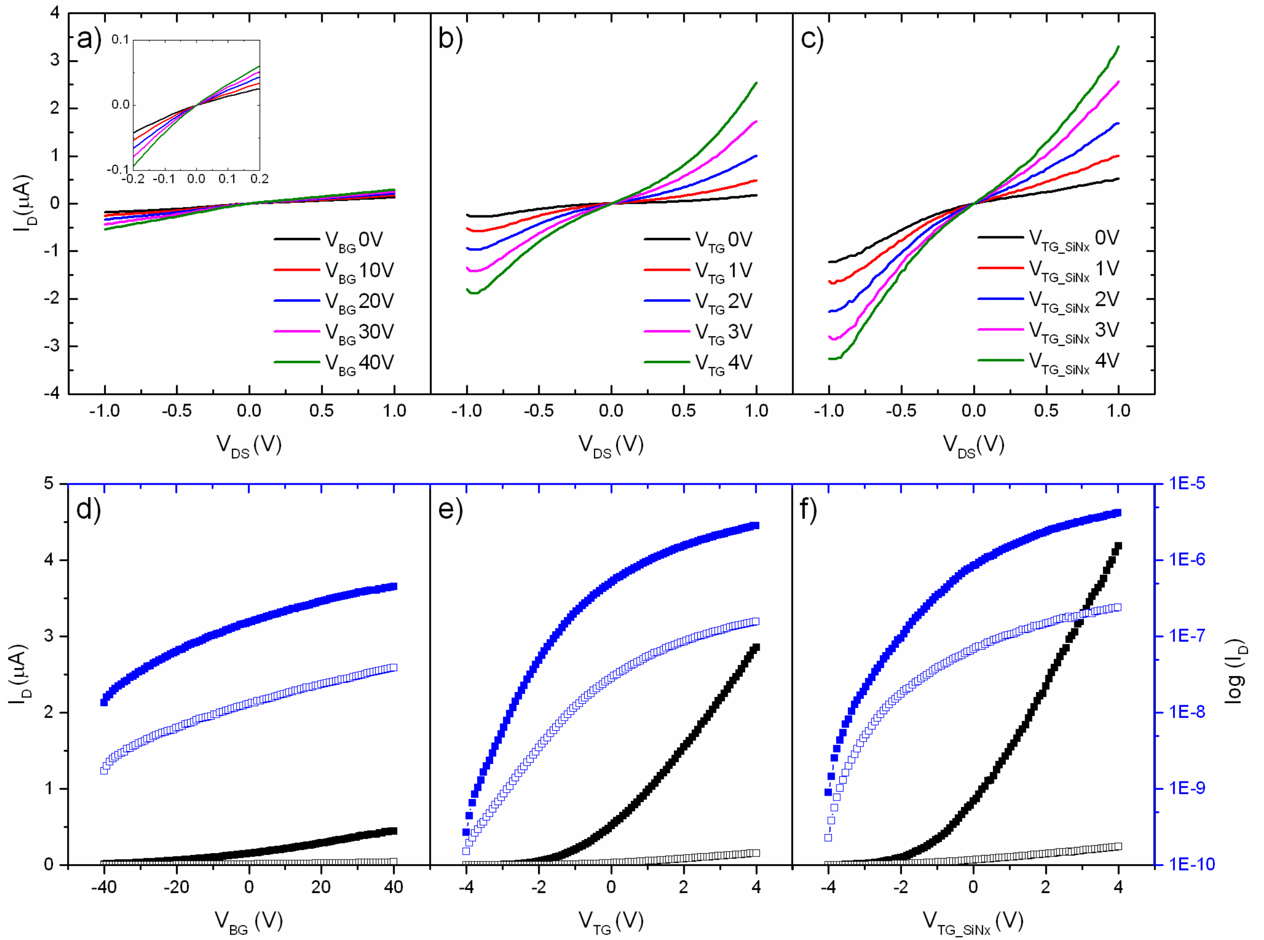


Figure 4.9 Output and gate transfer characteristics of transistor No.2

The extracted carrier transport parameters are plotted in Figure 4.10. The "on" and "off" currents are defined as the maximum and the minimum currents in the measured gate voltage range. The mobility values were obtained firstly by curve fitting to each I_D - V_{GS} curve and then calculated by applying the following equation [36]:

$$\mu_{FE} = g_m \cdot \frac{L}{W} \cdot \frac{1}{C_{ox}} \cdot \frac{1}{V_{DS}}$$

where C_{ox} = 1.2×10^{-8} F/cm^2 is the capacitance per unit area of the 285 nm-thick SiO_2 back- gate dielectric, and C_{ox} = 7.4×10^{-7} F/cm^2 for 30 nm HfO_2 top-gate dielectric. The aspect ratio of transistor No.2 is W/L = 7.5/1.8 μm. Note that the maximum value of the transconductance $g_m = dI_D/dV_{GS}$ was used in the calculation. The data plotted in Figure 4.10 were all obtained at V_{DS} = 1V.

Because of a more effective control of carrier concentration in top-gate, compared with back-gate, we notice significantly improved current on/off ratio from < 100 to ~ 10^4, a 43% increase of electron mobility, a 5 times increase in on-current, almost 98% decrease in off-current. Particularly, for the threshold voltage calculated using the linear extrapolation method [37], the value shrinks from -14 to -0.8 V, so does the sub-threshold swing, drops from 30 to 1.2 V. Two important findings when we compare top-gate and strain-gate FET: another 58% increase in electron mobility and 46 % increase in on-current magnitude, while the rest parameters show no drastic decay. Since the transistor structure remains top-gate for the final "strain-gate" electrical measurement, we can say that the continued improvement in mobility and on-current purely come from the strain effect induced by the nitride capping layer. Though the absolute value of the mobility is still too low for practical logic device, the ideas presented in this chapter can further be repeated in newly-prepared TMD material. Of all the three devices, FET No. 3 exhibits the same carrier transport enhancement as FET No.2, whereas no evident improvement was observed in FET No. 1. This could be due to incoherent stress experienced by the bi-layer MoS_2 flake, as PECVD results in rough granulated SiN_X surface at lower deposition temperature [38].

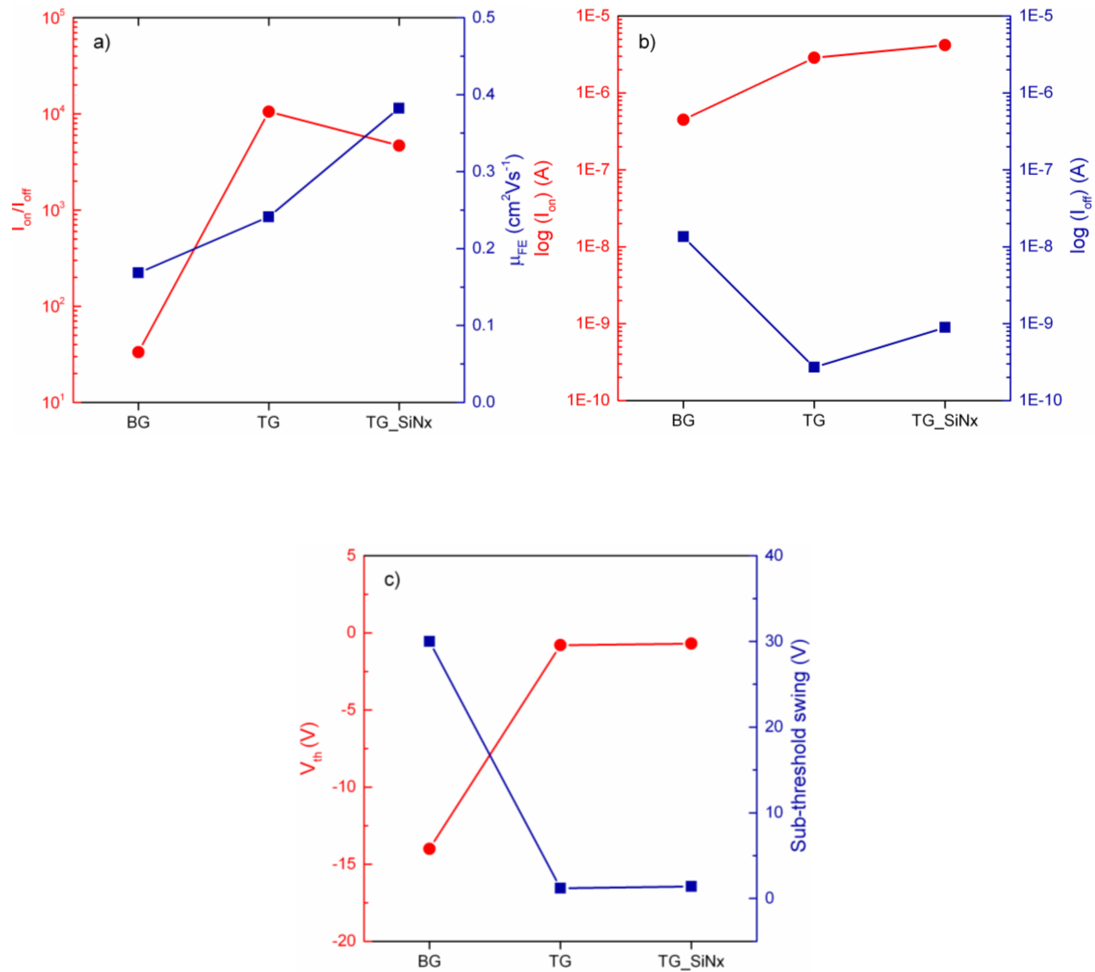


Figure 4.10 Transistor No.2: comparing the carrier transport properties of back-gate (BG), top-gate (TG) and strain-gate (SG) FET configurations

4.6 The extraction of contact resistance

Two-terminal and four-terminal measurements were implemented on the FETs discussed in Section 4.5 (electrode width = 1.5 μm). The I-V characteristic shows Ohmic-like profile, similar to the electrical data of the h-BN/MoS_2/h-BN device in Chapter 3.

Figure 4.11a shows the two-terminal output plots of FET No.2. Data in the positive half of the output plots was used to calculate the total channel resistance:

$$R_{total} = \frac{V_{DS}}{I_D}$$

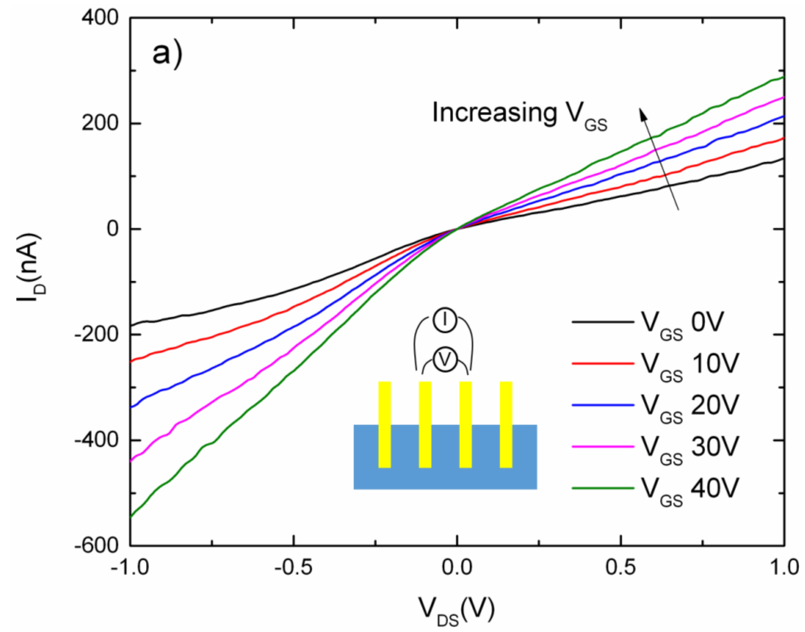
Four-terminal measurements (Figure 4.11b) allow us to calculate the actual channel resistance by:

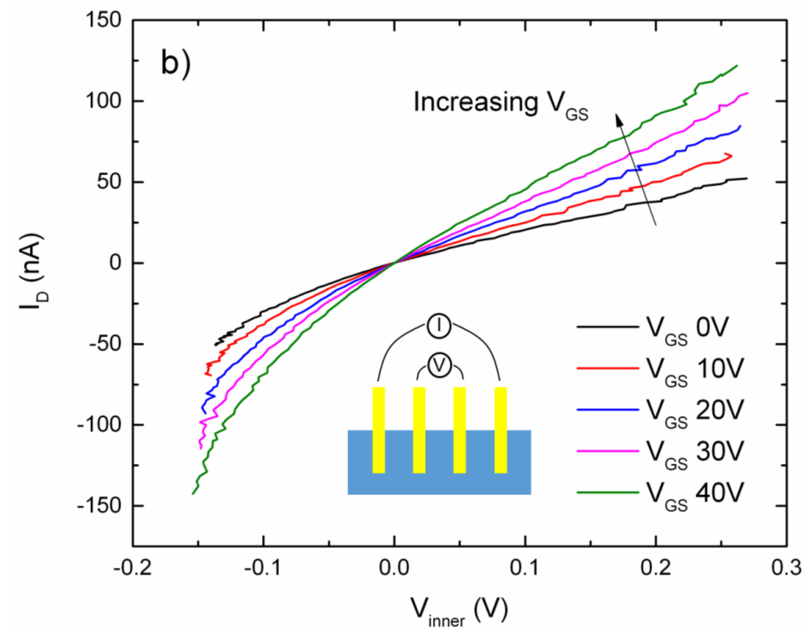
$$R_{ch} = \frac{V_1 - V_2}{I_D} = \frac{V_{inner}}{I_D}$$

Since the total resistance between two contacts can be modeled as:

$$R_{total} = R_{ch} + 2R_c$$

The total contact resistance R_c was found to be ~ 1.25×10^6 Ω (9.375×10^6 Ω·μm) at zero back-gate voltage, which decreased to ~ 6.29×10^5 Ω (4.72×10^6 Ω·μm) at $V_{GS} =$ 40V (Figure 4.11c).


a)
Increasing V_GS
I_D(nA)
V_DS(V)
V_GS 0V
V_GS 10V
V_GS 20V
V_GS 30V
V_GS 40V
I
V


b)
Increasing V_GS
I_D (nA)
V_inner (V)
V_GS 0V
V_GS 10V
V_GS 20V
V_GS 30V
V_GS 40V
I
V

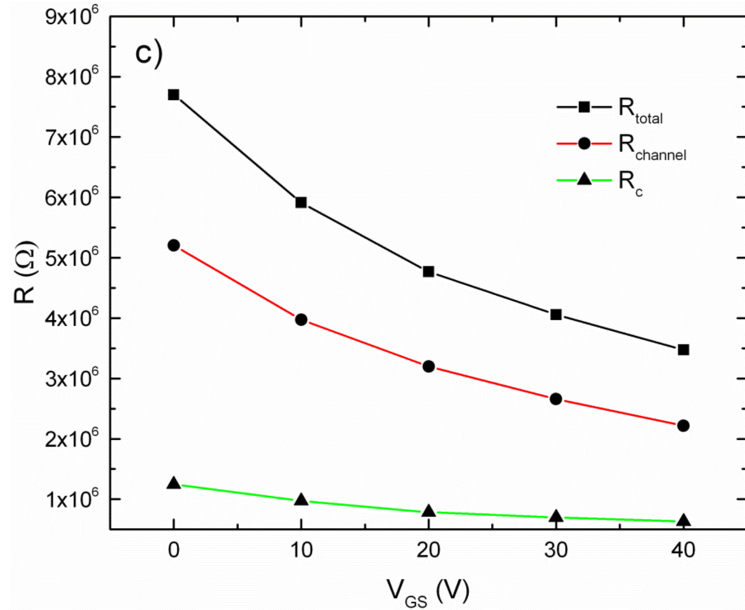


Figure 4.11 (a) two-terminal and (b) four-terminal I-V measurement of the transistor No.2 (c) the gate-dependent intrinsic channel resistance and contact resistance.

4.7 Conclusion

In summary, we have demonstrated the strain effect on MoS_2 through Raman/ photoluminescence spectroscopy and transistor characterization. The utilization of edge-contacts ensures the functioning of transistors through multiple cycles of clean room processing and electrical measurement from back-gate, to top-gate and finally strain-gate. The pioneering approach of strain induction through a nitride stress liner has brought a benign effect on improving the carrier transport property in top-gated MoS_2 FETs. We have seen significant improvement in on-current density and field-effect mobility. In next step, it is necessary to fine tune the nitride deposition recipe for a smoother and more uniform film, probably followed up with FTIR studies to estimate the chemical bonding conditions in the deposited silicon nitride films. It is expected that the strain effect would

be more prominent in an “all 2D” transistor that utilizes h-BN as gate dielectric and graphene as electrodes.

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