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Collective Dynamics in Coupled Spiking Oscillators

A Dissertation submitted in partial satisfaction of the requirements  
for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Erbin Qiu

Committee in charge:

Professor Ivan K. Schuller, Chair  
Professor Eric E. Fullerton, Co-Chair  
Professor Robert Dynes  
Professor Shaya Fainman  
Professor Tina Ng  
Professor Paul Yu

2024

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University of California San Diego

2024



## DEDICATION

**To all the free food at the seminars.**

**To the sunshine and moonlight I walked through.**

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4. J. Park, A. Kumar, Y. Zhou, **E. Qiu**, et al. Multi-level, forming and filament free, bulk switching trilayer RRAM for neuromorphic computing at the edge. Nat Commun 15, 3492 (2024).
5. H. Navarro, **E. Qiu**, et al, Disentangling transport mechanisms in a correlated oxide by photoinduced charge injection. Phys. Rev. Mater. 7, L123201 (2023).
6. **E. Qiu**, Y. Zhang, M. Ventra, I. K. Schuller. Reconfigurable cascaded thermal neurons for artificial intelligence. Adv. Mater. 2306818, (2023).
7. L. Singh, **E. Qiu**, et al., Controlling thermal radiation with a phase-change metasurface, 2022 Conference on Lasers and Electro-Optics (CLEO), San Jose, CA, USA, 2022, pp. 1-2.
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ABSTRACT OF THE DISSERTATION

**Collective Dynamics in Coupled Spiking Oscillators**

by

Erbin Qiu

Doctor of Philosophy in Electrical Engineering (Applied Physics)

University of California San Diego, 2024

Professor Ivan K. Schuller, Chair  
Professor Eric E. Fullerton, Co-Chair

Coupled oscillators always exhibit all kinds of emergent collective modes and intriguing synchronization phenomena, ranging from collective oscillations in bacteria to beating of cilia, from rhythms in biological neurons to phase synchronization in brain, from nanomechanical and nanoelectromechanical oscillators to spin Hall and spin torque nano-oscillators. This dissertation explores the unique dynamical behaviors of coupled spiking

oscillators based on Mott materials. Spiking oscillator, a special type of oscillator that produces short-duration spikes (around 30 ns), contrasts with smoothly evolving harmonic oscillators. Spiking oscillators can emulate the electrical activity of brain, can develop large scale spiking neural networks, and can potentially be the building block for the energy-efficient oscillator-based computing. To design a complex network capable of performing advanced computational tasks, it is necessary to understand the basic phenomenology of the interactions between two spiking oscillators. First, I report the unusual emergence of a stochastic pattern in capacitively coupled spiking oscillators. While a moderate capacitive coupling results in a deterministic alternating spiking, increasing the coupling strength leads counterintuitively to stochastic disruptions of the alternating spiking sequence. Then I switch my focus to the thermally coupled spiking oscillators. Transition between two integer modes occurs through an unusual stochastic synchronization regime instead of the loss of spiking coherence. In the stochastic synchronization regime, random length spiking sequences belonging to the 1:1 and 2:1 mode are intermixed. By carefully tuning the load resistance and the input voltages of the coupled spiking oscillators, termed neuristors, I demonstrate a wide variety of reconfigurable electrical dynamics mirroring biological neurons, including all-or-nothing law, rate coding, stochastic leaky integrate-and-fire, excitatory and inhibitory functionalities. Moreover, random number generator will be demonstrated by taking advantage of the stochasticity hiding behind the synchronization. This dissertation investigates the basic phenomenology of the interactions between two spiking oscillators, discovers several usual findings, and establishes the foundation for scalable and energy-efficient brain-inspired computing.

## Chapter 1 Introduction

### 1.1 Overview

A vast majority of data is being produced at an exponential pace, which demands substantial energy and financial resources to be manipulated effectively for everyday applications<sup>1,2</sup>. This poses considerable challenges to both the von Neumann architecture and Moore's law<sup>3</sup>. Moore's law, a guiding principle indicating that the number of transistors on a microchip roughly doubles every two years, plays a crucial role in directing the advancement of the semiconductor industry<sup>4-6</sup>. With the continuous advancement of photolithography techniques in technology, transistors continue to diminish in size, edging closer to their atomic limitations. However, within the next two decades, Moore's law is poised to become obsolete due to emerging obstacles such as atomic restrictions and issues related to heat dissipation<sup>7</sup>. Additionally, the von Neumann bottleneck<sup>8</sup>, shuttling data between the central processing unit and memory unit, imposes a constraint on computational speed. The back-and-forth data transfer incurs twice the energy expenditure. As a result, researchers are actively exploring innovative computing paradigms and novel functional materials to further amplify computational capabilities<sup>2,9-17</sup>.

Oscillator-based computing, an approach of using networks of interacting oscillators for information processing, can provide an efficient alternative to conventional computational algorithms implemented on von Neumann architecture<sup>10</sup>. Demonstrations of oscillator-based computing include networks capable of solving NP-hard combinatorial tasks, such as graph coloring<sup>18,19</sup>, maximum cut<sup>20,21</sup> and maximum independent set<sup>22</sup> problems. Furthermore, oscillator circuits are essential components of hardware-level implementation of spiking neural networks<sup>23,24</sup>. In many practical demonstrations the individual oscillators are implemented using

standard CMOS technology<sup>18,21,22,25</sup>. Recently, there has been a great interest in replacing CMOS oscillator circuits with devices based on quantum materials in order to reduce energy consumption and circuit footprint. Several approaches have been proposed including the use of magnetic spin-torque oscillators<sup>26,27</sup> micro- and nanoelectromechanical systems<sup>28-30</sup>, and spiking devices based on electrical triggering of an insulator-metal transition (IMT)<sup>31,32</sup>.

We focus on the spiking devices, termed as spiking oscillators, producing short-duration spikes. It contrasts with smoothly evolving harmonic oscillators, emulates the electrical activity of brain<sup>31,33</sup>, and can find applications in the development of hardware-level energy-efficient implementations of neural networks<sup>23,34,35</sup>

The key element that enables oscillator-based computing is the ability to achieve tunable coupling between the individual spiking oscillators. The implementation of coupling between non-CMOS devices is often complex and could result in a highly non-intuitive dynamical behavior<sup>36-40</sup>. In order to design a complex network capable of performing advanced computational tasks, it is necessary to understand the basic phenomenology of the interactions between two spiking devices.

In chapter 3, we report the emergence of an unusual stochastic pattern in coupled spiking Mott nanodevices. While a moderate capacitive coupling results in a deterministic alternating spiking, increasing the coupling strength leads counterintuitively to stochastic disruptions of the alternating spiking sequence. The disruptions of the deterministic spiking sequence are a direct consequence of the small intrinsic stochasticity in electrical triggering of the insulator-metal transition. While the stochasticity is subtle in the individual nanodevices, it becomes dramatically enhanced just in a single pair of coupled oscillators and thus dominates the synchronization. The stochastic spiking pattern in Mott nanodevices results in a discrete inter-



spike interval distribution resembling those in biological neurons. Our results advance the understanding of the emergent synchronization properties in spiking oscillators and provide a platform for hardware-level implementation of oscillator-based computing.

The stark differences between the spiking oscillators and harmonic oscillators motivate extensive studies of synchronization phenomena in spiking devices driven by different types of interactions.

Chapter 4 presents an investigation of the synchronization evolution in coupled spiking nano-oscillators based on a Mott material where strong thermal interactions promote in-phase synchronization. We observed the occurrence of unique spiking patterns controlled by a DC voltage applied independently to each oscillator. For small or large applied voltages, the oscillators develop robust 2:1 or 1:1 integer synchronization spiking mode. However, in a relatively wide range of intermediate applied voltages, the oscillators enter a stochastic synchronization regime where the spiking pattern unpredictably alternates between the two discrete integer synchronization modes. These findings highlight unique dynamic synchronization properties of spiking oscillators as compared to conventional harmonic oscillators. The ability to electrically control the synchronization modes and drive the coupled spiking devices into a stochastic synchronization regime is important for practical implementations of neuromorphic and stochastic computing circuits.

Chapter 5 is also based on the two thermally coupled spiking oscillators. These spiking oscillators, referred to as neuristors, exhibit a range of neural functionalities. Notably, we demonstrate the implementation of an inhibitory neuristor using simple Mott oxides, such as  $\text{VO}_2$ , by trapping the metallic state, eliminating the need for complex circuits. Additionally, both excitatory and inhibitory neuristors can be realized using the same device by employing different

inputs, thereby enhancing the device's versatility and applicability. The neuristor also displays a rich array of reconfigurable electrical behaviors such as rate coding and stochastic leaky integrate-and-fire. Crucially, we demonstrate the feasibility of cascading neural layers through thermal interactions, which effectively eliminate the necessity for complex input/output circuits between layers. Our straightforward and innovative approach paves the way for advancements in reconfigurable cascading neural layers, which hold promise for applications in artificial intelligence.

## 1.2 Mott materials

Mott materials, referred to as strongly correlated electron systems, constitute a class of substances that undergo transitions between insulating and metallic states<sup>41-44</sup>. This intriguing switch from insulator to metal can be readily initiated by a range of external influences<sup>42,45</sup>, including temperature fluctuations<sup>46</sup>, electrical fields<sup>42,43</sup>, light illumination<sup>47-49</sup>, mechanical strain<sup>50-53</sup>, chemical doping<sup>43,54,55</sup>, and pressure variations<sup>56,57</sup>. The comprehensive exploration of Mott materials has consistently captivated researchers due to their exceptional electronic characteristics, sensitivity to external perturbations, emergence of novel phenomena, and diverse potential applications across various domains, such as Resistive Random Access Memory (ReRAM)<sup>42</sup>, artificial spiking neurons<sup>58,59</sup>, electronics, and energy-related technologies. Gaining insight into and effectively manipulating the metal-insulator transition holds paramount importance in leveraging these materials within condensed matter physics and materials science to drive technological progress.

The focal investigating material of my dissertation centers on vanadium dioxide ( $\text{VO}_2$ ), an iconic archetype of Mott materials.  $\text{VO}_2$  exemplifies a phase transition characterized by a discontinuity in the first derivative of the free energy with respect to temperature, specifically a

first-order phase transition<sup>60,61</sup>. Within this transition, VO<sub>2</sub> undergoes a sudden change in electrical conductivity from metallic behavior to insulating behavior, featuring a distinctive hysteresis loop. Alongside this electronic transition, VO<sub>2</sub> also experiences a structural phase transition<sup>43,45</sup>. At lower temperatures, it resides in a monoclinic (M1) phase with low-symmetry (space group P21/c), and as temperature increases, it undergoes the crystal structure phase transition, transitioning to the high-temperature tetragonal rutile (R) phase with high-symmetry (space group P42/mnm).

### 1.3 Resistive switching

Applying an external voltage or current to transition metal oxide can lead to a resistance change once a certain threshold is reached. This phenomenon, characterized by a significant alteration in resistance, is referred to as resistive switching<sup>62-68</sup>. The interest in resistive switching has surged due to its potential for enabling rapid switching speeds, memory devices with high storage density and energy efficiency, as well as applications in neuromorphic computing.

Resistive switching behavior can be categorized into two types: volatile and non-volatile. Volatile reversible resistive switching behavior usually emerges from insulator-to-metal transitions activated by thermal processes<sup>42,43,55</sup>. In contrast, non-volatile irreversible changes in resistance are primarily attributed to ion migration<sup>69</sup> or the creation of new materials<sup>69,70</sup>.

Resistive switching devices often adopt a two-terminal configuration, featuring a metal-dielectric-metal setup. Applying a voltage exceeding the threshold to this two-terminal device initiates an insulator-to-metal transition, such as VO<sub>2</sub>. Once the electrical bias is removed, VO<sub>2</sub> reverts to its initial insulating state. This form of resistive switching is volatile and reversible. It is an ideal candidate for constructing a spiking oscillator<sup>59,71,72</sup>, capitalizing on this reversible

volatile behavior. By incorporating an appropriate load resistor, the insulating and metallic states can be manipulated back and forth, resulting in a stable auto-oscillation. This engineered spiking neuron holds promise for applications in spiking neural networks and neuromorphic computing.

Regarding non-volatile resistive switching, subjecting the device to a substantial electrical field can induce electronic breakdown, resulting in a permanent change in resistance that persists even after the external electrical bias is withdrawn in VO<sub>2</sub>'s case<sup>67,68,70,73</sup>. But in some other resistive switching materials, the resistance state can be adjusted and restored by applying a voltage, rendering them suitable for data storage purposes<sup>68,73</sup>. In spiking neural networks, such materials can function as synapses linking spiking neurons across different neural layers for adjusting the weight. The weight of these connections can be tuned through spiking voltage stimuli generated by neurons in the preceding layer.

By incorporating spiking oscillators and synapses, it becomes possible to build spiking neural networks and enable the development of neuromorphic computing.

#### 1.4 Neuromorphic computing

Neuromorphic computing, which takes inspiration from the brain's information processing capabilities, offers an energy-efficient alternative to traditional von Neumann architectures<sup>13,74-78</sup>. At the heart of neuromorphic computing are spiking neural networks (SNNs)<sup>74,79</sup>, which simulate the event-driven nature and sparse communication patterns of biological neurons by using precisely timed spikes across layers of artificial neurons and synapses. Input data is represented and transmitted through time-varying spikes that are processed by interconnected neurons. Much of the current research has been centered on software simulations<sup>11,80</sup> or implementations using complementary metal-oxide-semiconductors (CMOS)<sup>81-84</sup>. Notable CMOS-based SNNs include IBM's TrueNorth chip<sup>82</sup> and Intel's Loihi<sup>84</sup>

which are built using cutting-edge, costly technologies and complex circuit designs. A CMOS neuron typically encompasses components like temporal integration, spike/event generation, refractory period, spike frequency adaptation, and spiking threshold adaptation blocks<sup>83</sup>. However, the significant circuit footprint, limitations in scaling, and energy consumption may impede the progress of CMOS-based SNNs.

Beyond CMOS-based models, there has been a recent emergence of spiking neuron devices<sup>85,86</sup> constructed using quantum materials, which are now at the forefront of neuromorphic computing, including but not limited to Mott neurons<sup>87-90</sup>, magnetic neurons<sup>14,15,27</sup> and phase change neurons<sup>91-93</sup>. These devices have the potential to significantly reduce both the circuit complexity and the physical size of artificial neurons. However, the development of these quantum material-based artificial spiking neuron devices is still in its infancy, and various challenges and issues have been observed in initial demonstrations.

One of the primary challenges facing artificial spiking neuron devices, which is often overlooked, is the difficulty in directly transmitting information between layers without intricate circuit configurations. The issue stems from the fact that the presence of a subsequent neural layer alters the output of the preceding layer due to the loading effect. Solutions typically involve the integration of complex buffer circuits<sup>94,95</sup>, which substantially increase the overall size, often overshadowing the spiking neurons themselves in terms of space. Some studies sidestep this issue altogether<sup>16,96,97</sup>, focusing solely on network-level simulations based on the properties of individual neuron devices, without considering the challenges of transmitting information between layers at hardware level. As a result, the efficient integration of cascading neural layers remains elusive.

Furthermore, current spiking neuron configurations lack versatility. For instance, inhibitory neurons play a critical role in neural activities, but replicating this functionality in artificial spiking neurons is no easy feat. Some attempted solutions involve elaborate circuits<sup>98–100</sup>, synaptic weight alternations<sup>94</sup>, or optical inhibition<sup>95</sup>. However, none of these can directly implement an inhibitory neuron in a single simple device, which poses significant constraints on the application of learning algorithms.

### 1.5 Acknowledgements

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## Chapter 2 Techniques

### 2.1 Thin films growth technique

The VO<sub>2</sub> films were deposited on the (012)-oriented Al<sub>2</sub>O<sub>3</sub> substrate by reactive RF magnetron sputtering. To begin, the high-vacuum chamber, initially at a base pressure of approximately 1x10<sup>-7</sup> Torr, housed the (012)-oriented Al<sub>2</sub>O<sub>3</sub> substrate. The substrate was then heated to 680°C. Next, a combination of pure argon at a flow rate of 2.2 s.c.c.m and mixed gases (20% oxygen and 80% argon) at a flow rate of 2.1 s.c.c.m was introduced into the chamber. The sputtering plasma was initiated at a pressure of 4.2 mTorr by applying a forward power of 100 W to the target, which corresponded to an applied voltage of around 240 V. The deposition process for the VO<sub>2</sub> films took 30 minutes, resulting in a film thickness of 100 nm. Once the deposition was complete, the sample holder's temperature was gradually reduced to room temperature at a rate of 12°C per minute.

### 2.2 X-ray analysis

To enhance understanding of X-ray analysis, I will provide a brief overview of various types of scanning measurements.

Bragg's law:

$$2 * d_{hkl} * \sin\theta = n * \lambda$$

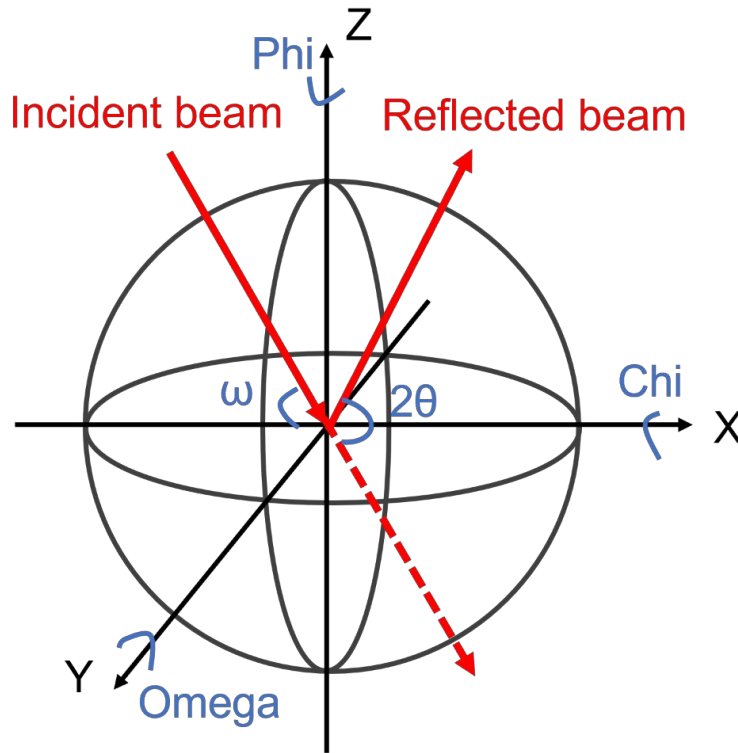


Figure 2.1 Schematic configuration.

The sample is positioned on the X-Y plane and situated at the central point of a sphere as shown in Figure 2.1. The incident beam  $K_0$  hits the sample's surface and subsequently reflects as  $K_1$ . The incident angle, labeled as Omega ( $\omega$ ), is defined as the angle between the incident beam and the sample's surface. The diffracted angle, labeled as 2-Theta ( $2\theta$ ), is defined as the angle between the incident beam and the reflected beam. The rotation of the X-axis corresponds to the Chi scan, while the Y-axis rotation represents the Omega scan. Furthermore, the Z-axis rotation corresponds to the Phi scan.

Measurement Procedures:

1. Perform optical alignment.
2. Execute sample alignment, a process comprising multiple automated steps that ensure alignment with the sample's surface. Multiple automated steps include direct beam half cut alignment with Z scan and Omega scan. Surface normal



alignment with Z scan, Omega scan, and Chi (Rx) Scan. Repeat these alignments three times.

3. Conduct X-ray Reflectivity (XRR) measurements.
4. Undertake manual control alignment, usually initiated from the Omega scan and progressing to the 2-Theta/Omega scan and Rx scan. This step should be repeated until peak intensity values reach saturation. This manual alignment step is crucial for achieving alignment with the atomic surface of the sample.
5. Carry out specular diffraction.

#### Important Considerations:

1. Whenever there is a change in hardware components, ensure that the hardware configurations are updated in software accordingly.
2. During manual alignment, ensure that the incident slit, receiving slit #1, and receiving slit #2 are open to the maximum. Using a small slit restricts the amount of beam passing through, which can make it challenging to locate the peak.

#### $2\theta/\omega$ Scan:

During the  $2\theta/\omega$  scan, both arms of the X-ray source and the X-ray detector undergo simultaneous movement. In essence, the wave vectors  $\vec{K0}$  and  $\vec{K1}$  alter their orientations, resulting in a change in the amplitude of the scattering vector while maintaining its direction, as depicted in Figure 2.2.

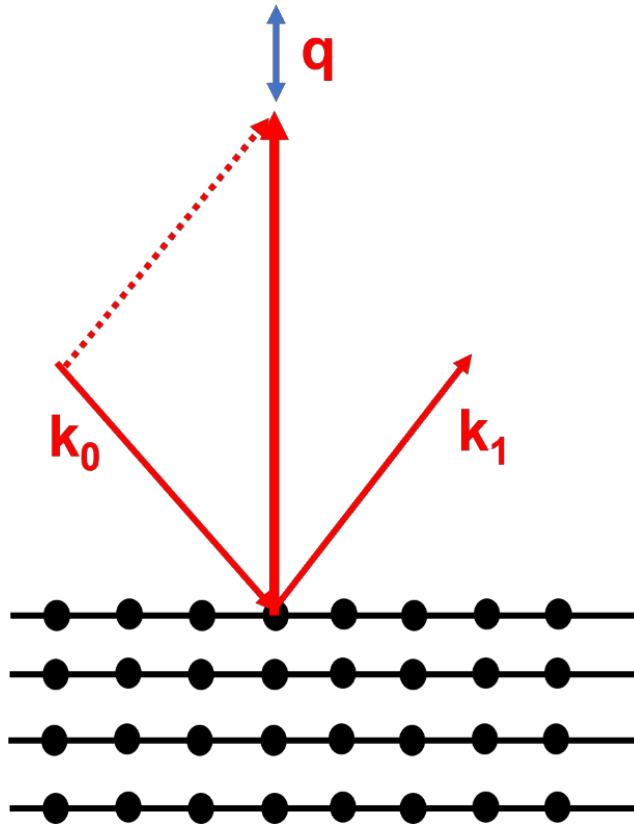


Figure 2.2 2-Theta/Omega scan schematic

$\omega$  Scan:

Within the  $\omega$  scan, the two arms of the X-ray source and the X-ray detector also move concurrently, but the diffraction angle  $2\theta$  remains constant. This implies that the wave vectors  $\vec{k}_0$  and  $\vec{k}_1$  change their directions while preserving the angle between them. Consequently, this leads to a change in the direction of the scattering vector while its amplitude remains unchanged, as illustrated in Figure 2.3.

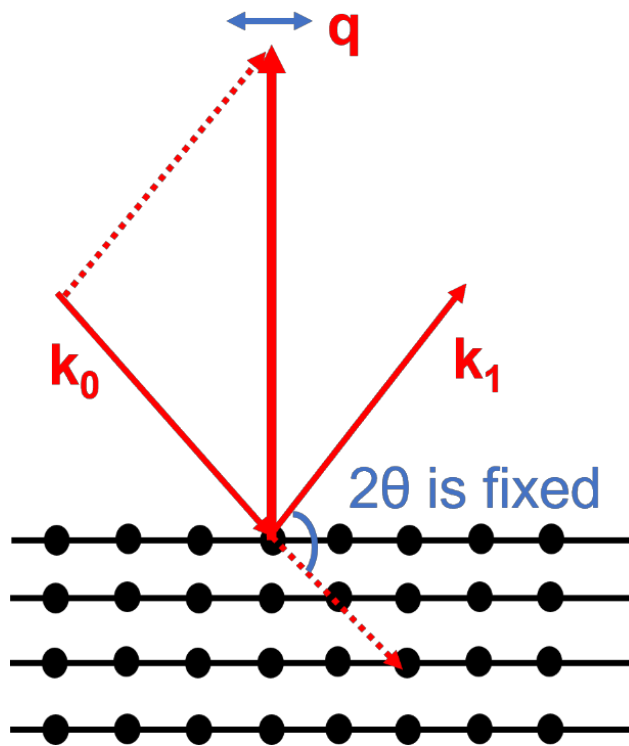


Figure 2.3 Omega scan schematic

$2\theta$  Scan:

In contrast, during the  $2\theta$  scan, only the arm of the X-ray source remains fixed, while the arm of the X-ray detector remains in continuous motion. Specifically, the wave vector  $\vec{k_0}$  remains unchanged while  $\vec{k_1}$  changes its direction. This results in a simultaneous alteration of both the amplitude and direction of the scattering vector, as shown in Figure 2.4.

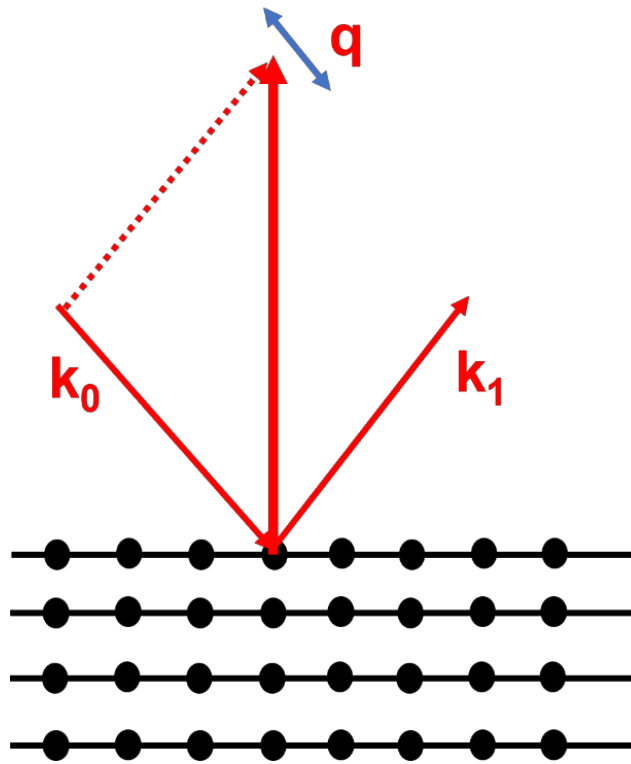


Figure 2.4 2-Theta scan schematic

X-ray Reflectivity (XRR) serves as a method for extracting information about the thickness, density, and surface roughness of thin films. The critical angle in this process is contingent upon the material's electronic density. The thickness of the thin film can be determined using the formula  $2\pi/\Delta q$ . The conversion of real space data ( $2\theta$ ) to reciprocal space data ( $q$ ) is facilitated through the utilization of Rigaku software PDXL. Notably, thicker films exhibit shorter oscillation periods in this context. One XRR example is displayed below in Figure 2.5.

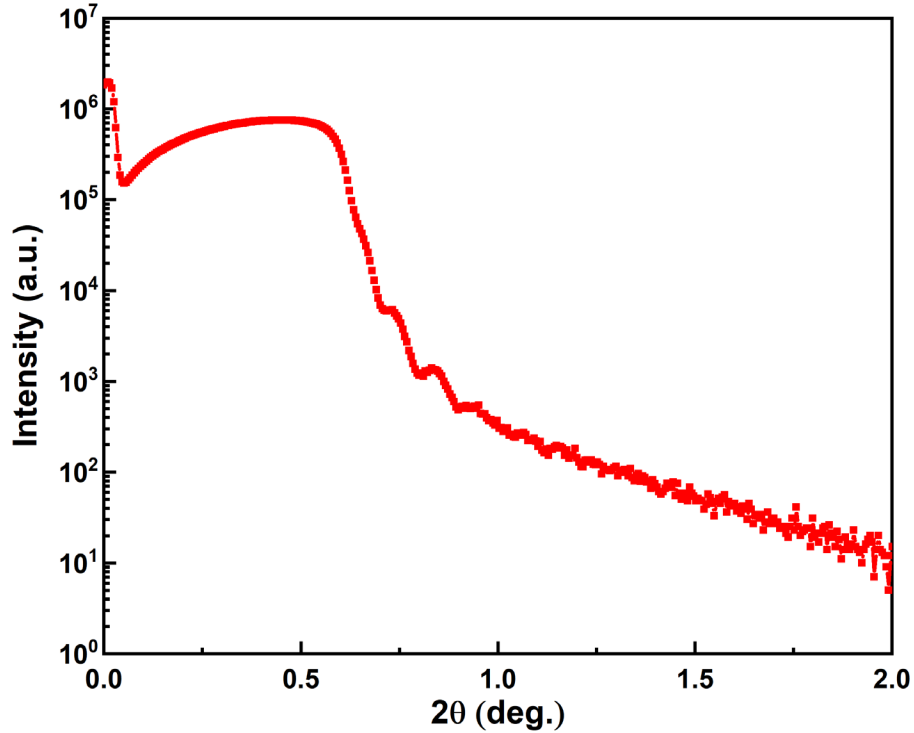


Figure 2.5 X-ray reflectivity (XRR) of one of VO<sub>2</sub> samples

X-ray Diffraction (XRD) determines the structural information of crystals. Bragg's equation is used to analyze and interpret the peak information obtained from materials in X-ray diffraction (XRD) studies. This equation relates the wavelength of the incident X-rays ( $\lambda$ ), the diffraction angle ( $\theta$ ), and the distance between atomic planes in the crystal lattice ( $d$ ). By applying Bragg's equation, we can determine the crystallographic structure of materials, including crystal orientation and the identification of different phases within the sample. An illustration of an XRD data example is provided in Figure 2.6.

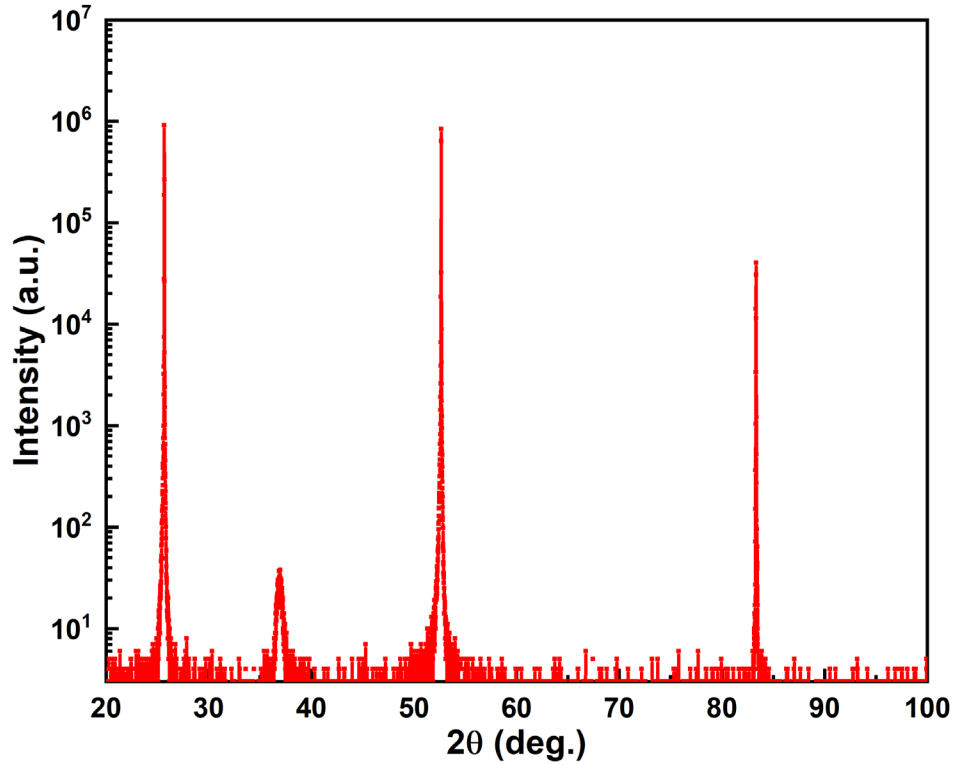


Figure 2.6 X-ray diffraction (XRD) of one of VO<sub>2</sub> samples

## 2.3 Device fabrication

After confirming the high quality of the thin films with X-ray analysis, I patterned thin films into devices for further characterization, particularly the transport measurements. Basically, I fabricate two types of devices, one is nanodevice using E beam lithography and the other is microdevice optical lithography.

### 2.3.1 E beam lithography

The E beam lithography process is as follows:

- a) Place the uncoated films into a beaker containing Acetone and immerse the beaker in an ultrasonic bath sonicator to eliminate any chemical residues on the substrate.

- b) Cleanse the substrate with IPA to eliminate any traces of Acetone. Repeat the first and second steps multiple times.
- c) Employ a high-purity nitrogen gun to thoroughly dry the sample, followed by placing the substrate on a hotplate set to 80°C for 1 minute to completely remove any moisture.
- d) Spincoat a positive E beam resist PMMA-A4 onto the sample using spinner for 60 seconds at a speed of 5000 rpm. This step defines the electrode pattern. Ensure complete coverage of the substrate surface with a substantial amount of electron beam resist before starting spinning, while being careful not to let the pipette contact the substrate. (For the second lithography step, spincoat a negative electron beam resist ma-N 2405 onto the sample for 40 seconds at the same speed. This step serves to safeguard the electrode pattern and devices.)
- e) Perform a soft baking process at 115°C for 20 minutes for the substrate coated with PMMA-A4 in the first lithography step. (In the second lithography step, carry out a brief soft baking at 91°C for 1 minute for the ma-N 2405-coated substrate.)
- f) Utilize the Vistec EBPG5200 Electron Beam Lithography system to expose our sample. The exposure dose for PMMA A4 is 1000UC/cm<sup>2</sup>, while the dose for ma-N 2405 is 280UC/cm<sup>2</sup>.
- g) Develop the exposed PMMA A4 by immersing it in a solution of 1:3 MIBK to IPA. Employ developer ma-D 532 for the negative resist ma-N 2405.
- h) Thoroughly rinse the sample with deionized water for 5-10 minutes and then proceed to dry the thin films.

### 2.3.2 Optical lithography

The E beam lithography process is as follows:

- a) Place the uncoated films into a beaker containing Acetone and immerse the beaker in an ultrasonic bath sonicator to eliminate any chemical residues on the substrate.
- b) Cleanse the substrate with IPA to eliminate any traces of Acetone. Repeat the first and second steps multiple times.
- c) Employ a high-purity nitrogen gun to thoroughly dry the sample, followed by placing the substrate on a hotplate set to 80°C for 1 minute to completely remove any moisture.
- d) Spincoat a photoresist AZ 1512 onto the sample using spinner for 60 seconds at a speed of 4000 rpm. This step defines the electrode pattern. Ensure complete coverage of the substrate surface with a substantial amount of electron beam resist before starting spinning, while being careful not to let the pipette contact the substrate.
- e) Perform soft baking at 95 °C for 1 minute.
- f) Expose the sample using Heidelberg MLA150. The employed light source is a 375 nm laser. The exposure dose is set at 150 UC/cm<sup>2</sup>.
- g) Immerse the sample in AZ 300 MIF for 40 seconds for development.
- h) Thoroughly rinse the sample with deionized water for 5-10 minutes and then proceed to dry the thin films.



### 2.3.3 Electrodes deposition

### 2.3.4 Etching

The etching process is as follows:

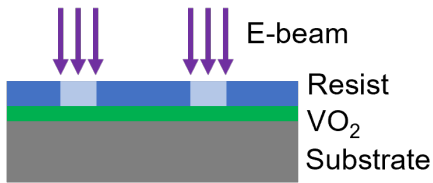
- a) Immerse the sample in AZ 300 MIF for 40 Perform a cleaning procedure on the Oxford Plasmalab 80 Plus RIE chamber using oxygen plasma.
- b) Execute the etching recipe in the chamber without any sample present to ready the chamber for operation.
- c) Formally initiate the etching recipe with the sample positioned inside the chamber. The recipe involves utilizing a supply power of 200 W, and the pressure within the etching environment is maintained at 50 mTorr. Introduce a flow of 6 sccm Ar and 30 sccm Cl<sub>2</sub>. Etch 100 nm VO<sub>2</sub> for 90 seconds.
- d) Immerse the sample in Acetone to remove the residual resist. Thoroughly rinse the sample with deionized water for 5-10 minutes and then proceed to dry the thin films.

The complete two steps of lithography are shown in Figure 2.7 and Figure 2.8, respectively.

### First lithography step



Spincoat  $\text{VO}_2$   
with PMMA A4



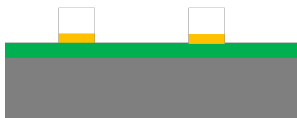
Expose with  
electron beam



Develop



Deposit  
Ti/Au electrodes



Lift-off

Figure 2.7 First lithography step

### Second lithography step

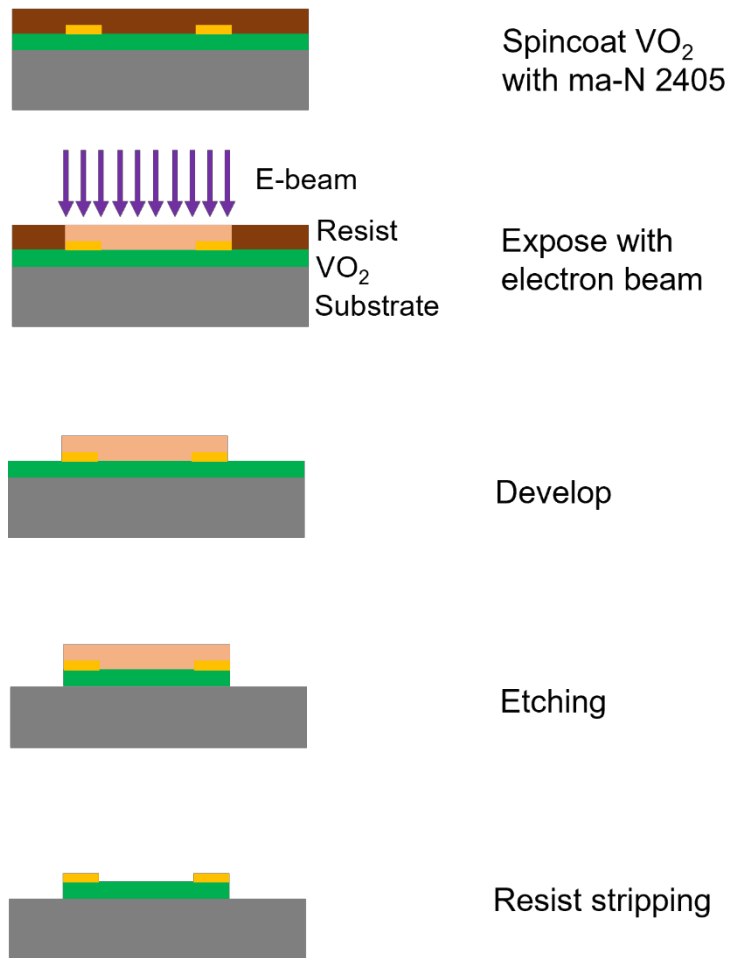


Figure 2.8 Second lithography step

#### 2.3.5 Examination of the fabricated devices

Following the completion of device fabrication, we typically employ two characterization techniques to assess the VO<sub>2</sub> device's quality and gauge any potential damage incurred during the fabrication process. The first method involves utilizing scanning electron microscope (SEM) to scrutinize the device's morphology and geometry. Subsequently, we proceed with electrical transport measurements, specifically examining resistance versus temperature. This step allows

us to compare the electrical behavior of VO<sub>2</sub> both pre- and post-fabrication to determine whether the VO<sub>2</sub> is damaged or not.

## 2.4 Electrical transport measurement

### 2.4.1 Resistance temperature

To characterize the crucial electrical property insulator-to-metal transition of the Mott insulator VO<sub>2</sub>, we conducted resistance versus temperature measurements. These measurements were carried out using a TTPX Lakeshore cryogenic probe station, which offers a temperature range spanning from 78 K to 400 K. This station includes a high vacuum chamber to prevent oxidation and degradation of the sample as it reaches elevated temperatures. In order to avoid heat generation by the sample itself, a fixed small current of 1 μA was employed from a Keithley 6221 current source to drive the VO<sub>2</sub> devices. Monitoring of the resistance across the devices was accomplished using a Keithley 2812 nanovoltmeter. Therefore, we acquired the resistance-temperature relationship while varying the temperature, as illustrated below.

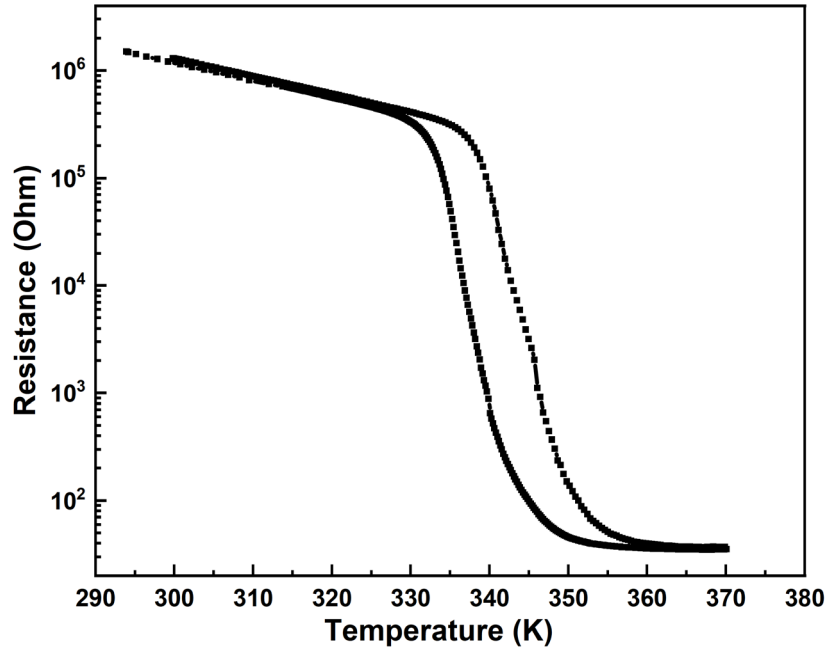


Figure 2.9 Resistance versus temperature of one of VO<sub>2</sub> samples

## 2.4.2 Current source

Upon confirming the insulator-to-metal transition through resistance-temperature measurements, I proceeded to conduct resistive switching measurements capable of alternating device resistance through applied electrical bias. These biases, including current source and voltage source, can induce distinct electrical behaviors. In the current source mode, a ramping current was directed through the device, while voltage source mode involved applying a ramping voltage, both leading to distinct electrical behaviors.

Figure 2.10 illustrates the current-controlled I-V curves for varied base temperatures. As the input current increases, the monitoring voltage across the device also rises. During this stage, VO<sub>2</sub> maintains its insulating state. However, as the input current increases, the joule heating produced by the insulating VO<sub>2</sub> itself keeps pushing the resistance of the device to follow the resistance versus temperature curve. The insulator-to-metal transition occurs once the VO<sub>2</sub> device hits the threshold voltage, signifying sufficient joule heating to trigger the transition. Beyond this point, the monitoring voltage drops as VO<sub>2</sub> becomes metallic. This metallic state persists as the input current rises. However, when reducing the input current, the joule heating can't sustain the metallic state, prompting a shift back to the insulating state. Consequently, the monitoring voltage exhibits an upward jump followed by a decrease. Different base temperatures yield varying threshold voltages, which decrease as the base temperature rises.

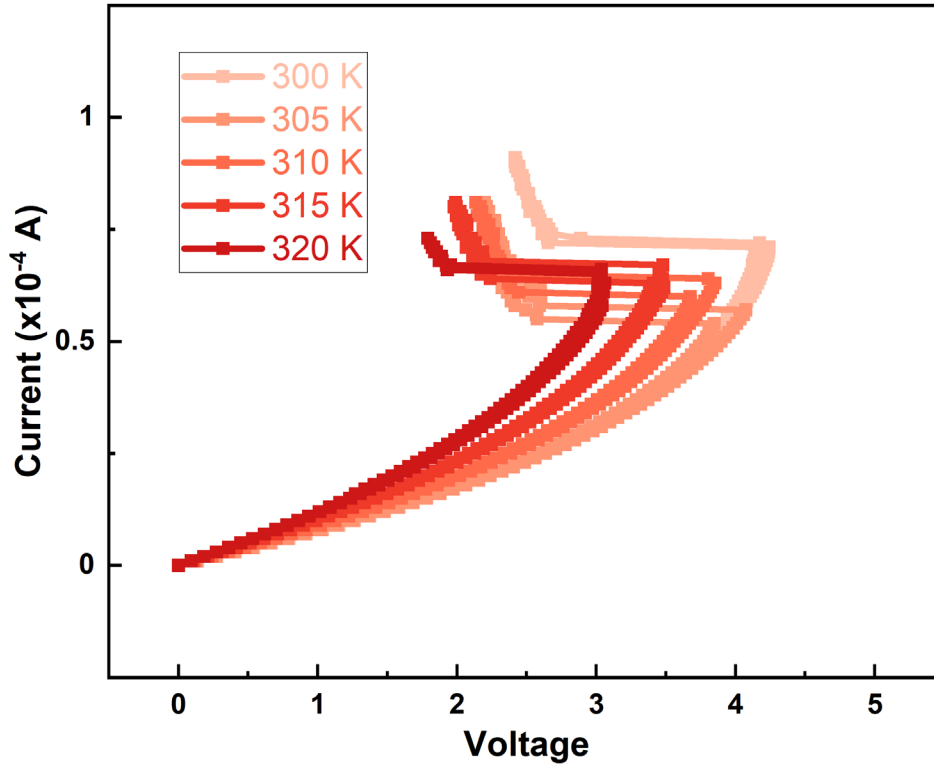


Figure 2.10 Current controlled I-V

### 2.4.3 Voltage source

Similarly, the voltage-controlled I-V curves, presented in Figure 2.11, demonstrate distinct behavior. With increasing input voltage, the monitoring current passing through the device increases. During this stage, VO<sub>2</sub> retains its insulating state. Yet, the joule heating resulting from the insulating VO<sub>2</sub> drives the device's resistance in accordance with the resistance-temperature curve (Figure 2.9) as the input current rises. The insulator-to-metal transition happens upon the device reaching the threshold voltage, where joule heating triggers the transition. Following this juncture, the monitoring current experiences a sharp surge as VO<sub>2</sub> shifts to a metallic state. This metallic state persists as the input voltage increases. However, as the input voltage starts to decline, the joule heating becomes insufficient to maintain the metallic state of VO<sub>2</sub>, causing it to revert to its insulating state. As a result, the monitoring current

displays a downward jump followed by a decrease. Varied base temperatures lead to diverse threshold voltages, which decline with higher base temperatures.

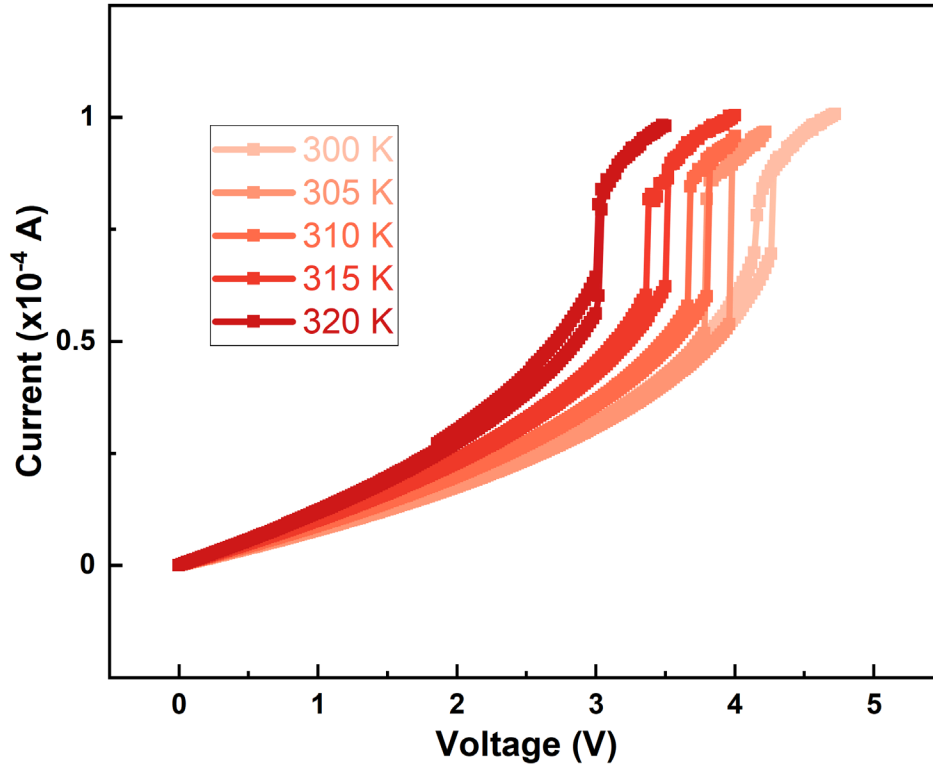


Figure 2.11 Voltage controlled I-V

#### 2.4.4 Time-resolved dynamical measurements

To capture the rapid electrical response of the spiking oscillator, we conducted time-resolved measurements. We employed a Tektronix Dual Channel Arbitrary Function Generator, specifically the AFG 3252C, for applying either DC or pulse voltage bursts to the circuit. The AFG 3252C offers precise waveform generation with remarkably fast rise and fall times of 2.5 nanoseconds. Its dual-channel capability allowed us to independently control the Device Under Test (DUT) while ensuring synchronized output signals to the circuit.

For recording ultrafast electrical dynamic signals, we utilized the Tektronix Oscilloscope MSO54, boasting a maximum bandwidth of 1 gigahertz and sampling rates of 6.25 Gigasamples

per second (GS/s). In our measurement, we typically recorded a time span of 4 milliseconds at a sampling rate of 312.5 Megasamples per second (MS/s). This corresponds to a recording duration of 3.2 nanoseconds per data point. We configured the acquisition mode to high resolution mode, ensuring a minimum of 12 bits of vertical resolution. Specifically, the channel impedance for measuring voltage dynamics was set at 1 megaohm, while the channel impedance for monitoring spiking current dynamics was adjusted to 50 ohms. The input voltage and output voltage dynamics are displayed in Figure 2.12 while Figure 2.13 shows the output current spikes.

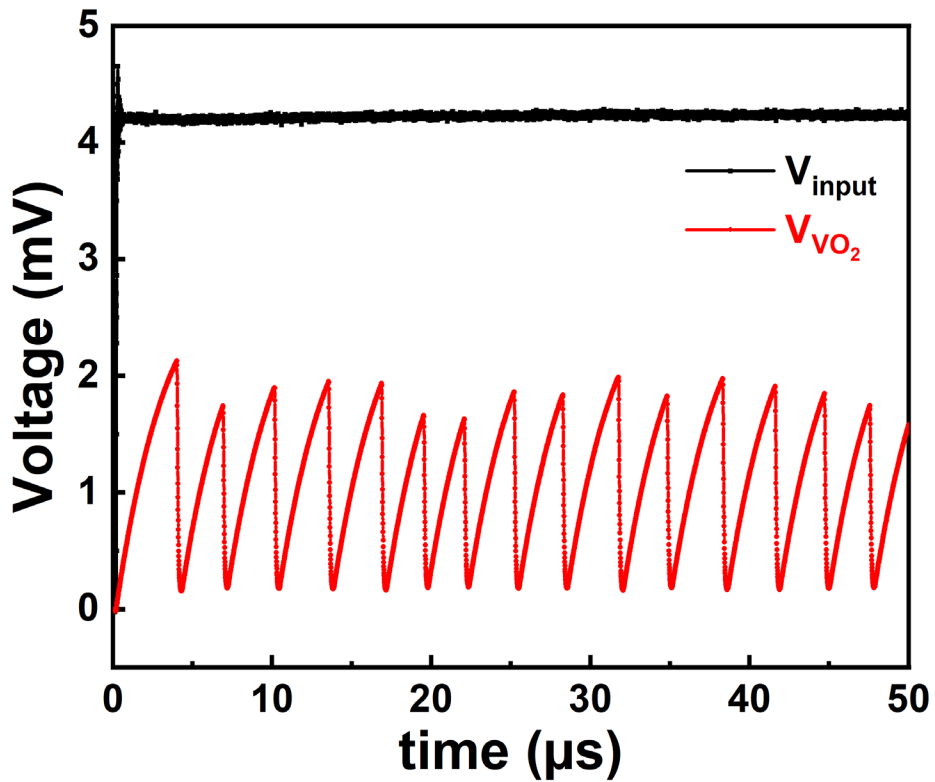


Figure 2.12 Input and output voltage dynamics of one of VO<sub>2</sub> samples



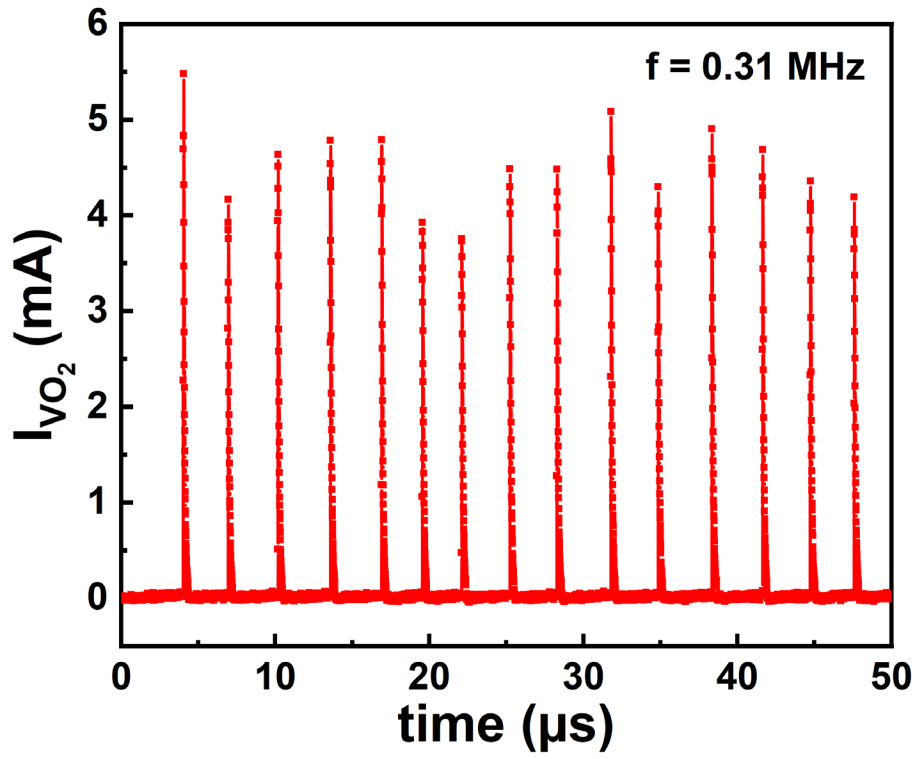


Figure 2.13 Current spikes of one of VO<sub>2</sub> samples

## Chapter 3 Stochastic disruption pattern in capacitively coupled spiking oscillators

### 3.1 Introduction

Oscillator-based computing, an approach of using networks of interacting oscillators for information processing, can provide an efficient alternative to conventional computational algorithms implemented on von Neumann architecture<sup>10</sup>. Demonstrations of oscillator-based computing include networks capable of solving NP-hard combinatorial tasks, such as graph coloring<sup>18,19</sup>, maximum cut<sup>20,21</sup> and maximum independent set<sup>22</sup> problems. Furthermore, oscillator circuits are essential components of hardware-level implementation of spiking neural networks<sup>23,24</sup>. In many practical demonstrations the individual oscillators are implemented using standard CMOS technology<sup>18,21,22,25</sup>. Recently, there has been a great interest in replacing CMOS oscillator circuits with devices based on quantum materials in order to reduce energy consumption and circuit footprint. Several approaches have been proposed including the use of magnetic spin-torque oscillators<sup>26,27</sup> micro- and nanoelectromechanical systems<sup>28-30</sup>, and spiking devices based on electrical triggering of an insulator-metal transition (IMT)<sup>31,32</sup>. The key element that enables oscillator-based computing is the ability to achieve tunable coupling between the individual oscillators.

The implementation of coupling between non-CMOS devices is often complex and could result in a highly non-intuitive dynamical behavior<sup>36-40</sup>. Here we report that increasing the capacitive coupling strength between only two Mott oscillators amplifies the influence of small intrinsic stochasticity leading to an emergent stochastic pattern with spiking sequence disruptions. The observed discrete inter-spike interval (ISI) distributions in coupled Mott nanodevices qualitatively resemble those in biological neurons, which could prove useful for hardware-level implementation of bio-inspired computing systems.

### 3.2 Single stochastic spiking oscillator

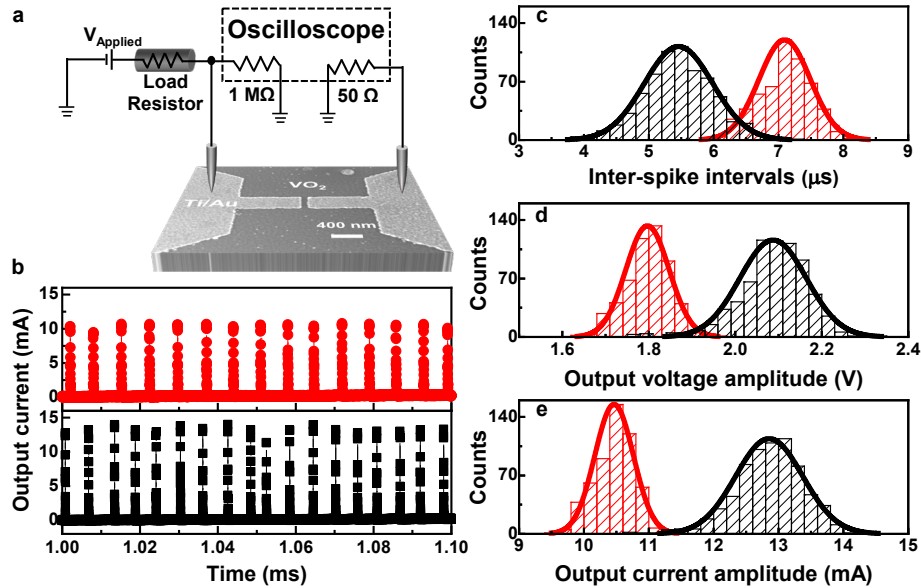


Figure 3.1 Intrinsic stochasticity in independent spiking nanodevices.

(a) Electrical circuit used to measure spiking properties of individual  $\text{VO}_2$  nanodevices. The SEM image shows a  $100 \times 400 \text{ nm}^2$   $\text{VO}_2$  device defined by Ti/Au electrodes. The voltage on the  $\text{VO}_2$  device and the current flow in the circuit were monitored by an oscilloscope. (b) Current time traces showing spiking oscillations in two independent  $\text{VO}_2$  nanodevices. (Red: oscillator A; Black: oscillator B.) (c-e) Distributions of the interspike intervals (c), spike-triggering voltages (d) and spiking currents (e) of the two  $\text{VO}_2$  oscillators shown in (b). Histograms correspond to experimental data and solid lines are Gaussian fits. Small stochasticity of these three parameters is evident.

Volatile resistive switching due to the triggering of an IMT in  $\text{VO}_2$  enables building a simple circuit that emits current spikes in response to a dc applied voltage. In our setup (Figure 3.1), dc voltage produced by a function generator is applied to a  $100 \times 400 \text{ nm}^2$   $\text{VO}_2$  nanodevice that is connected in series with a load resistor. A multichannel oscilloscope was used to monitor the voltage on  $\text{VO}_2$  nanodevices and the current flowing in the circuit. The operation principle of the spiking circuit is as follows. As voltage is applied to the circuit, the potential across the  $\text{VO}_2$  increases controlled by the RC time constant arising from the parasitic capacitance of the setup (estimated as 0.2 nF in our case). When voltage across the  $\text{VO}_2$  reaches a threshold, an insulator-

to-metal resistive collapse is induced, which produces a current surge (spike) in the circuit<sup>101,102</sup>. Because the resistance of VO<sub>2</sub> in the collapsed metallic state is low, most of the applied voltage drops over the load resistor. In this state, a small voltage applied across the VO<sub>2</sub> can no longer maintain the metallic state, causing the device to revert back to the insulating state and the cycle repeats. The spiking frequency (inverse of inter spike interval) can be controlled by adjusting the applied voltage (Figure 3.6), load resistor (Figure 3.7), or temperature (Figure 3.8). In our setup, the process described above resulted in the generation of periodic current spikes with the typical frequencies in the range of 0.1 – 1 MHz as shown in Figure 1b. Although the peak spiking current can be relatively large, ~10 mA, the power consumption per spike event is small, ~1 nJ, because of the extremely short spike width, ~30 ns. (Figure 3.9).

The spiking oscillations in VO<sub>2</sub> display a subtle stochastic behavior. Figure 3.1c shows the inter-spike interval (ISI) statistics for two independent oscillators. The ISI distributions can be fitted by Gaussians, which gives a small, approximately 5-10%, standard deviations of the spike timing with respect to the mean values,  $7.09 \pm 0.40 \mu\text{s}$  for the oscillator A (red color in Figure 1 b-e) and  $5.46 \pm 0.53 \mu\text{s}$  for the oscillator B (black color in Figure 3.1. b-e). Our experimental setup had the time resolution of 312.5 MS/s, which is much faster than the observed deviations of the ISI. We note that the spiking devices A and B are nominally identical, and the differences between them are due to unavoidable device-to-device variability. While minimizing the device-to-device variability requires careful optimization of the fabrication process, the average properties of the spiking devices, such as threshold voltage and spiking frequency, can be tuned by changing the device geometry (gap size and width), film growth conditions or by post-processing ion irradiation<sup>65,103</sup>. The oscillator circuit operates under dc voltage without injecting noise to artificially produce spike timing stochasticity. Therefore, the

measured ISI distributions are related to intrinsic properties of VO<sub>2</sub> nanodevices<sup>31,70,101,102</sup> and are not caused by the measurement uncertainty or external perturbations.

Spike timing stochasticity is often reported in single IMT-based oscillators<sup>31,102</sup> and it has a qualitative resemblance to the jittering in biological neurons<sup>104–107</sup>. Small variations in the spike timing in VO<sub>2</sub> could be related to stochastic relaxation of metallic domains back into the insulating state<sup>70,108,109</sup> resulting in deviations of the IMT triggering voltages in each oscillation cycle. Figure 1d shows the spike-triggering voltage distributions for the two independent VO<sub>2</sub> nanodevices. The spike-triggering voltage is defined as the maximum voltage that builds up on a device before a spike is emitted. Similar to the ISI, the switching voltage distribution can be fitted by Gaussians giving  $1.80 \pm 0.050$  V and  $2.09 \pm 0.077$  V, i.e., 2-4% deviations, for the oscillators A and B, respectively. Because in each oscillation cycle, the spikes are triggered by slightly different voltages, the current amplitudes of the spikes also show a stochastic distribution (Figure 3.1e). Although the cycle-to-cycle deviations of the spiking parameters (ISI, spike-triggering voltage, current amplitude) in the individual VO<sub>2</sub> nanodevices are relatively small, the intrinsic spiking stochasticity can have a strong impact on the behavior of the coupled oscillators as we demonstrate in this work.

### 3.3 Capacitively coupled spiking oscillators

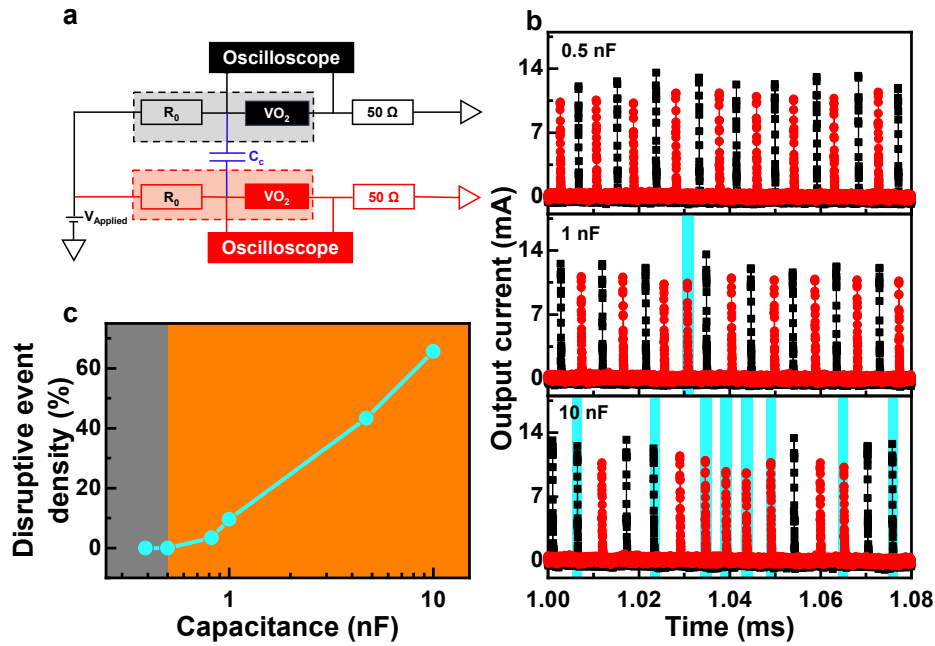


Figure 3.2 Synchronization behavior of two coupled spiking oscillators.

(a) Electrical circuit for spike synchronization of two oscillators. The synchronization was achieved by connecting two VO<sub>2</sub> nanodevices using a coupling capacitor (highlighted by blue color). The load resistors R<sub>0</sub> for both oscillators are 20 kΩ. (b) The overlaid current time traces of two spiking oscillators show the synchronization patterns obtained for different values of the coupling capacitance. Small coupling capacitance (top panel) leads to a perfect alternating spiking sequence. Increasing the coupling capacitance (middle and bottom panels) results in stochastic disruptions of the alternating sequence in which one oscillator emits multiple sequential spikes (highlighted by green stripes). (c) Disruption event density (the total number of disruption events per total number of spikes) as a function of coupling capacitance.

Connecting two independent VO<sub>2</sub> spiking oscillators using a coupling capacitor (Figure 3.2a) allows synchronizing the oscillators' frequency and phase. When the coupling capacitor is small (below 0.5 nF), the synchronized oscillators display a deterministic alternating spiking sequence (Figure 3.2b, top panel), which is consistent with multiple previous reports<sup>110–112</sup>. One might intuitively assume that the larger the coupling capacitance, the larger the coupling strength, and, consequently, the synchronization between the two spiking devices is more robust. Our measurements, however, show that increasing the coupling capacitance leads to the

emergence of stochastic disruptive events in the synchronization pattern. The middle and bottom panels in Figure 3.2b show the spiking current time traces of two VO<sub>2</sub> oscillators coupled using 1 nF and 10 nF capacitors, respectively. While the coupled nanodevices generate an overall periodic spiking, the alternating sequence is often disrupted by stochastic events when one of the oscillators (A or B) emits multiple sequential spikes. These stochastic disruption events are highlighted using green shaded stripes in Figure 3.2b. The stochastic disruption events can be also observed when we increase the applied voltages but a fixed coupling capacitor in Figure 3.10. The density of the disruption events (i.e., the total number of disruption events per total number of spikes) increases with increasing the coupling capacitance as shown in Figure 3.2c. The circuit RC constant increases with increasing the coupling capacitance, which, in turn, causes a proportional inter-spike interval increase (Figure 3.11). This implies that the circuit electrical inertia is the primary parameter determining the spiking dynamics for the coupled oscillators. It can be expected that if the parasitic capacitance becomes larger and the spiking frequency decreases, a larger coupling capacitor would be needed to synchronize the oscillators.

We note that the data presented in the figures were recorded in the same pair of VO<sub>2</sub> nanodevices and the only modification needed to induce stochastic disruption events in the alternating spiking sequence was increasing the coupling capacitance. Figure 3.2b shows only 80 μs time window of the spiking current traces to facilitate visual separation of individual spikes. Experimentally recorded traces were 4 ms long containing hundreds of spikes and the emergence of disruption events was observed throughout the entire recording time. A few examples of different time windows similar to data in Figure 3.2a are shown in Figure 3.12, Figure 3.13, Figure 3.14. We observed similar behavior in multiple pairs of different VO<sub>2</sub> nanodevices (Figure 3.15), therefore the emergence of disruption events in the deterministic alternating

spiking sequence is not accidental, but rather a general property of these coupled spiking oscillators. As we describe below, the origin of the observed alternating sequence disruptions stems from the interplay between the small intrinsic cycle-to-cycle stochasticity present in our VO<sub>2</sub> devices and the nature of coupled spiking systems, in which very short-time interactions occurring during the spike emission make the system highly susceptible to fluctuations.

### 3.4 Inter-spike interval distribution in capacitively coupled spiking oscillators

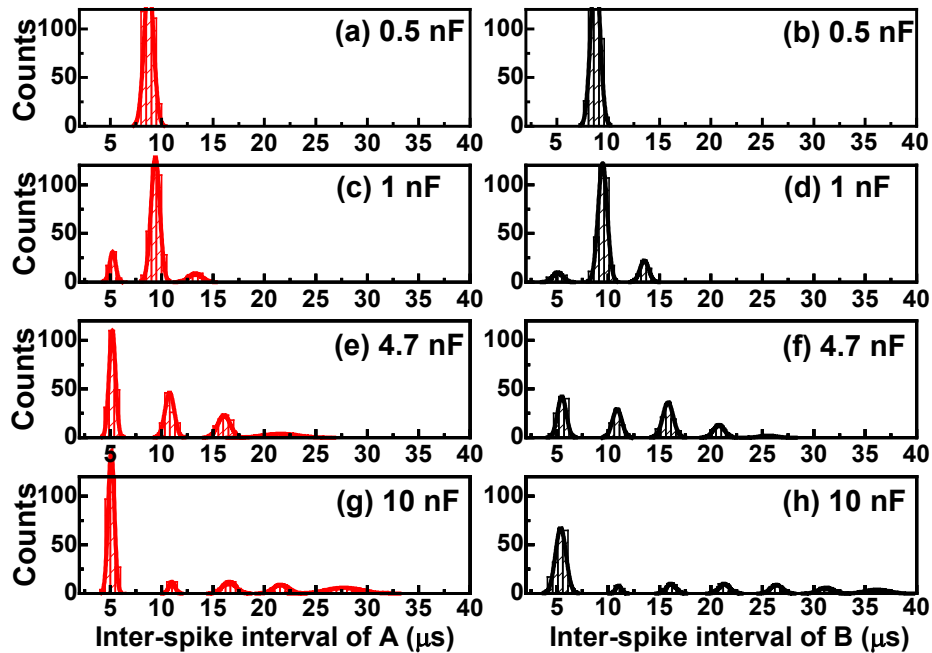


Figure 3.3 ISI distribution in coupled spiking oscillators.

(a-h) Statistical analysis of the ISI distributions of two coupled VO<sub>2</sub> spiking oscillators. The histograms are experimental data and lines are Gaussian fits. Same red and black coloring convention is used in the plots as in the previous figures. Perfectly alternating spiking sequence produces single ISI peak (a and b). The disruption events in the spiking sequence caused by increasing the coupling capacitance lead to the emergence of satellite peaks at multiples of the main ISI peak (c-d). At extreme coupling capacitance values (e-h), alternating spiking bursts become the dominant spiking pattern, which results in the pronounced ISI peak at a half-integer value of the alternating sequence ISI.



The disruptions of deterministic alternating sequence of the coupled spiking oscillators lead to an emergent stochastic pattern. Figure 3.3 shows the ISI statistics evolution of the two oscillators coupled using different capacitors. For a small coupling capacitor (0.5 nF, top panels), the ISI of both oscillators has only a single peak corresponding to the alternating spiking synchronization. As the coupling capacitor increases (1 nF and 4.7 nF, middle panels), satellite peaks emerge at multiples of the main ISI peak, corresponding to the emergent stochastic pattern. With the largest capacitor (10 nF, bottom panel), the most pronounced distribution peak shifts to half of the alternating spiking period, which indicates that alternating spiking bursts (i.e., several consecutive spikes of one oscillator followed by several consecutive spikes of the second oscillator) become the most prominent spiking pattern. The stochastic pattern in coupled VO<sub>2</sub> oscillators, caused by alternating sequence disruptions, qualitatively resembles those in biological sensory neurons<sup>113–116</sup>, which is argued to be an important feature for processing information from different sensory modalities in the nervous system. Thus, our results could find applications in expanding the range of biologically plausible behaviors that can be emulated using IMT-based spiking oscillator devices<sup>20,117–119</sup>.

### 3.5 Voltage dynamics of the capacitively coupled spiking oscillators

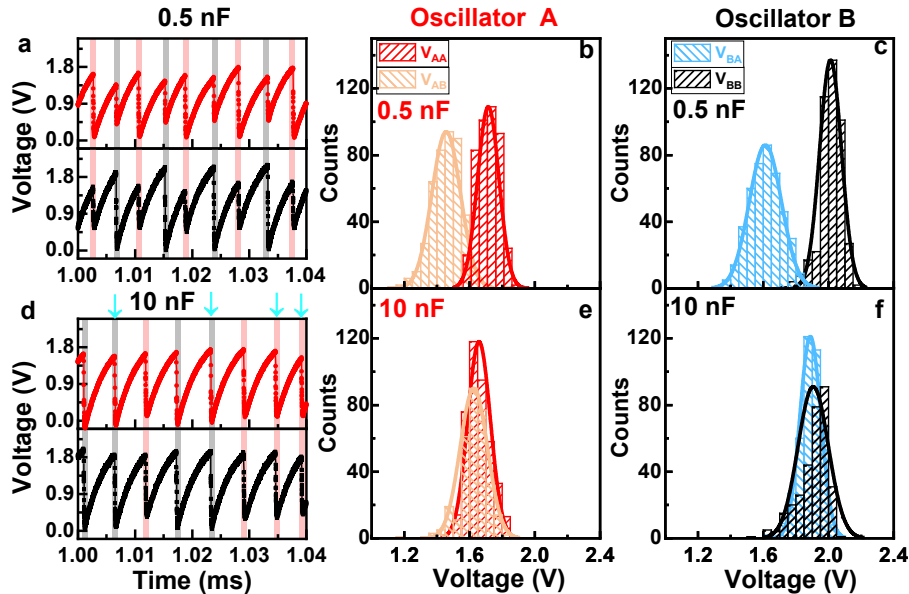


Figure 3.4 Voltage dynamics of coupled spiking oscillators.

(a,d) Voltage time traces of two VO<sub>2</sub> spiking nanodevice coupled using 0.5 nF (a) and 10 nF (d). Same red and black coloring convention is used in the plots as in the previous figures. Pink and grey shaded stripes highlight the spikes by the oscillators A and B, respectively. Blue arrows highlight disruption events. For a small coupling capacitance (a), one oscillator discharges only partially when the other one spikes. For a large coupling capacitor (d), both oscillators discharge nearly completely when one of them emits a spike. (b,c,e,f) Statistical analysis of the spike-triggering voltages. Histograms correspond to the experimental data and lines are Gaussian fits.  $V_{AA}$  and  $V_{BB}$  are voltages that trigger spikes in devices A and B, respectively.  $V_{AB}$  and  $V_{BA}$  are voltages on one device, A or B, when the other one, B or A, emits a spike. For small coupling capacitance (b,c), the distributions corresponding to the two types of voltages are well separated allowing perfect alternating spiking sequence. For large coupling capacitance (e,f), the distributions overlap making the spiking probability of oscillator A or B nearly identical, which results in stochastic disruptions of the alternating spiking sequence.

To understand the origin of stochastic disruptions of the deterministic alternating spiking sequence we investigated voltage dynamics in the circuit. Figure 3.4a shows voltage time traces of two VO<sub>2</sub> nanodevices coupled with a small capacitor of 0.5 nF. The pink and grey shaded stripes highlight which oscillator, A or B, emits a spike. An oscillator spikes when the voltage reaches the threshold to trigger the IMT in VO<sub>2</sub>. Because of the subtle intrinsic stochasticity of

the IMT triggering, the threshold voltage displays small cycle-to-cycle variations (Figure 3.16, Figure 3.17) producing proportional variations in spike current amplitudes (Figure 3.18). When a spike is emitted by oscillator A, its voltage discharges nearly to zero. At the same time, the voltage in the oscillator B also discharges, but only partially. This partial discharge is due to an extra current flow through the small coupling capacitor. In the next cycle, the charging of oscillator B is far ahead of oscillator A, assuring that the next spike is emitted by the oscillator B. As a result, synchronized deterministic alternating spiking sequence is produced when the two devices are coupled using a small capacitance.

Figure 3.4b and c show the statistical distribution of the  $VO_2$  voltages at the moments of the spike emission. We distinguish two cases: (i) voltage on a  $VO_2$  nanodevice when it emits a spike ( $V_{AA}$  or  $V_{BB}$ ), (ii) voltage on the  $VO_2$  nanodevice when the other oscillator emits a spike ( $V_{AB}$  or  $V_{BA}$ ). It is evident that when the two oscillators are coupled with a small capacitor, the two types of voltages are well separated,  $V_{AA} > V_{AB}$  and  $V_{BB} > V_{BA}$ . In other words, when one device spikes the voltage on the other one is far below the IMT triggering threshold. In contrast, when the oscillators are coupled by a large capacitor, such as 10 nF, it is no longer possible to distinguish between  $V_{AA}$  and  $V_{AB}$  and between  $V_{BB}$  and  $V_{BA}$ . When one oscillator spikes and discharges, the other oscillator also discharges almost completely because the large coupling capacitor allows a large current flow between the two  $VO_2$  devices (Figure 3.4d). Because both oscillators begin each cycle from a discharged state, they arrive at the IMT threshold at approximately the same time, which results in the overlap of  $V_{AA}$  and  $V_{AB}$  as well as  $V_{BB}$  and  $V_{BA}$  distributions (Figure 3.4e and Figure 3.4f). When both  $VO_2$  devices are on the verge of the IMT, it becomes indeterminate which oscillator, A or B, would emit a spike. Therefore,

alternating A-B spiking or consecutive A-A or B-B spiking are possible when the oscillators are coupled by a large capacitance.

### 3.6 Numerical simulations

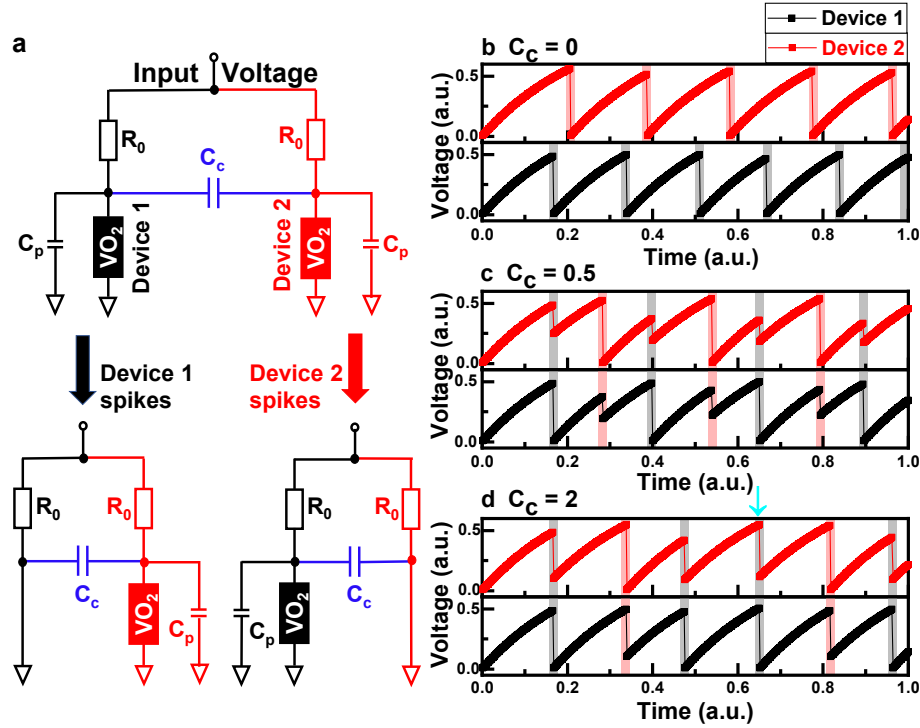


Figure 3.5 Simulations of synchronized stochastic spiking oscillators.

(a) The circuit schematically shows the simulation procedure. The model considers that the device turns into a short (i.e. switches into a low resistance state) when the device emits a spike. (b-d) Simulated voltage dynamics for different values of coupling capacitance  $C_c$ . Pink and grey shaded stripes in the plots highlight the spiking events produced by one or the other oscillator. Blue arrow highlight a disruption event. The oscillators are not synchronized when  $C_c = 0$  (b). The oscillators show a synchronized alternating sequence when  $C_c = 0.5$  (c). The alternating sequence is disrupted when  $C_c = 2$  (d). In (b, c, d), time, voltage and capacitance values are in arbitrary units.

Numerical simulations further corroborate the importance of small  $\text{VO}_2$  intrinsic stochasticity in the spiking properties of coupled oscillators. We modeled the experimental circuit by considering  $\text{VO}_2$  devices as lumped elements that can switch between high and low

resistance states under an applied voltage (Figure. 3.5a). The voltage- and time-dependent probability of the switching was introduced as

$$P(V, t) = 1 - \frac{1}{1 + t \exp[(V - V_{th})/\delta V]}, \quad (1)$$

where  $V_{th}$  is the instantaneous threshold voltage and  $\delta V$  describes the stochastic range. Eq. (1) was previously found to provide excellent fit for the experimental data of switching probability in VO<sub>2</sub> devices<sup>120</sup>. To enable self-oscillations in the simulated circuit, we introduced capacitors  $C_p$  connected in parallel to the VO<sub>2</sub> devices, which emulates the parasitic capacitance of the experimental setup. At the beginning of each oscillation cycle, the  $C_p$  capacitor charges producing gradual voltage buildup on the VO<sub>2</sub> device, thus increasing the probability of high-to-low resistance switching in accordance with Eq. (1). When switching is induced,  $C_p$  fully discharges resetting the voltage on the VO<sub>2</sub> device. The two VO<sub>2</sub> devices considered in the simulations had 10% different threshold voltages, therefore the natural oscillation frequencies differ when the devices are uncoupled, i.e., when  $C_c = 0$  (Figure 3.5b). When a small coupling capacitance is introduced ( $C_c = 0.5$ ), the oscillators synchronize and display an alternating spiking sequence (Figure 3.5c). This synchronization is due to the partial discharge of one oscillator when the other oscillator switches into the low resistance state. The remaining charge on one device when the other device switches can be written as

$$Q = Q_f \frac{C_p}{C_p + C_c}, \quad (2)$$

where  $Q_f$  is the accumulated charge on the device at the moment just prior to the switching of the other device. Eq. (2) shows that the larger the coupling capacitance, the stronger the discharge effect, i.e., the difference between  $Q_f$  and  $Q$ . When the coupling capacitor is large enough, both oscillators start the charging sequence from a relatively low level and arrive at the

switching conditions almost simultaneously. In such a case, it becomes random which device undergoes the switching and the alternating oscillations pattern is often disrupted by one device switching multiple times in a row (Figure 3.5d), reproducing well the experimental observations. We note that these disruptions in the alternating oscillation sequence cannot be achieved in the simulations if the two VO<sub>2</sub> devices switch at deterministic threshold voltages. The key aspect of the simulations that allowed reproducing the experimental results is the assumption of inherent stochasticity in the resistive collapse of VO<sub>2</sub> nanodevice.

### 3.7 Conclusion

We demonstrated that increasing the strength of capacitive coupling between spiking Mott oscillators results in stochastic disruptions of the deterministic alternating spiking sequence. We show that this effect is caused by the slight, unavoidable intrinsic stochasticity of spiking oscillators. Non-intuitive synchronization, such as oscillation clustering and chimera states, is often observed in large networks of coupled oscillators, which could stem from nonlinear and nonlocal coupling, coupling delay, network geometry and heterogeneity, etc<sup>121–127</sup>. The important result of our work is that stochastic disruptions of the alternating oscillation sequence already emerge on the level of a single pair of a strongly coupled spiking oscillators, in stark contrast to a pair of harmonic oscillators where increasing coupling strength produces more robust synchronization. Understanding unique features of spiking oscillators becomes extremely important with the advent of neuromorphic computing and particularly relevant to recent interest in spiking neural network<sup>23,128,129</sup>. Specifically, we point out that coupling between individual devices could lead to an emergent stochastic behavior as shown in this work. This might be a useful feature in large scale spiking neural networks to produce desirable such as found in

biological systems<sup>130</sup>. Stochastic coupling in spiking oscillators might also find applications in stochastic computing for the development of stochastic bit generation sources<sup>131–133</sup>.

### 3.9 Acknowledgments

Chapter 3, in full, is a reprint of the material as it appears in the publication: Erbin Qiu\*, Pavel Salev, Lorenzo Fratino, Rodolfo Rocco, Henry Navarro, Coline Adda, Junjie Li, Min-Han Lee, Yoav Kalcheim, Marcelo Rozenberg, and Ivan K. Schuller, Stochasticity in the synchronization of strongly coupled spiking oscillators. *Appl. Phys. Lett.* 122, 094105 (2023).

The dissertation author was the primary investigator and corresponding author of this paper.

#### **Author contributions:**

E.Q. and I.K.S. conceived the project. E.Q. fabricated the samples and performed all the measurements. L.F., R.R and M.R. performed the numerical simulations. All authors participated in the discussion and interpretation of the results. E.Q., P.S. and I.K.S. wrote the manuscript with input and corrections from all authors. I.K.S. supervised the project.

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## Chapter 4 Stochastic synchronization in thermally coupled oscillators

### 4.1 Introduction

Synchronization is a universal behavior that is commonly observed in a variety of natural and engineered systems<sup>134</sup>. In natural systems, synchronization ranges from collective oscillations in bacteria<sup>135</sup> to beating of cilia<sup>136</sup>, from rhythms in biological neurons<sup>137,138</sup> to phase synchronization in the brain<sup>139,140</sup>. Synchronization emerges in engineered physical systems of interacting oscillators, such as nanomechanical and nanoelectromechanical oscillators<sup>36,40,141,142</sup>, spin Hall and spin torque nano-oscillators<sup>38,143–145</sup>, chemical oscillators<sup>146–148</sup>, etc.

With the recent advent of biologically inspired computing, synchronization between special type of oscillators that produce short-duration spikes (in contrast to smoothly evolving harmonic oscillators) has attracted significant attentions<sup>149–151</sup>. Spiking oscillators can emulate the electrical activity of brain<sup>31,33</sup> and can find applications in the development of hardware-level energy-efficient implementations of neural networks<sup>23,34,35</sup>. Recently we showed that increasing the coupling strength between the anti-phase synchronized spiking oscillators leads to synchronization disruptions<sup>151</sup>, contradicting naïve expectations based on the typical behavior of harmonic oscillators in which stronger coupling develops more robust synchronization. The stark differences between the spiking and harmonic oscillators motivate extensive studies of synchronization phenomena in spiking devices driven by different types of interactions.

This work presents an investigation of the synchronization evolution in coupled spiking nano-oscillators based on a Mott material where strong thermal interactions promote in-phase synchronization. We observed the occurrence of unique spiking patterns controlled by a DC voltage applied independently to each oscillator. For small or large applied voltages, the oscillators develop robust 2:1 or 1:1 integer synchronization spiking modes. However, in a



relatively wide range of intermediate applied voltages, the oscillators enter a stochastic synchronization regime where the spiking pattern unpredictably alternates between the two discrete integer synchronization modes. These findings highlight unique dynamic synchronization properties of spiking oscillators as compared to conventional harmonic oscillators. The ability to electrically control the synchronization modes and drive the coupled spiking devices into a stochastic synchronization regime is important for practical implementations of neuromorphic and stochastic computing circuits.

#### 4.2 Heat propagation between nanodevices

We studied spike synchronization in VO<sub>2</sub> nanodevices. VO<sub>2</sub> undergoes an insulator-to-metal transition at  $T_c = 340$  K that can be also triggered by application of an electric stimulus, voltage or current<sup>152,153</sup>. A 100 nm thick VO<sub>2</sub> thin film was deposited on a (012)-oriented Al<sub>2</sub>O<sub>3</sub> substrate by reactive rf magnetron sputtering. Specular x-ray diffraction analysis revealed textured film growth along (110) crystallographic direction (Figure 4.5). The film had a sharp insulator-to-metal transition with  $\sim 2$  orders of magnitude resistance change across  $T_c$  (Figure 4.6). The film was patterned into 500×500 nm<sup>2</sup> devices separated by 500 nm gaps as shown in Figure 4.1a. The VO<sub>2</sub> between the devices was etched to electrically isolate each device. Although the nanodevices are electrically decoupled (Al<sub>2</sub>O<sub>3</sub> is a good electrical insulator), they are thermally coupled through the substrate (Al<sub>2</sub>O<sub>3</sub> is a good thermal conductor).

Heat propagation is observed by measuring the resistance change  $\Delta R$  in different nanodevices when one of the neighboring nanodevice is powered with a significant current. This way the powered device acts as a heat generator, while resistance of the surrounding devices serves as probe of the temperature change caused by the heat transfer through the Al<sub>2</sub>O<sub>3</sub> substrate. A small 1  $\mu$ A current was applied to measure the resistance of the probe devices. Such

a small probing current generates negligible heat and does not induce by itself any noticeable resistance change.

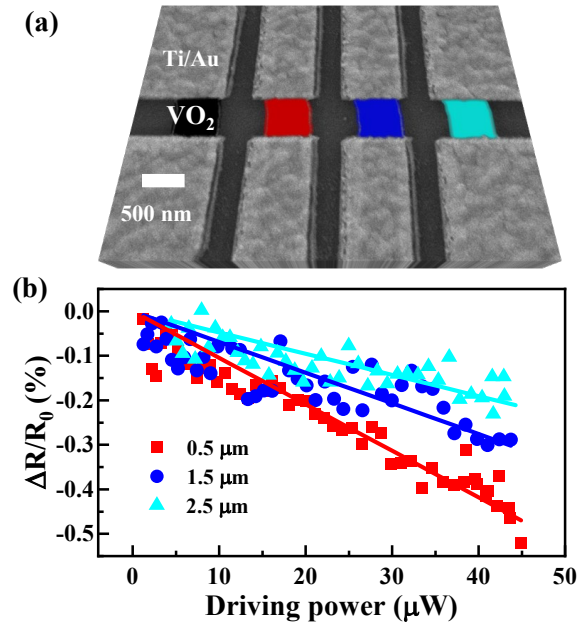


Figure 4.1 Heat propagation between nanodevices.

(a) SEM image with false color of four neighboring VO<sub>2</sub> devices. Each device is 500×500 nm<sup>2</sup>. The devices are separated by a 500 nm gaps and are electrically isolated from each other. The first device (black) acts as a “heat generator”, while the other three (red, blue, and cyan) are “probes”. (b) Normalized resistance changes ( $\Delta R/R_0$ ) of the second, third and fourth devices as a function of dissipated power in the first device. The measurements were performed at 327 K base temperature. The resistance decrease with increasing driving power indicates heat propagation from the first device that increases the temperature of the other devices.

We observed that as the power applied to the heat generator device increases (black device in Figure 4.1a), the resistances of the neighboring devices decrease linearly (Figure 4.1b). The resistance of the closest probe device (500 nm distance, red device in Figure 4.1a) is reduced by ~0.5% at 45  $\mu\text{W}$  power dissipated in the generator device. Comparing this resistance reduction to the equilibrium resistance-temperature dependence (Figure 4.6), temperature increase of the closet probe device can be estimated as ~0.1 K. The temperature increase of the

probe devices located further away from the generator device, as expected, is smaller, estimated as  $\sim 0.06$  K at 1500 nm distance and  $\sim 0.03$  K at 2500 nm distance. Detailed resistance-temperature mapping is shown in Suppl. Information (Figure 4.7). The small temperature increase in the probe devices under the employed measurement conditions explains the linear resistance-power dependence in Figure 4.1b. For higher driving power, the resistance change becomes nonlinear and even displays signatures of the electrical triggering of insulator-to-metal phase transition and filament formation (Figure. 4.8).

### 4.3 Synchronization of spiking oscillators via thermal interaction

Spiking auto-oscillations under the application of dc voltage can be produced using a simple circuit shown in Figure. 4.2a<sup>59,151,154,155</sup>. Individual dc voltage sources power each VO<sub>2</sub> nanodevice. Each nanodevice is connected in series with a load resistor and a 50  $\Omega$  input impedance oscilloscope channel to monitor current spikes. At the instant when dc voltage is turned on, voltage over the initially insulating VO<sub>2</sub> nanodevice begins to increase. The voltage increases dynamically and consequently the spiking frequency is set by the RC constant of the circuit where the reactive component is due to the parasitic capacitance (estimated as 0.2 nF). When voltage across the nanodevice reaches a threshold, the device transitions into the metallic state which produces a current surge (i.e., a spike) in the circuit. When VO<sub>2</sub> is in the metallic state, most of the applied voltage drops across the load resistor. As only a small voltage is applied across the VO<sub>2</sub>, the metallic state cannot be sustained and VO<sub>2</sub> reverts back to the insulating phase. Then the cycle repeats and persistent generation of spiking auto-oscillations is established.

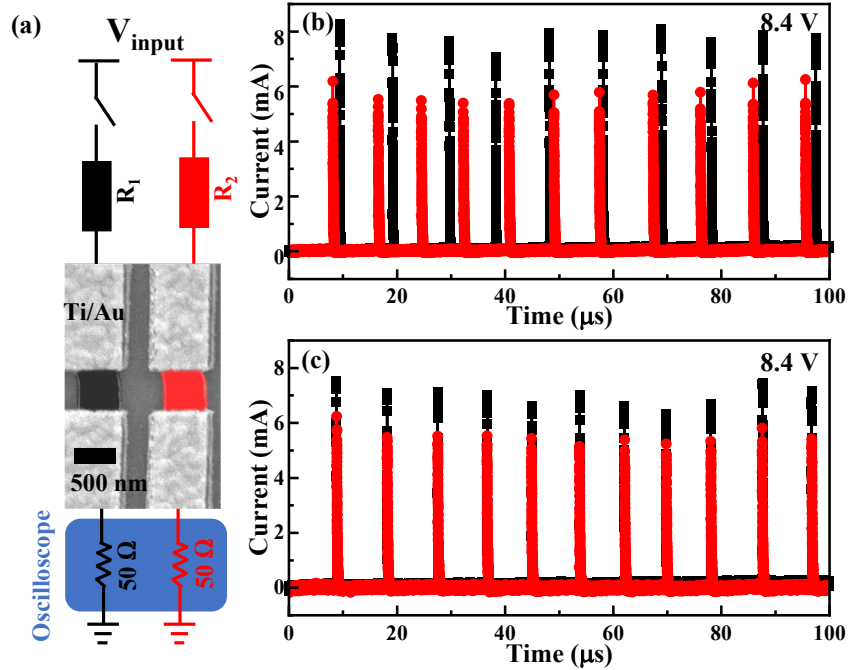


Figure 4.2 Synchronization of spiking oscillators via thermal interaction.

(a) Electrical circuit used to generate spiking oscillations in VO<sub>2</sub> nanodevices. The SEM image shows two neighboring VO<sub>2</sub> nanodevices. (b) Overlaid current traces showing incoherent spiking in two *non-interacting* VO<sub>2</sub> nano-oscillators when they are biased with 8.4 V independently in two separate measurements. (c) Current traces showing coherent in-phase spiking in the same pair of nano-oscillators as in (b) when they are biased with 8.4 V simultaneously.

Thermal interactions due to the very close physical proximity of the devices promote spike synchronization. When two neighboring oscillators (500 nm separation) are powered individually one at a time with the same voltage of 8.4 V, their inter-spike intervals (ISI) are different, 8.39 μs and 9.89 μs. Overlaying the individually recorded spike current time traces produces an incoherent pattern (Figure 4.2b). When two neighboring devices are biased with 8.4 V simultaneously, robust in-phase 1:1 current spiking synchronization establishes (Figure 4.2c), consistent with the previous report<sup>156</sup>. We note that resistance between the etched VO<sub>2</sub> nanodevices was higher than the measurement limit (10<sup>11</sup> Ω) excluding direct electrical current exchange, while capacitive coupling promotes anti-phase synchronization<sup>149</sup> inconsistent with

our observations. Because we observed thermal interactions in the dc measurements (see Figure 4.1b and the corresponding discussion), it is reasonable to conclude that the spike synchronization is also driven by thermal interactions. When one device spikes, the heat generated by the current surge propagates to the neighboring device through the sapphire substrate. As the temperature of the neighboring device increases, it approaches the insulator-to-metal transition, which reduces the threshold voltage for the generation of a current spike. Therefore, when one device spikes, it becomes favorable for the neighboring device to spike as well producing the observed 1:1 in-phase synchronization.

When the distance between nano-oscillators increases, the thermal coupling between them decreases weakening the synchronization. Application of an above threshold voltage simultaneously to two nanodevices separated by 1500 nm (first and third devices in Figure 4.1a), produces unstable synchronization. As shown in Figure 4.9, a sequence of several current spikes can be synchronized (i.e., the spikes overlap) while the following spike sequence can be incoherent. At the extreme, two nanodevices at the opposite corners of the sample (~14 mm distance) have completely incoherent current spike sequences when powered simultaneously (Figure 4.10). The above observations perfectly follow the expectation for the thermal coupling origin of the synchronization in our spiking nano-oscillators.

#### 4.4 Synchronized spiking pattern evolution

Varying the driving voltage individually on each nano-oscillator leads to the synchronization mode transition as shown in Figure 4.3. When the applied voltages are close (for example, 10 V and 9.2 V, Figure 3c), the two devices spike simultaneously, i.e., the synchronization mode is 1:1, similar to the results discussed in the above paragraphs. When one device is powered with a considerably larger voltage than the other one, a different

synchronization mode emerges (Figure 4.3a and Figure 4.3c): every second spike of the high-voltage oscillator coincides with a spike of the low-voltage oscillator, i.e., a 2:1 mode. We note that by fixing voltage on one device and adjusting voltage on the other or vice versa, 2:1 or equivalent 1:2 integer synchronization modes can be established (compare panels a and c in Figure 4.3), which highlights the generality of this one-to-two spikes synchronization.

One can expect that as the applied voltages change from the values favoring 2:1 mode to that favoring 1:1 mode, the spikes would first decohere and then lock into the new mode. We found, however, that the transition between the two integer synchronization modes in spiking nano-oscillators occurs through an unusual stochastic synchronization regime. Panels d and e in Figure 4.3 show that at intermediate applied voltages, the spikes emitted by the two nanodevices are still synchronized, i.e., the spikes always coincide and show no signs of decoherence, but no stable spiking pattern over prolonged time can be discerned. This stochastic synchronization is qualitatively different from the chaotic spiking that has been reported in the MIT-based nano-oscillators<sup>157</sup> as the spikes emitted in our devices occur at well-defined time intervals. Instead of chaotic or de-synchronized oscillations, the spike sequence in our experiments might show the 1:1 pattern, and then unpredictably break with the occurrence of a 2:1 pattern.

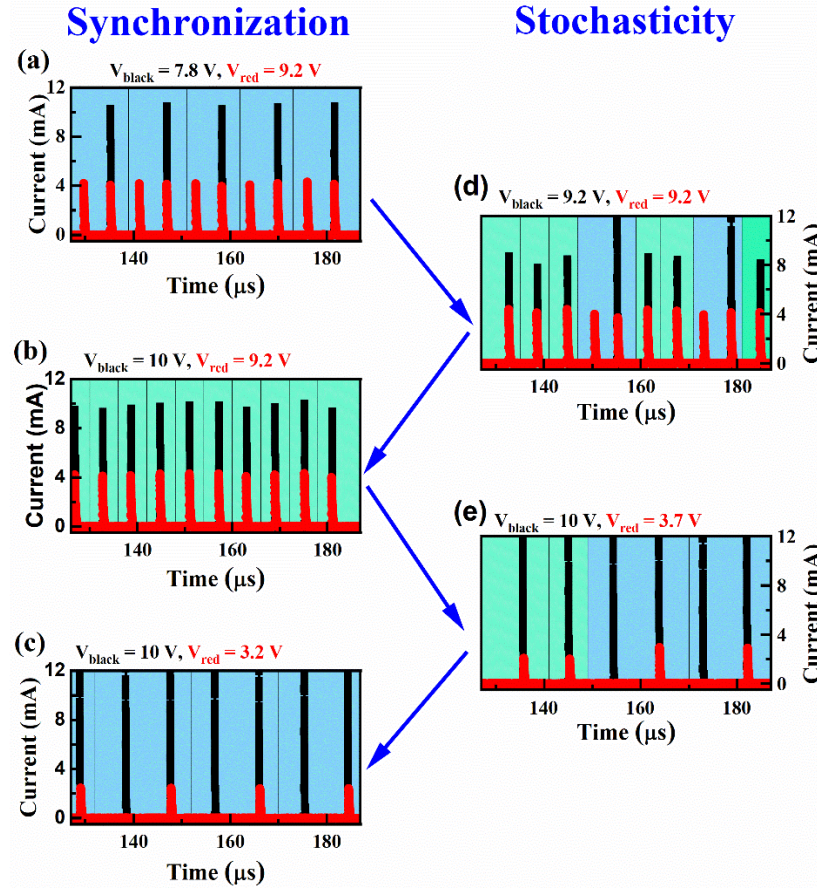


Figure 4.3 Synchronized spiking pattern evolution.

Current traces displaying spiking oscillations of two VO<sub>2</sub> nanodevices under different applied voltages. (a) 2:1 synchronization: two red spikes are locked to one black spike when 9.2 V is applied to the red oscillator and 7.8 V is applied to the black oscillator. (b) 1:1 synchronization: each red spike locks into each black spike when 9.2 V is applied to the red oscillator and 10V to the black oscillator. (c) 1:2 synchronization: one red current spike locks into every second black spike when 3.2 V is applied to the red oscillator and 10 V is applied to the black oscillator. (d, e) Stochastic synchronization emerges at transitions between the modes at intermediate applied voltages. While spikes of the two oscillators overlap, random length spiking sequences corresponding to 2:1 and 1:1 modes (highlighted by green and blue backgrounds, respectively) emerge at random positions.

It is important to note that the stochastic synchronization found here in closely spaced nano-oscillators is in stark contrast to the behavior in micron-size spiking devices. In the micron-size devices the transition between 2:1 and 1:1 modes occurs by the development of intermediate non-integer 3:2 and 4:3 modes<sup>156</sup>. In our case, the stochastic synchronization between integer

modes replaces the transient non-integer modes. We observed the stochastic synchronization in multiple device pairs located in different parts of the VO<sub>2</sub> sample and in multiple samples with different device geometry (Figure 4.11 and Figure 4.12). This robust reproduction of the same phenomenon between different devices and samples suggests that stochastic synchronization could be a general feature in spiking nano-oscillators. Although further studies are necessary to identify critical parameters enabling the stochastic synchronization, it is likely that nanoscale sizes (i) make the devices susceptible to fluctuations and (ii) allow strong thermal interactions because of the very close proximity as compared to the microscale devices. Our theoretical modeling further supports that the intrinsic stochasticity, i.e., cycle-to-cycle variations of the MIT triggering threshold, and strong thermal coupling promote stochastic synchronization at the transition between 1:1 and 2:1 modes (Figure 4.15), while lowering the thermal coupling strength, e.g., by increasing the separation between the devices, results in non-integer synchronization patterns (Figure 4.16).

Synchronization transitions in oscillator systems often display similarities to phase transitions<sup>147</sup>. Spatial phase coexistence is the basic feature of the 1<sup>st</sup> order phase transition. The stochastic transition between the 2:1 and 1:1 integer synchronization spike sequences in our nano-oscillators could be a manifestation of a time domain phase coexistence that develops at the transition between the two integer synchronization modes. Further experimental studies are necessary, however, to test if the synchronization transition in the coupled spiking oscillators exhibits other features of the 1<sup>st</sup> order phase transition, such as hysteretic 2:1 → 1:1 → 2:1 behavior and critical scaling phenomena.



## 4.5 Stochastic synchronization regime

For a quantitative characterization of stochastic synchronization, we analyze the interspike interval (ISI) distribution. Figure 4.4a shows the ISI time evolution during a 4 ms long measurement (corresponds to several hundred spikes) of one of the nano-oscillators during the transition between 2:1 and 1:1 integer synchronization modes. The ISI shows two distinct levels: a larger one of  $\sim 18 \mu\text{s}$  (cyan symbols) that belongs to 2:1 mode, and a smaller one of  $\sim 9 \mu\text{s}$  (blue symbols) that corresponds to 1:1 mode. The ISI spontaneously jumps between the two levels, which is highlighted by light red vertical lines in Figure 4.4a, providing a visualization of the stochastic synchronization. To obtain the boundaries of the stochastic regime, we sweep the applied voltage of one nano-oscillator while keeping the other one at fixed 10 V. By defining the 2:1 mode fraction as

$$\text{2:1 mode fraction} = \frac{\text{Number of ISI of 2:1 mode}}{\text{Total number of ISI}}, \quad (1)$$

we obtain that the stochastic regime emerges between 3.3 V and 4.2 V as the 2:1 mode fraction changes from 0 to 1 (Figure 4.4b). By adjusting voltage within the 3.3 – 4.2 V window, it is possible to create spiking sequences that contain random length inclusions of 2:1 mode at random positions, making this stochastic synchronization potentially interesting for stochastic computing and encryption applications<sup>133,158</sup>.

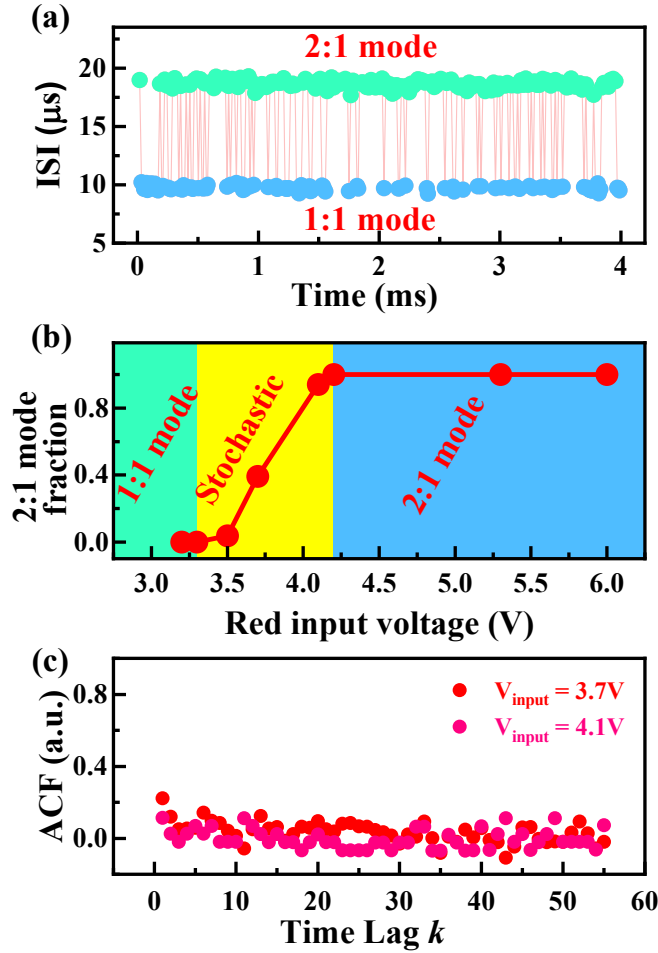


Figure 4.4 Stochastic synchronization regime.

(a) Inter-spike interval (ISI) evolution of one oscillator at 3.7 V applied voltage when the neighboring oscillator is powered with 10 V at the same time. (b) 2:1 mode fraction as a function of applied voltage. The stochastic region appears between 3.3 V to 4.2 V. (c) Autocorrelation function (ACF) of two ISI sequences recorded at 3.7 V and 4.1 V. Before applying ACF, the ISI data was converted into binary sequences (see the description in the text).

To further evaluate the stochasticity of the spiking sequence transitions, we apply an autocorrelation function (ACF) analysis to the ISI data. To develop sensitivity only to the order of 2:1 mode and 1:1 mode and not to small cycle-to-cycle deviations of the ISI, we converted the ISI data to a binary sequence by defining short ISIs (1:1 mode) as 0's and long ISI's (2:1 mode)

as 1's. This conversion can be applied straightforwardly because the ISI data has a clear two-level distribution (see Figure 4.4a). ACF is defined as

$$\text{ACF} = \frac{\sum_{i=1}^{N-k} (Y_i - \bar{Y})(Y_{i+k} - \bar{Y})}{\sum_{i=1}^N (Y_i - \bar{Y})^2}. \quad (2)$$

ACF tests for the presence of repeating patterns in the sequence  $\{Y_i\}$  by comparing it to its copy shifted by a time lag  $k$ ,  $\{Y_{i+k}\}$ .  $\bar{Y}$  in Eq. 2 is the mean of the sequence  $\{Y_i\}$ . ACF is commonly used to test the stochasticity of generated bit sequences<sup>159,160</sup>. As shown in Figure 4.4c, the ACF of the sequences generated by our nano-oscillators at different applied voltages is nearly zero at all time lags, revealing that there is no apparent order in the occurrence of 2:1 mode and 1:1 mode, i.e., the spiking sequence transitions are stochastic.

#### 4.6 Conclusion

In summary, we enabled thermally driven synchronization between nanoscale spiking oscillators by placing them in close physical proximity. By controlling the applied voltage, we achieved robust 1:1 and 2:1 synchronization. We found that the transition between the two modes occurs through an extended stochastic synchronization regime where random length spike sequences corresponding to the two modes are intermixed. This stochastic synchronization emerges in nano-oscillators instead of non-integer mode that separate different synchronization modes in micron-sized devices<sup>156</sup>. In dense integrated circuits containing large number of spiking nano-oscillators, for example in neural networks hardware, thermal interactions might become an important factor which determines the circuit operation. Basic understanding of the unique features of spiking nanodevice synchronization, such as the occurrence of the stochastic regime presented in this work, is important for designing circuits capable of harnessing the full potential of novel computational paradigms.

## 4.7 Acknowledgments

Chapter 4, in full, is a reprint of the material as it appears in the publication: Erbin Qiu\*, Pavel Salev, Felipe Torres, Henry Navarro, Robert Dynes, and Ivan K. Schuller, Stochastic transition in synchronized spiking nano-oscillators, Proc. Natl. Acad. Sci. 120, e2303765120 (2023). The dissertation author was the primary investigator and author of this paper.

### **Author contributions:**

E.Q., R.C.D. and I.K.S. conceived and designed the project. E.Q. fabricated the samples and performed all the measurements. All authors participated in the discussion and interpretation of the results. E.Q., P.S. and I.K.S. wrote the manuscript with input and corrections from all authors. I.K.S. and R.C.D. supervised the project.

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## Chapter 5 Reconfigurable cascaded thermal neuristors for neuromorphic computing

### 5.1 Introduction

Neuromorphic computing, which takes inspiration from the brain's information processing capabilities, offers an energy-efficient alternative to traditional von Neumann architectures<sup>13,74–78</sup>. At the heart of neuromorphic computing are spiking neural networks (SNNs)<sup>74,79</sup>, which simulate the event-driven nature and sparse communication patterns of biological neurons by using precisely timed spikes across layers of artificial neurons and synapses. Input data is represented and transmitted through time-varying spikes that are processed by interconnected neurons. Much of the current research has been centered on software simulations<sup>11,80</sup> or implementations using complementary metal-oxide-semiconductors (CMOS)<sup>81–84</sup>. Notable CMOS-based SNNs include IBM's TrueNorth chip<sup>82</sup> and Intel's Loihi<sup>84</sup> which are built using cutting-edge, costly technologies and complex circuit designs. A CMOS neuron typically encompasses components like temporal integration, spike/event generation, refractory period, spike frequency adaptation, and spiking threshold adaptation blocks<sup>83</sup>. However, the significant circuit footprint, limitations in scaling, and energy consumption may impede the progress of CMOS-based SNNs.

Beyond CMOS-based models, there has been a recent emergence of spiking neuron devices<sup>85,86</sup> constructed using quantum materials, which are now at the forefront of neuromorphic computing, including but not limited to Mott neurons<sup>87–90</sup>, magnetic neurons<sup>14,15,27</sup> and phase change neurons<sup>91–93</sup>. These devices have the potential to significantly reduce both the circuit complexity and the physical size of artificial neurons. However, the development of these quantum material-based artificial spiking neuron devices is still in its infancy, and various challenges and issues have been observed in initial demonstrations.

One of the primary challenges facing artificial spiking neuron devices, which is often overlooked, is the difficulty in directly transmitting information between layers without intricate circuit configurations. The issue stems from the fact that the presence of a subsequent neural layer alters the output of the preceding layer due to the loading effect. Solutions typically involve the integration of complex buffer circuits<sup>94,95</sup>, which substantially increase the overall size, often overshadowing the spiking neurons themselves in terms of space. Some studies sidestep this issue altogether<sup>16,96,97</sup>, focusing solely on network-level simulations based on the properties of individual neuron devices, without considering the challenges of transmitting information between layers at hardware level. As a result, the efficient integration of cascading neural layers remains elusive.

Furthermore, current spiking neuron configurations lack versatility. For instance, inhibitory neurons play a critical role in neural activities, but replicating this functionality in artificial spiking neurons is no easy feat. Some attempted solutions involve elaborate circuits<sup>98-100</sup>, synaptic weight alternations<sup>94</sup>, or optical inhibition<sup>95</sup>. However, none of these can directly implement an inhibitory neuron in a single simple device, which poses significant constraints on the application of learning algorithms.

In our study, we introduce a dynamic system comprised of two thermally coupled spiking oscillators based on Mott insulators, which effectively addresses the aforementioned challenges. These spiking oscillators, referred to as neuristors, exhibit a range of neural functions. Notably, we demonstrate the implementation of an inhibitory neuristor using simple Mott oxides, such as VO<sub>2</sub>, by trapping the metallic state, eliminating the need for complex circuits. Additionally, both excitatory and inhibitory neuristors can be realized using the same device by employing different inputs, thereby enhancing the device's versatility and applicability. The neuristor also displays a

rich array of reconfigurable electrical behaviors such as rate coding and stochastic leaky integrate-and-fire. Crucially, we demonstrate the feasibility of cascading neural layers through thermal interactions, which effectively eliminate the necessity for complex input/output circuits between layers. Our straightforward and innovative approach paves the way for advancements in reconfigurable cascading neural layers, which hold promise for applications in artificial intelligence.

## 5.2 Single spiking oscillator as a thermal neuristor

We have successfully implemented neuristors with reconfigurable functionalities using thermally coupled spiking oscillators, which are based on the insulator-to-metal transition (IMT) of the Mott insulator  $\text{VO}_2$ . We patterned a 100 nm thick  $\text{VO}_2$  thin film into an array of nanodevices, each measuring 100 x 500 nm<sup>2</sup>. As illustrated in Figure 5.1a, each nanodevice is separated from its neighbors by a 500 nm gap. To examine the thermal interactions between neuristors, we etched away the  $\text{VO}_2$  material between the nanodevices to electrically isolate each spiking oscillator. Despite electrical isolation, the oscillators remain thermally coupled through the  $\text{Al}_2\text{O}_3$  substrate, which serves as an effective thermal conductor due to its high thermal conductivity.

The working principle of the spiking oscillator circuit is described as follows. As depicted in Figure 5.1b, the  $\text{VO}_2$  nanodevice, initially in its insulating state, is connected in series with a variable load resistor,  $R_{load}$ , and in parallel with an intrinsic parasitic capacitance,  $C$ . When an input voltage is applied to the circuit, the ensuing current heats up the  $\text{VO}_2$  nanodevice, concurrently charging up the parasitic capacitance. Upon reaching the critical threshold voltage, the  $\text{VO}_2$  undergoes an IMT. This abrupt decrease in the  $\text{VO}_2$  resistance prompts the parasitic capacitance to discharge, resulting in a current spike. As the capacitance discharges, most input

voltage is dropped across  $R_{load}$ , and the voltage across  $VO_2$  does not generate sufficient heat to sustain the metallic state, causing the  $VO_2$  to revert to its insulating state (16, 17, 34). This process repeats, generating a series of stable, spiking, auto-oscillations as depicted in Figure 5.6. By tuning the input voltage and load resistance, a wide variety of reconfigurable neural dynamics can be demonstrated within the same neuristor.

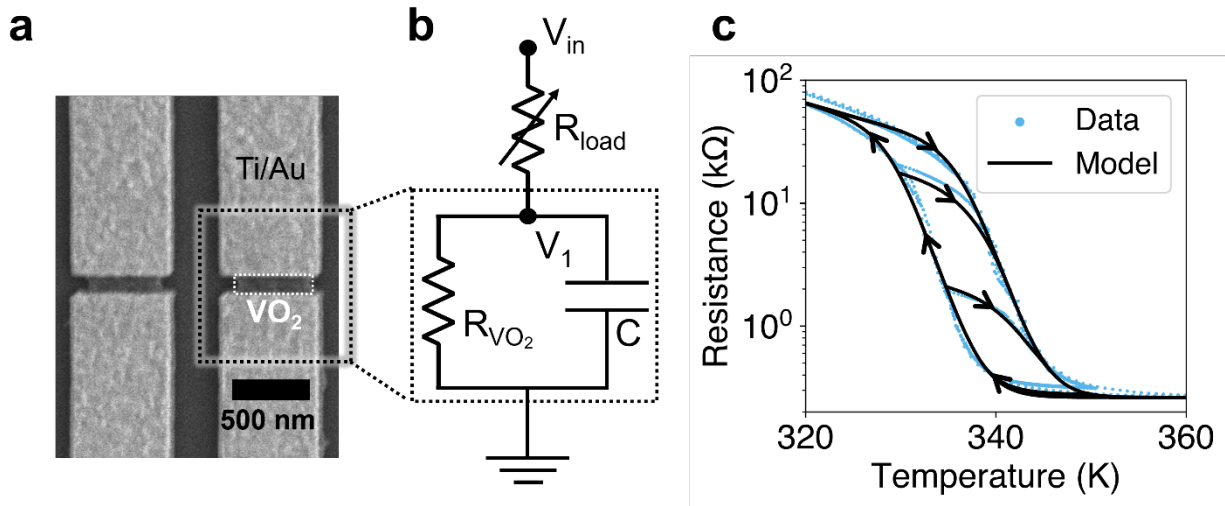


Figure 5.1 Spiking oscillator as thermally coupled neuristors.

(A) An SEM image of two adjacent  $VO_2$  nanodevices. Each nanodevice has dimensions of  $100 \times 500 \text{ nm}^2$ . To study the thermal interactions between two spiking oscillators, the nanodevices are placed in close proximity, separated by a 500 nm gap, electrically isolated by etching away the  $VO_2$  between them. (B) The schematic of the equivalent circuit setup for a single spiking oscillator. To generate electrical spikes, a variable load resistor,  $R_{load}$ , is connected in series with the  $VO_2$  nanodevice. An intrinsic parasitic capacitance, approximately 0.15 nF, is connected in parallel with the  $VO_2$  nanodevice. The circuit represents a single spiking oscillator configured as a neuristor, which is reconfigured for various neuronal functionalities in subsequent measurements. (C) The hysteresis loops of resistance versus temperature for both experimental data and theoretical modeling. The major loop ranges from 320 K to 360 K and two minor loops start from 330 K and 335 K, respectively. The cooling branches of the loops overlap, while the heating branches vary for different loops. The major and minor loops are essential for realizing excitatory and inhibitory neuronal functionalities. The theoretical model closely aligns with the experimental results.

### 5.3 Single neuristor characteristics

First, we demonstrate that our Mott insulator  $VO_2$ -based neuristor exhibits spiking behavior analogous to a biological neuron. Specifically, we demonstrate the all-or-nothing law



<sup>161</sup>, which states that with external stimuli, a neuristor either gives maximal response or no response at all; and the rate coding law <sup>88,162</sup>, showing that the spiking frequency increases with increasing input stimulus.

In Figure 5.2., we conducted measurements on a single neuristor configured in series with a 12 k $\Omega$  load resistor at a base temperature of 325 K under varying input voltages. With a 9 V bias, the neuristor displays no response due to the subthreshold input, as illustrated in Figure 5.2a. With a suprathreshold voltage of 12.5 V, the neuristor exhibits a full current spiking response as depicted in Figure 5.2b. Almost all current spikes exhibit nearly identical amplitudes, except the first, which has a larger amplitude due to the initial insulating state requiring a higher firing threshold, causing a larger current surge. This behavior, also observed at different suprathreshold voltages (Figure 5.7), exemplifies the “all-or-nothing” law <sup>161</sup>.

Although the amplitude of the current spikes remains constant as the input voltage varies, there is an observed increase in spiking frequency with increasing input voltage, as shown in Figure 5.7. We plotted the spiking frequencies against each input voltage (Figure 5.2d), revealing a discontinuous frequency-voltage relationship with a threshold at 10.5 V. Beyond this, the firing rate increases with stimulus intensity, mirroring typical type-II neuronal rate coding <sup>95,163,164</sup>. However, our neuristor exhibits a critical feature differing from traditional neuron models, which is the key to implementing the inhibitory functionality. As demonstrated in Figure 5.2c, when biased with 15.8 V, the neuristor becomes quiescent after a few initial spikes. This phenomenon arises because VO<sub>2</sub> gets trapped in its metallic state, with a constant current flowing through the metallic filament, instead of reverting to its insulating state <sup>46,165</sup>. The inhibitory behavior is also reproduced with a bias voltage of 17 V, as depicted in Figure 5.7K. To rule out the possibility of nanodevice degradation causing this behavior, we tested at 15.7 V again and confirmed stable

spiking behavior, as shown in Figure 5.7L. We incorporated this distinctive inhibitory feature into the rate coding graph in Figure 5.2D, presenting a comprehensive representation of neuristor behavior.

To understand the mechanism of the spiking oscillators, we constructed a theoretical model, which comprises of the circuit from Figure 5.1B, the hysteresis model in Figure 5.1C, and a simple heat conduction model. As depicted in Figure 5.2A-D, the simulations align well with the experimental results. A detailed explanation of this model is presented in the supplemental materials (SM).

Using the theoretical model, we show further insights into the three distinct operational modes of our neuristor, depicted in the resistance-time and resistance-temperature plots in Figure 5.2E. At a subthreshold voltage of 9 V, the generated heat is insufficient to trigger the IMT, thereby confining VO<sub>2</sub> to its insulating state. Conversely, at 15.8 V, the system produces excessive heat, preventing VO<sub>2</sub> from fully reverting to its insulating state before the arrival of the next current spike, eventually trapping VO<sub>2</sub> in its metallic state. However, with a moderate voltage of 12.5V, VO<sub>2</sub> is adequately heated to transition into its metallic state and subsequently allowed sufficient time to fully revert to its insulating state. This allows VO<sub>2</sub> to traverse the full hysteresis loop and return to its initial state, facilitating stable oscillations.

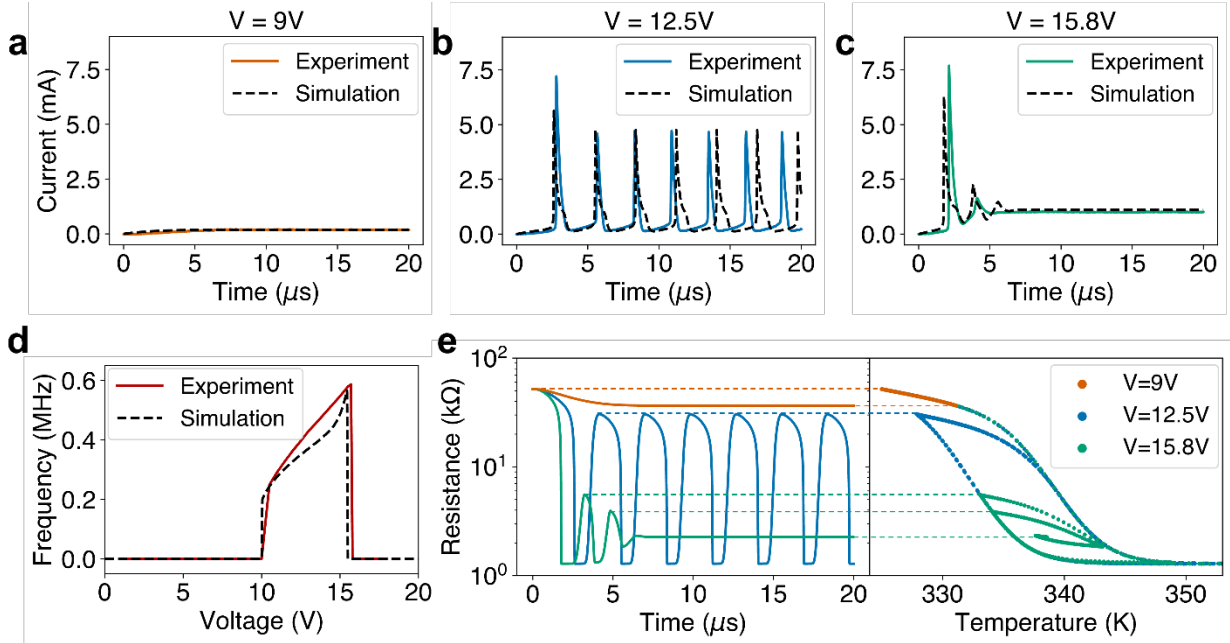


Figure 5.2 Single neuristor characteristics.

All measurements in this figure were conducted at a base temperature of 325 K, with a load resistance of 12 k $\Omega$ . (A) With an applied voltage of 9 V, the neuristor shows no current response in either the experiment (solid line) or simulation (dashed line). (B) When subjected to 12.5 V, the neuristor exhibits a full current response in both the experiment (solid line) and simulation (dashed line). This phenomenon is termed the “all-or-nothing” law. (C) When subjected to 15.8 V, both the experimental (solid line) and simulated (dashed line) neuristor become inhibited after the initial two spikes, failing to return to the insulating state and maintaining a thin metallic filament through which a small (1mA) current flow. (D) The graph shows the spiking frequency as a function of input voltages, for both experimental (solid line) and simulation (dashed line) data. This typical type-II neuronal functionality shows a discontinuous frequency jump upon reaching the 10.5 V threshold voltage. In between the threshold and cutoff voltages, the spiking frequency changes monotonically, a phenomenon known as “rate coding”. (E) Simulated resistance versus time (left panel), and resistance as a function of temperature (right panel) at different input voltages. This illustrates the mechanism behind the three different working modes of our neuristor.

#### 5.4 Reconfigurable neural functionalities

The diverse reconfigurable neural functionalities are manifested via the thermal interaction of coupled neuristors. As shown in the schematic inset of Figure 5.3A, the two neuristors, spaced 500 nm apart, are electrically isolated but thermally coupled through the Al<sub>2</sub>O<sub>3</sub>

substrate. The phenomenon of thermal interactions between spiking oscillators has been previously documented<sup>166,167</sup>. Leveraging the characteristics of a single neuristor, the pair of thermally coupled neuristors exhibits a diverse range of reconfigurable neural functionalities, which can be tuned by adjusting their input voltages and load resistances.

In Figure 5.3A, neuristor A is subjected to a short 200 ns pulse at 1.3 V without any load resistor, generating a 4 mA current pulse. This, in turn, creates a heat spike that propagates to neuristor B, which locally increases neuristor B's temperature, lowers its threshold voltage and causes the IMT at a subthreshold voltage of 1.5 V. Since neuristor B is not connected to any load resistor, it stays in the metallic state and yields a direct current (DC) output.

The spike-in and DC-out effect, as shown in Figure 5.3A, can be reconfigured to a spike-in and spike-out behavior, as shown in Figure 5.3B, by incorporating a 9 k $\Omega$  load resistor to neuristor B. On its own, with a 2.7 V bias and no thermal interaction, neuristor B is unable to trigger spikes, as illustrated in Figure 5.8. However, when neuristor A is subjected to a brief 200 ns pulse at 3.3 V, the heat spike it generates enables neuristor B to produce stable spikes. Remarkably, this process is highly energy efficient. As an example, a single spike consuming 6.45 nJ from neuristor A can initiate 14 spikes in neuristor B with a total energy output of 5.56 nJ, as detailed in Figure 5.9.

The electrical dynamics of coupled neuristors can also be reconfigured to exhibit another distinctive feature, known as stochastic leaky integrate-and-fire. In this configuration, neuristor A is consistently subjected to a suprathreshold voltage of 7V in series with a 22 k $\Omega$  load resistor, resulting in stable spikes, while neuristor B, in series with a 30 k $\Omega$  load resistor, is subjected to a subthreshold voltage of 5 V, which alone is not sufficient for it to fire. However, neuristor B can integrate multiple current spikes from neuristor A and fire a spike, as shown in Figure 5.3C. The

initial current spike from neuristor A is insufficient to elevate the temperature enough to activate neuristor B. Yet, the accumulated heat from multiple current spikes eventually causes neuristor B to undergo the IMT, resulting in a spike<sup>88</sup>. Importantly, the number of spikes neuristor B integrates from neuristor A before firing is inherently stochastic due to jittering behaviors in the neuristor<sup>72</sup> and stochasticity in thermal propagation<sup>168</sup>. In this case, neuristor B may integrate 3, 4, 5, or 8 spikes from neuristor A to produce a single spike.

Figure 3D depicts how the stochastic firing probability of the number of integrated spikes from neuristor A changes with different subthreshold voltages applied to neuristor B. When neuristor B is subjected to stronger subthreshold stimuli, it exhibits a more deterministic firing probability and requires fewer integrated spikes from neuristor A. Conversely, weaker subthreshold stimuli result in a more pronounced stochastic leaky integrate-and-fire behavior<sup>88</sup>. For a more comprehensive and detailed view of the stochastic and deterministic spiking patterns, Figure 5.10. presents the behavior of two thermally coupled neuristors, highlighting the distinctive stochastic leaky integrate-and-fire characteristic. Distance between neuristors also affects their coupling pattern, and a demonstration is shown in Figure 5.11.

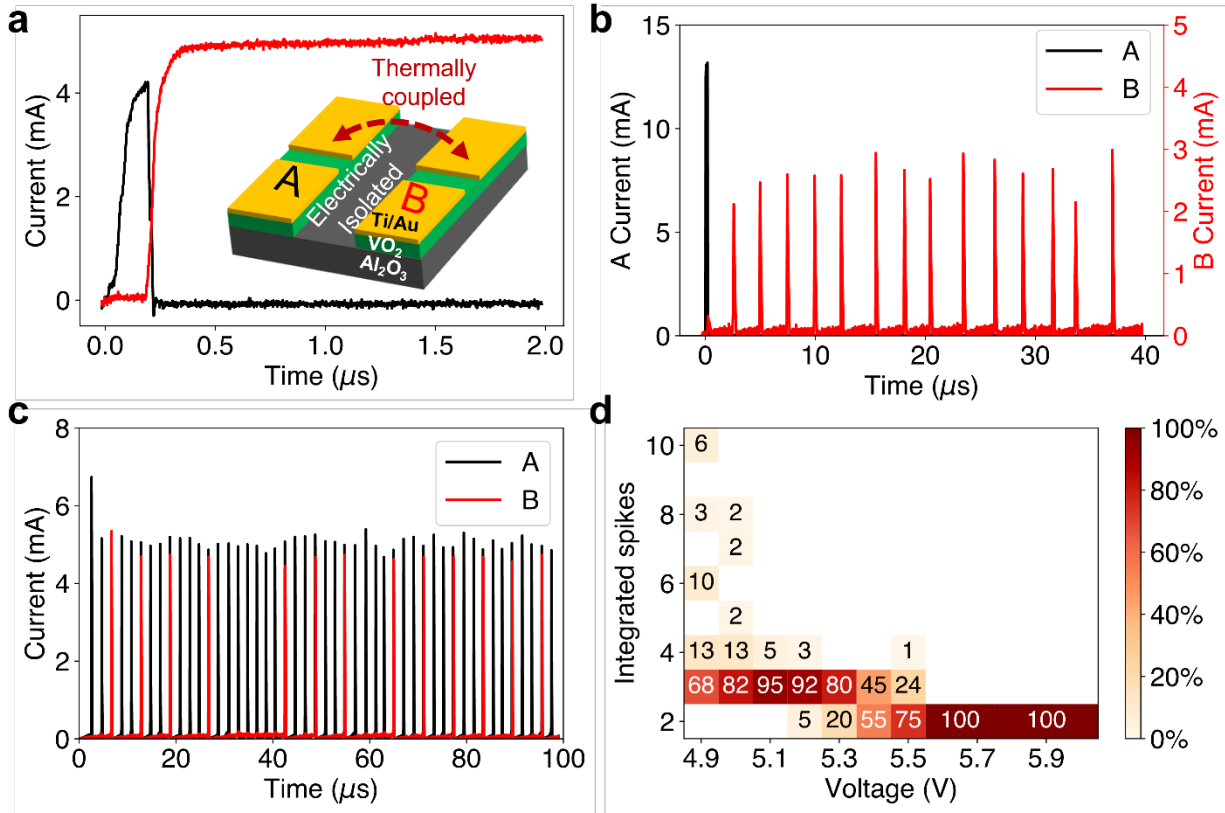


Figure 5.3 Reconfigurable electrical dynamics in coupled neuristors.

(A) Spike-in and DC-out. The load resistance for both neuristors is set to zero in this configuration. Neuristor A (black), triggered by a 1.3 V pulse lasting 200 ns, generates a 4 mA current spike. This functions as a heat spike-in for neuristor B (red), which is biased at a subthreshold voltage of 1.5 V. This induces an IMT and leads to a DC output. This is termed as the spike-in and DC-out effect. (B) Spike-in and spike-out. By adding a 9 kΩ load resistor to neuristor B, the output of neuristor B can be reconfigured from DC-out to spike-out. (C) Stochastic leaky integrate-and-fire functionality. This is an example where neuristor A, with a suprathreshold input voltage of 7V, generates stable spikes, and neuristor B, subjected to a 5V subthreshold voltage, produces current spikes by integrating multiple current spikes from neuristor A. (D) Heatmap of a comprehensive stochastic leaky integrate-and-fire behavior. This demonstrates the relationship between firing probability and input voltages. The x-axis represents the input subthreshold voltage to neuristor B, and the y-axis shows the number of spikes integrated from neuristor A. The heatmap values indicate the firing probabilities (in percentages) of neuristor B integrating different numbers of spikes for various input voltages.

To the best of our knowledge, this is the first instance of cascading neural layers in hardware exclusively implemented with thermally coupled neuristors, eliminating the need for complicated CMOS circuits. The top section of Figure 5.4 shows a flowchart that illustrates the

information transfer process between the neural layers. Neuristor A integrates multiple input electrical pulses and produces a current spike, which acts as the heat spike input for neuristor B through the sapphire substrate. Subsequently, neuristor B stochastically integrates the propagated heat spike from neuristor A to create its own spike.

As depicted in the bottom left panel, neuristor A in the preceding layer is supplied with consecutive square pulses at 9.1 V, with a period of 1  $\mu$ s and a 50% duty cycle (light blue curve). The rapid charging and discharging induced by these square pulses result in a serrated voltage curve for neuristor A (black curve). When the accumulated voltage across neuristor A reaches the threshold, it undergoes an IMT, leading to a full discharge and the generation of a current spike. Simultaneously, while neuristor B in the subsequent layer is subjected to a subthreshold DC voltage of 5.7 V, the heat spike from neuristor A lowers the threshold voltage and triggers an IMT in neuristor B (red curve), also resulting in a spike (see Figure 5.12). In this way, we achieve cascaded information transfer between different neural layers at the hardware level, eliminating the necessity for complex input/output circuits between layers <sup>94</sup>.

The bottom right panel portrays a similar scenario, but with input square pulses having an 80% duty cycle. Due to the extended duty cycle, neuristor A has longer charging and shorter discharging time per pulse. This means it needs fewer input pulses to reach the threshold, and consequently fires a spike at a faster rate. However, this does not necessarily speed up spiking in neuristor B, as its charging time to reach the threshold remains invariant. As a result, some current spikes from neuristor A do not trigger a corresponding spike from neuristor B, adhering to its refractory period – another key neural function <sup>88,90</sup>. As depicted in the bottom right panel, neuristor B needs to integrate 2 or 3 spikes from neuristor A to generate its own spike. More details about the impact of the duty cycle and the pulse amplitude can be found in Figure 5.12

and Figure 5.13. By adjusting the input waveform, the cascaded neuristors exhibit rich reconfigurable dynamics, effectively modulating the flow of information.

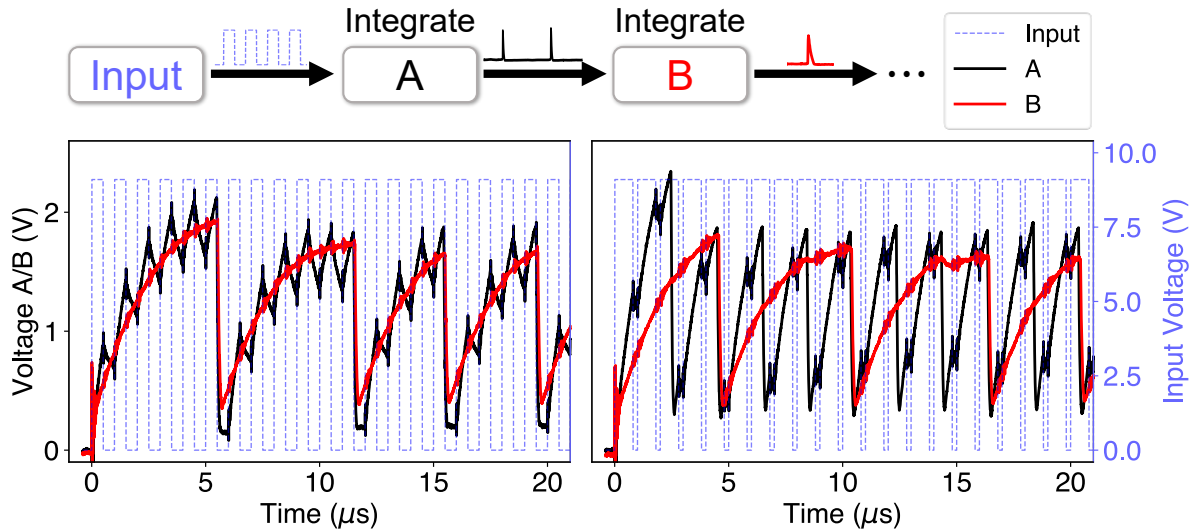


Figure 5.4 Cascaded information transfer between different neural layers.

Both neuristors A and B are connected in series with load resistors – 22 kW for neuristor A and 30 kW for neuristor B – and share the same input threshold voltage of 6 V. Neuristor A is fed with a sequence of suprathreshold pulses at 9.1 V, each with a 1 μs period, while neuristor B is powered with a constant subthreshold voltage of 5.7 V. Top: Flowchart illustrating the cascaded information transfer between different neural layers via thermal interactions through Al<sub>2</sub>O<sub>3</sub> substrate. Neuristor A in the preceding layer integrates multiple electrical pulses from the input and generates current spikes, which serve as the cascading heat spike input of the neuristor B in subsequent layer. In this fashion, neuristor B integrates multiple heat spikes from neuristor A and fires a spike. Bottom left: Voltage traces for neuristors A, B, with a 50% duty cycle square input pulses. Neuristor A exhibits leaky integration of the input electrical pulses, while neuristor B performs similar integration of heat spikes from neuristor A, eliminating the need for complex buffer circuits. Bottom right: Similar configuration but with 80% duty cycle square input pulses.

In large-scale spiking neural networks, not only is the information transfer important, but the inhibitory functionality is also significant<sup>79,80,94</sup>. In Figure 5.5, we demonstrate the versatility of our neuristors, where excitatory and inhibitory functionalities are displayed within the same neuristor by controlling their input voltages.

An excitatory neuristor becomes active upon receiving external stimuli. In our case, the neuristors interact with each other through heat interaction via the sapphire substrate. Neuristor



A functions as a heat pump, generating a continuous stream of heat spikes when biased at 2.9 V. Neuristor B, with an applied subthreshold voltage of 2.6 V, is excited by neuristor A in a 1:1 excitation mode, as shown in Figure 5.5A. The heat synchronizes the phases and frequencies of the two neuristors. When neuristor A is subjected to suprathreshold voltage of 4.3 V while neuristor B remains at a subthreshold voltage of 2.6 V, neuristor A excites neuristor B in a mixed integer excitation mode with 3:1 and 2:1 spiking pattern, demonstrating stochastic leaky-and-fire characteristics. Notably, the heat still maintains phase-locking between both neuristors. The evolution of excitatory interaction characteristics in response to changes in input voltage is shown in Figure 5.14.

We can convert neuristor B from an excitatory to an inhibitory neuristor by carefully adjusting its bias voltage just below its upper limit. Surprisingly, the inhibitory functionality emerges in the same device without any physical alterations. As shown in Figure 5.5D, neuristor B exhibits stable spiking when neuristor A is inactive. However, upon neuristor A's activation, neuristor B is effectively inhibited, ceasing to spike after a few initial spikes. The stream of heat spikes from neuristor A raises the temperature of neuristor B and this pushes B above the upper threshold of stable rate coding as described in Figure 5.2D. This consequently traps neuristor B in the metallic state with a conductive filament and disables its capability to sustain stable auto-oscillations. Another reconfigurable inhibitory characteristic is presented in Figure 5.15, showing mutual inhibition between neuristors.

By introducing a thermal coupling term for adjacent neuristors, our theoretical model accurately replicates these behaviors, as shown in Figure 5.5C and Figure 5.5F. The SM provides more details of this model, including a study on the effect of coupling strength in Fig. 5.16., and additional simulations of the excitatory and inhibitory behaviors in Figure 5.17 and Figure 5.18.

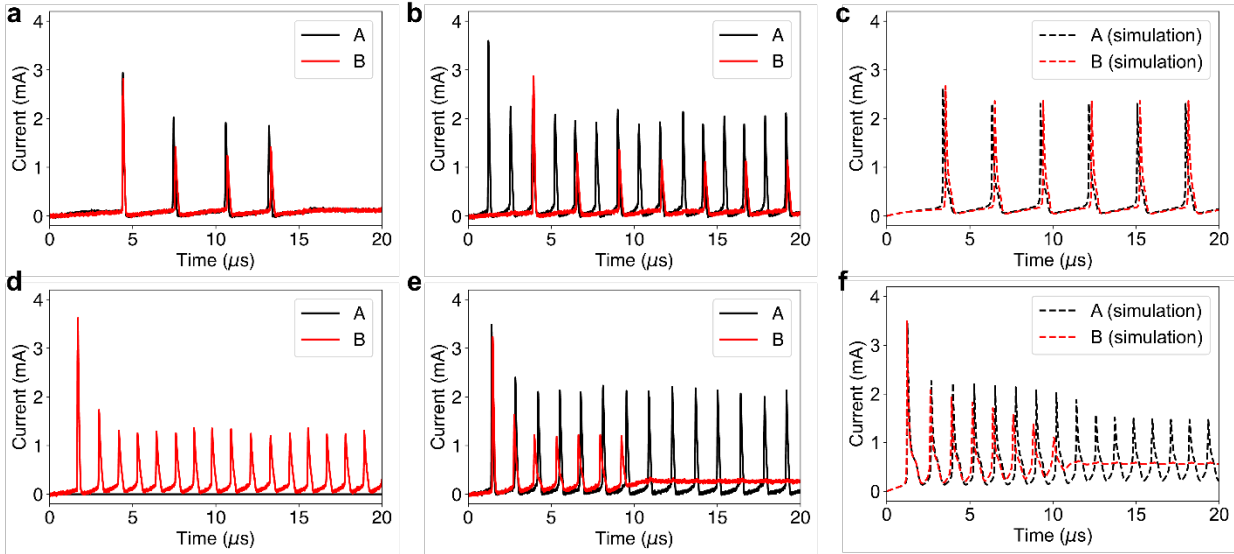


Figure 5.5 Excitatory and inhibitory interactions between neuristors.

Both neuristors are connected in series with a  $12\text{ k}\Omega$  load resistance. Neuristor A has an input threshold voltage of  $2.9\text{ V}$ , while neuristor B has an input threshold voltage of  $2.8\text{ V}$ . (A) When neuristor A is biased at  $2.9\text{ V}$  and neuristor B is biased at  $2.6\text{ V}$  subthreshold voltage, neuristor A excites neuristor B in a 1:1 excitation mode, resulting in both phase and frequency synchronization. (B) Neuristor A, at  $4.3\text{ V}$  suprathreshold voltage, excites neuristor B (at  $2.6\text{ V}$  subthreshold voltage) in a mixed-integer excitation mode with 3:1 and 2:1 spiking patterns. (C) Numerical simulation replicating the 1:1 excitation mode with subthreshold input voltages. (D) Neuristor B generates stable spikes when biased at  $4.1\text{ V}$ , with neuristor A inactive. (E) With both neuristors biased at  $4.1\text{ V}$ , neuristor B becomes quiescent after initial spikes due to inhibition by neuristor A. The stable heat spikes from neuristor A traps the neuristor B in the metallic state. (F) Numerical simulations mirroring the inhibitory behavior that neuristor A inhibits the stable spiking neuristor B, which is biased just below the upper threshold.

## 5.5 Conclusion

In this study, we engineered and analyzed thermally coupled neuristors utilizing the insulator-to-metal transition of vanadium dioxide. By exploiting  $\text{VO}_2$ 's hysteresis loop and thermal interactions, we demonstrated versatile neural dynamics without relying on complex CMOS circuits. This paves the way for scalable spiking neural networks and computation blocks like logic gates and feed-forward layers. Furthermore, our comprehensive theoretical model elucidates the neuristors' operational principles, facilitating simulation and design of large-scale

neuristor networks. This opens avenues for the advancement of efficient and compact neural networks with applications spanning artificial intelligence to brain-inspired computing.

Nonetheless, our design has its limitations. The spatial layout imposes constraints on thermal interactions, which in turn limit the fan-in/fan-out capacities of neuristors. Moreover, regulating heat flows in large-scale networks presents an important challenge. Intriguingly, a large, unregulated neuristor network could potentially be used as a reservoir in reservoir computing. Moreover, investigating long-range correlations among distantly positioned neuristors could also yield fascinating insights into the brain's dynamic behavior.

## 5.6 Acknowledgments

Chapter 5, in full, is a reprint of the material as it appears in the publication: Erbin Qiu\*, Yuan-Hang Zhang, Massimiliano Di Ventra and Ivan K. Schuller, Reconfigurable Cascaded Thermal Neuristors for Neuromorphic Computing. *Adv. Mater.* 2306818, (2023). The dissertation author was the primary investigator and the corresponding author of this paper.

### **Author contributions:**

E.Q. and I.K.S. conceived and designed the project. E.Q. fabricated the samples and performed all the measurements. Y.-H. Z. performed the modelling simulations. All authors participated in the discussion and interpretation of the results. E.Q., Y.-H. Z., M.D. and I.K.S. wrote the manuscript. I.K.S. and M.D. supervised the project.

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## Chapter 6 Conclusion and Future prospects

### 6.1 Conclusion

In this dissertation, we demonstrated stochastic spiking oscillator based on Mott insulator VO<sub>2</sub>. In order to design a complex spiking neural network capable of performing advanced computational tasks, we investigate the collective dynamics of the interactions between two spiking devices.

In Chapter 3, we observed unusual stochastic patterns in capacitively coupled spiking Mott nanodevices. When these oscillators are moderately coupled, they exhibit a predictable pattern of alternating spikes. However, increasing the coupling strength leads to unexpected disruptions in this sequence, resulting in a stochastic pattern. This behavior is linked to subtle inherent randomness in the electrical triggering of the insulator-metal transition, which becomes amplified when oscillators are capacitively coupled. The observed stochastic spiking pattern bears resemblance to those found in biological neurons, suggesting potential applications in hardware-based neural computing.

Chapter 4 explores the synchronization evolution in thermally coupled spiking nano-oscillators based on Mott materials. By varying the DC voltage applied to each oscillator, we observed a distinct spiking pattern, stochastic synchronization. At low or high applied voltages, the oscillators maintained robust integer synchronization modes (2:1 or 1:1). However, within a wide range of intermediate voltages, they entered a stochastic synchronization regime, where the spiking pattern unpredictably switched between the two integer synchronization modes. This unique behavior underscores the dynamic synchronization properties of spiking oscillators and their potential for use in neuromorphic and stochastic computing circuits.

Chapter 5 continues to examine thermally coupled spiking oscillators, also called neuristors, which exhibit neural functionalities. These thermal neuristors function and communicate exclusively through thermal processes, utilizing the insulator-to-metal transition in vanadium dioxide. We showcase a diverse range of reconfigurable electrical behaviors that closely resemble those of biological neurons, including phenomena like the all-or-nothing law, type-II neuronal rate coding law, spike-in and DC out effect, spike-in and spike-out effect, and stochastic leaky integrate-and-firing law. Remarkably, inhibitory capabilities are achieved using just a single oxide device, and the transmission of cascaded information occurs solely through thermal interactions without any intricate circuits. This research serves as the groundwork for scalable and energy-efficient thermal neural networks, advancing the field of brain-inspired computing.

Overall, these studies highlight the unique properties and behaviors of coupled spiking oscillators. Their ability to emulate neural functions, along with their adaptability and reconfigurability, offers promising prospects for energy-efficient large scale neural networks and hardware-based artificial intelligence systems. By understanding the intricate collective dynamics and synchronization patterns of the two coupled spiking oscillators, we are laying the groundwork for innovative hardware-level solutions in neuromorphic computing.

## 6.2 Future Prospects

There are still many intriguing follow ups to be explored in the spiking oscillator.

First and foremost, the spiking oscillator represents an artificial dynamic system that consistently stays in a state of nonequilibrium, displaying transient spiking behaviors. In chapter 3, I observed that the relaxation of the VO<sub>2</sub> metallic domain is stochastic due to the varied distribution of long-lived metallic domains. It is worthwhile to investigate the distinct relaxation

dynamics of these metallic domains. I also aim to investigate the nucleation and growth of metallic domains, as well as the formation of metallic filaments.

In my project on thermally coupled spiking oscillators, I discovered that randomness lies hidden within the synchronization of two such devices. This inherent stochasticity can be harnessed to create a true random number generator (RNG) that successfully passes the NIST test for randomness. What's even more significant is that this concept of an RNG based on synchronization might be applicable to all synchronized systems, offering valuable potential for cryptography and security applications.

It is also important to explore heat generation, heat transport, heat evolution, and heat interactions between the VO<sub>2</sub> spiking oscillators using transient thermal mapping techniques, such as time resolved Thermoreflectance Thermal Imaging and Infrared Thermography. Investigating how different distances between devices and various substrates affect heat interaction is also essential. Such thermal analysis is key to improving the thermal management of spiking oscillators and to support the electro-thermal co-design for future large-scale thermal neuristor network chips.

Last but not least, it is necessary to construct a crossbar array of thermal neuristors to perform some computational tasks. Within this network, individual thermal neuristors produce heat spikes, transfer heat, and engage with one another through heat interactions. This process results in a variety of complex collective dynamics, opening the door to computing methods that rely on collective states, such as Hopfield-like networks and reservoir computing.

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## **Appendix A - Supplementary Materials for Chapter 3**

### **Sample Preparation:**

A 100 nm-thick VO<sub>2</sub> thin film was grown on a (012)-oriented sapphire substrate by reactive rf magnetron sputtering in 86%-14% Ar-O<sub>2</sub> atmosphere. The substrate temperature during the growth was 500 °C. The sample was cooled down at a rate of 12 °C·min<sup>-1</sup> after the deposition. X-ray diffraction shows textured VO<sub>2</sub> thin film along (110) direction (Figure 3.19). The 100×400 nm<sup>2</sup> nanodevices were defined by e-beam lithography. (20 nm Ti)/(30 nm Au) electrodes were deposited by e-beam evaporation. To isolate electrically the devices, a combination of e-beam lithography and reactive ion etching in Cl<sub>2</sub>/Ar atmosphere was used.

### **Transport Measurements:**

The measurements were performed in a TTPX Lakeshore cryogenic probe station. A Keithley 6221 current source and a Keithley 2812 nanovoltmeter were used to obtain resistance vs temperature (Figure 3.20) and dc resistive switching (Figure 3.21). A Tektronix Arbitrary Function Generator 3252C was used to supply voltage and a Tektronix broadband mixed signal oscilloscope MSO54 was used to monitor the output signals. 1 MΩ impedance oscilloscope channel was used to measure the voltage across the nanodevice, while the 50 Ω impedance channel was used to monitor the current passing through the device. The spiking oscillation measurements were performed at 325 K.

### **Supporting figures.**

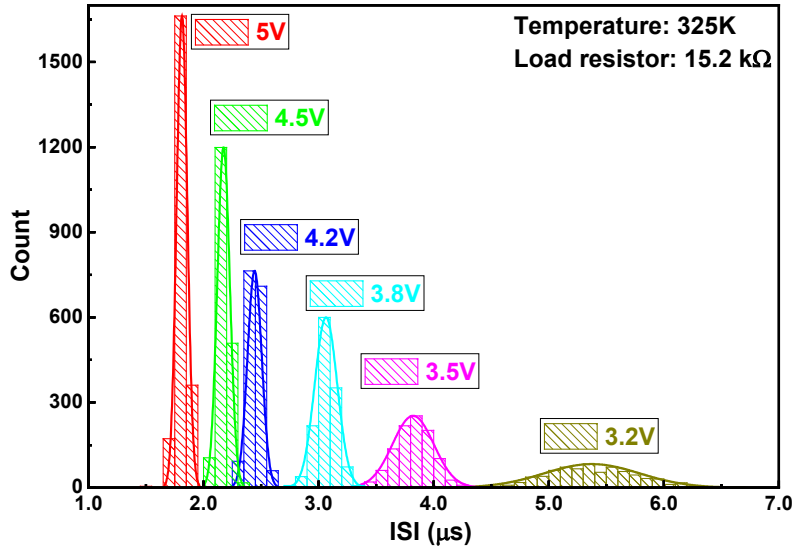


Figure 3.1 Inter-spike interval (ISI) for different input voltages. The device is measured at a fixed temperature 325 K in series with a fixed load resistor 15.2 k  $\Omega$ .

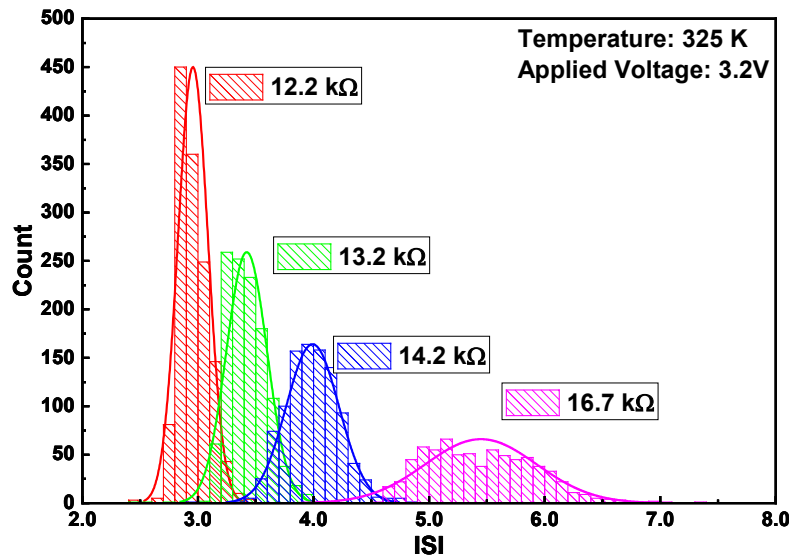


Figure 3.2 Inter-spike interval (ISI) for different load resistors. The device is measured at a fixed temperature 325 K with a fixed input voltage 3.2 V.

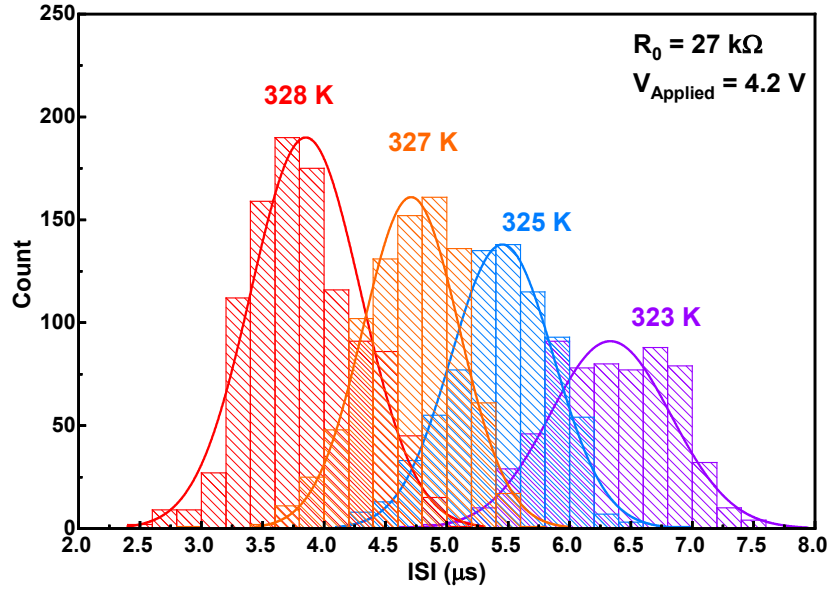


Figure 3.3 Inter-spike interval (ISI) for different temperatures. The device is applied a fixed input voltage 4.2 V in series with a fixed load resistor 27 k  $\Omega$ .

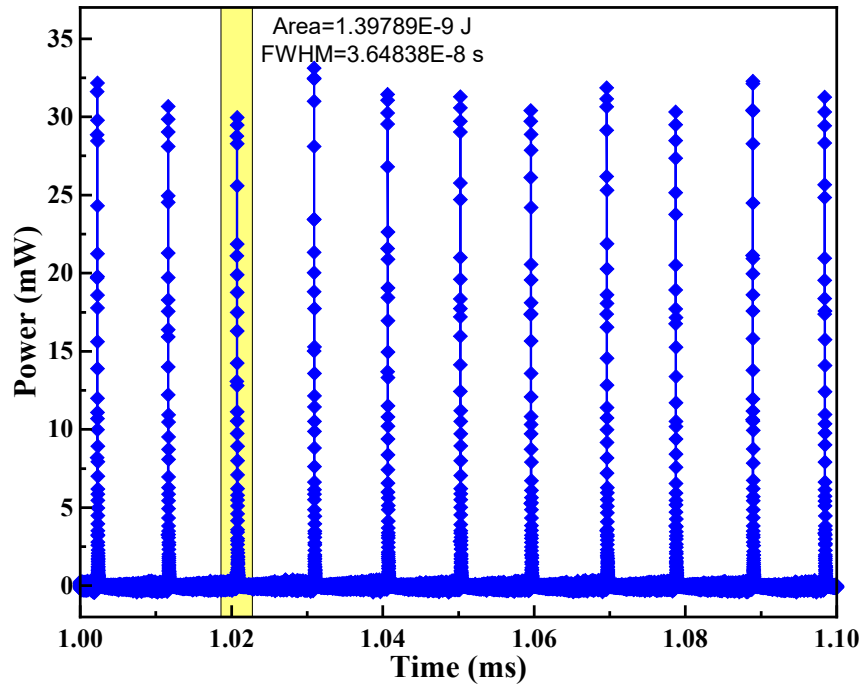


Figure 3.4 Power spikes of a random device on the chip. The power consumption per spike is around 1 nJ.

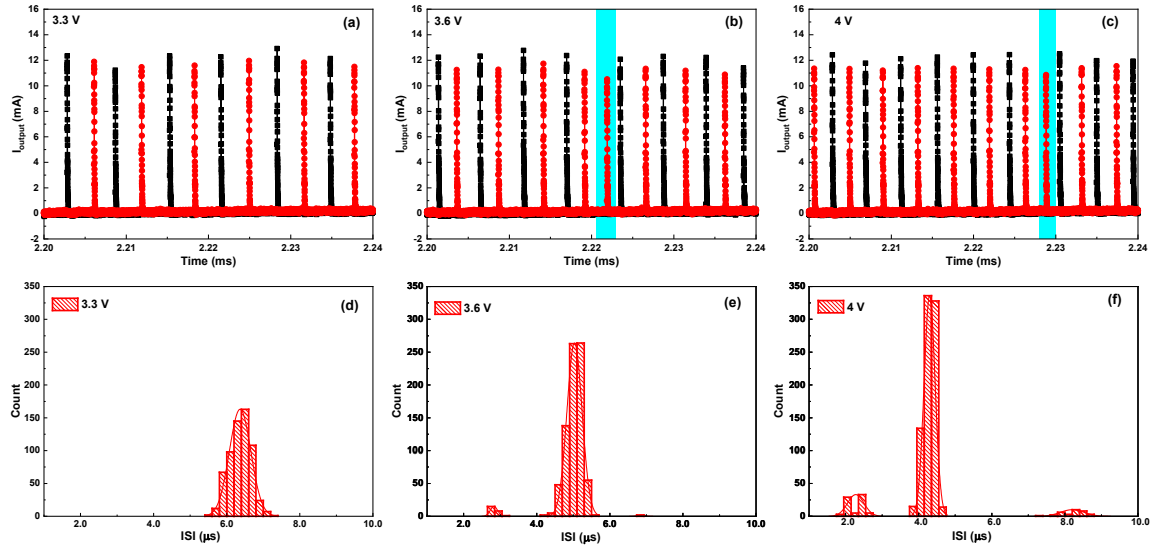


Figure 3.5 The influence of increasing input voltage on spiking pattern.

(a-c) The overlaid current time traces of two spiking oscillators show the synchronization patterns obtained for different values of the applied voltages and a fixed coupling capacitance of 0.39 nF. As the applied voltages increase, the deterministic alternating synchronization pattern is disrupted by stochastic events. (d-f) The inter-spike interval (ISI) distributions of the red oscillator. The satellite peaks appear when the applied voltage increases.

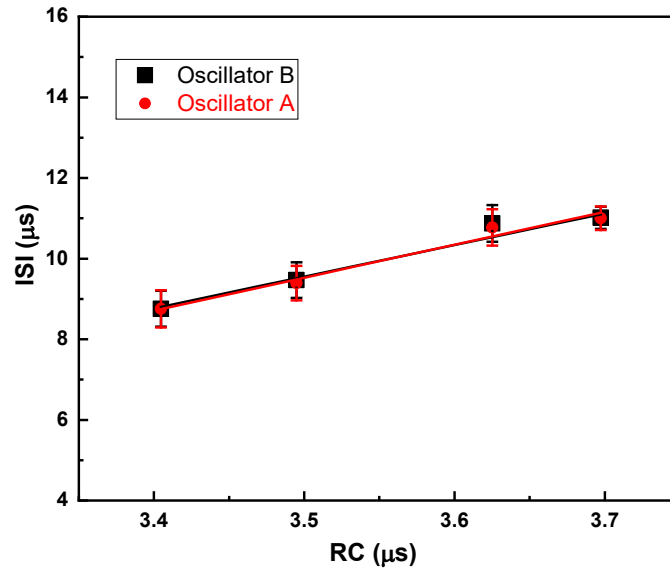


Figure 3.6 Inter-spike interval (ISI) of coupled VO<sub>2</sub> oscillators as a function of the circuit RC constant for different values of coupling capacitor (0.5 nF, 1 nF, 4.7 nF, 10 nF).

The RC constant was obtained by fitting recorded voltage-time traces. As the external coupling capacitance increases, the ISI increases linearly with the RC time constant, suggesting that the circuit electrical inertia is the primary parameter that determines the spiking frequency.

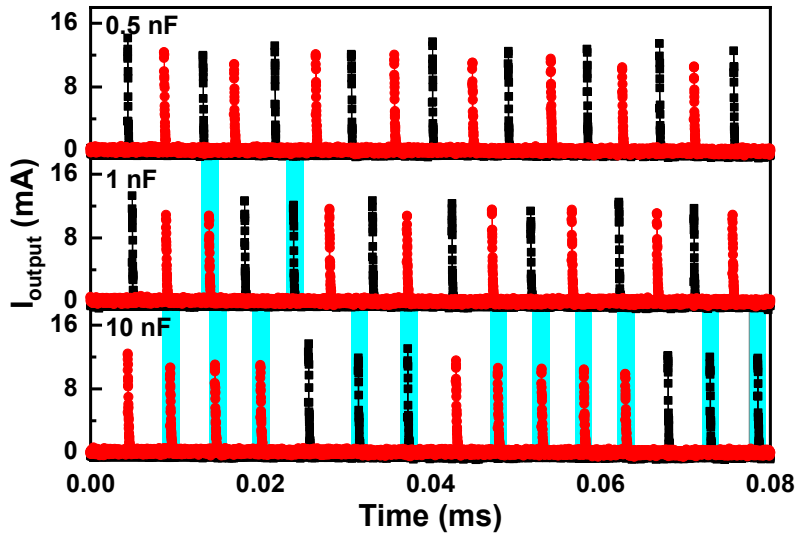


Figure 3.7 Current spiking time trace of two oscillators coupled using different capacitors.

Data is recorded in the same pair of VO<sub>2</sub> nanodevices as used in the main text. Different time window is shown compared to Figure 3.2b. Similar to the results discussed in the main text, increasing the coupling capacitance results in the emergence of stochastic disruptions of the alternating spiking sequence.

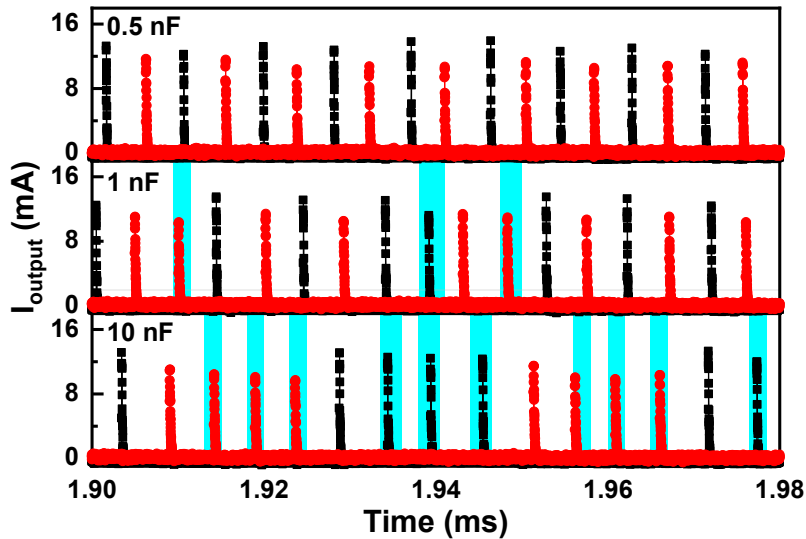


Figure 3.8 Current spiking time trace of two oscillators coupled using different capacitors.

Data is recorded in the same pair of VO<sub>2</sub> nanodevices as used in the main text. A different time window is shown compared to Figure 3.2b. Similar to the results discussed in the main text, increasing the coupling capacitance results in the emergence of stochastic disruptions of the alternating spiking sequence.

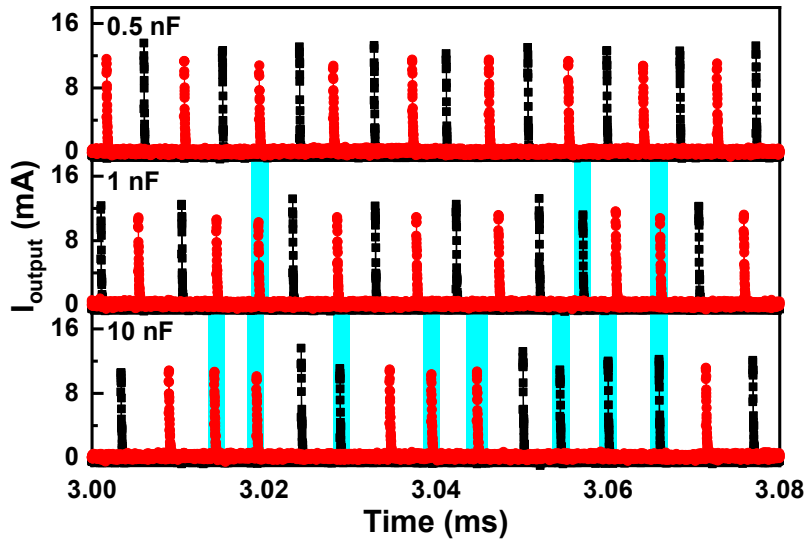


Figure 3.9 Current spiking time trace of two oscillators coupled using different capacitors.

Data is recorded in the same pair of VO<sub>2</sub> nanodevices as used in the main text. Different time window is shown compared to Figure 2b. Similar to the results discussed in the main text, increasing the coupling capacitance results in the emergence of stochastic disruptions of the alternating spiking sequence.

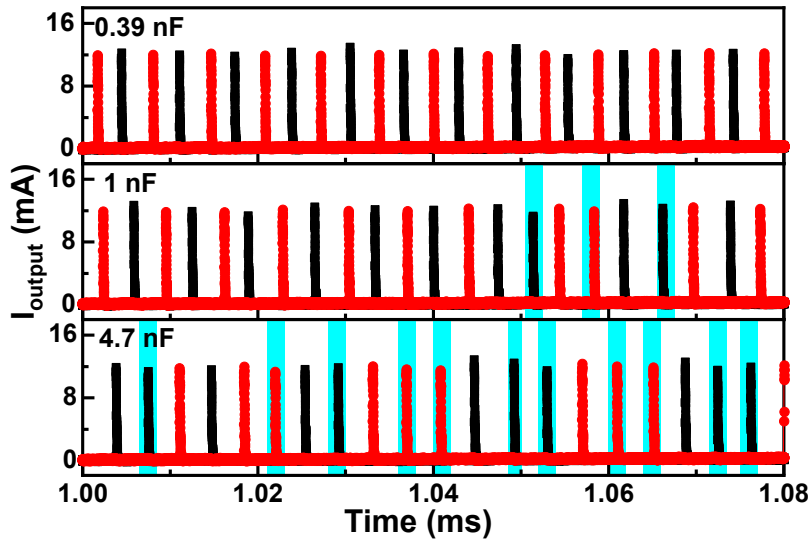


Figure 3.10 Current spiking time trace of two oscillators coupled using different capacitors.

Data is recorded in a different pair of VO<sub>2</sub> nanodevices compared to the main text. Similar to the results discussed in the main text, increasing the coupling capacitance results in the emergence of stochastic disruptions of the alternating spiking sequence.



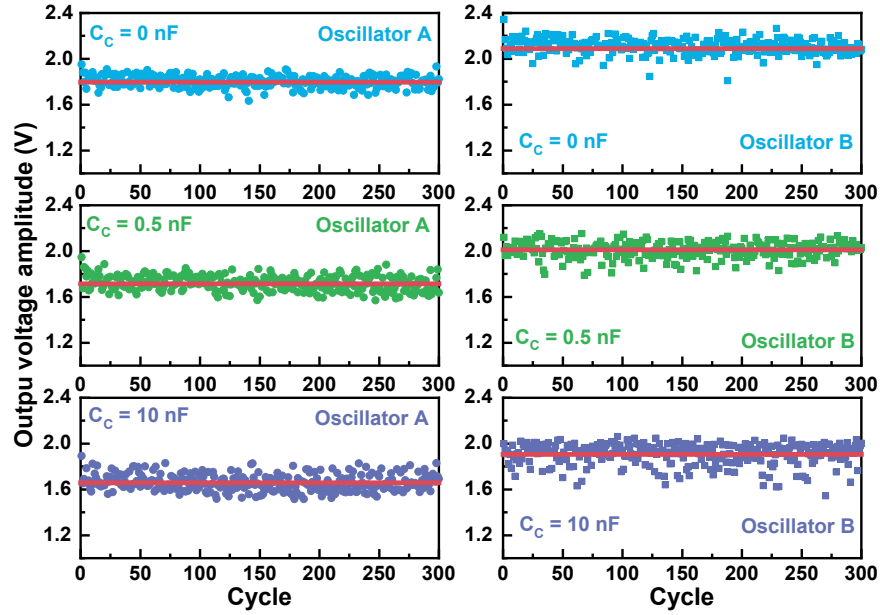


Figure 3.11 Experimental threshold voltage vs. cycle number (scatter plot). Threshold voltage, i.e. voltage that triggers spike emission, displays small stochastic undershoots/overshoots with respect to the mean value (horizontal red line).

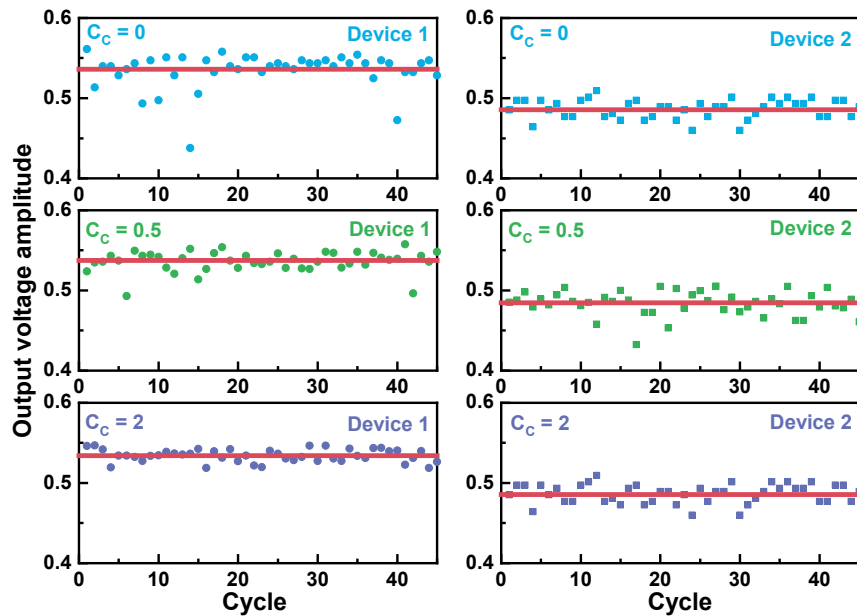


Figure 3.12 Simulated threshold voltage vs. cycle number (scatter plot). Threshold voltage, i.e. voltage that triggers spike emission, displays small stochastic undershoots/overshoots with respect to the mean value (horizontal red line), similar to experimental data in Figure 3.10.

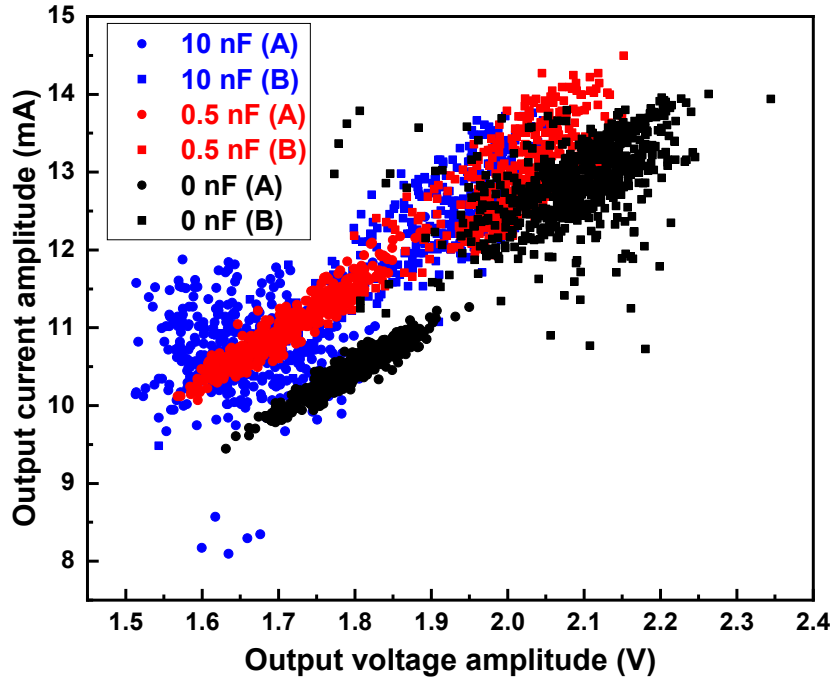


Figure 3.13 Threshold voltage vs. current spike amplitude. Stochastic cycle-to-cycle undershoot/overshoot in threshold voltage produces proportional increase of current spike amplitude for the coupled oscillator A and B.

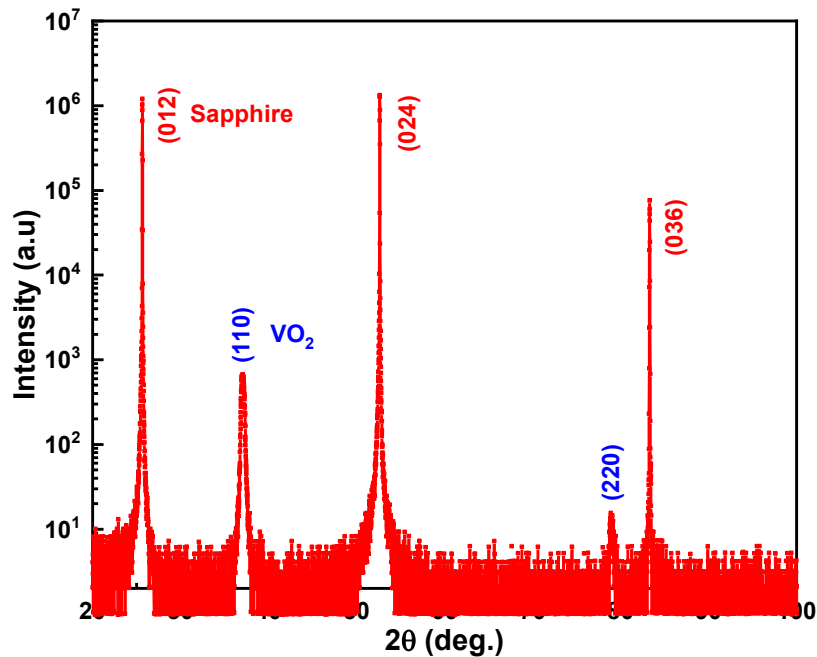


Figure 3.14 X-ray diffraction of an unpatterned VO<sub>2</sub> film showing the film growth along the (110) crystallographic direction.

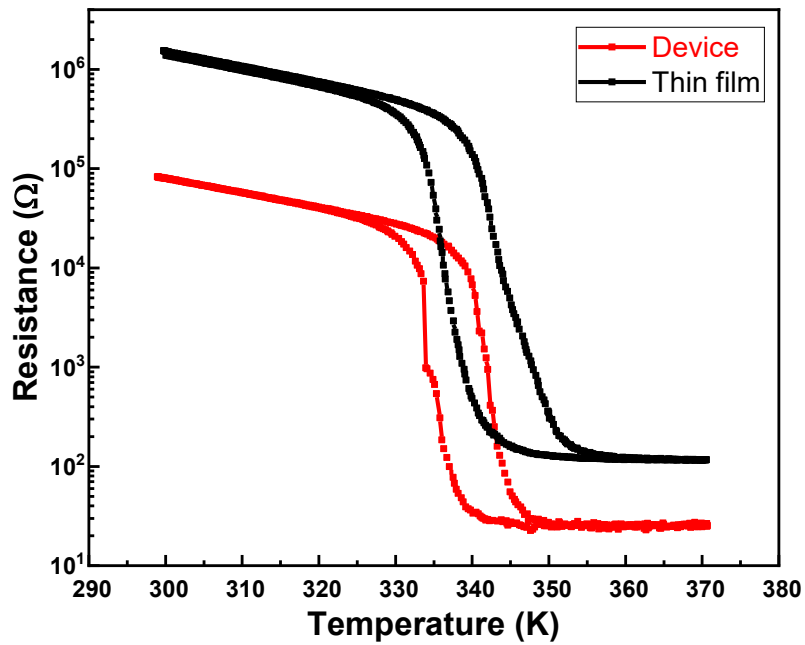


Figure 3.15 Resistance-temperature dependence of an unpatterned VO<sub>2</sub> film (black line) and fabricated 100×400 nm<sup>2</sup> nanodevice (red line). The two curves are identical proving that the device fabrication process did not alter the material properties.

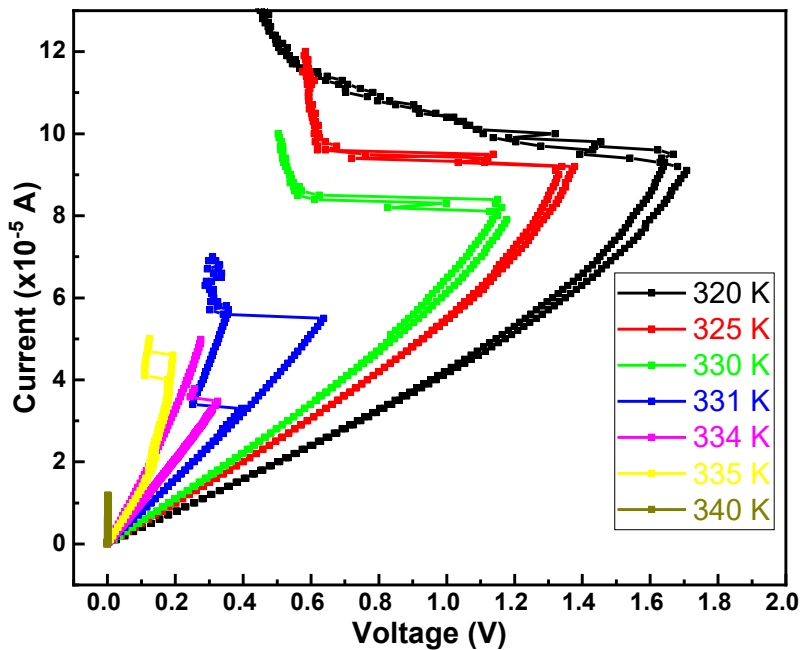


Figure 3.16 Current-controlled dc I-V curves of VO<sub>2</sub> nanodevices at different temperatures. Volatile resistive switching due to electrical triggering of the MIT can be observed, as normally expected in VO<sub>2</sub> devices.

## Appendix B - Supplementary Materials for Chapter 4

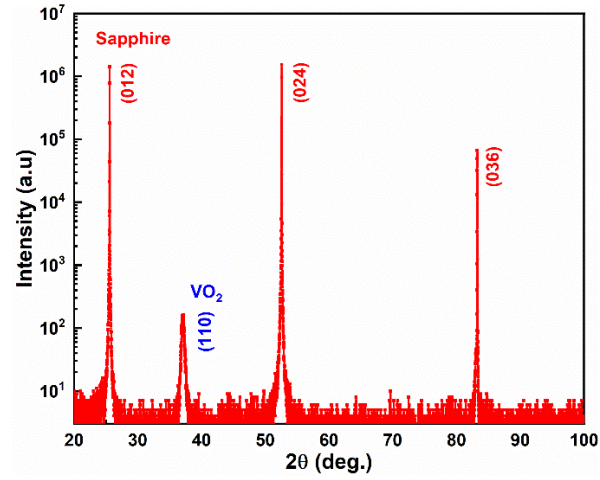


Figure 4.1. Specular x-ray diffraction of a  $\text{VO}_2$  thin film on an  $\text{Al}_2\text{O}_3$  substrate.

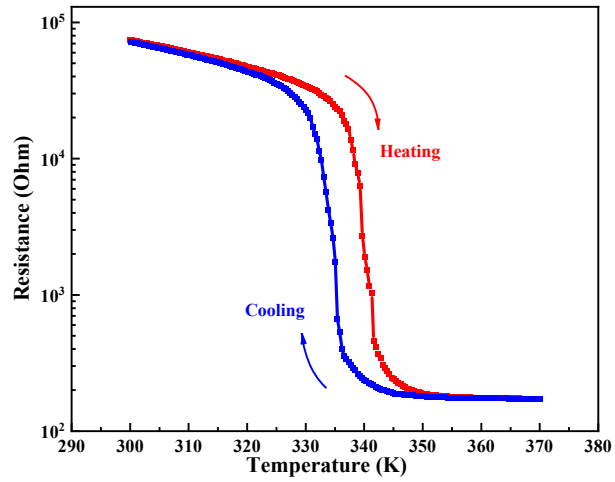


Figure 4.2 Resistance vs. temperature of 100 nm thick  $\text{VO}_2$ .

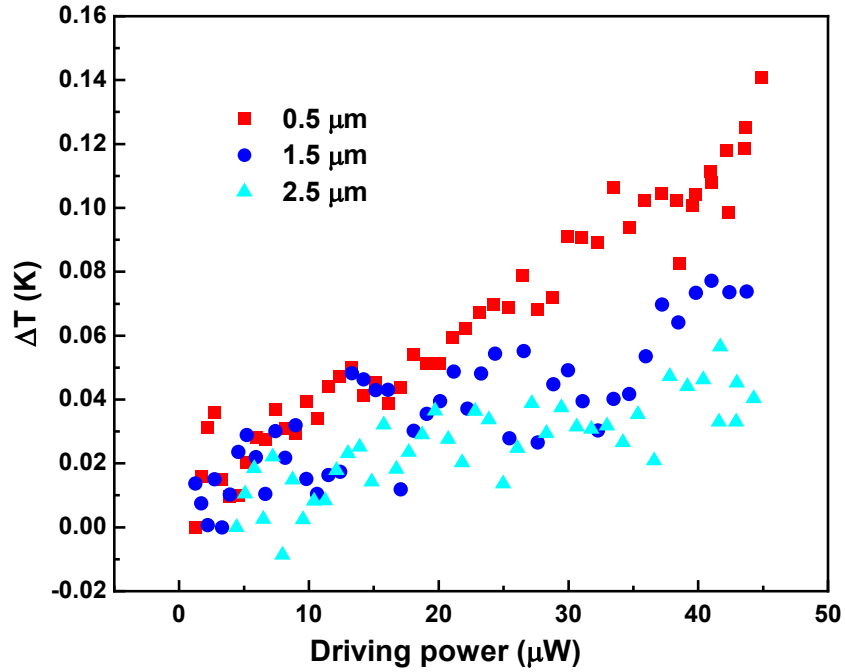


Figure 4.3 Inferred temperature change of three nanodevices when a neighboring nanodevice at 0.5, 1.5 and 2.5  $\mu\text{m}$  separation distance is powered with a significant current.

This graph was obtained by mapping the resistance change data shown in Figure 4.1b in the main text onto the equilibrium resistance-temperature dependence.

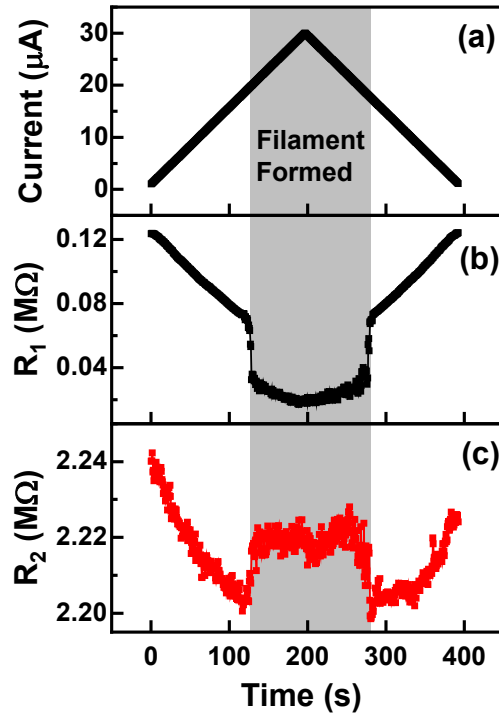


Figure 4.4 Non-linear resistive switching.

(a) A current trace of the first device (heat generator) vs. time. (b) The resistance trace of the first device (heat generator) vs. time. Resistive switching happened and the filament formed. (c) The resistance trace of the second device (probe device) vs. time. When resistive switching happens and the filament forms in the first device, less power is generated and propagated. Simultaneously, the resistance of the second device jumps up (i.e., probe device cools down).

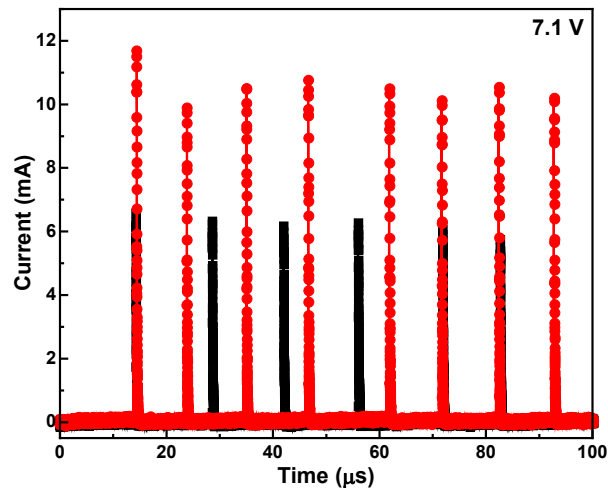


Figure 4.5 Weak thermal coupling between the first and the third nanodevices placed  $1.5 \mu\text{m}$  apart as shown in Figure 4.1a results in an unstable synchronization.  $7.1 \text{ V}$  (above threshold voltage) is applied to these two nanodevices simultaneously using the circuit shown in Figure 2a.

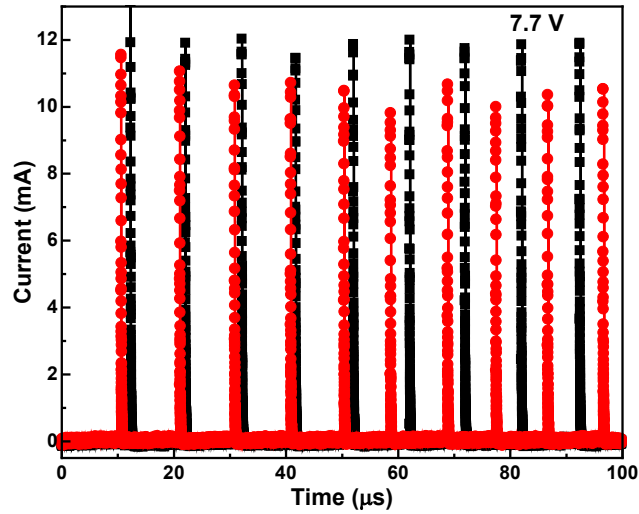


Figure 4.6 No thermal coupling between two nanodevices positioned on two opposite corners of the sample when 7.7 V (above threshold voltage) is applied to these two nanodevices simultaneously using the circuit setup in Figure 4.2a. The spike trains of the two devices show no sign of synchronization.

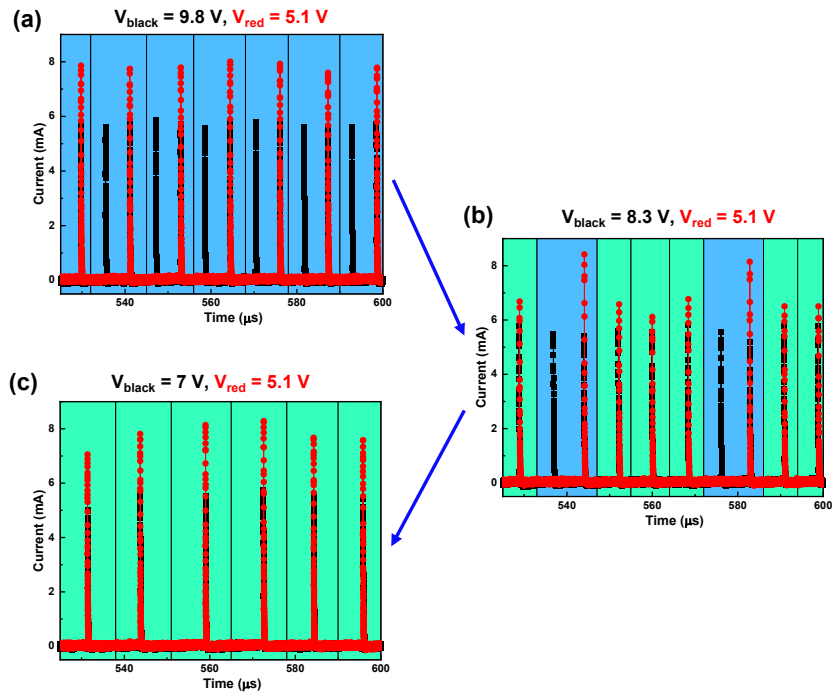


Figure 4.7 Synchronized spiking pattern evolution in a different pair of  $500 \times 500 \text{ nm}^2$  devices in the same  $\text{VO}_2$  sample.

Stochastic synchronization transition (b) between 2:1 synchronized mode (a) and 1:1 synchronized mode (c) observed in a different pair of  $500 \times 500 \text{ nm}^2$  devices in the same  $\text{VO}_2$  sample that was used to acquire data presented in the main text.

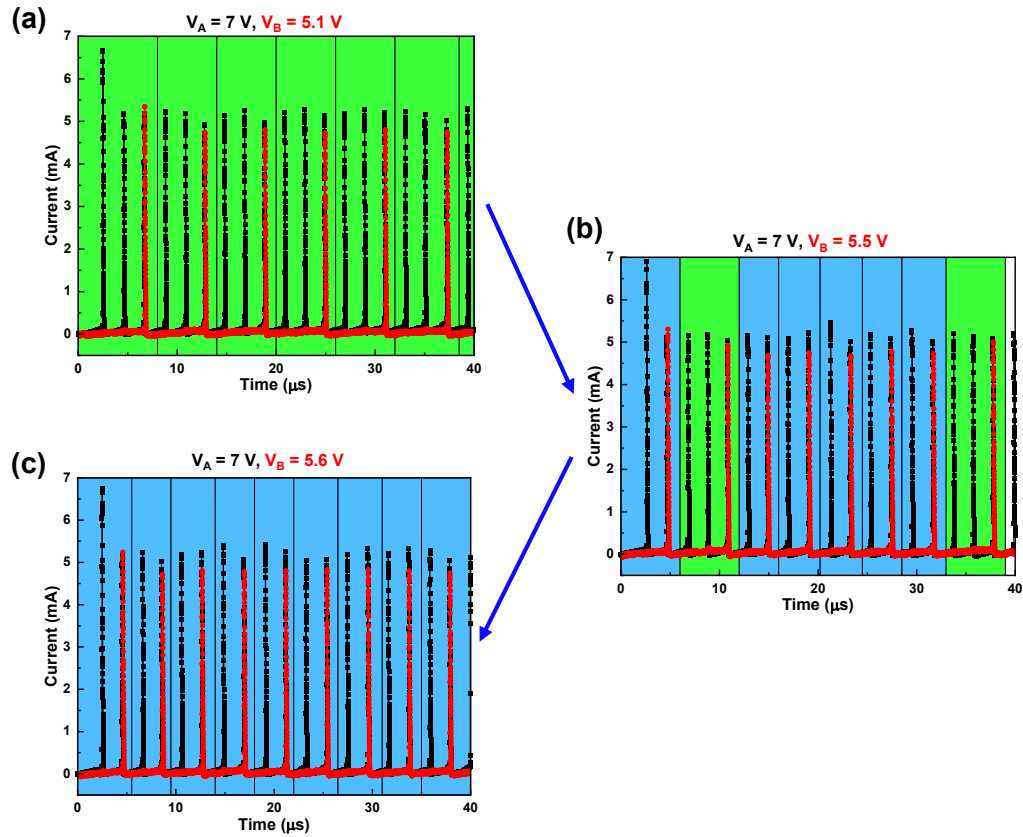


Figure 4.8 Synchronized spiking pattern evolution in a pair of  $100 \times 400 \text{ nm}^2$  devices in a different  $\text{VO}_2$  sample.

Stochastic synchronization transition (b) between 3:1 synchronized mode (a) and 2:1 synchronized mode (c) observed in a pair of  $100 \times 400 \text{ nm}^2$  devices in a different  $\text{VO}_2$  sample.



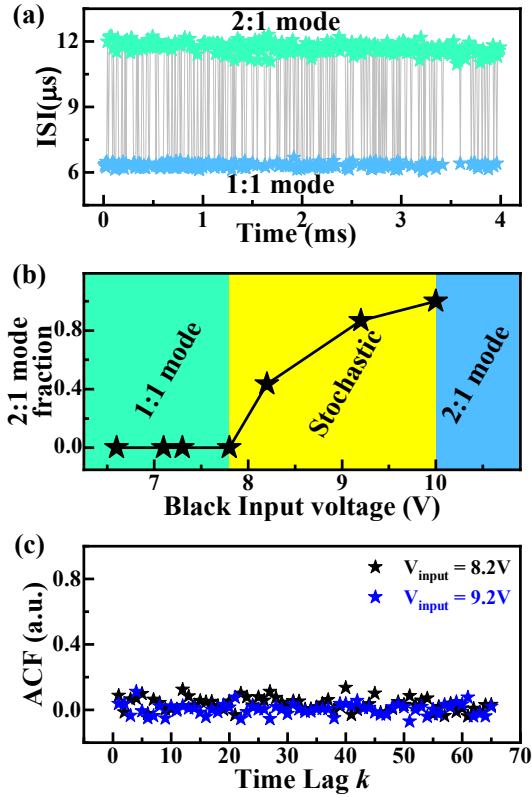


Figure 4.9 Stochastic pattern characterization for the black oscillator in Figure 4.2a.

(a) Inter-spike interval (ISI) evolution of the black oscillator versus time trace when 9.2 V is applied to the black oscillator and 9.2 V is applied to the red oscillator. (b) The dependence of 2:1 mode fraction on the black oscillator input voltage for different emergent patterns. 2:1 mode fraction is defined by the total number of 2:1 mode spikes per the total number of 2:1 mode spikes plus 1:1 mode spikes. The input voltage of the red oscillator is fixed at 9.2 V. The boundaries of the stochastic pattern region are 7.8 V and 10 V. (c) The autocorrelation (ACF) as a function of time lag  $k$  for the black oscillator.

### Simulation of the thermally coupled spiking oscillators:

We simulated the electro-thermal dynamics of the spiking devices by using a lumped-element circuit (Fig. S10). The behavior of VO<sub>2</sub> gap is modeled as a resistor in parallel with a capacitor to account for the parasitic capacitance. Same as in the experiments, a load resistance is connected in series and DC voltage is applied in the circuit.

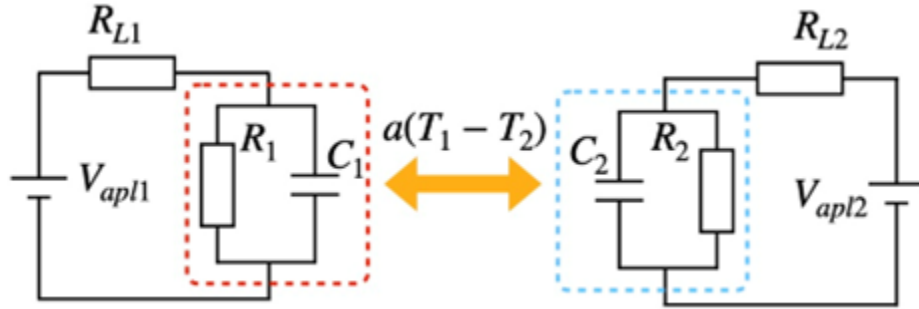


Figure 4.10 Lumped-element model.

$V_{apl1,2}$  are the applied voltages,  $R_{L1,2}$  are load resistors,  $R_{1,2}$  are resistances of the VO<sub>2</sub> devices that can switch between insulator and metallic phase,  $C_{1,2}$  are parasitic capacitances. The term  $\alpha(T_1 - T_2)$  introduces thermal coupling between the devices. Here  $T_{1,2}$  are temperatures of the two VO<sub>2</sub> devices.

The state of the thermally coupled oscillators are described by the coupled electrical (1-2) and thermal (3-4) differential equations:

$$C_1 R_{L1} \frac{dV_1}{dt} + \left(1 + \frac{R_{L1}}{R_1}\right) V_1 - V_{apl1} = 0, \quad (1)$$

$$C_2 R_{L2} \frac{dV_2}{dt} + \left(1 + \frac{R_{L2}}{R_2}\right) V_2 - V_{apl2} = 0, \quad (2)$$

$$C_{th} \frac{dT_1}{dt} - \frac{V_1^2}{R_1} - k(T_s - T_1) - \alpha(T_2 - T_1) = 0, \quad (3)$$

$$C_{th} \frac{dT_2}{dt} - \frac{V_2^2}{R_2} - k(T_s - T_2) - \alpha(T_1 - T_2) = 0, \quad (4)$$

where  $V_i$ ,  $R_i$ ,  $T_i$ ,  $C_i$ ,  $R_{Li}$ ,  $V_{apli}$  are voltage, resistance, temperature, parasitic capacitance, load resistors, and applied voltage in the  $i$ -th oscillator circuit ( $i = 1,2$ ).  $T_s$  is the substrate temperature,  $k$  is thermal conductivity describing the heat exchange between the VO<sub>2</sub> and the substrate,  $\alpha$  is the substrate thermal conductivity allowing the heat transfer between the oscillators, and  $C_{th}$  is thermal capacitance. Importantly, the resistances of VO<sub>2</sub> devices were allowed to switch between low and high resistance states as the temperature of the device crosses the phase transition temperature  $T_c$ . To account for subtle cycle-to-cycle stochastic variability commonly observed in experiments, we explicitly introduced in the model the cumulative transition probability into the metallic phase as a function of temperature given by sigmoid function:

$$P(T) = 1 - \frac{1}{1 + \exp\left(\frac{T - T_c}{\delta T}\right)} \quad (5)$$

where  $\delta T$  is the parameter describing the temperature window where the metal-insulator transition can occur.

The simulations showed that the stochastic transition between 1:2 and 1:1 synchronization modes appears when the coupling between the devices is strong and when devices have a moderate intrinsic stochasticity (Fig. S11). Such a case can correspond to the closely placed nanoscale devices, as studied in this work (small devices are susceptible to

fluctuations and short physical separation enables strong thermal interactions). On the contrary, when the coupling is weak and the stochasticity is insignificant, the transition between 1:2 and 1:1 synchronization modes occurs by the development of an intermediate 2:3 mode (Figure S12). Such a case can correspond to microscale devices, as studied in A. Velichko, M. Belyaev, V. Putrolaynem, V. Perminov, A. Pergament, *Solid State Electronics* **141**, 40, 2018 (large size devices are robust against fluctuations and the separation distance between them is large reducing the thermal coupling).

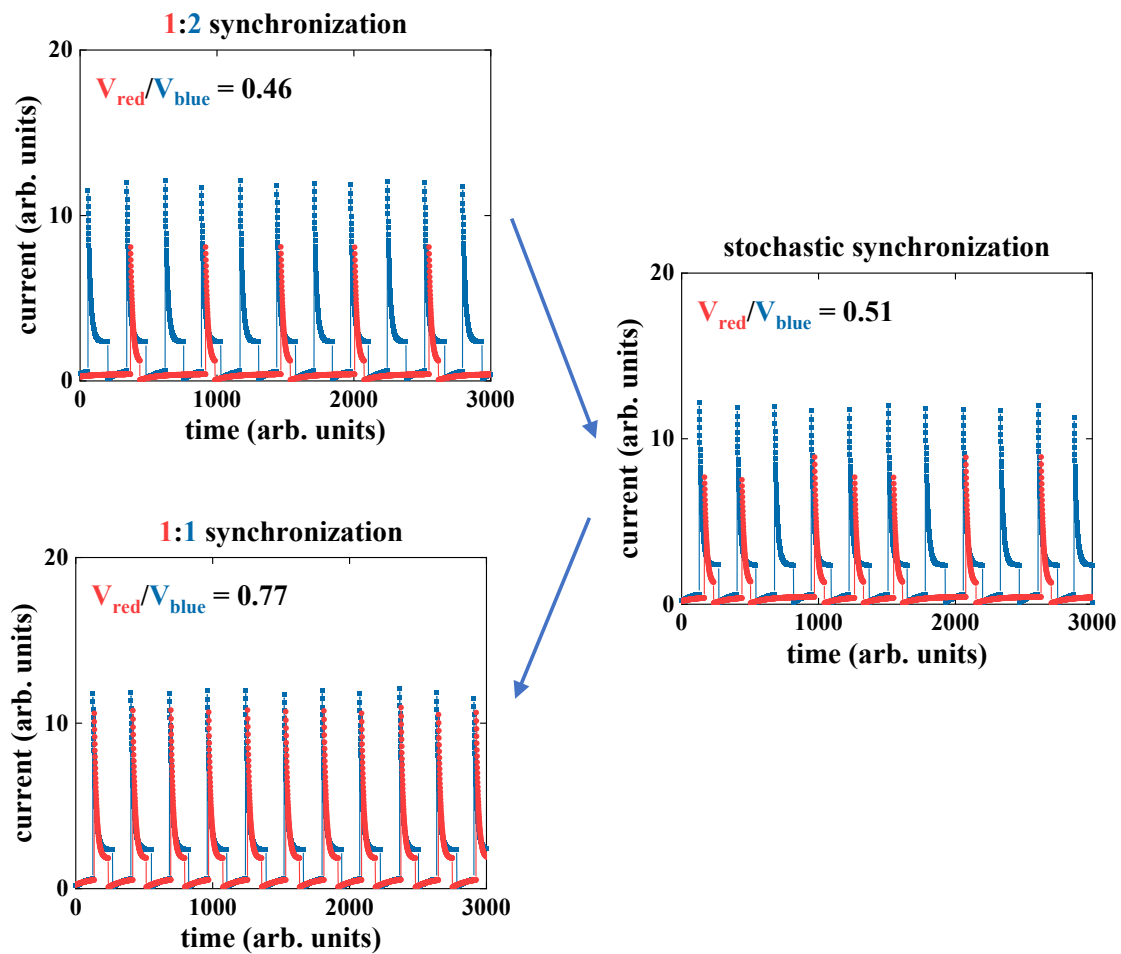


Figure 4.11 Simulation results for stochastic synchronization pattern.

Stochastic transition between 1:2 and 1:1 synchronization modes occurs when the coupling between the oscillators is strong ( $\alpha = 0.1$  arb. units) and the intrinsic stochasticity is moderate ( $T_c = 340$  arb. units,  $\delta T = 1$  arb. units). These simulation results closely resemble the experimental data presented in this work.

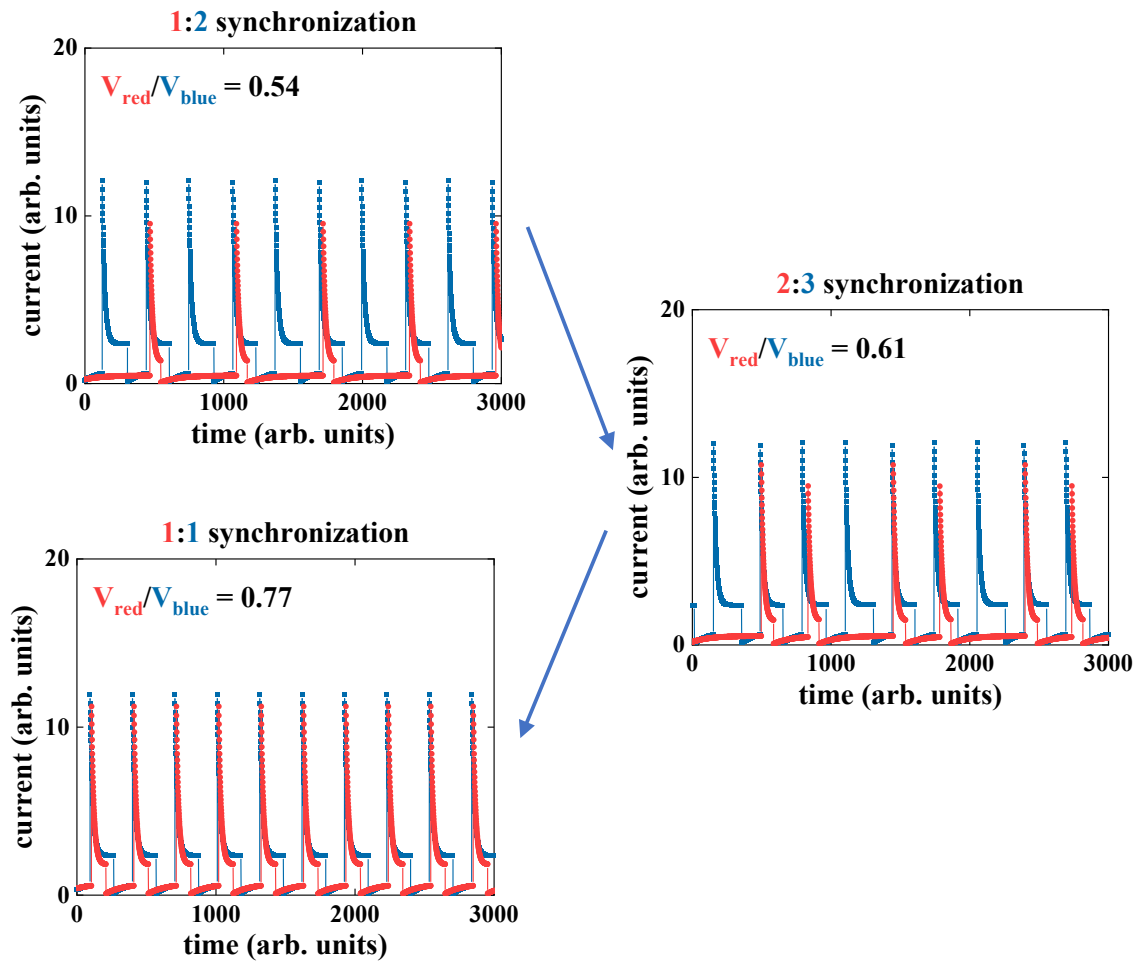


Figure 4.12 Simulation results for non-integer synchronization patterns

Intermediate 2:3 synchronization mode appears at the transition between 1:2 and 1:1 synchronization modes when the coupling between the oscillators is weak ( $\alpha = 0.06$  arb. units) and the intrinsic stochasticity is negligible ( $T_c = 340$  arb. units,  $\delta T = 0.01$  arb. units). These simulation results are reminiscent of the synchronization in microscale devices reported in *Solid State Electronics* **141**, 40 (2018).

## **Appendix C - Supplementary Materials for Chapter 5**

### **Synthesis of epitaxial VO<sub>2</sub> on Al<sub>2</sub>O<sub>3</sub> substrate**

The VO<sub>2</sub> films were deposited on the (012)-oriented Al<sub>2</sub>O<sub>3</sub> substrate by reactive RF magnetron sputtering. Initially, the (012) oriented Al<sub>2</sub>O<sub>3</sub> substrate was loaded into a high vacuum chamber with a base pressure of  $\sim 1 \times 10^{-7}$  Torr. The sample holder was heated to 680 °C. Then pure argon was flown into the chamber at 2.2 s.c.c.m and 2.1 s.c.c.m mixed gases (20% oxygen and 80% argon). The sputtering plasma was triggered at a pressure of 4.2 mTorr by applying a forward power of 100 W to the target, which corresponded to an applied voltage of approximately 240 V. The deposition of VO<sub>2</sub> films lasted 30 mins, achieving a thickness of 100 nm. Upon completion, the sample holder was cooled down to room temperature at a 12 °C/min rate.

### **VO<sub>2</sub> crystal structure**

The crystal structure of the VO<sub>2</sub> thin film was confirmed with a Rigaku Smartlab using 2-theta/omega scan from 20 deg. to 100 deg. in 0.01 deg steps. The Smartlab has a high resolution of 0.0001° and the characteristic wavelength of the copper X-ray tube is 1.5406 Angstroms.

### **Fabrication of VO<sub>2</sub> neuristor arrays**

A Vistec (100kV) Electron Beam Lithography system was used to pattern VO<sub>2</sub> neuristor arrays. Each neuristor has dimensions of 100 x 500 nm<sup>2</sup> and is separated by 500 nm gaps. The e-beam resist, PMMA-A4, was spin-coated onto samples measuring 10 mm x 10 mm followed by a baking process at 115 °C for 20 mins for the first lithography step. Electrodes were defined by depositing a 15 nm Ti layer followed by a 40 nm Au layer. To investigate the thermal interaction between two neuristors, a second lithography and etching process were required. The negative e-beam resist ma-N 2405 was spin-coated onto the previously prepared samples and subsequently

baked for 1 min at 91 °C for the second lithography step. An Oxford Plasmalab 80 Plus RIE system was used to etch the uncovered VO<sub>2</sub> films between the devices, while the negative resist protected the covered electrodes and the devices from being etched away.

### **Fast electrical dynamics measurements**

A Tektronix Dual Channel Arbitrary Function Generator, AFG 3252C, was used to apply DC or pulse voltage bursts to the circuit. The AFG 3252C offers precise waveforms with both fast leading and trailing times of 2.5ns. The dual-channel feature allows us to control the device under test (DUT) individually while ensuring synchronized output signals to the circuit.

For recording ultrafast electrical dynamic signals, we employed the Tektronix Oscilloscope MSO54, which offers a maximum bandwidth of 1GHz and sampling rates of 6.25 GS/s. In particular, the channel impedance for measuring the voltage dynamics was configured to 1 M $\Omega$ , while the channel impedance for measuring the spiking current dynamics was set to 50  $\Omega$ .

## Numerical simulations

### Model of the VO<sub>2</sub> hysteresis loop.

We employed the hysteresis model developed in (44), which assumes that in the insulating phase, VO<sub>2</sub> functions as an inherent semiconductor, characterized by an exponential R-T curve. Conversely, the metallic phase of VO<sub>2</sub> exhibits constant resistance. The metallic phase fraction of VO<sub>2</sub> undergoes a smooth transition from 0 to 1 across a critical temperature, which is different for the heating and cooling branches. Without delving into the derivations, we present the resulting equations:

$$R(T) = R_0 \exp\left(\frac{E_a}{T}\right) F(T) + R_m \quad (S1)$$

$$F(T) = \frac{1}{2} + \frac{1}{2} \tanh\left(\beta \left\{ \delta \frac{w}{2} + T_c - \left[ T + T_{pr} P\left(\frac{T - T_r}{T_{pr}}\right) \right] \right\}\right) \quad (S2)$$

$$T_{pr} = \delta \frac{w}{2} + T_c - \frac{1}{\beta} [2F(T_r) - 1] - T_r \quad (S3)$$

$$P(x) = \frac{1}{2} (1 - \sin \gamma x) [1 + \tanh(\pi^2 - 2\pi x)] \quad (S4)$$

In Eq. (S1),  $R_0 \exp\left(\frac{E_a}{T}\right)$  represents the resistance of the insulating phase,  $R_m$  denotes the resistance of the metallic phase, and  $F(T)$  is the volume fraction of the insulating phase.  $F(T)$  is defined by Eq. (S2), exhibiting a smooth transition from 1 to 0. In Eq. (S2),  $\beta$  serves as a fitting parameter,  $\delta$  takes the value of 1 in the heating branch and  $-1$  in the cooling branch,  $w$  is the width of the hysteresis loop, and  $T_c$  is the critical temperature.  $T_{pr}$  is the proximity temperature at the reversal point, which is introduced to characterize the distance from the current point to the major loop and is essential for characterizing minor and nested loops.  $P$  stands for the proximity function, which is an arbitrarily chosen, monotonically decreasing function, introduced to



approximate the proximity temperature at an arbitrary point.  $T_{pr}$  is further defined in Eq. (S3), in which  $T_r$  is the reversal temperature. Additionally,  $P(x)$  is provided in Eq. (S4), with  $\gamma$  as another fitting parameter. A detailed description and explanation of Eqs. (S1) - (S4) is described in reference (44).

We conducted experimental measurements of the R-T curves for our VO<sub>2</sub> sample using various heating and cooling cycles. The results are illustrated in Figure 1C in the main text. To estimate the optimal parameters for the model, we employed the differential evolution algorithm (45), as implemented in the SciPy library (46), to fit the experimental data to Eqs. (S1) - (S4). The results are:  $R_0 = 5.359 \times 10^{-3} \Omega$ ,  $R_m = 262.5 \Omega$ ,  $E_a = 5220 K$ ,  $\beta = 0.253 K^{-1}$ ,  $w = 7.193 K$ ,  $T_c = 332.8 K$ , and  $\gamma = 0.956$ .

Note that the measured resistance curves contain non-ideal factors such as contact resistance between VO<sub>2</sub> and the electrodes. For comparison, the conductivity of metallic VO<sub>2</sub> is  $8 \times 10^5 S/m$  (47), or  $2.5 \Omega$  for our sample of dimensions  $100 \text{ nm} \times 500 \text{ nm} \times 100 \text{ nm}$ . Given the fitted  $R_m = 262.5 \Omega$ , this indicates that the contact resistance is the primary contributor in the metallic state. On the other hand, for the insulating state, the activation energy of VO<sub>2</sub> thin films at 20°C is about 0.22 eV (44), which gives a theoretical value of  $E_a = 2553 K$ , about half of the fitted result. Indeed, we can observe a divergence between data and model in the insulating state as depicted in Figure 1C, suggesting some limitation in our model. However, it is important to note that this model does accurately reproduce the R-T curves near the insulator-to-metal transition, which is our principal area of interest.

### Model of a single neuristor.

The circuit configuration is shown in Figure 1B in the main text, where the VO<sub>2</sub> nanodevice is modeled as a temperature-dependent resistor in parallel with an intrinsic parasitic capacitance. A variable load resistor is connected in series with the VO<sub>2</sub> nanodevice, whose resistance is typically comparable to the insulating state of the VO<sub>2</sub> nanodevice.

The model of the hysteretic behavior of VO<sub>2</sub> is already illustrated in the previous section. However, it is worth noting that the hysteresis loop in Figure 1C is measured through a quasi-static process, where the device undergoes slow heating, ensuring the entire sample transitions completely into the metallic state above the transition temperature. On the other hand, the scenario in a spiking oscillator is markedly different. As demonstrated in (39), narrow metallic channels emerge within the insulating bulk during each current spike, which yields a higher resistance relative to the fully metallic state recorded in the quasi-static process. In practice, to bypass the intricate task of modeling the complex nonequilibrium thermodynamics, we assume that the metallic channel has a volume fraction of  $1/k$ , where  $k$  is a numerically fitted parameter. In other words, the resistance of the metallic state increases to  $k$  times the value measured through the quasi-static process. Then, thermal conduction is modeled assuming uniform temperature within the neuristor and a constant environmental temperature.

Combining the circuit model and thermal model, we arrive at the following equations:

$$\frac{dV_1}{dt} = \frac{V_{in}}{R_{load}C} - V_1 \left( \frac{1}{R_{VO_2}C} + \frac{1}{R_{load}C} \right) \quad (S5)$$

$$\frac{dT}{dt} = \frac{V_1^2}{R_{VO_2}C_{th}} - \frac{S_{th}(T - T_0)}{C_{th}} \quad (S6)$$

Here,  $V_1$  represents the voltage across the neuristor,  $V_{in}$  is the input voltage,  $R_{VO_2}$  refers to the resistance of VO<sub>2</sub>,  $C$  is the parasitic capacitance,  $T$  denotes the temperature of VO<sub>2</sub>,  $T_0$  denotes the environment temperature, and  $S_{th}$  and  $C_{th}$  stands for the thermal conductance and thermal capacitance of the neuristor, respectively.

The resistance of VO<sub>2</sub> is slightly altered from the quasi-static hysteresis behavior in Eq. (S1) and is expressed as:

$$R_{VO_2}(T) = R_0 \exp\left(\frac{E_a}{T}\right) F(T) + kR_m \quad (S7)$$

where an additional factor,  $k$ , is introduced in Eq. (S7). This factor accounts for the formation of thin metallic channels during the spiking dynamics.

To precisely emulate the spiking behaviors, we extracted key features from the experimentally measured I-t curves and employed the numerical model to replicate these features. Specifically, the characteristics utilized in the numerical fittings include the amplitudes and positions of the first three spikes, the average width of the spikes, and the frequency of spiking. Once again, the differential evolution algorithm was employed to optimize the parameters, yielding the following results:  $C = 145pF$ ,  $k = 4.90$ ,  $S_{th} = 0.206mW/K$  and  $C_{th} = 49.6pJ/K$ . These lead to an excellent agreement between the experimental and simulated curves as shown in Fig 2.

It is important to mention that we operated under the simplified assumption of a uniform temperature across the neuristor and a constant environment temperature. Therefore, the thermal conductance and capacitance calculated here are equivalent values considering the entirety of the device, which includes the VO<sub>2</sub>, the electrodes, and the surrounding substrates. For comparison, the heat capacity per volume of VO<sub>2</sub> at 336K is  $3.07 \times 10^6 J m^{-3} K^{-1}$  (48). For our sample with dimensions  $100 \text{ nm} \times 500 \text{ nm} \times 100 \text{ nm}$ , the heat capacitance is a mere 15.2 fJ/K, representing

only 1/3000 of the fitted value. This demonstrates that the heat capacitance of VO<sub>2</sub> constitutes only a minuscule portion of the neuristor.

Model of thermal coupling between adjacent neuristors.

To account for the thermal coupling between two adjacent neuristors, we introduce a coupling term to Eq. (S6):

$$\frac{dT_1}{dt} = \frac{V_1^2}{R_{VO_2,1}C_{th}} - \frac{S_{th}^{env}(T_1 - T_0)}{C_{th}} - \frac{S_{th}^{12}(T_1 - T_2)}{C_{th}} \quad (S8)$$

$$\frac{dT_2}{dt} = \frac{V_2^2}{R_{VO_2,2}C_{th}} - \frac{S_{th}^{env}(T_2 - T_0)}{C_{th}} - \frac{S_{th}^{12}(T_2 - T_1)}{C_{th}} \quad (S9)$$

Here, the subscripts 1 and 2 denote the two neuristors.  $S_{th}^{env}$  represents the thermal conductance between a neuristor and the environment, and  $S_{th}^{12}$  represents the thermal conductance between the two neuristors.

We define the coupling strength,  $\eta$ , such that  $S_{th}^{12} = \eta S_{th}$  and  $S_{th}^{env} = (1 - \eta)S_{th}$ . As depicted in Figure 5C and 5F of the main text, this thermal coupling model effectively replicates the experimentally observed excitatory and inhibitory behaviors.

The coupling strength  $\eta$  is hard to measure experimentally so we investigated it using numerical simulations. Figure S11 illustrates the coupling between two neuristors under varying values of  $\eta$ . As the coupling strength increases, the neuristors exhibit a phase-locked, 1:1 spiking pattern. Conversely, when the coupling strength is decreased, neuristor B integrates a higher number of heat spikes from neuristor A, resulting in 2:1 or 3:1 spiking patterns, and the synchronization between the neuristors also weakens.

To delve deeper into the phenomenon of thermal coupling, we carried out supplementary simulations using the theoretical model, and the outcomes are depicted in Figure S12 and S13.

Interestingly, phase shifts and interference patterns emerged in these simulations, though these phenomena are not as pronounced in experimental environments. When the spiking frequency of one neuristor is an integer multiple of the other's, a stable synchronization is achieved, which enhances excitatory interaction and reduces the likelihood of inhibitory interactions. Conversely, at non-matching frequencies, phase discrepancies arise, dampening the excitatory interactions while amplifying the inhibitory ones.

Supporting figures.

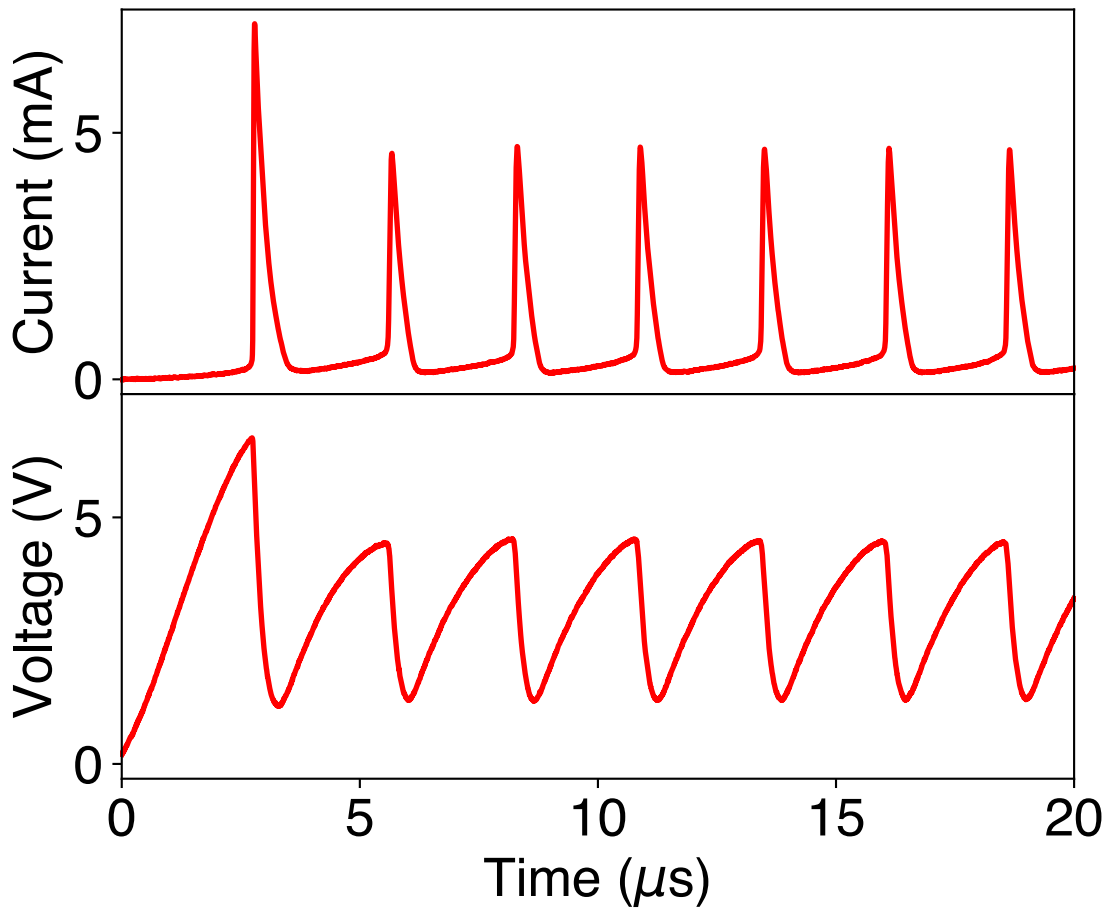


Figure 5.1. Typical Single Neuristor Behavior.

In this figure, the neuristor is connected in series with a  $12\text{ k}\Omega$  load resistor, and the input voltage is  $12\text{ V}$ . When an input voltage is applied to the circuit, the ensuing current heats up the  $\text{VO}_2$  nanodevice, concurrently charging up the parasitic capacitance. Upon reaching the critical threshold voltage, the  $\text{VO}_2$  undergoes an IMT. This abrupt decrease in  $\text{VO}_2$ 's resistance prompts the parasitic capacitance to discharge, resulting in a current spike. As the charge in the capacitance depletes, the majority of the input voltage is dropped across  $R_{load}$ , and the voltage across  $\text{VO}_2$  does not generate sufficient heat to sustain the metallic state, causing the  $\text{VO}_2$  to revert to its insulating state. This process repeats, generating a series of stable spiking auto-oscillations.

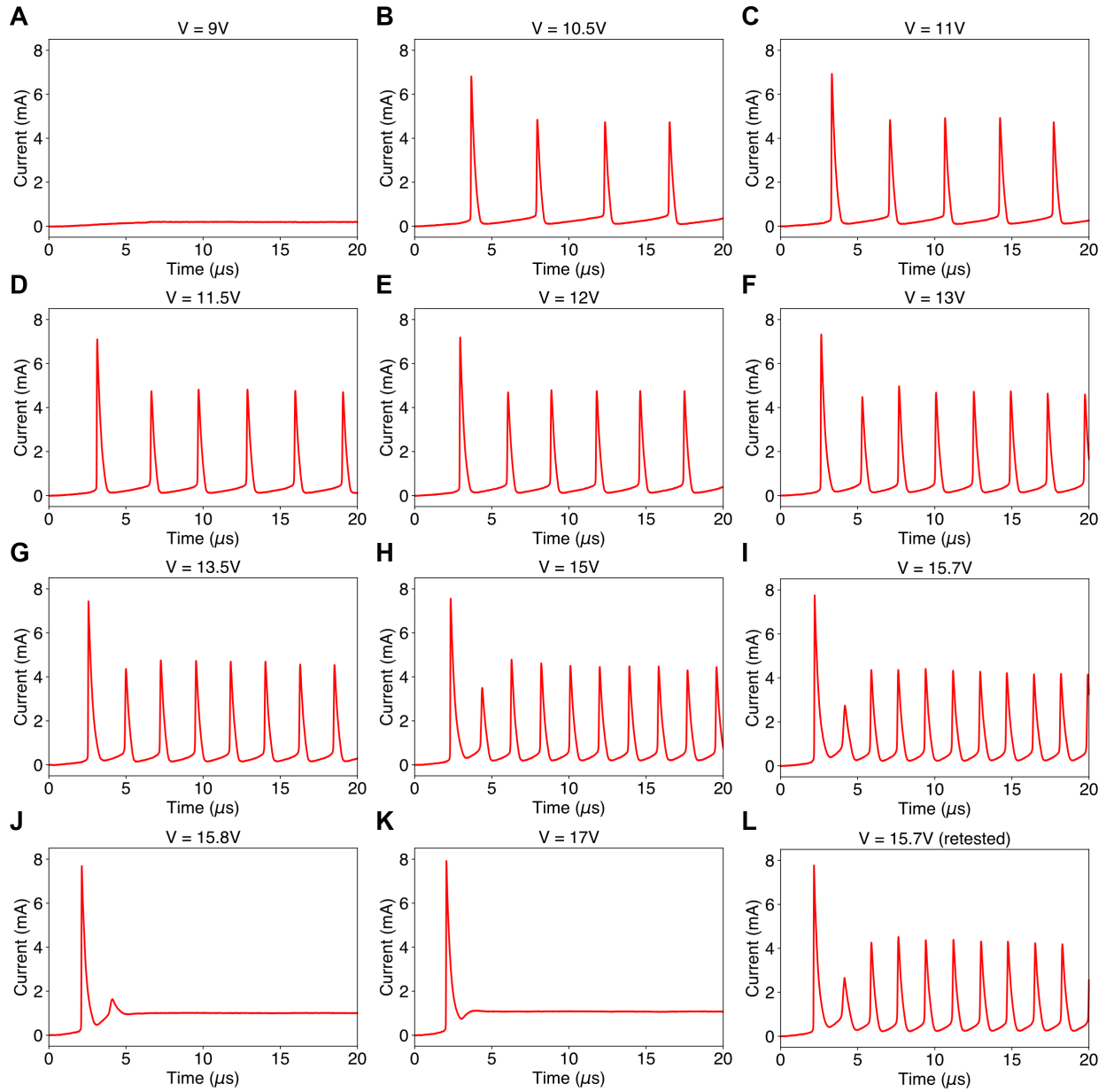


Figure 5.2 Comprehensive Analysis of Single Neuristor Behavior.

All the measurements presented in this figure were carried out at a baseline temperature of 325 K and with a load resistance set at 12 k $\Omega$ . The frequency response depicted in Figure 2D of the main text is computed utilizing this data set collected using various voltage levels. (A) At a subthreshold voltage of 9V, the neuristor exhibits no current response. (B)-(I) When supplied with a sufficiently high input voltage, the neuristor operates as a spiking oscillator, with the spiking frequency increasing as the input voltage increases. (J)-(K) Upon the application of voltage exceeding the upper boundary, the neuristor becomes confined to its metallic state following a single current spike. (L) Subsequent to the experiments outlined in panels (J) and (K), the neuristor's behavior was rebiased at 15.7V, where stable spiking resumes. This confirms that the inhibitory behavior depicted in panels (J) and (K) is not due to degradation of the nanodevice.

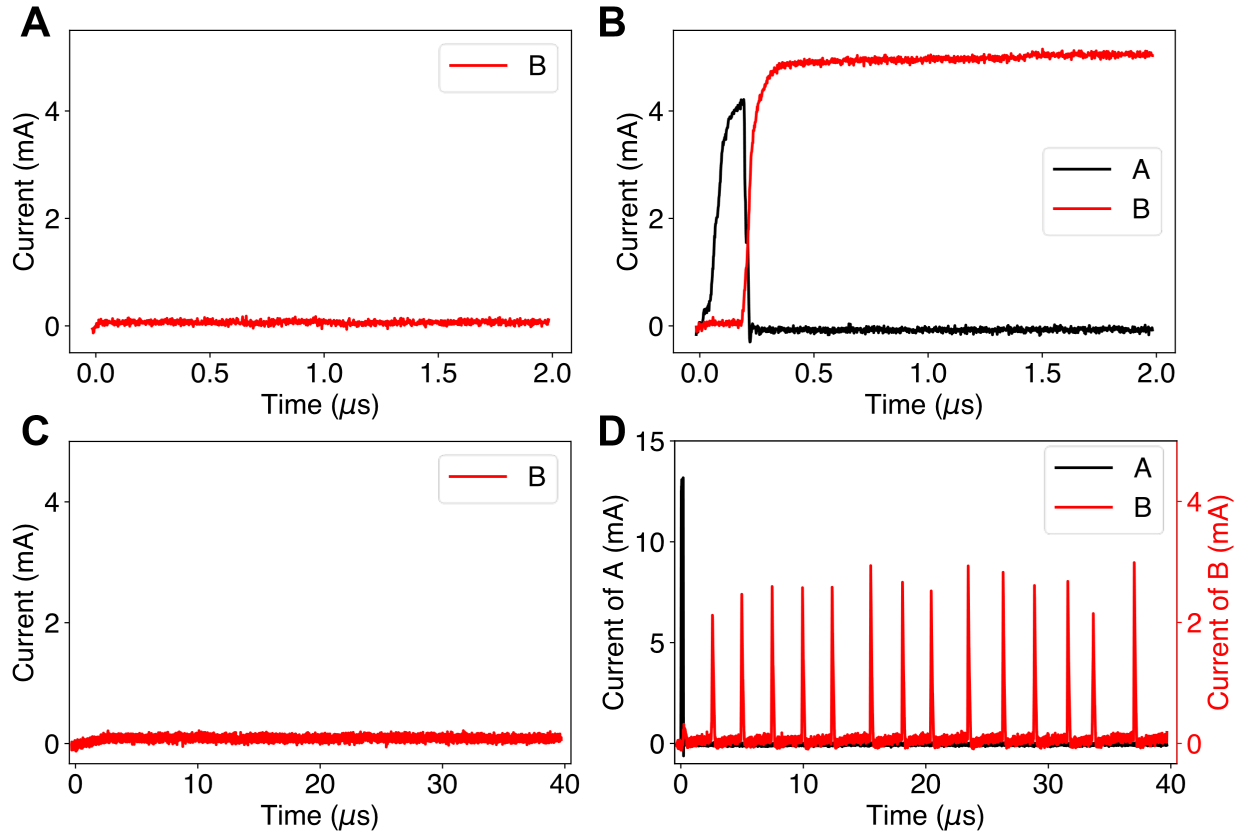


Figure 5.3 Baseline currents in coupled neuristors.

This figure serves as a supplement to Figure 3A and 3B in the main text, showing the baseline currents. (A)(B) Spike-in and DC-out. Panel (A) demonstrates that neuristor B, biased with a subthreshold voltage of 1.5V, exhibits no current response when there is no input to neuristor A. However, as illustrated in panel (B), a current spike in neuristor A triggers the insulator-to-metal transition (IMT) in neuristor B, resulting in a direct current (DC) output. (C)(D) Spike in and spike out. Similarly, panel (C) indicates that neuristor B remains unresponsive when neuristor A is deactivated. However, a single spike in neuristor A initiates stable spiking patterns in neuristor B, as depicted in panel (D).



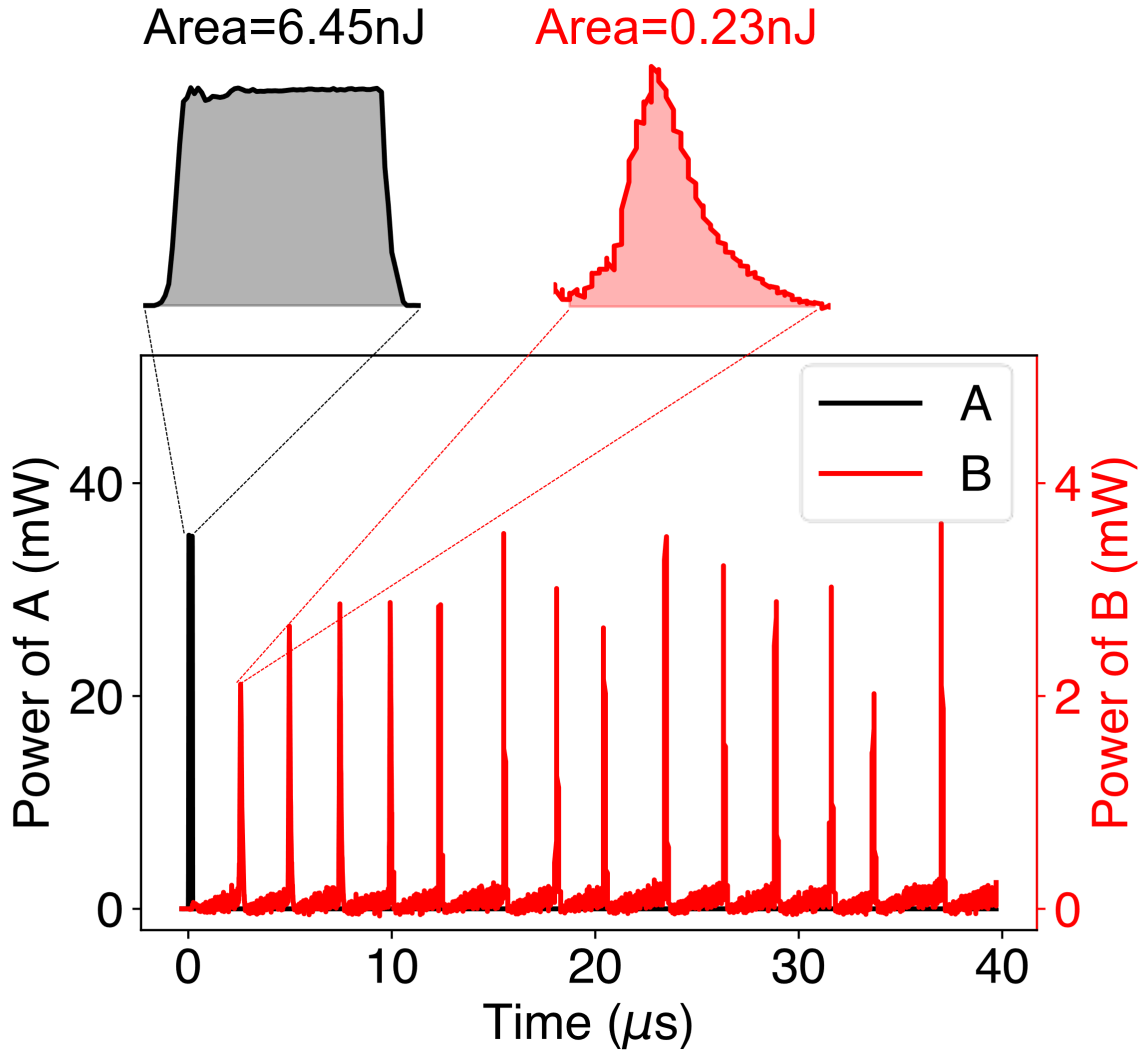


Figure 5.4 Power dissipation in coupled oscillators.

This figure is related to Figure 3B in the main text and depicts the power dissipation over time in two coupled neuristors. The initial spike in neuristor A consumes 6.45 nJ of energy and activates 14 subsequent spikes in neuristor B. The energy consumption of the first spike in neuristor B is 0.23 nJ, and the total energy output for the 14 spikes is 5.56 nJ.

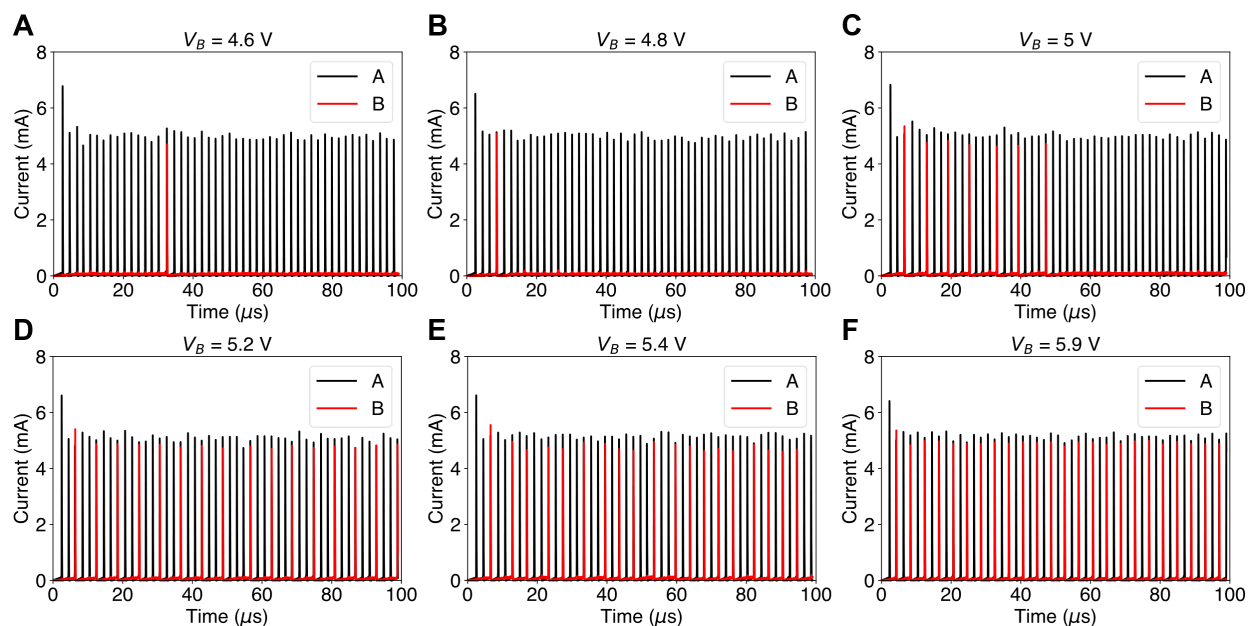


Figure 5.5 Stochastic leaky integrate-and-fire behavior in coupled neuristors.

This figure employs the same parameters as Fig. 3C in the main text, with neuristor A receiving an input of 7V in series with 22k ohms and neuristor B subjected to varying input voltages in series with 30k ohms. As the input voltage is increased, neuristor B needs to integrate fewer spikes from neuristor A, and the spiking pattern becomes more deterministic. This phenomenon has been systematically analyzed, and a corresponding heatmap is presented in Figure 3D in the main text.

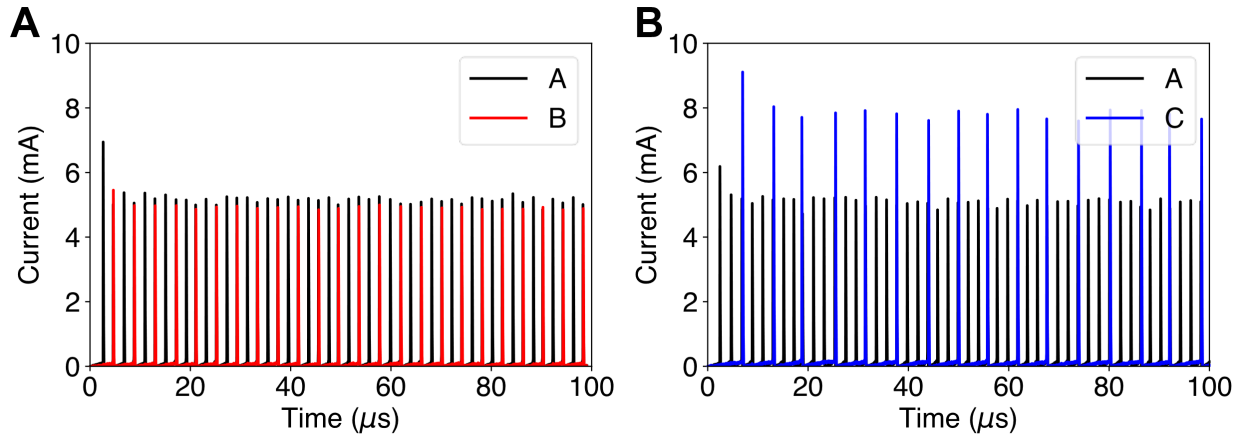


Figure 5.6 Impact of Distance on Information Transfer Among Neuristors.

In this figure, neuristors A, B, and C are positioned in parallel to each other, with a  $0.5\mu\text{m}$  distance between A and B and a  $1.5\mu\text{m}$  distance between A and C. All three neuristors have an identical threshold voltage of 6V. Neuristor A receives an input voltage of 7V, while neuristors B and C both receive input voltages of 5.9V. In this configuration, neuristor B needs to integrate two spikes from neuristor A to generate its own spike, whereas neuristor C needs to integrate three spikes.

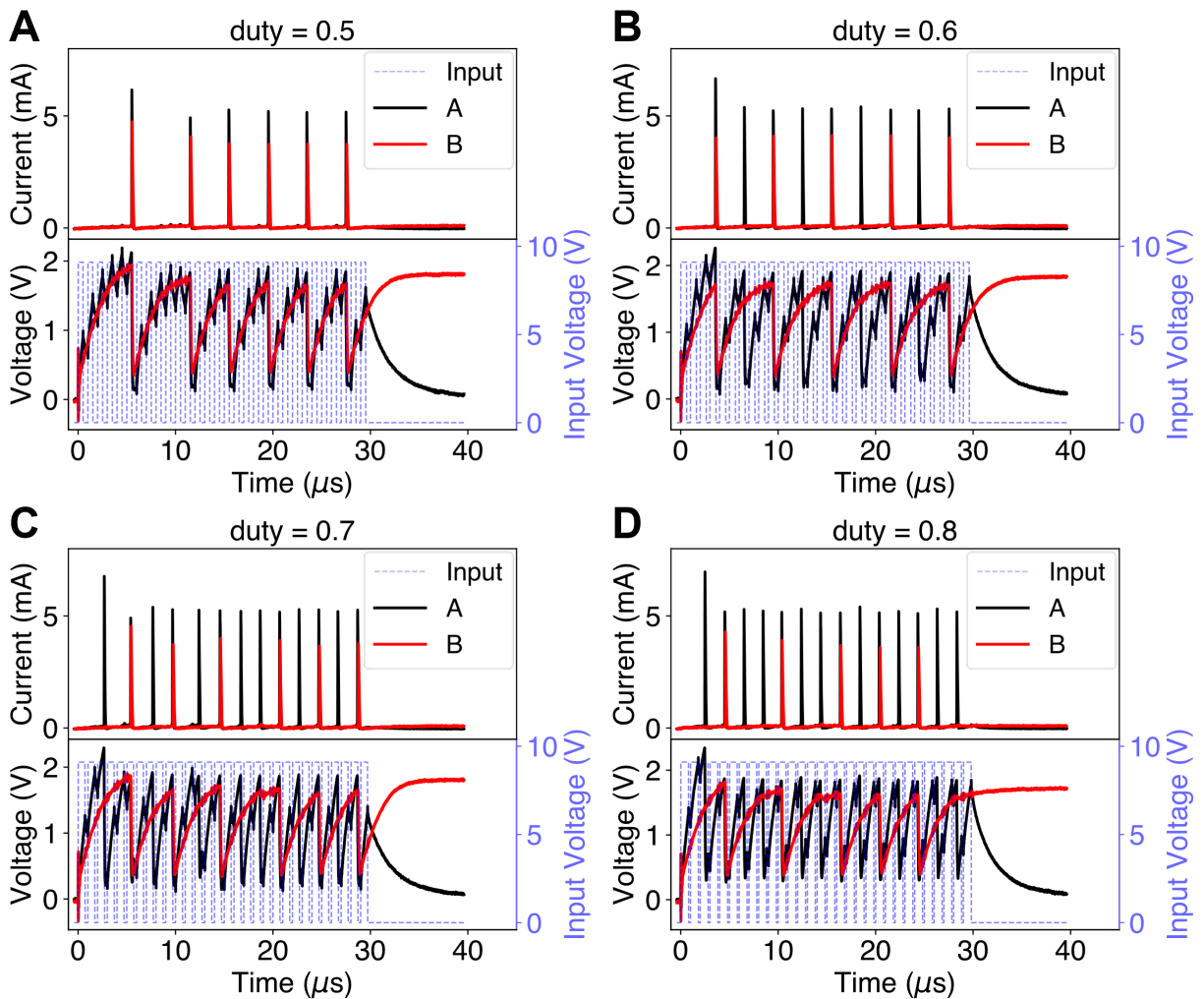


Figure 5.7 Cascaded information transfer between coupled neuristors.

This figure serves as an extension to Figure 5.4 in the main text and illustrates the variations in spiking rates under different input duty cycles, as well as the relationship between current and voltage curves. In each panel, the sudden drop in voltage corresponds to a current spike. At a 50% duty cycle, neuristor A integrates more input electrical pulses, providing neuristor B with ample time for heat spike integration from neuristor A, and resulting in a 1:1 spiking pattern. As the duty cycle increases, the spiking frequency of neuristor A escalates. However, this leads to some spikes from neuristor A coinciding with neuristor B's refractory period, rendering them unable to trigger subsequent spikes in neuristor B. As a result, 2:1 or 3:1 spiking pattern emerges.

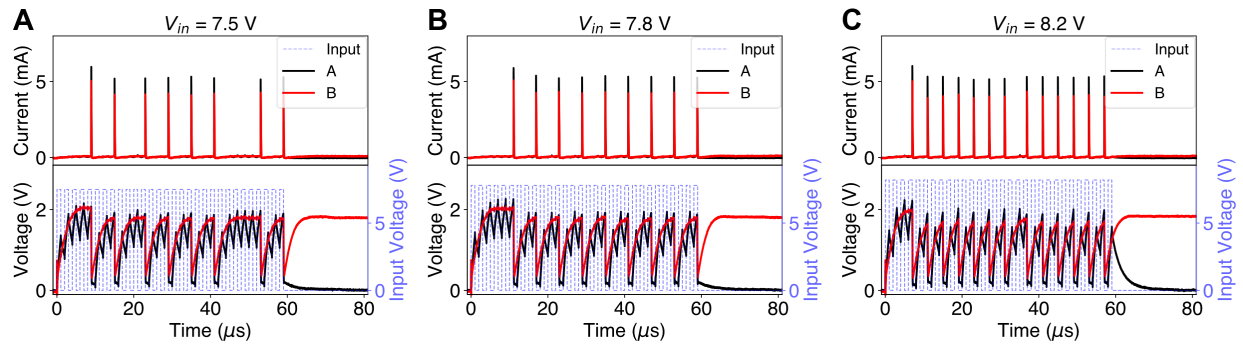


Figure 5.8 Cascaded Information Transfer in Coupled Neuristors with Varying Amplitudes.

This figure shares a similar setup with Figure S6, with the distinction that neuristor A receives square pulses having a 50% duty cycle, a period of  $2\mu\text{s}$ , and varying amplitudes. The rate coding behavior is evident, where an increased input voltage correlates with a higher frequency. This behavior is subsequently propagated through the following layers.

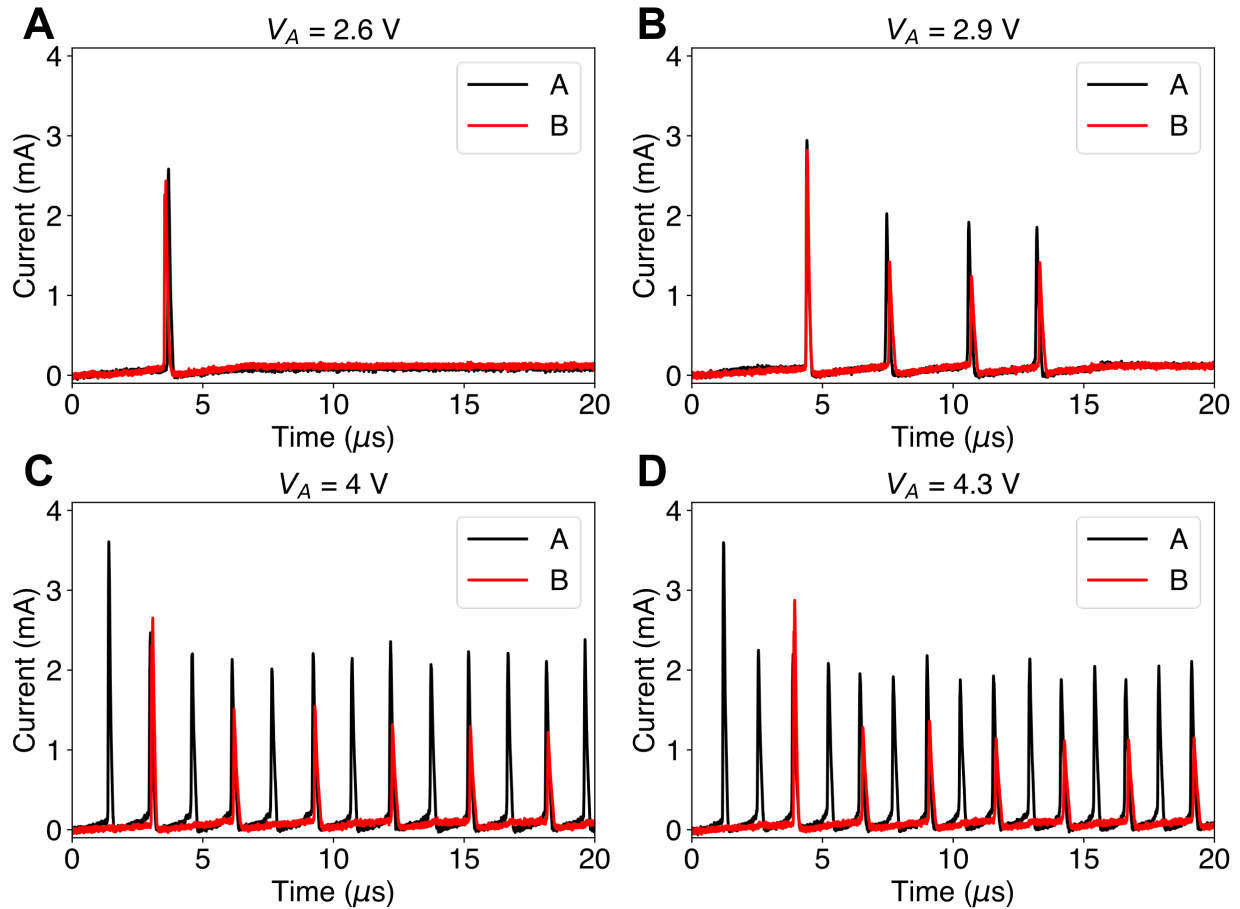


Figure 5.9 The evolution of excitatory characteristics with input voltage between adjacent neuristors.

This figure is an extension to Figure 5 in the main text. Both neuristors are connected with a load resistance of  $12\text{k}\Omega$ . Neuristor A has a threshold voltage of  $2.9\text{V}$ , whereas neuristor B has a threshold voltage of  $2.8\text{V}$ . In all panels, the input voltage to neuristor B is kept constant at  $2.6\text{V}$ , which is insufficient for it to spike independently. (A) With  $V_A$  at  $2.6\text{V}$ , the two neuristors mutually excite each other, generating a single spike. (B) At the threshold voltage  $V_A = 2.9\text{V}$ , every spike from neuristor A induces a corresponding spike in neuristor B, yielding a 1:1 spiking pattern. (C) At  $V_A = 4\text{V}$ , neuristor A exhibits a higher spiking frequency, leading to a 2:1 spiking pattern. (D) At  $V_A = 4.3\text{V}$ , the spiking frequency of neuristor A increases even further, while neuristor B adjusts to sustain the 2:1 spiking pattern.

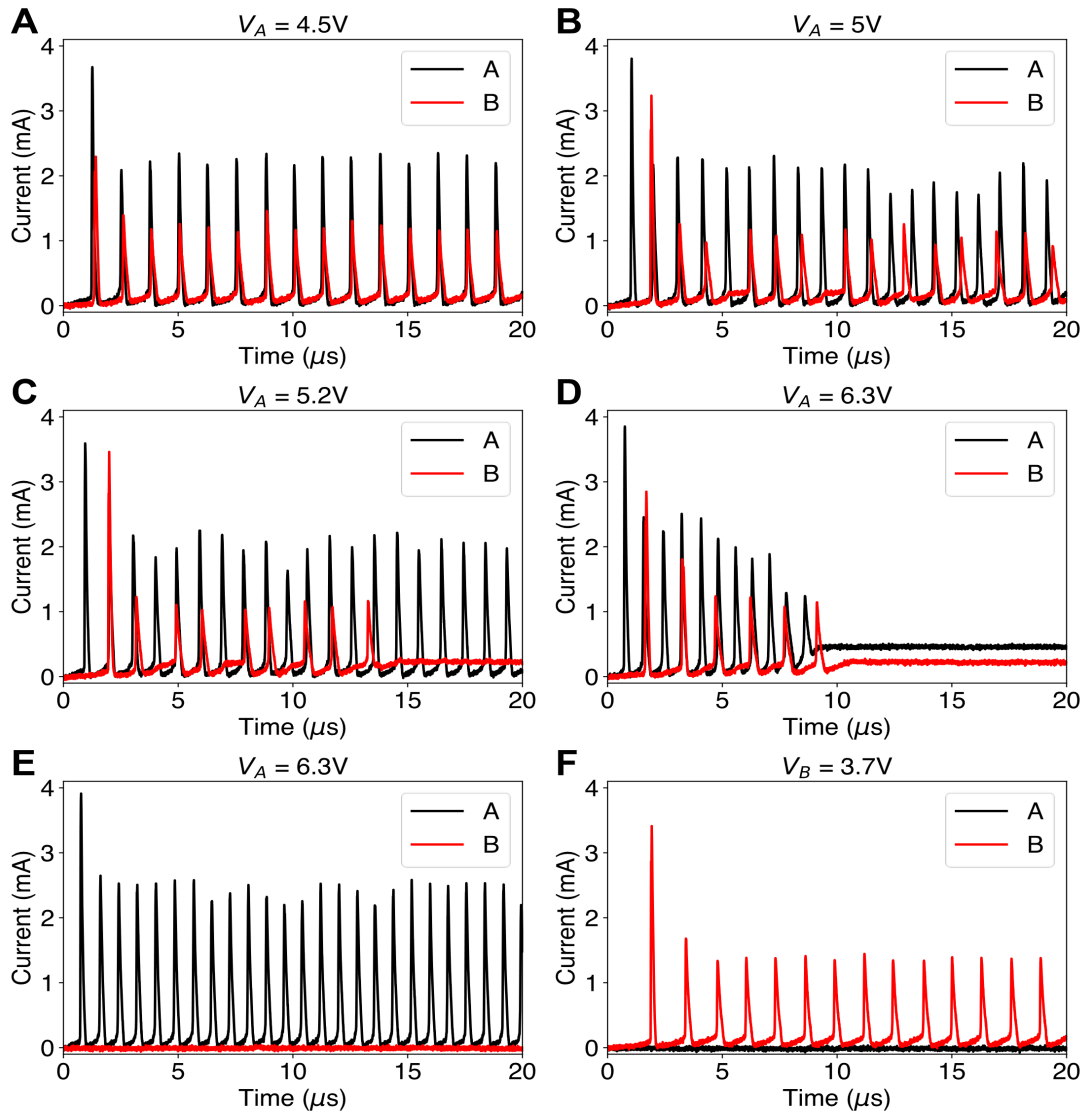


Figure 5.10 Another reconfigurable inhibitory characteristic between adjacent neuristors.

This figure also complements the results presented in Figure 5 of the main text. Both neuristors are coupled with a load resistance of  $12\text{k}\Omega$ . Neuristor A possesses a threshold voltage of  $2.9\text{V}$ , whereas neuristor B has a threshold voltage of  $2.8\text{V}$ . Neuristor B's input voltage remains fixed at  $3.7\text{V}$ , close to its upper boundary. (A) At  $V_A = 4.5\text{V}$ , the neuristors synchronize, displaying a 1:1 spiking pattern. (B) Elevating  $V_A$  to  $5\text{V}$  increases neuristor A's spiking frequency, thereby disrupting the synchronization and causing irregular spiking amplitudes and phase mismatches in neuristor B. (C) Further increasing  $V_A$  to  $5.2\text{V}$  exacerbates the irregularities in neuristor B's spiking pattern to the extent that it eventually stops spiking. (D) With  $V_A$  at  $6.3\text{V}$ , mutual inhibition occurs between the neuristors, causing both to terminate spiking after their initial spikes. (E) Without input to neuristor B, neuristor A can spike independently with an input voltage of  $6.3\text{V}$ . (F) Similarly, without input to neuristor A, neuristor B is capable of spiking independently at an input voltage of  $3.7\text{V}$ .

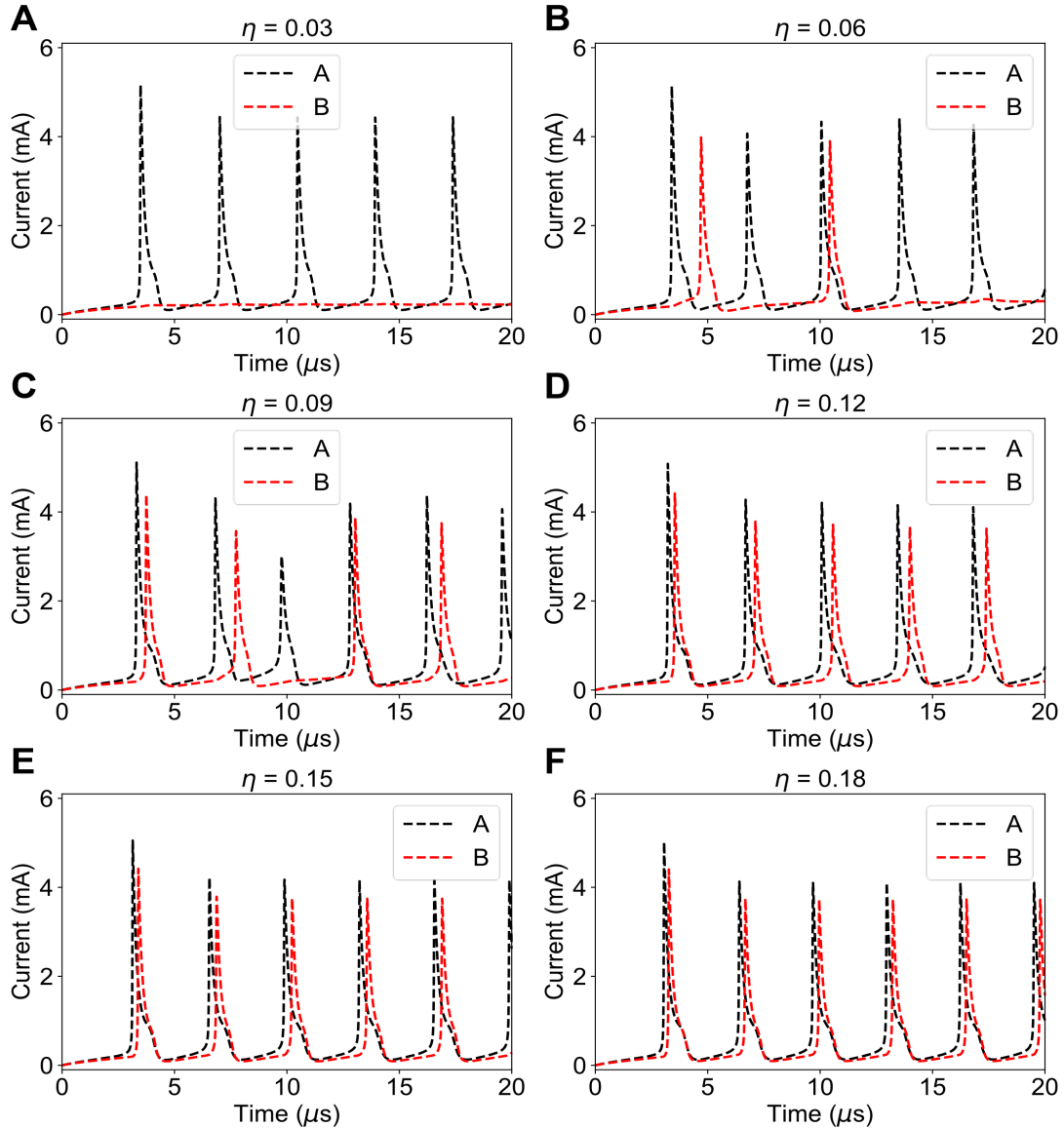


Figure 5.11 Numerical simulations illustrating excitatory behavior under various coupling strengths.

The parameters for the two neuristors in this simulation are the same as those outlined in Figure 5.2 of the main text, with a spiking interval ranging from 10V to 15.7V when a 12k $\Omega$  load resistance is connected. The input voltages are set at  $V_A = 11V$  and  $V_B = 9.4V$ , while the coupling strength  $\eta$  between the two neuristors changes. (A) When  $\eta = 0.03$ , thermal energy from neuristor A is insufficient to induce spiking in neuristor B, which remains inactive. (B) At  $\eta = 0.06$ , spikes are excited within neuristor B, but the interaction is not strong enough to achieve synchronization. (C) With  $\eta$  at 0.09, synchronization begins to emerge, albeit with occasional mismatches. (D)-(F) As  $\eta$  continues to increase, the neuristors achieve stable 1:1 spiking synchronization, with the phase difference between them diminishing as  $\eta$  grows.



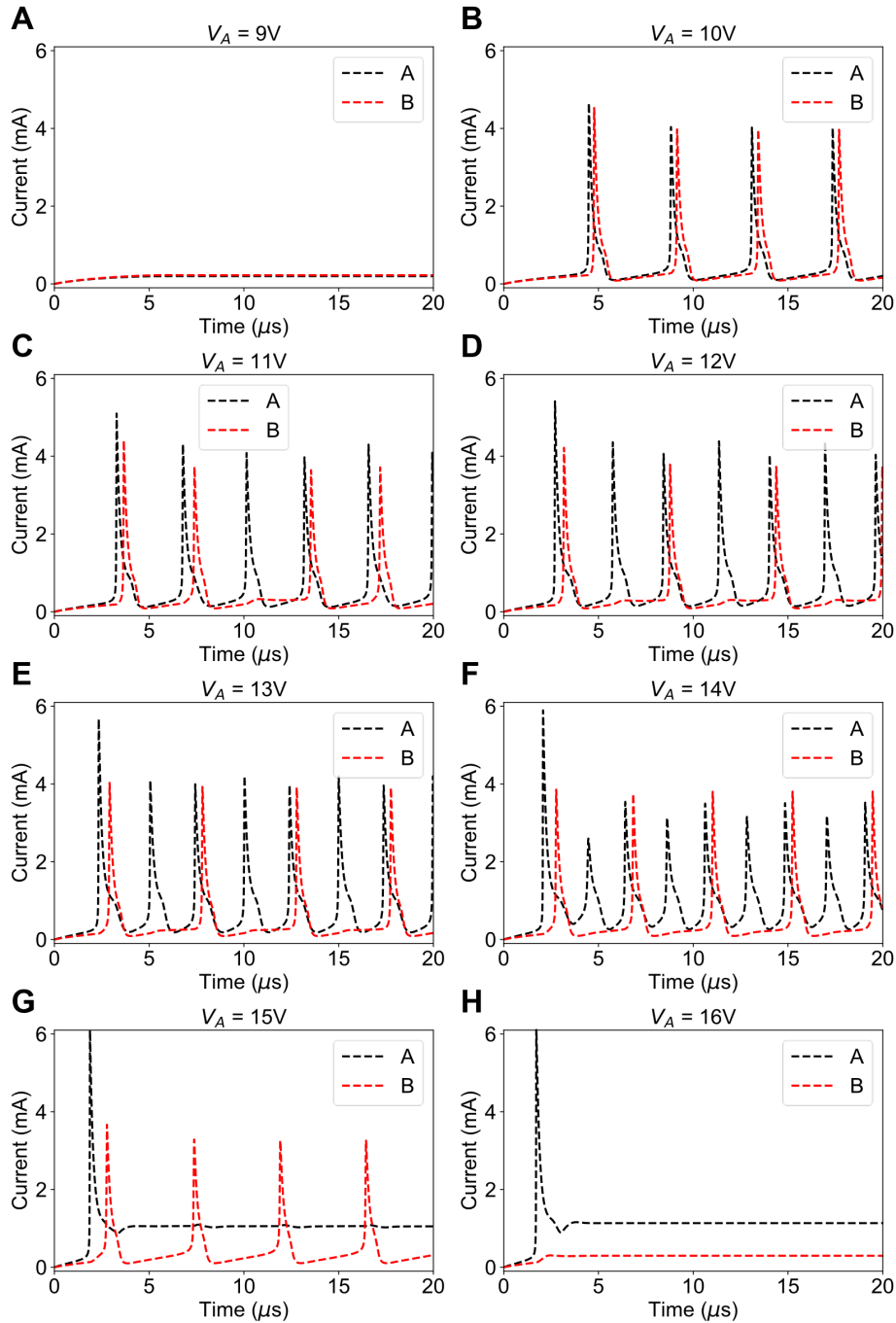


Figure 5.12 Numerical simulations of excitatory behavior under various input voltages.

This simulation uses a similar setting to Figure 5.15, with a fixed coupling strength of  $\eta = 0.1$  and  $V_B = 9.4V$ , while varying  $V_A$ . As depicted from panel (A) to panel (H), as  $V_A$  increases, neuristor B transitions from a quiescent state to a 1:1 spiking mode, then to a 2:1 spiking mode, and ultimately reverts back to a quiescent state. When the frequency of neuristor A matches an integer multiple of the intrinsic frequency of neuristor B, pronounced synchronization is observed between the two neuristors. However, in cases where the frequencies do not align in this manner, phase mismatches occur, and the spiking amplitudes of the neuristors are slightly suppressed.

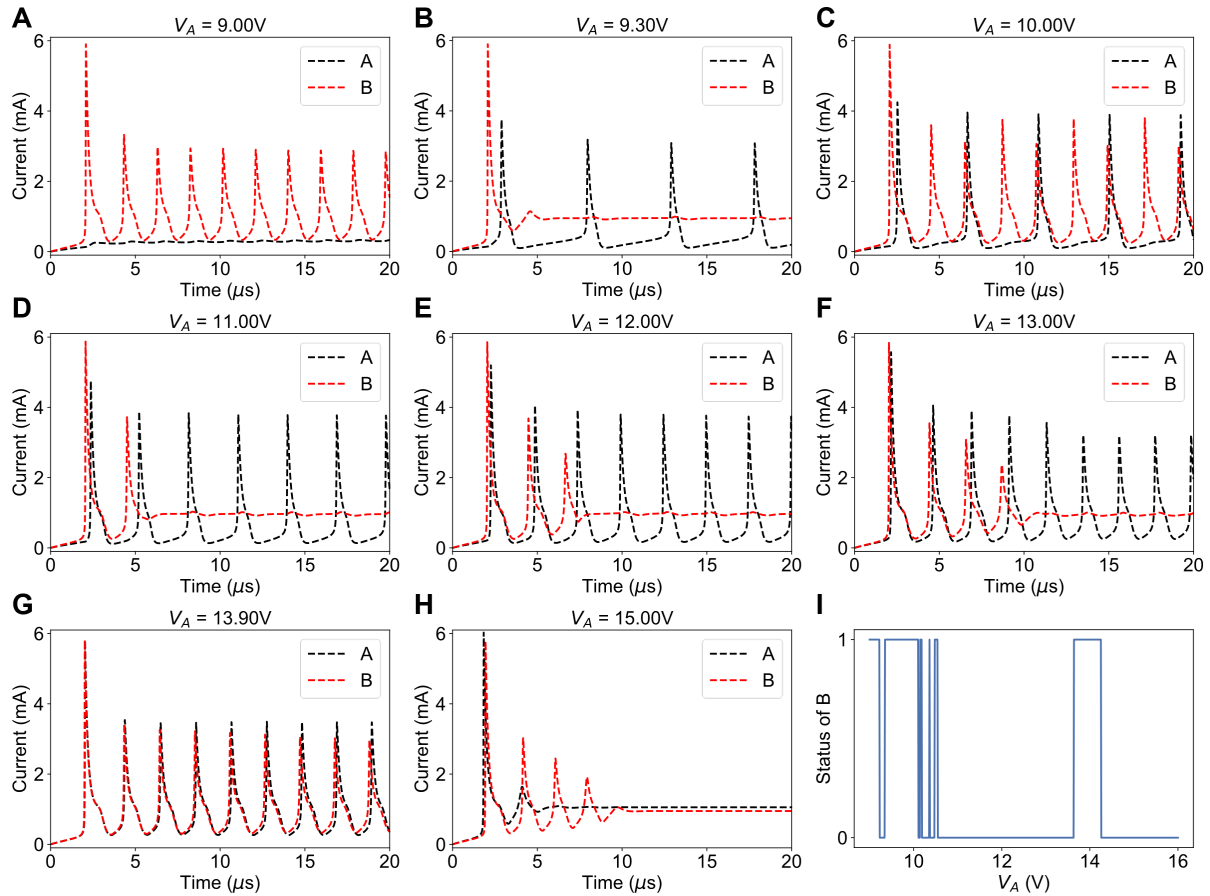


Figure 5.13 Numerical simulation of the inhibitory behavior under various input voltages.

This simulation also has a similar setting to Figure S11, with a fixed coupling strength of  $\eta = 0.1$  and  $V_B = 14\text{V}$ , while varying  $V_A$ . (A) With an input voltage of  $9\text{V}$ , neuristor A does not spike, whereas neuristor B exhibits stable spiking at  $V_B = 14\text{V}$ . (B)-(H) A range of inhibitory interactions between the two neuristors. When neuristor A spikes stably, neuristor B is typically inhibited and ceases to spike after initial spikes. Notable exceptions are observed in panel (C), which shows a stable 2:1 spiking pattern, and panel (G), which features stable 1:1 spiking. This suggests that the inhibitory interaction stems from phase mismatches between the two neuristors. In panel (H), with  $V_A$  set too high, mutual inhibition occurs between the neuristors. (I) This panel presents the state of neuristor B when different  $V_A$  are applied. 1 representing spiking and 0 representing inhibition. The interaction proves to be rather complex; however, in general, neuristor B resumes spiking when the frequency of neuristor A is an integer multiple of its own.