UNIVERSITY OF CALIFORNIA, SAN DIEGO

Sulfur Passivation of Interface between Aluminum Oxide and Silicon Germanium

A Thesis submitted in partial satisfaction of the requirements for the degree Master of Science

in

Engineering Sciences (Mechanical Engineering)

By

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The Thesis of Kai-Ting Hu is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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List of Abbreviations

Atomic Layer Deposition	ALD
Angle Resolved X-Ray Photoelectron Spectroscopy	AR-XPS
Capacitance-Voltage	C-V
Complementary Metal-Oxide Semiconductor	CMOS
Current-Voltage	I-V
Direct Current	DC
Equivalent Oxide Thickness	EOT
Field-Effect Transistor	FET
Fin Field-Effect Transistor	FinFET
Integrated Circuit	IC
Metal-Oxide-Semiconductor Capacitor	MOSCAP
Metal-Oxide-Semiconductor Field Effect Transistor	MOSFET
Molecular Beam Epitaxy	MBE
Three dimensional	3D

List of Symbols

Aluminum	Al
Aluminum Oxide	Al_2O_3
Ammonium Sulfide	$(NH_4)_2S$
Angstrom	Å
Argon	Ar
Dimethylaluminum	DMA
Density of Border Traps	N_{bt}
Density of Interface Traps	D_{it}
Flat Band Voltage	V_{FB}
Gallium Arsenide	GaAs
Gallium Nitride	GaN
Germanium	Ge
Germanium Dioxide	GeO_2
Germanium Oxide	GeO_x
Hafnium Dioxide	HfO_2
Hydrogen	H_2
Hydrogen Fluoride	HF
Indium Gallium Arsenide	InGaAs
Nickel	Ni
Nitrogen	N_2
Oxygen	O
Silicon	Si
Silicon Dioxide	SiO_2
Silicon Germanium	SiGe
Trimethylaluminum	TMA
Water	H_2O

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Abstract of the Thesis

Sulfur Passivation of Interface Between Aluminum Oxide and Silicon Germanium

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Master of Science in Engineering Sciences (Mechanical Engineering)

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Professor Andrew Kummel, Chair

It is well known that silicon germanium (SiGe) is a promising candidate for the next generation of complementary metal-oxide-semiconductor (CMOS) integrated-circuit (IC) with the advantage of having high electron and hole mobility compared to silicon (Si). The high-k materials are commonly been used for scaling down the gate oxides. However, efficient strategies to passivate the interface between SiGe and high-k gate oxides still need to be understood since the native oxide on the SiGe surface increases the interface defects and adversely affect the device quality.

In this thesis, aluminum oxide (Al_2O_3) had been deposited on SiGe (001) substrates by atomic layer deposition (ALD). To minimize the defect density between Al_2O_3 and SiGe, two wet clean recipes with HF and HF plus $(NH_4)_2S$ have been

developed to both remove the native oxide and chemically passivation SiGe surfaces. Based on cleaning recipes, two studies were performed, one on the effect of ALD temperature on quality on Al_2O_3/SiGe interfaces and the other, on air stability of SiGe surfaces with different wet clean recipes prior to ALD. Al2O3/SiGe interfaces were characterized electrically by capacitance-voltage (C-V) spectroscopy and chemically by angle-resolved X-ray photoelectron spectroscopy (AR-XPS).

It has been shown that low-temperature ALD processes have the ability to attain a high interface quality with lower density of interface and border traps. Both cleaning methods led to good air stability up to an hour, extending the viable manufacturing queue time. In addition, sulfur treatment suppressed GeOx formation and increased Al2O3 nucleation density on SiGe surfaces, which led to lower leakage current while achieving the record equivalent oxide thickness (EOT) of 2.0nm for Al2O3/SiGe devices.

Chapter One

Introduction

1.1 Preview

In over seventy years of the semiconductor electronics development, the power of electronics and logic devices have raised exponentially with increasing the density of silicon CMOS transistor. Based on Moore's law and by the development of nanotechnology, semiconductor industry has continually pushed to the extremes of device size and performance. This push has led silicon transistor scaling to reach its limits, threatening end the revolution of micro/nano electronics. Therefore, seeking alternative materials to replace Silicon has attracted many of the researchers in the past two decades. One material system that has received an increasing amount of attention over the past few years is Silicon Germanium (SiGe) alloy. SiGe offers a combination of high electron and hole mobility and high saturation velocity all of which make it an attractive channel material in future CMOS devices.

One of the most common device architectures in IC products is metal-oxide-semiconductor field effect transistor (MOSFET). The MOSFET is a type of transistor used for switching or amplifying electronic signals. The major advantage of MOSFET is the low current switching requirements and low power consumption and low susceptibility to gate oxide leakage. There are several challenges while scaling the MOSFET. One of the most critical of these is the creation of low-defect interfaces between the gate dielectrics and underlying SiGe channel. Failure to form a low-defect oxide/SiGe interface can severely impact the device performance in that defects cause

degradation of carrier mobility, time-dependent breakdown, anomalous current outputs, as well as Fermi level pinning[13].

The work presented in this thesis is focused upon developing the different wet clean processes before gate oxide deposition that minimize the formation of interfacial and bulk oxide defects.

1.2 Overview of Silicon Germanium Fin Field-Effect Transistor

The challenge of next generation of MOSFET is to reduce the leakage current as scaling down the structure including the gate oxides. To maintain a sustainable progress in device scaling, major semiconductor foundries introduced smaller geometry CMOS process nodes using planar field-effect transistor (FET) technology to increase the gate density. However, as MOSFET channel length and oxide thickness lowered, static leakage became an important factor such that the leakage current will increase as a function of gate density.

One of the promising method to deal with short channel effects on leaky transistors is the fin field-effect-transistor (FinFET). FinFETs are the three-dimensional (3D) structures that rise above the planar substrate and resemble a fin, giving them more volume than a planar gate for the same planar area. The gate wraps around the fin giving an excellent control of the conducting channel and allows small current leakage through the structure when the device is in the off state. This structure property allows the use of the lower threshold voltages and result in better optimal switching speeds and power. FinFETs promise to speed up the transistor to reduce the power consumption compare to the equivalent planar FET.

Except focusing on the MOSFET structure design, the change of substrate material can improve transistor effectiveness. Silicon germanium will be a good alternative material to silicon considering its high mobility particularly by virtue of strain-induced effects. Inducing strain fundamentally improves MOSFETs' drive currents by altering the band structure of the channel and can therefore enhance performance even

at aggressively scaled channel lengths. A relaxed $Si_{1-x}Ge_x$ graded buffer creates a larger lattice constant on a Si substrate (i.e., “virtual substrates”) and can be used as an epitaxial template for depositing Si-rich layers in a state of biaxial tension or Ge-rich layers in a state of biaxial compression. The $Si_{1-x}Ge_x$ substrates, a band-engineered hetero-structure, intentionally induced uniaxial strain in the channel regeion of Si bulk MOSFETs, allows the electrons and holes confine in wafer-scale strained layer during fabrication.

To combine both finFETs and SiGe advantage, the SiGe finFET is a promising structure for next generation transistor. Unlike other substitute materials such as gallium arsenide (GaAs), SiGe is fully compatible with current silicon manufacturing technology. With the enhancement of high electrons-holes mobility and reducing leakage current effects by SiGe finFET, the structure allows transistors to have higher performance with lower power consumption and apply to high-speed telecommunications and wireless applications.

1.3 Atomic Layer Deposition of Aluminum Oxide

In order to maintain Moore's law, high-k gate dielectrics such as aluminum oxide (Al_2O_3) and hafnium dioxide ($HfO_2$are replacing the conventional silicon dioxide (SiO_2) to increase the gate capacitance while maintaining low gate leakage current. Therefore, the desire of having high quality high-k oxide layer on substrate is important.

One and the best way to deposit high quality thin oxide layers on semiconductor surfaces is Atomic Layer Deposition (ALD) method. The ALD process is a modified chemical vapor deposition technique that uses different gaseous precursors to react on substrate's surface and form oxide layers of desired composition. Compare to other vapor deposition techniques, in ALD the gaseous precursors are introduced in the chamber in separate stages and fully saturate on the substrate surface before next precursor is introduced. Since the substrate surface is fully covered by material and limited to one monolayer in maximum, the growth of oxide layer is self-limiting and controls the film thickness precisely to the angstrom range. Additionally, the resulting film grown by ALD process is highly conformal due to the fully saturated surface coverage by single precursor in different dosing stages.

The Al_2O_3 deposition processes were designed using a Beneq TFS-200 ALD system. A diagram of the reactor setup is shown in Figure 1.1. During the deposition, a there is a continuous argon (Ar) carrier gas flow over the sample at all times. Precursor gases are pulsed into the continuous Ar flow and they react on the substrate as the stream passes over the substrate surface. During ALD processes, the reactor pressure was maintained at 1.7-2.1 torr.

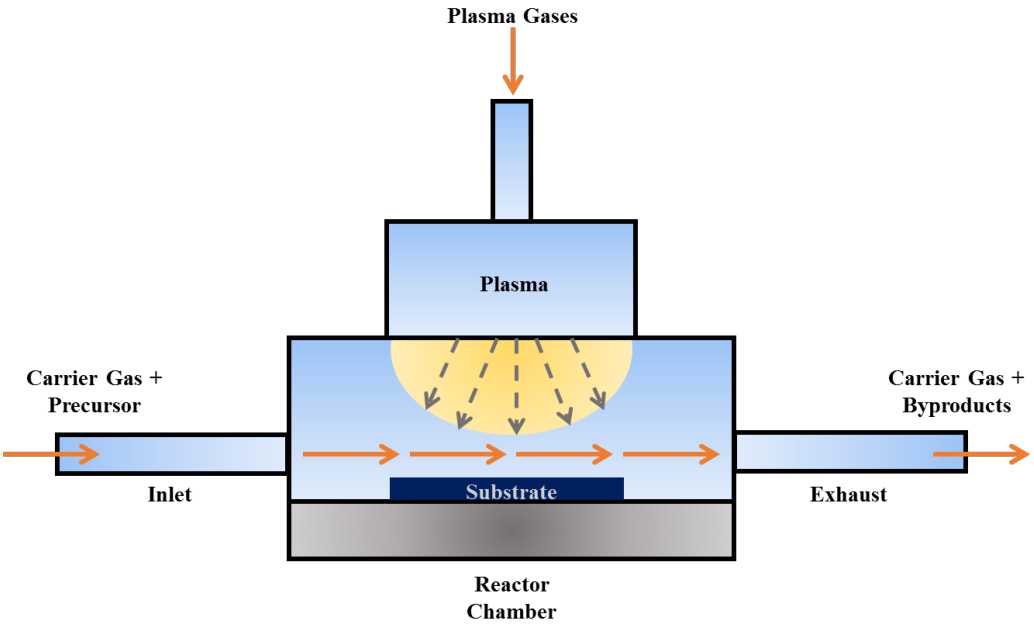

Figure 1.1 Schematic of Beneq TFS-200 ALD chamber. A constant stream of carrier gas flows across the sample at all times. Precursor gases are pulsed into this stream where they react on the substrate from right to left. A plasma source is attached from the top of the chamber allow for plasma cleaning or plasma enhanced ALD base on users need.

The chemical reaction in Al_2O_3 ALD processes is outlined here (see Figure 1.2), with metalorganic compound trimethylaluminum (TMA) and water to form Al_2O_3 dielectric film.

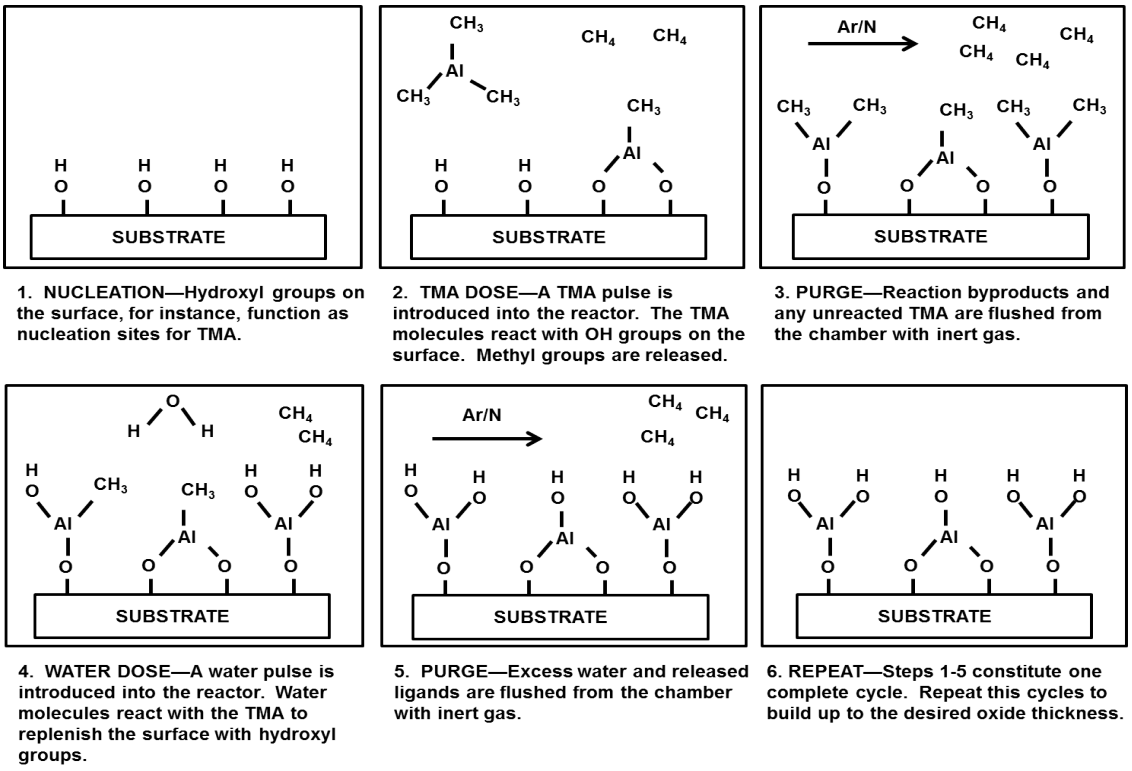

Figure 1.2 A cartoon illustrating the chemistry and deposition mechanics of the TMA and water ALD process. Steps 1-3 demonstrate TMA nucleation on the surface, TMA saturation, and puring. Steps 4-6 illustrate the water saturation dose, purge, and the final surface that has been re-hydroxylated.

The chemical reaction during Al_2O_3 ALD processes can be described into two half-reaction as:

$$Al(OH)_x^* + Al(CH_3)_3(g) \rightarrow AlO_x(CH_3)_{3-x}^* + xCH_4(g) \quad (1)$$

$$AlO_x(CH_3)_{3-x}^* + (3-x)H_2O(g) \rightarrow AlO_xAl(OH)_{3-x}^* + (3-x)CH_4 \quad (2)$$

where the asterisk denotes the surface species. In this thesis, Al_2O_3 ALD growth occurs during alternating exposure to TMA and H_2O.

In the Eq.1, It assumed that substrate surface be terminated by Al-OH bonds. The chemisorption of TMA occurs on active surface sites such as surface hydroxyl groups[20, 21, 24-26]. During the nucleation process, TMA undergoes dissociative chemisorption into dimethylaluminum (DMA) and a methyl ligand[20, 21, 24, 27, 28]. The dissociation occurs through the formation of an intermediate state in which the empty p-orbital on the Al in TMA interacts with the lone electron pairs present on the oxygen (O) atom in the surface hydroxyl group[29]. A methane molecule is then formed and released.

Eq.2 states the second half-reaction corresponding to the reaction caused by water pulse. During the water pulse, water molecules are introduced into the system where they dissociate on the methyl terminated surface[29]. They dissociate through the formation of the same intermediate species that forms during the TMA half-cycle[29]. The difference is the surface species is Al-CH_3 (due to methyl termination from TMA pulse) as opposed to Al-OH. This saturation dose subsequently leaves the surface hydroxyl terminated.

The combination of the two-half reactions effectively results in alternating surface terminations, which can be built up until the desired film thickness is achieved. Between

TMA/water or water/TMA processes, the inert gas purge is introduced to ensure that any unreacted TMA as well as byproducts are completely expelled from the chamber.

The overall reaction between TMA and water can be described as

$$Al(CH_3)_3(g) + \frac{3}{2}H_2O(g) \rightarrow \frac{1}{2}Al_2O_3(s) + 3CH_4(g). \quad (3)$$

where Eq. 3 describes the production of stoichiometric Al_2O_3 from TMA and water.

To conclude from the chemical reaction, processes parameters such as precursor pulse lengths, purge times, and gas flows must be tailored to accommodate particular thin film deposition and to get good ALD performance. In this thesis, the parameters shown in Table.1 were used for Al2O3 deposition.. The deposition rate determined by ellipsometry on a Si (100) monitor was 1.03 Å /cycle.

Table 1 Recipe of Al2O3 ALD parameter.

TMA pulse length (ms)	**TMA purge (s)**	**H_2O Pulse Length (ms)**	**H_2O Purge (s)**
200	6	50	6

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Chapter Two

Ex-Situ Wet Clean Optimization of Silicon Germanium Surfaces for Atomic Layer Deposition of Aluminum Oxide

2.1 Background

One key areas for improvement of SiGe MOSFET devices is the reduction of defects originating at the gate dielectric/channel interface. Improving insulated gate device performance by designing and optimizing the cleaning processes before gate dielectric growth. In this case, Al_2O_3 was chosen as the gate oxide since it has a large dielectric constant and large conduction band offset with respect to SiGe.

Controlling the state of the interface prior to oxide growth is crucial for realizing low interface trap densities. Controlling the state of the semiconductor surface often involves multi-step cleaning procedures involving both wet and dry methods. Several studies have demonstrated success in removing the native oxide on SiGe using wet chemical solutions[32-35]. Base on the ideas of Si and Ge surface passivation ideas, the thesis proposed HF plus sulfur clean to passive the SiGe surface.

In an effort to replicate the improvements seen in those studies, an Al_2O_3 ALD process as well as TMA pretreatment was developed as a part of this work. The surface cleaning methods in each experiment were characterized using capacitance-voltage (C-V) and current-voltage (I-V) spectroscopy on MOS capacitors (MOSCAP), as well as angle resolved x-ray photoelectron spectroscopy (AR-XPS) on 0.8nm thick Al2O3 over layers on cleaned SiGe surfaces.

2.2 SiGe MOSCAP Setup

Al_2O_3 films were deposited on 12nm thick p-type $Si_{0.7}Ge_{0.3}$ (100) with doping level of $2x10^{18}$ cm^{-3} grown epitaxially on p-type Si (100) via molecular beam epitaxy (MBE). The SiGe MOSCAP structure is shown in Figure 2.1. Al_2O_3/SiGe MOSCAPs were fabricated by 3nm ALD Al2O3 deposition, followed by 50nm nickel (Ni) gate deposition via thermal evaporation. The SiGe was grown on Si substrates, thus the contact to the SiGe can be made on the back surface. Direct current (DC) sputtering was employed to deposit 100-nm thick aluminum (Al) contacts uniformly on the substrate back side. In order to remove native oxide from the back surface before Al sputtering, the back surface was etched ex-situ by 1:10 HF solution plus in-situ by Ar plasma . After fabrication, MOSCAPs were annealed in forming gas (5% H_2, 95% N_2) at 250°C for 15min. To assess the quality of these films, MOSCAPs were characterized by C-V and I-V spectroscopy (Agilent B1500 Semiconductor Analyzer).

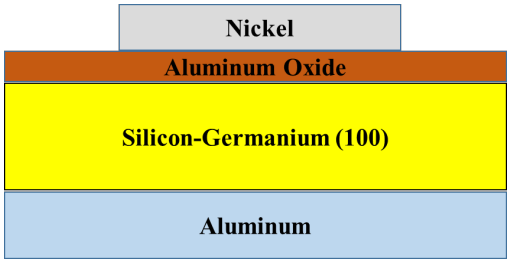

Figure 2.1 Schematic of SiGe MOSCAP structure.

C-V spectroscopy was carried out on the MOSCAPs with AC modulation amplitude of 30mV, in the gate bias range of -2 to 2V, at multiple frequencies from 2 KHz to 1 MHz. To determine the composition of $Al_2O_3/Si_{0.7}Ge_{0.3}$ (100) interfaces as a

function of surface treatment, AR-XPS as well as grazing angle XPS were performed on SiGe samples after 0.8 and 1.6 nm of Al_2O_3 deposition. AR-XPS measurements were performed by a VG Theta Probe system using an Al-Kα excitation source (1486.7 eV). Si2p, Ge2p, Ge3d, Al2p and O1s spectra were obtained at various take off angles starting from 26.75° To 79.25° with 7.5° steps. Grazing angle XPS was performed using a monochromatic XM 1000 MkII/SPHERA (by Omicron Nanotechnology) XPS system with an Al-Kα source (E = 1486.7 eV). For all measurements, a take-off angle of 30° from the sample surface was used.

The purpose of the annealing process after MOSCAP fabrication is to reduce the traps between Al2O3/SiGe interfaces. The gate metal, Ni, is a catalytic material that allows H_2 pass through the metal and dissociate into atomic hydrogen to remove the traps between device interfaces. In Figure 2.2, the C-V results for forming gas anneal at different temperatures are shown where 250°C anneal has the best capacitance quality. Therefore, for all the samples shown in the future sections forming gas annealed for 15 minutes at 250°C was performed.

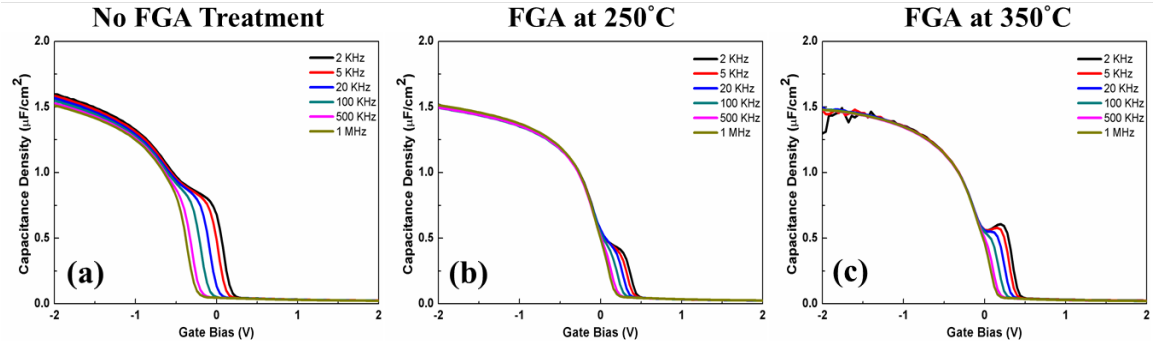

Figure 2.2 C-V curves for SiGe samples with or without forming gas anneal (FGA) after MOSCAP fabrication. For samples (b) and (c), both were FGA for 15 minutes.

2.3 Wet Clean Experiment Setup

In total, two sets of wet clean experiments were performed to characterize the surface passivation quality on SiGe surfaces. The first experiment examined the hydrogen fluoride/de-ionized water (HF/DI water) cyclic clean while the second experiment was focused on HF/DI water cyclic clean followed by ammonium sulfide ($(NH_4)_2S$) dip for 30min. Both cleaning methods are compared with the results for standard organic clean recipe (with no native oxide removal) composed of consecutive rinse by Acetone, Isopropanol and DI water.

A. Hydrogen Fluoride Clean

After standard organic clean, samples were dipped in 2% HF for 1 minute, DI water for 1 minute for three 2 cycles followed by final HF dip. The HF solution removes the native oxide and other impurities on substrate surface; on the other hand, DI water can dissolve germanium oxide (GeO_x) and remove the oxide from substrate surface. After wet clean processes, samples were loaded into the ALD chamber within 2 minutes.

B. Hydrogen Fluoride plus Ammonium Sulfide Clean

Ge is known for out diffusion into the gate oxide and reduced the device reliability. Therefore, this thesis introduced the idea of sulfur passivation on Ge to passivate the defect sites on Ge atoms by forming Ge-S bonds at the surface. Such passivation was achieved by wet chemical treatment using 28-30% $(NH_4)_2S$ solution. Combining the standard HF/DI water cyclic for removing most of the SiO_x on SiGe surface, the Table 2.1 shows samples with different wet clean recipe that present the discussion in chapter 2.

Table 2.1 HF plus $(NH_4)_2S$ clean recipes optimization

Sample	Organic clean	2%HF/DI water cycles	$(NH_4)_2S$ dipping time (minutes)
1	V	-	-
2	V	3	-
3	V	3	15
4	V	3	30
5	V	3	60

2.3 Results and Discussion

To remove the native oxide, after organic clean processes, SiGe surfaces were cleaned with HF/DI water cyclic clean. Oxide removal can be followed by sulfur passivation by exposure to $(NH_4)_2S$. Figure 2.3 shows the C-V curves at 2KHz to 1MHz for the sample 1-3 with 3nm of Al_2O_3 at 120°C. Base on the C-V results, both HF/DI water and HF/DI water plus $(NH_4)_2S$ surface cleaning treatments showed similar levels of frequency dispersion in accumulation and near the flat band. The sample with organic clean had lower capacitance density showing that the capacitance is mixed with gate dielectric and native oxide.

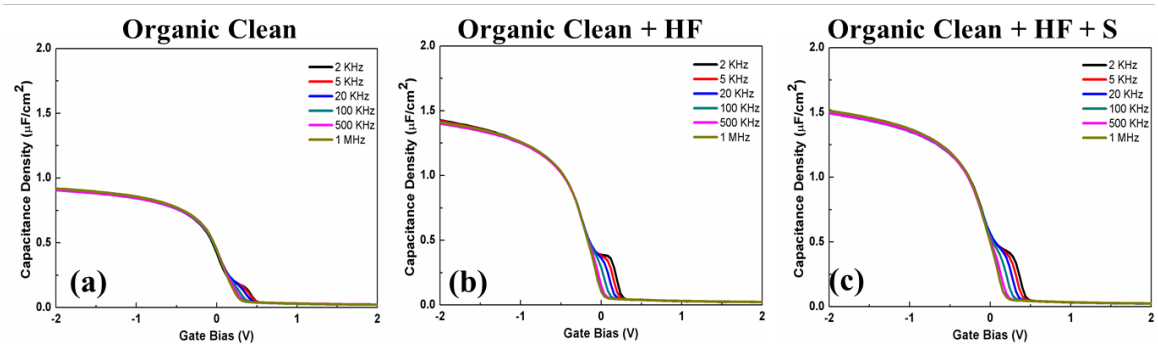

Figure 2.3 C-V curves for SiGe samples with different wet clean treatment

The C-V profiles for samples 3-5 are shown in Figure 2.4. The C-V plots indicate that sample 4 with 30 minutes of $(NH_4)_2S$ dipping is the best recipe for sulfur treatment. Although sample 3 had the same maximum capacitance density with sample 4 in accumulation part, 15 minutes sulfur dipping have wider border traps within accumulation and nearby flat band. The wider border traps may be identified that the sample is not sufficient to fully saturate the surface. For sample 6, the maximum capacitance density is smaller that two other sulfur dipping samples. Although it had the

smallest D_{it} bump, the ratio between maximum capacitance density and D_{it} height is consistent with sample 3 and sample 4. The low levels of dispersion in both accumulation and depletion are indicative of low levels of near-interface oxide traps as well as a low density of interfacial traps, respectively[36, 37].

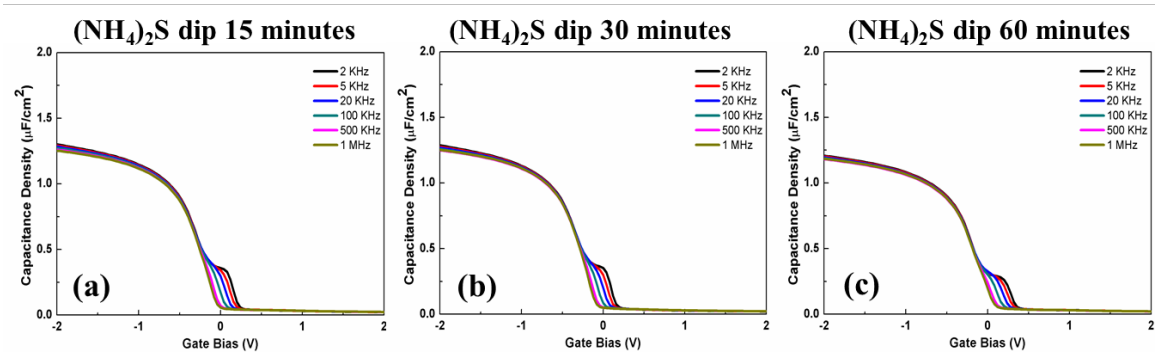

Figure 2.4 C-V curves for SiGe samples with different $(NH_4)_2S$ dipping time

2.4 Conclusions

In sum, it has been shown that both HF/DI cyclic clean and HF/DI water plus $(NH_4)_2S$ dipping wet surface clean methods did provide a significant improvement in film or interface quality over samples compare to organic surface clean only sample. Organic clean recipe only removed the organic solvents on surfaces rather than etch the surfaces, so it is necessary to introduce other cleaning methods to remove native oxide.

Proper cleaning of the substrate is crucial to any successful surface modification. The HF/DI water cleaning method is modified from the Si cleaning method. HF mainly remove the SiO_x, especially SiO_2, on the SiGe surface. The chemical reaction of hydrogen fluoride clean proceeds as follows:

$$SiO_2 + 6HF \rightarrow H_2(SiF_6) + 2H_2O \quad (4)$$

$$SiO_2 + 4HF \rightarrow SiF_4(g) + 2H_2O \quad (5)$$

The reactions can remove the SiO_2 from substrates surface to form gaseous or water-soluble silicon fluorides. However, HF single step wet clean cannot completely apply on the native oxide removal processes on SiGe substrate since GeO_x offers no protection and it might roughen the SiGe surfaces. Therefore, DI water dip follow by HF dipping become a solution since GeO_x is water-soluble.

Repeated etching cycles in aqueous acid etchants and water can remove most of native oxide on SiGe surface, but still leave open the possibility for further surface oxidation during transporting samples to ALD processes. To protect the SiGe surface, $(NH_4)_2S$ dip not only provides protection to the surface by forming Ge-S on the substrate surface and preventing its reaction with oxidants such as H2O and O2.

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Chapter Three

Sulfur Passivation of The Interface Between Aluminum Oxide and Silicon Germanium

3.1 Abstract

Silicon-Germanium (SiGe) has shown a great promise for future CMOS technology, as the FinFET channel material, by combining the high hole and electron mobility with the ability to have both tensile and compressive strain by fabrication of alloys of higher and lower Ge content. However, the nature and passivation strategy of the interfaces between high-k dielectrics and SiGe still needs to be understood. In this study, Al_2O_3 high-k dielectric has been deposited on $Si_{0.7}Ge_{0.3}$ (100) substrates by atomic layer deposition (ALD). Prior to oxide deposition, SiGe surfaces were treated by wet clean processes that include exposure to HF and $(NH_4)_2S$. Interfaces compositions were determined by angle resolved x-ray photoelectron spectroscopy (AR-XPS). Electrical properties of the interfaces were examined by fabrication and characterization of metal-oxide-semiconductor capacitors (MOSCAPs). $(NH_4)_2S$ treatment suppressed GeOx formation and resulted in formation of only SiO_x at the Al_2O_3-SiGe interface, consistent with direct Al-O-Si bonding between the Al_2O_3 and SiGe surfaces. After $(NH_4)_2S$ passivation, significantly smaller GeO_2 was detected within the first few layers of oxide adjacent to the interface. In addition, $(NH_4)_2S$ treatment led lower leakage current and longer air stability of the cleaned surfaces prior to ALD, maintaining the same level of equivalent oxide thickness (EOT) and flat band voltage.

3.2 Introduction

As one of the promising material for the extension of the future CMOS technology, SiGe considers its high mobility particularly as a result of strain-induced effects. $Si_{1-x}Ge_x$ attracts semiconductor foundries attention because of offering higher low-field holes motilities than Si and can be more easily integrated into a Si CMOS process flow.

To improve the performance, it is necessary to have a low-defect high-k oxide/SiGe interface that ensures high channel mobility with minimal carrier scattering and trapping. Unlike Si, SiGe native oxide, generally denoted by $SiGeO_x$, has low interface quality and stability due to the presence of the GeO_x. Ge is known for out diffusion into the gate oxide and reducing the device reliability. In addition, to minimize the punch-through effect in scaling the channel length, thinner oxides with larger permittivities are essential. Therefore, instead of thermal oxide growth, it is necessary to employ ALD processes for gate oxide deposition in SiGe MOS devices. In order to passivate the defects at the oxide/SiGe interface, surface clean and interface passivation is very crucial for device performance. High-k/semiconductor interface passivation has been extensively studied for Ge and III-V compounds such as GaAs, InGaAs. Previously, S termination was used as a passivation technique for high-k / III-V and IV interfaces/Give some references of S passivation in GaAs, InGaAs, GaN and Ge.

This study determines the effect of $(NH_4)_2S$ clean on Al_2O_3 bulk and Al_2O_3/SiGe interface quality in terms of oxide leakage and interface and near-interface (border) trap density. Effect of ALD temperature with and without Sulfur passivation has been studied as well by performing Al_2O_3 ALD at 120°C and 300°C. Electrical properties of the

$Al_2O_3/Si_{0.7}Ge_{0.3}$ (100) interfaces were characterized by capacitance-voltage (C-V) and current-voltage (I-V) measurements on MOS capacitors. Chemical compositions of the oxide/SiGe interface for different ALD temperature in the presence or absence of the $(NH_4)_2S$ clean were determined by angle resolved x-ray photoelectron spectroscopy (AR-XPS). Complete removal of GeO_x from the Al_2O_3/SiGe is successfully demonstrated improving the reliability of Al_2O_3/SiGe gate stacks in future SiGe devices. Al_2O_3 ALD at 120°C combined with by $(NH_4)_2S$ clean resulted in low density of interface and border traps.

3.3 Experimental Details

A 12nm thick p-type $Si_{0.7}Ge_{0.3}$ (100) with doping level of $2x10^{18}$ cm^{-3} was grown epitaxially on p-type Si(100) by molecular beam epitaxy (MBE). Al_2O_3/SiGe MOSCAPs were fabricated by ALD Al_2O_3 deposition, followed by 50nm Ni gate deposition via thermal evaporation and finished by 100nm Al back contact deposition using DC sputtering.

Prior to atomic layer deposition, native oxide was removed by cyclic HF clean using 2% HF solution and DI water. For ex-situ sulfur clean, samples were dipped for 30min in 25% $(NH_4)_2S$ solution at room temperature.

To deposit Al_2O_3 by ALD, samples were transferred to the ALD chamber with minimal exposure to air. Thin Al_2O_3 ALD was performed at 120 °C in a Beneq TFS-200 continuous flow reactor, with Ar as the carrier gas, where 30 consecutive cycle of 200 ms of Trimethylaluminum (TMA) and 50 ms of H_2O were dosed on the sample surface by pulse valves. After each of TMA and H_2O pulses a 6-s purge was applied. The chamber base pressure during the ALD process was 1.7 torr. Deposition rate determined by Elliposometry on a Si(100) monitor was 1.03 A/cycle. Therefore, the oxide thickness is estimated as 3.1nm. After fabrication, MOSCAPs were annealed in forming gas (5% H_2, 95% N_2) at 250 °C for 15 minutes.

C-V spectroscopy was carried out on the MOSCAPs with AC modulation amplitude of 30 mV, in the gate bias range of -2V to +2V, at multiple frequencies from 2KHz to 1MHz.

To determine the composition of $Al_2O_3/Si_{0.7}Ge_{0.3}$(001) interfaces as a function of surface treatment, angle resolved x-ray photoelectron spectroscopy (AR-XPS) as well as

grazing angle XPS were performed on SiGe samples after 0.8 and 1.6 nm of Al_2O_3 deposition. AR-XPS measurements were performed by a VG Theta Probe system using an Al-Kα excitation source (1486.7 eV). Si2p, Ge2p, Ge3d, Al2p and O1s spectra were obtained at various take off angles starting from 26.75° To 79.25° with 7.5° steps. Grazing angle XPS was performed using a monochromatic XM 1000 MkII/SPHERA (by Omicron Nanotechnology) XPS system with an Al-Kα source (E = 1486.7 eV). For all measurements, a take-off angle of 30° from the sample surface was used.

3.4 Results and Discussion

For more reliable devices with thin gate oxides it is necessary to prepare a clean SiGe surface with minimum amount of native oxide. To remove the native oxide, SiGe surfaces were cleaned with HF and DI water cyclic clean. Oxide removal can be followed by sulfur passivation by exposure to $(NH_4)_2S$. Figure 3.1 shows the C-V curves at 2KHz to 1MHz for the samples with HF only and HF+$(NH_4)_2S$ treatment with Al2O3 at 120°C and 300°C. At lower ALD temperatures, both cleaned surfaces showed similar levels of frequency dispersion in accumulation and near the flat band. However, for HF-cleaned surfaces at higher ALD temperatures, larger frequency dispersion in accumulation was observed consistent with higher oxide leakage knowing that contact series resistant is absent for this sample. Figure 3.2 shows the D_{it} vs. E_V-E for surfaces treated by HF and HF plus $(NH_4)_2S$ with different ALD temperature processes. Both the clean recipes resulted in similar D_{it}-E distribution. Regardless of surface treatment recipe, lower ALD temperature resulted in smaller interface trap density. Therefore, in order to attain a high quality interface with reasonably low density traps at or near the interface, it is necessary to deposit the oxide at lower temperatures.

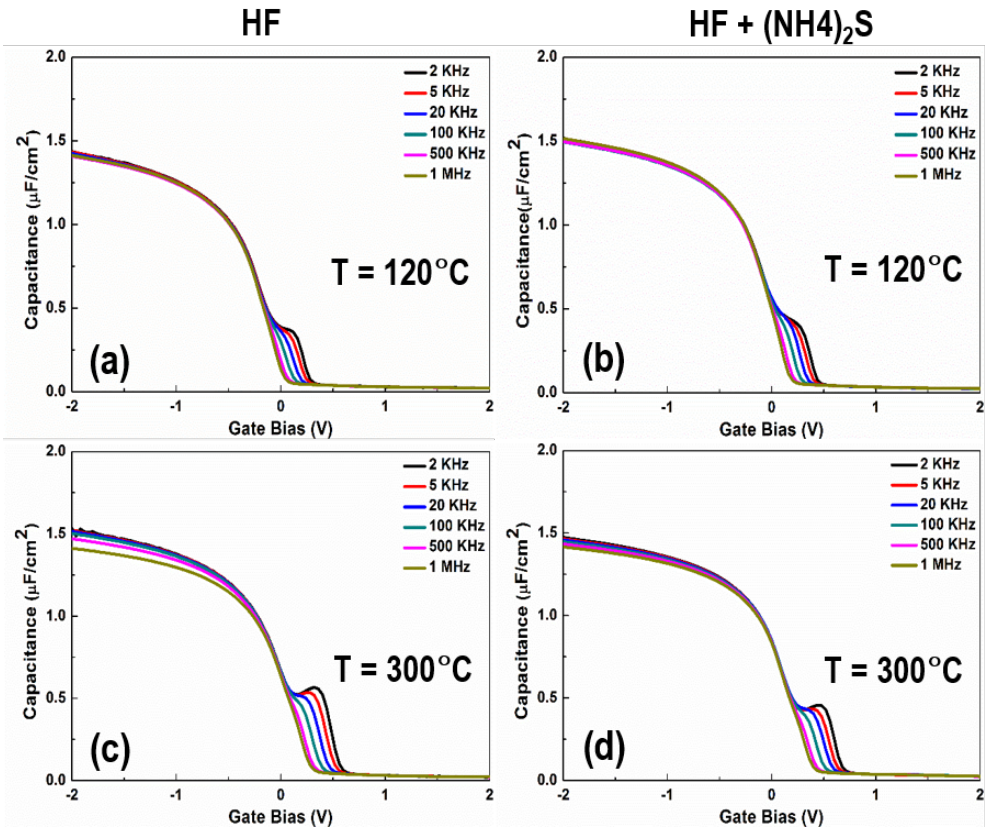
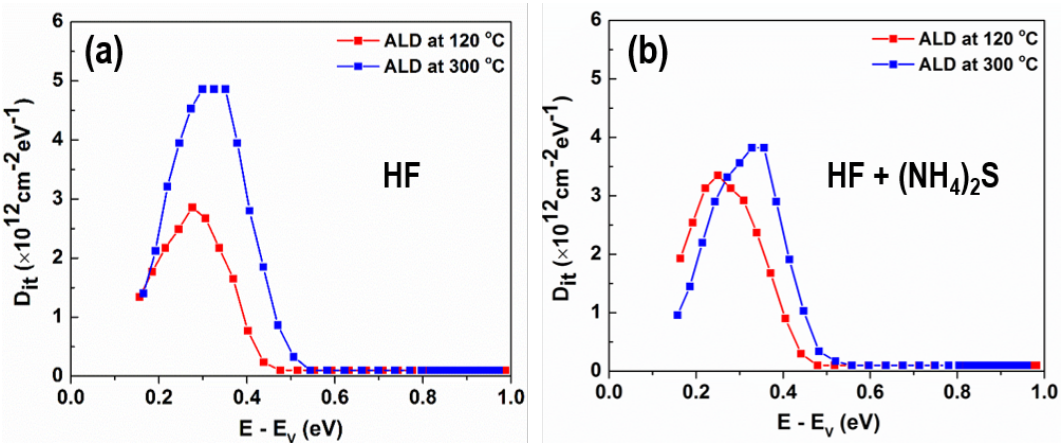


Figure 3.1 C-V curves for SiGe sample HF cyclic clean and HF+S clean at 120 and 300



C showing the behavior does not change significantly as a function of temperature

Figure 3.2 Dit vs. Ev-E for 120C and 300C ALD with HF and HF+S

To quantitatively compare the electrical quality of Al_2O_3/SiGe interfaces, equivalent oxide thickness (EOT), maximum density of interface traps (D_{it}), density of border traps (N_{bt}) and flat band voltage (V_{FB}) were extracted for the curves shown in Table 3.1. Compared to the surface with native oxide, both cleaning methods led to small EOT (2.3-2.4 nm) that is suitable for device scaling. $(NH_4)_2S$ treatment caused slight reduction in EOT to 2.28nm while caused slightly higher density of border traps. It only applies to lower ALD temperature and at 200°C or 300°C, similar EOT levels were obtained regardless of the surface preparation prior to oxide deposition. Lower interface trap and border trap density as well as smaller EOT for oxides deposited at 120°C emphasizes the importance of low temperature ALD on good performance of the Al_2O_3/SiGe interface.

Table 3.1 EOT, D_{it}, N_{bt}, V_{FB} as functions of ALD temperature with three wet clean methods

	No clean	*HF*		*HF + $(NH_4)_2S$*	
Parameter / Temperature	**120 °C**	**120 °C**	**300 °C**	**120 °C**	**300 °C**
EOT (nm)	3.49	2.23	2.13	2.09	2.23
N_{bt} (x 10^{19} cm^{-3}.eV)	7.0	6.2	10.0	5.8	11.0
V_{FB} (V)	0.10	-0.05	0.14	0.10	0.35

To quantitatively compare the electrical quality of Al_2O_3/SiGe interfaces, equivalent oxide thickness (EOT), maximum density of interface traps (D_{it}), density of border traps To quantitatively compare the electrical quality of Al_2O_3/SiGe interfaces, equivalent oxide thickness (EOT), maximum density of interface traps (D_{it}), density of border traps To characterize the insulating properties of the Al_2O_3 gate oxides, Ig-Vg measurements were carried out on the samples with various surface cleanings and ALD temperatures. Figure 3.3 shows the Ig-Vg curves for HF treated surfaces with 3nm of Al_2O_3. Raising the ALD temperature for HF-treated sample from 120°C to 300°C resulted in an order of magnitude increase in the maximum leakage current (at Vg = -2V). In contrast, leakage current is independent of ALD temperature for sulfur-passivation surfaces. Additionally, for 120°C ALD, the maximum leakage current at Vg = -2V is an order magnitude smaller than that of HF-treated surface. This is consistent with better insulating properties and higher nucleation of the Al_2O_3 on S-passivation SiGe (100) surfaces.

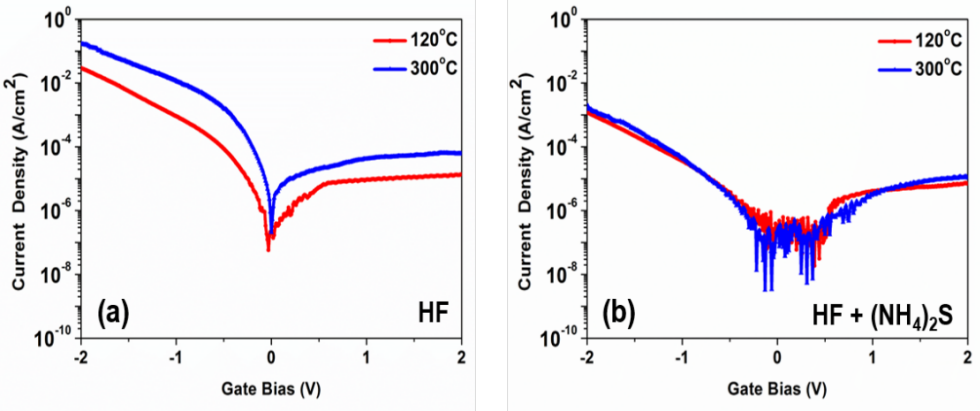


Figure 3.3 Leakage current for sample at 120C and 300 C for both HF and HF+S

In addition to stability of surface against in-situ oxidation during the ALD process, it is favorable to have surfaces that are more stable in air. Longer stability of the clean surface in ambient extends the queue time in the manufacturing of relevant electronic devices. To determine the air stability H- and S-passivation surfaces were exposed to air for 30 minutes and 60 minutes prior to insertion into the ALD reactor and subsequent Al_2O_3 deposition. Figure 3.4 displays the C-V behavior the Al_2O_3/SiGe MOSCAPs fabricated with air-exposed surfaces. In terms of frequency dispersion of the curves, both samples showed very small changes as a function of exposure time. However, S-passivation resulted in slightly lower EOT and high D_{it} capacitance than HF-clean.

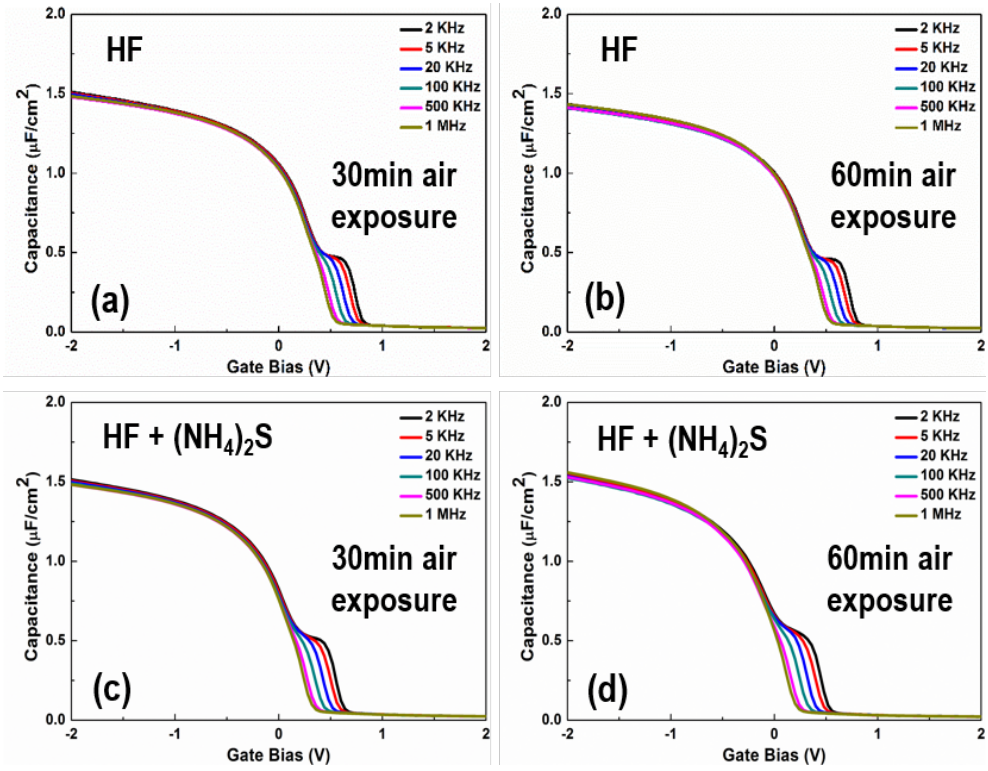


Figure 3.4 Queue time measurements of S-cleaned surface vs. HF-cleaned surface after 30, 60min exposures – 3rd column added to compare Dit vs. Ev-E

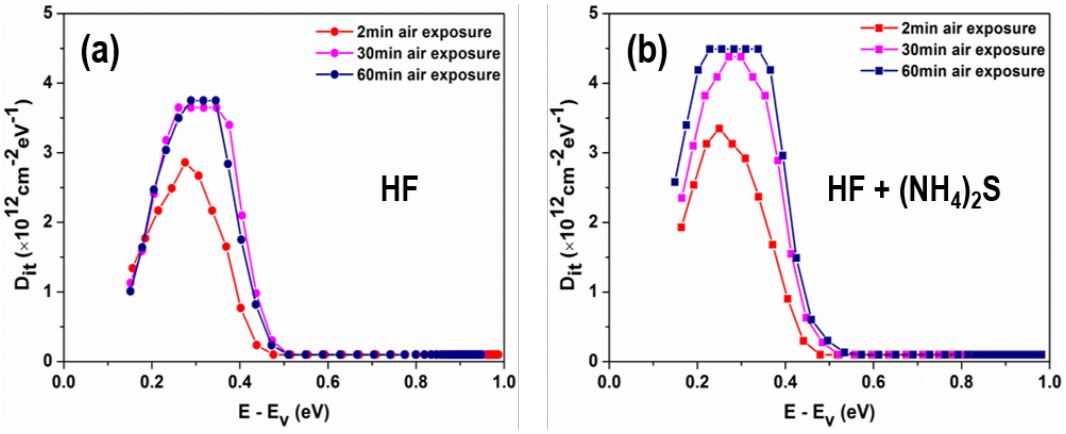


Figure 3.5 Dit vs. Ev-E for 120C and 300C ALD with HF and HF+S

Equivalent oxide thickness (EOT), maximum density of interface traps (D_{it}), density of border traps (N_{bt}) and flat band voltage (V_{FB}) as functions of air exposure were listed in Table 3.2. For HF-cleaned samples, V_{FB} shifted for 480mV after exposure to air. This can have an adverse effect in the device performance by significant shifts in the threshold voltage of the resulting devices [REF]. In contrast, after exposure to air, V_{FB} for S-passivated interfaces were maintained in a narrower range (up to 130 mV) variation. This makes the S passivation the more favorable process for the purpose of extending the queue time for the SiGe devices before gate oxide ALD deposition.

Table 3.2 EOT, Dit, Nbt, Vfb as functions of air exposure

	HF			*HF + $(NH_4)_2S$*		
Parameter / Air Exposure	**2min**	**30min**	**60min**	**2min**	**30min**	**60min**
EOT (nm)	2.23	2.09	2.20	2.09	2.10	2.00
N_{bt} (x 10^{19} cm^{-3}.eV)	6.2	5.5	6.2	5.8	6.5	6.6
V_{FB} (V)	-0.05	0.40	0.40	0.10	0.22	0.12

Gate leakage vs. gate voltage has also been measured as a function of air exposure (Figure 3.5). Similar to S-passivated surfaces with various ALD temperatures, air exposed S-passivated surfaces exhibit lower leakage current. In addition, leakage current in accumulation is almost independent of the length of the air exposure as opposed to H-passivated surfaces.

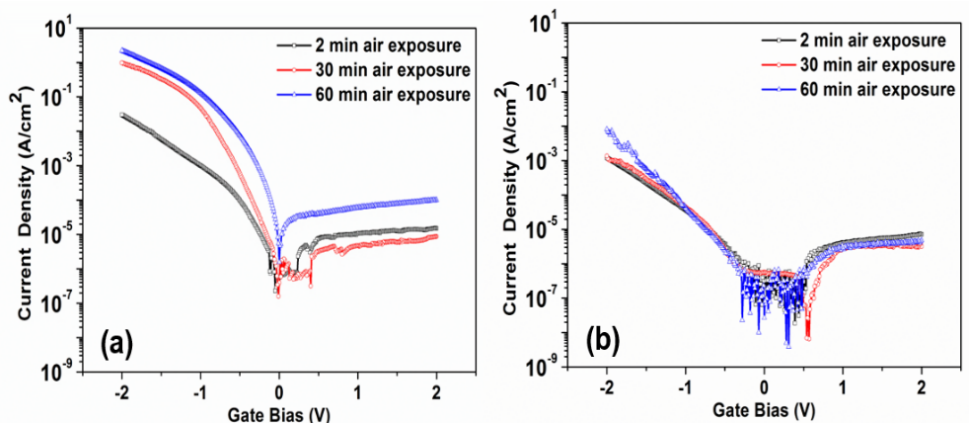


Figure 3.6 Leakage current for 30 and 60min exposure times compared with references with almost no exposure

To correlate the electrical characterization results with interface chemistry, angle-resolved XPS was performed on the samples after HF and HF + (NH4)2S treatment and deposition of only 0.8-0.9nm of Al_2O_3. This thin oxide makes it possible to detect photoelectrons from the oxide/SiGe interface without significant attenuation. The interfacial chemical bonding at the SiGe-Al_2O_3 interface has been determined by monitoring the Si2p, Ge3d and Ge2p XPS peaks. Ge2p electrons specifically have lower kinetic energy that makes them more surface sensitive in case of bare SiGe surface.

However, in this case, a large portion of this single might be correlated with the thin oxide composition rather than the Al_2O_3/SiGe interface. Although 20 cycles of TMA pre-pulse in combination with ex-situ surface clean using HF (with and without sulfur) was used to remove the surface oxide, for normal angles (close to 30 degree), a large amount SiO_x can be observed. Note that there is no peak in the energy range of 103-105 eV confirming the absence of SiO_2 at the interface. However, a significant amount of Si-O bonding has been probed. In contrast to Si2p, Ge2p peaks (Figure 6c and 6d) showed the difference between the S and H passivation of SiGe surface. S-passivated interfaces showed significantly smaller formation of Ge-O bonding at the interface, limiting the oxide-SiGe bonding to Si-O-Al only. Ge2p signal (Figure 6e and f) is showing the presence of GeO2 as well as GeOx most probably within the first few monolayers of the oxide. Similar to Ge3d peaks, a larger ratio of Ge seen in Ge2p peaks is in the form of GeO2 for H-passivation surfaces. This peak completely disappears at very grazing angle on S-passivation sample. In contrary, GeO_2 becomes the main peak at grazinf angle of 79.25 for H-passivation sample.

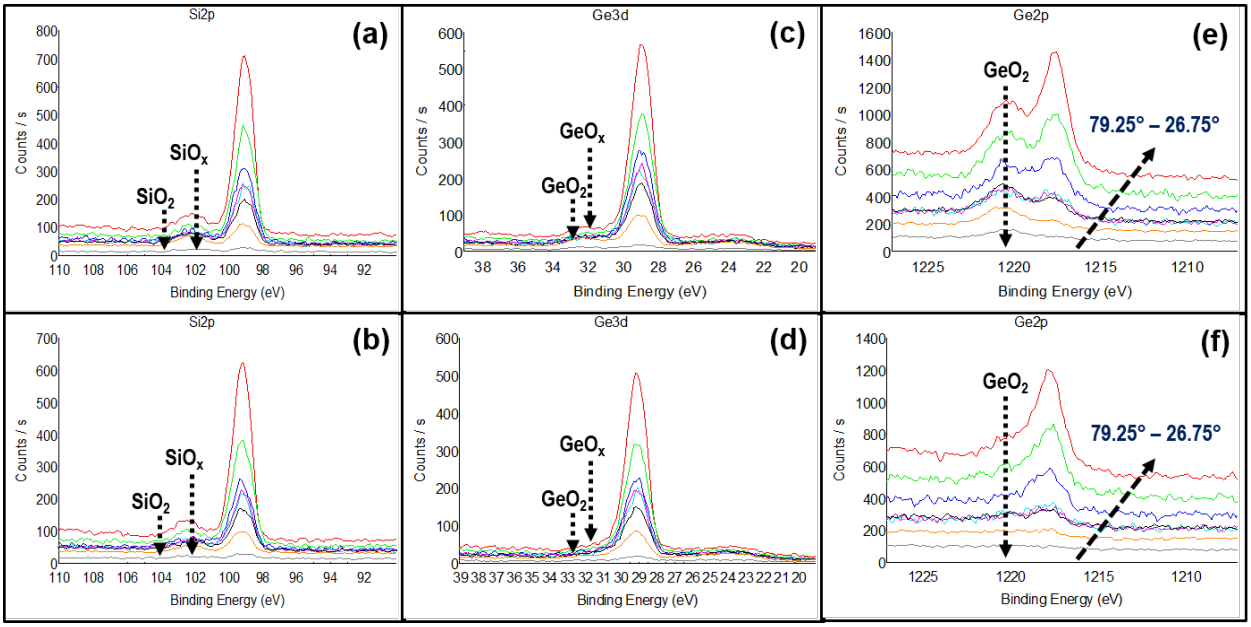


Figure 3.7 AR-XPS data showing the absence of GeO_x and smaller GeO_2 on the sample with HF+S clean compared with cyclic HF clean (No FGA). Ge incorporation is a well-known phenomenon in Ge devices. Ge out-diffusion has been suppressed by various techniques. It can lead to low reliability and high leakage in the gate oxides

To simulate the forming gas anneal condition while avoiding the Ni deposition and resulting metal contamination during the XPS measurements, a set of experiments were carried out using XPS at 30 degree take off angle (more normal) before and after UHV anneal and dosing the surface with atomic hydrogen generated by a thermal cracking H source. Figure 7 displays the Si2p, Ge3d and Ge2p peaks before and after each of the processing steps including 0.5 nm oxide deposition, UHV anneal at 300 C and atomic H dosing on the sample at 330 C. Combination of atomic H with anneal resulted in complete transfer of oxygen from Ge to Si ensuring the direct bonding between the Si atoms and Al_2O_3 in the form of Al-O-Si.

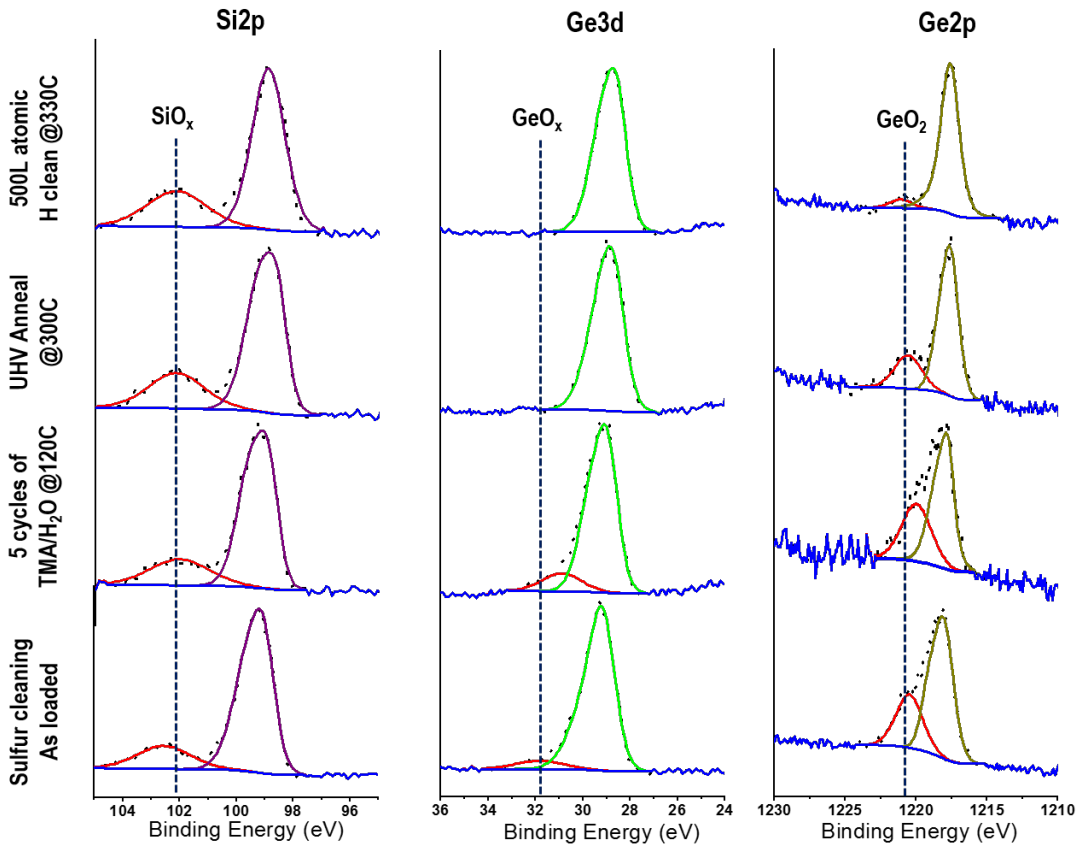


Figure 3.8 XPS results on the sample after 5 cycles of Al2O3 on SiGe showing how atomic hydrogen can remove the GeOx from the interface and leave the surface bonds as Al-O-Si bonds.

S passivation on Ge and most of the III-V surfaces such as GaAs and GaN results in formation of direct bonding between the surface atoms and S (Ge-S bonds, etc). To determine bonding condition and S surface coverage, S2p peaks were measured by near normal angle XPS (Figure 3.8). Regardless of the processing, there is a very small amount of residual S on the sample surface that results in less than 5% coverage. Therefore, S atoms should only form –S bonds at certain defect sites and step edges. These defect sites could be the favorable locations for interfacial GeO_x to form. Therefore,

S passivation only prevents the GeO_x formation and out diffusion into Al_2O_3, reducing the gate oxide leakage and improve the interface properties.

In addition to chemical bonding at the interface, it is necessary to understand how each of the S and H passivation steps can affect the nucleation density of Al_2O_3 on SiGe surfaces. Figure 8b shows the Al2p peaks on H- and S- passivated surfaces after 0.8nm of Al2O3 deposition at 120°C, 200°C and 300°C. These peaks were measured by AR-XPS at the take-off angle of 26.75 degrees. S-passivation resulted in at least twice larger Al2p intensity consistent with better nucleation density of Al_2O_3 on the S-passivated surfaces. This is consistent with smaller pinhole density on S-passivated MOSCAPs with an order of magnitude smaller leakage current.

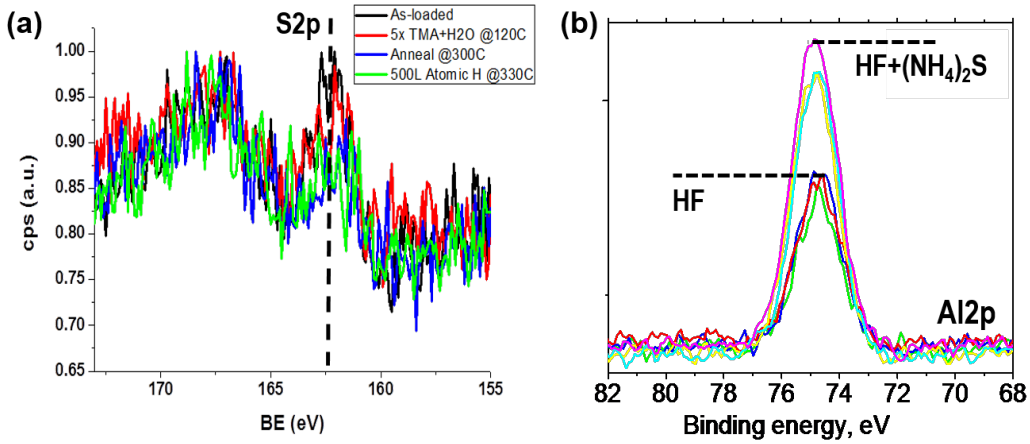


Figure 3.9 S2p peaks for various processing steps on the sample surface confirming the very small amount of S residue on the sample that could passivate defects only (could be related to Ge since we have only 30% Ge). Add the Al2s peak from AR-XPS measurements showing the higher nucleation density at all temperatures for HF+S cleaned sample

3.5 Conclusions

In conclusion, it has been shown that low temperature ALD can result in higher interface quality and lower gate oxide leakage in the absence of S-passivation. The dependence of oxide and Al_2O_3/SiGe on the air exposure has strongly been reduced by the use of S-passivation. Specifically, for an hour of air exposure, V_{FB} has been maintained in the same range as the sample with no air exposure, showing the capability of this passivation in extending the device fabrication queue time. In addition, S passivation resulted in large removal of Ge-O bonds at the Al_2O_3-SiGe interface, leading to Al-O-Si direct bonding. Moreover, S-passivation led to higher nucleation density consistent with an order of magnitude smaller leakage current compared to H-passivated only samples. Based on the very small sulfur coverage after H anneal, it has been hypothesized that S only passivated certain defect sites on the surface i.e step edges, leaving the other interfacial defects such dangling bonds and Si-Al and Ge-Al bonds intact,

3.6 Acknowledgements

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