# A Hybrid Life Cycle Inventory of Nano-Scale Semiconductor Manufacturing

NIKHIL KRISHNAN,*,† SARAH BOYD,‡ AJAY SOMANI,§ SEBASTIEN RAOUX,|| DANIEL CLARK,⊥ AND DAVID DORNFELD‡

*Columbia University, New York, NY, University of California, Berkeley, CA, Massachusetts Institute of Technology, Cambridge, MA, Transcarbon International, San Francisco CA, and Applied Materials Inc., Santa Clara, CA*

*Received May 18, 2007. Revised manuscript received January 25, 2008. Accepted January 29, 2008.*

The manufacturing of modern semiconductor devices involves a complex set of nanoscale fabrication processes that are energy and resource intensive, and generate significant waste. It is important to understand and reduce the environmental impacts of semiconductor manufacturing because these devices are ubiquitous components in electronics. Furthermore, the fabrication processes used in the semiconductor industry are finding increasing application in other products, such as microelectromechanical systems (MEMS), flat panel displays, and photovoltaics. In this work we develop a library of typical gate-to-gate materials and energy requirements, as well as emissions associated with a complete set of fabrication process models used in manufacturing a modern microprocessor. In addition, we evaluate upstream energy requirements associated with chemicals and materials using both existing process life cycle assessment (LCA) databases and an economic input-output (EIO) model. The result is a comprehensive data set and methodology that may be used to estimate and improve the environmental performance of a broad range of electronics and other emerging applications that involve nano and micro fabrication.

## 1. Introduction

Semiconductor devices are ubiquitous components of modern electronics. Device fabrication is complex, involving numerous process steps that use a broad set of specialized equipment in a tightly controlled environment. Over the past few years, life cycle assessment (LCA) has been increasingly used to assess the environmental implications of semiconductor fabrication. A 2002 study highlighted the importance of assessing manufacturing and upstream environmental impacts associated with semiconductor devices (*1*). Other studies have worked toward developing within-facility (gate-to-gate) semiconductor manufacturing inventory data (*2*–*7*). Some of these studies present data from the fab as a black-box (*2, 3*), whereas Smati and collaborators present a "bottom-up" gate-to-gate inventory analysis with a focus on gaseous emissions (*4*) and Murphy and collaborators develop a methodology to parametrize semiconductor gate-to-gate inventories with a focus on material and electricity inputs (*5*).

However, there are three key gaps in previous work that this analysis addresses: (i) Given rapid rates of technological change and an emerging set of nanofabrication applications there is a need for an analysis methodology and a library of manufacturing data that is transparent and structured to allow for modifications; (ii) Previous work has typically focused on fabrication process-related material and energy inputs. There is a need to both quantify unit process emissions and the impacts of auxiliary equipment at the facility scale; (iii) There is a need for streamlined methodologies to assess upstream impacts of manufacturing chemicals, materials and equipment infrastructure.

In this work, we first develop a bottom-up, within-fab life cycle inventory (LCI) for semiconductor fabrication (Figure 1). We follow an approach similar to Murphy (*5*), but also base our analysis on equipment sets (*7*) in order to estimate configurations and materials/energy flows related to auxiliary equipment (pumps, chillers, heat exchangers, abatement systems, etc.) required in the subfab (typically below the cleanroom floor), or at the facilities scale. Additionally, we significantly add to Murphy's work by developing and presenting a detailed library of material and energy process models (both input and emissions) for a complete set of manufacturing processes. The primary contribution of our work is a detailed and transparent bottom-up analysis of within-fab inventories (both inputs and emissions) of a broad set of fabrication processes used to manufacture a modern microprocessor.

Second, we utilize a hybrid approach, an emerging methodology in LCA, to perform a streamlined evaluation of the impacts of upstream chemicals and equipment (Figure 1). Hybrid approaches combine conventional process-based LCA (*8*) with input−output (IO) LCA strategies (*9*) (Figure 1). A conventional process-model based life cycle study of upstream chemical/material impacts is problematic because of the significant data gaps associated with specialty chemicals. Our work represents the first attempt to apply a hybrid approach to a complete set of semiconductor manufacturing processes. Such an approach combines the strengths of process LCA (assessment of impacts associated with specific products and technologies) and IO LCA (representation of the complete supply chain), providing a more inclusive model of upstream impacts (*10*). At this point we restrict our analysis of upstream environmental impacts to primary energy requirements.

## 2. Methodology and Scope

The manufacturing of a modern semiconductor device may involve hundreds of different process steps. We focus here on high performance complementary metal-oxide semiconductor (CMOS) logic devices (microprocessors), although many fabrication steps are similar for different device types or in different applications that use nano or microfabrication processes. Integrated circuits are manufactured on high-purity silicon substrates (wafers), using ultrapure chemicals and materials in clean-rooms. Each finished wafer is comprised of hundreds of individual devices called "dies". Once the wafer is diced, the dies are packaged into chips.

In its most basic form, semiconductor manufacturing involves variations on the following three methods. First, thin films of materials are deposited on the wafer using

* Corresponding author phone: 1-212-854-9366; fax: 1-212-854-7081; e-mail: nk2162@columbia.edu.
† Columbia University.
‡ University of California.
§ Massachusetts Institute of Technology.
|| Transcarbon International.
⊥ Applied Materials Inc.

10.1021/es071174k CCC: $40.75 
Published on Web 03/19/2008

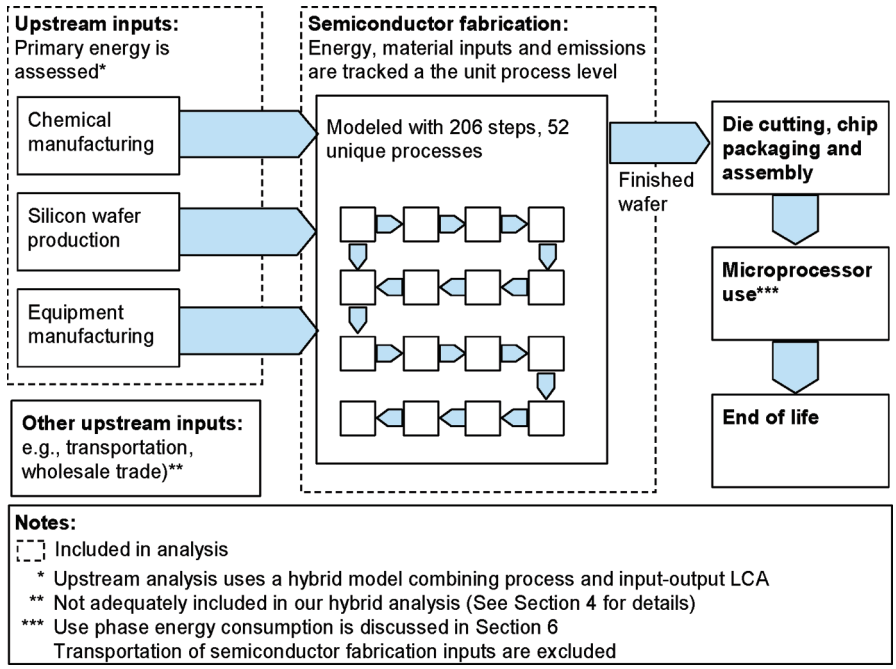



**FIGURE 1. Scope and boundary of analysis.**

physical or chemical processes. This is followed by lithography, the coating the wafer with sacrificial photosensitive materials to transfer a pattern through a mask. Finally, the thin films are etched, resulting in the transfer of the pattern to the films. Other processes are related to the introduction and control of dopants required for transistor active regions (ion implant), planarize films, clean substrates, etc. Details on fabrication processes appear in the Supporting Information.

In this work we use a case example of a modern semiconductor microprocessor at the 130 nm technology "node" (defined by the smallest feature size fabricated in a repeated array). Devices are fabricated on silicon wafer substrates that are 300 mm in diameter, and we choose this wafer as a functional unit. The microprocessor described in this work is equivalent to a Pentium 4. Each 300 mm wafer can produce 442 such functioning Pentium 4 equivalent processors (the wafer can be diced into 491 processors, with a mature die yield of approximately 90%).

Fabrication of the microprocessor is modeled based on a process flow consisting of 195 sequential steps, 53 of which represent unique steps that are repeated with some modifications. The entire inventory and process flow are included in the Supporting Information, Tables S2–S17 . While the existing process flow is most readily adapted to model other integrated circuits (including logic devices, memory and analog devices), our models cover a wide range of typical nanofabrication technologies (different processing techniques and materials), and are linked to the thickness of films deposited, etched or grown. The underlying data set can therefore be adapted by LCA practitioners to model other products such as flat panel displays, photovoltaics and microelectromechanical systems (MEMS). The data set may be adapted by (i) adjusting the process flow; (ii) scaling unit processes inventories based on different film thicknesses; (iii) scaling the inventory based on changes in substrate area, and (iv) modifying or adding specific processes or materials.

We primarily use process emissions, abatement efficiency, and energy consumption data (from 2002 to 2006) that were collected as part of a long-running and ongoing measurement program at Applied Materials Inc. For the purposes of this work, the process flow is organized into four key manufacturing modules: silicon on insulator (SOI), shallow trench isolation (STI), gate stack, and interconnect. Each module consists of numerous individual unit process steps performed on different equipment sets. To perform an inventory analysis, we organize facility mass/flow data according to process and equipment sets to construct a library of environmental process models. For each process step, a hierarchy of three data components is required:

(i) Unit process inputs/outputs: This includes information on identity of and mass of chemicals and other resources used as well as emissions.

(ii) Point-of-use (POU) infrastructure requirements: Each process tool is supported by infrastructure equipment located in the subfab, such as pumps, chillers, heat exchanger, POU abatement equipment, and gas panels.

(iii) Facility infrastructure: Emissions from equipment may require additional treatment at the facility scale (end of pipe), prior to discharge. Also, resources used by equipment may require facilities support. We include mass and energy data associated with systems such as fluoride waste treatment, house scrubbers, heating ventilation, and air conditioning (HVAC), etc.

A description of key fabrication processes, POU infrastructure modules and facility infrastructure modules appear in the Supporting Information.

A hybrid approach is used to evaluate upstream energy requirements. We combine the use of detailed process-based LCA databases for some chemicals and materials with an economic input-output LCA (EIO-LCA) model developed at Carnegie Mellon (*11*) for all other upstream inputs (Figure 1).

In this work our focus is on materials and energy use in semiconductor manufacturing and nanofabrication processes. We, therefore, close the boundaries of the analysis at the point at which wafer processing is complete (Figure 1). We exclude steps related to the dicing of wafers into dies and the packaging of dies in ceramic materials, the mounting and assembly of packaged chips onto circuit boards, and subsequent end of life impacts associated with the devices. We briefly touch upon use-phase electricity consumption in the discussion section.

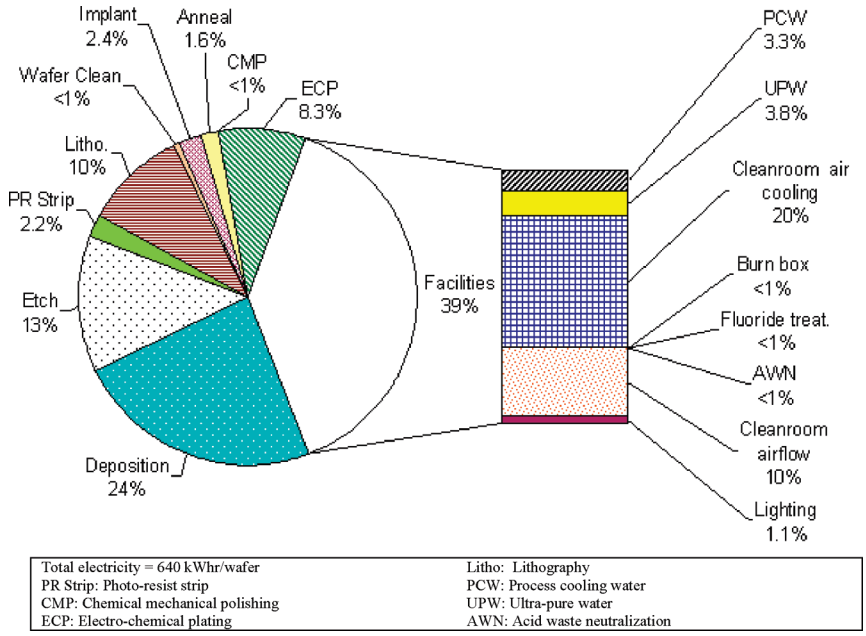



**FIGURE 2. Fab electricity consumption: process vs facility.**

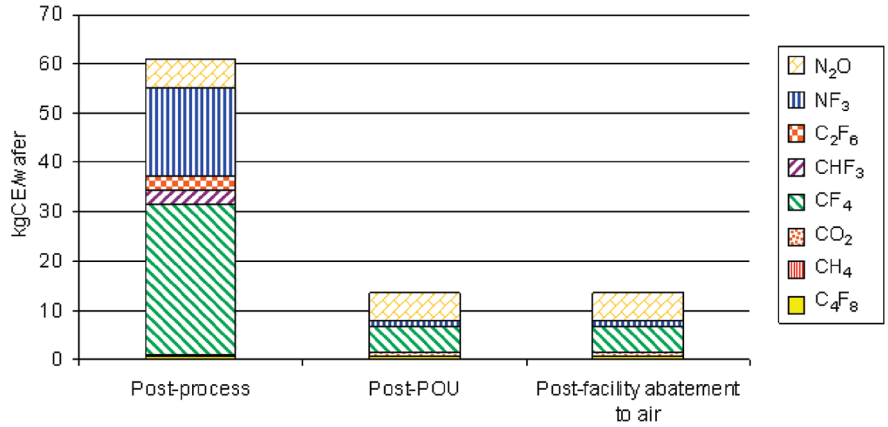



**FIGURE 3. Greenhouse gas (GHG) emissions: postprocess, post-point of use (POU) abatement, and postfacility abatement to air.**

## 3. Manufacturing-Stage Life Cycle Material Inventory Results

Details on selected material and energy flows are presented below. Additional information and detailed inventory tables are included in the Supporting Information, Tables S3–S17. The electrical demands in the fab are illustrated in Figure 2. Process electricity accounts for approximately two-thirds of the total electrical demands inside the facility. Deposition and etch processes are seen to drive process electricity consumption. Electricity consumption at the facility scale is driven by clean-room air cooling and airflow (which includes purification), followed by process cooling water (PCW) pumping and cooling, and ultrapure water (UPW) purification systems.

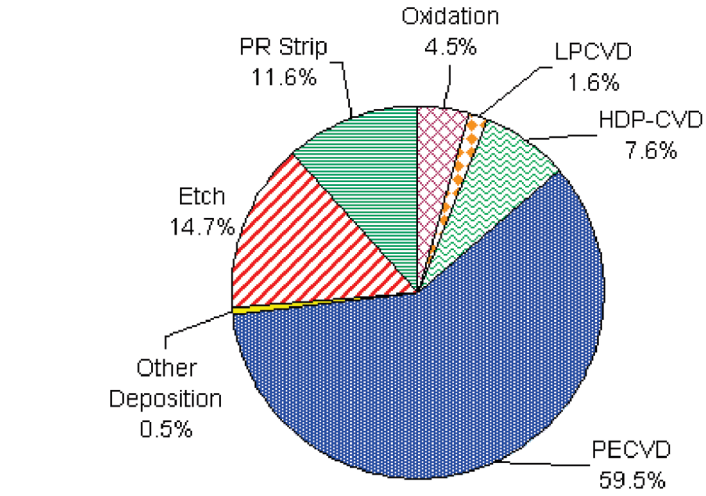
Manufacturing processes often involve the use and emission of perfluorocarbons (PFCs) that have high global warming potentials. POU abatement based on combustion or plasma technologies can be located downstream of process chambers and used to break down emissions (Figure 3). Considering all processes, POU abatement reduces global warming impact of chamber emissions from 61 kg carbon equivalent (kgCE)/wafer to 13 kgCE/wafer, which is close to an 80% reduction. Conventional facility abatement systems use water scrubbers and provide no abatement of GHGs.

All deposition processes use a plasma to clean residues from chamber walls in between deposition steps. In our inventory, we consider chamber cleaning technologies that use $NF_3$ remote plasma formation (plasma is formed external to the process chamber). This technology is increasingly finding adoption, because it helps reduce both GHG emissions and clean times (*12*). Despite this improvement, PE-CVD (a deposition process) still remains the largest contributor to GHG emissions (Figure 4). Etch processes are the second largest contributors primarily due to emissions of $N_2O$, which is not abated as efficiently as other GHGs.

Volatile organics are a growing concern for fabs, and are used in parts cleaning, lithographic processes, and to a lesser extent, in deposition. Only deposition steps have POU abatement of VOCs, in which trimethyl-silane (TMS) is abated with a typical efficiency of >98% (Figure 5). Other process VOCs may be abated at the facility level through oxidation, at efficiencies between 95 and 99%. Liquid organic wastes of propylene glycol monomethyl ether (PGME), p-cresol, m-cresol and formaldehyde are collected through solvent drains and hauled away for further treatment.

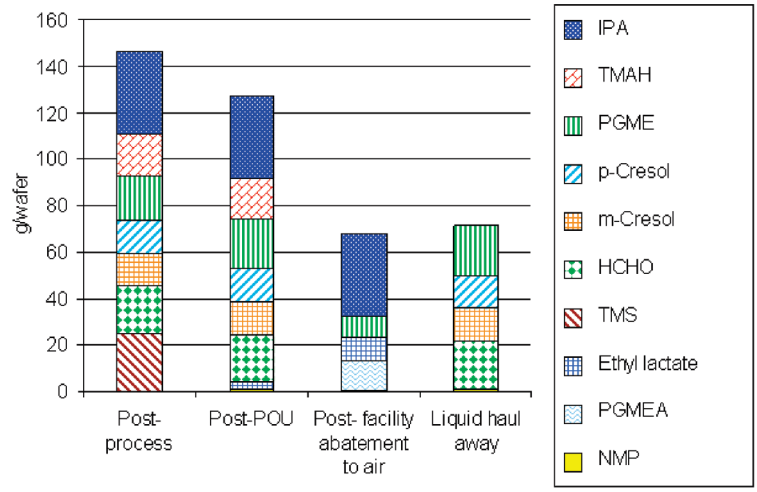
## 4. Upstream Energy Requirements

We use a hybrid formulation (*10*) to estimate upstream energy requirements (eq 1), where *E* refers to life cycle primary energy




| | |
|---|---|
| Total Post-POU GHG emissions = 29 kgCE/wafer | HDP-CVD: High density Plasma CVD |
| CVD: Chemical Vapor Deposition | PECVD: Plasma Enhanced CVD |
| LPCVD: Low Pressure CVD | PR: Photo-resist |

**FIGURE 4. Global warming potential of post POU abatement emissions by process (% kgCE/wafer).**




| | |
|---|---|
| IPA: Isopropyl alcohol | TMS : trimethyl silane |
| TMAH : tetra methyl ammonium hydroxide | PGMEA: propylene glycol methyl ether acetate |
| PGME : propylene glycol monomethyl ether | NMP : n-methylpyrrolidone |

**FIGURE 5. Organic compounds: postprocess, post-point of use (POU) abatement, postfacility abatement to air, and liquid haul away.**

requirements and the subscripts *i* and *j* refer to inputs that are modeled using process-based LCA and IO LCA respectively.

$$E_{\text{Life\_Cycle}} = \sum_{\text{i}} E_{\text{ProcessSum},i} + \sum_{\text{j}} E_{IO,j} \qquad (1)$$

Such a formulation expands the number of inputs that we can include in the analysis. While we explicitly include upstream inputs related to chemicals, silicon wafer production, and equipment, such an approach may still leave out other upstream processes that may be important. Running EIO-LCA for the semiconductor sector offers a rough estimate of processes that may be important and that are not included. In terms of primary energy demand, there are eight sectors in the top 25 (that together contribute to approximately 11% of total primary energy) that may have been excluded in our analysis—related to transportation, wholesale trade, warehousing, and storage, paper manufacturing, couriers, and management of companies. Given that the top 25 most important sectors account for close to 90% of total primary energy requirements, we estimate that our hybrid LCA formulation may undercount primary energy by at least 12%.

**Chemical Manufacturing.** As described before, modern semiconductor manufacturing involves the use of hundreds of specialty chemicals and materials, most of which are of high purity. For a modern microprocessor this means that some chemicals have allowable metallic contamination levels of 0.1−1 ppb (*13*). LCI data on high purity or specialty chemicals are extremely scarce in the literature (*13, 14*), and chemical manufacturers are reluctant to share process information owing to proprietary concerns. To make this analysis tractable, we therefore leave out purification energy requirements from any process LCI data used with the understanding that this may result in a degree of undercounting of energy. We identify an examination of purification energy requirements, along with detailed gate-to-gate LCI for semiconductor chemicals, along the lines of previous work on bulk chemicals (*15, 16*), as an important topic of future work.

Given these limitations, when upstream life cycle chemical manufacturing energy data exist (even if for industrial grades), we use these numbers. For our process flow, total energy use from process LCI amounts to 580 MJ/wafer. For the remaining chemicals, we use EIO-LCA. The price per unit mass of specialty chemicals can be up to 2–3 orders of magnitude

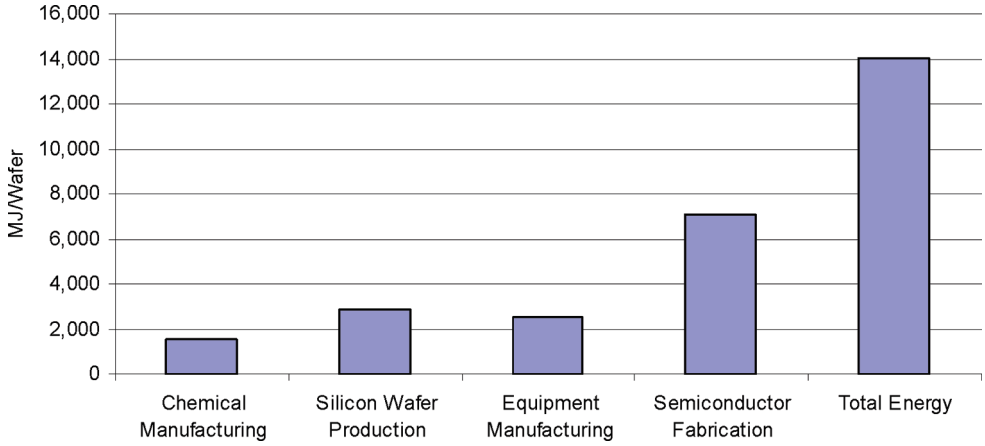



**FIGURE 6. Life cycle primary energy requirements.**

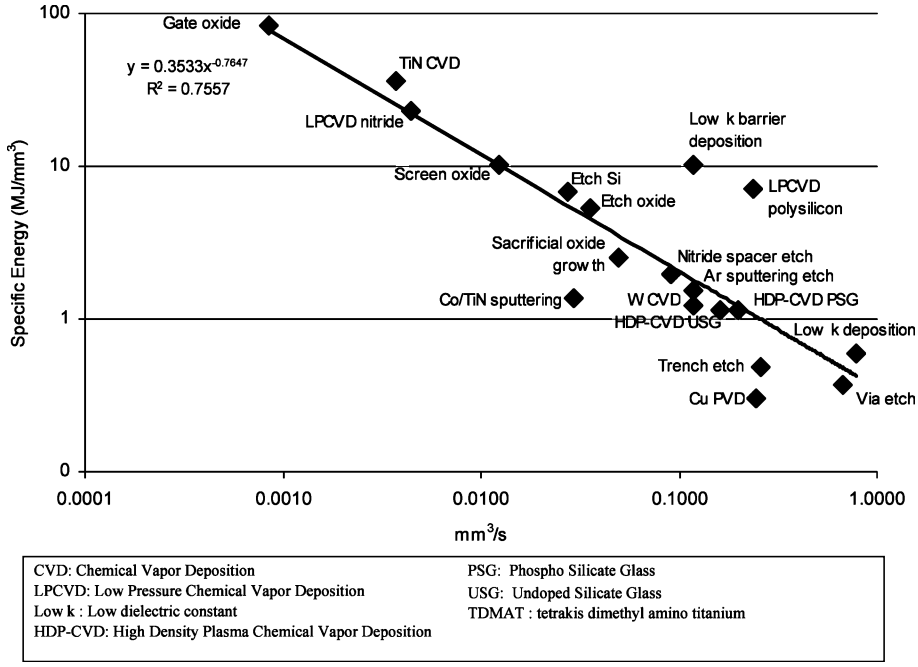



**FIGURE 7. Specific processing energy (MJ/mm³) vs process rate (mm³/s).**

greater than bulk chemicals (10–100 $/kg as opposed to 1 $/kg for bulk chemicals). It is, therefore, not reasonable to use specialty chemical prices in combination with EIO-LCA supply chain energy intensities ($E_{sc}$) for bulk chemical sectors. Bulk chemical sectors represent a high energy consumption for a low $ value. We therefore adopt an approach described by Williams (*17*) and utilize the sector, photographic film, paper plate and chemical manufacturing, that has an $E_{sc}$ of 7.5 MJ/$ ($E_{sc,photo\_films}$), that is similar to the silicon supply chain ($E_{sc,Si}$ = 5 MJ/$). Upstream energy requirements for the remaining chemicals ($E_{rem\_chem}$) are obtained by multiplying this $E_{sc}$ figure with the sum of the producer prices for all corresponding input chemicals, $C_j$ (124 $/wafer in 1997 $) resulting in 930 MJ/wafer (eq 2). Estimates for producer prices are obtained from semiconductor industry sources.

$$E_{rem\_chem} = \left(E_{sc,photo\_films}\frac{MJ}{\$}\right)\cdot\left(\sum_j C\frac{\$}{\text{wafer}}\right)$$

$$= (7.5)\cdot(124)\frac{MJ}{\text{wafer}}$$

$$= 930\frac{MJ}{\text{wafer}} \qquad (2)$$

**Silicon Wafer Production.** We estimate energy requirements related to silicon using data from the literature. To form 1 kg of crystalline silicon wafer, 2,127 kWh of electricity is required (*1*), which translates to 2,900 MJ/wafer for a standard 300 mm wafer. This energy figure accounts for: processing of mined quartz into metallurgical grade Si, purification of metallurgical Si into an ingot and processing of the ingot into wafers.

**Equipment Manufacturing.** We use an IO approach to estimate the embedded energy of semiconductor capital equipment. $E_{sc}$ for the sector, semiconductor machinery manufacturing ($E_{sc,\ semi\_equipment}$) is 7.09 MJ/$. A typical fab producing microprocessors on 300 mm wafers invests roughly $ 1.1 billion (in 1997 $) in equipment, $C_{equipment}$ (*18*) and produces 6000 wafer starts per week ($N_{Wspw}$). Although semiconductor manufacturing processes change rapidly (with time cycles of 18 months), equipment lasts much longer and often has a lifetime of 10 years ($t$ = 520 weeks). Process chambers may be upgraded or modified, but the core equipment platform remains. Also, older equipment are often used to run less critical processes. As a first-order estimate, we leave out the embedded energy related to chamber upgrades and maintenance (parts, supplies) and estimate equipment embedded primary energy as below (eq 3).

$$E_{E\text{quipment}} = \left(E_{sc,\text{semi\_equipment}}\frac{MJ}{\$}\right)\cdot\left(\frac{C_{\text{equipment}}\$}{N_{W\text{spw}}\cdot t}\right) = (7.09)\times \left(\frac{1.1\cdot 10^9}{6,000\cdot 520}\right) = 2,500\frac{MJ}{\text{wafer}} \quad (3)$$

## 5. Uncertainty

Of the various components of the hybrid LCI model presented, the material and energy inventory related to semiconductor manufacturing is the most up to date and accurate. Material flows are primarily based on process recipes, and an emissions measurement program at Applied Materials. Stoichiometric balances are used to check mass flows, and most unit process mass balances are closed within 10%. Care must be taken, however, in translating the data presented to any specific logic or memory product. Variations in recipes, overall process flow (number and type of steps), and presence of different types of abatement equipment will influence the inventory. For example, fabs that do not have POU abatement equipment for GHGs may have a factor of 4–5 more GHG emissions as compared with fabs that do (Figure 3). Additionally, technological change occurs rapidly in the semiconductor industry. While the addition of new processes or process modifications with new technology nodes will require that the underlying data set be modified, we have attempted to streamline the process of updating this analysis by presenting detailed and disaggregated inventory tables (at the unit process level).

We expect there is greater uncertainty in the models used for estimation of upstream energy requirements. In addition to known issues with EIO and process LCA—owing to errors in economic data, errors in sector aggregation, and potential boundary errors with process LCA (*8–10*)—there are two key sources of uncertainty. First, as described before, the hybrid model we have used requires an explicit definition of upstream inputs (we have included chemicals, equipment and silicon) and may exclude some important processes. Second, we have somewhat excluded chemical purification energy. The process LCI data we have used are associated with industrial grades (90–99% purity range) (*19–22*). Purification energies associated with industrial chemical grades could be several MJ/kg; by comparison, semiconductor grade silicon requires processing energies of 10–100 MJ/kg (*1*). It is doubtful, however, that such large purification energies would be required for all semiconductor grade chemicals. Data on the production of $H_2O_2$ indicates that industrial grade requirements are 6.7 MJ/kg. Processing to super large scale integration (SLSI) specifications that emerged in the mid 1990s (<1 ppb of impurity metals) requires an additional 1.3 MJ/kg and to extra large scale integration (XLSI) specifications that emerged in the late 1990s (<100 ppt of impurity metals) requires an additional 0.2 MJ/kg (*13*). The EIO-LCA model we use may account for purification energy to a certain extent, because we use the energy intensity (MJ/$) value of the photographic film sector. If a purified specialty chemical sector existed, it may have a lower energy intensity than photographic films (specialty semiconductor chemicals have higher specific energy but are also significantly more expensive). For both these reasons (exclusion of upstream processes and partial exclusion of purification energy), our analysis should be viewed as a lower bound on total life cycle energy.

## 6. Discussion

**Energy Consumption.** We estimate the total primary energy requirement associated with upstream (chemicals and infrastructure) and device manufacturing at 14 100 MJ/wafer, with about half of this going to device fabrication itself (7100 MJ/wafer for a 6-layer microprocessor), followed by silicon wafer production (2900 MJ/wafer) (Figure 6). It is interesting to note that equipment infrastructure, at 2500 MJ/wafer and chemical manufacturing (1510 MJ/wafer) represent a non-negligible fraction of the overall amount. While our estimate for chemical energy is slightly higher than that by Williams (1020 MJ/wafer) (*1*), it may still be an underestimate, since we only approximately account for purification energy requirements.

Our estimate for fabrication energy consumption related to process equipment alone is 4700 MJ/wafer, which is lower than Murphy's figure of 8000 MJ/wafer (*5*) (wafer size, which varies among these studies, is normalized to 300 mm for comparison). Our overall result for semiconductor fabrication energy (combining process and facility infrastructure) is 7100 MJ/wafer, which is lower than that cited by both Williams (11 900 MJ/wafer) (*1*) and Yao (16 600 MJ/wafer) (*6*). Differences between these studies may be driven by technology evolution. Our analysis is based on more recent fabrication techniques and involves larger, 300 mm wafers that tend to cost more and are less energy efficient per unit area of production (*23*). Furthermore, both Williams and Yao use a "top-down" type of approach to estimate energy/wafer so it is reasonable to find that these studies are more inclusive and have energy estimates higher than those found in our work. In particular, our estimate for facility infrastructure energy use may be low.

Use phase energy consumption for a logic device designed on the 130 nm node and produced on 300 mm wafers is an Intel Pentium 4 processor, which uses 6–8 W of power in operation (*6*). The lifetime of a desktop computer is taken to be three years (*17*) and we assume a home use at a duty cycle of 3 h/day, with no standby (*24*). Such a processor will consume 20–26 kWh of electrical energy over a lifetime of use, which translates to 211–281 MJ/die of primary energy for 10.7 MJ of primary energy per kWhr (*1*). Given that 442 Pentium 4 Northwood processors are produced per wafer, we determine use phase energy to be 93–124 GJ/wafer. This quantity is almost a factor of 8 larger than our total upstream production chain energy estimate. This result is consistent with analysis performed by Yao et al. (*6*) in which gate-to-gate manufacturing energy for a Pentium 4 (3.5 kWhr/die) is an order of magnitude lower than use-phase energy number (25–45 kWhr/die). The result is, however, contrary to that presented by Williams (*1*), in which an analysis of a 32 MB DRAM device indicates that fabrication energy (27 MJ/die) exceeds use-phase energy (15 MJ/die). The primary reason for this discrepancy is the significantly lower power requirements of the DRAM device (0.3 W) when compared with a logic device (6–8 W). In order to reduce overall energy consumption of logic devices, use phase power reduction and effective power management are the most important areas requiring improvement. For memory and passive devices, semiconductor fabrication energy consumption is relatively more important.

**Energy Consumption in Nanofabrication.** Researchers have conjectured that manufacturing processes used to manipulate materials at smaller ("nano") length scales may have disproportionately high energy demands (*1, 25*). Gutowski and collaborators have examined the specific manufacturing energy (the energy per unit volume material addition or removal, MJ/mm$^3$) for a range of manufacturing processes (*25*). They observe that specific manufacturing energy increases dramatically with increasing precision, and that an inverse trend is observed between specific manufacturing energy and rate of material removal.

Based on our data sets, we develop an equivalent process energy map for several key fabrication processes used in semiconductor manufacturing (Figure 7). Our results also indicate an upward trend in specific manufacturing energy as a function of decreasing processing rate (increasing precision). Given trends toward increasing precision and

nanoscale fabrication in semiconductor and other applications (smaller features, thinner films), the results indicate that it may be important to examine energy consumption related to nanofabrication processes in more detail. The processes with highest specific energy consumption are formation of the gate oxide (thermal oxidation) and CVD of thin films (TiN CVD and LPCVD of silicon nitride). The analysis presented only considers the specific processing energy within the manufacturing facility. As mentioned before, additional work is also required to quantify energy requirements related to ultrapure materials used in nanofabrication.

The semiconductor industry has made significant progress in improving its environmental performance, and continues to develop a proactive environmental roadmap (*6, 26*). However, it is important for the semiconductor industry, and other industries using nanofabrication processes, to continue to optimize fabrication processes, and to reduce the use and emissions of toxic and hazardous materials. Our life cycle inventory model provides a methodology and data set to quantify the environmental implications of a broad set of nanofabrication processes. It is our hope that many applications and tools will emerge from this work.

## Acknowledgments

We thank Mehran Moalem of Applied Materials Inc. for helpful comments. The manuscript reviewers also provided invaluable feedback.

## Supporting Information Available

Section A: Acronym guide; Section B: Semiconductor manufacturing overview; Section C: Manufacturing process flow; Section D: Supplemental results; Section E: Detailed inventory tables; Figures S1–S8; Tables S1–S17. This material is available free of charge via the Internet at http://pubs.acs.org.

## Literature Cited

(1) Williams, E. D.; Ayres, R. U.; Heller, M. The 1.7 kilogram microchip: Energy and material use in the production of semiconductor devices. *Environ. Sci. Technol.* **2002**, *36* (24), 5504–5510.

(2) Schischke, K.; Stutz, M.; Ruelle, J. P.; Griese, H.; Reichl, H. Life Cycle Inventory Analysis and Identification of Environmentally Significant Aspects in Semiconductor Manufacturing. *Proceedings of the 2001 IEEE Symposium on Electronics and the Environment*, Denver, CO, 2001, 145–150.

(3) Taiariol, F.; Fea, P.; Papuzza, C.; Casalino, R.; Galbiati, E.; Zappa, S. Life Cycle Assessment of an Integrated Circuit Product. *Proceedings of the 2001 IEEE Symposium on Electronics and the Environment*, Denver, CO, 2001, 128–133.

(4) Smati, R.; Raoux, S.; Ho, D.; Woolston, M.; Measuring and modeling gas consumption and emissions from semiconductor manufacturing processes. *EHS Assessment Techniques, Semi Technology Symposium*, SEMICON West, 2002.

(5) Murphy, C. F.; Kenig, G. A.; Allen, D. T.; Laurent, J-P.; Dyer, D. E. Development of parametric material, energy, and emission inventories for wafer fabrication in the semiconductor industry. *Environ. Sci. Technol.* **2003**, *37* (23), 5373–5382.

(6) Yao, M.; Wilson, A. R.; McManus, T. J.; Shadman, F. Comparative Analysis of the Manufacturing and Consumer Use Phases of Two Generations of Semiconductors. *Proceedings of the 2004 IEEE International Symposium on Electronics and the Environment*, Scottsdale, AZ, 2004, 97–103.

(7) Krishnan, N.; Raoux, S.; Dornfeld, D. Quantifying the environmental footprint of semiconductor equipment using the environmental value systems analysis (EnV-S). *IEEE Trans. Semiconduct. Manuf.* **2004**, *17* (4), 554–561.

(8) *Environmental Management—Life Cycle Assessment—Goal and Scope Definition and Inventory Analysis*; International Organization for Standardization: Brussels, 1998; ISO 14041.

(9) Hendrickson, C.; Horvath, A.; Joshi, S.; Lave, L. Economic input-output models for environmental life-cycle assessment. *Environ. Sci. Technol.* **1998**, *32* (7), 184A–191A.

(10) Suh, S.; Lenzen, M.; Treloar, G. J.; Hondo, H.; Horvath, A.; Huppes, G.; Jolliet, O.; Klann, U.; Krewitt, W.; Moriguchi, Y.; Munksgaard, J.; Norris, G. System boundary selection in life-cycle inventories using hybrid approaches. *Environ. Sci. Technol.* **2004**, *38* (3), 657–664.

(11) Economic Input-Output Life Cycle Assessment (EIO-LCA). http://www.eiolca.net.

(12) Raoux, S. Remote microwave plasma source for cleaning CVD chambers—A technology for reducing global warming gas emissions. *J. Vac. Sci. Technol., B* **1999**, *17* (2), 477–485.

(13) Plepys, A. The Environmental Impacts of Electronics: Going Beyond the Walls of Semiconductor Fabs. *Proceedings of the 2004 IEEE Symposium on Electronics and the Environment*, Scottsdale, AR, 2004, 159–165.

(14) Geisler, G.; Hofstetter, T. B.; Hungerbuhler, K. Production of fine and specialty chemicals: Procedure for the estimation of LCIs. *Int. J. LCA* **2004**, *9* (2), 101–113.

(15) Jiminez-Gonzalez, C.; Kim, S.; Overcash, M. R. Methodology for developing gate-to-gate life cycle inventory information. *Int. J. LCA* **2000**, *5* (3), 153–159.

(16) Kim, S.; Overcash, M. Energy in chemical manufacturing processes: Gate-to-gate information for life cycle assessment. *J. Chem. Technol. Biotechnol.* **2003**, *78*, 995–1005.

(17) Williams, E. Energy intensity of computer manufacturing: Hybrid assessment combining process and economic input-output methods. *Environ. Sci. Technol.* **2004**, *38* (22), 6166–6174.

(18) Marmillion, N., Controlling Fab Tool Costs with Improved Equipment Productivity, Micro Magazine, May 2006. http://www.micromagazine.com.

(19) *BUWAL 250, Life Cycle Inventories for Packaging, Forests and Landscape, II*; Swiss Agency for the Environment: Berne, 1998.

(20) Boustead, I.; Hancock, G. F. *Energy and Packaging*; Ellis, Horwood, Chichester/John Wiley: New York, 1981.

(21) ETH-ESU, SIMAPro 6 Database Manual: The ETH-ESU Libraries. Pre Consultants, 2004. http://www.pre.nl.

(22) Frischknecht, R. ecoinvent Data v1.1 (2004): From heterogenous databases to unified and transparent LCI data. *Int. J. LCA* **2005**, *10* (1), 1–2.

(23) LoPiccolo, P.; ISMI REPORT: Intel Touts Environmental Benefits of 300 mm Conversion. Solid State Technology WaferNews. October 2006. http://sst.pennnet.com.

(24) Williams, E.; Hatanaka, T. ; Residential Computer Usage Patterns in Japan and Associated Life Cycle Energy Use. *Proceedings of the 2005 IEEE International Symposium on Electronics and the Environment*, New Orleans, LA, 2005, 177–182.

(25) Gutowski, T.; Dahmus, J. Thiriez, A.; Branham, M.; Jones, A.; A Thermodynamic Characterization of Manufacturing Processes. *Proceedings of the 2007 IEEE International Symposium on Electronics and the Environment*, Orlando, FL, 2007, 137–142.

(26) International Technology Roadmap for Semiconductors (ITRS) 2006 Update: Environment, Safety and Health. http://www.itrs.net.

ES071174K