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A Method of Partial Inductances to Evaluate and Optimize Switching Cells

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Abstract—**Advances in wide-bandgap devices have enabled increased switching frequencies in modern power converters. As a result, the parasitic inductance arising from switching cell layout has become critical to converter performance and operation. This inductance not only reduces slew rate, which degrades efficiency, but can also cause electromagnetic interference and destructive voltage overshoot. This paper presents a method for estimating the inductance of printed circuit board (PCB) commutation loops, targeted for rapid iteration by the power electronics designer. Based on partial inductances, the computationally efficient approach is amenable to fast parametric sweeps. The proposed technique is also platform-independent, such that it may be scripted into existing optimization tools. To validate the accuracy of the technique, a detailed quantitative comparison is performed with commercial simulation tools as well as experimental measurements on a number of hardware prototypes.**

I. INTRODUCTION

The switching speed of power transistors has increased dramatically in recent years, due in large part to improvements in packaging as well as the proliferation of commercial wide-bandgap devices, such as gallium-nitride high-electron-mobility transistors (GaN HEMTs) [1]–[3]. With reduced on-resistance, lower output capacitance, and minimal package inductance, especially for flip-chip and BGA packages, these switches are capable of extremely high dv/dt transitions. As such, converter performance is now greatly determined by PCB layout.

The switching cell of a buck converter provides a canonical example, as shown in Fig. 1. When the converter is in state 1, the input capacitor and high-side switch, C_{IN} and Q_{HS}, carry the load current. When the converter is in state 2, the low-side switch, Q_{LS}, carries this current. These components see a step-change in operating current upon state transitions and therefore define the switching cell (or commutation loop, used interchangeably in this paper). The loops depend on converter topology and operation, but typically include at least one capacitor and complementary switches.

Parasitics arising from the routing of this commutation loop must be minimized to take full advantage of high switching speed [4]–[7]. Commutation loop inductance can be detrimental in multiple ways. If the devices are switched quickly, energy stored in the current flowing through this inductance will be rapidly transferred to the C_{OSS} of the off-state device. This leads to over-voltage, as well as electromagnetic interference from the resultant high-frequency ringing [8]. If
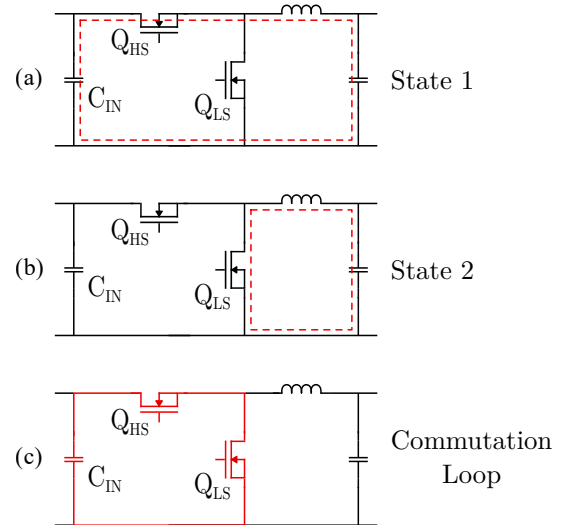

Fig. 1: Highlighting the commutation loop for a buck converter (a) Current path when Q_{HS} is on, (b) Current path when Q_{LS} is on, (c) Components with step-change in conducted current upon state transition.

this behavior is mitigated by slowing the switching transition (e.g., by increasing the gate resistance), converter performance will suffer due to increased overlap loss.

Although these parasitic inductances in switching loops significantly affect operation and performance, their impact is often difficult to estimate at the design stage. At the same time, performance metrics of power converters are tightly coupled, requiring an understanding of trade-offs associated with operating parameters, such as switching speed, and physical constraints imposed by the hardware implementation of the converter. As a result, multi-objective optimization programs have become popular [9]–[11].

In this work, we present a new technique which utilizes partial inductances [12] and linear algebra to evaluate commutation loop inductance. The proposed technique is efficient and platform-independent, to facilitate integration within existing converter design and analysis scripts. This allows for rapid iteration and fast parametric sweeps of loop geometries. Users can therefore optimize a design before fabrication, and develop more accurate predictions of converter performance. Existing simulation/modeling tools are either highly detailed finite

element analysis (FEA) that require a full electrical design to simulate (e.g., Ansys Q3D), or are intended for general purpose use (e.g., FastHenry [13]) or the design of semiconductor power modules [14]. These tools also require the use of a specialized software package. This represents a barrier towards integrating accurate commutation loop considerations as part of the design process.

The remainder of this paper is organized as follows: Section II details the proposed analytical approach. Then, Section III illustrates techniques by which commutation loop prototypes can be accurately characterized and provides experimental results. Finally, Section IV concludes the paper.

II. ANALYTICAL FRAMEWORK

A. Segmentation

A segmentation process approximates the loop into straight segments and divides them at each corner or turn. This greatly simplifies the calculations as current paths become either parallel segments, which influence each other magnetically according to known formulas [15], [16], or perpendicular segments, whose interaction is ignored. This approach is especially suited for PCB commutation loops, where conductors are either horizontal planes or vertical vias. Moreover, component and trace spacing is typically limited by either the rectangular package dimensions or by creepage/clearance limitations between conductors. As a result, diagonal current flow in-plane is often negligible, and the perpendicular approximation is sufficient.

Next, each segment is labeled with a starting and ending node. Mesh and nodal analysis are used to determine the overall circuit schematic. As such, the proposed technique can be employed to study commutation loops containing an arbitrary number of parallel or series current paths without requiring further specification. This functionality is particularly applicable to cases with paralleled capacitors, paralleled switches, or other programming studies. The netlist derived at this stage is stored in binary matrices defined by the relations in (1) and (2).

$$\mathbf{0} = \mathbf{C}_N \mathbf{I} \quad (1) \qquad \mathbf{0} = \mathbf{C}_M \mathbf{V} \quad (2)$$

Here, $\mathbf{C}_N$ represents the nodal matrix indicating that the current flow out of every node equals zero. Similarly, $\mathbf{C}_M$ is the mesh matrix indicating that the voltage drop around every loop equals zero.

B. Meshing

At high frequency, the magnitude of current density through a conductor is highly position-dependent due to skin and proximity effects [17]. These effects cause nearly all of the current to flow at the edges of the conductor. To account for this, a meshing stage further divides each loop segment into sub-segments along the length of the conductor. To limit model complexity, the proposed approach utilizes a meshing technique for which the number of sub-segments is independent of frequency; Fig. 2 shows how only the edge
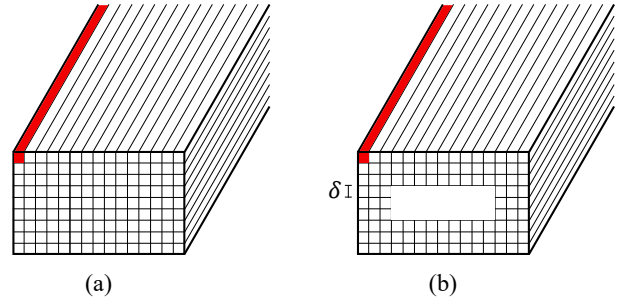

Fig. 2: Illustration of meshing with one sub-segment highlighted. (a) Uniform grid, (b) Proposed mesh with reduced number of sub-segments covering outer 3 skin depths.

of the conductor is divided into a uniform grid of skin-depth (δ) thick sub-segments, while the inner portion remains lumped together. As the frequency increases, the width of the outer sub-segments simply become thinner. Compared to fully meshing the conductor, the number of sub-segments can be reduced greatly, while the edges of the conductor are always measured with high fidelity.

C. Partial Inductances

While closed-form approximations for the DC inductance of simple loops have been derived [18], precisely computing the high-frequency inductance of typical commutation loops is not practical. Even for simple geometries, combining the inverse quadratic magnetic field equation with exponential current densities makes the problem intractable. Therefore, the proposed analytical technique extends prior work on partial inductance modeling [18]–[20]. With the segmentation and netlist previously defined, the resulting problem can be written concisely as (3).

$$V_i = I_i(R_i + jwL_i + jw\sum_j M_{i,j}) \qquad (3)$$

Here, V_i, and I_i are the voltage across and current through the ith sub-segment. R_i and jwL_i are the self-impedance of this sub-segment; and $M_{i,j}$ is the mutual inductance between sub-segments i and j.

Considering all of the sub-segments of the loop, (3) can be extended to matrix form, as shown in (4).

$$\underbrace{\begin{bmatrix} V_1 \\ \vdots \\ V_{N_S} \end{bmatrix}}_{\text{Vs}} = \underbrace{\begin{bmatrix} Z_{1,1} & \dots & Z_{1,N_S} \\ \vdots & Z_{i,j} & \vdots \\ Z_{N_S,1} & \dots & Z_{N_S,N_S} \end{bmatrix}}_{\text{Zs}} \underbrace{\begin{bmatrix} I_1 \\ \vdots \\ I_{N_S} \end{bmatrix}}_{\text{Is}} \qquad (4)$$

Here, N_S is the total number of sub-segments. On the diagonals, $Z_{i,i} = R_i + jwL_i$ and for the off-diagonals, $Z_{i,j} = jw\sum M_{i,j}$. Equation (4) can be rewritten with admittance and simplified by noting that the voltage drop across every sub-segment within the same segment is identical. Therefore, the admittances of all the sub-segments in a segment can be summed, the sub-segment currents can be summed, and the
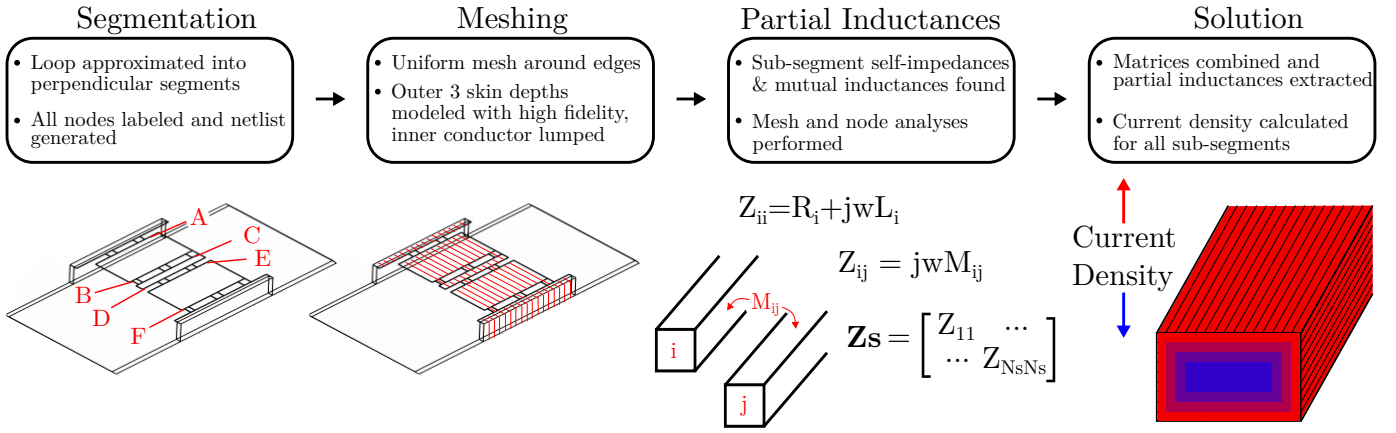
Fig. 3: Summary of proposed analytical approach.

matrix can be written in terms of segments instead of sub-segments.

$$\begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} Y_{1,1} & \cdots & Y_{1,N} \\ \vdots & Y_{p,q} & \vdots \\ Y_{N,1} & \cdots & Y_{N,N} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_N \end{bmatrix} \quad (5)$$

$$\underbrace{}_{\mathbf{I}} \quad \underbrace{}_{\mathbf{Y}} \quad \underbrace{}_{\mathbf{V}}$$

Here, N is the number of segments. I_p is the current through segment p; V_q is the voltage across segment q; and $Y_{p,q}$ is the admittance between segments p and q, found by summing the admittances between all of their sub-segments.

At frequencies of interest (determined by the slew rate of the switch transition, e.g. 100 MHz for WBG devices), δ widths are on the order of microns, while segments may have lengths which are many orders of magnitude larger. This vast range of scales makes most mutual inductance formulas numerically unstable–or at the very least inaccurate. Correspondingly, the proposed implementation selects an appropriate formula to calculate mutual inductance based on the geometry for each pair of sub-segments. For example, if the thickness of the conductor is much smaller than the length and width, it can be approximated as a surface as opposed to a rectangular prism.

D. Solution

The solution to the loop inductance problem can be found by combining (1), (2) and (5) into (6).

$$\mathbf{0} = \begin{bmatrix} \mathbf{C}_N \mathbf{Y} \\ \mathbf{C}_M \end{bmatrix} \mathbf{V} \quad (6)$$

Without loss of generality, the current through the loop is chosen to be 1 A, such that the voltage across each segment represents its impedance. This equation is then solved for $\mathbf{V}$ using this constraint. Given that the entries in $\mathbf{V}$ correspond to the impedance of each segment, the overall loop inductance may be computed as the sum of the imaginary components, which is shown in (7), where f is the frequency.

$$L = \frac{\mathrm{Im}\{ \sum_{q=1}^{N} V_q \}}{2\pi f} \quad (7)$$

The current through each sub-segment is computed as well by dividing the segment voltages, V_q, by the impedance of each sub-segment (from $\mathbf{Z}_S$) within that segment. Fig. 3 summarizes the process of the proposed technique.

III. EXPERIMENTAL VALIDATION

To investigate the accuracy of the proposed technique and develop a high-precision methodology for experimental verification, two versions of a characterization PCB were fabricated each with four different types of half-bridge switching cell layouts (utilized in e.g., a buck or boost converter), and a flying capacitor multilevel (FCML) cell. These layouts were designed in lateral, lateral with ground plane beneath, hybrid, and vertical topologies [5], [7], which represent common approaches to commutation loop routing, and are illustrated in Fig. 4.
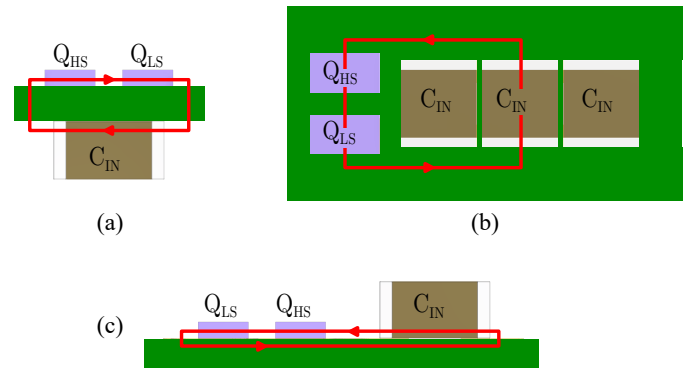

Fig. 4: Typical half-bridge switching cell designs with path of current flow highlighted. (a) Vertical layout, (b) Lateral layout, (c) Hybrid layout.

To highlight applications in high-power-density designs, each assembled circuit utilized EPC2034C [21] BGA switches
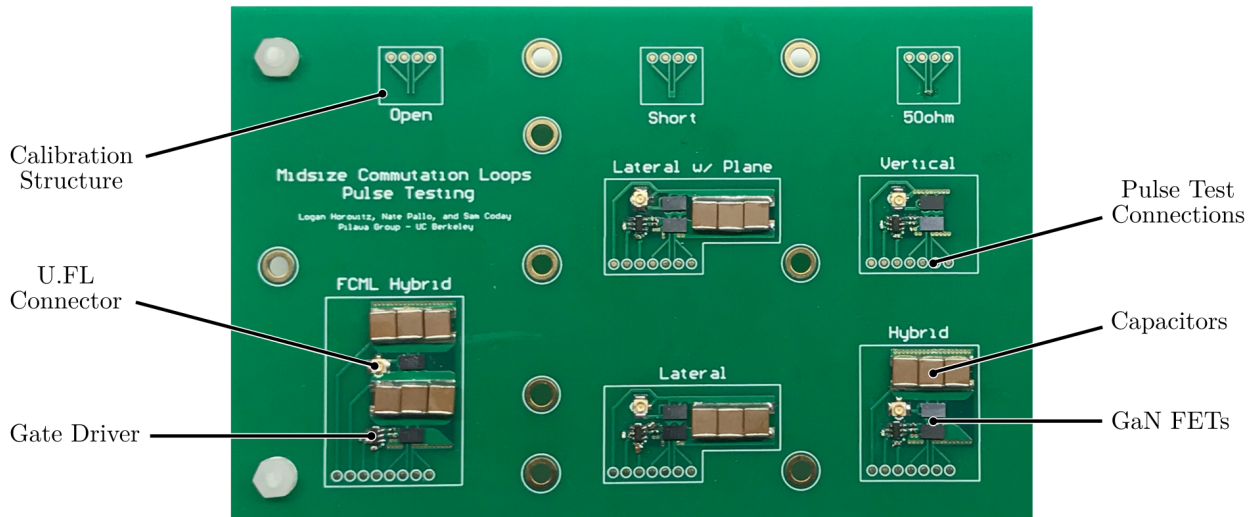
Fig. 5: Pulse testing PCB with various switching cell designs and calibration structures.

and high-energy-density surface-mount ceramic capacitors. One PCB version was designed for precise measurements using an impedance analyzer, with the capacitors and high-side switch pads shorted to capture only the impedance imposed by the PCB routing. The second PCB was designed for pulse testing, with all components populated, as shown in Fig. 5.

The aforementioned analytical methodology was implemented as a MATLAB script, but is not reliant on any specific capabilities of the program, and could thus be implemented in Python or other programming languages. The bulk of computation time goes into calculating the mutual inductances for the impedance matrix in (4). For each of the loop designs on the characterization PCB, the overall inductance was computed at various frequencies with this program. To measure the loop inductances with FEA software, the copper from the layouts was extracted and the AC inductance across frequency was computed in Q3D for each loop. For both of these programs, the components are modeled as thin copper shorts.

Next, a Keysight E4990A impedance analyzer was used with 42941A probe to measure the inductance of each loop. Calibration structures were placed on the PCB, as shown in Fig. 5, to provide a short, open, and $50\,\Omega$ reference load with the exact same preceding connections as for the loops themselves. The board is held in a vise, and the probe is similarly held by a clamp at fixed height. The impedance measurement is taken at 100 MHz, which is a sufficiently high frequency to measure the small reactance reliably [22].

Finally, the inductance was also estimated by measuring the ringing frequency of the drain-to-source voltage of the high-side transistor during a switching transition. A new 'single pulse test' circuit was used to generate this transition, as shown in Fig. 6. As opposed to a double pulse test, the large inductance is replaced by a resistance, and there is no need for a large decoupling capacitance. Only a single voltage measurement is taken. Other information about switching losses or voltage overshoot under realistic operating conditions
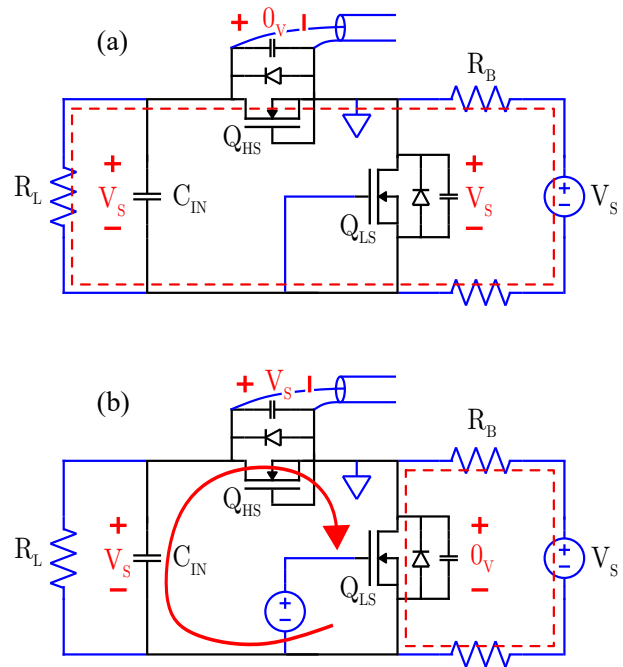

Fig. 6: Single pulse test circuit. The switching cell is shown in black, and connections to the circuit are shown in blue. Red lines indicate current flow for each state. (a) Q_{LS} is initally off and the measured voltage is zero, (b) Q_{LS} turns on and the V_{DS} of the high-side transistor rises to V_S with some overshoot and ringing.

cannot be extracted from this setup. The functionality is as follows.

1) Initially, Q_{LS} is off, and a small current flows from the supply through R_B, R_L, and the body-diode of Q_{HS} (or, as in the case of GaN transistors used here, reverse conduction). As such, the output capacitance (C_{OSS}) of Q_{LS} is charged up to the supply voltage and the V_{DS} of Q_{HS} is zero.
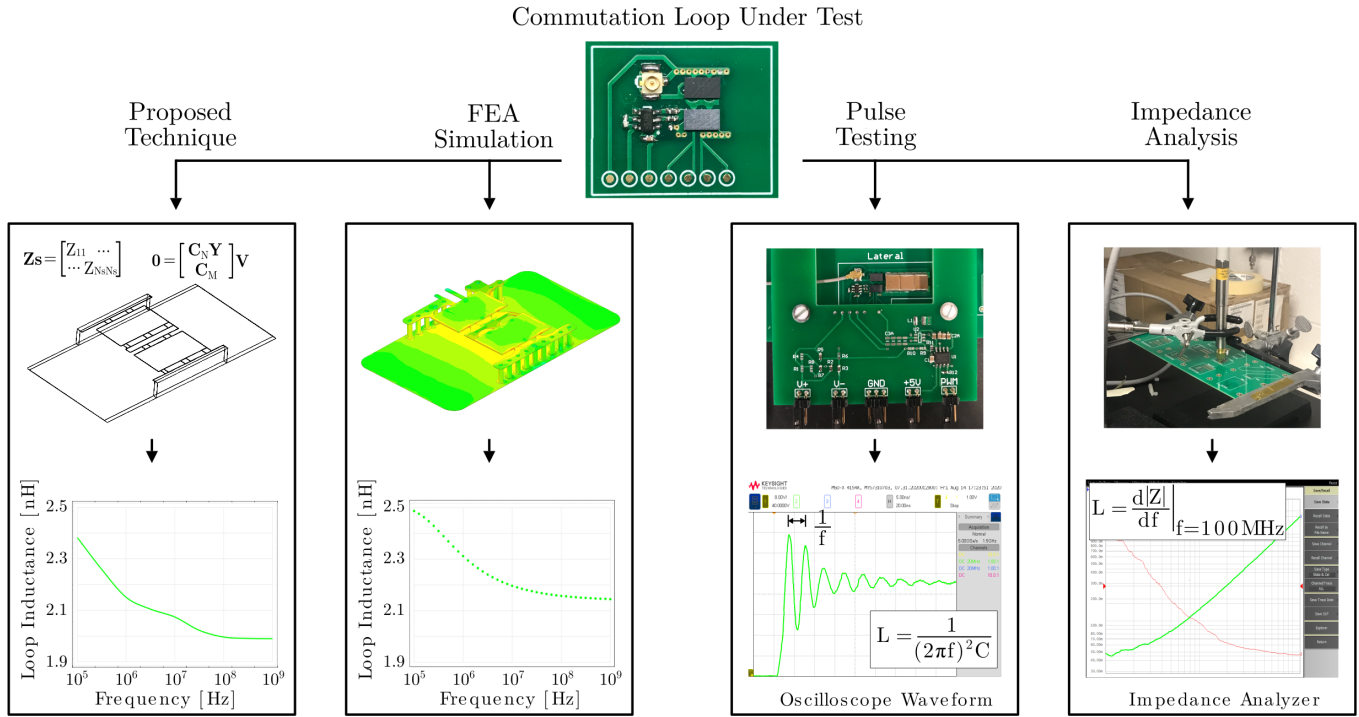
Fig. 7: Flow diagram illustrating various measurement techniques.

Table 1

Measured and Simulated Commutation Loop
Inductance @ 100 MHZ

Loop Type	Proposed Technique	FEA Simulation	Pulse Testing	Impedance Analysis
Lateral	4.71 nH	4.62 nH	5.15 nH	5.55 nH
Lateral w/ Plane	0.81 nH	0.93 nH	1.26 nH	0.87 nH
Vertical	2.00 nH	2.16 nH	2.41 nH	2.56 nH
Hybrid	0.45 nH	0.45 nH	0.83 nH	0.76 nH
FCML Hybrid	0.58 nH	0.60 nH	1.2 nH	.79 nH

Note: Pulse test frequencies depend on
resonance and range from 78MHz-225MHz

Fig. 8: Inductance across frequency for each of the loops.

2) Then, Q_{LS} is turned on, forcing its V_{DS} to zero. The C_{OSS} of the high-side transistor must then charge to the supply voltage. The resistors are chosen to have high impedance compared to C_{IN}, ensuring that the high-side transistor C_{OSS} is charged from C_{IN}. The parasitic inductance of this loop and C_{OSS} of the high-side transistor provide the only non-negligible series impedances, such that they determine the amplitude and frequency of the voltage overshoot.
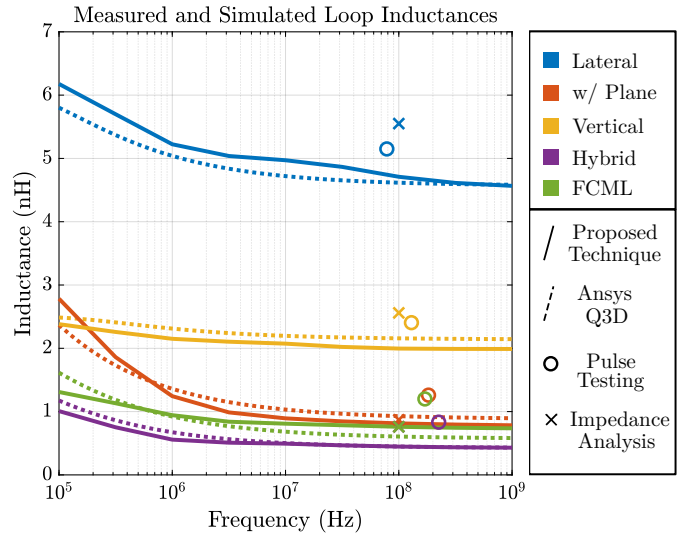
3) The ringing frequency in the voltage measurement is extracted and the value of C_{OSS} at the blocking voltage in the experiment is obtained from the device datasheet. From there, the inductance value can be computed as $L = 1/(2\pi f)^2 C$.

To ensure a reliable voltage measurement for this high-frequency waveform, a 1.5 GHz, 5 GSa/s, Keysight Infini-iVision MSOX4154A oscilloscope is used with 750 MHz N2894A passive probe. The connection is made with a uFL connector placed very close to the loop, which is run with

a coax cable directly to a uFL-to-probe-tip adapter. All of the other connections to the switching cell do not affect the measurement, and can be made with high-inductance paths. This 'single pulse test' extends prior work, providing a new half-bridge version of the design for FCML switching cells by [6].

A summary of these measurement techniques is shown in Fig. 7. The corresponding results are shown in Fig. 8. Table 1 summarizes the results at 100 MHz. The estimated inductance values by the proposed program were within 20% of FEA in all cases. The error is likely attributable to the approximation of each loop into straight, perpendicular segments, and discrete meshing of the conductors. The measured results show good agreement with simulation.

IV. Conclusion

This paper has presented a computationally efficient approach for estimating commutation loop inductance. Based on partial inductances, it is platform-independent and may be scripted into existing converter design and analysis programs. In addition, the effect of design choices such as stackup or component selection can be analyzed before fabrication. The mathematical technique is described and an implementation is created in MATLAB. The accuracy of the proposed method is compared to a commercial FEA simulation tool as well as measurements on multiple hardware prototypes. The results show reasonable accuracy, within 20% of FEA across all frequencies and commutation loop designs, and agreeing with hardware measurements.

V. Acknowledgments

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