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Microwave Power Limiters Exploiting the Insulator to Metal Transition of Lanthanum Cobalt Oxide

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Materials Science and Engineering

by

Rajashree Bhattacharya

2023

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Rajashree Bhattacharya

2023

ABSTRACT OF THE DISSERTATION

Microwave Power Limiters Exploiting the Insulator to Metal Transition of

Lanthanum Cobalt Oxide

by

Rajashree Bhattacharya

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2023

Professor Dwight Streit, Chair

The objective of this work is to leverage the unique insulator to metal transition of Lanthanum Cobaltite ($LaCoO_3$, LCO) towards the next generation of power limiters for high temperature, wide bandwidth, and high-power operation. $LaCoO_3$ is a semiconducting perovskite that demonstrates a spin-state transition to metallic behavior about 500 K. In this

dissertation we establish a wafer-scale reactive sputtering deposition process, characterize the temperature-dependent properties of thin film LCO, and estimate the thermally driven band gap collapse by near-IR absorption measurements.

The aforementioned sputtering process was used in the fabrication of power limiters that can be triggered either by external DC bias or by self-turn on at an input power threshold around 16 dBm. We present a 2 GHz LCO-based shunt power limiter constructed on silicon carbide with continuous wave power handling capability of 40 dBm, flat leakage of 20 dBm, and insertion loss less than 1 dB over a broad operating temperature range of 10 °C to 75 °C. Furthermore, very high temperature limiting response is recorded up to 225 °C with a flat leakage of 15 dBm and power handling up to 33 dBm. LCO limiters of varied dimensions and geometries were studied to better understand the necessary tradeoffs in design for low insertion loss and high-power handling. To that end, a 3D COMSOL Multiphysics simulation was also developed that accurately predicts limiting performance and switching speed. This model is used to propose further improvements to the power limiter design.

S-parameter testing was conducted from 0.1 to 50 GHz, verifying the broadband viability of LCO microwave devices. We present extremely low small signal losses, with a maximum insertion loss of 1.2 dB at 125 °C and 50 GHz. Benchmarking against both recent research art and commercial products indicates that LCO is a strong candidate for the next generation of microwave power limiters. Finally, we conclude the thesis with an evaluation of an LCO-based series radio frequency switch fabricated on sapphire substrate. We further summarize and discuss the significant potential of LCO in a wide range of thermally or electronically driven switching applications.

The dissertation of Rajashree Bhattacharya is approved

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University of California, Los Angeles

2023

DEDICATION

For Raja and Swetha Bhattacharya, with love and gratitude for all you gave

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PRESENTATIONS AND PUBLICATIONS

1. R. Bhattacharya, V. Gambin "Influence of crystallinity and stoichiometry on the high temperature semiconductor-metal transition of lanthanum cobalt oxide deposited by reactive dc sputtering" *Materials Science in Semiconductor Processing,* vol. 163, p. 107595 (2023)

2. R. Bhattacharya, A. Khanna, B. Bosworth, N. Orloff, V. Gambin, D. Streit, P. Fay, S. Datta. "Thermally Resilient Microwave Switch and Power Limiter based on Insulator-Metal Transition of Lanthanum Cobalt Oxide", *2022 International Electron Devices Meeting (IEDM)* (2022) 70–73.

3. R. Bhattacharya and V. Gambin, "LaCoO3 THIN FILM DEPOSITION BY DC METAL CO-SPUTTERING," U.S. Patent Filing 20220364219A1, May 12, 2021 (Patent Pending)

4. M. Islam, C. Perez, R. Bhattacharya, S. Wahid, T. Brown, Matthew Marcus, H. Ohldag, V. Gambin, S. Kumar, E. Pop. "Physics of Resistive Switching in LaCoO3 Revealed by X-Ray Absorption Spectromicroscopy" *Materials Research Society Spring Meeting 2023* (Oral presentation)

5. R. Bhattacharya, V. Gambin. "Materials Characterization of LaCoO3 Grown by Optimized Reactive DC Magnetron Sputtering" *64th Electronic Materials Conference 2022* (Oral Presentation)

6. R. Bhattacharya "New Materials for Fuses that Work in Space" *UCLA GradSlam 2022* (Oral Presentation)

7. R. Bhattacharya, V. Gambin. "Material characterization and contact resistivity of LaCoO3 grown by optimized DC magnetron sputtering" *ACerS Electronics Materials and Applications Conference 2022* (Oral Presentation)

8. R. Bhattacharya, V. Gambin. "$LaCoO_3$ as an insulator-metal transition material for RF Power Limiters" *Northrop Grumman Basic Research Seminar 2021* (Oral Presentation)

Chapter 1: Background and Motivation

1.1 Introduction to Radio Frequency Power Limiters

As our society grows increasingly dependent on wireless communications, having a robust satellite network is crucial. Malicious high power microwave signals can reach peak powers of 1 gigawatt and can easily cause irreversible damage to the sensitive components of receiver technology. Particularly for applications in GHz and THz frequency ranges, there is a growing need for advanced protection circuitry to defend against electronic warfare. Power limiters are front-end non-linear devices that prevent incident signal above a certain power threshold from passing, thus protecting downstream devices such as Low Noise Amplifiers (LNAs) that can typically only handle up to 20 dBm (100 mW). These components are typically arranged in receiver circuitry as depicted in Figure 1.1, ideally turning on well before the failure point of the LNA or other downstream components. The first block in Figure 1.1 (a) represents a bandpass filter, which narrows incoming signal to desired frequency bands. The limiter itself is then specifically designed to work within the frequency band with low insertion loss for the desired signals of sub-threshold power magnitude. We refer to a shunt-configuration limiter as being in the OFF state in the "normal operation" zone when signal is passing. At a given threshold input power, the device will transition to the ON state, or "limiting" range of operation (Figure 1.1(b)). Limiters can be designed to function both passively (self-activation from input signal) or actively (external turn-on via DC bias).

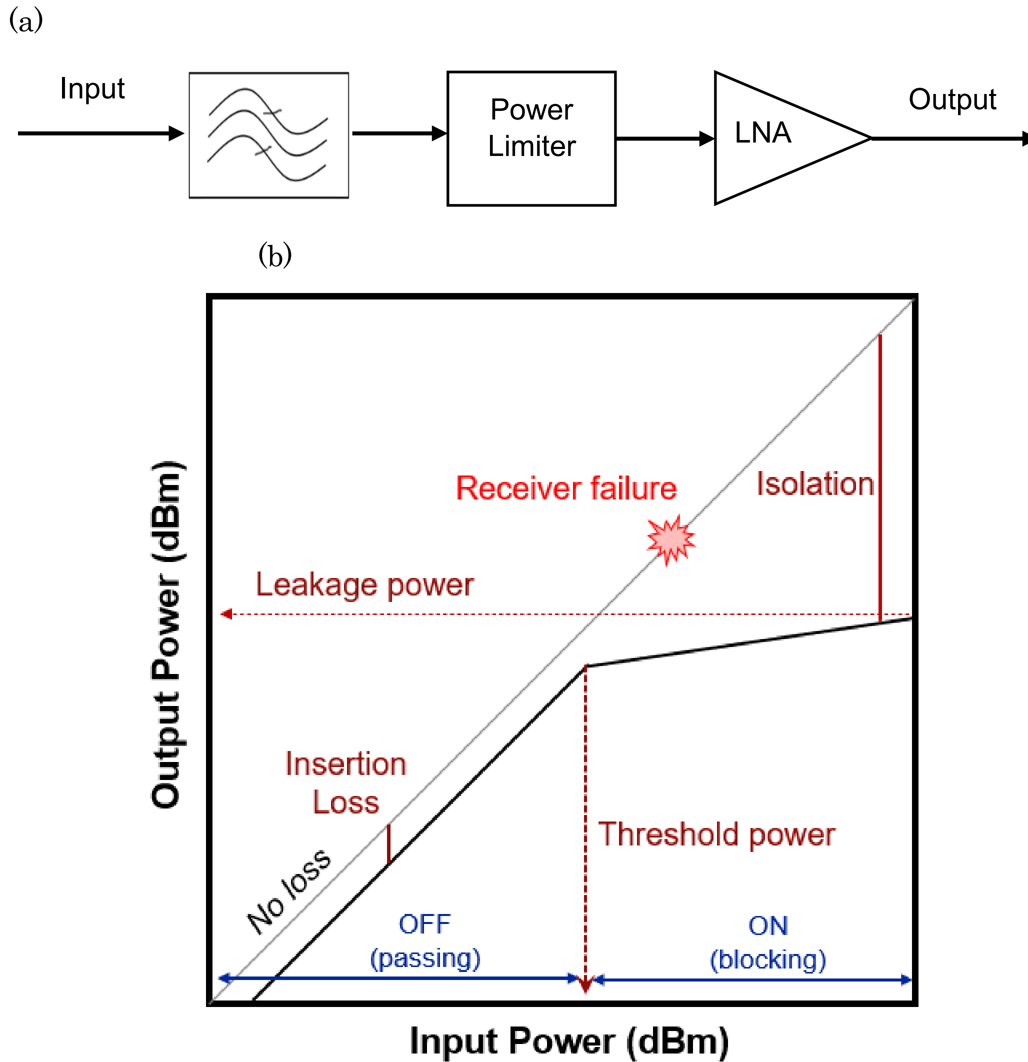


Figure 1.1 (a) typical positioning of a power limiter in receiver line. (b) targeted limiter attenuation input power response.

1.1.1 Metrics of Limiter Performance

There are many performance metrics for power limiters, including but not limited to 1) insertion loss 2) power handling and endurance 3) response time 4) frequency band 5) isolation and 6) environmental compatibility. Units of measurement of gain are denoted as dB. Magnitude of power (dBm) is defined in reference to 1 mW. The defining equations are:

$$dB = 10*\log_{10}(P_1/P_2)$$

$$P_{dBm} = 10*\log_{10}(P_{watts}/1\ mW)$$

Insertion Loss:

Insertion loss refers to the signal loss or signal attenuation through the limiter in its OFF state and is defined as the ratio of powers from input to output in dB. The ideal limiter demonstrates zero insertion loss. However, most real-world devices perform between 0.2 to 1.5 dB loss. Because a major source of insertion loss is parasitic capacitance, it typically worsens at high frequencies.

Power Handling:

Peak power handling refers to the maximum one-time surge a limiter can handle before irreversible damage occurs, reported in dBm. Endurance of a limiter's function over time is also important, as even repeated bombardment by pulsed attacks below the peak power handling value has been known to gradually damage components. In this dissertation we describe continuous wave power handling characteristics, referring to the ability of components to survive sustained input signals applied for at least 100 microseconds.

Response Time:

If the input RF pulse has a faster rise time than the time for the limiter to transition to the ON state, some amount of RF power will get through and is called spike leakage. State of the art limiters respond in nanoseconds to block incoming signal, and the faster the response, the better the limiter's protection. Limiters must also be able to recover quickly to the OFF state after dangerous signal has been blocked. The scale of recovery times is typically in the hundreds of nanoseconds to micro-seconds.

Frequency Band

The ideal limiter has the same behavior across all frequency bands. Realistically, limiters must be optimized for small capacitance to avoid low shunt impedance in the OFF-state white maintaining high attenuation in the ON state with low frequency dependent

response. In this research we focus on the microwave regime, testing devices from 0.1 GHz to 50 GHz. This range, for example, includes such common consumer applications at 2.4 GHz such as cordless telephones, Wi-Fi, and Bluetooth. The X and K_a bands, from 8-12 and 26.5-40 GHz respectively, are often allocated for satellite communications, military aircraft, space telescopes, defense tracking, and air traffic control.

Isolation/ Flat Leakage

Isolation is the measure of attenuation of the limiter and is calculated the same as insertion loss, just for the device in its ON state. Maximum isolation is defined as the greatest attenuation measured for the device at the highest input power, reported in dB. Higher isolation is considered better performance. Flat leakage, in dBm, refers to the output power of the device in the limiting operation. Most limiters do not exhibit the ideal, a truly flat limiting performance, but instead the leakage will slope upward as input power increases.

Environmental compatibility

Satellites must perform efficiently within the harsh conditions of outer space. Power limiters must be robust at extreme temperatures, pressures, and against the onslaught of solar and cosmic radiation. The standard operating temperature rate of limiters is typically from -50 °C to 85 °C, sometimes up to 150 °C [1]. Reported metrics of performance such as insertion loss or isolation often include temperature dependence in units of dB/ °C.

1.1.2 Current Art

The conventional form of solid-state power limiter is the P-I-N diode, based on silicon. At the DC and low frequency limit, P-N and P-I-N diodes behave similarly. But the intrinsic region can store charge, and at radio frequencies, may not have time to completely deplete. This allows the flow of RF signal through a P-I-N diode. The thickness of the diode's intrinsic region determines the threshold power for switching and can also be influenced by DC bias.

Below the threshold power, a P-I-N diode will produce a large impedance. When placed in a shunt configuration to the RF transmission line, this will result in low insertion loss. As the input power increases, however, carriers are pushed into the I-region, flooding the layer. Within nanoseconds, DC current is shunted through the loop formed by the diode and the return RF choke. Thus, input signal is blocked by either reflection back to the source or shunt to ground. However, the effectiveness of P-I-N diode limiters drops off at higher frequencies (Figure 1.2(a)), where power handling, response time, and leakage tradeoffs become an issue.

(a)

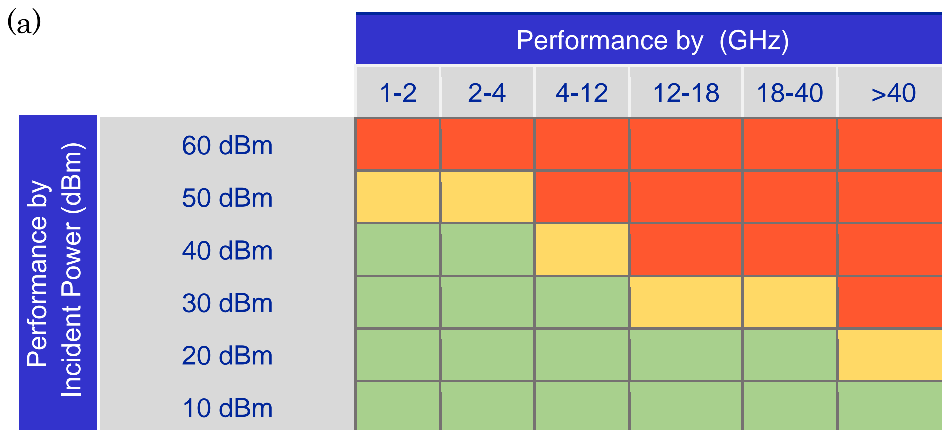


Figure 1.2 an illustrated review of P-I-N diode limiter performance, based on available products from one vendor, Microsemi [2]. The graphic highlights the typical constraints of commercial silicon P-I-N diode limiter function as a function of peak power and frequency. Green indicates good performance, red indicates poor or limited functionality

Power handling of limiters is directly related to their efficiency at dissipating power and avoiding damage. One mechanism for the P-I-N diode failure was detailed by Zhao *et.al.* [3], who demonstrated by microwave pulsed power tests that even 20 pulses of 2.5 GHz 63 dBm (~2 kW) input power can drastically deteriorate the insertion loss of a commercial diode designed for GHz operation. The P-I-N diodes show signs of ablation at the metal electrodes well below the material's melting temperature. The damage accumulation is attributed to ablation burn-out of first the I-region, then the N+ region above 600 pulses. One method of improving on this form of power failure would be to increase the size of the diode. However, this introduces response delays, increased spike leakage, and greater power consumption [4].

Additionally, if trying to reduce the thickness of the I-region to improve speed, parasitic capacitances arise that worsen high frequency insertion loss (capacitance=k εA/d). Thus, there is simply a material constraint in the use of traditional diodes for receiver protection, and the next generation of power limiters will have to look elsewhere.

While for the most part the commercially available power limiter is still the traditional Si diode, several alternate constructions have been recently emerging to tackle silicon's weaknesses. For one, GaAs-based diodes have acquired attention for high frequency operation. In general, a multi-stage design has thus far been required to approach the performance standards of a single-stage Si P-I-N diode. One group demonstrated a 4-stage GaAs P-I-N diode limiter with excellent 13 dBm flat leakage performance, under 1 dB insertion loss, and power capacity of 40 dBm [5]. Other novel materials for diode-based limiters are also on the horizon. For example, the high thermal conductivity and high breakdown field of diamond suggests improved power dissipation and power handling capabilities. A p-type diamond Schottky diode has been recently tested in a multi-stage limiter configuration, demonstrating operation up to 50 dBm, with a flat leakage of 27 dBm. The technology has only been reported at 1 GHz, though research is on-going [6]. While a multi-stage limiter is certainly a viable commercial option as well as single-stage, a smaller form factor and simpler construction is often desirable for greater signal sensitivity.

Other alternates to P-I-N diodes include the usage of high-power HEMT switches on AlGaN. Non-diode designs of power limiters also include gas-ionization based plasma limiters and micromechanical systems (MEMS). Plasma limiters work by using high power to ionize an inert gas discharge tube, thus allowing the power to dissipate, or be absorbed into the gas. While they have exhibited impressive power handling and frequency response, plasma limiters are constrained by recovery time and insertion loss [7]. Further, when the gas breaks down, ions are driven across the discharge gap and bombard the electrodes, which can lead

to surface degradation over time [8]. MEMS switches can be actuated by thermal gradients or electrostatic fields and have recently achieved impressively low insertion losses below 0.1 dB with broadband response [9], but continue to suffer from reliability issues. The small moving parts in MEMS devices are highly sensitive to environmental effects such as vibration and acceleration as well as contact fatigue from deformation and melting [10,11].

1.2 "Smart Materials" and the Insulator to Metal Transition

Transition metal compounds that exhibit unusually rapid, reversible changes in conductivity as a function of temperature (a.k.a Insulator to Metal Transition, IMT) may present a new pathway to construction and a solution to the current constraints in limiter technology. Emerging technologies based on these "smart" materials can potentially achieve very high endurance and higher power handling.

In traditional band theory, a fermi level in a band gap leads to insulating behavior, and a finite amount of energy is required to excite an electron to the next highest accessible orbital to carry electric current. Band theory fails when other effects such as electron-electron interactions within orbitals or disorder cause unpredicted electron localization. A classic example is NiO. NiO would be a metal according to traditional band theory due to its partially filled 3d band, but it is in fact insulating. Mott and Hubbard proposed complementary explanations for the phenomenon. In the Hubbard model [12] of periodic potential systems, Coulombic electron repulsion potential (U) prevents hopping from one atomic (or molecular) orbital to the next. This allowed that even in the case of one electron per lattice site (half filling), localization would cause insulating behavior. The Mott transition [13] describes that at a critical carrier density (increased by doping or temperature), electrons flood the conduction band and charge screening allows for delocalization and metallic conduction. In a Mott insulator, the band gap is formed between like orbitals (eg. 3d-3d), as opposed to

traditional valence/conduction bands formed by the energy difference between two spatially distinct orbitals (eg 2s-2p) or electron-periodic potential interaction. Unlike the Hubbard model, the Mott model is more general and does not require long-range order. For further distinction from other mechanisms, an Anderson insulator is based on electron-disorder interaction, and a Peierls insulator has a band gap based on electron-lattice deformation interaction. Theoretically, the Mott transition is first order and purely electronic. In reality, competing mechanisms and defects can often slow the transition or cause hysteresis.

1.2.1 Vanadium Dioxide

There are many materials that exhibit the IMT transition; by far the most thoroughly studied is Vanadium dioxide (VO_2). VO_2 exhibits a first-order nano-second phase transition (high-temperate rutile to low-temperature monoclinic) at around 68 °C with high reversibility in conductivity and optical transmission in the near IR regime. The transition mechanism for VO_2 is Peierls-assisted Mott-Hubbard– the structural transition at 68 °C creates a lattice distortion and enables the injection of carriers into the conduction band. This screens repulsion and leads to electron delocalization and metallic behavior [14]. Given the strong dependence on lattice quality and periodicity, the magnitude and hysteresis of the VO_2 IMT is highly sensitive to deposition condition, crystallinity, and substrate. The best reported VO_2 thin film achieves a four-order of magnitude on/off ratio when epitaxially grown on sapphire. In contrast, single crystal VO_2 can demonstrate five orders of magnitude. VO_2 also sees a significant drop in the on/off ratio for polycrystalline films over epitaxially grown materials, and easily devolves into other phases with slight off-stoichiometry [15,16]. Despite these challenges, VO_2 has been heavily studied for a wide variety of novel devices including switches (2 and 3 terminal), optical devices, chemical sensors, thermal sensors, oscillators, and mem-resistive devices [16].

VO_2 Power Limiters

In 2010, Givernaud *et.al.* [17] presented a microwave power limiter constructed from 250 nm of VO_2 grown on sapphire. They used strips of VO_2 to fill the gap between the signal and ground lines of a co-planar waveguide Figure 1.3 (a). They reported RF-power triggering of the transition where above a certain power threshold, the VO_2 switched to a metallic state and highly attenuated the input signal. The threshold power of the device could be further reduced by application of voltage-controlled DC bias up to 22 V. The highest substrate temperature that Givernaud *et.al* reported switching the limiter was 50 °C (Figure 1.3 (b)). The article also outlines several multi-stage configurations and verification of broadband low insertion loss up to 40 GHz.

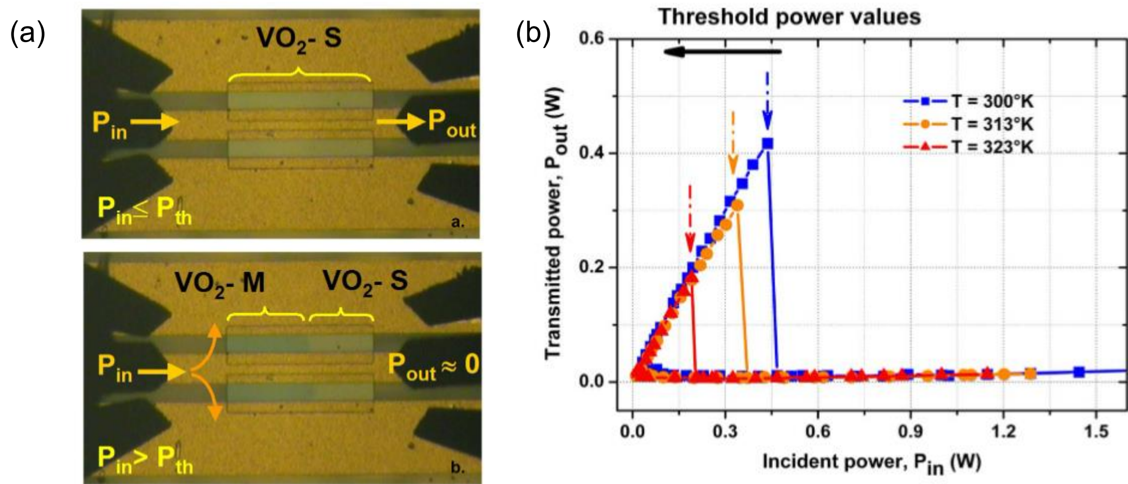


Figure 1.3 (a) microscope image of a vanadium dioxide-based power limiter with (b) demonstrated self-turn on limiting behavior at 10 GHz and up to 50 °C as reported by [17] © 2010 IEEE

In 2018, Nordquist *et.al* [18] reported a similar planar shunt limiter based on thin-film VO_2 on SiO_2. This film achieved a resistance on/off ratio of 500 when measured at 40 °C and 100 °C by the four-point probe method. A tapered geometry was utilized to enable higher power handling, with repeatable operation up to 47 dBm. A summary of the VO_2-based RF limiter performance is shown in Table 1.1.

Table 1.1: Prior Work in IMT-based Power Limiters based on Vanadium Dioxide

Insertion Loss (dB)	Power Threshold	Isolation (dB)	Test Frequency	Test Temperature	Structure	Source
0.6	20-30 dBm	26	10 GHz	25-50 °C	co-planar waveguide	[17]
0.7	36 dBm	27	2 GHz	25°C	tapered	[18]

In a similar vein of research, a free-space millimeter-wave photonic limiter based on nano-layer VO_2 has very recently been reported for W-band function [19]. Polycrystalline VO_2 was grown on a large area of sapphire substrate and presented with RF signal at 95 GHz and up to 60 W. Due to low absorbance of the signal into the film, neither significant self-heating nor self-turn-on was observed at room temperature even when presented with the maximum power. When the ambient temperature was raised closer to the critical transition of VO_2, self-turn on was observed starting at 30 W and the device showed maximum isolation of 20 dB at ~47 dBm. Only a very slow switching time of 7 seconds was achieved in this proof-of-concept device [20]. It is worth noting that this photonic limiter was not designed to be positioned along the transmission line but instead to provide a wide area of protection, so the expectations of performance would be different.

Despite these developments, ultimately VO_2 power limiters devices are impractical. High on/off ratios are only achievable for films grown on sapphire substrate, restricting integration avenues. Furthermore, operational guidelines for many military and satellite applications requiring operation up to at least 85 °C because of the self-heating caused by high power shunting and the difficulty of cooling systems without convection in space. With VO_2's transition occurring below that point, the high temperature operation is thus constrained, and it has become necessary to look at other potential IMT materials.

1.2.2 Lanthanum Cobalt Oxide

A graphic with extracted values from [14] displays the resistance on/off ratio of various IMT materials as a function of their switching temperature (Figure 1.4 (a)). Clearly, for

higher temperature device operation, the next choice after VO_2 would be Lanthanum cobalt oxide ($LaCoO_3$, LCO). It is worth highlighting that the figure assembled does not clarify the broad transition profile that makes $LaCoO_3$ distinct from VO_2, which is then displayed in Figure 1.4 (b). This can provide both a benefit and a challenge. Without the sharp transition seen in VO_2, LCO-based devices must be carefully designed to enable reasonably fast switching speed. However, the broader transition temperature range can also allow LCO devices to access a wide operating range with minimal loss in functionality.

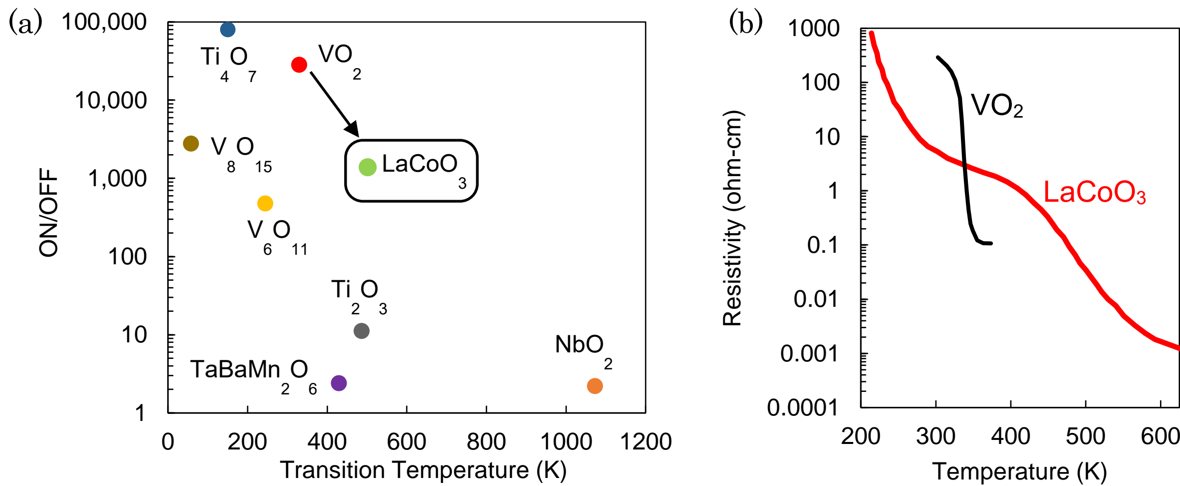


Figure 1.4 (a) compilation of resistance drop ratios for known IMT materials [14] (b) comparison of transition profiles for bulk $LaCoO_3$ and polycrystalline VO_2 [21,22]

$LaCoO_3$ is a perovskite previously most researched for catalytic applications and as a cathode in solid oxide fuel cells. It has a stable rhombohedral structure up to 1698 K, at which point it becomes cubic. The ideal cubic perovskite cell is structured as FCC-based, with oxygens at each face center, A-site ions at each corner, and B-site cations at the center of the cell (Figure 1.5 (a)). In LCO's slightly distorted R3C structure, the (100) planes are shifted diagonally to give one angle of 120° and lattice constants of 5.44 Å, 5.44 Å, and 13.13 Å. The pseudo-cubic LCO structure, assuming all angles are 90°, has lattice constant of 3.82 Å.

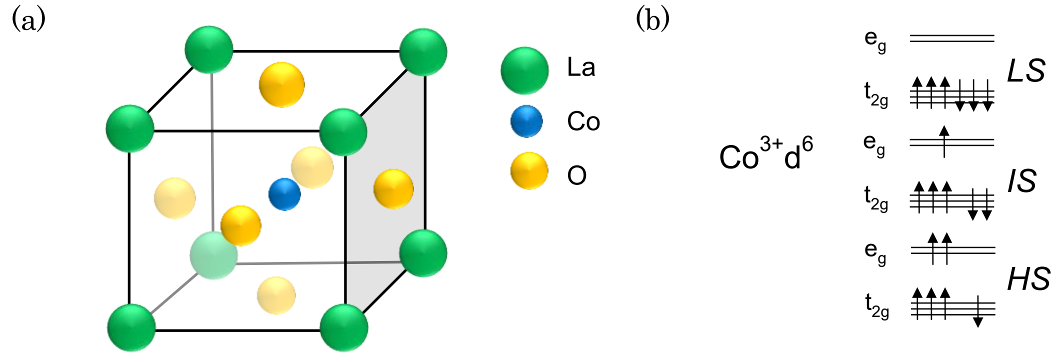


Figure 1.5 (a) Pseudocubic perovskite structure for $LaCoO_3$ (b) progression of the Co^{3+} spin state transition from Low Spin S=0, to Intermediate S=1, and High Spin S=2. The consensus is that the LS state exists below 100 K, and HS metallic state far above 500 K. However, the temperature transition boundaries and spin states' relative stability remain under debate. [23]

The cobalt ion in $LaCoO_3$ holds the key to its spin state insulator to metal transition, which is similar to a traditional Mott transition. One can understand why the transition profile is so gradual by considering a two-stage transition. Below 35 K, LCO behaves as a nonmagnetic insulator where the cobalt lies in the low spin ground state (LS, $^1A_1$, $t^6{}_{2g}$ $e^0{}_g$) with a band gap estimated at 1.5 eV. With temperature, the cobalt eventually shifts to the high spin fully metallic state (HS, $^5T_2$, t_{2g} $4e_g{}^2$) at some point above 500 K. Originally Goodenough *et.al.* proposed a LS-HS transition of based on Co (III) crystal splitting energy being only slightly larger than the exchange energy and electron repulsion, which mimics the makings of a Mott-Hubbard insulator [24,25]. In that original model, the mixed LS-HS phase between 100 K and 500 K provided semiconducting behavior. However, this model served insufficient to fit the magnetic susceptibility and thermal expansion properties of LCO, and was later updated to include an intermediate spin level (IS, $^3T_1$,t_{2g} $^5e_g{}^1$) [26–28]. There continues to be discussion and disagreement about the exact mechanism for the transition. The low spin state of Co^{3+} is a highly symmetric octahedron. There may be significant stabilization of the orbitally ordered IS state by Jahn-Teller distortions. This orbitally ordered state formed by the hybridization of Co e_g and O 2_p orbitals may then "melt" around 500 K, giving rise to metallic conduction, and the HS state (which is not JT active) could then

be occupied at higher temperatures above 800 K [28–31]. However, other groups counter this model, stating that there is a 3-stage LS-IS-HS transition, with the HS state beginning population and overtaking the stabilized IS state at the semiconductor-metal transition [27,32]. Even others reject the importance of the IS state altogether [33], offering that while it does exist (and thus shows up in Raman spectroscopy results), the LS-HS state crossover is the primary mechanism of transition, with no temperature region seeing domination by IS. They suggest that the short-range LS-HS order of the semiconducting region melts and leaves space for IS-HS coexistence at around 500 K and a Mott-like transition [34–36]. Based on the results of this work, we suggest that the spin state transition of LCO does not demonstrate the homogenous thermal transition with a critical carrier concentration as characteristic of a thermal Mott insulator. Instead, with increasing temperature, conductive HS clusters grow in an entropy driven transition as supported by other researchers [37,38].

For thin film LCO, it has been shown that the spin-state transition can be regulated by deliberate distortion of CoO_6 octahedron by strained epitaxial growth. For example, LCO has previously been epitaxially grown on (100), (110), and (111) lanthanum aluminate ($LaAlO_3$, LAO) substrate [39]. Of these, the (100) orientation best supported the Jahn Teller distortion by forcing the greatest elongation of Co-O bonds, leading to higher intermediate state population at lower temperatures and thus most likely the earliest transition to the metallic state.

Previous work in $LaCoO_3$ electronic switches

Despite all the debate over the mechanism of this electronic shift, practical application of $LaCoO_3$ in an electronic switch had scarcely been explored before the inception of this project, conducted in cross-collaboration between the University of Notre Dame (UND), the Northrop Grumman Corporation (NGC), and University of California, Los Angeles (UCLA).

Initial evaluation of LCO for use in electronic switches was conducted at UND using epitaxial material grown by molecular beam epitaxy [21] on Lanthanum Aluminate (LAO), a perovskite substrate with only -0.8% mismatch. As expected, the magnitude of the epitaxial film's transition was reduced compared to bulk material (3000x to 780x). This has been characterized previously by groups that show that epitaxial strain prevents population of the LS state at lower temperatures, thus reducing resistivity overall [40–43]. This epitaxial material was subsequently investigated for memory-selectors in 3D cross-point architecture [44]. LCO was fabricated into 2-terminal switches, and current-voltage sweeps demonstrated abrupt switching up to 125 °C. Voltage applied over a thin strip of LCO will trigger the switch to conductive state for small resistive domains. As each individual domain switches, the total current pushed through the material increases, the temperature increases by Joule heating, and a cascading effect allows for fast turn-on times of 20 nanoseconds. Scaled devices exhibited high endurance with minimal drift up to 10^{10} cycles.

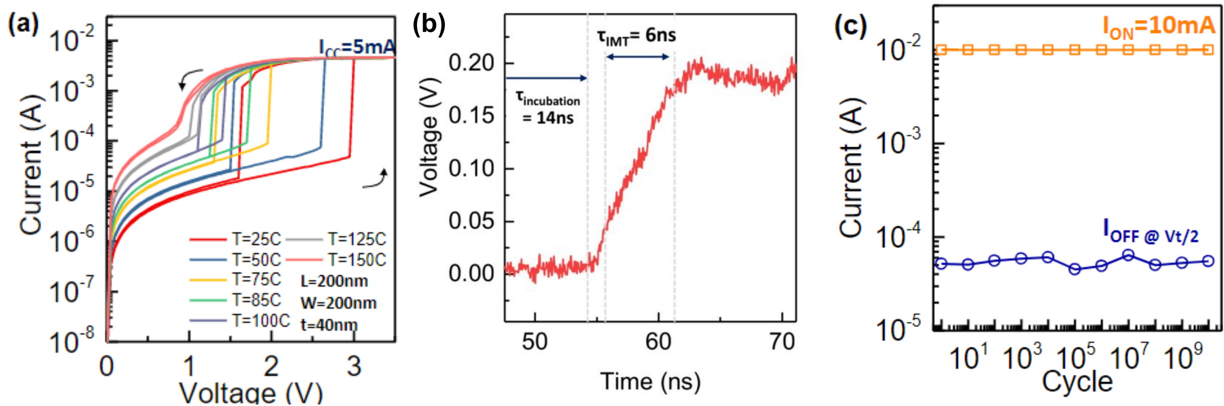


Figure 1.6 (a) I-V sweeps of 200 nm x 200 nm LCO 2-terminal device areas exhibit abrupt switching from 25 °C to 125 °C (b) Pulsed DC measurements at V_{in}= 3 V are used to measure turn-on times. A 14 ns incubation delay time is followed by 6ns for the IMT transition (c) Repeated I-V sweeps demonstrate consistent non-linearity up to 1010 cycles. [44], all graphics reprinted with permission, © 2020 University of Notre Dame

Researchers at UND also fabricated prototype LCO RF switches (normally blocked, turns-on to pass signal) based on the MBE-grown material [44]. They demonstrated the

ability to control the passing of RF signal through both temperature and DC-bias up to 50 GHz. The RF switch showed insertion loss of 3.2 dB in the on-state, 15.2 dBm isolation in the off-state at 20 GHz, and a cut-off frequency of 0.55 THz. Performance was similar across 25 °C to 125 °C, supporting our hypothesis on the potential broad operating range of LCO-based mm-wave switches.

1.3 My contribution to the field

Through the valuable efforts of my predecessors in this field, $LaCoO_3$ has been shown to possess the switching characteristics (speed, high temperature stability, endurance) that make it a promising candidate for power limiters. However, previous LCO deposition methods were not conducive to wafer-scale production or larger scale testing. Molecular beam epitaxy is a slow (0.2 nm/min) and non-economically scalable process with only a small central area of the lattice matched substrate, LAO, available for fabrication. Furthermore, the high dielectric constant of LAO (k=25) led to parasitic capacitances and high loss in the RF switches. Therefore, there was strong interest in depositing LCO onto a high thermal conductivity, low dielectric constant substrate such as silicon carbide (SiC). One objective of this project is to fulfill the need to deposit at wafer-scale on alternate low-k substrates. Additionally, in this research I have demonstrated the fabrication of RF limiters based on the sputtered LCO material. We have engaged in optimization of performance metrics such as thermal stability, insertion loss, frequency response, and power-handling through variations in device geometry. I also built a highly accurate COMSOL model to aid in the simulation of the influence of various device parameters. The following is the outline of each chapter of results of this thesis.

In Chapter 2, I report on the development of a reactive sputtering process of both polycrystalline and epitaxial $LaCoO_3$. Thin-film material characterization and estimation of the temperature-driven band gap collapse of the sputtered films is also presented.

Chapter 3 expands upon 2-terminal DC bias triggered LCO switches collaboratively constructed with UND. Switches are fabricated and tested from sputtered LCO material grown at NGC. This chapter also presents the introduction of our transient Multiphysics COMSOL model, with accurate prediction of both the magnitude, incubation delay, and switching speed of the voltage triggered IMT.

In Chapter 4, we present polycrystalline LCO-based shunt power limiters characterized by Power-in-Power-out (PiPo) experiments at 2 GHz. Various configurations are tested to evaluate design trade-offs on performance. I report on the progression of different failure modes as the limiters' geometry and operating temperature is changed, as well as proposed improvements to the most recent configurations with simulation-backed substantiation.

In Chapter 5, I further evaluate the aforementioned LCO power limiters at high frequency and temperature. S-parameter tests are conducted up to 50 GHz, and we demonstrate DC-bias external activation of the devices.

Finally, Chapter 6 includes the characterization of sputtered-LCO RF series switches. I summarize the work presented in this dissertation and discuss the potential future of LCO in other thermally or electronically driven applications.

Chapter 2: Deposition of Thin Film Lanthanum Cobalt Oxide

2.1 Abstract

Much of this chapter is reprint from the published article [45] © Elsevier 2023. Lanthanum cobalt oxide (LCO) has garnered growing interest in electronic switch applications based on its unique insulator to metal transition. A single-step high temperature deposition process was developed for thin film LCO *via* reactive dc magnetron sputtering, starting with exploration of target poisoning within the context of Berg's theory. By tracking target voltage on metal targets during reactive deposition, we reason that increasing inert gas flux to the target improves target hysteresis, thus increasing target lifetime. Furthermore, it is shown that the onset of the critical region of oxide deposition has a stronger dependence on reactive gas flow rate than on partial pressure. The critical region is found at approximately 1.5 sccm and 5 sccm oxygen flow rate for the La and Co targets, respectively. We subsequently probed substrate and stoichiometry influence on LCO film quality and electronic properties. Epitaxial (100) $LaCoO_x$ (Rq = 0.412 nm) films grown on lanthanum aluminate ($LaAlO_3$) demonstrate similar reductions in resistivity over 300 K to 623 K as polycrystalline LCO films on 4H-SiC and sapphire (Rq= 1.59, 2.36 nm respectively). However, La-heavy films, grown as $La_{2.6}CoO_{4.8}$, can demonstrate significantly steeper resistivity drops. Finally, we estimate the band gap collapse and insulator-metal transition of thin-film LCO over temperature by near-IR absorption.

2.2 DC Magnetron Sputtering

Magnetron sputtering is a vacuum physical vapor deposition process achieved by using magnets to confine an electron density that increases ionization rates. The resulting plasma strike that bombards a solid target thus ejects material towards a mounted substrate. Sputtering can be classified as DC or RF based on the power input. Typically, the inert gas

used is argon, and reactive gases such as oxygen or nitrogen are introduced into the chamber for compound films. The vaporized target materials and ionized oxygen gas react in the chamber and deposit on the surface of the substrate. Having many tunable parameters allows for a wide range of film growth options. Grain size can be influenced by substrate temperature; higher substrate temperature encourages higher surface mobility for the arriving atoms, thus leading to larger grains. High surface mobility also tends to lead to smoother films as concavities are filled during the deposition [46]. Post-annealing at high temperatures can also allow grain growth, but the gain is reduced due to the high activation energy of thermal diffusion for already condensed species. The growth temperature of the perovskite structure is above 600 °C, so LCO film must either be deposited at or above that temperature [47]. Working pressure also has an influence on film roughness and deposition rate, as a higher working pressure reduces the mean free path between ion collisions. This could reduce the kinetic energy of atoms that diffuse towards the substrate, leading to lower surface mobility and higher roughness, particularly if the applied target power was also low. The deposition rate can also be expected to reduce at higher working pressures. In general, at lower temperatures and higher pressures, one can expect to see rough or columnar growth, and lower pressure and higher substrate temperature will favor smooth crystalline films [48].

2.2.1 Berg sputtering theory

A well-known complication of DC reactive sputtering is the non-linear relationship between oxygen partial pressure and film composition. The formation of an oxide layer on the target surface itself, known as poisoning, can lead to charge build-up and arcing, which will damage both target and film. Operating near the critical oxygen pressure for one reactive metal is difficult due to the inherent instability of a reactive sputtering process; co-sputtering two metals in that region is therefore exceedingly challenging. Here, we characterize the

sputter behavior of the La-Co sputtering system in an oxygen-argon environment by cathode discharge voltage hysteresis experiments.

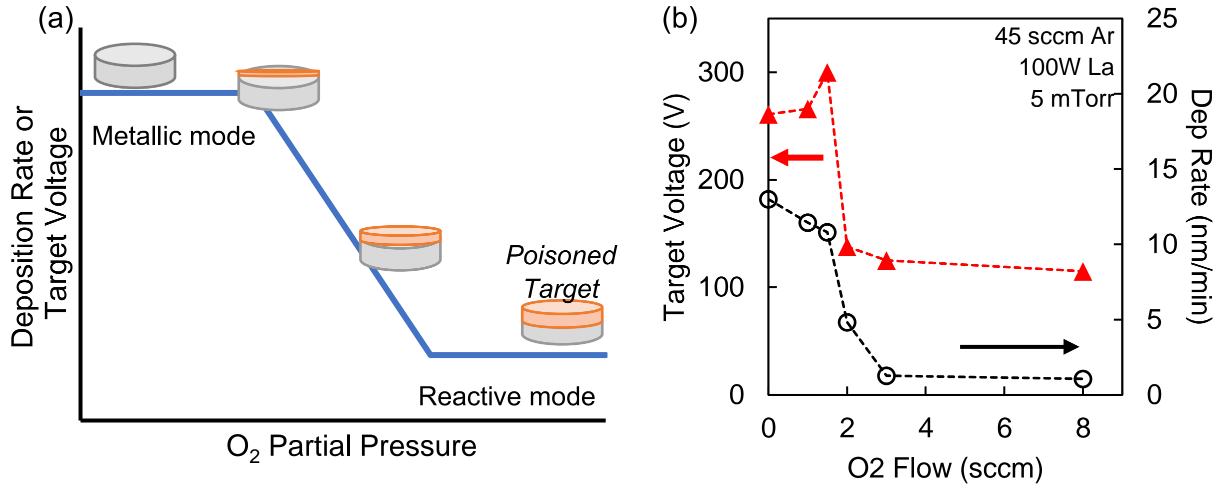


Figure 2.1 (a) non-linearity of reactive sputtering has similar effects on deposition rate and target voltage from the cathode. (b) Deposition rate (○) and target voltage (▲) as function of reactive gas flow rate for the La target at 100 Watts DC power. Dashed lines are provided to guide the eye [45]

The Berg model provides a simple reasoning for the reactive process non-linearity and hysteresis effect seen in reactive sputtering. The Berg model, with modification by Depla et.al, uses steady state equations to describe the mass balance of reactive gas flow [49]. The total reactive gas introduced to the system is equal to the sum of molecules consumed at the target, those exiting the chamber through the vacuum pump, and those that make it to the substrate to form a film. At the target, the gas can be consumed by either chemisorption at the surface or ion implantation by ionized molecules. At low oxygen flow rates, the system operates in metallic sputtering mode and can achieve high yield (high deposition rate), but the film will likely be oxygen deficient. As oxygen flux increases, it becomes harder to control the deposition rate as the target poisons. At a critical reactive gas flow where poisoning causes the deposition rate to drop sharply, the film is oxygen stoichiometric [50,51]. However, at the same time, oxygen partial pressure in the chamber spikes dramatically, as less target surface is available for reaction. Thus, further increasing the oxygen pressure could lead to

an overly oxygenated film and arcing target [52]. One method of actively tracking the target condition during deposition is the discharge voltage, $\boldsymbol{V_T = W/(q\gamma_e\, \epsilon)}$, where W is the average energy loss per ionization of the gas atom, $\boldsymbol{\gamma_e}$ describes the secondary electron emission yield, and epsilon is a probability value related to various possible energy loss mechanisms. Like deposition rate, the target voltage is roughly flat until the critical reactive gas flow rate and falls dramatically afterward. When the target is poisoned, the electron emission coefficient increases. There is a slight peak in voltage at the critical point that may be explained by the transition to the unaffected metal below the target's oxidized surface regions [49]. Discharge voltage hysteresis tests have been conducted for few other processes such as vanadium dioxide [53], and La-Fe co-sputtering [54], but not for the La-Co system. In this work, we determine the effect on target recovery of increasing the inert gas flow rate and co-sputtering reactive metals. We find a critical oxygen flow rate for a subsequent co-sputtering process that prevents both arcing and a prohibitively slow deposition process.

Results: Target Hysteresis

The sputter system used is an AJA Orion-8 fitted for 2" magnetron sources, equipped with 2 DC guns, one of which is capable of Pulsed DC operation. We conducted both individual and co-sputtered cathode voltage hysteresis tests for the La and Co metal targets in room-temperature processes. Power (La=100 W, Co=200 W) and overall chamber pressure (5 mTorr) were set constant. Argon flow was set to 20 sccm, and oxygen flow was stepwise increased from 0 to 12 sccm, at which point both targets could be expected to be well into the reactive mode. The target voltage was noted after it reached a steady value between each step (approximately 1 minute). Then, oxygen flow was stepwise reduced until the target was in a fully metallic mode. These hysteresis experiments were repeated at a higher (45 sccm) Ar flow rate.

In Figure 2.1 (b), the parallel influence of oxygen gas flow rate on target voltage and film deposition rate is depicted for the La target at 100 W DC power. We can clearly observe the expected simultaneous drop in both deposition rate and target voltage as predicted by Berg's theory on metal target poisoning. For metals, secondary electron emission is dominated by potential emission, or the ionization energy of the target material work function. On the other hand, for compounds such as La-O, emission is dominated by kinetic emission [49]. The sharp drop in target voltage in Fig. 1 corresponds with the rapid formation of a resistive oxygenated surface and thus an increase in the secondary emission coefficient γ_e. The poisoning of the Lanthanum target occurs at a relatively low oxygen flow rate, corresponding to the highly sensitive nature of this metal.

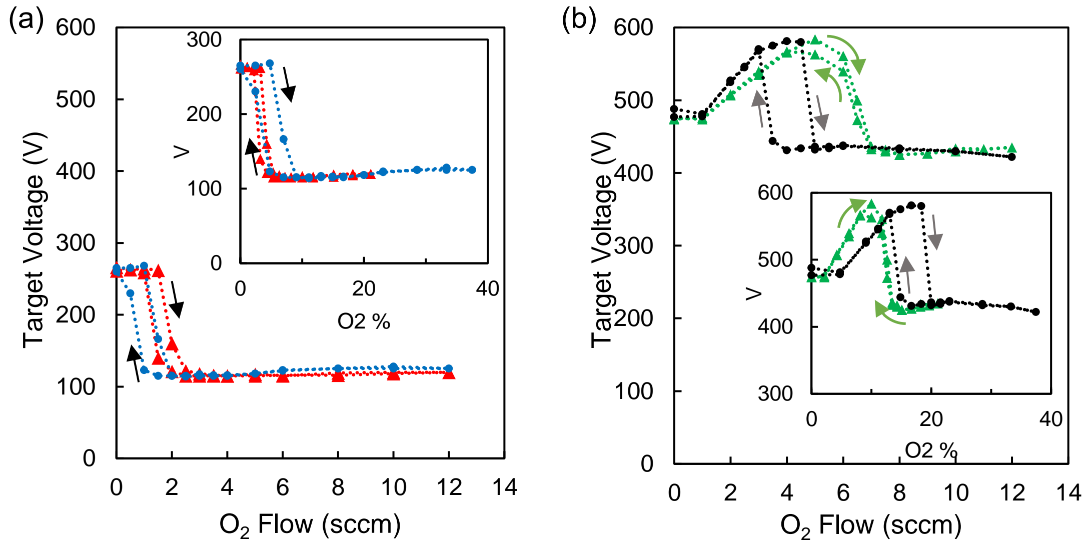


Figure 2.2 Target condition hysteresis as measured by target voltage as a function of reactive gas flow rate for (a) La target at 20 sccm Ar (●), 45 sccm Ar flow rate (▲). (b) Co target at 20 sccm Ar (●) and 45 sccm Ar (▲). Insets illustrate same data with x-axis converted to oxygen percentage [45]

The hysteresis of La and Co targets (when sputtered in isolation) is illustrated in Figure 2.2 (a-b). As expected for the Lanthanum metal target, the element is larger, more electropositive, and consequently more reactive with oxygen than Co. However, the oxide formed is surface-level – the low hysteresis effect on the La target indicates that most of the oxidized material is ejected from the target surface upon impact. Increasing the Ar flow rate

slightly pushes out the La critical point by further enabling ejection of any reactive species from the surface and thus keeping γ_e low for longer.

For the cobalt target sputtered in 20 sccm Ar, the voltage curve is characteristic of a less reactive metal target, with a peak in target voltage at a higher value, 4 sccm O_2. However, in contrast to La, Co shows strong target hysteresis upon reducing the oxygen flow rate, indicating deeper penetration of reactive species into the target. Increasing the argon flow rate serves to extend the critical region and greatly narrows the hysteresis curve. This indicates that higher argon flow rate, even as overall chamber pressure is held constant, limits formation of the oxide layer by continually cleaning the metal surface of the target. This effectively reduces the residence time of the reactive species and prevents deeper implantation. As this behavior is true both when data is plotted as a function of reactive gas flow rate or partial pressure, we infer that flux of gas particles is the controlling factor, rather than the ratio of inert to reactive gas.

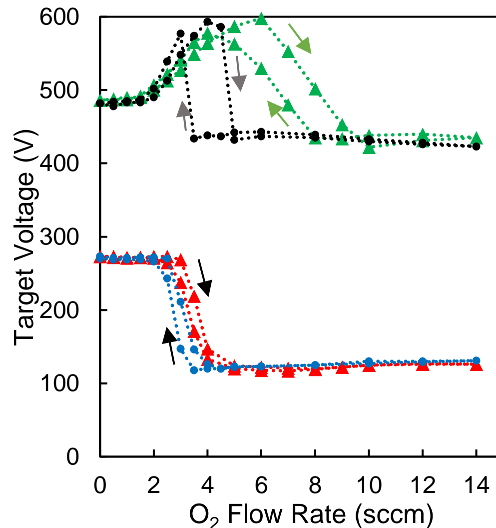


Figure 2.3 Target voltage as a function of oxygen flow rate for co-sputtering target hysteresis experiments and both high and low inert gas flow rate. For 20 sccm Ar, La target is indicated by (●) and Co target by (●). At 45 sccm Ar, La is depicted by (▲) and Co by (▲) [45].

In Figure 2.3, we demonstrate the influence of co-sputtering the La and Co targets on the target condition. Here, La and Co express similar hysteresis profiles to the independently

sputtered cases. However, at both low and high Ar flow rate, the reactive mode for Lanthanum when co-sputtered with Co starts at a higher oxygen flow rate. This implies that the Co target consumes some of the oxygen in the chamber, requiring a higher O_2 flux to oxidize the target. The shared consumption of inert gas flow in returning to a metallic state works to favor the La target to faster clean its oxidized surface and slightly reduce hysteresis, while simultaneously worsening the hysteresis on the Co target at high pumping speeds.

2.3 Film Growth

2.3.1 Methodology

The La target was installed in the pulsed DC gun to protect against arcing using 50 kHz pulses with 4 μs intermittent reverse biases to discharge the target. It is not expected that these short reverse bias times will have a significant effect on the deposition rate [55]. All films have been deposited at chamber pressures of 5 mTorr and on multiple substrates. $LaAlO_3$ (100) served as a closely lattice-matched substrate (a=3.787 A) with 0.9 % mismatch to LCO in this orientation. We also chose c-plane (0006) sapphire for transparency in the near-IR and visible regime for optical measurements of the LCO films. We additionally sputtered on 6-H (0006) silicon carbide, as it is a common substrate for high-power/high frequency switch applications. Fused silica was also tested, a thermally stable amorphous material also transparent in the near-IR regime, to study the properties of a non-crystalline LCO film. All substrates were prepared by rinses in acetone, isopropyl alcohol, and DI directly before being mounted into the sputtering chamber.

Gas flow rate, based on the results of the target voltage hysteresis experiments, have been set to 8 sccm O_2 + 45 sccm Ar. These settings ensure stable reactive processes with little run-to-run drift. We heat the substrate above the crystallization temperature of LCO (600

°C) and hold there for at least 30 minutes before deposition to ensure uniformity [47]. The composition of the films was controlled by varying the DC power on the La and Co targets.

The sputtered LCO films were characterized by several techniques. Film thickness was measured by a Bruker DektakXT® profilometry tool. X-ray diffraction (2 theta-omega) is used to determine crystallinity and texture. X-ray photoelectron spectroscopy was used to characterize composition after a 50 second argon etch to clean the sample surface. Atomic force microscopy (Bruker Dimension Icon ®) was used to image the film surface.

Temperature dependent resistivity was determined by four-point measurements. The four-point probe method allows for the elimination of contact resistance and is conducted by forcing current through two outer probes and measuring voltage across two inner probes. Resistivity is calculated as resistivity $\rho = 4.53Vt / I$, where t is film thickness in centimeters. The collinear sense and force probes were connected to the 4200A-SC Keithley parameter analyzer with 62.5 mil tungsten probe spacing. Ohmic contact is achieved on the bare film surface. Samples were heated by a Linkam HFS600E temperature control stage. The temperature was stepped from room temperature up to 350 °C and at each point the force current is set so that the positive and negative sense readings match within 2%. We define the IMT on/off ratio as $\rho_{25°C}/\rho_{350°C}$.

2.3.2 Influence of substrate

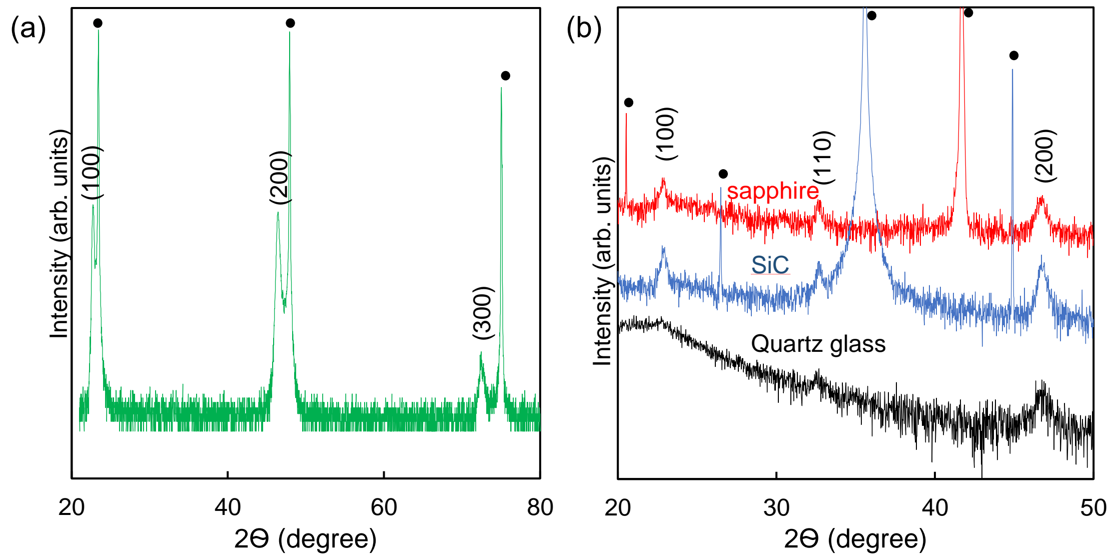


Figure 2.4 X-ray diffraction pattern for 150 nm $LaCoO_{2.7}$ film, epitaxially grown on (a) Lanthanum Aluminate and (b) sapphire, 4H-SiC, and fused glass. The substrate peaks are labelled with a ● [45].

Figure 2.4 (a) depicts x-ray diffractogram for a 150 nm $LaCoO_{2.7}$ film deposited lanthanum aluminate (LAO), indicating a highly textured epitaxial film grown oriented to the (100) direction. The out-of-plane lattice constant is estimated to be 3.91 Å by Nelson-Riley analysis. As the relaxed pseudo-cubic lattice parameter of LCO is 3.82 Å, this value aligns with the expectation of in-plane compression (out-of-plane expansion). In contrast, with their out-of-plane lattice constant calculated at 3.89 Å, the LCO films on sapphire and SiC (Fig. 4(b)), are more relaxed. Grown by Wolmer-Veber, or island, growth, the (110) peak of these films are also distinguishable in the x-ray diffraction pattern, indicating a polycrystalline, random orientation. On quartz glass the small peaks indicate a higher critical thickness for crystallization on the amorphous substrate.

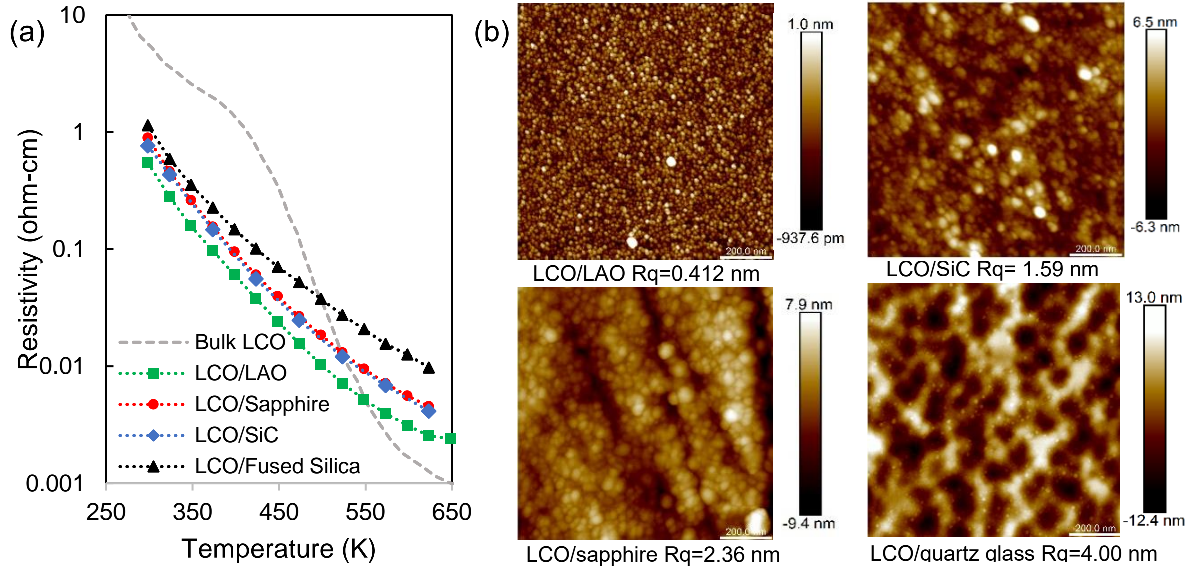


Figure 2.5 (a) 4-point resistivity measurements as a function of measurement temperature for 150 nm sputtered LCO film co-deposited on multiple substrates. Comparative results are shown for bulk material, extracted from [21] (b) corresponding 1 μm x 1 μm AFM images [45]

As shown in Figure 2.5 (a), the measured resistivity of thin film samples is lower than the bulk at room temperature and may be attributed to oxygen deficiency, with oxygen vacancies serving as donor impurities, leading to more semiconducting behavior at the lower temperatures [56]. In addition, the LCO spin state transition is dependent on unit cell volume. The high spin case is favored in higher cell volumes because high spin Co^{3+} has a larger atomic radius. When the unit cell volume is constrained, the IS state is favored [57]. This reduction in on/off ratio moving from bulk to thin-film LCO has been similarly observed in strained films grown by molecular beam epitaxy [58]. However, four-point probe measurements reveal that despite the differences in texture and grain size, the films on sapphire, SiC, and LAO all demonstrated comparable resistivity on/off ratio of ~205 over the measured temperature range. The polycrystalline films on sapphire and SiC demonstrate an overall shift to higher resistivity, indicating increased grain boundary resistance that does not have a corresponding influence on the spin-state transition. In addition, the low crystallinity of the LCO on quartz substrate exhibits both the highest roughness, lowest on/off

ratio (118x), and highest resistivity. This is understandable because while long-range order is not necessary for the mechanics of the Co spin state transition, local symmetry is required.

2.3.3 Influence of stoichiometry

Off-stoichiometry may hold the key to an improved resistivity on/off ratio. There is little prior work exploring the resistivity drop and spin-state transition in off-stoichiometric lanthanum cobalt oxide phases. We deposited a set of LCO films with the x-ray diffraction pattern illustrated in Figure 2.6 (a), demonstrating deteriorating crystallinity grown on LAO as the La/Co ratio increases. We also find evidence that La-heavy films may grow as Ruddlesden -Popper (K_2NiF_4) phase on sapphire, given the close match to powder diffraction patterns of La_2CoO_4 material (Fig. 2.6 (b)).

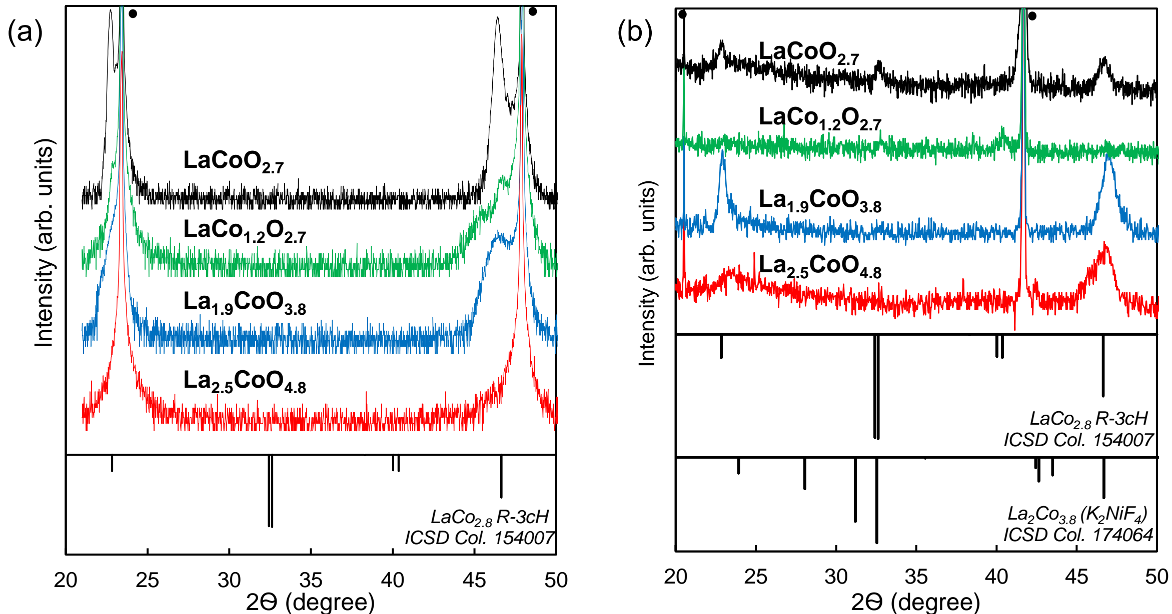


Figure 2.6 X-ray diffraction pattern of 150 nm lanthanum cobalt oxide films at varying composition deposited on (a) LAO and (b) sapphire. Reference diffraction patterns are obtained from ICSD database. Substrate peaks are labelled with a ● [45].

Furthermore, we have observed that the lanthanum-rich films have greatly increased overall resistivity and much higher switching ratios (Figure 2.7). For example, while the stoichiometric LCO film resistivity will drop ~200 times from room temperature to 350 °C,

the $La_{2.6}CoO_x$ film demonstrates greater than 850 times drop over the same range. We do not entirely comprehend this phenomenon, which has not previously been reported. We may consider the formation of the RP-phase of La_2CoO_4, the layered perovskite phase, with a layer of O-Co-O confined two-dimensionally between Lanthanum layers. This phase reduces the degeneracy of the e_g energy level, stabilizing the IS state and pushing the resistivity higher. However, others have reached the conclusion that the IMT in single crystal La_2CoO_4 would be suppressed and it would behave entirely as an insulator [59]. In sputtered films, perhaps the greater disorder from the sputtering process favors transition to the entropically favored metallic state. These intriguing composition-structure-property relationships demonstrate the high tunability of the LCO spin-state transition and provide a potential pathway of study.

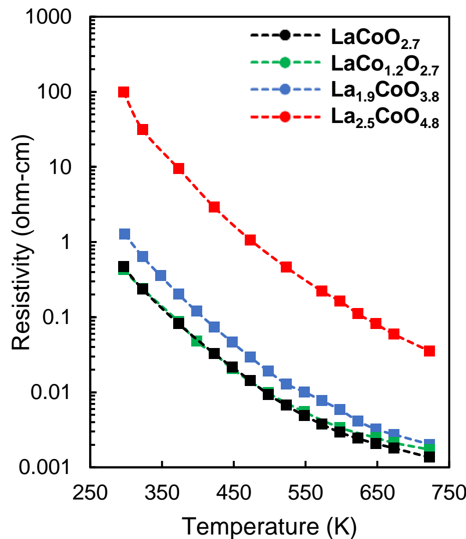


Figure 2.7 Temperature dependent resistivity data for LCO/LAO demonstrates how increased La concentration increases steepness of the transition profile, as well as the overall resistivity [45].

2.4 Estimation of Band Gap Collapse

Near-IR absorption measurements allow for visualization of the band gap collapse as a function of temperature. For semiconductors and insulators, light is absorbed at wavelengths lower (energies higher) than the band gap.

2.4.1 Methodology

. Transmission, reflection, and absorption data were collected over the over the 900 nm to 1700 nm range, using a Fianium laser as a light source and calibrated against a GaAs standard. A Linkam temperature controller was modified to allow for simultaneous heating and transmission measurements through the sample holder and was carefully aligned to minimize secondary reflections. Measurements were taken in 25 °C increments from 25 °C to 350 °C. Use of a beam splitter allows two Germanium detectors to simultaneously collect transmission and reflection data. Because the laser power is expected to drift mildly over the course of the two hours of data collection time, all data is normalized to a third reference beam that is unobstructed by the sample. Transmission data is also normalized to a scan of the empty sample holder, and reflection data is normalized to a mirror standard. In total, the equations used are summarized below.

$$\frac{\frac{Sample_{Transmission}}{Sample_{Reference}}}{\frac{Empty_{Transmission}}{Empty_{Reference}}} = T\% \qquad \frac{\frac{Sample_{Reflection}}{Sample_{Reference}}}{\frac{Mirror_{Reflection}}{Mirror_{Reference}}} = R\%$$

$$Absorption\ \% = 1 - Transmission - Reflection$$

The Tauc method is used to estimate band gap. In this method the photon energy of the measurement wavelength (eV) is plotted against $(\alpha h\nu)^{1/r}$ where α is the absorption coefficient and r = 2 for indirect crystalline semiconductors. It is difficult to determine an exact band gap as there is a blurred onset due to the indirect nature [60]. Further, the sputtered film disorder and in-gap defect states leads to the formation of an absorption tail in the Tauc plot (known as the Urbach tail). However, by extracting a linear fit from the absorption data we can estimate the band gap value at the x-intercept and make comparisons between the magnitude of collapse for films.

2.4.2 Results

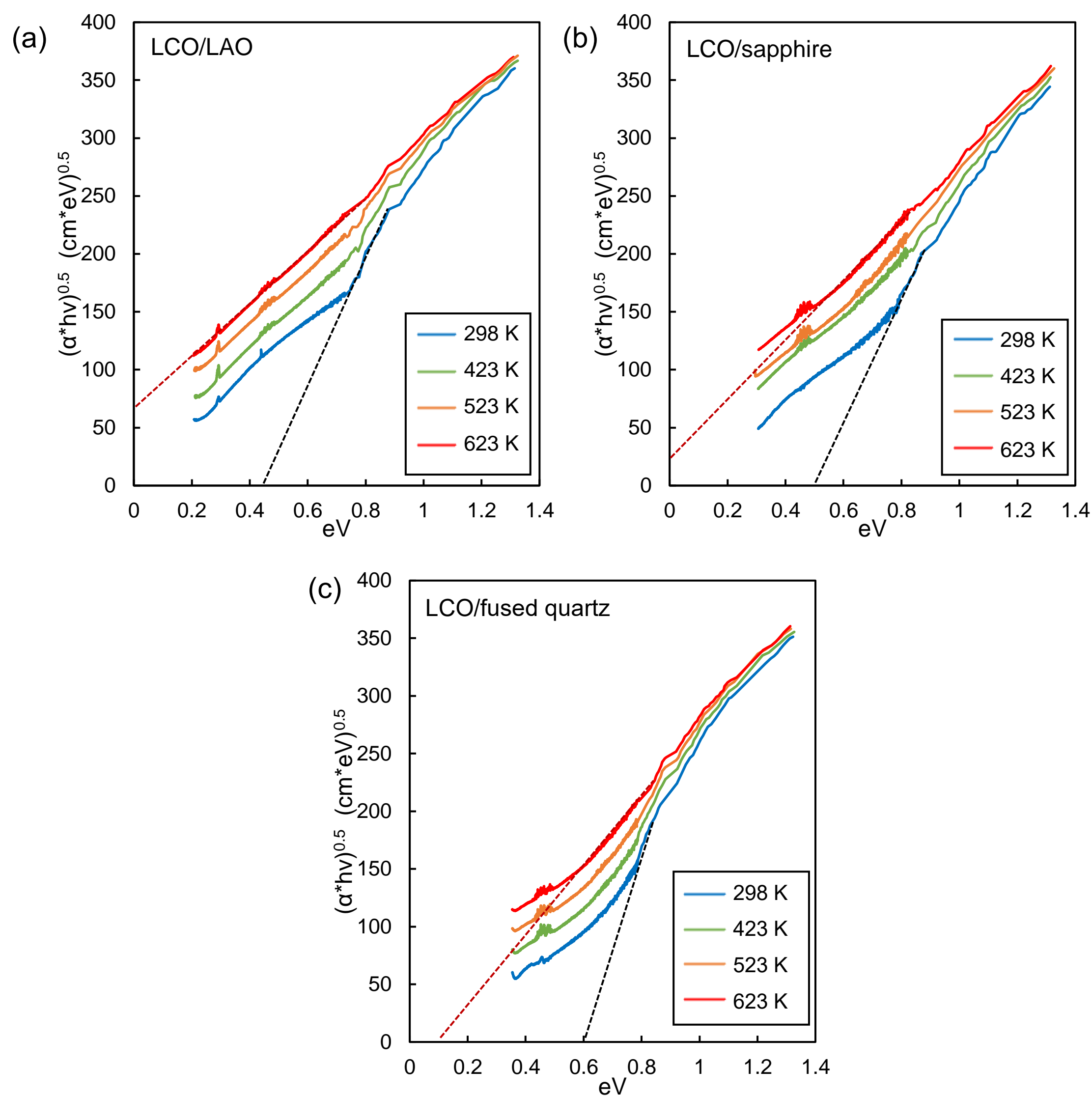


Figure 2.8 Tauc plots, used to estimate band gap collapse over temperature for 150 nm sputtered LCO grown on (a) LAO (b) sapphire (c) fused quartz [45].

In Figure 2.8 (a-c) we illustrate the Tauc plots for 150 nm $LaCoO_{2.7}$ films grown different substrates, with measurements taken from 25 ˚C to 350 ˚C. At room temperature, the band gaps of the LCO films are estimated to be 0.45, 0.5, and 0.6 eV for films grown on LAO, sapphire, and fused quartz, respectively. The curvature of the Urbach tail is most prominent in the LCO/quartz glass measurements, which is as expected given the amorphous

nature of that film and thus the greater number of in-gap defects. At 350 °C, only LCO/quartz glass continues to express a bandgap greater than 0 eV (estimated at 0.1 eV based on the x-intercept of the Tauc plot). In contrast, both high temperature Tauc plots for the crystalline LCO/sapphire and LCO/LAO linearize and align with the absorption tail, leading to negative x-intercepts. A "negative" estimation of band gap magnitude suggests the completion of the semiconductor-semimetal transition by 523 K for those films. The near-IR absorption estimate of relative magnitude of band-gap collapse over temperature supports the observed magnitude of the temperature-dependent resistivity drop for all these films.

2.5 Conclusions

With the ultimate goal of depositing smooth lanthanum cobalt oxide films for electronics applications, we conducted cathode discharge hysteresis experiments in mixed Ar/O_2 atmosphere in order to better understand the reactive dc sputtering mechanics. This method allows for live tracking of target condition during deposition. Increasing inert gas flow (increasing pumping speed) reduces residence time of reactive species at the target surface, increasing target lifetime and process stability. However, it does not have a strong influence on the onset of the critical reactive sputtering range in terms of reactive gas flow rate. We further investigated the influence of sputter deposition parameters (stoichiometry, substrate) on the electrical properties of lanthanum cobalt oxide grown by a single-step, high-temperature low-pressure process. Firstly, we found, in accordance with previously reported epitaxial films grown on LAO, a reduction in room-temperature electrical resistivity due to strain on the unit cell. Polycrystalline LCO films were grown on SiC and sapphire with surface roughness under 2.5 nm, showing comparable resistivity switching ratio to epitaxial films. We reported that the switching ratio above 25 °C is much greater when the La/Co ratio is increased, with suggested crystallization of the Ruddlesden-Popper phase on sapphire.

Near-IR absorption measurements indicated a semiconductor to semimetal transition at around 523 K for crystalline LCO films grown on sapphire and LAO. In contrast, amorphous LCO grown on quartz glass remained semiconducting up to 623 K.

Chapter 3: 2-Terminal Voltage-triggered Switches

3.1 Abstract

In this chapter I first evaluate various e-beam evaporated metals as ohmic contacts to LCO *via* the transfer length method. This method is used to determine the most thermally stable and lowest contact resistivity options to aid in integration of LCO into power devices. Next, two-terminal LCO switches were fabricated from sputtered films grown on LAO, sapphire, and SiC. We demonstrate an abrupt voltage-triggered transition from semiconducting to conductive state from 25 ^{o}C up to 150 ^{o}C. The threshold voltage for the switch is shown to have strong dependence on device length and weak dependence on device width. Rather than having a critical resistivity (critical carrier concentration) criterion as expected for homogenous Mott materials, the LCO switches demonstrate a critical power criterion as test temperature increases. This supports the theory that conductive HS clusters grow in a primarily entropy (and Joule-heating) driven mechanism [37,38]. Finally, we report that LCO switches can easily achieve nano-second switching speeds through pulsed voltage time-dependent measurements of scaled devices. In this chapter I also introduce the construction of a multi-physics COMSOL simulation that is proven to accurately predict the speed and magnitude of the LCO IMT.

3.2 Contact metal evaluation by transfer length method

The transfer length method (TLM) is a technique for determining the specific contact resistivity between a metal and semiconductor. Two-point resistivity is measured between rectangular contact pads deposited over a blanket semiconducting film. By varying the distance between the pads, we may isolate metal-oxide contact resistance from the oxide

sample resistance [61]. TLM structures are deposited over 150 nm of blanket sputtered LCO on sapphire substrate by e-beam evaporation (AJA), in the variations listed in Table 3.1.

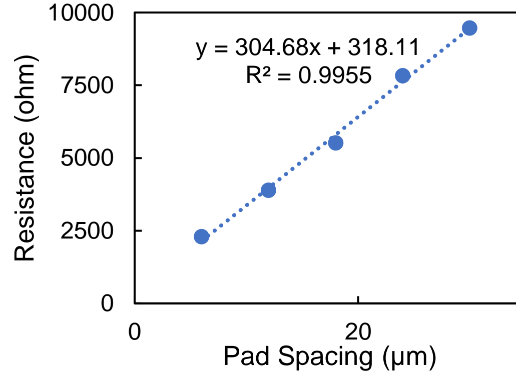


Figure 3.1 Example TLM plot for 40 nm Pt on LCO at 200 °C. Two-point resistance is typically measured at each spacing at 10 μA. Calculated contact resistivity here is R_c= 8.30 E-05 ohm-cm^2

Table 3.1: Candidate contact metals tested by the transfer length method, along with the corresponding measured room temperature specific contact resistivity.

Metal	Room temperature specific contact resistivity (ohm-cm^2)
50 nm Au only	4.44E-04
40 nm Pt/ 40 nm Au	1.62E-03
40 nm NiCr/ 40 nm Au	3.80E-02
10 nm Ti/ 40nm Au	9.42E-01
40 nm Cr/40nm Au	9.21E-01
40 nm Pd/ 40 nm Au	5.71E-03

The conventional wisdom is that while a noble metal (Pt, Pd, or Au) will form a lower resistance contact, a reactive metal will provide better adhesion to the semiconductor surface [62]. At room temperature, we observed these expected results too. However, we require LCO-based devices to function at high temperatures and power. Only the noble contact metals of Pd and Pt remained ohmic when the samples were heated above 100 °C, as shown in Figure 3.2 (a). The contact resistivities of those metals when measured at 200 °C are 5.32 E-05 ohm-cm^2 and 8.30 E-05 ohm-cm^2, respectively. However, for other contact metals, at higher temperatures and voltages, the slope of the I-V curve increases, indicating the formation of a resistive barrier to current passing. We deduced that reactive metals formed a parasitic oxide

against the LCO films, resulting in non-ohmic behavior from to the metal-insulator-semiconductor junction.

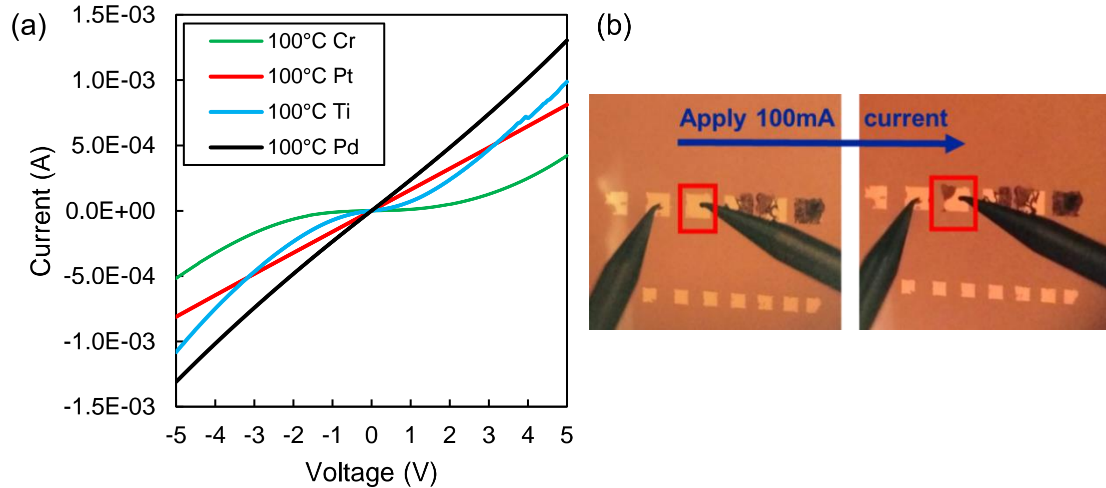


Figure 3.2 (a) I-V curves for various contact metals at 100 °C (b) microscope image of degradation of chromium contacts upon forcing of higher current.

Furthermore, the oxygen sensitive metals are physically unstable; when 100 mA was applied, for example, the Cr contact reacted and delaminated from the LCO surface (Figure 3.2 (b)). Similar results recurred even after attempting to anneal the contacts in nitrogen at 250 °C. Thus, practical LCO device contacts must comprise of a starting noble metal layer such as Pd or Pt, which consistently demonstrate lower Rc (~10^{-3} to 10^{-5} ohm-cm^2) up to 300 °C. This layer also serves as a diffusion barrier to an Au contact layer deposited next. However, due to the poorer adhesion qualities of a noble metal, we find that thin Pt/Pd structures delaminate from LCO at higher input voltages. As described further in Chapter 4.3.4, the minimum line width of a Pt/Au metal contact on LCO should be 1 μm to avoid that form of device failure.

Future optimization in this area is needed, either in the use of other contact metals, or more complex stacks. It is not expected that molybdenum (which oxides rapidly at 500 ^{o}C) or indium (which melts at 156 ^{o}C), would be appropriate choices. However, we may consider

the use of alloy metals, such as Sr or Al, at the LCO interface to assist in adhesion without forming a resistive barrier. We may also consider the use of other high melting point, refractory metals such as tungsten.

3.3 Voltage-Triggered Abrupt Transition

3.3.1 Methodology

All LCO-based structures in this section are constructed from stoichiometric films sputtered in the process described in Chapter 2.3.1. Metal contacts (Pt or Pd with Au cap layer) are deposited on top of LCO at room temperature using e-beam evaporation at a rate of ~1 A/sec. Electrical probing is conducted using a Keithley 4200A Network Analyzer, on a variable temperature Linkam HFS600E sample heating stage. $LaCoO_3$ pads were defined in positive photoresist S1813 and patterned *via* wet etch in diluted HCl (originally 37%,CAS 7647-01-0). Etch rate of LCO was determined as a function of HCl percentage by measuring etch depth over time on thick 200 nm starting film using a Bruker DektakXT® profilometer. Etch rate study results are given in Figure 3.3 (a,b). Films remained smooth (R_q < 2 nm) post etch, as verified by AFM.

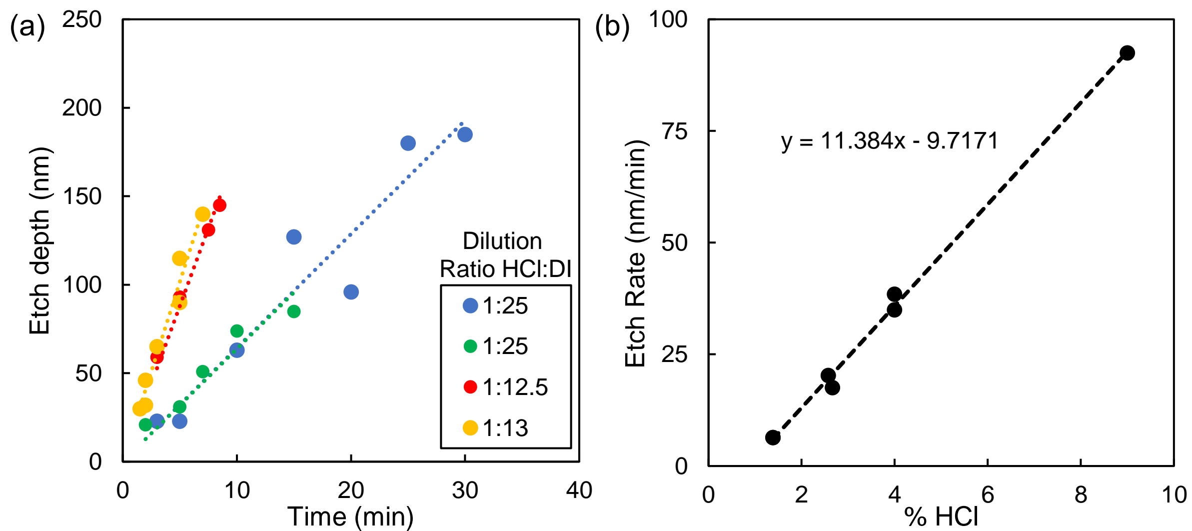


Figure 3.3 (a) Trench etch depth for 100 µm features for various dilution ratios of 37% Hcl to DI water (b) calculated etch rate of LCO as a function of % HCl

For the fabrication of two-terminal switching structures, 40 nm sputtered LCO films were etched into pads of device length L and width W (Figure 3.4 (a)). Larger devices were patterned using a contact aligner. Due to lithography limitations, smaller device dimensions were patterned *via* e-beam lithography courtesy of Suman Datta's group at University of Notre Dame, and electrically tested there as well. We provided our collaborators films of LCO sputtered on LAO, SiC, and sapphire.

3.3.2 Results

When thermally activated, bulk LCO shows a gradual IMT transition due to the coexistence and shifting LS-IS-HS population (see Chapter 1.2.2 for more details). However, sufficiently thin LCO films will display an abrupt transition to the metallic state at and around room temperature, as demonstrated in the voltage triggered switch in Figure 3.4 (b) with active area width = 100 μm and length = 10 μm. In these 2-terminal devices, the voltage applied over a thin strip of LCO allows for IMT switching of small resistive domains. As each domain switches, the current pushed through the material increases and the temperature of the material increases by Joule heating. Previous studies in current-driven transition of LCO switches have indicated the presence of negative differential resistance events and the formation of conductive filaments [63]. Thus, the resistivity of the LCO area reduces, allowing more current to flow, and a cascading Joule heating effect allows for fast turn-on times and the appearance of abrupt switching. It is not known definitively whether a dual NDR is expected due to the dual nature of the LS-IS and IS-HS transition, or simply is sometimes observed from the formation of multiple conductive filaments [44].

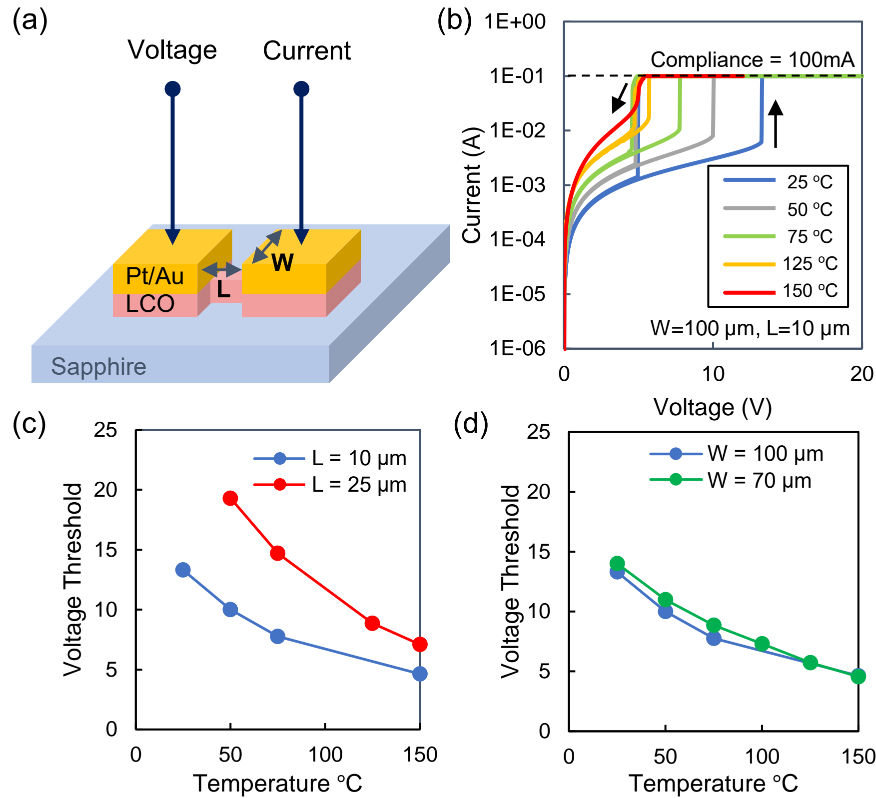


Figure 3.4 (a) schematic of the fabricated LCO switches (b) demonstration of abrupt voltage triggered switching with 40 nm LCO on sapphire. Current compliance is set at 100 mA to avoid material damage (c) voltage threshold as a function of sample temperature and showing length dependence (d) voltage threshold over sample temperature showing weak width dependence.

We demonstrated abrupt voltage-triggered transition from the LCO semiconducting to metallic state across a broad temperature range from 25 °C to 150 °C for sputtered films grown on sapphire (Figure 3.4 (b)). The voltage threshold decreases as temperature increases, which is expected due to the entropy driven nature of the LCO spin-state transition. Above 150 °C, the film starts in a more conductive state, so we cannot distinguish a significant transition with increasing voltage. There is a hysteresis curve associated with the transition. The width of the hysteresis on the down sweep is associated with the latent heat of the material and is thus wider at room temperature.

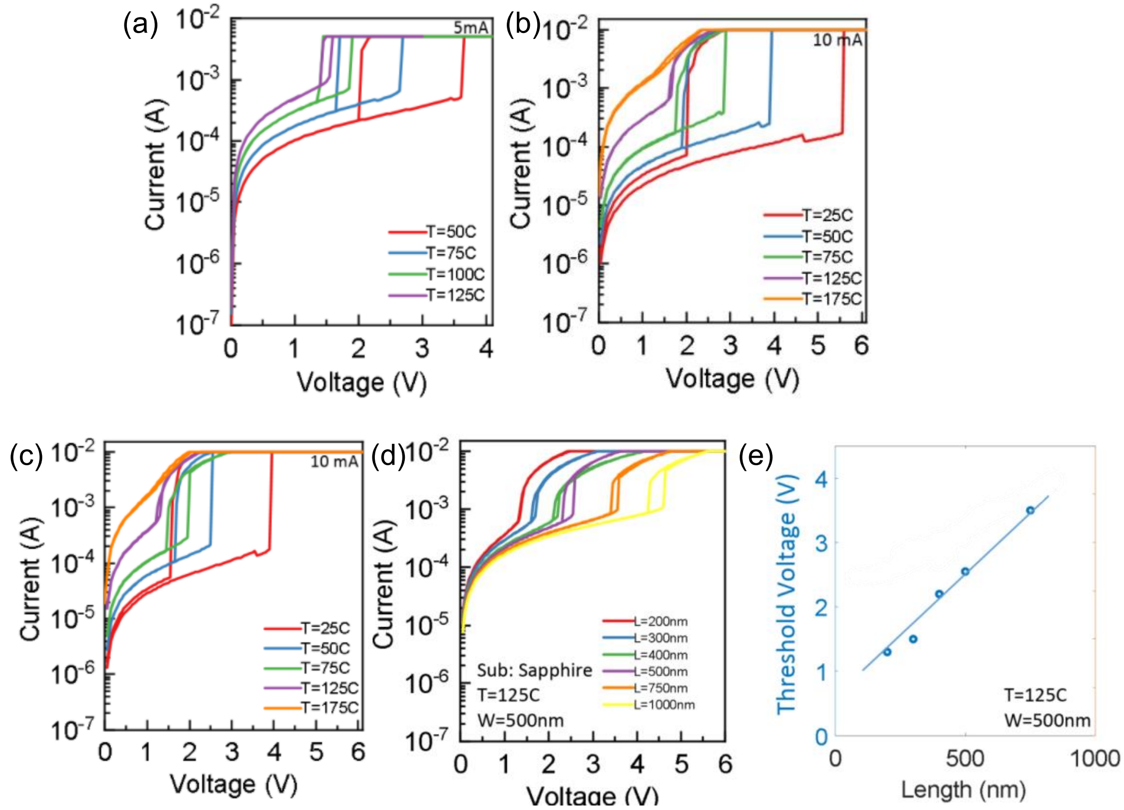


Figure 3.5 Measurements for voltage-triggered abrupt switching collected with collaboration from University of Notre Dame. The device areas are 200 nm long by 500 nm wide for (a) sputtered LCO on LAO (b) sputtered LCO on SiC devices (c) sputtered LCO on sapphire (d, e) increasing the device length for LCO on sapphire devices. There is a strong linear reduction of V_{Th} with length, and the hysteresis width of the switch reduced, as expected for smaller device areas at high temperature.

Results from the scaled (width = 500 nm, length = 200 nm) devices are shown in Figure 3.5 for sputtered 40 nm LCO on sapphire, SiC, and LAO. Also shown are a comparison of 125 °C switching threshold voltage V_t as a function of increasing device length. Similar to the larger devices, there is clearly a strong linear trend between V_t and device length. In addition, there is a weaker dependence on width scaling. In most cases, it is necessary to have the device width be larger than length to prevent overheating and contact delamination from too high current density.

In Figure 3.5 (a-c) we compare the switching behavior on different substrates. SiC shows a tendency towards reduced hysteresis width on the down-sweep. This is likely due to SiC's high thermal conductivity (2.8 W/cm-K @ 300 K) [64] compared to LAO (0.117 W/cm-K)

[65] or sapphire (0.25 W/cm-K). This could be promising for high power handling RF devices since survivability would depend on the device's ability to dissipate heat quickly and have low recovery times after the electronic attack has passed.

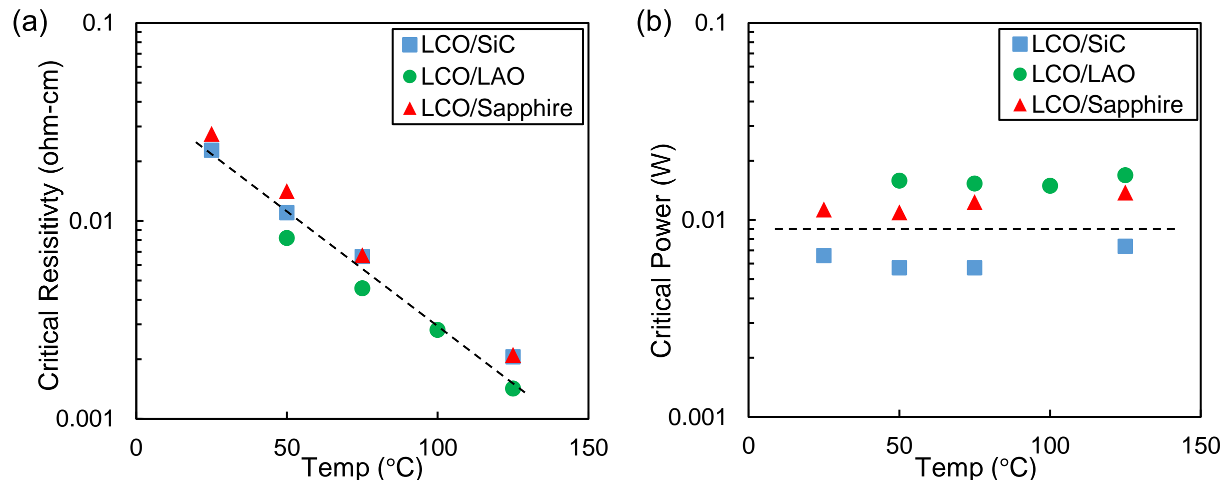


Figure 3.6 (a) critical resistivity $R_{Th} = V_{th}/I_{th}$ for 200 nm x 500 nm sputtered LCO switches decreases with increasing substrate temperature (b) critical power $P_{th} = I_{Th} * V_{th}$ for the same devices shows no temperature dependence

The results from Figure 3.5 can also be interpreted in terms of critical resistance or critical power density required to induce a voltage controlled abrupt transition. V_{Th} and I_{Th} are extracted from Figure 3.5 and used to calculate R_{th} and P_{th} for every film. These terms are then plotted in Figure 3.6 (a, b) as a function of base substrate temperature. Given the known relationship between rho and T, we can use resistivity as a stand-in term for average active device temperature, or carrier concentration of the device material. For a Mott insulator like VO_2, it is expected that the critical resistivity/temperature of transition is constant, regardless of substrate temperature, due to the satisfied Mott criterion of critical carrier concentration for electron delocalization. However, in LCO devices, we find that the critical resistivity drops as the test temperature increases. This means the device area needs to get to a higher average temperature to achieve an abrupt transition, therefore LCO cannot be a Mott material.

However, the LCO IMT seems to be based on critical power input onto the device area (Figure 3.6 (b)). Thoma P. *et.al* writes that a critical power density implies localized instabilities, with inhomogeneous current densities (perhaps filamentary in nature) that are driving the transition [66]. This trend, which is the same as previously reported measurements for epitaxially grown LCO on (100) LAO [44], supports the theory of spin state LCO domains switching as entropy driven conductive clusters, that grow into the surround insulator areas, rather than as a homogenous Mott transition. At some critical inflection, the domains switch enough to allow current flow to increase, which in turn leads to Joule heating and more domains switching, which leads to a cascading effect to fully metallic state.

3.4 Transient Switching Characteristics

In this section, we investigate the switching speed of the LCO two terminal devices both through pulsed voltage measurements and simulation methods. A rapid response time at the nanosecond scale is crucial to satisfactory spike leakage performance of power limiters.

3.4.1 COMSOL Multiphysics Simulation Set-up

A 3D Multiphysics model of a LCO switch was built in COMSOL to model the transient insulator-metal transient and explore the influence of material choice and dimensions on LCO switches. This model should help us develop physics-based solutions and trends to support experimental results for the thermally engineered switches. Two physics engines, heat transfer in solids and electric currents, enable the calculation of electromagnetic Joule heating, which is known to be a primary contribution for the abrupt LCO switch. The model is constructed to the same dimensions as the fabricated devices (Figure 3.7 (a)). All relevant temperature dependent material properties for substrate, contact metal, and LCO film were incorporated. Properties for contacts and sapphire substrate were primarily drawn from the COMSOL database for bulk materials.

Temperature dependent LCO resistivity was based on empirical measurements by four-point probe method of our own films. Other LCO properties such as thermal conductivity and heat capacity were pulled from literature sources on bulk material [67]. We assume no convective or radiative heat losses but allow for conductive heat transfer to maintain the substrate base temperature. For more details on the simulation parameters , see Chapter 3 Supplemental.

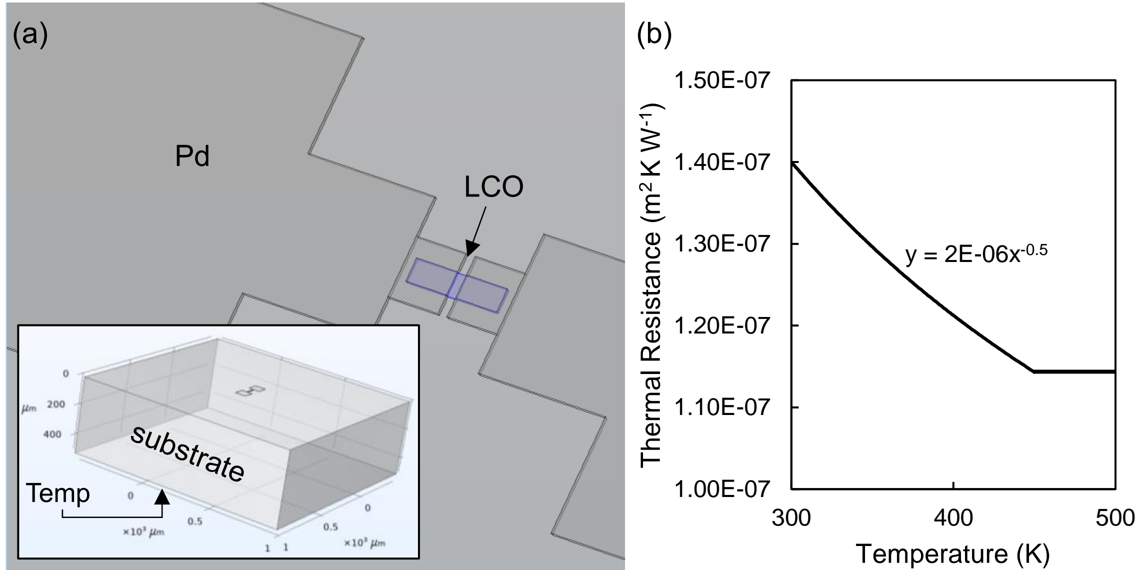


Figure 3.7 (a) screenshot of model of 200 nm length x 500 nm width LCO device. Inset provides zoomed-out view of device, with ambient temperature set on the bottom surface of the substrate (b) estimated interfacial LCO/substrate thermal boundary resistance.

The primary source of uncertainty in the 3D COMSOL model was the interfacial thermal resistances, which were key contributors to the insulation of the LCO pad that enabled a rapid transition. To the best of our knowledge, this value has not previously been reported for LCO grown on any substrate. Thus, we had to approximate the value. Based on reported values from other insulator-semiconductor interfaces [68], we initially estimated the room temperature LCO/substrate thermal boundary resistance at ~7E-08 m^2K/W. However, this proved too low, and we inferred that the sputtered LCO film must have poor thermal contact with the substrate, leading us to modify the value to 1.4E-07 m^2K/W, in range for a moderately degraded interface [69]. Theoretically, thermal boundary conductance between

two materials has a dependency T^3 for temperatures << the Debye temperature (use the lower Debye temperature of the two materials). At T > Debye, the TBC will saturate. In the intermediate, the relationship is more moderate (T^n) where $0<n<1$ [70,71]. As the Debye temperature of LCO is 455 K [72], we believe the LCO/substrate interface would be in the intermediate regime throughout the simulation range. The value of n is unknown for LCO. We set n=0.5, which gave the most similar simulation results to measured data, then set the value constant at 450 K with no smoothing term.

3.4.2 Nano-second scale switch at 75 °C

These results have previously been published in [73]© IEEE 2022. We demonstrated nano-second turn-on time of the voltage-triggered two terminal LCO switch fabricated on sapphire substrate in [73]. The device areas were 200 nm long by 500 nm wide. Figure 3.8 (a) shows the experimental setup. A three-step pulse scheme as shown in Figure 3.8 (b) is used to probe the electronic transition at fast time scales. The 'set' pulse, followed immediately by a 'read' pulse with a fixed delay, serves to trigger the IMT in the LCO switch and then assess the required recovery time to the insulating state. A third 'check' pulse is used to trigger the IMT a second time, ensuring that the LCO switching speed is maintained for multiple cycles. The switching speed measurement at 75 °C is shown in Figure 3.8 (b) with set/check pulse amplitudes of 2 V and a read amplitude of 1 V, each of 50 ns pulse width and 5 ns rise and fall times. The triggering of IMT in LCO is observed in the output current response (I_{OUT}), which reaches a steady value after a delay of 20 ns compared to the application of the input 'set' pulse (V_{IN}). The transient behavior includes approximately 10 ns of incubation delay and 10 ns of output rise time. Upon removal of the higher voltage bias, we observe rapid, <10 ns turn-off of the device. For simulation, a fully coupled iterative time-dependent solver calculates output current for the given input voltage pulse every 0.05 nanoseconds.

Simulation result is depicted in Figure 3.8 (c), showing high accuracy predicting both the magnitude of transition as well as transient thermal incubation and rise times.

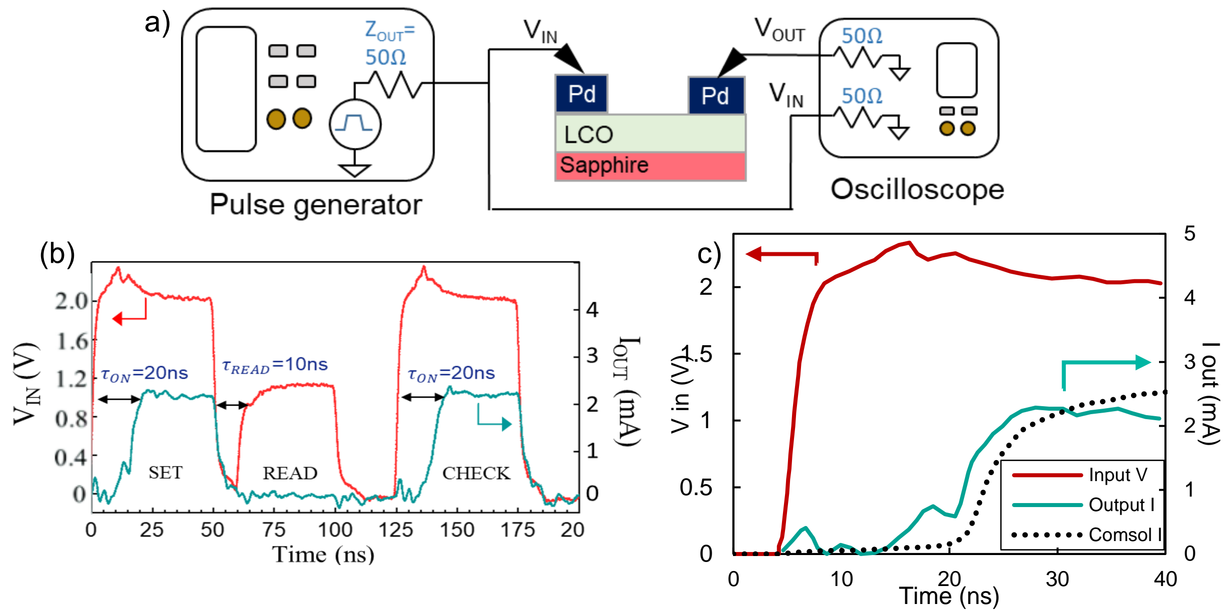


Figure 3.8: a) Schematic of set-up for fast pulsed measurement at 75 °C. (b) Repeated probing oscillating from set bias of 2 V to read bias of 1 V [73] © IEEE 2022 (c) Zoom-in into turn-on transition for one pulse shows approximately 10 ns of thermal incubation time and 10 ns of transition time. Dashed black line represents the output current of the Multiphysics model for the same input voltage pulse.

3.5 Supplemental

3.5.1 COMSOL Simulation Parameters

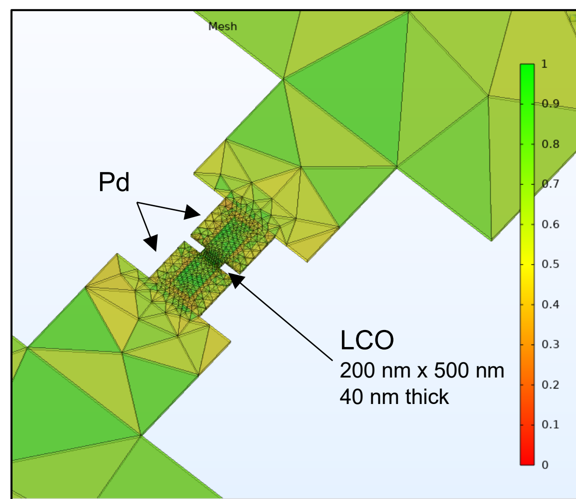


Figure 3.9 Adaptive mesh refinement is used to ensure high mesh quality throughout the model. Thus, high resolution is found at the thin LCO, with coarser mesh resolution at the contact pads. Scale is the default COMSOL-generated representation of mesh quality

The following graphs are of temperature-dependent material and interface properties that were incorporated into the model if not already found in the COMSOL database.

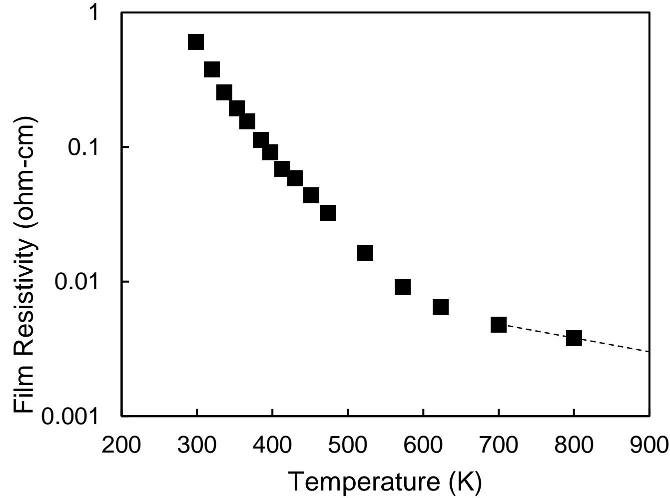


Figure 3.10 LCO film resistivity is based on 4-point probe results (Chapter 2.3.2) up to 623 K, used in the simulation described in Chapter 3.4.2. Since it is expected that the HS population will continue to grow above that temperature, we estimate a continued drop in resistivity, but at a slower pace. A linear extrapolation was taken from the last two points.

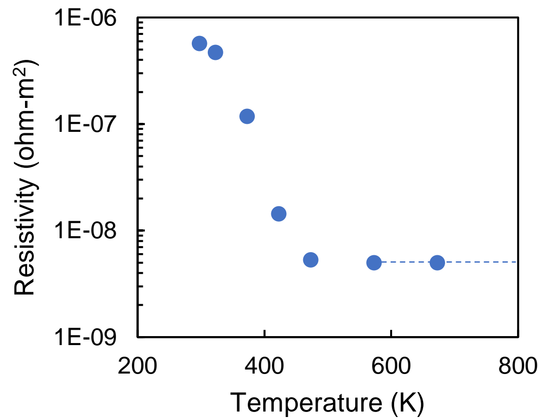


Figure 3.11 Interfacial resistance to current flow for the LCO/Pd interface was based on the transfer length method conducted up to 473 K in Chapter 3.2.1, with linear extrapolation between measurements. It is expected that the devices will overheat beyond our measured range. We set a constant value at 5E-09 ohm-m^2 for higher temperatures.

Chapter 4: $LaCoO_3$ - based RF Shunt Power Limiter

4.1 Abstract

Wireless technologies require robust RF switches to maintain operation in challenging environments. Further, there is a present need for reliable microwave power limiters that prevent incident signals above a certain power threshold from passing and damaging the sensitive low noise amplifier (LNA) in the receiver chain. Current microwave power limiter performance, based on P-I-N diodes, are restricted by tradeoffs between power handling, frequency response, and scalability. Insulator-to-metal phase transition (IMT) oxides exhibit unusually fast, reversible changes in conductivity as a function of temperature and present an opportunity to overcome the constraints in RF limiter technology. Previous attempts have focused on IMT-based limiters with vanadium dioxide (VO_2). These devices show high endurance, high ON/OFF ratios, and potential for significant power handling up to 40 dBm. However, their usefulness is hampered by inherently low operating temperatures, with no VO2 switch capable of operating above 50°C [17,18].

In this chapter, I report on the fabrication and 2 GHz Power-in Power-out testing of shunt power limiters based on sputtered LCO grown by the process described in Chapter 2.3.2. These LCO limiters achieve the highest power limiting over the broadest temperature range ever reported for an IMT material-based RF limiter, from 10°C to 225°C. Additionally, we present a three-dimensional COMSOL Multiphysics model incorporating material temperature-dependent properties that accurately predicts LCO RF device behavior. We establish that due to the high thermal boundary resistance between sputtered film and substrate, there is little difference in thermal performance between LCO limiters based on LAO, SiC, or sapphire. However, we can expect reduced parasitic capacitances on the low

dielectric constant substrates, especially at high frequency. Results from our published work [73] are included in Chapter 4.3.1.

Further, a variety of LCO limiter geometries and dimensions are constructed at the wafer scale on 4" SiC, demonstrating the feasibility of integration into standard chip manufacturing processes. In this chapter we analyze the impact of geometry on limiter performance and discuss possible trade-offs in design between insertion loss and power handling. Our thus far best performing devices provide <1 dB insertion loss up to 75 °C, resilience up to 40 dBm, and leakage power of 21 dBm.

Failure analysis is conducted for high temperature and power failure, and we identify at least three distinct failure modes: contact delamination, contact melting, and LCO material degradation. The validated COMSOL device model then serves as a useful predictive design tool for furthering optimization. We propose simulation-backed designs that will enable improvements to LCO shunt device performance. Benchmarking against both recent research art and commercial products indicates that LCO is a strong candidate for the next generation of microwave power limiters.

4.2 Methodology

4.2.1 Device Structure and Fabrication

Radio-frequency shunt limiters were devised as illustrated in Figure 4.1 from sputtered LCO. At low powers, the LCO pads are resistive, the device is turned OFF (a.k.a. passing state) and the signal will continue downstream (Figure 4.1 (a)). Above a critical power, the LCO switches to a low resistance state and shunts power to ground, a.k.a. the ON state (Figure 4.1 (b)). LCO strips link the signal to ground by either a linear pad (Figure 4.1 (c)), or underneath interdigitated metal fingers (Figure 4.1 (d)). It is hypothesized that the interdigitated fingers configuration will minimize the ON state resistance, improving

isolation. Conversely, having so many fingers close together increases the device area and may lead to greater parasitic capacitances. The linear device, in contrast, is expected to demonstrate the opposite performance of improved insertion loss and reduced capacitance at the cost of worsened isolation. Based on our results from the 2-terminal voltage triggered LCO switches, it is desirable to keep the length (dimension L or S) of the LCO shunt short to reduce the voltage drop, threshold power, and switching speed.

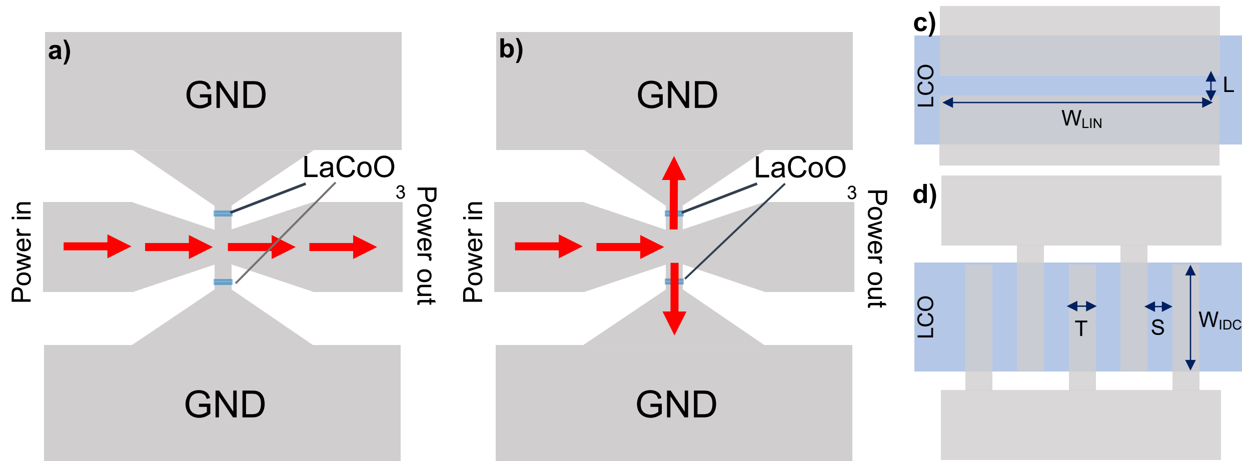


Figure 4.1. Schematic of the shunt limiter depicts (a) OFF state signal flow when $P_{in} < P_{th}$ (b) ON state when $P_{in} > P_{th}$. The LCO pads are found at the GND-SIG junctions. (c) close-up of one of the junctions in linear configuration. (d) close-up of the junction in an interdigitated configuration. We define width of the fins "T" and spacing between the contacts "S".

The first set of LCO limiters, in interdigitated configuration only, were fabricated onto three different substrates (sapphire, SiC, LAO) in collaboration with the University of Notre Dame. First, blanket sputtered 40 nm LCO was wet etched down to the 9 µm x 4 µm pads with diluted HCl. Palladium contacts were defined on top by e-beam lithography and e-beam evaporation on 1 cm^2 chips. Device dimensions are T = 800 nm, S = 500 nm, W_{IDC} = 4 µm.

Wafer scale fabrication (4" SiC).

The second round of LCO limiters was fabricated on a wafer scale on 4" 6H-SiC. A layout was designed to include a variety of geometries and dimensions. First, alignment marks are placed on the wafer. Then, blanket LCO is sputtered (at 40 nm and 65 nm),

patterned with positive resist, and wet etched in diluted HCl to 15 μm × 4 μm pads. A dual positive photoresist is then used to define the contacts. 60 nm Pt + 60 nm Au contacts are e-beam evaporated and patterned *via* lift-off. Numerous chips are patterned by use of a stepper with 5:1 projection of the designed 10 mm x 10 mm layout. The minimum expected feature size and spacing resolution is 500 nm, which primarily limits definition of the metallization layer. Figure 4.2 illustrates successful fabrication of the limiters through this process, as imaged by SEM.

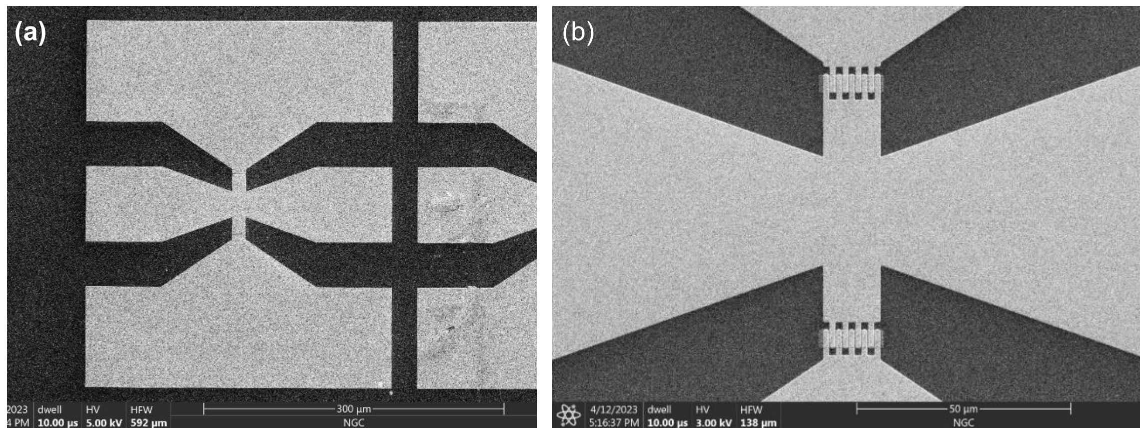


Figure 4.2 SEM images of fabricated LCO shunt limiters (a) full view including 130 μm pitch G-S-G planes (b) zoom-in to the active areas with interdigitated fingers of T = 1 μm and S = 500 nm

4.2.2 RF Measurement: Power-in, Power-out

Power-in, Power-out (PiPo) is used to quantify threshold power, insertion loss, and isolation. A heating stage is used to set the operating temperature, with a range from 10 ^{o}C to 225 ^{o}C. Chips were allowed to equilibrate to the temperature for at least 30 minutes before test. Experiments were conducted at 2 GHz in sweeps from -10 dBm up to 25 dBm or 40 dBm, depending on availability of equipment. System compensation was completed to ensure accurate power to the device-under-test (DUT).

The test set-up is as follows: Agilent 83650 Signal Generator → 0.8-2.7 GHz power amplifier → 100 μm pitch GSG input probe → DUT → 100 um pitch GSG output probe → Agilent E4418B Power Meter. Measurement uncertainty is ± 0.25 dBm.

4.2.3 Simulation set-up

The COMSOL simulations of LCO shunt devices are based on the model parameters outlined in Chapter 3.4.1. However, we now calculate steady-state response to input RF power, rather than transient characteristics. As before, the simulation is built to the same dimensions as the fabricated devices and a custom mesh is applied to ensure quality mesh resolution at the small LCO junction dimensions (Figure 4.3). Input signal at 2 GHz is input at one end of the transmission line at a "terminated" Terminal type. The other end of the transmission line is also a terminated Terminal, with 0 W applied power. Ground pads are also specified. COMSOL is able to directly solve for the steady-state S-parameters, from which we can deduce attenuation at every input power. We utilize a frequency-stationary segregated study, with Electric Currents determined by an iterative FGMRES solver, and Heat Transfer by PARDISO MUMPS. These solvers were chosen primarily to ensure fast solution times and accuracy despite the highly non-linear behavior.

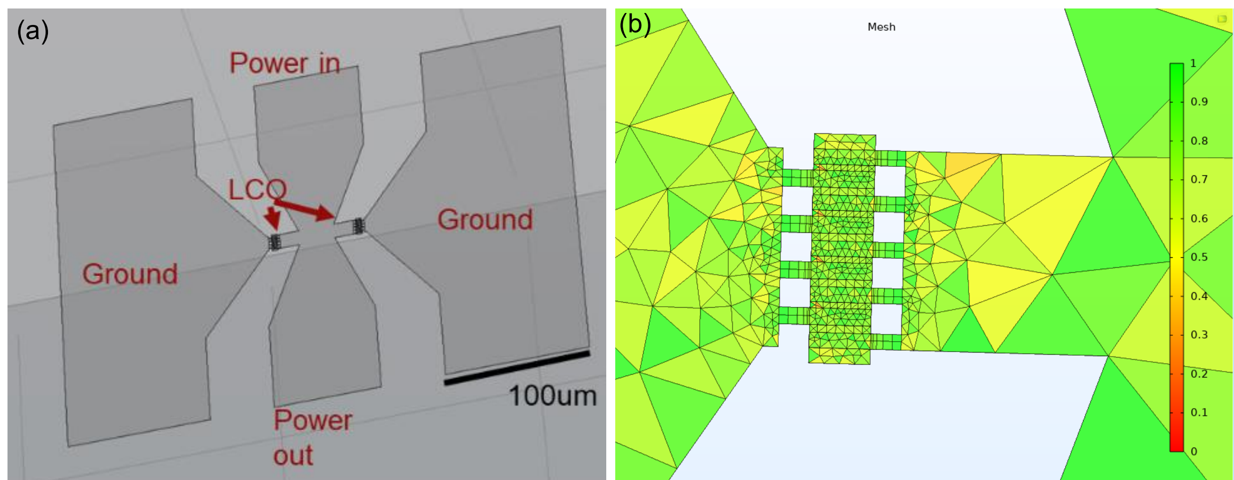


Figure 4.3 (a) screenshot of model of an interdigitated LCO shunt device (b) custom mesh sizing is used to ensure high mesh quality throughout the model. Thus, high resolution is found at the thin LCO and contact fingers, with coarser mesh resolution on the contact pads. Scale is the default COMSOL-generated representation of mesh quality

The following materials property additions were made to the simulation. Relative permittivity has been assigned to each material as follows: LCO = 4 [74], (006) 6H-SiC = 9.66, c-plane sapphire = 9.3, (100) LAO = 25, to support the calculation of signal flow at radio frequencies. Room temperature LCO/sapphire and LCO/SiC thermal boundary resistances are assumed to be 1.4E-07 m^2K/W, with a $T^{-0.5}$ dependency up to 450 K. Contact metal/substrate thermal boundary resistance is assumed to be a constant 3E-09 m^2K/W. Lastly, epitaxially grown LCO on LAO is expected to demonstrate lower resistivity over temperature than the polycrystalline LCO/SiC or LCO/sapphire (see Chapter 2.3.2). This is incorporated into the model by multiplying a factor of 0.9 correction to the input LCO resistivity values illustrated in Figure 3.12 for simulations of LAO-based devices.

It is important to acknowledge that for an alternating current, current density is distributed most strongly at the conductor surface, a phenomenon known as skin effect. This has not been explicitly programmed into the COMSOL simulation. Skin depth is a function of a material's resistivity, permeability, and permittivity, as well as the frequency of the input signal. For the extremely thin geometries in this simulation (LCO is under 100 nm thick), it was estimated that the theoretical skin depth will still be at least an order of magnitude larger than the material cross-section. Therefore, it can still be an appropriate approximation that current is evenly distributed.

4.3 PiPo Results

4.3.1 Interdigitated Limiter on Various Substrates

In this section we demonstrate the modest substrate dependence of 2 GHz LCO interdigitated shunt limiters with device dimensions: T= 800 nm, S = 500 nm, W_{IDC} = 4 μm, LCO = 0.04 × 4 × 9 μm^3. Power-in, power-out measured results are given in Figure 4.4 (a-b) for sputtered LCO-based devices grown on LAO, SiC, and sapphire, respectively.

All limiters performed similarly regardless of substrate, demonstrating abrupt limiting from 25 °C up to 125 °C with extremely low insertion loss of < 0.5 dB up to the threshold power. Threshold power decreased with increasing temperature from P_{in}=19 dBm to 13 dBm. This threshold power reduction was unexpected given the critical power density switching criterion found from 2-terminal voltage-triggered experiments. We hypothesize that this could be a result of thin contact fingers delamination from the LCO surface at high temperature. This would reduce the contact area, increasing the effective power density applied to the devices, and thus reducing the overall power threshold. Further explanation on this mode of device damage is found in the Chapter 4.4 Failure Analysis.

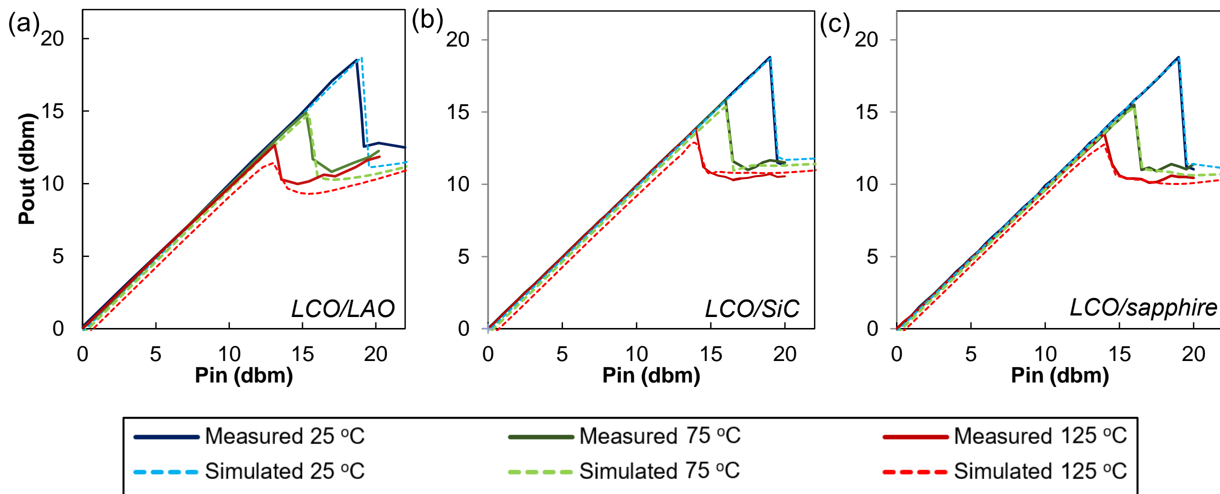


Figure 4.4: 2 GHz PiPo results from 25°C to 125 °C for shunt limiters based on sputtered LCO grown on (a) LAO (b) SiC (c) sapphire [73]© IEEE 2022. Solid lines indicate measured data, dashed lines for simulation.

Furthermore, it was originally expected that as a high thermal conductivity substrate, SiC would wick away heat from the LCO pad, thus increasing the input required to heat the material to the critical power density. However, this was not observed in the measured devices, as all devices demonstrated similar threshold powers. We attribute this to poor thermal contact of the sputtered films to the substrates, as we similarly deduced in the previous simulation study on transient switching. In other words, the observed minimal

influence substrate had on device performance indicates high interfacial thermal resistances. This hypothesis can be supported by simulation results. Without the inclusion of any thermal boundary resistance condition between LCO and substrate, the model did not predict power limiting at 25 ^{o}C, and much higher threshold powers for the higher temperatures. However, we then set the room temperature TBR of sputtered polycrystalline films is set to 1.4e-07 m^2K/W, a high value appropriate for poor thermal contact. This number was the only unknown in the simulation parameters, all else being drawn directly from literature sources or empirical measurements of the LCO films. Then, the COMSOL model accurately predicted limiting performance compared to the measured data (illustrated by the dashed lines in Figure 4.4 (b,c)).

Flat leakage power for LCO/sapphire and LCO/SiC at P_{in} = 20dBm is approximately 11 dBm, with minimal upwards slope. On the other hand, it was observed that LCO/LAO limiters tested at 75 ^{o}C and 125 ^{o}C demonstrate an input power dependence for leakage. This may be attributed to the epitaxial LCO film having slightly improved thermal boundary conductance against the LAO substrate compared to the polycrystalline films on SiC and sapphire. Indeed, this hypothesis can also be supported by simulation results. The room temperature TBR of LCO on LAO was set to 5E-08 m^2K/W. This is still a high magnitude TBR that doesn't strongly affect the threshold power, especially given that epitaxial LCO demonstrates lower resistivity as a function of temperature than the sputtered films. However, this adjustment allows us to predict an upwards slope in leakage same as is observed in the fabricated devices (Figure 4.4 (a)). Because the TBR is lower, the film is allowed to dissipate more heat to the substrate. Thus, it does not heat up as much, preventing the same high conductivity and thus higher ON state attenuation demonstrated by the LCO/SiC, LCO/sapphire devices.

There are advantages and disadvantages to the poor thermal contact of the sputtered LCO on any substrate. If indeed that is one of the key factors that determines the switching threshold, as our simulation supports, it is a crucial design requirement. Most limiters are required to turn-on by input powers less than 20 dBm. Results from these simulations indicate that a high thermal boundary resistance may be required to reach lower threshold powers at room temperatures. On the other hand, high TBR is also often associated with thermal failure. Future iterations of LCO limiter devices ought to be carefully designed to maintain both low power threshold and high-power stability. We discuss possible methods to meet these requirements in the next sections.

4.3.2 Interdigitated versus Linear Geometry on SiC

Despite the low substrate influence on thermal dissipation, we chose to fabricate our subsequent LCO limiters on 4" SiC for the following reasons 1) low dielectric constant supports high frequency operation 2) ease of integration into existing RF chip manufacturing processes 3) high thermal conductivity (~300 W/K-m) to protect against contact pad failure.

In this section I compare the performance of linear versus interdigitated configurations of the shunt device. Figure 4.5 shows PiPo measurements of linear devices with dimensions: W_{Lin} = 13 μm, L= 500 nm, LCO = 0.04 × 4 × 15 μm^3. While very few research papers report cycling tests, I believe it to be an important indicator of endurance and progression of any damage. All graphs in Figure 4.5 illustrate repeated sweeps of CW input power from -10 to 25 dBm. To avoid the effect of previous measurements on power response, each graph represents a different device fabricated on the same wafer, which was diced into chips. Each chip is heated and tested separately. The total number of runs is annotated in the corner of each graph. All devices demonstrate some initial migration of device behavior with increasing run count. However, all devices settle into a repeatable attenuation response

(represented by the red curve in each graph). Note: every red curve represents a minimum of 5 sweeps for which no run-to-run variation was observed. These results definitively establish the resilience of the LCO limiter design under CW input power up to at least 25 dBm.

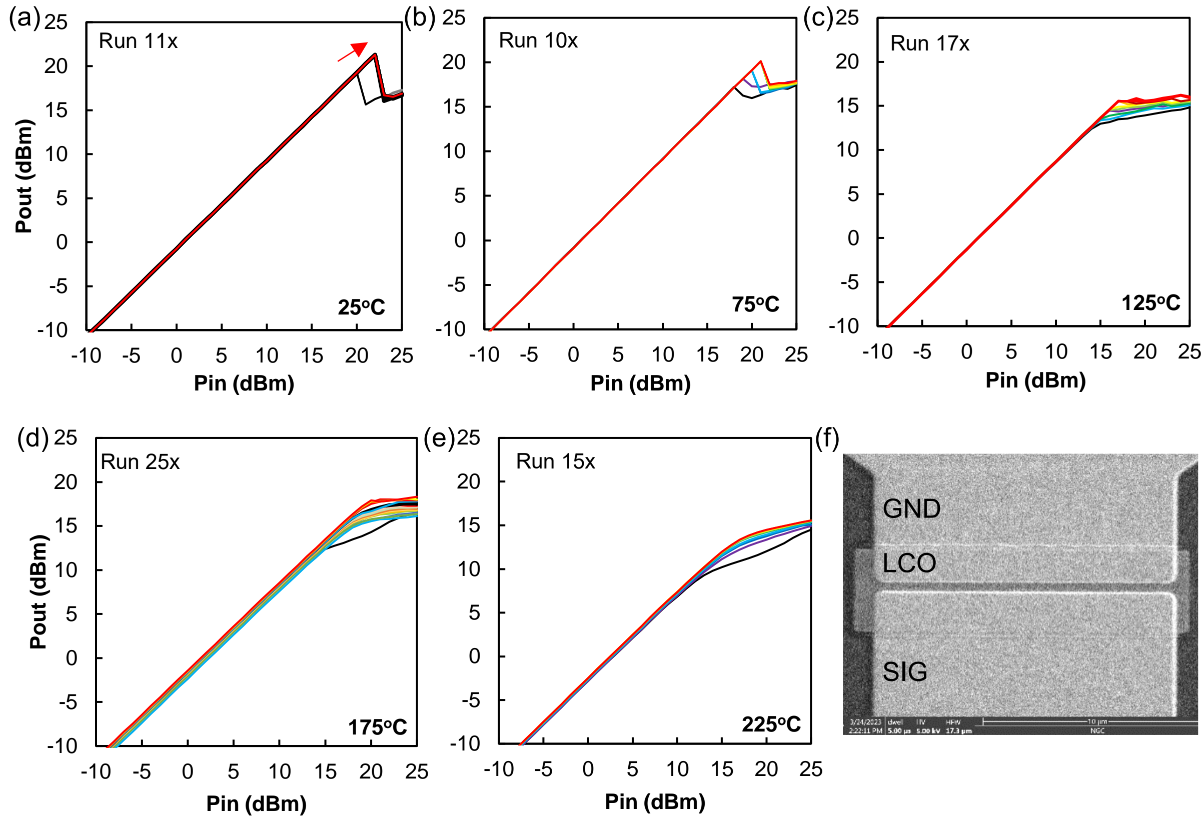


Figure 4.5: Repeated 2GHz PiPo sweep results for linear LCO limiter with device length 500 nm where the black line indicates the first run, and the red line represents device behavior that was repeated at least 5 times. Sweeps conducted at (a) 25 °C (b) 75 °C (c) 125 °C (d) 175 °C (e) 225 °C. (f) SEM image after measurement of one of the linear devices, zoomed in on the LCO pad to show that there is no visible evidence of damage.

At all test temperatures, there is little to no variation in insertion loss with increasing run count. Insertion loss as a function of temperature has been extracted and graphed in Figure 4.6 (light blue circles). As expected, insertion loss does increase with temperature given the thermally driven nature of the LCO IMT. However, the IL easily remains below 1 dB up to the standard operating maximum of RF power limiters, 125 °C. Any performance above that is on top of minimal requirements. The fact that the LCO limiter is stable and successfully limits input power up to even 225 °C demonstrates the strong thermal resilience

and potential for this new material in extreme environments. Flat leakage @ P_{in} = 25 dBm does not exceed 18 dBm at any temperature.

Threshold power does change with increasing run count. For all devices, the threshold power is initially lower, and progresses upward until the settled curve. This indicates that with increasing number of runs, the length of the device increased, necessitating higher power input to transition the LCO. Figure 4.5 (f) shows the SEM image of the GND-SIG junction of the linear devices after repeated input power sweeps. As no visible damage to the LCO pad or contacts is discernable, we infer that the initial run-to-run variation in the switch response is due to either small migrations in metal contact or slight delamination from the LCO surface. However, the devices still clearly work after those minor fluctuations, and eventually find a steady-state performance.

Interdigitated devices with the same device length, 500 nm, were also fabricated and tested for repeatability up to 25 dBm. The dimensions of these devices are T= 1 μm, S = 500 nm, W_{IDC} = 4 μm, LCO = 0.04 × 4 × 15 μm^3. Like for the linear devices, these are based on chips tested individually to avoid any historical test influence on results. The interdigitated configuration also shows some initial migration of increasing threshold power before settling into a repeatable behavior. The detailed results can be found in the Supplemental in Figure 4.15. However, here in Figure 4.6 we present extracted insertion loss and power threshold results for the interdigitated devices in comparison to the linear geometry. Insertion loss is attenuation at a small signal input of P_{in} = 0 dBm. Threshold power is defined as input power just before the 1 dB compression point in reference to the small signal IL.

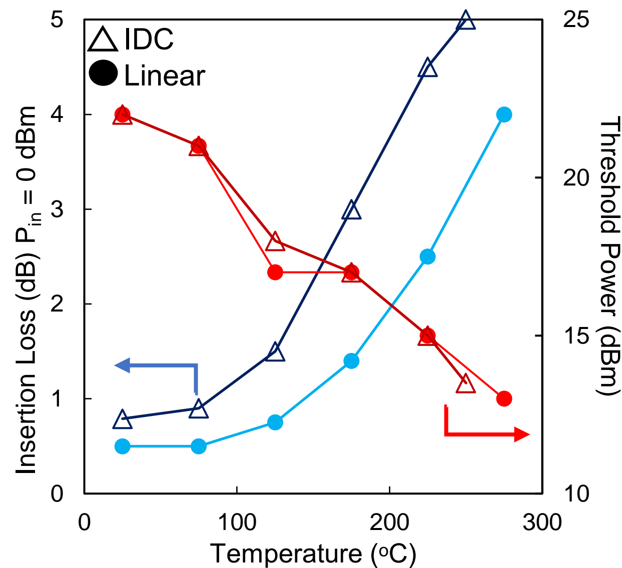


Figure 4.6 Comparison of device performance for interdigitated versus linear. Red/orange is threshold power, blue is insertion loss. Hollow triangles represent interdigitated devices, while solid circles are the linear junction geometry. Note: there is an uncertainty of ± 0.25 dB for insertion loss.

The threshold power doesn't vary significantly between the two configurations at any temperature. This aligns with previous results on DC triggered switches. Device length, which in the limiter case can be either finger spacing S or linear spacing L, is a key determiner of threshold power. In this case, as S =L = 500 nm, threshold power is the same. In contrast, it has been shown that device width has little influence on threshold switching voltage. For linear devices, device width is the width of the contact. In interdigitated devices, switch width is W_{IDC} times the number of fingers.

Insertion loss is worser for the IDC configuration at all temperatures. This is expected due to the higher parasitic capacitances between GND and SIG lines as effective capacitor area increases with the fingers. It would be possible to reduce the insertion loss of the IDC configuration by either increasing device length (increase S), reducing the number of fingers, or by using a thinner LCO layer. It is worth mentioning that insertion loss is not strictly due to resistive loss of signal through the LCO pads. There is also expected to be some loss directly from capacitive coupling from substrate or between GND and SIG pads. These losses were

estimated to be 0.5 ± 0.25 dB from a PiPo sweep of a thru-line at 25 °C. Based on the equation for parallel plate capacitance = εA/d, substrate-related losses can be further reduced by increasing substrate thickness or by reducing contact pad area. A is the cross-sectional area of the dielectric substrate, d the thickness, and ε the permittivity.

4.3.3 Demonstrated Resilience up to 40 dBm

In the last section LCO limiters proved capable of low insertion loss and very high temperature repeatable limiting response. In the following experiments we further establish high-power resilience as well. On-wafer high-power testing was conducted on an interdigitated limiter of dimensions T= 1 μm, S = 500 nm, W_{IDC} = 4 μm. The LCO is grown 65 nm thick, and the lateral pad area is 4 × 15 μm^2. Repeated PiPo sweeps from -10 dBm to 40 dBm are conducted on a device at room temperature (Figure 4.7 (a)) and demonstrate very little run-to-run change in performance. An SEM image of the device post-test shows no damage to the contacts or LCO material.

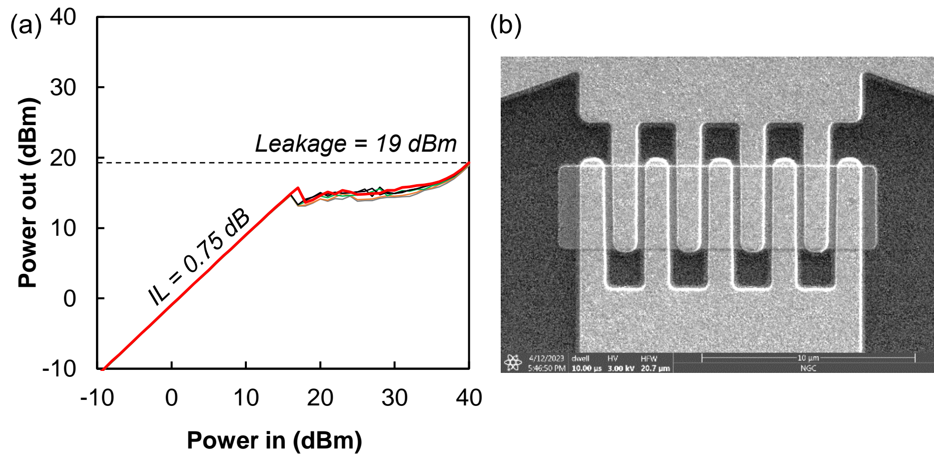


Figure 4.7 (a) Repeated high power PiPo sweeps at 25 °C for an interdigitated LCO limiter where the black line indicates the first run, and the red line represents device behavior that was repeated 3 times b) image of device after 40 dBm CW power input.

Based on the results from this device, increasing the LCO thickness from 40 to 65 nm has the potential to improve stability over runs and much higher power resilience. The room temperature power threshold also decreases from 21 dBm to 16 dBm even though the device

length remains 500 nm. This can be explained by the increased thickness of the LCO pad reducing resistance, allowing the passage of greater current density, and thus increasing the rate of Joule heating. The abruptness of the turn-on is also reduced, in-par with 2 terminal switches where only films around 40 nm thick demonstrated room temperature voltage triggered abrupt switching. However, if the switching time is not compromised (yet to be tested), this smoother limiting profile is still within desired device behavior.

At an input power of 40 dBm, the leakage power is 19 dBm. This suggests that the LCO limiter successfully dissipates ~ 9.9 W with no damage. Assuming that all that power is sent evenly through the two LCO pads, the power dissipation could be up to 8250 kW/cm^2. In contrast, a typical melting power density for Si is around 500 kW/cm^2 [75] highlighting the remarkable high-power resilience of lanthanum cobalt oxide and its' strong potential for power electronics.

This LCO IDC limiter also demonstrates a broad temperature operating range, as depicted in Figure 4.8. From 10 ^{o}C to 75 ^{o}C, the LCO limiter was able to block up to 40 dBm (10 W) of input power with a maximum leakage power of 22 dBm. These measurements were repeated multiple times, and on different devices. At 125 ^{o}C and higher, we began to observe permanent device failure to the passing state. As temperature increases, the input power failure point decreases, indicating the root cause is thermal stresses or melting. Further examination can be found in Chapter 4.4 Failure Analysis.

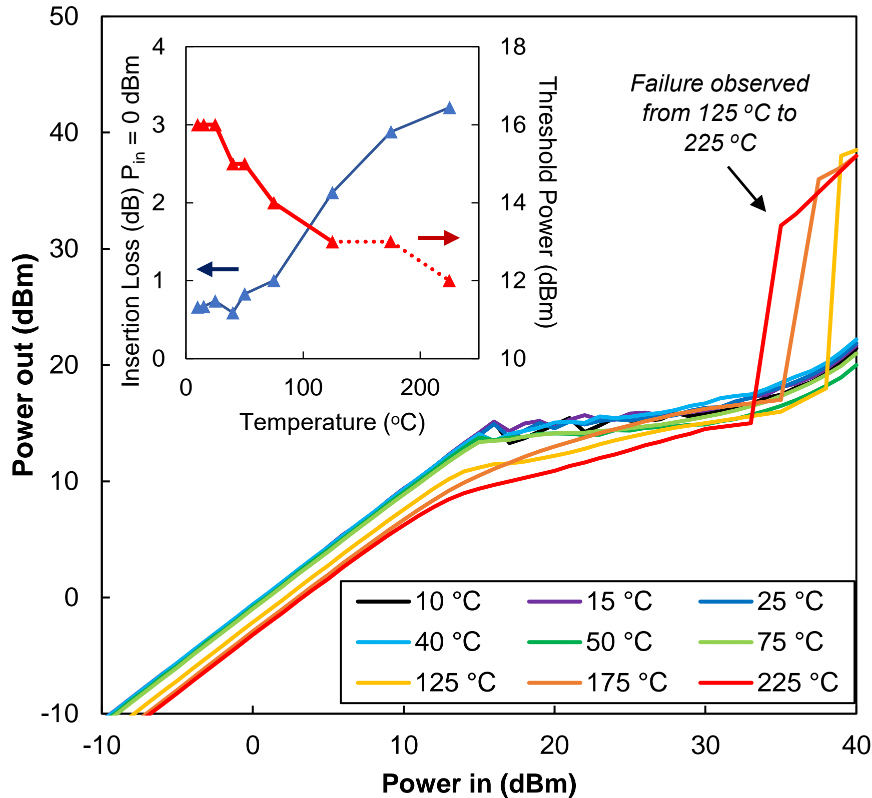


Figure 4.8 PiPo measurements [-10 dBm to 40 dBm] from 10 °C to 225 °C. Device dimensions are T= 1 µm, S=500 nm W_{IDC} = 4 µm. LCO is sputtered 65 nm on SiC. Inset shows extracted insertion loss at P_{in} = 0 dBm and threshold power as a function of test temperature. Note: uncertainty is ± 0.25 dB for insertion loss.

Up to 75 °C, insertion loss (extracted and plotted in Figure 4. 8 inset) remains within a satisfactory range, 1 dB or lower. Threshold power is both generally lower and is a weaker function of operating temperature than observed in the previous 40 nm LCO devices, indicating that increasing the LCO thickness may stabilize the threshold power. These LCO limiters successfully demonstrate high power resilience and broad temperature performance. With further optimization, it may be possible to widen the operating range even more.

4.3.4 Increasing device length

In this section I report on the influence of device length, using the interdigitated configuration. It was expected that increasing device length would also increase threshold power for limiting, and this was indeed observed experimentally (Figure 4.9 (a,b)). Because

the area of the LCO pad does not change with increasing spacing S, there will be fewer pairs of interdigitated fingers. That. in conjunction with the increased resistance across the LCO pad from increased length, insertion loss is reduced.

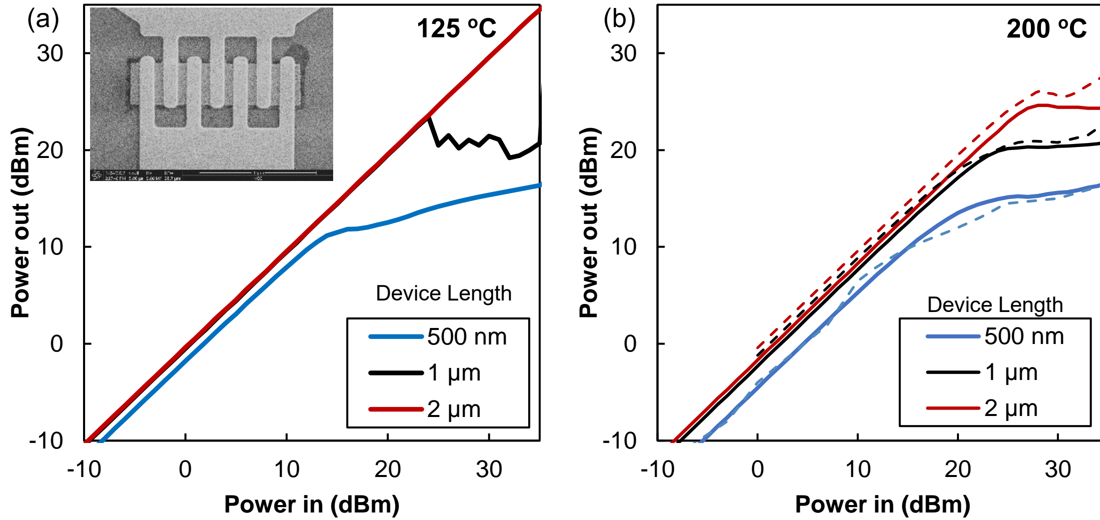


Figure 4.9 (a) 125 °C PiPo data for limiters of finger width T = 1 μm and LCO deposited to 65 nm. Device length is varied S = 0.5, 1, 2 μm. Inset shows SEM image of S = 1 μm device before test. (b) 200 °C PiPo data for limiters of finger width T = 1 μm and LCO deposited to 40 nm. Device length is varied S = 0.5, 1, 2 μm. Dashed lines show supporting COMSOL simulation results.

Figure 4.9 (a) shows that increasing device length has a strong influence on threshold power. It is possible to take advantage of this trend to access extremely high operating temperatures. Figure 4.9 (b) depicts limiting response at 200 °C up to an input power of 35 dBm, with a small signal insertion loss of 1.5 dB. This is well over the standard power limiter operating temperature of 125 °C but still may be useful for extreme applications. For example, resilient super high temperature LCO limiters could be included in chips as a secondary protection against the harsh thermal gradients in space.

4.4 Failure Analysis

It is not only valuable to know the CW power handling maximum of the LCO limiters, but also by what mechanism the devices fail. In this section I analyze what we have observed

thus far to be three distinct failure mechanisms. Figure 4.10 exhibits SEM images of 6 devices post-test, with either different geometry or imaged after different test temperature.

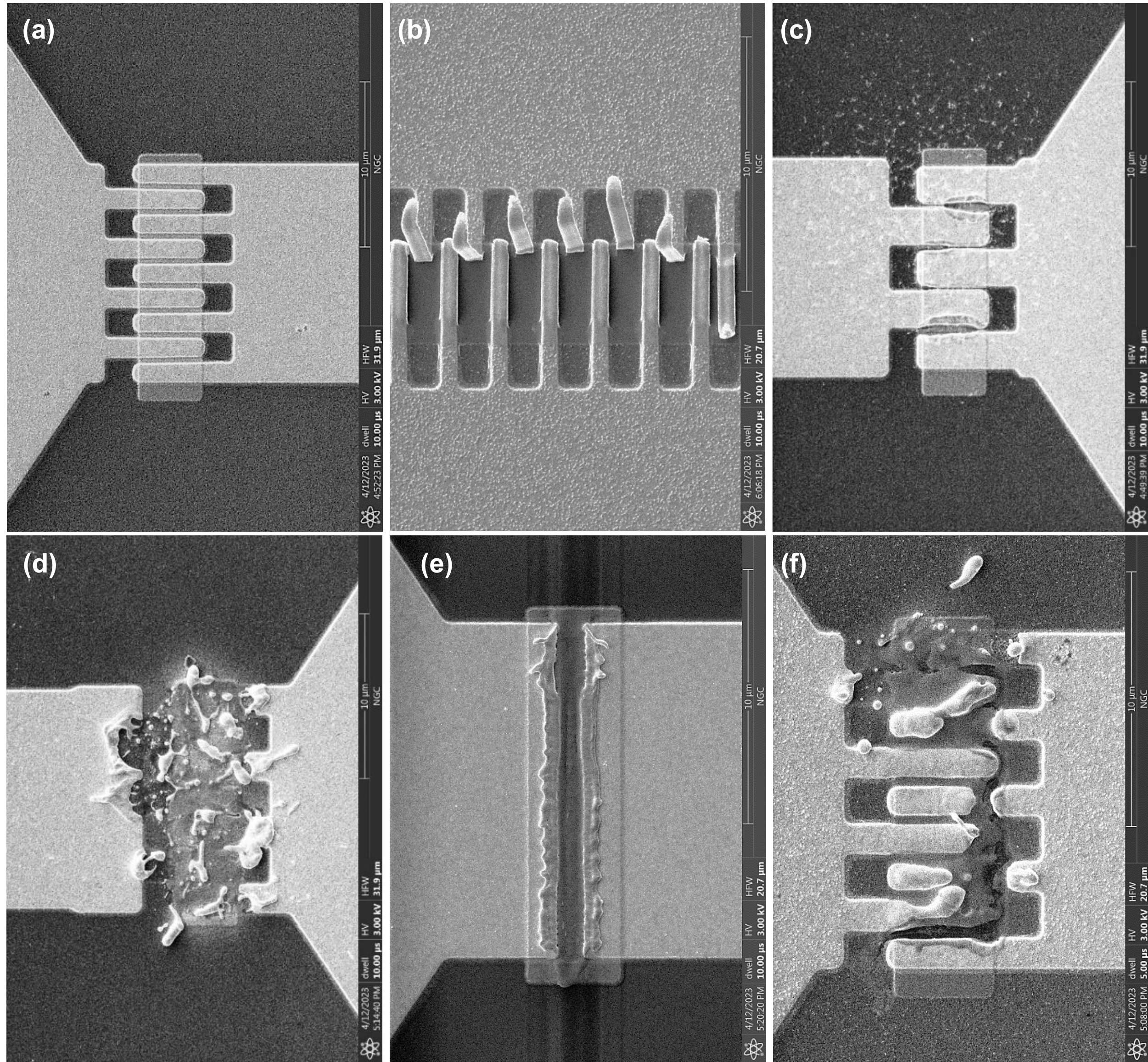


Figure 4.10: Images of shunt devices taken after -10 dBm to 40 dBm Pipo test. All are devices fabricated from 65 nm LCO sputtered on SiC. Given are the device dimensions and test temperature: (a) T = 1 μm, S = 500 nm, 25 °C (b) T = 500 nm, S = 500 nm, 25 °C (c) T = 2 μm, S = 500 nm, 25 °C (d) T = 1.5 μm, S = 500 nm, 75 °C (e) Linear L =1 μm, 175 °C (f) T = 1 μm, S = 500 nm, 225 °C

Figure 4.10 (a) depicts the only device configuration that could consistently survive repeated signals of power 40 dBm. Here SEM imaging showed no visible damage after high input power up to 75 ^{o}C. The first form of device failure we observed was delamination of

contact fingers from the LCO surface, as mentioned in section 4.3.1. We attribute this issue to the poor contact adhesion of noble metals such as Pd or Pt. This failure mode is only observed in very thin fingers with T = 800 nm or less, as depicted in Figure 4.10 (b). The fingers appear to curl away from the wafer surface, likely from thermal stresses.

In Figure 4.10 (c), we also depict devices with finger width T = 2 μm. Here, we see that the fingers remain adhered to the LCO surface. However, we can begin to see evidence of the next failure mechanism – contact melting. The LCO pad underneath the fingers appears undamaged, but the fingers themselves melt and migrate apart. This effectively increases device length S. As we know, device length determines power threshold for limiting. Thus, after contact melting the device fails back to the OFF state and allows signal to transmit, as the required input power to trigger blocking has increased.

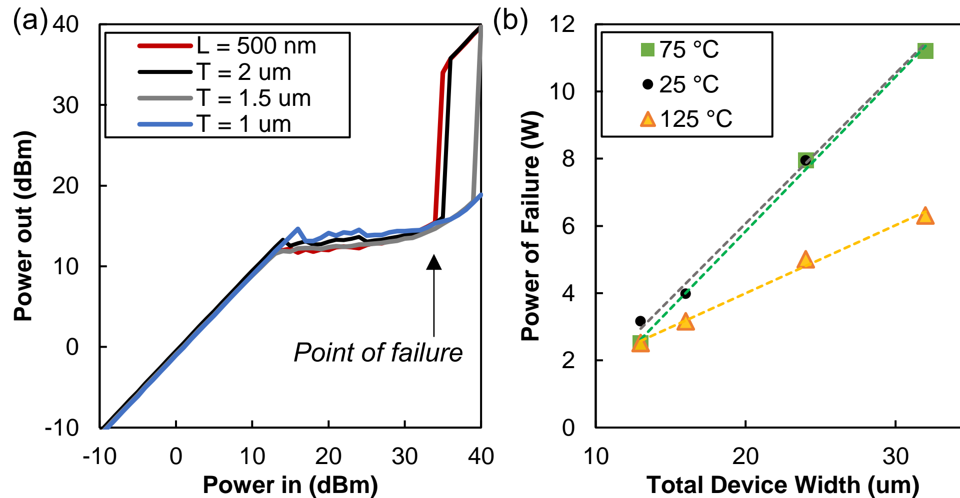


Figure 4.11. 2 GHz Pipo at 25 °C of all fabricated device limiters with device length 500 nm. This includes linear device L = 500 nm and interdigitated geometry with T = 2 μm, 1.5 μm, 1 μm. The P_{in} where the limiter response abruptly jumps back to the passing state corresponds with irreversible device point of failure B) Extracted point of failure in watts plotted as a function of total device width for limiters of device length 500 nm at 25 °C, 75 °C, 125 °C.

The reason why the limiter in Figure 4.10 (a) survives P_{in} of 40 dBm while the one in Figure 4.10 (c) melts comes down to device width. For linear geometry, device width is defined as W_{Lin} (See Figure 4.1 (c)). For the IDC structures, we define total device width as W_{IDC} ×

pairs of fingers (Figure 4.1 (d)). For all fabricated devices, the dimension of the LCO pad was set at $0.065 \times 4 \times 15\ \mu m^3$. Therefore, total device width for IDC structures decreases with increasing finger thickness T.

In Figure 4.11 (a), we present the overlaid PiPo results from a subset of limiters with device length S = L= 500 nm. As expected, all have the same power threshold of 16 dBm. However, the linear limiter, L = 500 nm, failed at the lowest input power. The linear geometry has the lowest total device width, $W = W_{LIN} = 15\ \mu m$. The device with the highest total width, that with IDC fingers of thickness T = 1 μm, survived to 40 dBm. In that case, total width = $W = W_{IDC} * 8$ pairs of fingers = 32 μm. In Figure 4.11 (b), we plot the extracted failure power as a function of total device width. Also shown are the extracted values for limiters of device length S = L = 500 nm tested at 75 ^{o}C and 125 ^{o}C. When the input power is converted from the dBm log scale to watts, we see a clear linear correlation between power of failure and total device width at all temperatures. Therefore, it is clear that higher total device width supports better power handling, as the fingers essentially act as heat transfer fins, and the more there are improves efficiency of heat dissipation to the contact peds.

Returning to Figure 4.10, we see that contact melting continues to be the primary failure mode as temperature increases. In Finger 4.10 (d), a device tested at 75 ^{o}C demonstrates dramatic melting and ejection of metal from the LCO surface, which still appears mostly undamaged. Even though the melting temperature of bulk $LaCoO_3$, which is 1750 ^{o}C [76], is similar to the melting point of Pt, 1768 ^{o}C, it appears that in these LCO devices the limiting factor for high power handling is currently metal resilience. However, the third the final failure mode that we identified, degradation of the LCO material itself, is observed in Figures 4.10 (e) and (f). At very high operating temperatures, it is clear that the LCO breaks down and cracks under thermal strain.

Figure 4.12 shows scanning transmission electron microscopy and EDS mapping data for the cross-section of a similarly damaged 2 -terminal device that was pushed to high powers and temperatures. Imaging and spectra were collected by EAG Laboratories in El Segundo, CA. Because the EDS data is a line-scan of a cross-section, it is thus essentially a depth profile of the imaged region. We observed that the LCO material has pulled away from the SiC substrate surface, and that melted Pt contact has migrated under it, possibly forming at Pt-Si alloy at the substrate surface. Furthermore, the overlapping La, Co, and Pt curves at approximately 120 nm along the x-axis of the EDS line scan indicates that the LCO and metal contacts may have also coalesced at these conditions. This data represents only initial compositional analysis of devices post-failure and should ideally be followed up with higher resolution imaging.

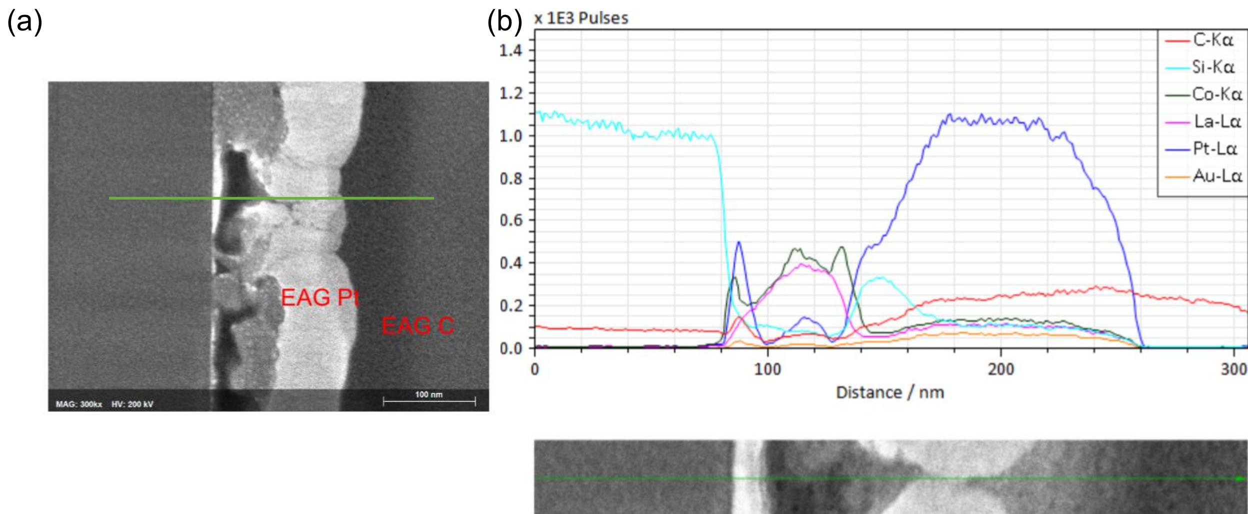


Figure 4.12 (a) STEM imaging for a 2-terminal device subjected to 20 V at 150 °C in order to force irreversible damage comparable to that produced by high temperature 40 dBm PiPo sweeps. Note that the STEM is a cross-sectional cut of the cut. The green line on (a) indicates the location of the EDS line scan in (b) acquired using a Bruker Quantax system. The carbon layer is from sample preparation. Note: higher C in Pt is due to overlap of C K-line with Pt N-line and thus does not reflect actual composition in that region.

With high-power experiments and SEM imaging, we were able to identify three key failure modes of the LCO limiters: contact delamination, contact melting, and LCO thermal

burnout. The first failure mode, contact delamination, can be easily avoided by increasing contact width. However, the emergence of the second failure mode, contact melting, is strongly dependent on total device width (which is inversely related to contact width "T"). Thus, as fingers cannot be used with T < 1 μm, we have identified an upper limit on total device width for LCO pads of dimensions 4 μm x 15 μm. In the next section, we propose changes to the device geometry that could improve power handling based on our analyses here. That being said, further testing would be useful to better understand how we can design better power capacity. For example, thermo-reflectance imaging of devices under test would help us identify heat distribution and at what peak temperature the thin-film LCO and metals degrade.

4.5 Simulation Predictions of Changes to Limiter Geometry

The COMSOL simulation of LCO shunt switches developed in this work provides an accurate prediction of device behavior, as shown in section 4.3.1. Further verification of model fidelity is provided in the Supplementary section 4.8.2. Therefore, it is reasonable to assume that we can utilize the simulation to design for better performance without having to physically fabricate and individually test a range of LCO limiters.

4.5.1 Increasing LCO Thickness

Many factors in scale, substrate, or configuration, can strongly influence limiter performance. For example, in Figure 4.13, we present the predicted tradeoff of higher insertion losses for reduced power threshold and lower flat leakage as the LCO thickness increases. The simulation geometry here is based on the LCO limiters on SiC of section 4.3.1, where the LCO pad is 40 nm thick and 4 μm by 9 μm laterally. The contact dimensions are T = 800 nm and S = 500 nm. Lower off-state resistance of thick films leads to higher insertion

losses. However, this also lowers on-state resistance and improves isolation as well as lowers the power threshold for limiting.

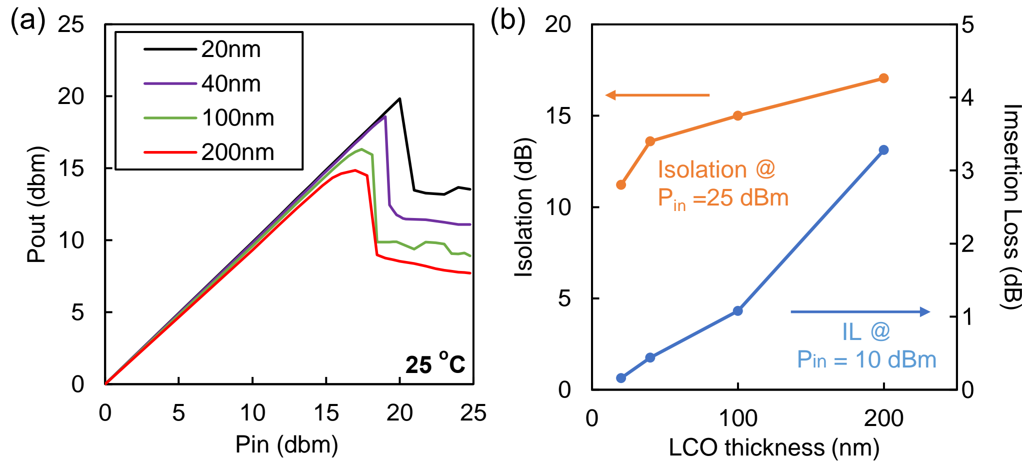


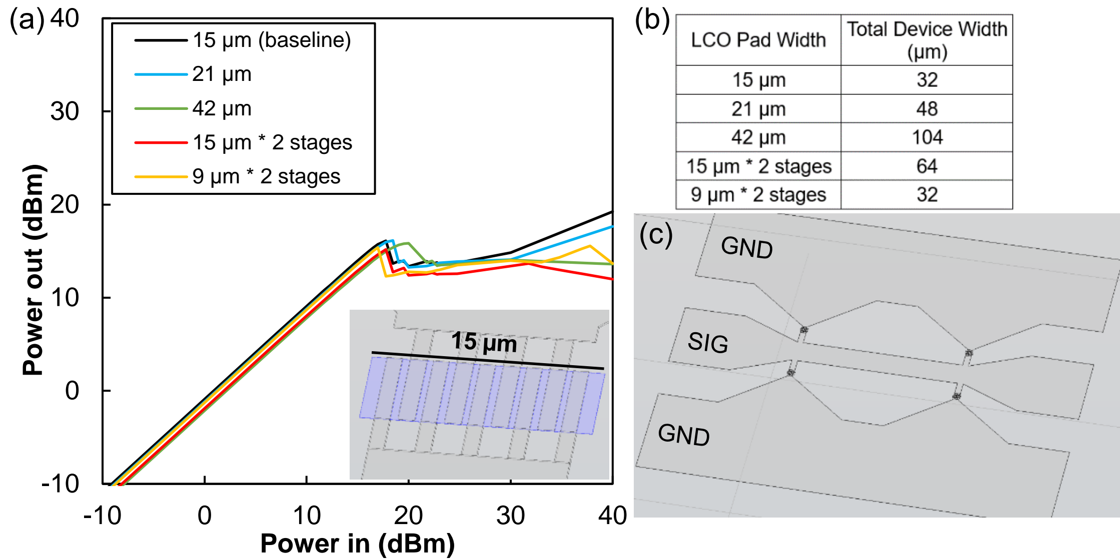
Figure 4.13 a) Model prediction of PiPo at 2GHz, 25°C, over varied LCO film thicknesses in nm. Power threshold decreases as thickness increases. (b) Extracted isolation and insertion losses.

4.5.2 Increasing Total Device Width

As shown in Chapter 4.4, increasing total device will help improve power handling capacity by improving efficiency of heat dissipation. At this stage, the model does not include calculation of any material deformation (no thermal expansion, contact delamination, high temperature oxygen loss, or metal melting and migration). Thus, there is no reason to expect that the simulation can predict failure, which is most likely due to those physical changes.

However, it is still worth exploring through simulation the other potential effects of the many different ways we could go about increasing total width. One way would be to increase the dimensions of the LCO pad, which for all wafer-scale fabrications thus far have been set at 4 μm by 15 μm. By lengthening the pad to 21 μm long, for example, we allow space for the addition of more pairs of interdigitated fingers. Another way of increasing effective total width could be to increase the number of limiting stages, as all devices thus far have only included one LCO pad at each GND-SIG junction. Figure 4.14 depicts the predicted PiPo

results for several of these proposed changes to geometry. The baseline geometry results were verified against measured data (Supplementary Figure 4.17).



LCO Pad Width	Total Device Width (μm)
15 μm	32
21 μm	48
42 μm	104
15 μm * 2 stages	64
9 μm * 2 stages	32

Figure 4.14 Simulation predictions for increasing total device width by either widening LCO pad or adding stages. (a) 2 GHz PiPo simulation, with inset specifying the dimension of interest (b) calculation of total device width for each set-up (c) screenshot of the two-stage 9 μm geometry

Widening the LCO pad for an IDC structure will provide space for additional pairs of interdigitated fingers. This will increase the capacitance of the structure, worsening the off-state insertion loss. This is reflected in the model simulation (Figure 4.14 (a)). Rather than do that, perhaps a better pathway to increasing total device width would be to use a multi-stage configuration. This geometry, depicted in Figure 4.14 (c), separates the IDC structures, thus reducing parasitic capacitances. Simulation results for the 2-stage configurations suggest that the limiters would experience a 2-stage power response. For example, the 9 μm * 2 stage PiPo results show the first limiting behavior at 15 dBm, and a second power threshold at 38 dBm when the second pair of LCO pads transition to the conductive state. Even though this configuration increases the overall device footprint, we propose that it could be worth significant improvements in limiter performance. It remains to be verified through fabrication and testing of real devices whether we will continue to see the same trend between power handling and total device width for multi-stage designs.

4.6 Benchmarking

Table 4.1: Benchmarking $LaCoO_3$ limiters against recent art at the research scale

Technology	Test Frequency (GHz)	[1]Test Temperature (°C)	[2]Insertion Loss (dB)	Flat Leakage (dBm)	CW Power Handling (dBm)	Device Area (mm^2)	[3]Max power density (W/mm^2)	Ref
GaAs Schottky diode MMIC	10	25	1.5	20	36	3.04	1.31	[77]
Integrated P-I-N LNA	30-36	25	0.45	-	39	2.1	3.78	[78]
3-stage SiGe CMOS	4-6	25	2	7.5	20	0.3	0.33	[79]
RF-MEMS Single stage	10.24	25	0.2	-	32	0.075	21.1	[80]
RF MEMS 4-stage	10.24	25	0.65	27	36	0.19	20.9	[80]
GaAs pHEMT	8-12	25	1	25	40	1.162	8.6	[81]
Multistage MMIC P-I-N	2-4	25 to 85	1.3	20	55	-		[82]
2-stage MEMS + gas discharge	1-3	25	0.2	26	47	-		[8]
CPW VO_2	10	25 to 50	0.6	17	33	0.25	8.0	[17]
Tapered VO_2	2	25	0.7	20	47	~0.5	100	[18]
This Work Section 4.3.1	2	25 to 125	0.5	10	20	0.11	1	[73]
This work Section 4.3.3	2	10 to 75	0.74	21	40	0.11	91	
This work Section 4.3.3	2	125	2	15	38	0.11	57	

[1]If not explicitly stated in journal paper, we assumed room temperature operation

[2]Insertion Loss measured at a maximum P_{IN}= 0 dBm @ 25 °C

[3]Max power density based on total device area, including contact pads, assuming all blocked signal is absorbed. Therefore, it may not directly correlate to active material power stability, nor account for what portion of input signal is reflected back to the source in the ON state

Table 4.2: Benchmarking $LaCoO_3$ limiters against commercial level L and S band products marketed for high temperature or high-power handling

Technology	Frequency (GHz)	Operating Temperature (°C)	[3]Insertion Loss (dB)	IL over T (dB/ °C)	Flat Leakage (dBm)	CW Power Handling (dBm)	Ref
Macom ® LM501202-M-C P-I-N	0.4-2.5	-65 to 125	0.6	0.003	[2]22	45	[83]
pSemi PE45361 UltraCMOS	1-6	-55 to 85	0.95	-	[1]16	50	[84]
RFuW RFLM-052402QC 2-stage P-I-N	0.5 – 4	-65 to 125	0.5	0.005	[2]17	53	[85]
Microsemi ® GG77317-04 Coaxial	3-4	-55 to 85	1.2	-	[2]13	50	[86]
This work Section 4.3.3	2	10 to 75	0.74	0.0122	[2]21	40	
This work Section 4.3.3	2	125	2 dB @ 125 °C		[1]15	38	

[1]Flat leakage defined at $P_{IN} = 30$ dBm
[2]Flat leakage defined at $P_{IN} \geq 40$ dBm
[3]Insertion Loss measured a maximum $P_{IN}= 0$ dBm and @ 25 °C unless otherwise noted

4.7 Conclusions

In this chapter, we reported on the fabrication and testing of numerous LCO-based radio frequency power limiters. Comparisons were made between various device configurations and dimensions. Results on three different substrates suggest that the thermal boundary resistance for sputtered LCO is very high, causing there to be very little influence of substrate on device performance, which could be both an advantage and a drawback. We further demonstrate that the LCO limiting response is reversible and highly repeatable. Additionally, we show that threshold power is tunable by adjustment of either device length (strongest dependence), LCO thickness (moderate), or operating temperature (weakest dependence).

Overall, the best performance was achieved by an interdigitated shunt switch based on 65 nm LCO sputtered on 4” SiC. This device showed limiting response over a broad temperature range (10 °C to 225 °C). Additionally, it demonstrated low insertion loss < 1 dB and power handling up to 40 dBm from 10 °C to 75 °C. For such a novel technology, the LCO limiters we have fabricated and tested in this work are highly promising, and even competitive to some commercial products in terms of insertion loss, operating temperature range, and power handling.

However, there are still ways to improve. To that end, we also conducted failure analysis of the devices after high power input and identified 3 progressive forms of irreversible failure: contact delamination, contact melting, and LCO degradation. We know that there are design tradeoffs to be considered for any technology. In these LCO limiters, we must evaluate the tradeoffs between ultra-low insertion loss (which requires a linear geometry) and high-power handling (which requires a large total device width). We proposed there may be a compromise reached through the use of a multi-stage configuration, which separates sets of interdigitated fingers by enough distance to reduce parasitic capacitances. Additionally, it may be possible to reduce the need for large device widths by improving the metal contact resilience. Currently, construction of LCO limiters is constrained to the use of noble metals such as Pt or Pd to avoid the formation of a parasitic oxide layer at the LCO – metal interface. However, this inherently worsens metal adhesion to the surface. We may be able to improve adhesion through the use of low-reactivity metals such as tungsten. Another avenue of exploration would be to engineer reduced interfacial thermal resistance through annealing or doping of the LCO film. Lastly, for more thorough assessment of the LCO switch performance we need to conduct spike leakage experiments, pulsed power endurance trials, high frequency testing (see Chapter 5), and low temperature measurements.

4.8 Supplementary

4.8.1 Supporting Data for 4.3.2

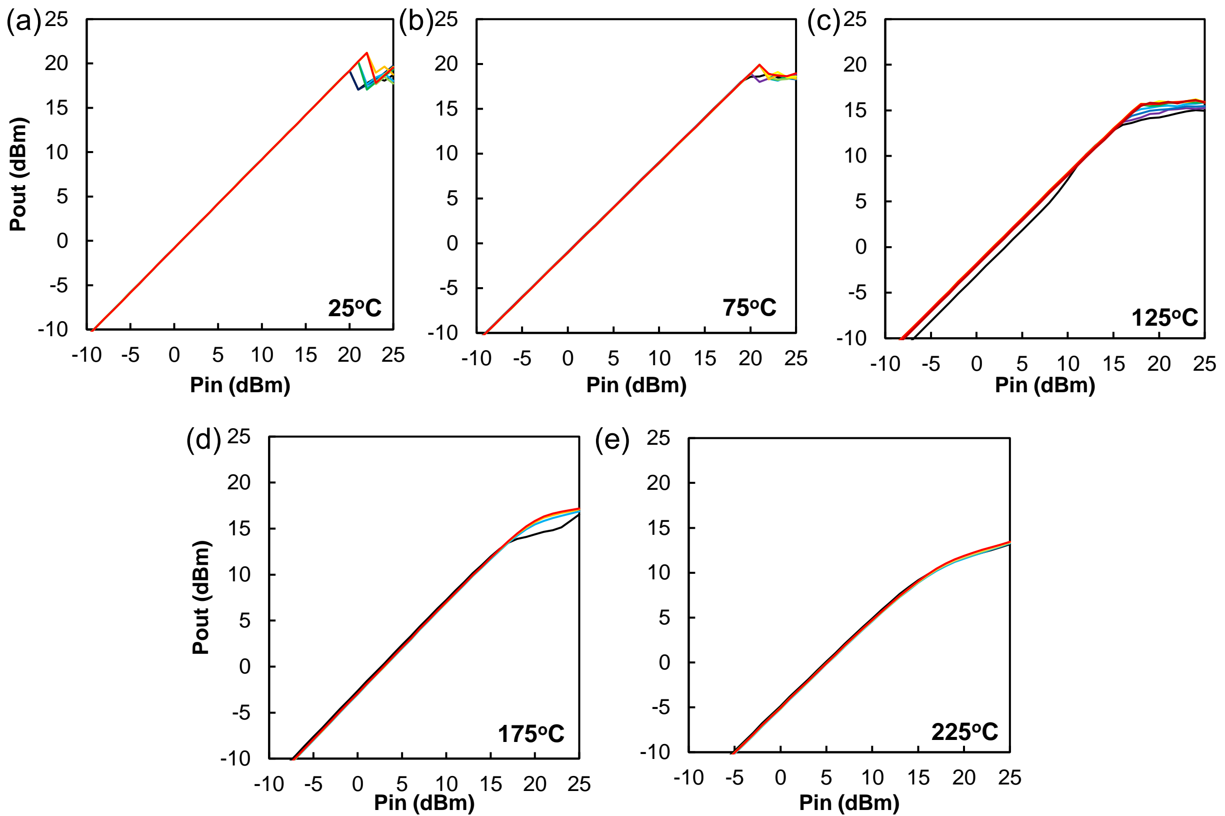


Figure 4.15 Repeated 2 GHz PiPo sweep results for interdigitated LCO limiter with device length 500 nm and finger width 1 µm. LCO is deposited 40 nm on SiC. The black line indicates the first run, and the red line represents device behavior that was repeated at least 5 times.
(a) 25 °C (b) 75 °C (c) 125 °C (d) 175 °C (e) 225 °C

4.8.2 COMSOL Simulation Accuracy against Measured Devices

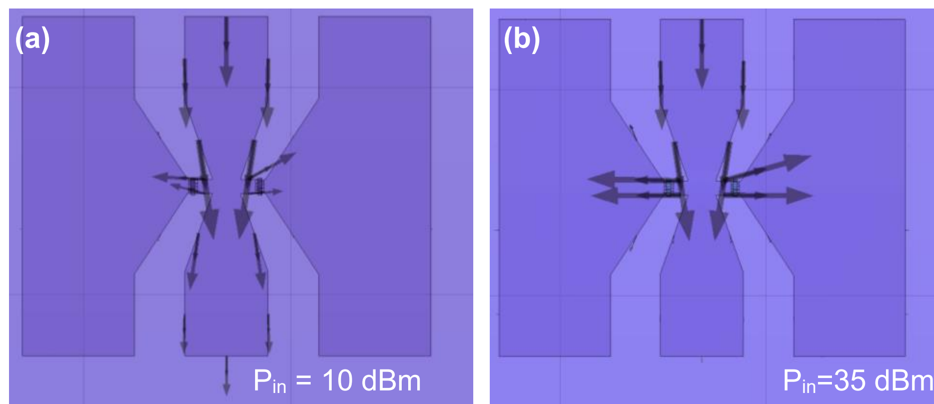


Figure 4.16. Model dimensions: Interdigitated configuration with T= 1 µm, S = 500 nm, W_{IDC} = 4 µm, LCO = 0.065 × 4 × 15 µm^3. Visualization of current density for (a) OFF state at Pin = 10 dBm (b) ON state at Pin = 35 dBm, showing that RF power is shunted through LCO pads at GND-SIG junctions

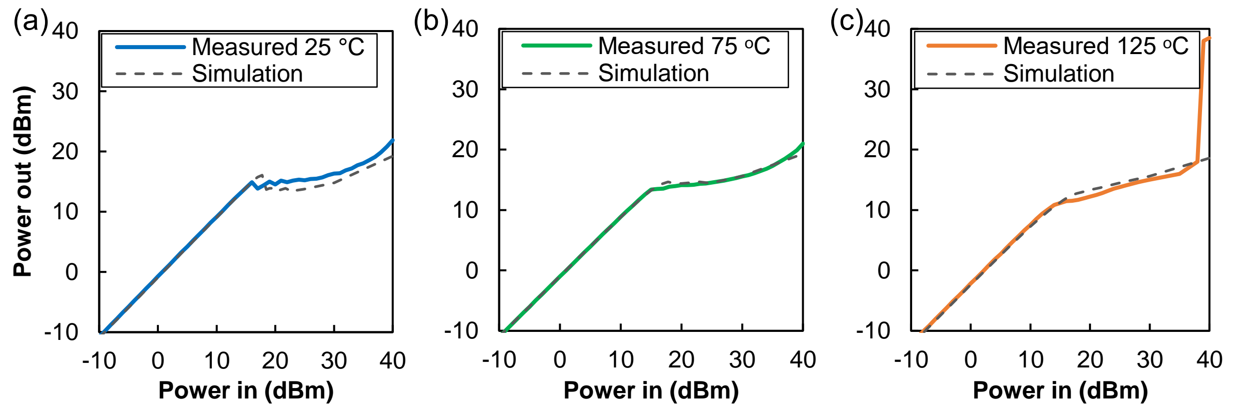


Figure 4.17 Comparison of measured PiPo data against simulated results at (a) 25 °C (b) 75 °C (c) 125 °C, showing the high accuracy of the model. However, while it predicts power response very well, the COMSOL simulation cannot predict failure, such as that observed at P_{in} = 38 dBm at 125 °C.

Chapter 5: High Frequency Performance and DC Bias Turn-on

5.1 Abstract

Important metrics for RF limiters include insertion loss, isolation, stability, and broadband performance. In the previous chapter we established that LCO is a strong candidate for the former three criteria, based on the S-band power-in, power-out experiments. Now, we explore the higher frequency band behavior. We expected that LCO itself, as a low dielectric constant semiconductor, will produce only modest frequency dependence. To verify this hypothesis, we utilized scattering parameter (S-par) measurements, which characterize signal propagation through an electrical network in terms of gain between ports of a device. S-parameter results are presented for LCO limiters across 0.1 - 50 GHz and from 25 °C to 125 °C. We present extremely low insertion losses, with a maximum IL of 1.2 dB at 125 °C and 50 GHz. This value is competitive with commercial 40 GHz P-I-N diode limiters.

Self-turn-on is an important operation mode of power limiters, to simplify construction and enhance response sensitivity. However, it may also be useful to be able to use direct current bias to tune the power threshold or force a switch to the blocking state. To that end, in this chapter we further characterize the LCO shunt response to voltage-driven DC bias alongside S-parameter measurements. We demonstrate that a voltage of 5 V is sufficient to abruptly turn-on the LCO limiter across the test temperature range. ON- state attenuation (between 14-16 dB) is broadband, with no frequency dependence.

5.2 Methods

A 2-port network is relevant for our device geometry. Complex S-parameters are given as the ratio of powers. As these devices are symmetric, reflection coefficients S_{22} and S_{11} are equivalent. Similarly, transmission coefficient $S_{21} = S_{12}$, so in this chapter, only S_{11} and S_{21} are reported. These values can also be converted to either scalar linear or scalar logarithmic

terms. In this report, we refer exclusively to the scalar logarithmic S-parameters in dB, with the relevant equations given:

$$\text{Gain [dB]} = -\text{IL [dB]} = S21 = S12 = 20 \log |S_{21}|$$

$$-\text{Return Loss [dB]}: S22 = S11 = 20 \log |S_{11}|$$

For power limiters, in the OFF state we desire as small insertion loss (low S21) as possible. In the ON state, the attenuation (S21) should be as high as possible over the entire frequency range.

5.2.1 S-parameter Set-up

For S-parameter testing, we used a Keysight PNA Network Analyzer N5245A calibrated over 0.1-50 GHz. Two-port off-chip short-open-load-through (SOLT) calibration was completed to move the reference plane of measurement to the end of the test cables and probes. Measurement uncertainty is +/ 0.1 dB. Input power is 0 dBm, small enough signal that it is not expected to trigger the LCO IMT alone, so that we can further explore DC bias effect. To apply DC bias in S-parameter testing, bias-tees are placed in series with the probes (100 μm pitch) on either end of the signal line in the device-under-test. We used a Keithley 2420 source meter, with 60 W max output power. Note: Bias tees can only handle 1 W max (30 dBm). Compliance current was set to 1250 mA to protect both DUT and bias tees. All devices tested in this chapter were fabricated from 40 nm LCO sputtered on 4" SiC.

5.3 Results

5.3.1 Effect of Temperature on Loss

In this section we characterize the temperature-dependent frequency response of linear shunt LCO limiter with device length L = 500 nm, The volume of the LCO pads at the GND-SIG junctions are $0.04 \times 4 \times 15$ μm^3.

At room temperature (Figure 5.1 (a)), S11 is approximately -27 dB across the entire frequency range 100 MHz to 50 GHz. Return loss (S11*-1) describes how much signal is reflected from the device and can be increased by an impedance mismatch. A high return loss indicates good impedance matching, where 60 dB typically indicates perfect matching, and 15 dB is a standard industry minimum. These results indicate that the LCO limiters are very well-matched to a 50 Ω load to high frequencies.

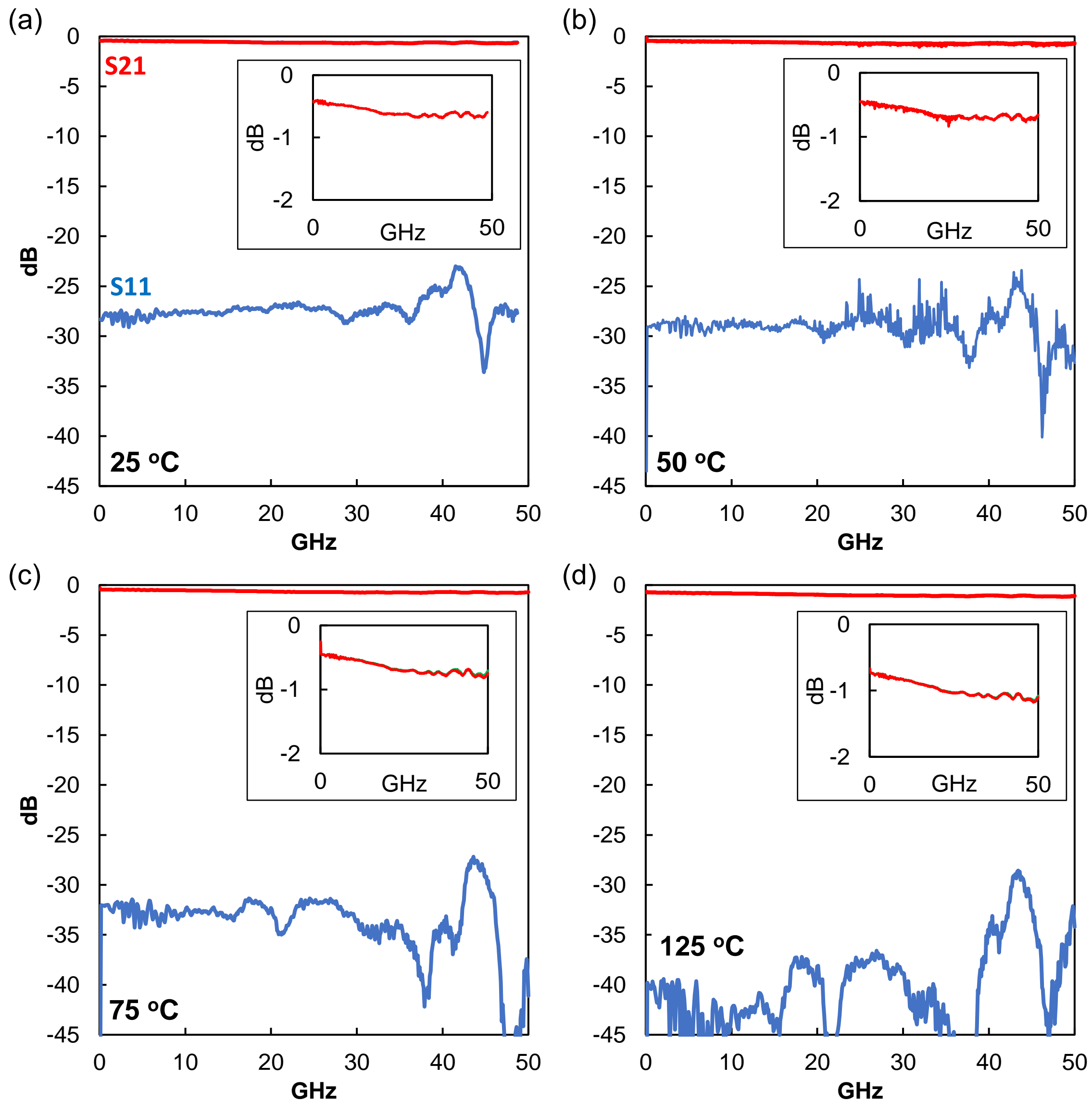


Figure 5.1. S-parameter measurements for 0 V bias on linear LCO shunt limiters with device length L = 500 nm. Transmission S21 is depicted in red, and reflection S11 in blue. Insets depict zoom in for S21 for better comparison of insertion losses at (a) 25 °C (b) 50 °C (c) 75 °C (d) 125 °C

At room temperature, the insertion loss remains below 1 dB up to 50 GHz. There is a slight increase in IL as frequency increases from worsened capacitive losses. Capacitive reactance, which is a materials opposition to voltage change, is $X_C = 1/(2\pi f C)$ and reduces with increasing frequency. At the limit $f \rightarrow \infty$ capacitive reactance goes to zero, and the line behaves as a short circuit. The fact that the insertion loss of the device doesn't worsen much indicates that the frequency dependence of the dielectric constant of LCO is either very low or that the permittivity decreases at high frequencies. This result validates the broadband usage of LCO in microwave devices, where capacitive losses are often a significant problem.

The temperature-dependent insertion losses as measured by S-par complement the previous PiPo experiments. In both measurements, there is a slight increase in insertion loss with increasing temperature. Only at 125 ^{o}C and at about 20 GHz does the insertion loss reach 1 dB, verifying suitable small signal operation of the limiters at high temperatures.

The LCO limiter insertion loss characteristics compares extremely favorably against commercial products, even surpassing some high frequency P-I-N diode-based limiters. For example, the Keysight N9355F limiter is advertised as a broadband protector operating from 0.1 to 50 GHz. The N9355F only achieves 2 dB insertion loss up to 26.5 GHz, with poorer insertion loss of 3.5 dB at 50 GHz and CW power handling of 45 dBm [87]. Another example is the Marki HLM-40 High Power 40 GHz Limiter. This product has good insertion loss characteristics, with a maximum insertion loss of 1.5 dB at 40 GHz, on par with our device, but only 36 dBm CW power handling [88]. Of course, this is not an extensive comparison, and both high frequency power handling and switching speed experiments must be conducted for thorough benchmarking of the LCO limiters. Nevertheless, based solely on frequency and temperature dependent insertion loss characteristics, the LCO limiters can easily compete with broadband commercial P-I-N diodes.

5.3.2 *DC bias Turn-on, Linear Device*

In this section we show that voltage driven DC biasing of LCO shunt switches can be used for abrupt turn – on to the limiting state. The following measurements were conducted on linear configuration with device length 500 nm.

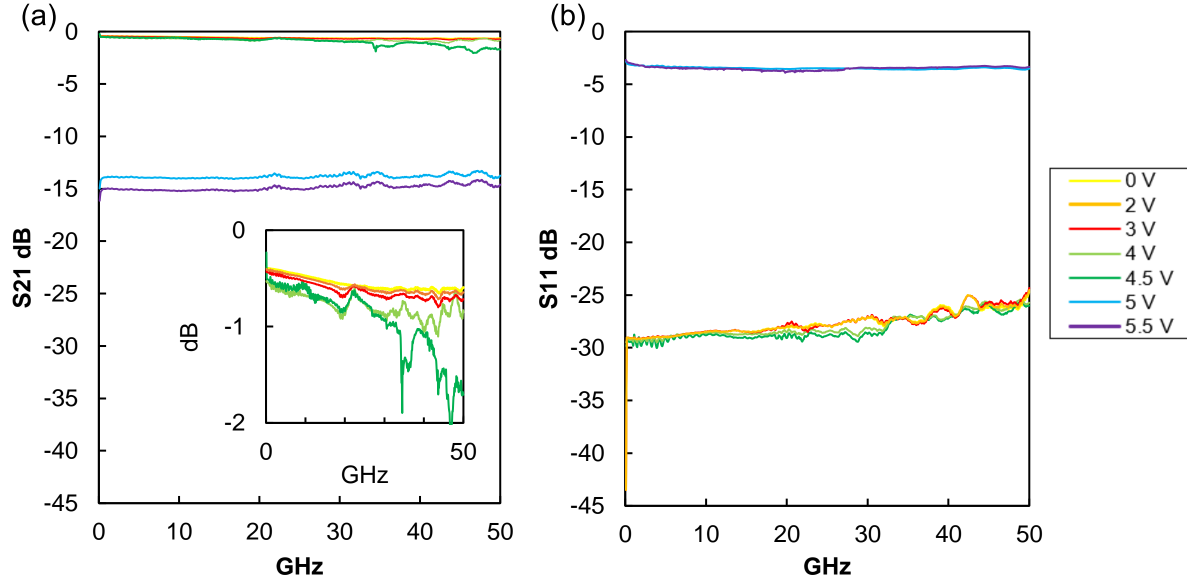


Figure 5.2. 2-port S-parameter measurements at varied DC voltage bias on linear LCO shunt limiters with device length L = 500 nm at 25 °C. (a) Transmission, S21. Insets depict zoom-in for better comparison of insertion loss before the threshold bias switch of 5 V (b) Return Loss S11

Figure 5.2 (a) depicts the transmission S-parameter S21 up to 50 GHz with varying voltage bias, while Figure 5.2 (b) illustrates the corresponding S11 data. From the 0 bias case up to 4.5 V, the LCO limiter remains in the OFF, passing state. With increasing bias, we see very slightly increasing frequency-sensitivity and the insertion loss gradually increases as well. However, at 5 V bias the device switches abruptly to the ON, limiting condition, with an S21 attenuation of 14 dB. We attribute this to a voltage triggered abrupt insulator to metal transition. The magnitude of the voltage threshold is similar to that observed for previously tested 2 terminal DC switches of length 500 nm (Chapter 3.3.2). Increasing the voltage bias to 5.5 V slightly further increases isolation. We also observe that the return loss of the limiters abruptly drops to 3 dB upon voltage bias of 5 V. This implies that the LCO

limiter impedance changes with IMT, and that blocked signal is not only absorbed into the ground pads, but is also reflected back to the source.

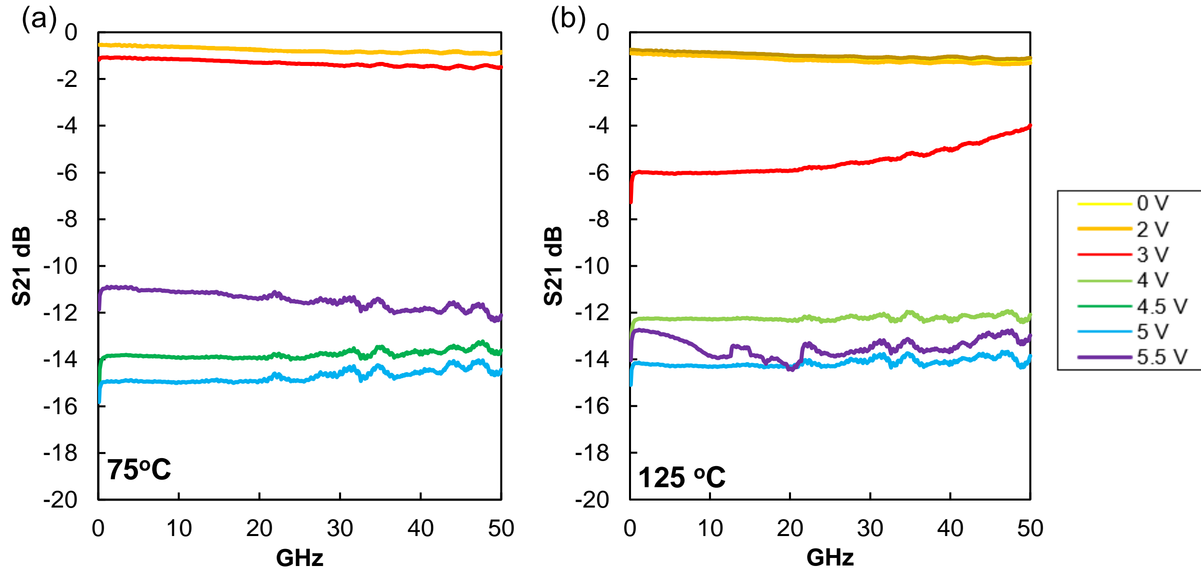


Figure 5.3: Transmission S-parameter S21 measurements at varied voltage bias on linear LCO shunt limiters with device length L = 500 nm at (a) 75 °C (b) 125 °C

DC bias experiments at higher temperatures also mirror the previously conducted 2 - terminal voltage triggered results of Chapter 3, in that threshold voltage decreases with increasing temperature. We observed that at 75 °C, the threshold voltage is 4.5 V bias. The device deteriorates at 5.5 V bias, with the attenuation actually worsening. Furthermore, after this event, we could not recreate the bias turn-on of the device again, indicating permanent damage. As this irreversible phenomenon was not seen at 25 °C, we infer that the increased temperature accelerated burnout or thermal stresses within the device, as was also observed in PiPo measurements in Chapter 4. At 125 °C the threshold voltage is less abrupt, as the LCO material's starting condition is already closer to its metallic state. At 3 V bias, the switch transitions partially to an attenuation of 5-6 dB, before fully transitioning by 4 V. Irreversible damage is again recorded at 5.5 V bias. Overall, regardless of operating temperature, once the LCO limiter switches to a blocking state, attenuation performance is broadband and flat across the frequency range.

5.3.3 High frequency behavior, Interdigitated geometry

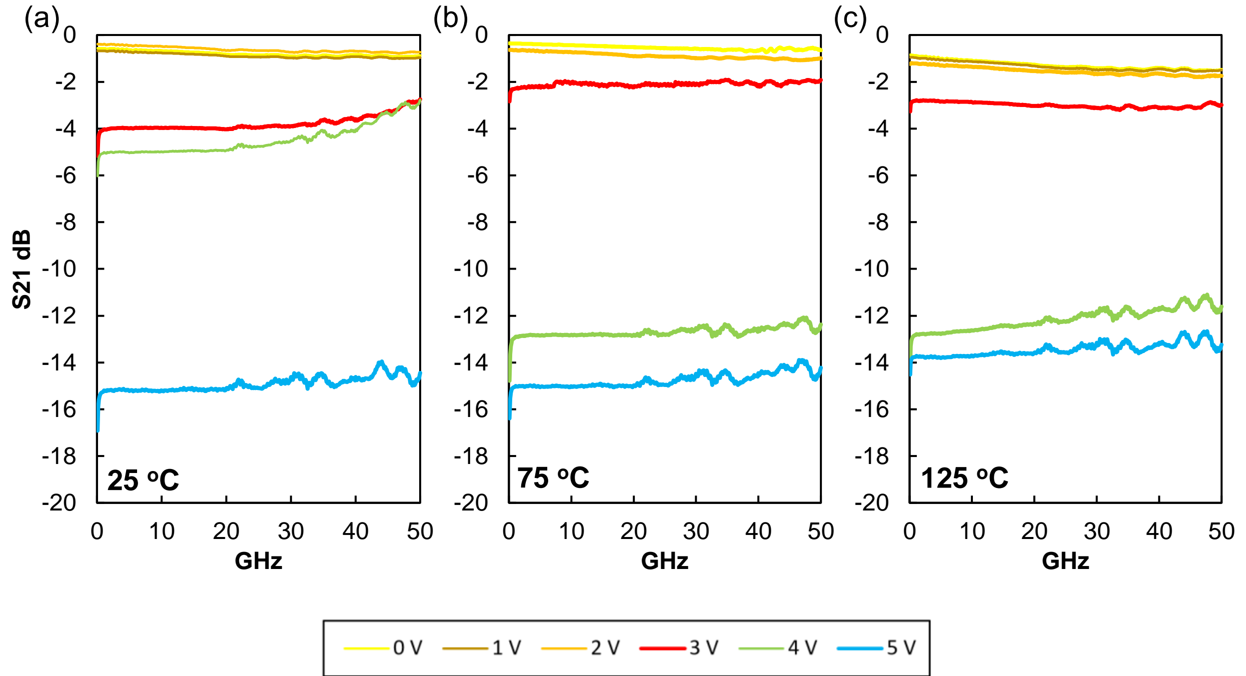


Figure 5.4: Transmission S21 measurements at varied DC voltage bias on interdigitated LCO shunt limiters with finger dimensions T = 1 μm, S = 500 nm at (a) 25 °C (b) 75 °C (c) 125 °C

In Figure 5.4 we present key results from the same S-parameter DC bias experiment conducted on an interdigitated LCO limiter with finger width T = 1 μm and spacing S = 500 nm. Overall, insertion loss performance is worse for the interdigitated devices due to increased capacitive effects especially at higher frequencies. This is not directly because of the LCO material, but instead due to the greater number of parallel plate capacitors formed between the parallel metal contact fingers. Otherwise, the same trends for DC bias effect are seen, with increasing temperature reducing the threshold voltage for switching, albeit less dramatically. On-state isolation at 5 V bias at all temperatures remains at about 14-15 dB up to 50 GHz. For comparison, P-I-N diode limiters can require from about 3 V_{DC} up to 25 V_{DC} forward bias for external turn-on [89,90].

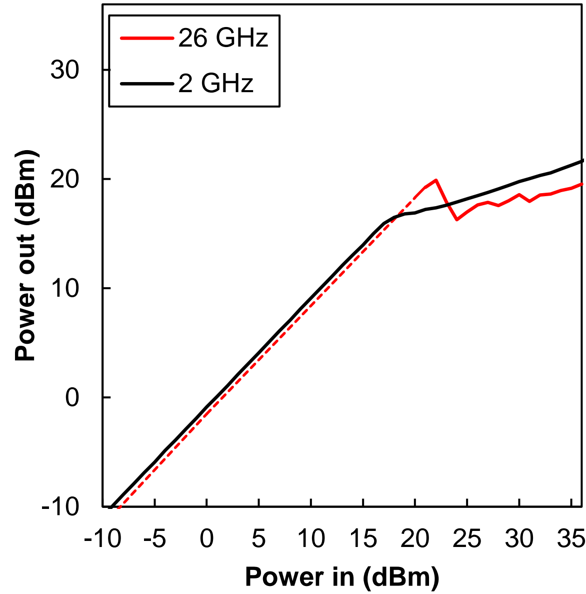


Figure 5.5 125 °C PiPo sweep for interdigitated limiter, device length S = 500 nm at both 2 GHz and 26.5 GHz operation. Note: the power amplifier available could only provide input power from 20 to 36 dBm at 26.5 GHz. Dashed lines indicated extrapolated small signal response.

Due to limited access to equipment, we were not able to entirely repeat the PiPo experiments of Chapter 4 at higher frequencies. However, we were able to conduct one set of measurements at 125 °C and 26.5 GHz. The results are given in Figure 5.5 for an interdigitated configuration with device length 500 nm. Overlaid on the same graph is the corresponding PiPo measurement at 2 GHz, highlighting the low frequency response of device behavior. The 26.5 GHz insertion loss in the PiPo sweep (1.7 dB at P_{in}=20 dBm) is the same as that observed in the 0 V bias S-parameter measurement.

5.4 Conclusion

The LCO limiters reported in this chapter consistently perform low frequency sensitivity up to 50 GHz, with strong indication that the material itself is appropriate for application across a broad range of frequency bands. Future improvements on these designs would come primarily from changes to the metal geometry and substrate to reduce capacitive losses. For example, we could construct high frequency structures where the input and output

ports are spread farther, to reduce coupling losses. We could also reduce the area of the GND-SIG pads. The strongest improvement would come from avoiding interdigitated geometry altogether. However, we would then run into the same power handling issues discussed in Chapter 4. It is crucial to improve upon the thermal stability of the contacts before we can simultaneously succeed in both high power and high frequency characteristics. Additionally, future work in the area of external bias would be to determine if it is possible to tune threshold power during PiPo testing. We also do not yet know the effect of voltage bias on the transients of the RF power response. Thus, it would be beneficial to conduct spike leakage experiments at high frequency with and without DC bias.

Chapter 6: $LaCoO_3$ - Beyond Power Limiters

6.1 Summary

In this thesis thus far, I have primarily focused on the promising application of lanthanum cobalt oxide for high temperature broadband power limiters. However, the unique insulator to metal transition characteristics of LCO also make it a strong candidate for several additional thermally or electronically driven switching applications. For example, we fabricated a set of series LCO RF switches (results shown here are reprint from [73] © IEEE 2022), which demonstrated self-turn on to the passing state upon increase of input power. The devices were also shown to be activated by 30 mA current-controlled DC bias. The linearity of the RF switch was characterized, and it showed a crossover point of greater than 35 dBm about 2 GHz. Finally, the bit error rate (BER) was demonstrated to be a low 10^{-9} at 6 dBm of 40 Gbps signal. With further optimization, series LCO switches could be used in conjunction with the shunt configuration to enable more complex RF networks. To conclude, I provide discussion on future directions of research and comment on both the strong advantages and possible drawbacks of LCO technology.

6.2 RF Series Switch

6.2.1 Design and Fabrication

The fabrication method for the series switch was conducted similarly to the shunt device. First, blanket sputtered 40 nm LCO was wet etched down to a 20 μm x 10 μm pad with diluted HCl. Palladium contacts were defined on top by e-beam lithography and e-beam evaporation on 1 cm^2 chips. The LCO pad is placed at the center of the signal line (Figure 6.1). The finger dimensions are T = 500 nm, S = 200 nm, W_{IDC} = 1 μm. As these fingers were thin, delamination at high input powers were a concern, so 2 GHz PiPo measurements were only taken from -20 to 18 dBm.

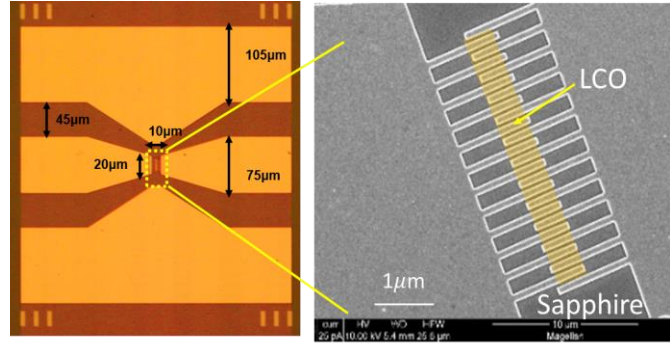


Figure 6.1 G-S-G coplanar waveguide based two-terminal LCO RF Switch on sapphire substrate consisting of interdigitated Pd metal contact fingers with 200nm spacing, 500nm width and 40nm LCO thickness. Left is image of layout, right is false-colored SEM image [73] © IEEE 2022

6.2.2 Results

The following results on the LCO-based series switch were collected in collaboration with the University of Notre Dame, reprint from [73]© IEEE 2022. Results from the PiPo sweeps are shown in Figure 6.2 (a). There is no measurable compression of the output power (P_{out}) up to 18 dBm input power (P_{in}). Isolation up to P_{in}=15 dBm is shown, even at 125 °C. However, we do then see self-turn on of the switch. The threshold turn-on power seems to increase at lower temperatures, as self-turn is not observed at room temperature.

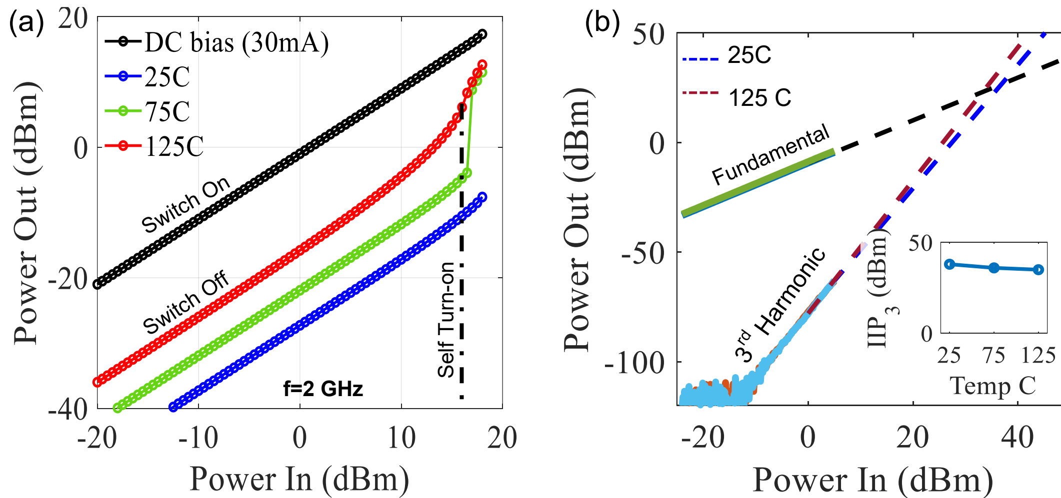


Figure 6.2 (a) 2 GHz PiPo sweep of LCO series switch from room temperature to 125 °C. Switch is OFF with variable small signal isolation of 30 to 15 dB depending on test temperature. Switch is turned to the ON state with 2 dB insertion loss with 30 mA bias. (b) IIP3 characterization of switch in ON state (with 30 mA bias) [73]© IEEE 2022

With the application of current-controlled DC bias of 30 mA, we can actively turn the switch on for any input power. At all operating temperatures the ON -state behavior was identical and is depicted in the black curve in Figure 6.2 (a). There is 2 dB of insertion loss in the ON state. We imagine this value can be improved by increasing the finger spacing and reducing the number of fingers to reduce capacitive losses. However, doing so would necessitate higher DC bias for turn on and overall greater power consumption. The cutoff frequency was estimated by equivalent circuit modelling (F_{CO} = 3.2 THz).

The linearity of the RF switch is calculated by passing a dual tone signal with closely spaced frequencies and measuring the power of any higher order harmonics introduced due to the switch (Figure 6.2 (b). Across temperatures from 25 °C to 125 °C the LCO switch shows greater than 35 dBm IIP3 crossover point. IIP3 crossover is defined as the P_{in} at which the P_{out} of the 3rd order harmonic overtakes the P_{out} of the fundamental frequency.

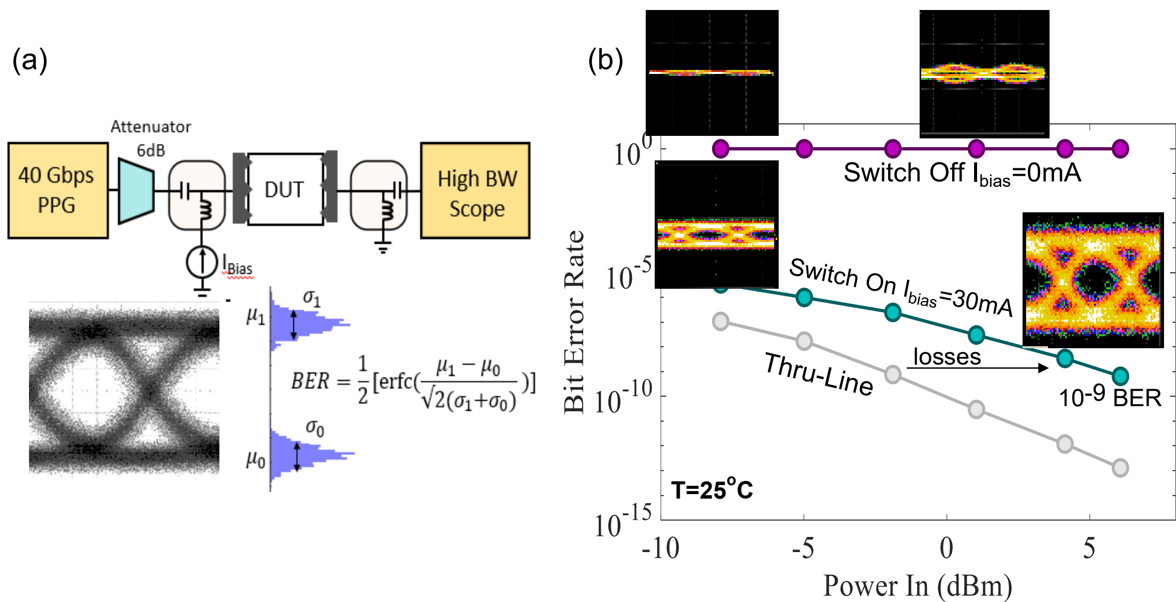


Figure 6.3 (a) Measurement setup for high frequency pulse throughput across LCO Switch at 25 °C. (b) LCO Switch shows less than 10^{-9} BER at 6 dBm of input power in the ON state with no spurious throughput of input signal in OFF State as seen by Eye diagrams [73] © IEEE 2022.

Lastly, in order to evaluate the ability of the series switch to transmit meaningful signal, we measured the throughput performance. A 40 Gbps signal was passed across the

switch at 25 °C (Figure 6.3 (a-b)). The signal was completely blocked in the OFF state as evidenced by the 'closed' eye diagram. The Bit Error Rate (BER) was extracted from the spread in the output Eye diagram histogram. It passes through the switch in the ON state with less than 10^{-9} bit error rate at 6 dBm input power, which is a generally acceptable value for the telecommunications sector.

A proof-of-concept linear configuration (no interdigitated fingers) was also fabricated using 65 nm LCO on SiC, with an LCO pad at the center of the signal line. Here, the device length is 2 μm and width of the junction is W= 4 μm. Results of a 2 GHz PiPo sweep at 75 °C are given in Figure 6.4. The setup was the same as described in the methods section of Chapter 4. Without the thin fingers, the power handling of the switch is much better, so we were able to push the device and tested to 40 dBm.

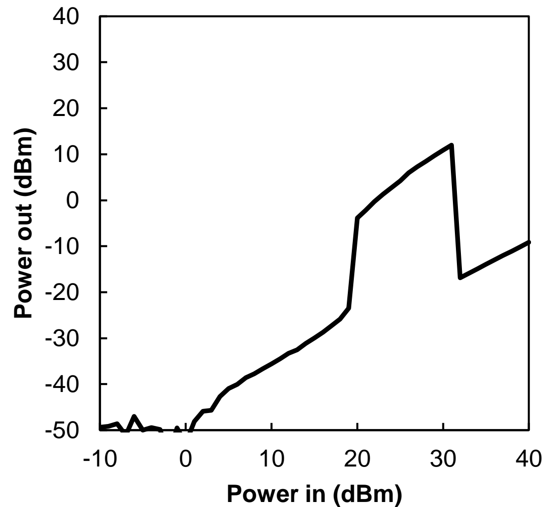


Figure 6.4 Series LCO switch with linear geometry of device length 2 μm.
2 GHz PiPo sweep at 75 ˚C.

The OFF state small signal isolation is not constant, indicating that with increased input power, the LCO gradually heats and allows a small amount of signal through before a critical abrupt transition at 20 dBm to a turned-on state. The isolation is an impressive 50

dB at 0 dBm input power, indicating almost complete blocking of signal. At P_{in}= 17 dBm, the isolation is closer to 45 dB.

Above the threshold power of 20 dBm, insertion loss is still quite high (20 dB), indicating that the LCO ON state resistance is simply too high. This can be improved by reducing the device length (which would likely also reduce power threshold and sacrifice OFF state isolation). At the failure point of 31 dBm, we observed the same failure mechanism as was seen for the high power tested linear shunt limiters. First, the contacts melted, then the LCO material itself cracked under thermal strain. While this device's performance is far from ideal, it represents an initial stage in design. With further optimization of geometry, the LCO series switch too may achieve the competitive characteristics of high-power handling and low insertion loss of the LCO shunt limiters.

6.3 Other avenues of research

Besides in discrete power limiters, $LaCoO_3$ could also potentially be very useful in other forms of power dissipation and thermal management. One simple mechanism would be direct integration of LCO material at the gate electrode of an LNA or beneath any sensitive component. Upon overheating, the LCO would transition to a conductive state, providing high sensitivity in a small, focused area while reducing the need for active cooling. This could function as both a signal attenuator and an integrated thermal fuse. LCO, with its' low dielectric constant and low frequency response, would present very little loss characteristics to the adjoining unit. Furthermore, the non-structural phase transition, being both thermally resilient and reversible, could offer minimal expansion stress. It should be noted that one significant drawback of LCO is the necessity of high temperature sputter deposition to form crystalline films. As BEOL interconnect processing is often constrained to 450 ^{o}C maximum, we would need to find alternate methods of deposition. Perhaps the issue could be addressed

through some form of rapid thermal annealing or thin-film transfer of crystalline films *via* wafer bonding technology.

Future explorations of $LaCoO_3$ devices may even move beyond the realm of thermal fuses and RF receivers. Thin film LCO is eligible for many of the same resistive switching technologies as its lower temperature predecessor vanadium dioxide. LCO provides the advantage of high temperature operation at possibly the drawback of less dramatic response in certain testing conditions compared to VO_2. Because of the inherently broad temperature gradual IMT mechanism, usage of bulk $LaCoO_3$ is constricted, as external stimulus would have to be of large magnitude to trigger any significant response. Furthermore, LCO cannot be triggered to complete an IMT strictly through electric field actuation alone – there must always be a thermal component. However, a short list of possible use cases could include resistive switches for neuromorphic computing, as a selector material in cross-point architecture, thermochromic coatings, or in optical modulation. Additionally, Lanthanum cobalt oxide itself has not been thoroughly investigated – we still don't fully understand the spin-state transition mechanism, or how we could further modulate the IMT through strain, stoichiometry, defect, or domain engineering. These unexplored routes imply that the field of LCO-based technology is still in its early stages, nascent but full of opportunity for stimulating research.

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