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SANTA CRUZ

HIGH STABILITY CURRENT SUPPLY FOR ELECTRON MICROSCOPY

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ELECTRICAL ENGINEERING

by

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List of Acronyms

AMP	Amplifier
BW	Bandwidth
CMRR	Common mode rejection ratio
dB	Decibels
EF	Emitter follower
F	Farad
GBW	Gain Bandwidth
GND	Ground
H	Henry
Hz	Hertz
K	Kelvin
KHz	Kilo Hertz
LDO	Low Drop Out
LPF	Low-pass Filter
MHz	Mega Hertz
ms	millisecond
ns	nano second
OSC	Oscillator
pF	picofarad
p-p	peak to peak
ppb	parts per billion
ppm	parts per million
PSR	Power-Supply Rejection
PSRR	Power Supply Rejection Ratio
PTC	Positive temperature coefficient
rms	root mean square
SYNC	Synchronous
TC	Temperature Coefficient

ABSTRACT

HIGH PRECISION CURRENT SUPPLY FOR ELECRON MICROSCOPY

by

Maryam M. Motamedi

With the advent of aberration corrected electron microscopy, the need for ultra stable power supplies for controlling the currents in magnetic lenses becomes one of the limiting factors in attaining atomic resolution. When we talk about resolution and depth of the field it is always assumed that all the components of the microscope are perfect and will focus the light/electron from any point on the object to a similar unique point in the image, but this is not the case because of the lens aberrations and diffraction. Unlike light optics, where lenses are used to refract and bend light rays for image formation, in electron optics magnetic lenses are used to do the same thing. Magnetic force is used to change the direction of electrons in the same way that a lens changes the direction of light rays. Therefore one of the limiting factors of resolution in electron microscopy is variation of the current that creates the magnetic field. With the advancement in lowering aberrations in electron microscopic lenses the need for higher stability in the lens current supplies becomes paramount. In order to achieve resolution of 0.5 angstrom level or better we need current supplies that are stable up to 1 part in 10^{-8}. In this work, the aim is to design a high stability current supply capable of producing 1 Amp of current within 0.01 parts per million (ppm) of stability for electron microscopy. In this thesis, an ultra stable current supply was designed and simulated. The stability of the current is 0.0086 ppm/^{o}C, over 15 minutes which is within the range that is required for this design.

DEDICATION

I would like to dedicate this Doctoral dissertation to my beloved family and especially to my dearest baby boy Darian.

ACKNOWLEDGMENTS

First of all, I would like to thank my dearest husband for his nonstop encouragement throughout the years of my studies. I would have not been able to reach my goals without his enormous support over the years. In the same token, I'm extremely thankful to my parents and my brother who have always been there for me and supported me emotionally. They are the ones who built up the foundation of my thoughts and my goals. I would like to thank them for loving me unconditionally and extensively. I also would like to thank my dear friends and extended family members who have helped me throughout the years by their love and support.

My sincere appreciation and gratitude goes to my dear advisor Dr. Michael Isaacson. His guidance has been invaluable to my research as well as my career. I'm also grateful for the advice, recommendations, and support of Dr. Joel Kubby, Dr. Athanasios Kottas, Dr. Holger Schmidt, and Dr. Ali Shakouri throughout my graduate studies and in various examination committees. I'm very thankful to my supervisor at Lockheed Martin Space Systems, Mr. Bill Hennig, who has been extremely considerate, helpful, and supportive over past three years. I also would like to thank my dear colleagues for their insightful comments and technical support.

In hopes of
worldwide peace and individual liberty!

Chapter 1

Introduction

Electron microscopes have become instrumental in many areas of materials and life science. In particular, with the advent of research in nanotechnology, there is the need for a tool to characterize materials at the nm to 0.1nm scale. Generally, the wavelength that is used to visualize an object must be smaller than size of the object that is to be observed due to the diffraction. The resolving power of a light microscope is limited by the smallest wavelength of light, which is about 250 nm. In observing objects smaller than the wavelength of 250nm down to the size of an atom or even smaller, an electron microscope must be used.

In a light microscope, a glass lens refracts light waves. In electron microscopes magnetic lenses accomplish the same task. Electrons carry a charge, so that when they pass through a magnetic field their trajectories are bent. The degree to which they are bent is related to their speed and the strength of the magnetic field as shown by equation (1.1):

$$F = qv \times B \qquad (1.1)^{1}$$

where B is strength of magnetic field, q is the electron charge and its value is $1.6\times10^{-19}C$, v is the charge's velocity.

The strength of the magnetic field inside an infinitely long solenoid is shown below (1.2):

[1] Reference (1)

$$B = \mu_o nI \qquad (1.2)^2$$

where μ_o = permeability of free space,
n = number of turns per unit length of wire, and
I = current.

In following chapters, the exact relationship between the field, focal length, and the current is shown.

The aberrations in optical lenses limit the ultimate resolution that can be achieved. A magnetic lens will also have aberrations that could, consequently, limit its ultimate resolution. The aberrations and the ultimate resolution that can be achieved by a magnetic lens are limited by the stability of the current that is producing the field. For this reason, it is fundamental to design an extremely stable current supply with stability as high as possible.

One of the most important characteristics of a current supply is the degree of stability with which it can deliver current. The external variables, such as temperature, line voltage, etc. could have profound impacts on the system. It is apparent that systems that adjust themselves to changes must employ some type of a feedback. A feedback system monitors the output and makes the necessary changes at the input to keep the desired variable within the accepted margin. A power element is used at the output of a regulator, either current or a voltage, when it provides large amounts of currents.

In a practical current source, a stable reference is converted to a current by dropping the voltage across a resistor. A reference, by definition, cannot supply currents in large amounts and for that matter it must be connected to an amplifier. In most systems, this configuration is enough to satisfy the system's requirements. In

[2] Reference (2)

reality, the current of the system can change as a function of a transistor's drain to source voltage. For systems, like magnetic lenses, the stability of the focusing properties is dependent on the stability of the current. Any minor changes in the current changes the focal length in the magnetic lens resulting in a decrease in resolution.

Chapter 2 gives a brief history and background of the electron microscope. In this chapter, the dynamics of electrons and how they are used in electron microscopy are explored and examined in detail. The wave nature of electrons and the concept of diffraction and its relevance in optical resolution are explained.

Aberrations and diffraction in lenses are explained in Chapter 3. All lenses have aberrations that could limit their resolution. Some of these aberrations arise due to the defect in the structure of the lenses. Spherical and Chromatic aberration of magnetic lenses and their level of dominance are calculated in this chapter.

In Chapter 4 the resolution limit is calculated. There is a theoretical limit of the resolution that cannot be surpassed. In this chapter it is shown what type of stability is required in the current that runs through the coils for the generation of the magnetic field to achieve the resolution limit.

Chapter 5 discusses two different methods that were used previously in the literature to generate a stable current supply needed for the electron microscope. In this chapter, it is shown how a much more stable current supply can be materialized. Two different circuit topologies are explored and explained in detail. The advantages and disadvantages of each method is discussed and analyzed as to whether or not those ideas can be incorporated in the current design.

The system consideration of the design of the current supply for this research is explored in chapter 6. The methodology of the current supply design is discussed in detail and all the considerations that are necessary for a successful implementation of

the design is discussed. A current supply can have different architectures to create the extreme stability that is demanded of it. In this chapter, a detail discussion of the overall design and its advantages and disadvantages are considered. The overall blocks of the design are drawn out and discussed to show how and why they are used.

Chapter 7 is a complete and detailed design of the intended current supply. The overall design contains numerous circuit components. The transistor level design of each block is shown and its design methodology is discussed in detail. After the design of all the sub blocks, the integrity of the complete system and its relation to each sub block is shown. Also In this chapter, the waveforms of each circuitry and then the complete system are shown and discussed in detail.

Chapter 8 discusses the results of this research, the challenges and difficulties of this design. This chapter starts with a discussion of the problems that must be taken into account in constructing this high precision current supply system. The right technology, the precise circuitries, and the specific physical structures of the overall system are of paramount importance. The summary chapter will conclude with the potential of future research and the recommendations for improving the future undertakings of building an ultra high precision current supply.

Chapter 2

A Brief History

The Electron Microscope

The typical Light-Microscope is limited in its resolving power by the wavelength of light itself. When one wants to examine certain small objects at the scale of atoms or smaller another technique must be used. This technique is based on the theory that was set by the French Physicist Louis de Broglie (3). He postulated that matter has its own characteristic wave, and the relationship can be written as

$$\lambda = \frac{h}{mv} = \frac{h}{p} \tag{2.1}$$

where h = Plank's constant = 6.626 × 10 ^ (-34) J.s,
m = particle mass (mass of an electron = 9.109 × 10 ^ (-31) Kg), and
v = velocity (m/s)
An electron of charge e (1.6e-19 C) and mass m (9.11e-31 kg) passing through a potential difference V will have the kinetic energy (non-relativistically):

$$\frac{1}{2}mv^2 = eV \tag{2.2}$$

where e = 1.6 × 10^-19 C

V = Potential difference in volts

By substituting equation (2.1) to equation (2.2) we have

$$\lambda = \frac{h}{\sqrt{2meV}} \qquad (2.3)$$ [3]

Equation (2.3) illustrates that when electrons are energized to very high kinetic energies, their corresponding wavelengths can become smaller than the size of an atom, and it would be possible to see detailed structure of matter at atomic dimensions.

Example:

The de Broglie wavelength of the electron accelerated through 50V is:

$$\lambda = \frac{h}{\sqrt{2meV}} = \frac{6.63 \times 10^{-34} J.s}{\sqrt{2(9.11\times10^{-31}Kg)(1.6\times10^{-19}C)(50V)}} = 1.74\times10^{-10}m = 0.174nm$$

This wavelength is of the order of atomic dimensions and the spacing between atoms in a solid. Such low-energy electrons are normally used in electron diffraction experiments (3).

Magnetic lenses

In geometric optics, when light rays pass through a lens, a medium of different index of refraction than air, they will become refracted. The light rays will bend by refraction upon entering the lens, and again upon exit from the lens. By following the light rays, it can be seen that an image of the object is formed either on the opposite side of the lens, a real image or on the same side of the lens, a virtual image. Thus, it is possible to form an image of the object by changing the direction of light rays through a lens, in a way that the light rays will converge at the desired point to form the image of the object.

An important equation that is used for the case of thin lenses is:

[3] Reference: (3)

$$\frac{1}{f} = \frac{1}{i} + \frac{1}{O} \qquad (2.4)^4$$

where o is the distance of the object to the lens, and i is the distance of the image from the lens. f is called the focal length and is a property of the lens itself.

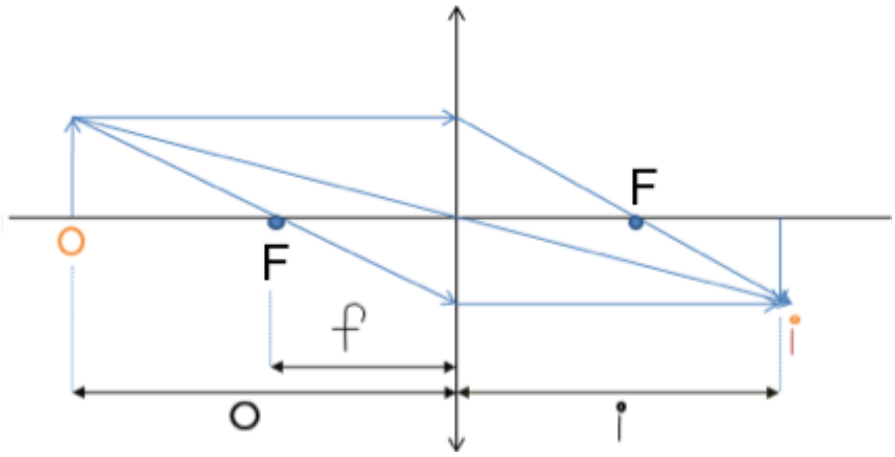


Figure 2.1: Image formation in a convex lens. The object is outside of the focal point (F).

The magnification of the lens can be found by the equation

$$M = \frac{O}{i} \qquad (2.5)^5$$

Unlike light optics, where lenses are used to refract and bend light rays for image formation, in electron optics magnetic lenses are used to do the same thing. The magnetic force is used to change the direction of the electron in the same way that a lens changes the direction of light rays. In a magnetic field, an electron will experience the Lorentz Force defined by:

[4] , [5] Reference: (4)

$$F = qv \times B \qquad (2.6)^6$$

where F is Lorenz force,

v is the electron velocity,

B is the magnetic field, and

q is the electron charge.

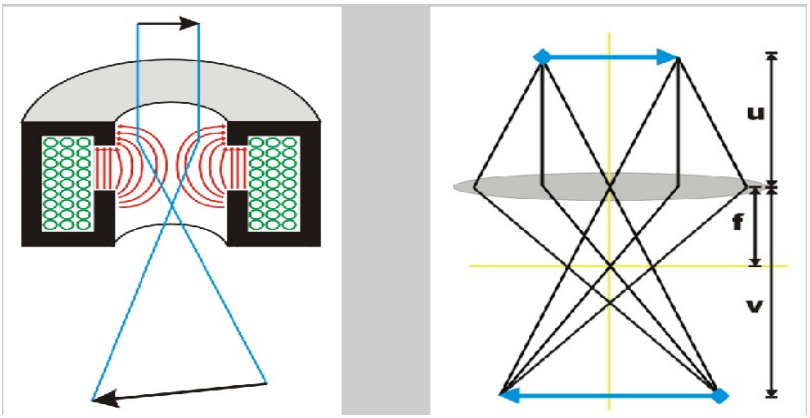


Figure 2.2: Formation of image in an electron microscope and in a lens (11).

In magnetic lenses, a coil is used to create the magnetic field. The magnetic field produced by an air core solenoid can be shown to be (at the center):

$$B = \mu_o nI \qquad (2.7)^7$$

where μ_o = permeability of free space,

n = number of turns per unit length of wire, and

I = current.

Also, the intensity of the magnetic field can be improved by encasing the coil in a sheath of soft iron (different μ). This way a much more powerful

[6] Reference: (1)

[7] Reference: (2)

magnetic field is produced for the same amount of current flowing through the coil. As shown in Figure 2.2, the coil can be enclosed completely except at a narrow gap in the inside of the coil. This will create an even greater magnetic field to achieve shorter focal length lenses (5).

In the electromagnetic lens, the focal length depends on two factors: the kinetic energy of the electrons, which determines the velocity *v*, and the amount of current through the coil, which determines the magnetic field, B. Therefore, the operator controls the focal lengths of the lenses by adjusting the currents supplied to them (6). For a thin magnetic lens, the focal length is related to current through the relation (7):

$$f = \frac{KV_r}{(NI)^2} \tag{2.8}$$

where f = focal length,
K = a constant,
V_r = relativistic accelerating voltage[8],
I = current, and
N = number of turns in the excitation coil.

Equation (2.8) shows that the focal length varies inversely with I^2. Therefore, a fixed and stable focal length requires a stable current flowing through the coil. In order to see the importance of a stable current we can differentiate equation (2.8):

$$\frac{df}{dI} = \frac{d}{dI}\left(\frac{KV_r}{(NI)^2}\right) = \frac{-2KV_r}{N^2I^3} = \frac{-2f}{I} \tag{2.9}$$

by rearranging equation 2.9 we get

[8] $V_r = \frac{1}{e} m_0 c^2 \left(\frac{1}{\sqrt{1-\left(\frac{v}{c}\right)^2}} - 1\right)$ where m_0 is the rest mass of the object, and *c* is speed of light.

$$\frac{\Delta f}{f} = \frac{-2\Delta I}{I} \tag{2.10}$$

Equation (2.10) shows that stability of the focal length is directly proportional to the stability of the current that is setting up the magnetic field in the coils. Thus, it is paramount to design a highly stable current source for a high quality magnetic lens.

Chapter 3

Aberrations

What are the optical aberrations?

When we talk about resolution and depth of field of an optical system, it is always assumed that all the components of the microscope are perfect and will focus the light from any point on the object to a similar unique point on the image. But this is not the case because of the lens aberrations and diffraction (the wave property of light) (8).

There are three major kinds of aberration:

- Chromatic aberration (Geometric Optics)
- Spherical aberration (Geometric Optics)
- Diffraction (Wave Optics)

Note: there are other optical aberrations, but they will not be considered in this thesis.

Chromatic aberration

Ideally, when light rays passes through a (convex) lens, they all land at one point called the focal point. α is the microscope semi-aperture angle (the angle defined at the image) as shown in figure 3.1.

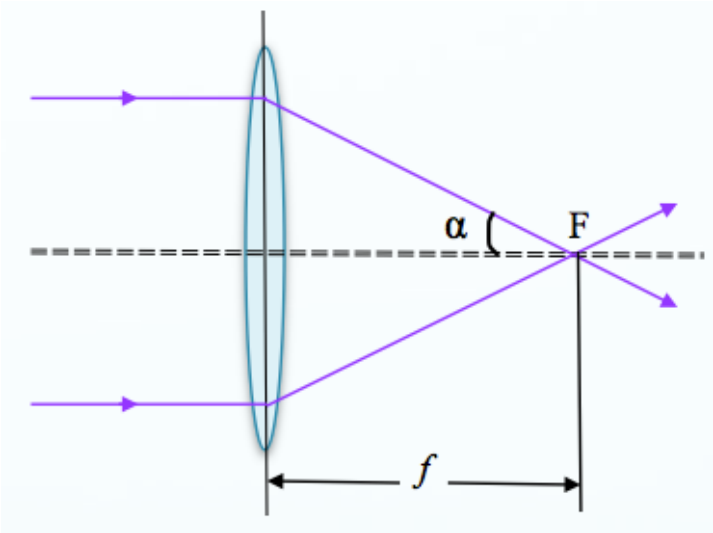


Figure 3.1: Light rays passing through a convex lens.

Chromatic aberration is due to the fact that different wavelengths get focused to different points. This is shown in figure 3.2. In the light microscope improvements are done in two different ways. Either by combining lenses of different shapes and refractive indices or by eliminating the variation in wavelength from the light source by using filters.

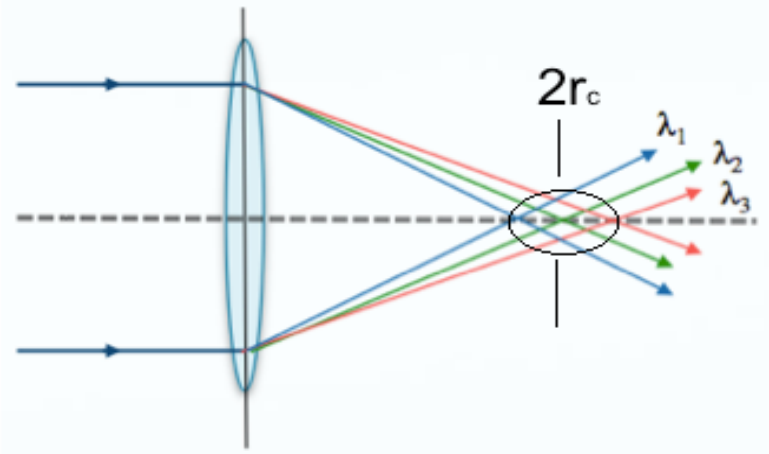


Figure 3.2: Chromatic aberration

Since the electron wavelength depends upon its energy, then electrons leaving a point with different energies will be brought to a focus at different points and the greater the energy the smaller the effect of the magnetic field and the longer the resulting focal length. It can be shown that (8):

$$r_C = C_C \alpha \frac{\Delta V}{V} \tag{3.1}$$

where r_c is the spot size due to the chromatic aberration of the lens,

α is the microscope semi-aperture angle,

C_C is the coefficient of chromatic aberration; values of C_C are, typically, of the order of the focal length (8), and the $\frac{\Delta V}{V}$ term is the fractional spread in electron energy. It arises from a variety of sources. High voltage instability is one of them.

Spherical aberration

Spherical aberration results from the fact that the focal lengths of rays far from the optic axis may be different from the focal length of rays of the same wavelength passing near the center. This is shown in the figures 3.3 and 3.4:

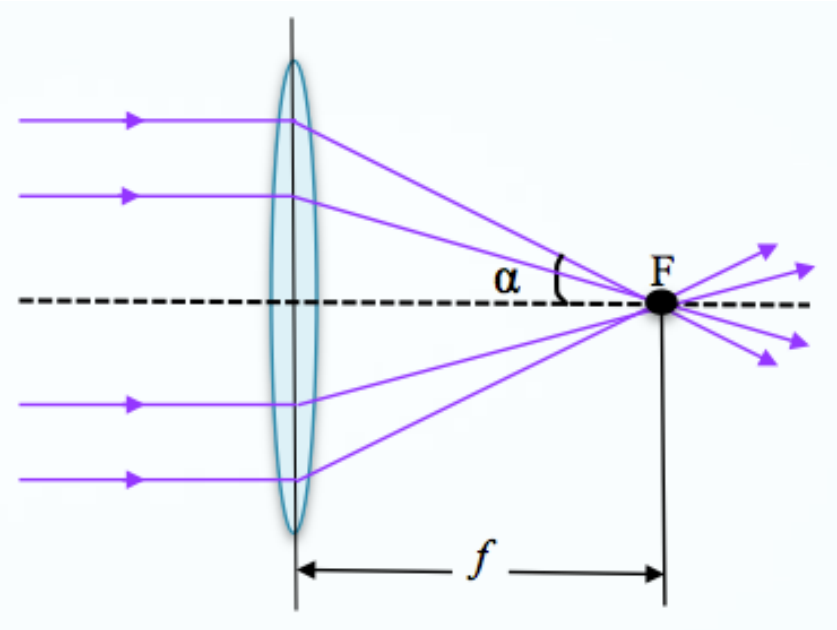


Figure 3.3: Ideal lens

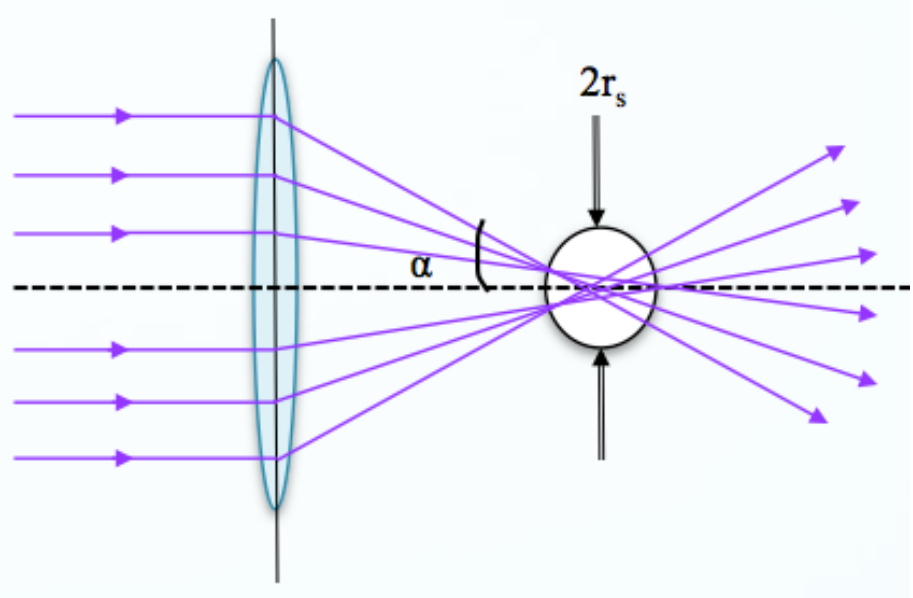


Figure 3.4: Real lens with spherical aberration

The spot size due to the spherical aberration is related to α through (8):

$$r_S = C_S \alpha^3 \tag{3.2}$$

where C_S is defined as of the coefficient of spherical aberration.

For electron microscopes utilizing cylindrical magnetic lenses, the spherical aberration coefficient is approximately the same order as the focal length of the lens (8).

Diffraction

Diffraction is the spreading of a wave as it goes through a narrow gap or passes round a small obstacle. The effect of diffraction increases when the width of the gap is decreased. In a microscope, light of a certain wavelength is used which, by a series of lenses, provides a magnified picture of an object. There exists a fundamental limit of the resolving power of a microscope, however, due to diffraction effects (shown in figure 3.5). Significant diffraction occurs when radiation of a certain wavelength is shone through an opening whose width is comparable to the wavelength of the light (8).

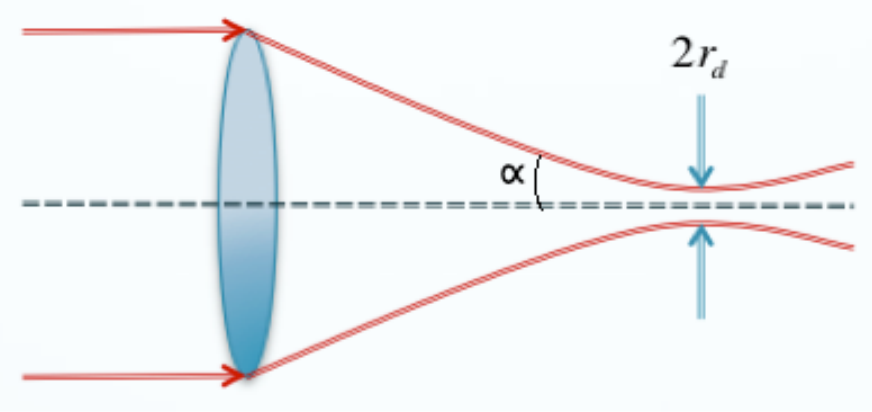


Figure 3.5: Diffraction

$$r_d = \frac{0.61\lambda}{\alpha} \tag{3.3}$$

Where λ is the wavelength of the electron and α is the semi-angle (assuming $\sin\alpha \approx \alpha$ since α is very small for electron). In the figure above, the spreading angle is related to the opening size.

Relationship between resolution and α

Figure 3.6 shows the relationship between resolution and α considering diffraction, spherical aberration, and chromatic aberration. Note that resolution for diffraction gets better as the aperture half angle increases, but for spherical and chromatic aberration, it gets worse as that angle increases. This is based upon assuming all the effects are independent of one another.

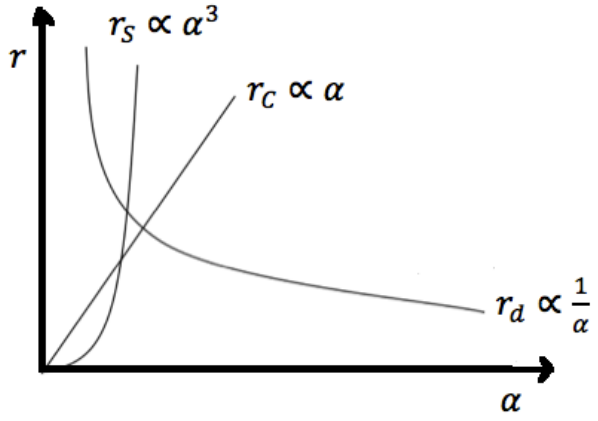


Figure 3.6: Relationship between the resolution and α

Imaging at high resolution with decreasing imaging aperture semi-angle α, the geometric optical aberrations become smaller while the diffraction increases (8). An optimum of the angle α can be found for which the total aberration becomes smallest. The aberrations discussed above all have different dependences on alpha. For high resolution work the compromise is between spherical aberration and diffraction (if one neglects chromatic aberration). According to Scherzer (using wave optics), the best resolving power, which can be expected, in this case is (9 and 10):

$$r_{Sd} = A(C_S\lambda^3)^{1/4} \tag{3.4}$$

where Cs is the spherical aberration, λ is the wavelength of the electron, and A is a constant. It is readily seen that for Cs of the order of 1mm, which is close to the practical lower limit for electromagnetic lenses, and for λ in the range of 1.64 to 3.7pm, corresponding to accelerating voltages of 400 down to 100 KeV, the equation (3.4) gives the resolution limits (9).

Chapter 4

Calculating the resolution limit

Calculations

The resolution limit can be expressed by the following equation:

$$r = f\,[\text{Diff}, C_s, C_c, \Delta V/V, \Delta I/I] \qquad (4.1)$$

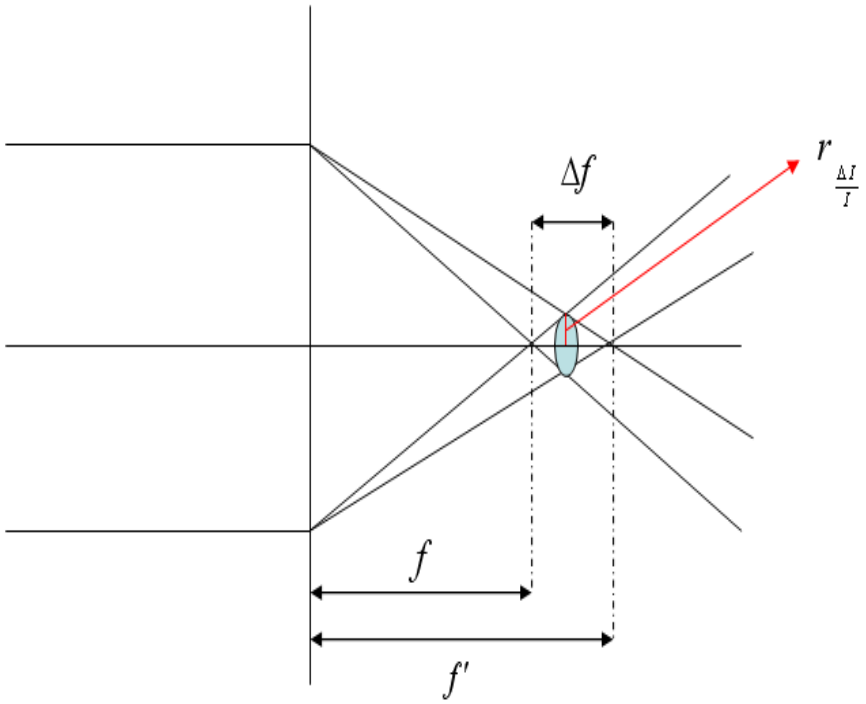
This means that the resolution limit is a function of diffraction, spherical aberration (C_s), chromatic aberration (C_c), potential variations in the electron energy $\frac{\Delta V}{V}$ (this includes variation in the accelerating potential as well as the energy spread of the electron source), and current variations in the magnetic lens used to focus the electrons $\frac{\Delta I}{I}$. Potential variations $\frac{\Delta V}{V}$ and current variations $\frac{\Delta I}{I}$ are due to instrumental limitations. Potential variation is due to two factors; source energy variation and high-tension variation therefore:

$$\frac{\Delta V}{V} = \sqrt{\left(\frac{\Delta V}{V}\right)^2_{Source} + \left(\frac{\Delta V}{V}\right)^2_{HT}} \qquad (4.2)$$

Assuming the above factors are independent of one another then this equation can be rewritten in its exact form:

$$r = \sqrt{r^2_{Diffraction} + r^2_{C_S} + r^2_{C_C} + r^2_{\frac{\Delta I}{I}}} \qquad (4.3)^{9,10}$$

where $r^2_{Diffraction}$, $r^2_{C_S}$ and $r^2_{C_C}$ are fundamental and $r^2_{\frac{\Delta I}{I}}$ depends upon the stability of the magnetic focusing lenses. Note that r_{C_C} the radial smear due to chromatic aberration depends upon the instrumental factors as well as the natural energy spread of the electrons leaving the source, which is a fundamental effect. Note: Cc only depends upon the geometry of the lens.



[9] r_{C_C} in equation 4.3 includes all $\frac{\Delta V}{V}$

[10] $r_{\frac{\Delta I}{I}}$ is the radius of the disk of confusion that is created due to current variation as shown in the figure 4.1.

Figure 4.1: Relationship between $r_{\frac{\Delta I}{I}}$ and Δf

If, 1) the diffraction and spherical aberrations are combined to form r_{sd}^2 in equation 4.3, and

if 2) the effect of chromatic aberration is neglected, equation 4.3 can be written in a simpler form:

$$r = \sqrt{r_{sd}^2 + r_{\frac{\Delta I}{I}}^2} \tag{4.4}$$

or

$$r = r_{sd}\sqrt{1 + \frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}} \tag{4.5}$$

If one neglects Cc and instrumental limitations then one can calculate wave optically the resolution limit considering only spherical aberration and diffraction that has been calculated by Scherzer (10) using $r_{Sd} = A(C_S\lambda^3)^{1/4}$:

Note: A is a constant and by convention it is about 0.43 (9). Cs is usually of the order of 1mm. λ is in the range of 1.64 to 3.7pm for an accelerating voltage between 400 to 100 KeV.

Table 4.1: Relationship between λ (pm), V(KeV), and r_{sd}

λ (pm)	V (KeV)	r_{sd} (m)
1.64	400	1.11×e-10
3.7	100	2.04× e-10

From equation 4.5 we can conclude that resolution, r, can't be better than the value of r_{sd}. We also can conclude that the total resolution, r, will be better if the ratio $\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}$ has a smaller value. For example, if the ratio $\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}$ is equal to 0.1

(assuming that the total resolution would be about 5% larger than r_{sd}) and r_{sd} is equal to 1.11 × e-10m then:

$$r = r_{sd}\sqrt{1+\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}} = 1.11\times10^{-10}\sqrt{1+0.1}$$

$r = 1.164\times10^{-10} m.$

Calculating $\frac{\Delta I}{I}$ with respect to $r_{\frac{\Delta I}{I}}$, f and α:

Using figure 4.1 we can find the relationship between $r_{\frac{\Delta I}{I}}$ and $\frac{\Delta I}{I}$. Since the angle α is very small for electron microscopy, we can assume that $sin\alpha = \alpha$ and $tan\alpha = \alpha$.

Therefore:

$$tan\,\alpha = \frac{r_{\frac{\Delta I}{I}}}{\Delta f/_2} = \frac{2r_{\frac{\Delta I}{I}}}{\Delta f}$$

from this relationship we can conclude that:

$$r_{\frac{\Delta I}{I}} = \frac{(\Delta f)(\tan\alpha)}{2} = \frac{\Delta f\alpha}{2} \qquad (4.6)$$

Combining Equation 2.10 ($\frac{\Delta f}{f} = \frac{-2\Delta I}{I}$) and Equation 4.6 will give us a relationship between $r_{\frac{\Delta I}{I}}$ and $\frac{\Delta I}{I}$:

$$\frac{\Delta I}{I} = \frac{\Delta f}{-2f} = \frac{2r_{\frac{\Delta I}{I}}}{-2\alpha f} = \frac{r_{\frac{\Delta I}{I}}}{\alpha f} \tag{4.7}$$

The relationship between $r_{\frac{\Delta I}{I}}$ and $\frac{\Delta I}{I}$ is shown in figure 4.2.

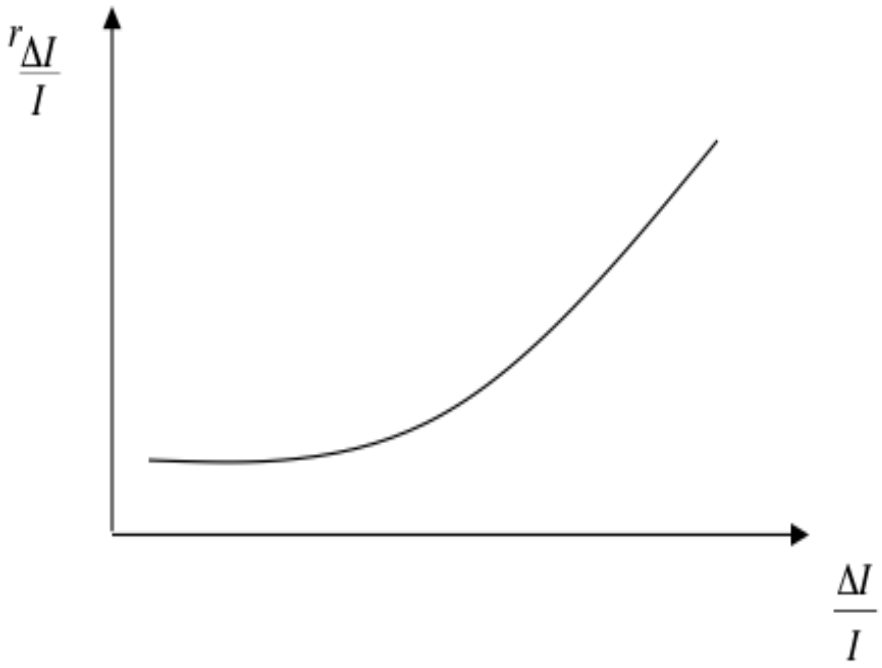


Figure 4.2: Relationship between $r_{\frac{\Delta I}{I}}$ and $\frac{\Delta I}{I}$

Total resolution can therefore be calculated with respect to $\frac{\Delta I}{I}$:

From Equation 4.5 we know that: $r = r_{sd}\sqrt{1+\frac{r^2_{\frac{\Delta I}{I}}}{r^2_{sd}}}$ therefore:

$$r = r_{sd}\sqrt{1+\frac{[(f)(\frac{\Delta I}{I})(-\alpha)]^2}{r^2_{sd}}} \tag{4.8}$$

Example 1:

Let us calculate r_{sd} and $\frac{\Delta I}{I}$ for a lens with focal length of 1.5mm and C_s of approximately 1mm (note: the square term is chosen to be 0.1):

Assuming A is approximately equal to 0.43 (9) and $\lambda = 3.7\times10^{-12}$m (for V = 100KeV):

$$r_{sd}=A(C_s\lambda^3)^{1/4}=0.43(1\times10^{-3}\times(3.7\times10^{-12})^3)^{1/4}=2.04\times10^{-10}\text{m}$$

$$r = r_{sd}\sqrt{1+\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}} = 2.04\times10^{-10}\sqrt{1+0.1} = 2.14\times10^{-10}\text{ m}$$

Now let us calculate the optimum α (7) with the above characteristics:

$$\alpha_{opt}=1.4\left(\frac{\lambda}{C_s}\right)^{1/4}=1.4\left(\frac{3.7\times10^{-12}}{1\times10^{-3}}\right)^{1/4} = 10.91\times10^{-2}rad = 10.91\ mrad$$

Assuming $\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2} = 0.1$ then $r_{\frac{\Delta I}{I}} = 0.32\times1.11\times10^{-10} = 3.51\times10^{-11}$m

Therefore by using equation 4.7 we can find $\frac{\Delta I}{I}$:

$$\frac{\Delta I}{I}=-\frac{r_{\frac{\Delta I}{I}}}{\alpha f}=-\frac{3.51\times10^{-11}}{7.87\times10^{-3}\times1.5\times10^{-3}}=-2.97\times10^{-6}$$

This number tells us how small $\frac{\Delta I}{I}$ needs to be in order to reach a total resolution of 2.14 Angstrom.

Example 2:

Let us calculate the $\frac{\Delta I}{I}$ for a corrected lens with $C_s = 0.1\,\mu$m:

Assuming A is approximately equal to 0.43 (9) and $\lambda = 3.7\times10^{-12}$m (for V = 100KeV):

$$r_{sd}=A(C_s\lambda^3)^{1/4}=0.43(0.1\times10^{-6}\times(3.7\times10^{-12})^3)^{1/4}=2.04\times10^{-11}\text{ m}$$

$$\alpha_{opt}=1.4\,(\frac{\lambda}{C_s})^{1/4}=1.4\,(\frac{3.7\times10^{-12}}{0.1\times10^{-6}})^{1/4}=0.1092\text{rad}=109.2\text{ mrad}$$

Since we assumed $\frac{r_{\frac{\Delta I}{I}}^2}{r_{sd}^2}=0.1$ then $r_{\frac{\Delta I}{I}}=0.316\times2.04\times10^{-11}=6.45\times10^{-12}$m

then,

$$\frac{\Delta I}{I}=-\frac{r_{\frac{\Delta I}{I}}}{\alpha f}=-\frac{6.45\times10^{-12}}{109.2\times10^{-3}\times1.5\times10^{-3}}=-3.94\times10^{-8}$$

In other words, to achieve sub angstrom resolution, the current stability needs to be in order of 10^{-8}.

Conclusion

It is apparent from all the above that magnetic lenses with ultra levels of stability can only be obtained with an extremely stable current supply. Such current supplies can be extremely difficult to design and manufacture. In the next chapter, an overview of the attempts to reach such high precision current supplies is shown.

Chapter 5

Previous Designs

This chapter discusses two different methods that were used previously in the literature to generate a stable current supply needed for electron microscopy. In this chapter, it is shown how an extremely stable current supply can be materialized. Two different circuit topologies that have been used in the literature are explored and explained in detail. The advantages and disadvantages of each method is discussed and analyzed as to whether or not those ideas can be incorporated in the current design.

Method 1 by Rust, H. P. (11):

In this approach, which is shown in figure 5.1, an amplifier monitors the voltage across a resistor and the control loop adjusts the power stage so that the product of I_{L1} and R_1 was equal to V_{ref}. Unfortunately, this approach has the problem that the resistor R_1 varies as a function of temperature, and this limits the stability of this method.

$$I_L = \frac{V_{ref}}{R_1} \tag{5.1}$$

$$\Delta I_L = -I_L T_{KRE} \Delta\theta \tag{5.2}$$

where T_{KRE} is R_1's temperature coefficient, and

$\Delta\theta$ is the change in temperature.

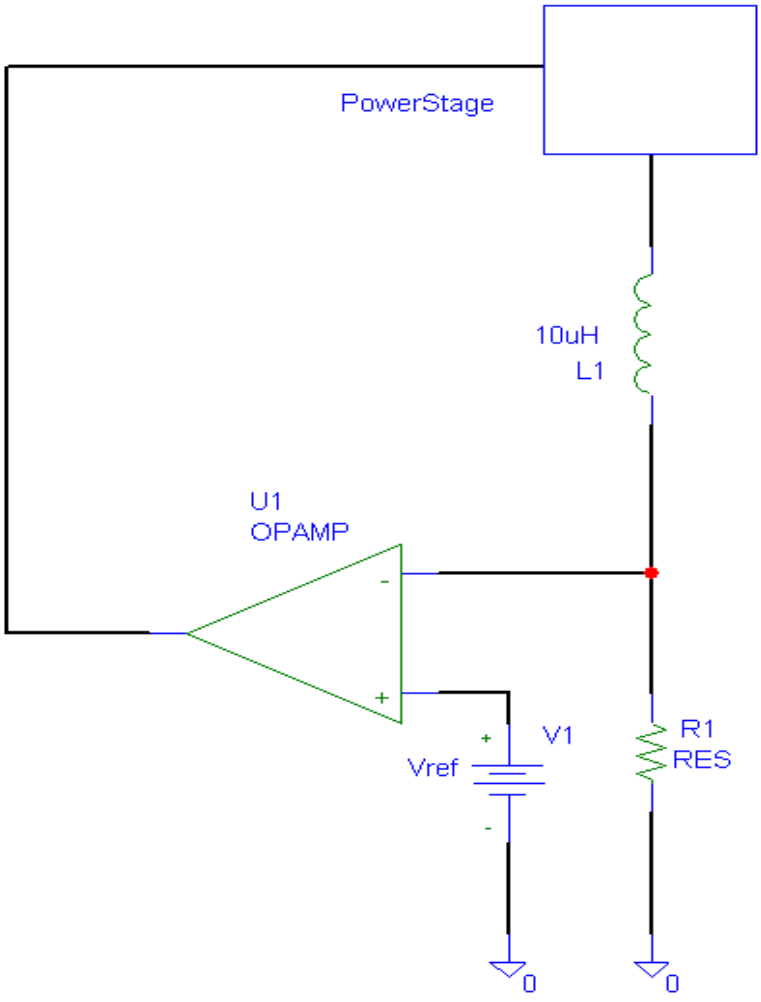


Figure 5.1: The Rust's method to create a constant current (11)

In order to get around this temperature coefficient problem, a more elaborate method was devised which is shown in figure 5.2.

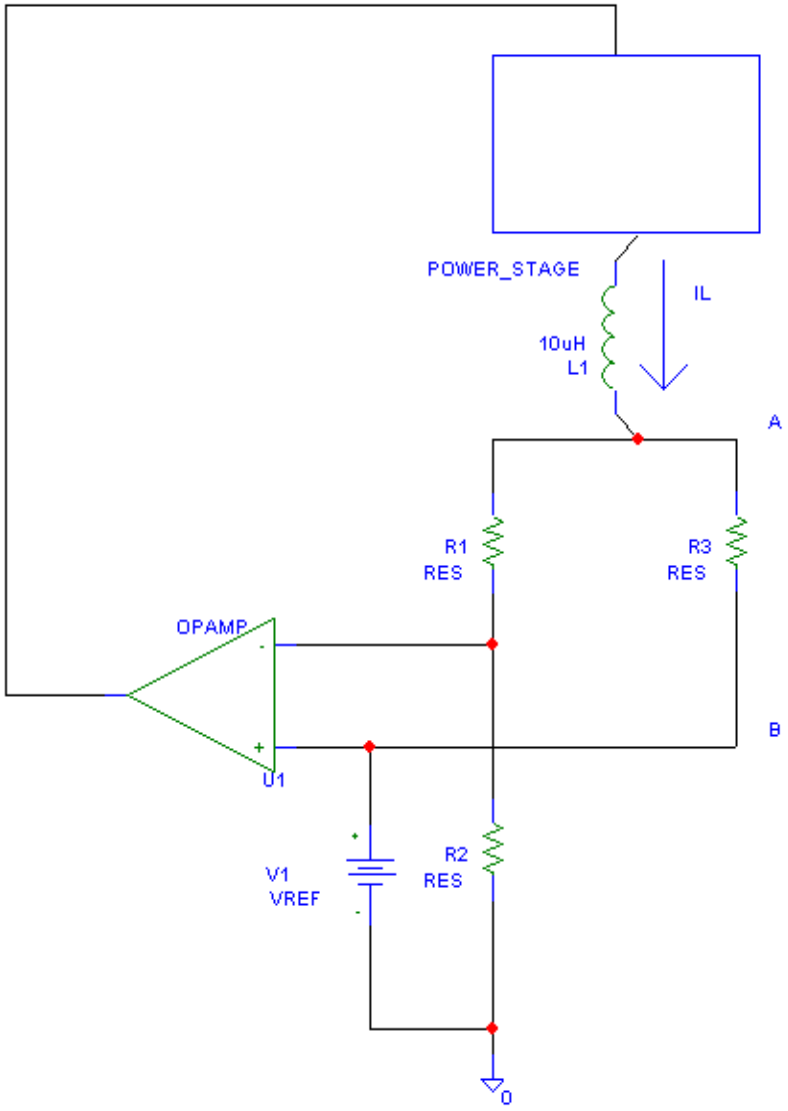


Figure 5.2: Rust's improved version of circuitry shown in figure 5.1 (11)

The equations for the system shown in figure 5.2 are as follow:

$$V_A = V_{REF} + V_{REF}\frac{R_1}{R_2} \quad (5.3)$$

$$I_L = \frac{V_{REF}}{R_2} + \frac{V_{REF}+V_{REF}\frac{R_1}{R_2}-V_{REF}}{R_3} = \frac{V_{REF}}{R_2}(1+\frac{R_1}{R_3}) \quad (5.4)$$

$$\Delta I_L = \frac{V_{REF}}{R_2}(\frac{R_1}{R_3}\frac{\Delta R_1}{R_1} - \frac{R_1}{R_3}\frac{\Delta R_3}{R_3}) \quad (5.5)$$

$$\frac{\Delta R_1}{R_1} = Tk_{R_1}\Delta\theta_1 \quad (5.6)$$

$$\frac{\Delta R_2}{R_2} = Tk_{R_2}\Delta\theta_2 \quad (5.7)$$

$$\Delta I_L = \frac{V_{REF}}{R_2}\frac{R_1}{R_3} = \left(Tk_{R_1}\Delta\theta_1 - Tk_{R_3}\Delta\theta_3\right) = 0 \quad (5.8)$$

By going through this set of equations, we can see that the variations in current across the load in equation 5.8 should be zero if the quantities in the brackets are balanced. So for the first order effect, the system should create a constant current as a function of temperature.

Goals reached in Method 1:

In this method the temperature-dependent drift of the current was reduced by a factor of about 5. The drift caused by a change in current from 550 to 650mA was, after one minute, less than $1\times10^{-6}min^{-1}$, and after three minutes below the relative statistical fluctuations of $\frac{\Delta I}{I} = 0.3\times10^{-6}$. These fluctuations were mainly caused by noise from the supply reference voltages and the measuring device (11).

In order to test our simulation tools, we have evaluated the circuit used in method 1 to compare with their experimental results. Figure 5.3 shows the schematic the way the authors had implemented their system. The system

cannot be simulated as shown in this figure since the authors make the assumption that resistors R_1 and R_3 are the only components that change when current through them changes. The relation in equation 5.8, as defined by the authors, assumes the temperature coefficients of R_1 and R_3 cancel each other and the variation of current as the result of thermal changes can be theoretically zero. Because of those problems, in order to check our simulations with their results, a circuit similar to theirs was used but which had components that varied with temperature (see figures 5.3 and 5.4).

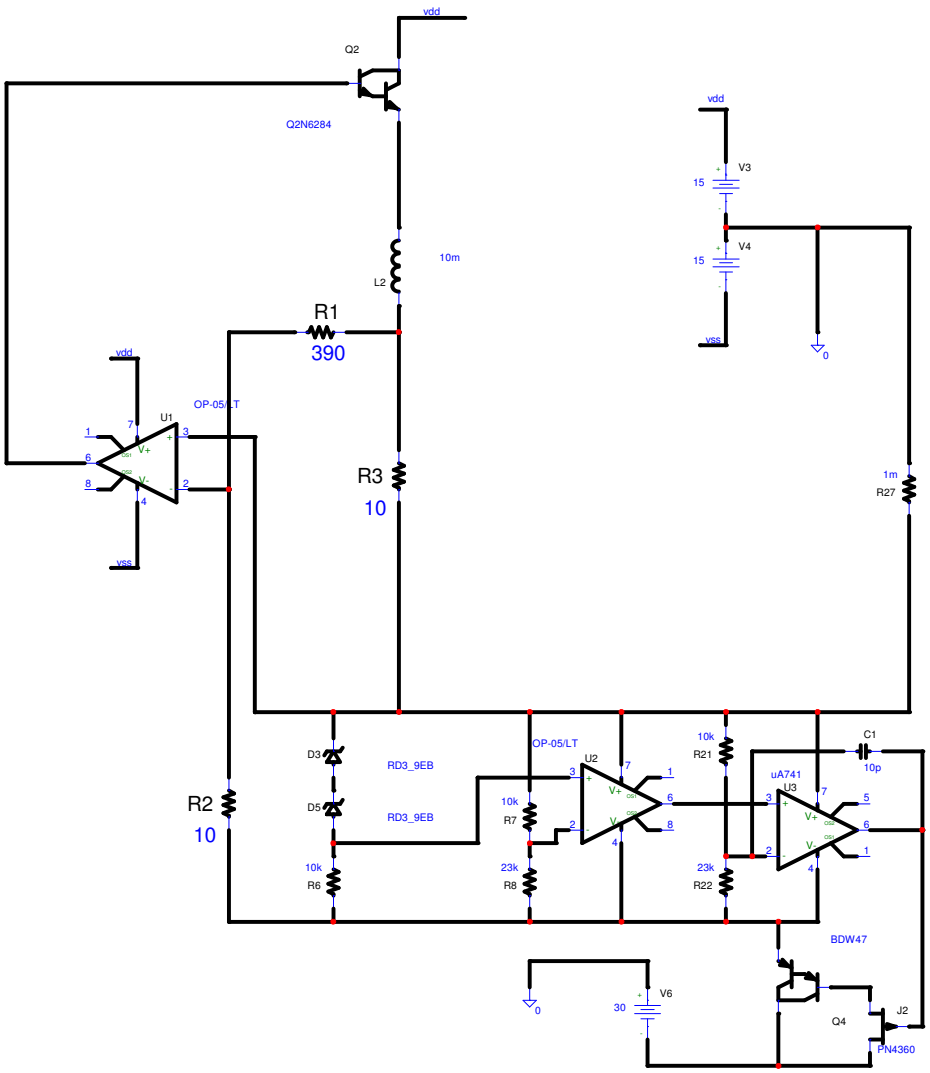


Figure 5.3: A similar circuit to Rust's design

The system was simulated with respect to temperature by using the schematic in figure 5.4. In this particular simulation, all components are ideal except the two resistors R_1 and R_3, which have temperature coefficients. The temperature coefficients, regardless of their absolute values, cancel each other out and a small change results. But, if the thermal coefficient of resistor R_2 is considered then the relation in equation 5.8 is not accurate.

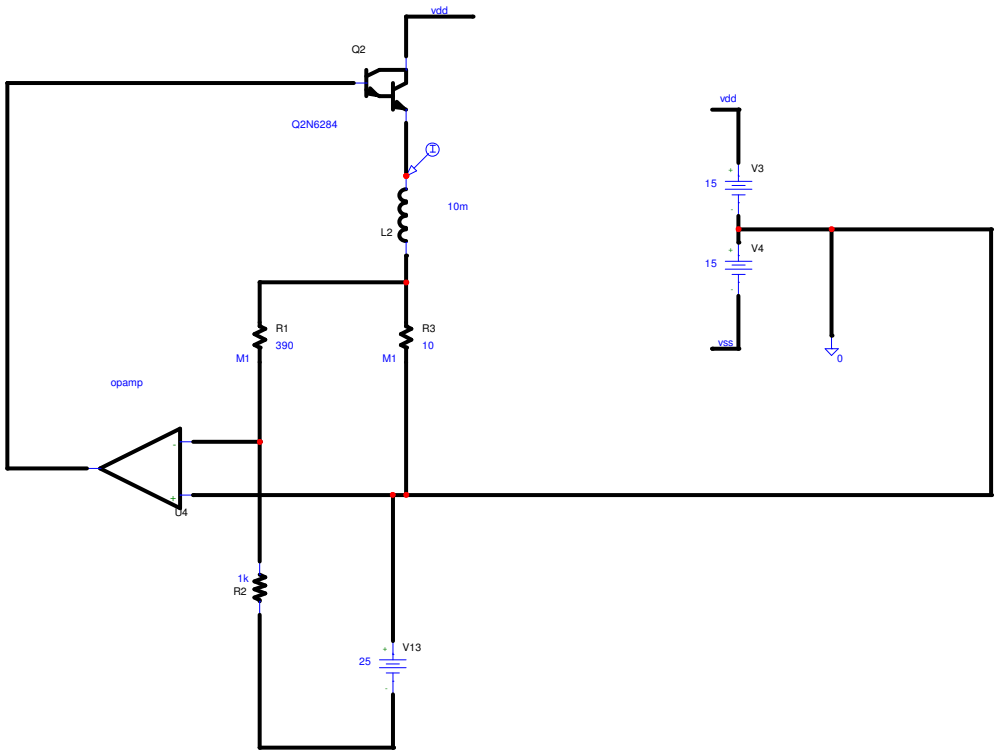


Figure 5.4: Circuit used to run simulations

The graph shown in figure 5.5 shows the result of how this circuit behaves. The lower graph shows the behavior of the system when R2 does not have any temperature coefficients. The stability of the system will be 0.666 ppm/℃, which is close to the 0.3 ppm/℃, as the authors claim. The upper graph shows the system where R2 is in not an ideal resistor, and the system shows a stability of only 4100 ppm/℃. This result demonstrates that this system must be kept in an environment where the temperature is tightly controlled otherwise any temperature variations, as demonstrated by the upper graph of figure 5.5 will jeopardize the stability of the system.

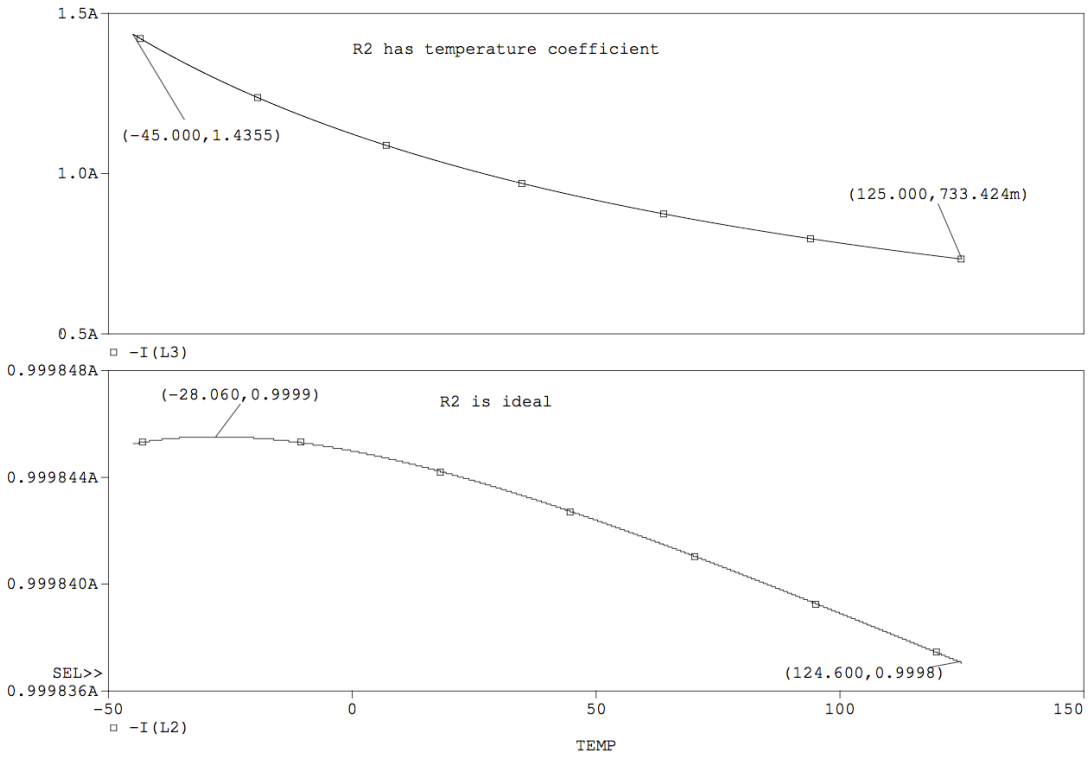


Figure 5.5: Simulation results for circuitry shown in figure 5.4

Method 2 by Wisnivesky, D. & Lira, A. C. (12):

In this method, shown in figure 5.3, a sensing transformer senses the voltage across the sensing resistor (12). An amplifier then amplifies the sensing voltage, and the sensing comparator turns the power stage on and off accordingly. This method is known as a hysteretic mode. $\frac{\Delta I}{I}$ is equal to 5ppm. The converter uses the window hysteresis of the comparator to control the current through the load.

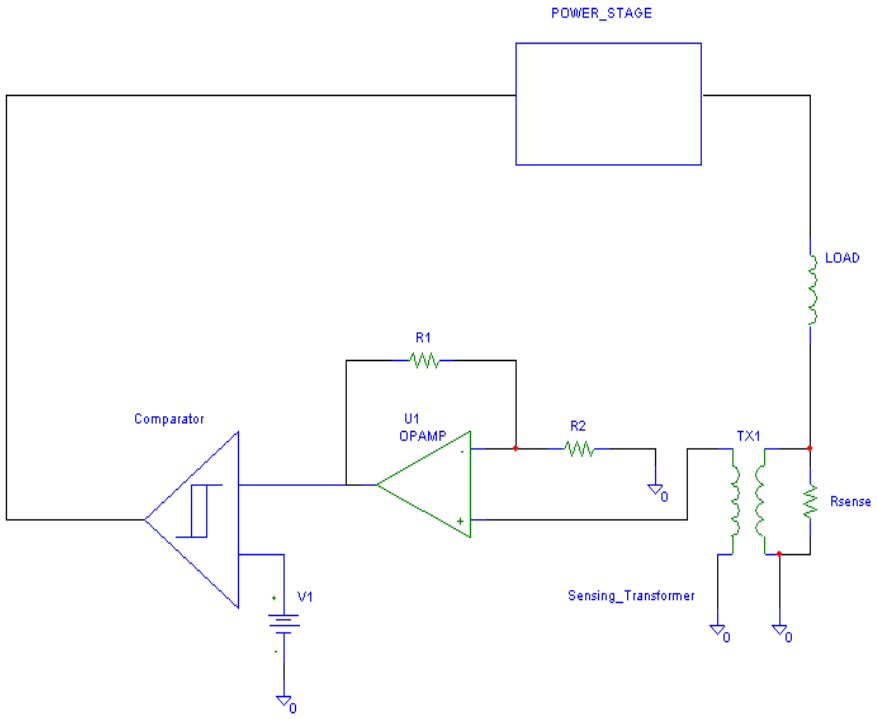


Figure 5.6: The schematic of an accurate and stable constant current supply by Wisnivesky

The current through the load can be calculated as follows:

$$V_{Rsense}=I_{Load}R_{Sense} \tag{5.9}$$

$$V(out)_{OPAMP}=V_{Rsense}\frac{n_1}{n_2}(1+\frac{R_1}{R_2}) \tag{5.10}$$

$$V_{HYSTERESIS}=V_{Rsense}\frac{n_1}{n_2}(1+\frac{R_1}{R_2}) \tag{5.11}$$

$$I_{Load}=\frac{V_1}{V_{Rsense}\frac{n_1}{n_2}(1+\frac{R_1}{R_2})} \tag{5.12}$$

$$I_{Load(Ripple)}=\frac{V_{HYSTERESIS}}{V_{Rsense}\frac{n_1}{n_2}(1+\frac{R_1}{R_2})} \tag{5.13}$$

Goals reached in Method 2:

Maximum output voltage: 45V,

current range: 8-200A,

current ripple: ±22mA at 200A,

long term current stability ±50ppm,

average current tracking error: 0,

ramping speed <25 A/s, and

magnetic field ripple <10ppm.

This system can be considered a good system for two reasons:

1. The feedback loops of hysteretic systems are digital feedbacks, and that means that there are not stability issues, like with analog feedback, that can create sustained oscillations. This is a good technique for power supplies of Electron Microscopes that can have large magnets that can cause stability issues. The large magnets, which are inductive, are the

loads for the power supply. The inductive loads are difficult to compensate and stabilize due to the fact they introduce a zero in the small signal loop gain of the system. In order to counter the effect of this zero, a pole must be placed within the useful bandwidth of the system to counter the effect of this zero. But, the introduction of this artificial pole requires much-complicated circuitry that might not be effective throughout the load, temperature, and other variation that might arise. The hysteretic systems are open loop systems that do not require small signal stability, and for that matter the inductive loads are not problems.

2. The hysteretic systems can have efficiencies well above 90%; so in systems with output power generations of 20 Watts or lower the heat generation remains well below the temperatures, usually 150C, that the junctions in the solid-state devices are damaged. This means that there is no need for heat sinks and other bulky materials that help in cooling the system. Also, the way that current is amplified in this system, as shown in equation 5.13, helps keep the current ripple to very low levels, which is mandatory for high stability in magnetic lenses.

In order to evaluate method 2, a similar system was put together with known components. The system was simulated by the schematic shown in figure 5.7. This system has a hysteretic comparator and a ripple amplifier that lowers the hysteresis of the comparator by the amount of gain of the amplifier. This system is not compensated and it can respond quickly to any changes that are imposed on the system. In this simulation, the built-in hysteresis of the comparator is 10mV. The gain of the ripple amplifier is 50, and the load current is 200A. On a 200A load current, the ripple is only $\pm$25mA a result close to what the authors have achieved experimentally.

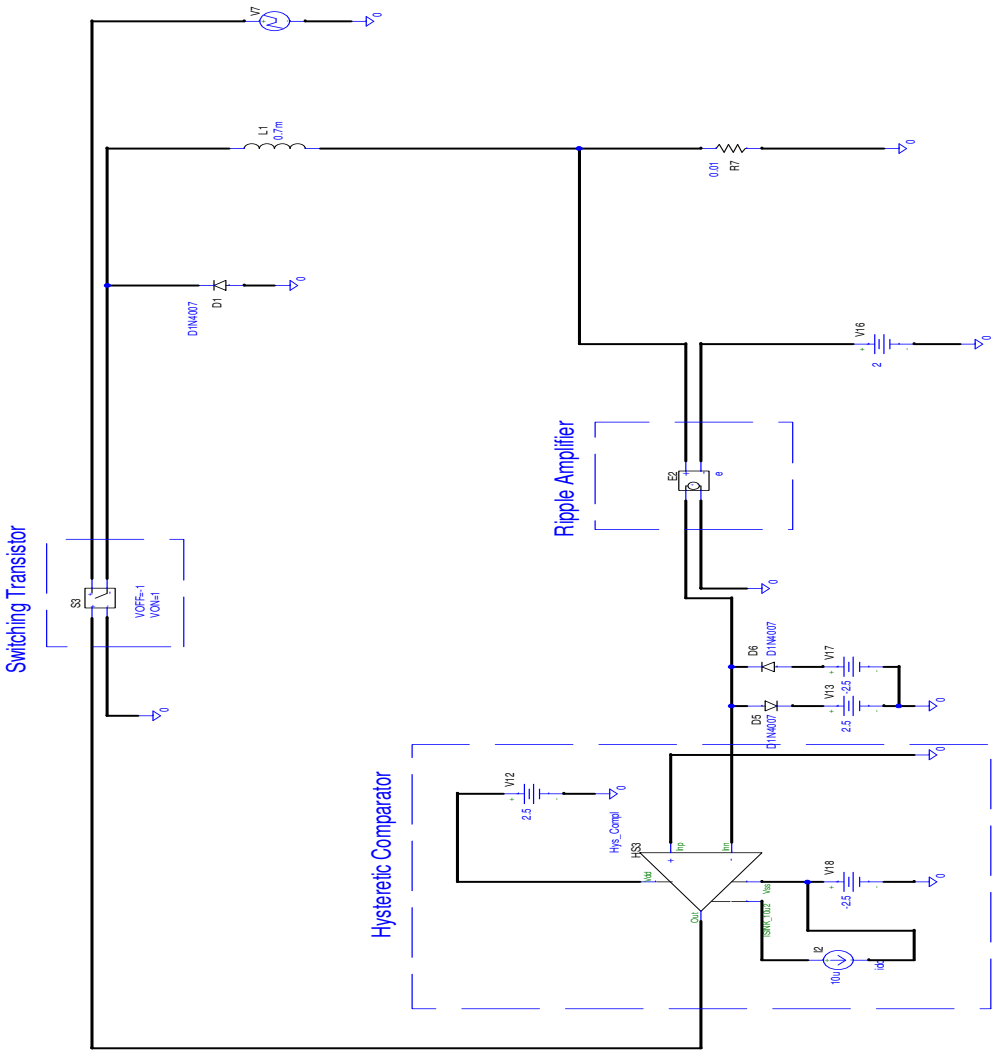


Figure 5.7: A similar circuit to current supply designed by Wisnivesky

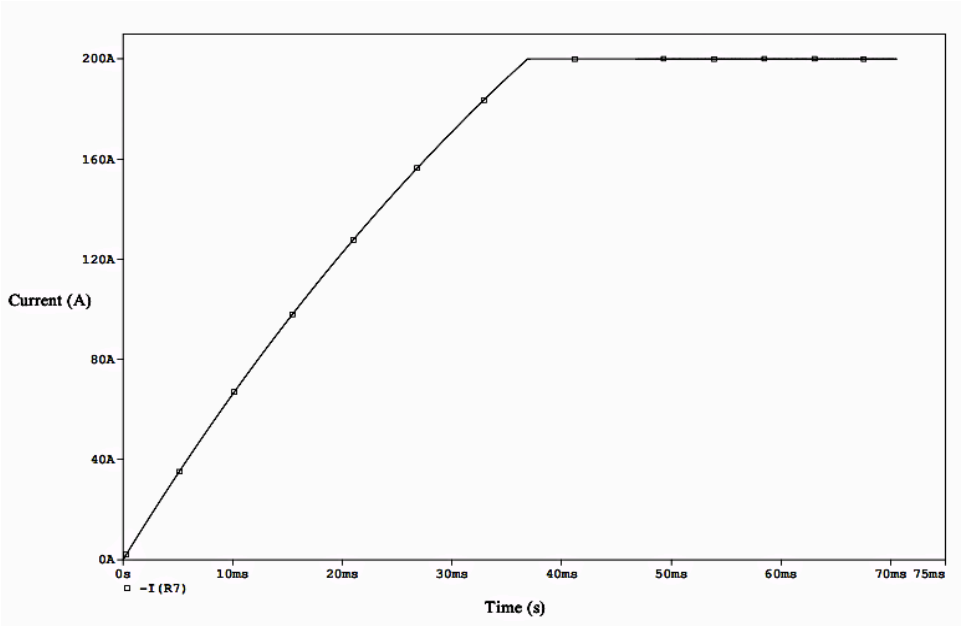


Figure 5.8: Simulation result for circuitry shown in figure 5.7

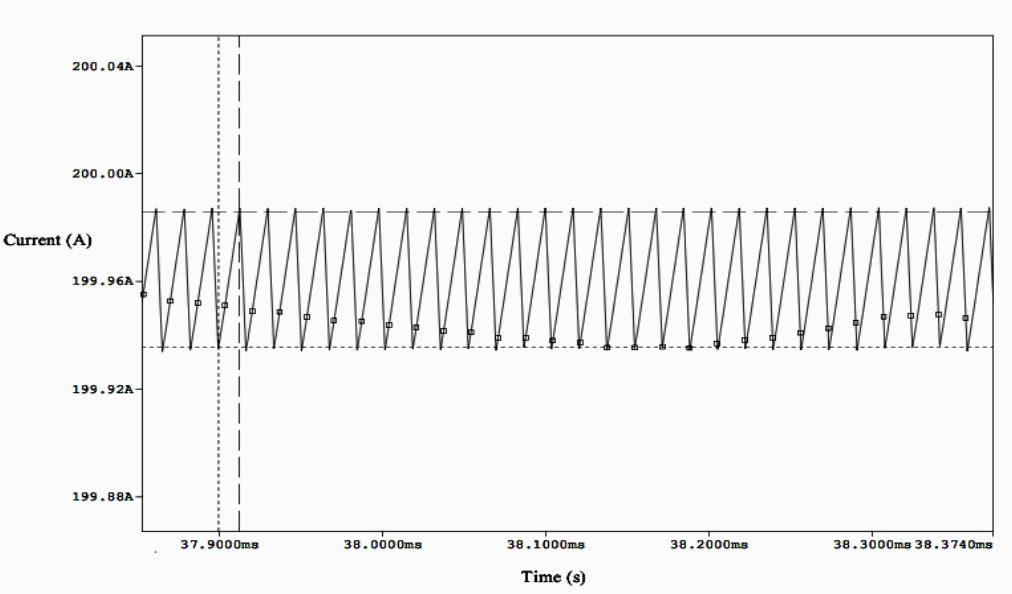


Figure 5.9: Ripple current of the circuitry shown in figure 5.7

Conclusion

The two designs that were explained above made good attempts to produce a stable current supply, but they fall short of the 0.01-ppm requirement that is needed for atomic resolution electron microscopy. The first approach assumes that all the instability in the supply current is due to the thermal variations in the resistors. The new design uses a new methodology that eliminates, to the first order, the thermal effects of the resistors on this current generation. The variations of current due to the other factors such as changes in reference voltage and offset variations of the amplifier that can arise from the changes of temperature and supply voltage are completely ignored. The authors are not clear as to how they can ignore the effects of R_2 when they quantify the relation in equation 5.8. Simulation results clearly show R_2 can introduce large errors if its thermal variations are not taken to account. The second approach is a more elaborate design that uses a hysteretic system, a more power efficient but a noisier method than the first design. The transformer turn ratio and the close loop gain of the OPAMP will lower the ripple at the output, but it will not eliminate nor attenuate it to the levels that is needed to attain the 0.01 ppm stability. The second method is suitable for systems that supply large currents and don't require such current stability as we need.

Chapter 6

System Considerations

In this chapter an overview of a stable current supply and its components are described. At the end of this chapter we will conclude with a discussion of why the particular design strategy was chosen. An ideal current supply is a circuit element that has its current independent of the voltage source, temperature, or any other variations that can disturb the system. Figure 6.1 shows how a current supply works in a system. The most important requirement for the system is to have a current source that remains as constant as possible regardless of the changes in the load, input supply, temperature, and any other variations that can arise.

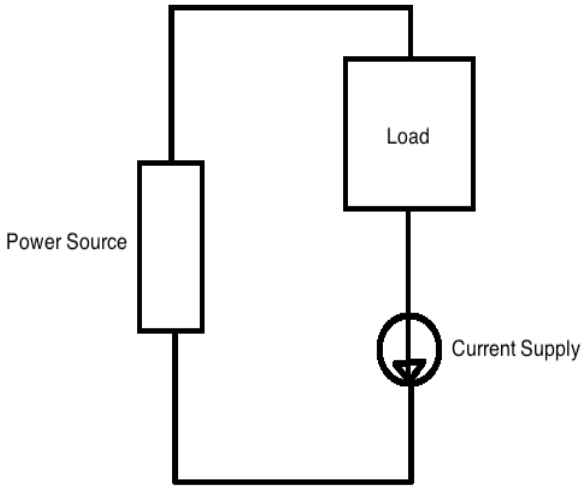


Figure 6.1: A simple block diagram of a general current supply

Current Supply

The current supply in figure 6.1 can be implemented in its simplest form by connecting a resistor to a power supply and duplicating that current to the intended load by using a current mirror as shown in figure 6.2.

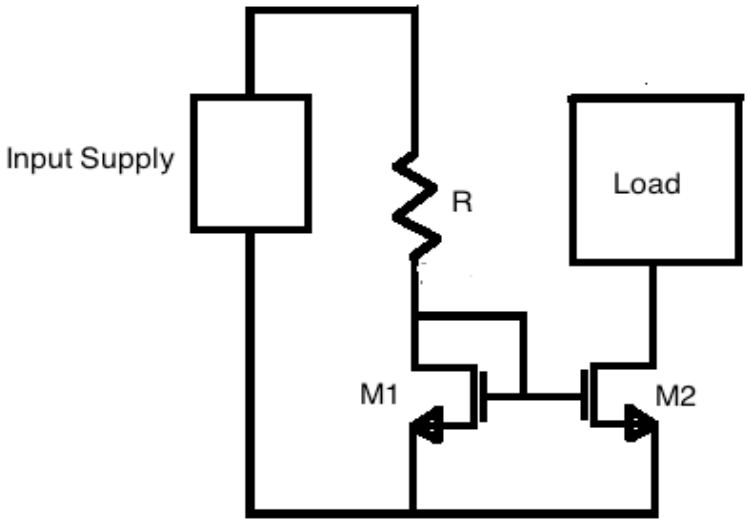


Figure 6.2: A current source generation

A current can be generated whenever a resistor is connected to a voltage source and in this case the current through transistor M1 is:

$$\frac{V_{Input\_Supply} - V_{GS_{M1}}}{R} \tag{6.1}$$

where V_{Input_Supply} = the supply voltage,

$V_{GS_{M1}}$ = gate to source voltage of transistor M1

R = resistor.

The current through M1 is duplicated in M2 through the load by the principle of current mirrors, which is (18):

$$\frac{I_{M2}}{I_{M1}} = \frac{\frac{1}{2}\mu C_{ox}\frac{W_{M2}}{L_{M2}}(V_{GS_{M2}}-V_{th_{M2}})^2(1-\lambda V_{DS_{M2}})}{\frac{1}{2}\mu C_{ox}\frac{W_{M1}}{L_{M1}}(V_{GS_{M1}}-V_{th_{M1}})^2(1-\lambda V_{DS_{M1}})} \quad (6.2)$$

W = width of MOSFET transistor

L = length of the MOSFET transistor

μ = mobility of charge carriers

C_{ox} = oxide capacitance per unit area

V_{th} = threshold voltage

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

λ = channel modulation

The main drawback of this simple system is the inaccuracies in the generated current first, and its sensitivity to the variables within and external to the system.

In reality, power source, temperature and other variations must not impact the system. Therefore, one has to come up with a design that can lower the impacts of these variations to the system. In any type of regulating system a feedback is used to monitor the system and change the variables in a way that system is insensitive to any changes. The way the feedback is implemented depends on whether or not the source and the output is current or voltage. The two most common way of creating a lower output voltage from input voltage are through a linear regulator or a buck regulator (13, 14).

Linear Regulators

A linear regulator is a type of a voltage regulator in which the pass transistor is always on. A linear regulator samples the output voltage and compares it with a stable reference voltage. An error voltage is generated that is used to correct the output voltage accordingly. The operation of the circuit is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. This type of regulator has two inherent characteristics:

1) the magnitude of the input voltage is greater than the respective output and

2) the output impedance is low to yield good performance (14).

Linear regulators can be categorized as either low power or high power. Low power regulators are typically those with a maximum output current of less than 1A, exhibited by most portable applications. On the other hand, high power regulators can yield currents that are equal to or greater than 1A to the output, which are commonly demanded by many automotive and industrial applications (15).

Figure 6.3 is showing a simple schematic of how a low dropout voltage regulator (LDO) accomplishes its operation. One input of the error amplifier is connected to a reference voltage and the other input is connected to the output via a network. Through the network, the error amplifier samples the output and compares it to the reference. An error voltage is created by means of this differential sampling, and this error voltage adjusts the conductance of the power element that will correct the output. The error amplifier, the pass element (transistor), and the feedback network constitute the regulation loop. The temperature dependence of the reference and the amplifier's input offset voltage define the overall temperature coefficient of

the regulator, hence, low drift references and low input offset voltage amplifiers are preferred (16, and 17).

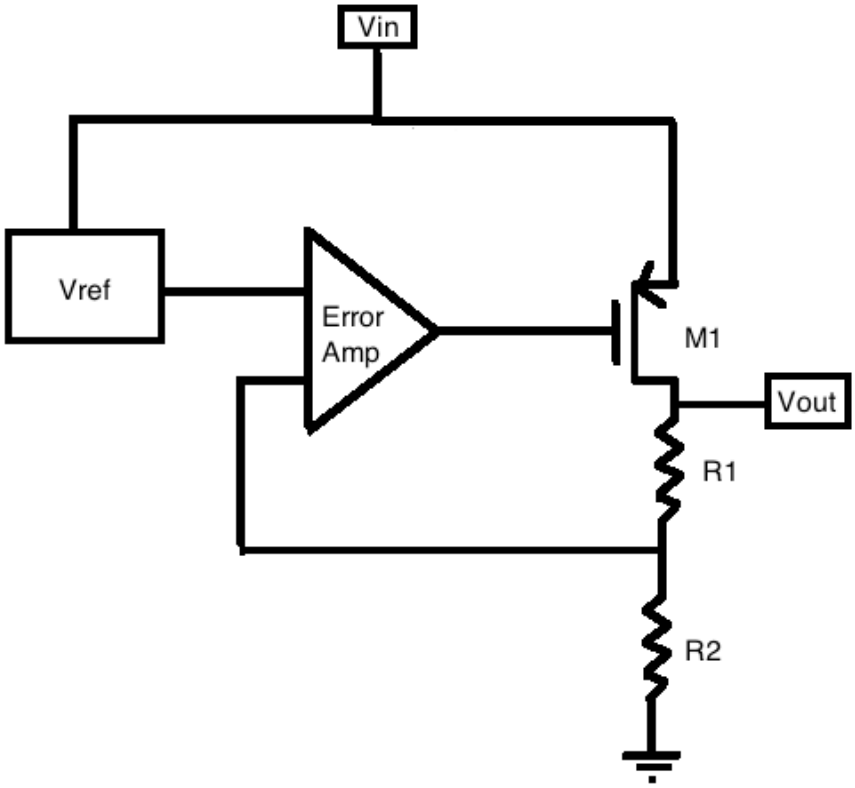


Figure 6.3: A simple block diagram of a low dropout voltage regulator (LDO)

Advantages of Low Dropout Voltage Regulator

The advantages of linear regulators are the simplicity of their design and the rapid response of the system to the changes that are imposed on it. The draw back of using linear regulators is their low efficiency in accomplishing the regulation. Generally speaking the efficiency of the linear regulator can be defined as the output voltage divided by the input voltage:

$$Efficiency = \frac{I_{out}V_{out}}{[I_{out}+I_{sup}]V_{input}} \approx \frac{V_{out}}{V_{input}} \qquad (6.3)$$[11]

where I_{out} and V_{out} correspond to the output current and voltage, I_{sup} corresponds to supply current. If the maximum load current is much greater than the ground current then the maximum possible power efficiency is defined by the ratio of the output and the input voltages, as seen in equation (6.3). Power efficiency increases as the voltage difference between the input and output decreases. Under these conditions, LDOs are better suited for many applications than switching regulators because of the lower cost, complexity, and output noise (16).

Disadvantages of a Low Dropout Voltage Regulator

The choice (between Linear regulator and other regulators) becomes obscure, however, if the output current increases to the point where the LDO requires a heat sink (19). A heat sink not only increases cost by requiring an additional component but it also means more real estate area overhead on the board, which further increases cost. Low dropout regulators tend to necessitate large output capacitors that occupy large board areas. Furthermore, typical LDOs require that these capacitors have low electrical series resistance (ESR). Consequently, capacitors play an intrinsic role in the cost of the LDO (16).

Switching Regulators

Switching regulators belong to another class of voltage regulators where stable output is provided regardless of the variations in the input voltage and the output load conditions. Similar to linear regulators, the output voltage is sampled and compared to a stable reference voltage and the system adjusts its conductance to correct the output voltage. Unlike the linear

[11] Reference (16)

regulators where the power transistor works in the linear region, the switching regulators operate the power transistors in either ON or OFF mode. To put it simply, the switching regulators operate the transistors as switches.

Switching regulators are essentially mixed-mode circuits that feed back an analog error signal and digitally gate it to provide bursts of current to the output. The circuit is inherently more complex and costly than LDO realizations (20). Furthermore, switching regulators can provide a wide range of output voltages including values that are lower or greater than the input voltage depending on the circuit configuration, buck or boost (16). The circuit, for the most part, requires a controller with an oscillator; pass elements, an inductor, capacitors, and diodes. Some switched-capacitor implementations do not require an inductor (21, 22).

Hysteretic Regulator

There are different families of switching regulators that are used by application designers. The first, and the most commonly used, are the fixed frequency regulators, commonly known as Pulse Width Modulators (PWM). The other mode of operation is the variable frequency regulator where the switching frequency changes as a function of load current (23). A particular group of these variable frequency regulators, known as hysteretic regulators, are advantageous since they are unconditionally stable (23). As it can be seen from figure 6.4, the system works by using a comparator with hysteresis. The output voltage is regulated around the reference voltage with a known hysteresis multiplied by the gain factor $\left(1+\frac{R_2}{R_1}\right)$.

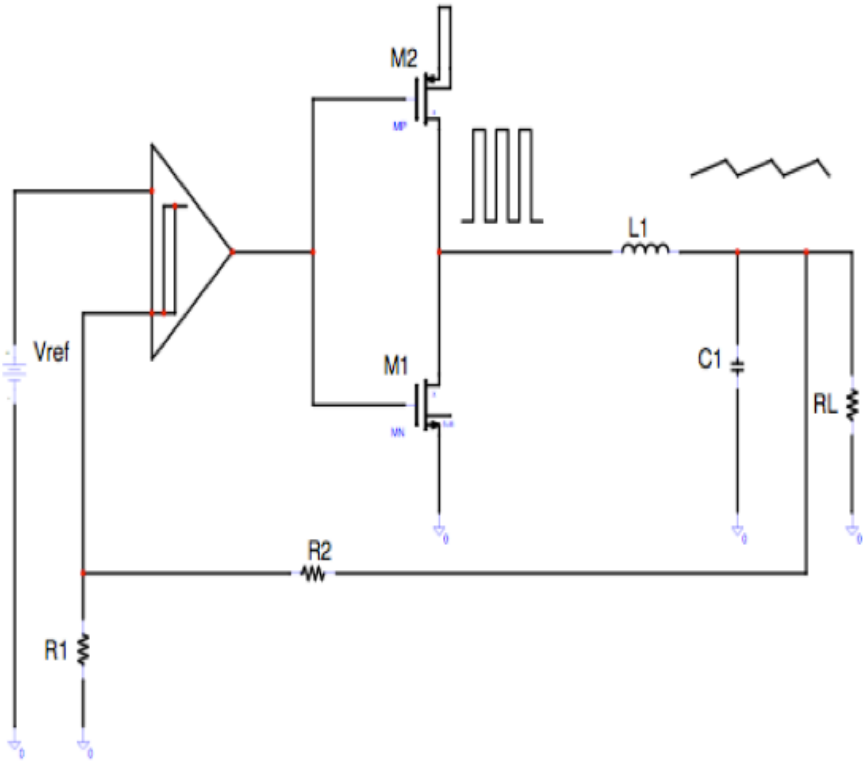


Figure 6.4: A block diagram of a hysteretic regulator

For the design of the intended current supply, a hysteretic regulator is used because it does not require a complex compensation network for loop stability. This will give much flexibility to the designer in choosing the order and type of the filter that is used (24). In a typical switching regulator, a second order filter that is composed of an inductor and a capacitor is used as a filter. This network of an inductor and a capacitor also creates two poles in the small signal domain of the system that makes the loop compensation complicated (13). The addition of higher order filters will lower the output ripple but at the cost of a more complicated compensation scheme. For that matter, most systems will use a two-pole system of an inductor and a

capacitor. But, in a hysteretic regulator, a higher order filter can be used to attenuate the unwanted signals more effectively (25).

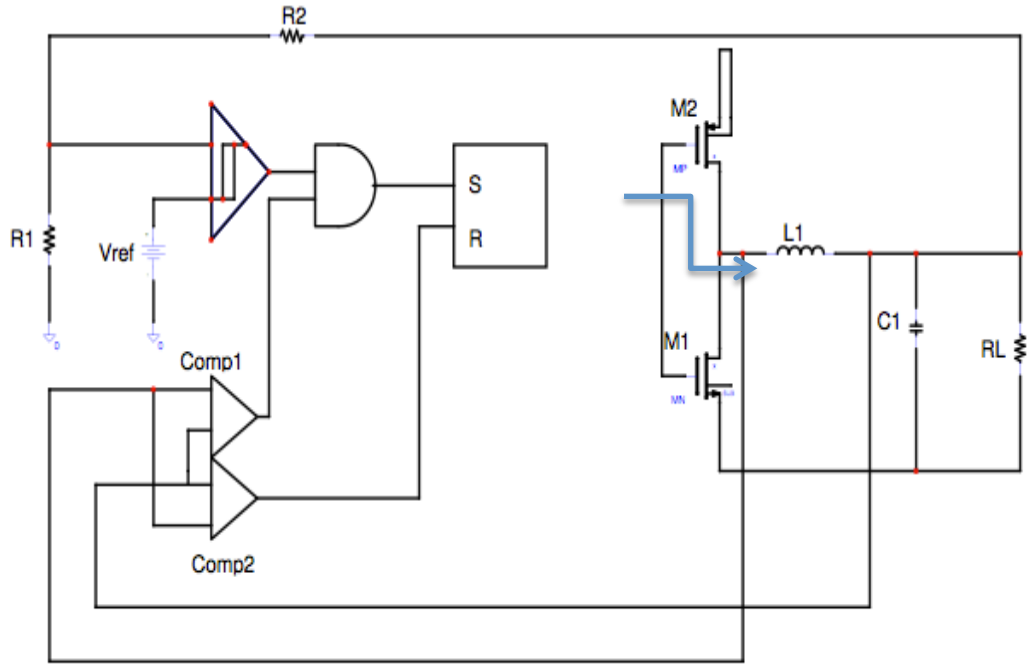


Figure 6.5: A detailed block diagram of hysteretic converter

It is shown in figure 6.5 that there are two loops working to achieve a regulation with limited stability (26). The first loop is the voltage loop that is controlled by the hysteretic comparator, and the second loop is controlled by the current loop. The two comparators Comp1 and Comp2 control the current loop. The waveform in figure 6.6 shows in detail how a hysteretic converter operates. The voltage loop that is controlled by the hysteretic comparator is the master loop. The other two comparators that control the current through the inductor are part of the slave loop.

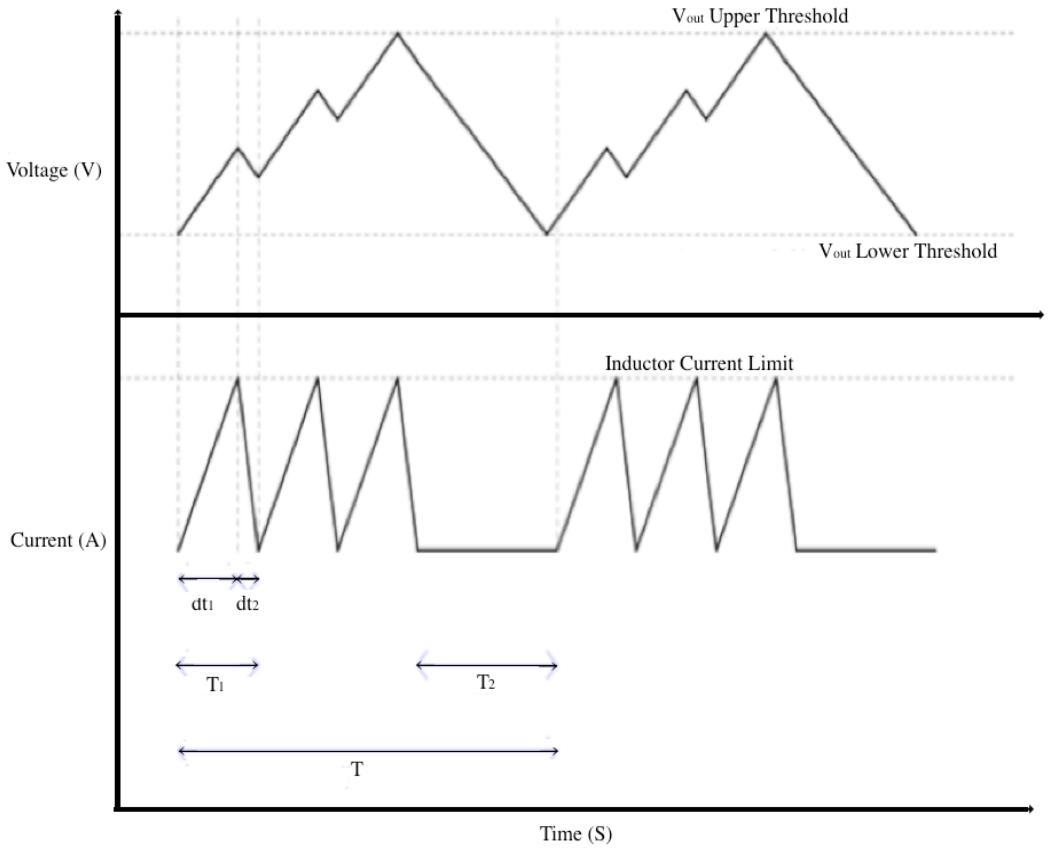


Figure 6.6: The hysteretic mode waveforms

When the voltage at the output has reached the V_{out} lower threshold, then the converter will turn on the system and it will stay on until the V_{out} Upper Threshold is reached. When the system is turned on, the current through the inductor is monitored. Comp1 and Comp2 monitor the information through the inductor and that information is used to turn on and turn off the high side power MOSFETs. The sequence of events work as the following: 1. The PMOS turns on the current though the inductor that increases until the Inductor current limit is reached and Comp2 will turn off the PMOS M2 and turn on the NMOS M1, 2. The inductor current decreases until it reaches zero and Comp 1 will turn on the PMOS and the cycle repeats

itself, 3. This cycle is repeated until the V_{out} Upper Threshold is reached, 4. The system will remain off until the V_{out} Lower Threshold is reached.

In figure 6.6, the values of dt1, dt2, T1, T2, and T must be determined to understand the frequency and the efficiency of the overall system (27). The following design equations must be defined to design the system properly:

$$I_{peak\_PFM} = \frac{V_{in}-V_{out}}{L} dt1 \tag{6.4}$$

$$dt1 = \frac{I_{peak\_PFM}*L}{V_{in}-V_{out}} \tag{6.5}$$

$$dt2 = \frac{I_{peak\_PFM}*L}{V_{out}} \tag{6.6}$$

$$I_{out}T = \frac{I_{peak_{PFM}}}{2} NT1 \tag{6.7}$$

$$NT1 = \frac{2I_{out}}{I_{peak_{PFM}}} T \tag{6.8}$$

$$V_R C1 = I_{out} T2 \tag{6.9}$$

$$T2 = \frac{V_R C1}{I_{out}} \tag{6.10}$$

$$T = NT1 + T2 = \frac{I_{peak\_PFM} V_R C1}{2I_{out}(\frac{I_{peak_{PFM}}}{2} - I_{out})} \tag{6.11}$$

where I_{peak_PFM} = inductor peak current

V_R = output peak to peak ripple

N = number of times that the system will be turned on before reaching the V_{OUT} upper threshold

L = inductor Value

These equations must be used to design the system parameters such as I_{peak_PFM}, and V_R in a way that the system can function properly. For example, the I_{peak_PFM} must be designed to be at least twice as big as the I_{out}; otherwise the converter will become unstable. The theoretical efficiency of this

hysteretic converter can be as high as 100%, but in reality there are losses in the system. The two power switches, NMOS and PMOS are not ideal and they will generate losses in them.

The control circuitries also need current to turn on and start functioning and that lowers the efficiency of the system as well. But, in reality, these converters can have efficiencies as high 90% to 95% (13). One of the main drawbacks of the hysteretic converter is the higher output ripple compared to the typical fixed frequency switching regulators and the linear regulators. This higher ripple at the output can jeopardize the ultimate stability of the current supply; consequently the ripple must be filtered out by a linear regulator.

Linear Regulator

A linear regulator is used to filter out the ripple at the output of hysteretic converter and provide a constant and filtered voltage to the load and the current converter (28,29). For that matter, the linear regulator must have a high power supply rejection ratio at the frequency where the hysteretic converter is switching (30). In figure 6.7, we can see the block diagram of a linear regulator. It is a closed loop feedback system that is composed of a gain stage G_{m1}, A buffer stage A_{v1}, A power transistor stages M2, A resistive network R1 and R2, the load and the C_{out}. In this type of regulator where the output transistor has a follower configuration the output is the low impedance source of the transistor. For that matter, the linear regulator is not compensated at the output, but it is compensated at a high impedance node within the system (14).

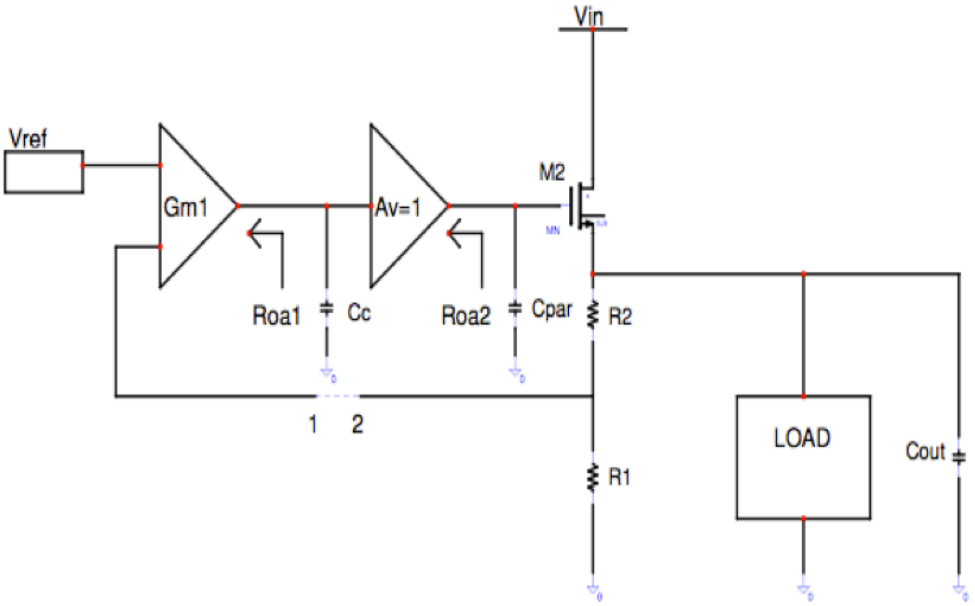


Figure 6.7: The block diagram of a linear regulator

The loop gain can be described by the following expression:

$$\frac{V_2}{V_1} = \frac{G_{m1}R_{oa1}}{1+sC_cR_{oa1}} * \frac{A_v}{1+sC_{par}R_{oa2}} * \frac{G_{mM2}*(R_1+R_2)}{1+G_{mM2}(R_1+R_2)\left[\frac{sC_{out}(R_1+R_2)}{1+G_{Mm2}(R_1+R_2)}\right]} * \frac{R_1}{R_1+R_2} \quad (6.12)$$

From the equation above three poles can be identified that are:

$$p_1 = \frac{1}{2\pi C_cR_{oa1}} \quad (6.13)$$

$$p_2 = \frac{1}{2\pi C_{par}R_{oa2}} \quad (6.14)$$

$$p_3 \approx \frac{1}{2\pi\frac{C_{out}}{G_{mM2}}} \quad (6.15)$$

The first pole, p_1, is the dominant pole of the system and it is used to make the system stable. The second pole is due to the presence of a large gate capacitance of the power MOSFET. That is why a buffer is used with low output impedance so that p_2 is shifted to frequencies beyond the bandwidth of the system. The third pole, p_3, is due to the output capacitance C_{out}, and the

output impedance of the regulator. One of the advantages of a linear regulator is the low output impedance of the regulator, and that automatically shifts up the third pole to frequencies beyond the bandwidth of the system (14, 31). The fact that poles p_2 and p_3 are shifted to higher frequencies, beyond the bandwidth of the system makes the system unconditionally stable.

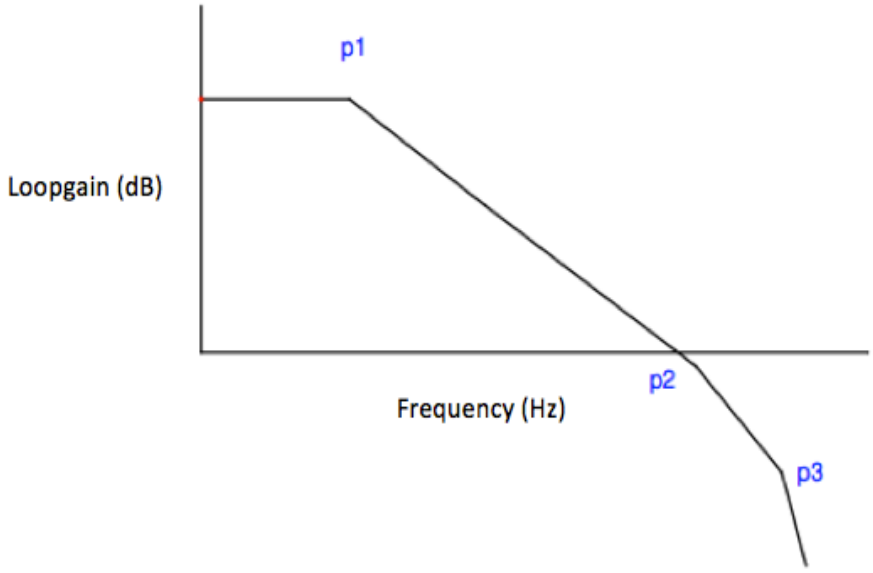


Figure 6.8: The bode plot of the intended linear regulator system

The other significance of the Bode plot in figure 6.8 is in relation to the power supply rejection ratio (PSRR) of this regulator. The PSRR deteriorates as the loop-gain of the system decreases (14, 32). The PSRR can be understood by looking at the figure 6.9.

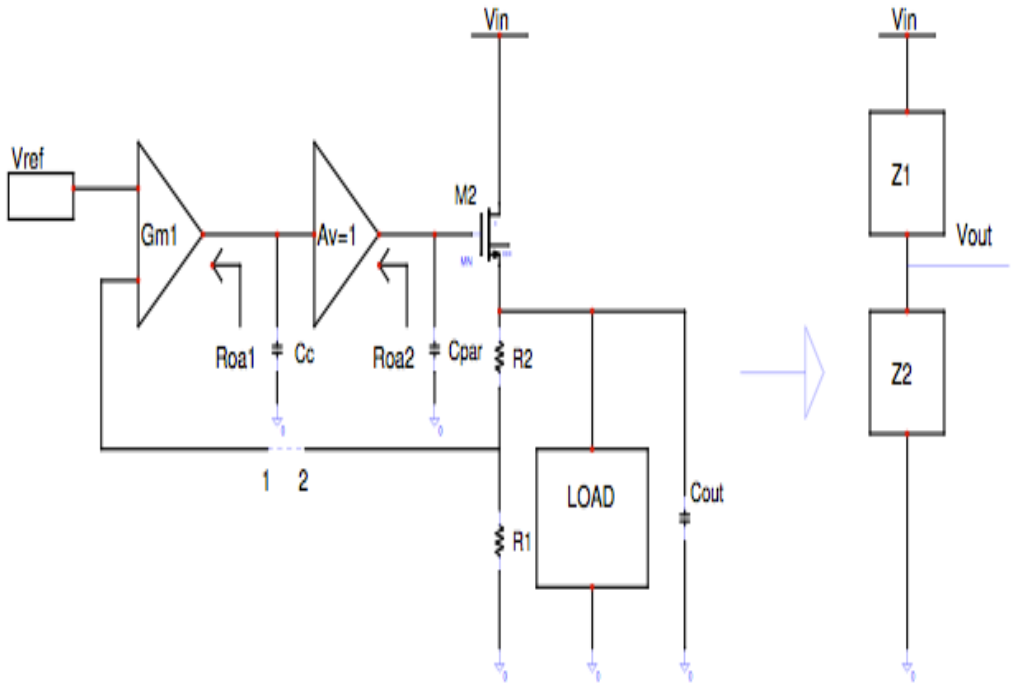


Figure 6.9: An intuitive diagram for understanding the PSRR of the linear regulator

The noise from V_{in} will be coupled to V_{out} through the voltage divider with the impedances Z1 and Z2 . The impedance Z1 is the r_{ds} of the NMOS transistor M2, and the impedance Z2 is the collection of the impedances from V_{out} to ground (32). The following terms will be defined as:

$$Z1 = r_{dsM2} \tag{6.16}$$

$$Z2\_open\_loop = (R_1 + R_2) \| Z_{LOAD} \| \left(\frac{1}{sC_{out}}\right) \tag{6.17}$$

$$V_{out} = \frac{\frac{Z2\_open\_loop}{1+A\beta}}{\frac{Z2\_open\_loop}{1+A\beta} + Z1} V_{in} \tag{6.18}$$

As long as there is loop-gain, the ripple and noise from V_{in} will be attenuated to a large extent before appearing at the output. But as the frequency increases, the loop-gain decreases and consequently, the ability to

attenuate the noise from V_{in} is worsened. In this particular design, the linear regulator must have enough loop-gain at the frequency where the hysteretic converter is switching to filter out the switching ripple. This simplified model only shows the effect of the V_{in} to V_{out}, through the voltage divider model, and it does not take into account the effect of the V_{in} ripple to the amplifier itself and how that will affect the supply noise. The power MOSFET of this linear regulator is of an NMOS type that means whatever signal appears at the gate of NMOS will appear at the output of the system (14, 32). Figure 6.10 shows that if there are disturbances at the gate of the power NMOS, then the noise appears at the output also.

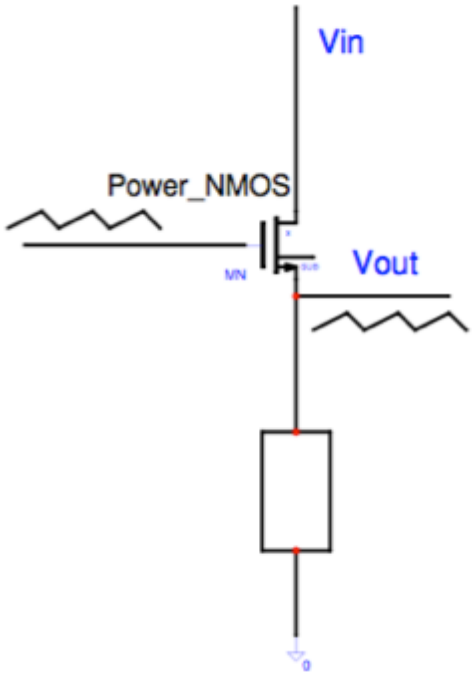


Figure 6.10: The noise transfer from the gate to source of power NMOS

It is clear the amplifier that controls the power NMOS must be insensitive to the noise and variations at the supply. The architecture that will

be used for this design must be able to address this important specification. The architecture shown in figure 6.11, inherently cancels all the noise seen at the gate of power NMOS. The resistive model on the right is the simplification of the circuit on the left, where the resistors represent the drain to source resistance of the circuit on the left. There are two contributions to V_{out} from V_{in}. The first one is through the voltage divider R1 and R2, and the other one is through the current that is generated by the current mirror M4 and M3 (32):

$$V_{out}=V_{in}\frac{R_3}{R_3+R_2}-I_1(R_2||R_3) \tag{6.19}$$

$$I_1=\frac{V_{in}}{R_2} \quad , \quad R_2 \gg \frac{1}{g_{m4}} \tag{6.20}$$

$$V_{out}=V_{in}\frac{R_3}{R_3+R_2}-\frac{V_{in}}{R_2}*\frac{R_3R_2}{R_2+R_3}=0 \tag{6.21}$$

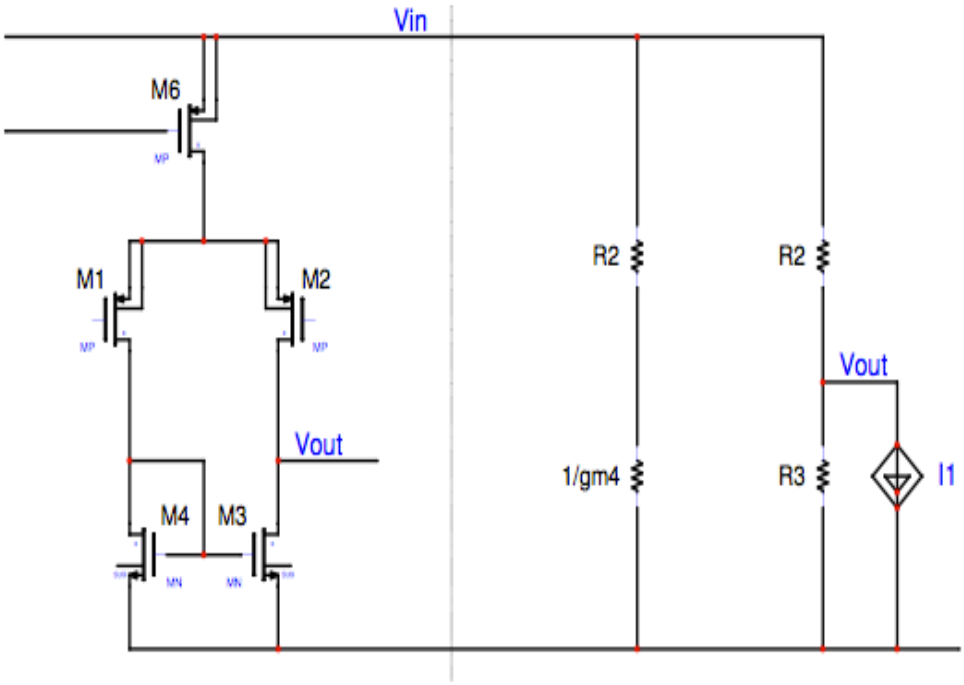


Figure 6.11: An example of a circuit with good PSRR for driving NMOS power FET

The contribution at V_o due to V_{in} has cancelled which means the gate of the NMOS power FET will not modulate due to the noise that is generated at $V_{in.}$ Any architecture where the mirror is referenced with respect to ground will have similar behavior as the example shown above.

The circuit of figure 6.12 shows the purpose of using a linear regulator in this configuration. The figure shows the output of hysteretic regulator has ripples that must be filtered out. In some systems, this ripple can be tolerated, but in ultra sensitive systems these ripples must are not. In order to suppress the output ripple effectively, the linear regulator must have enough loop-gain to do that. The graph in figure 6.8, shows that at the frequency where the system is switching there should be enough loop-gain for an effective ripple suppression.

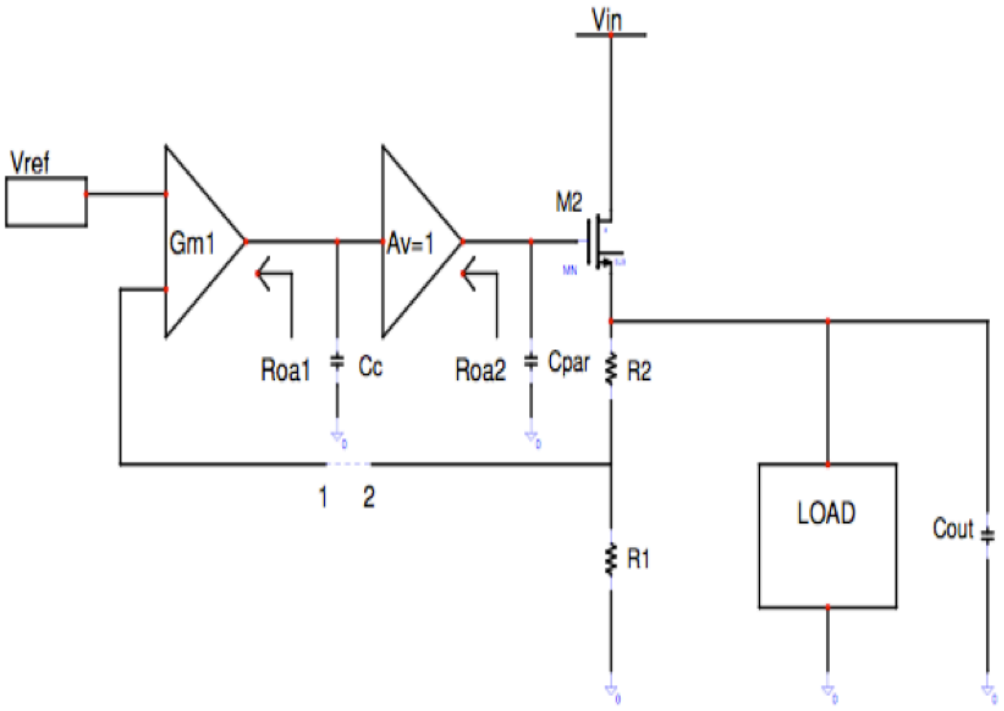


Figure 6.12: The Block diagram of ripple suppression

Current Regulator

A current regulator is, basically, a current source that sinks a constant current. The output impedance of the current source is high, and the higher the output impedance of the current source, then the more ideal the current source becomes. The block diagram in figure 6.13 shows a practical method of generating a stable current supply. This type of current source uses an architecture known as series-series feedback (18, 33). A stable reference voltage V_{ref} is attached to an amplifier, and the amplifier, through the properties of negative feedback, converts this voltage to a current that is

$$I = \frac{V_{ref}}{R} \tag{6.22}$$

In reality a higher output resistance will minimize the variations of current I due to the variations of the drain to source voltage of transistor M_1. Basically, the variations are defined by

$$\Delta I = \frac{\Delta V_{ds}}{R_o} \tag{6.23}$$

where R_o is the output impedance of the complex, which is defined by [39]

$$R_o = (R + r_{dsM1} + g_{mM1} * R * r_{dsM1})(1 + A) \approx g_{mM1} * R * r_{dsM1} * A \tag{6.24}$$

where A is the open loop gain,

r_{dsM1} is the drain to source resistance of M1, and

g_{mM1} is the transconductance of transistor M1.

The actions of negative feedback clearly increase the output impedance of the current supply (18, 33).

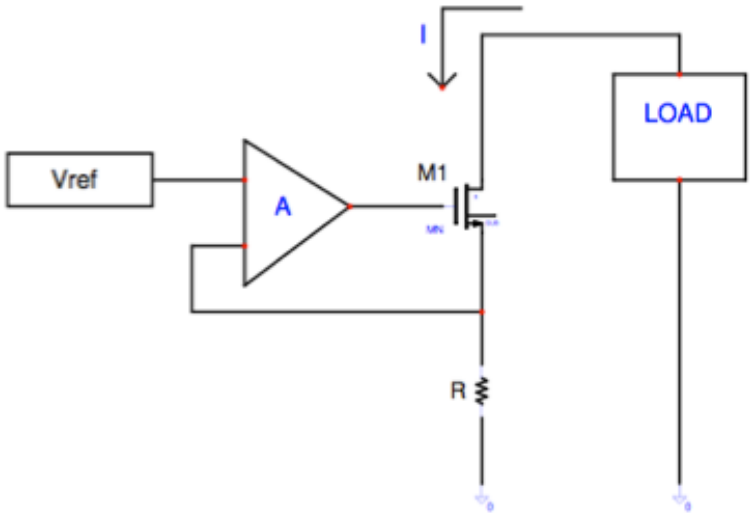


Figure 6.13: The block diagram of a current supply

The current regulator in this system must generate currents of ultra-stability, which means it is desirable to increase the output resistance of the current source of figure 6.13 even more. Any differential voltage change from drain to source of transistor M_1 can cause variations in the current of the current regulator. In order to keep the current absolutely stable, the design must implement a way that prevents any voltage change across the V_{ds} of M_1 (18). In order to achieve this objective, an amplifier is used that will monitor the drain voltage of M_1 and keep it constant by the way shown in figure 6.14. The voltage adjust amplifier (VAA) monitors the drain voltage of the power transistor M_1 against a stable reference voltage V1.

The reference voltage of the hysteretic regulator and the reference voltage of the linear regulator, shown with red lines, are adjusted up and down dynamically. This dynamic readjustment of the reference voltages will guarantee a steady voltage at the drain of M_1, regardless of the conditions of

this particular system. This technique increases the r_{dsM1} by the amount of open-loop gain of the voltage adjust amplifier that is A. The modified expression for the output impedance of the current regulator is:

$$R_o = (R + A_2 r_{dsM1} + R g_{mM1} A_2 r_{dsM1})(1 + A_1) \approx R g_{mM1} A_1 A_2 r_{dsM1} \quad (6.25)$$

R_o increases by the amount of open-loop gain of the voltage adjust amplifier (34), which should be designed to be around 80,000 to 100000. The value of R_o has increased to such an extent that the output impedance of this current source resembles an ideal current supply.

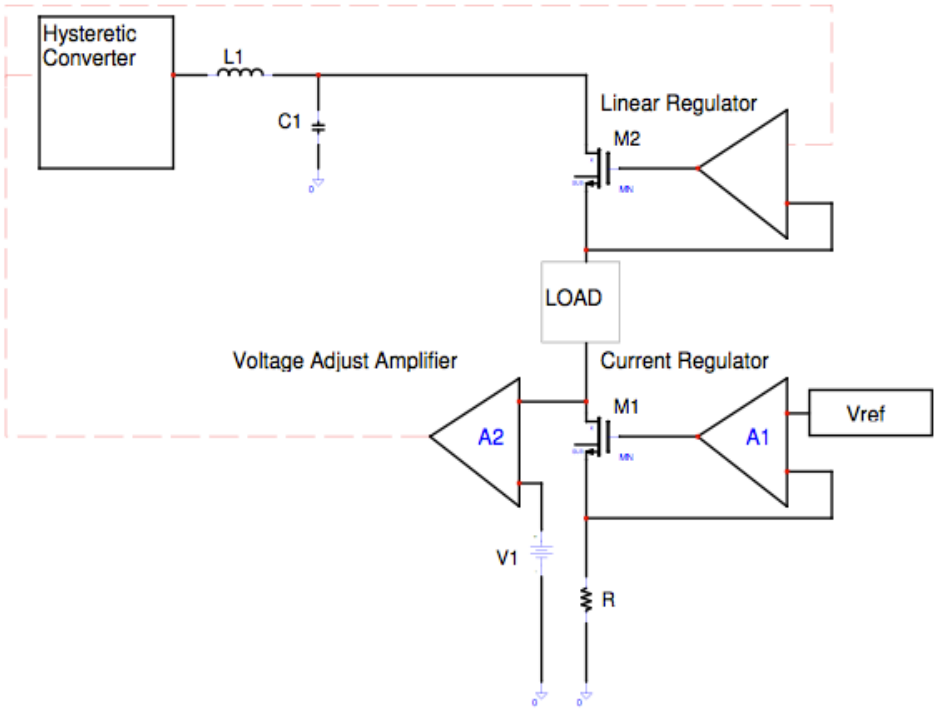


Figure 6.14: The Simplified block diagram of the overall system

Another factor that must be taken in account is the power dissipation of the system. Most of the power dissipation occurs within the power FETs. The hysteretic regulator has more power FETs than any other block in this system, but due to the switching nature of this particular converter, the losses are minimized (35). The major portions of the losses are through the power FETs of the linear regulator and the current regulator. The power losses through the power FETs are (31):

$$Power\ Loss = I_{drain} V_{ds} \tag{6.26}$$

The drain current (I_{ds}) in this current supply, on average, is fixed around 1A, but the parameter that can vary by design to lower the power loss is the drain to source voltage (V_{ds}) of the transistors. The drain to source voltage of the transistors should be as low as possible to lower the losses, but it should not be lower than the minimum V_{dsat} of the transistor. If the voltage falls below the minimum V_{dsat} of the transistor, then the transistor will enter the linear region and its output impedance drops. By looking at the I_{DSAT} vs. V_{DSAT} graph of the power FET transistor, it can be determined as to what the minimum V_{ds} of these power FETs should be.

The I_{ds} vs. V_{ds} in figure 6.15 shows the characteristics of these transistors, and at what voltage they enter the linear region and lose their gain. The change from linear region to saturation region happens at the drain to source differential voltage of 200mV. For that matter, the drain to source voltages of the power FETs M1 and M2 are kept at 200mV to lower the losses and at the same time keep the power FETs in saturation for maximum gain. For that matter, the voltage adjust amplifier will keep the drain voltage of the current Supply power transistor M1 at 800mV. It will adjust the source voltage of the linear regulator power FET M2, always, 200mV below the output voltage of the hysteretic converter.

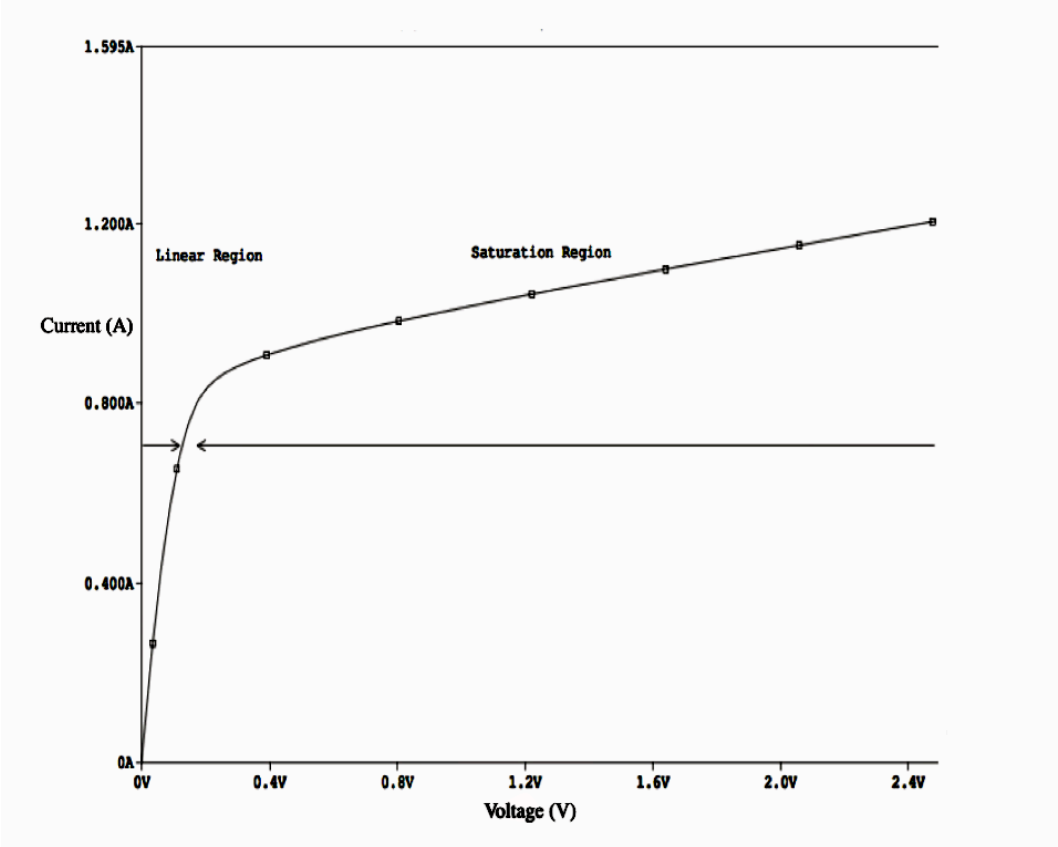


Figure 6.15: The I_{ds} vs. V_{ds} graph of the power NMOS FETs

The picture of the system, as shown, in figure 6.16 shows how the voltages are set up in the system to make certain the differential drain to source voltages of both transistors M1 and M2 are always about 200mV. The reference voltage to current regulator is 600mV and due to its buffer configuration the source voltage of M2 is 600mV. The voltage adjust circuitry, through the action of the overall negative feedback, guarantees the drain voltage of M2 will be 800mV. In order to make the drain voltage of transistor M2 800mV, the voltage adjust amplifier varies the reference voltage of digital converter and linear regulator dynamically throughout the operation.

The digital converter has a buffer configuration; so it's output voltage will be the same as its reference voltage. The reference voltage of the linear regulator is set to be 200mV lower than the hysteretic converter, and by looking at figure 6.16, it can be seen the source voltage of power transistor M1 will 200mV lower than its drain voltage.

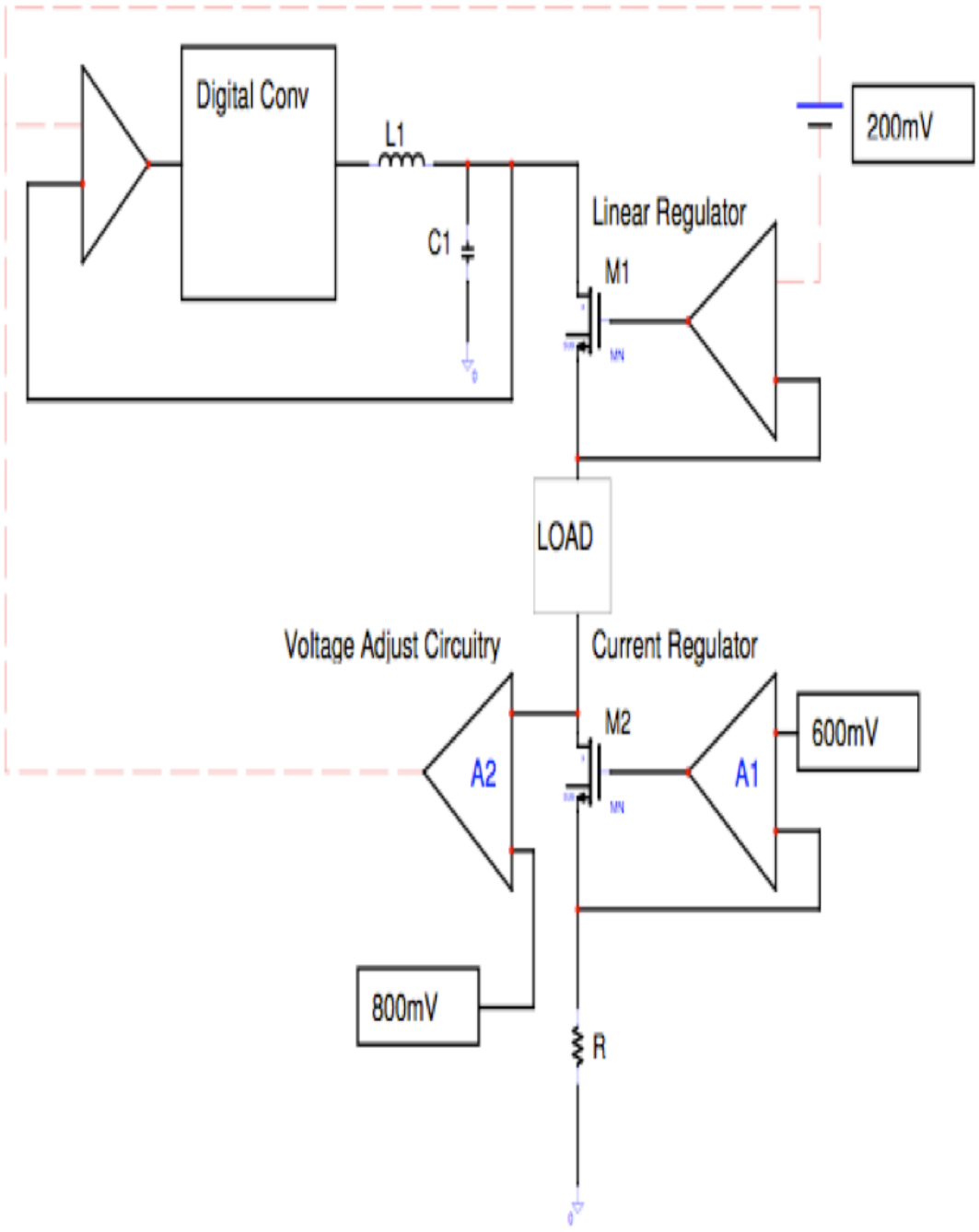


Figure 6.16: Methods of creating 200mV V_{ds} across Power FETs M1 and M2

The voltage adjust amplifier's functions are twofold. Its first purpose is to increase the output impedance of current regulator block by the amount of its open-loop gain, which is substantial. The increase in the output impedance of the current regulator makes sure the load current, which supplies the magnetic lens of the microscope remains within the range allowed to reach the required stability. The other function of the voltage adjust amplifier is to adjust the reference voltages of the hysteretic converter and the linear regulator to keep the drain to source voltage differentials of the power transistors M1 and M2 around 200mV. In keeping this voltage differentials 200mV, the power loss is minimized and the transistors are still in the saturation region.

Reference Voltage

The ultimate integrity of this design lies in the quality and stability of the reference voltage. The reference voltage must remain, absolutely, stable regardless of the changes in temperature or input voltage. The design of this reference must satisfy two objectives that are:

1. A stable voltage with respect to temperature, and

2. A stable voltage with respect to supply voltage.

A Stable Voltage Reference

The stability of this reference is explained by the term temperature coefficient (TC) and is normally expressed in parts-per-million per degree Celsius (ppm/^{o}C) (36),

$$TC_{ref} = \frac{1}{Reference} * \frac{\Delta Reference}{\Delta Temperature}. \quad (6.27)$$

The overall stability is determined, primarily, by the inherent or initial stability of the reference and, secondarily, by the line regulation and temperature drift performance that is described by

$$Stability = \frac{\Delta Reference_{IC} + \Delta Refernce_{TC} + \Delta Reference_{LNR}}{Reference} \quad (6.28)$$

where the subscripts IC, TC, and LNR refer to initial stability, temperature coefficient, and line regulation performance, respectively. In order to have the overall ultra stability that is required, this current supply requires a second order bandgap voltage reference. A bandgap voltage reference is a temperature independent voltage reference circuit that is mostly used in integrated circuits. Its output voltage is around 1.25V that is close to the theoretical 1.22eV bandgap of silicon at 0K (In this paper bandgap voltage reference is sometimes referred to as bandgap).

A bandgap voltage reference is a combination of two voltage sources that have opposing responses with respect to temperature. Figure 6.17 shows the basic concept of a bandgap and how it works. The V_{BE} of a bipolar transistor has a negative temperature coefficient -2mV/^{o}C as shown in figure 6.17. Another voltage, V_{PTAT} that has a positive temperature coefficient is added to it in the right proportion and the result is a voltage that is constant with respect to temperature. The equation shows this relation (37)

$$V_{ref} = V_{BE} + V_{PTAT} \quad (6.29)$$

The V_{BE} of a bipolar transistor can be expressed as [43]

$$V_{BE} = A - BT - CT^2 - DT^3 - ET^4 - \ldots \quad (B >> C >> D >> E >> \ldots) \quad (6.30)$$

where the coefficients A, B, C, D, and D are constants. A first order bandgap adds a V_{PTAT} that cancels the first order term BT only. The stability of such

bandgaps is in the range of 10 ppm/^{o}C and is not good enough for the current design. A second order bandgap adds a voltage that cancels a first order term BT and the second order term CT^2. The stability of such bandgap references can be in the range of 0.005 to 0.01 ppm/^{o}C. So, the V_{PTAT} voltage that is designed for this current supply will have the characteristic of

$$V_{PTAT} = bT + cT^2 \tag{6.31}$$

and when the two voltages are added, it can be written as

$$V_{BE} + V_{PTAT} = A - (BT - CT - DT3 - ET4 - \ldots) + (bT + cT2) \tag{6.32}$$

$$V_{BE} + V_{PTAT} = A + (b - B)T + (c - C)T2 + (d - D)T3 - ET4 - \cdots \tag{6.33}$$

If the coefficient of b and c are designed properly, then a second order bandgap with the desired temperature stability can be achieved.

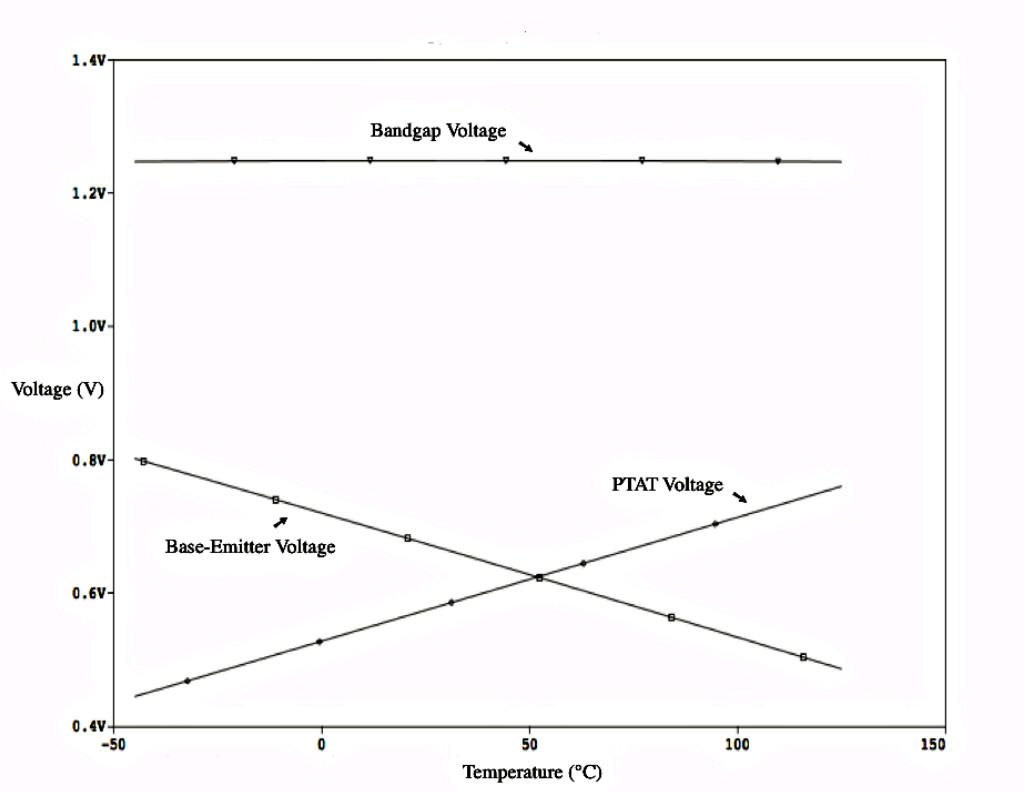


Figure 6.17: The basic operation of bandgap system

In order to get the stability of voltage with respect to temperature that is required for the design of this particular current supply, a second order bandgap reference is designed. Figure 6.18, shows the general waveform of a 1st and 2nd order bandgap, and it can be seen that second order, due to its shape, varies less with respect to temperature (38, 40).

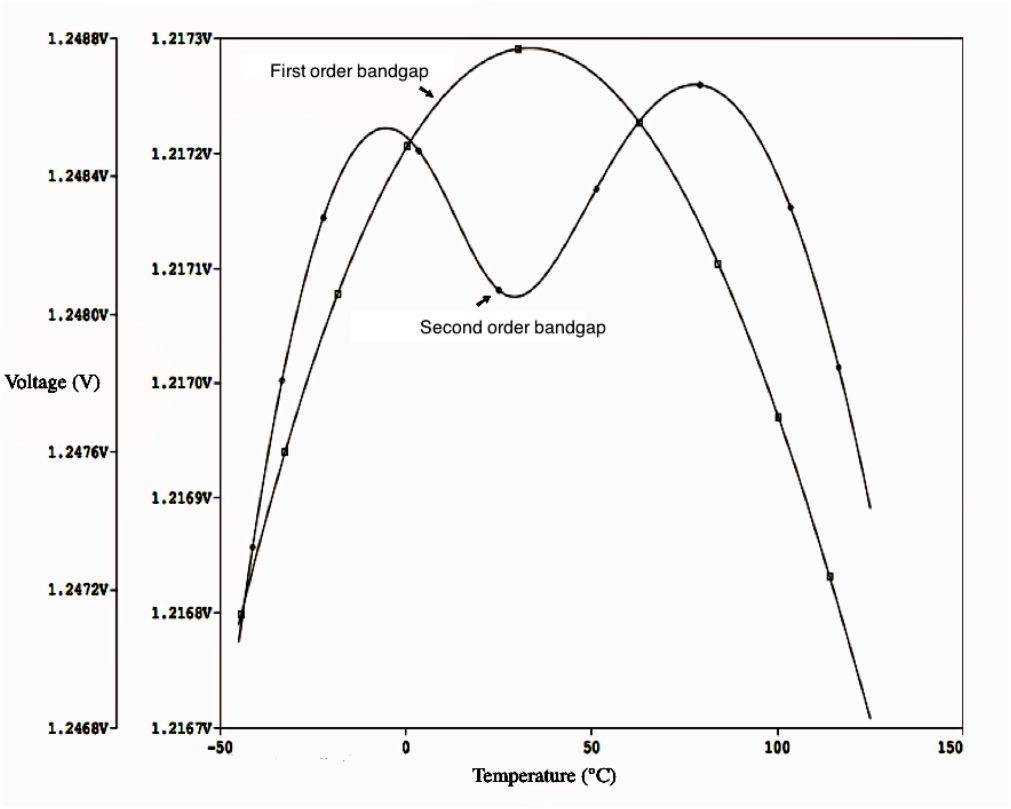


Figure 6.18: The waveforms of 1st and 2nd order bandgaps

The other factor that is important in designing the ultra stable voltage reference is the stability of the reference with respect to supply voltage. The supply voltage could have noise and ripple voltage present on it and that could

jeopardize the stability requirements of the current supply. In this design, the bandgap is completely isolated from the supply by a second supply.

Instead of connecting the bandgap directly to the supply, a secondary bandgap is designed that creates a reference voltage for the amplifier that supplies the primary bandgap. This scheme is shown in figure 6.19 where the ultra high PSRR bandgap complex is shown. The intent of this complex design is to isolate the primary bandgap as much as possible from the external supply (36).

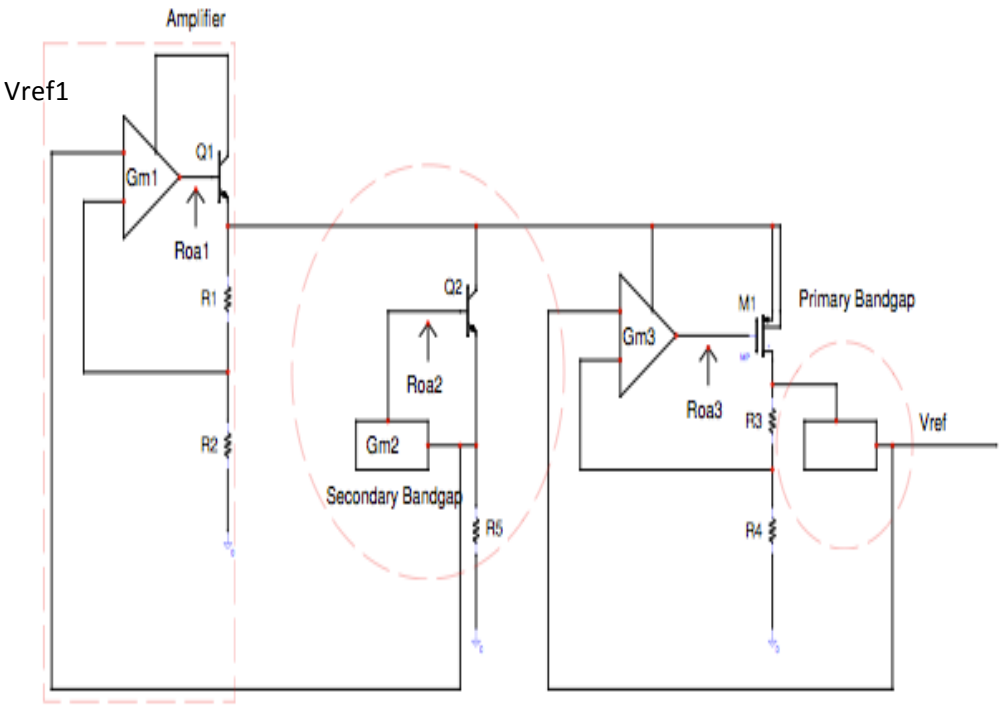


Figure 6.19: The block diagram of the bandgap complex

When the power supply is turned on, the amplifier is turned on first. A coarse voltage reference, low quality voltage reference, is used to bring up the output voltage of the amplifier to the point that the secondary bandgap can

function properly. After the secondary bandgap is turned on, it will be used as the reference voltage to the amplifier. This technique is used to isolate the secondary bandgap from the supply. The noise from the supply that can jeopardize the stability of the current supply will be attenuated by the PSRR of the amplifier and the secondary bandgap. This relation can be described by the following equation:

$$V_{ref1} = V_{Secondary\ Bandgap} + \Delta V_{noise} * PSRR_{Amplifier} * PSRR_{Secondary\ Bandgap} \tag{6.34}$$

$$PSRR_{General\_Description} = \frac{\frac{Impedance_{Output\_to\_Ground}}{1+Loop\ Gain}}{Impedance_{Input\_to\_Output} + \frac{Impedance_{Output\_to\_Ground}}{1+Loop\ Gain}} \tag{6.35}$$

$$PSRR_{Amplifier} = \frac{\frac{R1+R2}{1+G_{m1}R_{oa1}*\frac{R2}{R1}+R2}}{R_{Collector\ to\ Emitter(Q1)} + \frac{R1+R2}{1+G_{m1}R_{oa1}*\frac{R2}{R1}+R2}} \tag{6.36}$$

$$PSRR_{Secondary\ Bandgap} = \frac{\frac{R_5}{1+G_{m2}R_{oa2}}}{R_{Collector\ to\ Emitter(Q2)} + \frac{R_5}{1+G_{m2}R_{oa2}}} \tag{6.37}$$

where the G_ms represent the transconductances of the amplifiers and the R_{oa}s represent the output resistances of the G_m stages. It can be seen that this technique attenuates any noise that is present on the supply. The loop gain decreases with increasing the frequency as shown in figure 6.8, so the PSRR will degrade and the noise on the supply attenuates less as frequency is increased. Since there will be ripple at the switching frequency of the hysteretic converter, then the bandgap complex must have enough loop-gain to filter out the noise. By the same analysis, the PSRR of the primary bandgap can, also, be defined with the equation

$$PSRR_{Primary\ Bandgap} = \frac{\frac{R3+R4}{1+G_{m3}R_{oa3}G_{mM1}R_{OUT}\frac{R4}{R4+R3}}}{R_{Drain\ to\ Source\ M1} + \frac{R3+R4}{1+G_{m3}R_{oa3}G_{mM1}R_{OUT}\frac{R4}{R4+R3}}} \tag{6.38}$$

where R_{out} is the output impedance of the primary bandgap. The overall PSRR of this bandgap complex is:

$$PSRR_{COMPLEX}=PSRR_{Amplifier}PSRR_{Secondary\ Bandgap}PSRR_{Primary\ Bandgap}. \quad (6.39)$$

The changes in the main reference voltage, ΔV_{ref}, with the disturbances in the input voltage, ΔV_{input}, can be defined by the expression

$$\Delta V_{ref} = \Delta V_{input} PSRR_{COMPLEX} \quad (6.40)$$

If each stage is designed to have a PSRR of 10,000, which is typical of a basic analog block, then the PSRR of the complex will have a value of $10{,}000^3$, which is one trillion. This value is more than adequate to meet the design requirements of this current supply design.

Conclusion

In this chapter, the basic design strategy of this particular current supply was laid out. Since the ultimate stability of this current supply must be, at least, 0.01 ppm/^{o}C, that means the sensitivities to any changes in the system must be well understood and controlled. The first stage of this design requires a step down in voltage, and this voltage step down can be accomplished in different ways. This, particular, design uses a switching converter to achieve the step down due to its high conversion efficiency. One of the most sensitive parameters that must be controlled in the design of the ultra stable current supply is the heat generation.

The hysteretic converters step down the voltage with good efficiency that can be in the range of 92-95%. Whereas a linear regulator performs the same task with an efficiency of less than 30% and that means much heat generation. Heat can cause variations in important parameters such as the reference voltages, change in the offset voltage of the important analog blocks in the system, and other things. These changes can influence the ultra stability that is required and jeopardize the design of the ultra stable current supply. For that reason, a hysteretic converter is selected instead of linear regulators.

The hysteretic converters also have the advantage that they are unconditionally stable, so the complexity of compensating the system is relieved.

The drawback of a hysteretic converter is a higher ripple at the output of the converter. The ripple must be filtered; otherwise the noise might jeopardize the stability that must be obtained. A linear regulator is, usually, used as a post regulation point of the switching regulators. The linear regulator must be designed for wide bandwidth and it must have the right architecture for an inherent high power supply rejection ratio (PSRR). Finally, a clean supply is connected to the load and the load is connected to the current regulator. The current regulator uses a high-gain and high-bandwidth amplifier to increase the output impedance of the current source over a wide frequency range.

In order to increase the output impedance of the current regulator another amplifier, the voltage adjust amplifier (VAA) is added to the system. The VAA increases the output impedance of the current regulator by the open-loop gain of the VAA, which could be around 100000 V/V. Another function of the VAA is to lower the thermal waste that is generated in the power NMOS FETs of the linear regulator and the current regulator. By keeping the drain to source voltage differential at the edge of saturation voltage (V_{DSAT}), then the thermal waste is minimized and the system does not lose the large gain that it needs for proper operation. A bandgap complex is designed in a special way to increase the integrity and stability of the system to a reasonably high degree.

Chapter 7

General Design Strategy

In this chapter a general description of the overall circuit and each of its blocks will be given. There are 9 general blocks. The complete block diagram of this current source system is shown in figure 7.1

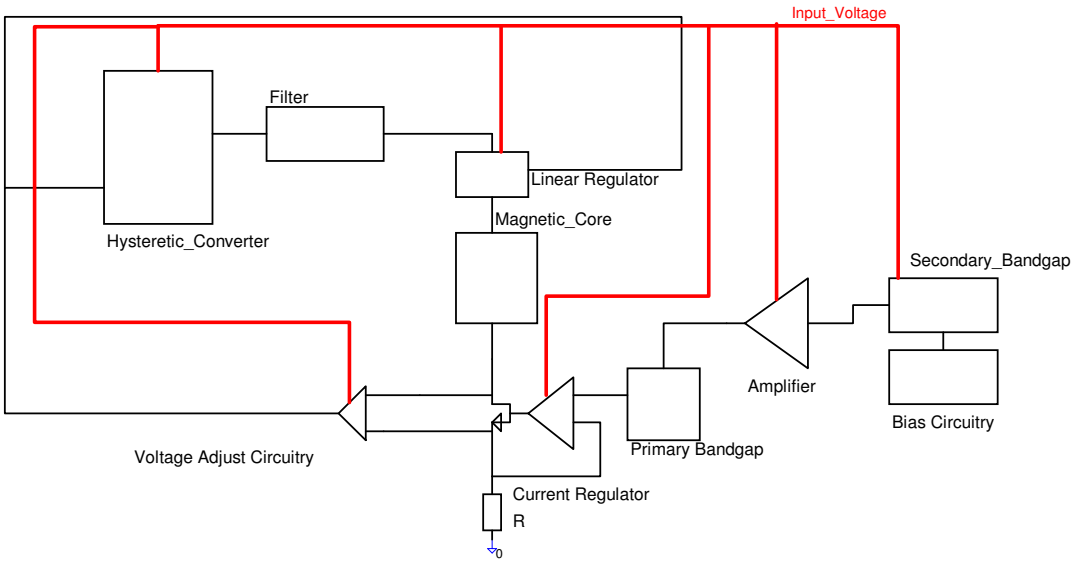


Figure 7.1: The complete block diagram current supply

The current supply system is composed of many sub block levels that are:

- Hysteretic regulator
- Bandgap complex which includes the secondary bandgap, amplifier, and the primary bandgap
- Filter
- Linear regulator
- Current regulator

- Voltage adjust circuitry

In the subsequent pages, each part of the system will be elaborated. Finally, the whole integrated system will be examined and discussed. The hysteretic converter, which is comprised of different sub blocks, converts a higher input voltage to lower output voltage with high efficiency. The Filter block integrates the output of the hysteretic converter and it puts out a constant output voltage, although with ripple. The linear regulator with a high power supply rejection ratio (PSRR) will filter out the ripple. The current regulator draws the actual current through the load that does not change with time, temperature, or supply voltage.

The voltage adjust circuitry ensures a constant drain to source voltage of 200mV across the power NMOS transistor of the current supply for two reasons. The output resistance of the current supply is increased by the open loop gain of the voltage adjust circuitry amplifier, and heat generated by the power NMOS transistor is kept at minimum through a low drain to source differential voltage. The secondary bandgap and bias circuitry generate all the reference voltages and bias currents. The primary bandgap produces the ultra stable voltage that is used by the current regulator for current generation.

Hysteretic Regulator:

A hysteretic regulator establishes a regulated output voltage from an unregulated input voltage. It will do so by comparing a portion of the output voltage to a voltage reference and adjust the output power transistor in a way that output voltage will stay to the reference voltage. Unlike standard switching power supplies and linear power supplies where the feedback must be compensated for stability, the hysteretic regulator does not need to do so. The hysteretic regulator can be called a digital counterpart to the typical linear switching regulators. It will respond immediately to any variations at the input

voltage, output load variations, temperature drifts, and all other parameters that could interfere with the output regulation. But, a hysteretic regulator has disadvantages of its own. The main drawback of this particular family of regulator is that it has a higher ripple output voltage. For example a typical linear regulator has output voltage ripples in the range of nano-volts a switching regulator can have voltage ripples as high as 10mV to 40mV, but a hysteretic regulator could have output voltage ripples as high as 100mV.

Each hysteretic block contains seven sub-blocks. They are as follows:

- Hysteretic comparator
- High-side current sense amplifier
- Current limit comparator with hysteresis
- Low-side zero crossing amplifier
- NMOS and PMOS power switches
- NMOS and PMOS drivers

The simplified picture of a hysteretic regulator is shown in figure 7.2. The hysteretic converter is a self-oscillating system and it will switch with a frequency that is directly related to the load. There are two loops that enable the system to monitor and regulate the output voltage, the voltage loop and the current loop.

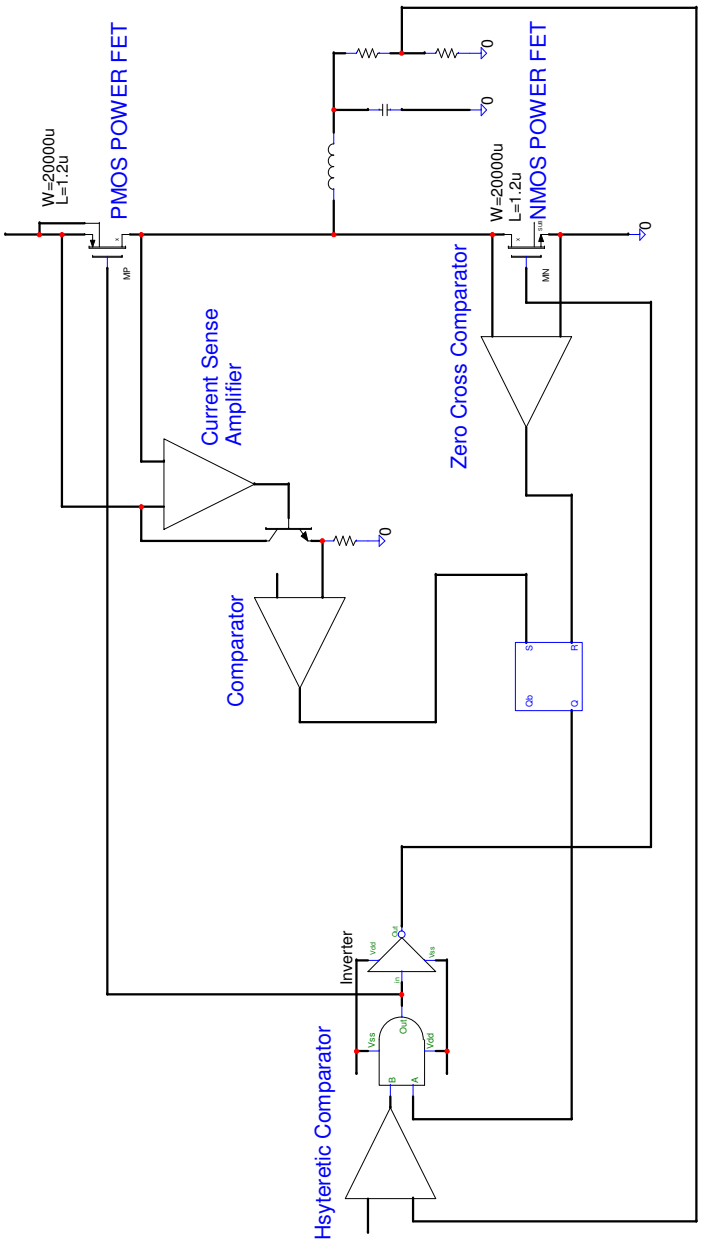


Figure 7.2: The simplified schematic of proposed hysteretic regulator

The hysteretic comparator monitors the voltage loop, and this loop will determine whether or not the current loop is on or off. The hysteretic regulator functions as follows:

When the hysteretic comparator determines the output voltage is below the optimum value, then it will activate the current loop. The current loop is composed of the current sense amplifier, comparator, zero cross comparator, and the detection logic. The current loop will function in four steps. The PMOS POWER FET is turned on, and the inductor current starts increasing by the following relation $\frac{V_{in}-V_{out}}{L}$. The current sense amplifier will convert this current information to a voltage, and a comparator monitors this voltage. When the peak current is reached, a pre-determined value as set by design, then the comparator sends a signal to the Detection Logic to shut off the PMOS POWER FET and turn on the NMOS POWER FET.

A diode can be used instead of the NMOS POWER FET, but due to the lower voltage across the NMOS POWER FET a higher efficiency is obtained. But, the higher efficiency comes at the cost of higher complexity in the circuit design. When the NMOS POWER FET turns on the inductor current will ramp down with the following relation $\frac{V_{out}}{L}$. The NMOS POWER FET is on until the current through the inductor reaches zero, and at this point the ZERO CROSS COMPARATOR turns off the NMOS POWER FET. At this point, if the output voltage has reached its optimum point, then the system will be turned off until the system is turned on. But, if the output voltage is still below the optimum voltage, then the DETECTION LOGIC will turn on the PMOS POWER FET and the cycle will repeat itself.

The waveform of figure 7.3 clearly shows the sequence of actions summarized above. The level of switch node will determine whether or not the PMOS POWER FET is on or off. When the switch node is high, the

PMOS POWER FET is on, and the inductor current is increasing by the relation described above. When the inductor current reaches the value determined by the design, the switch node falls, which means the NMOS has turned on. The current through the inductor will ramp down until it reaches a zero current level, and the NMOS POWER FET will turn off. At this point, the output voltage has reached the positive voltage threshold of the hysteretic comparator and the system shuts off, but if it had not reached the optimum value, then it would have shut off. The true schematic of the hysteretic Regulator is shown in Figure 7.4.

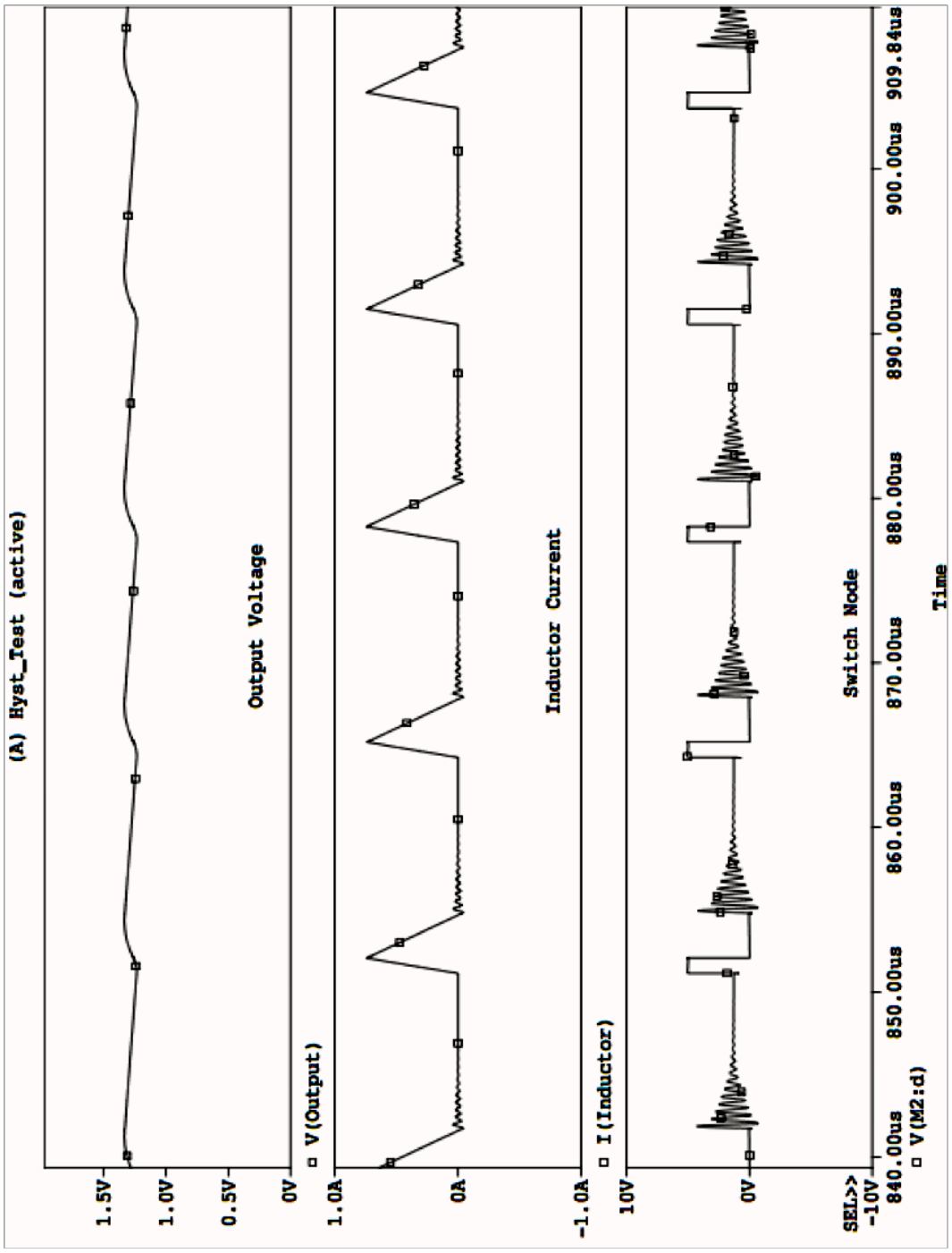


Figure 7.3: Waveforms of hysteretic regulator

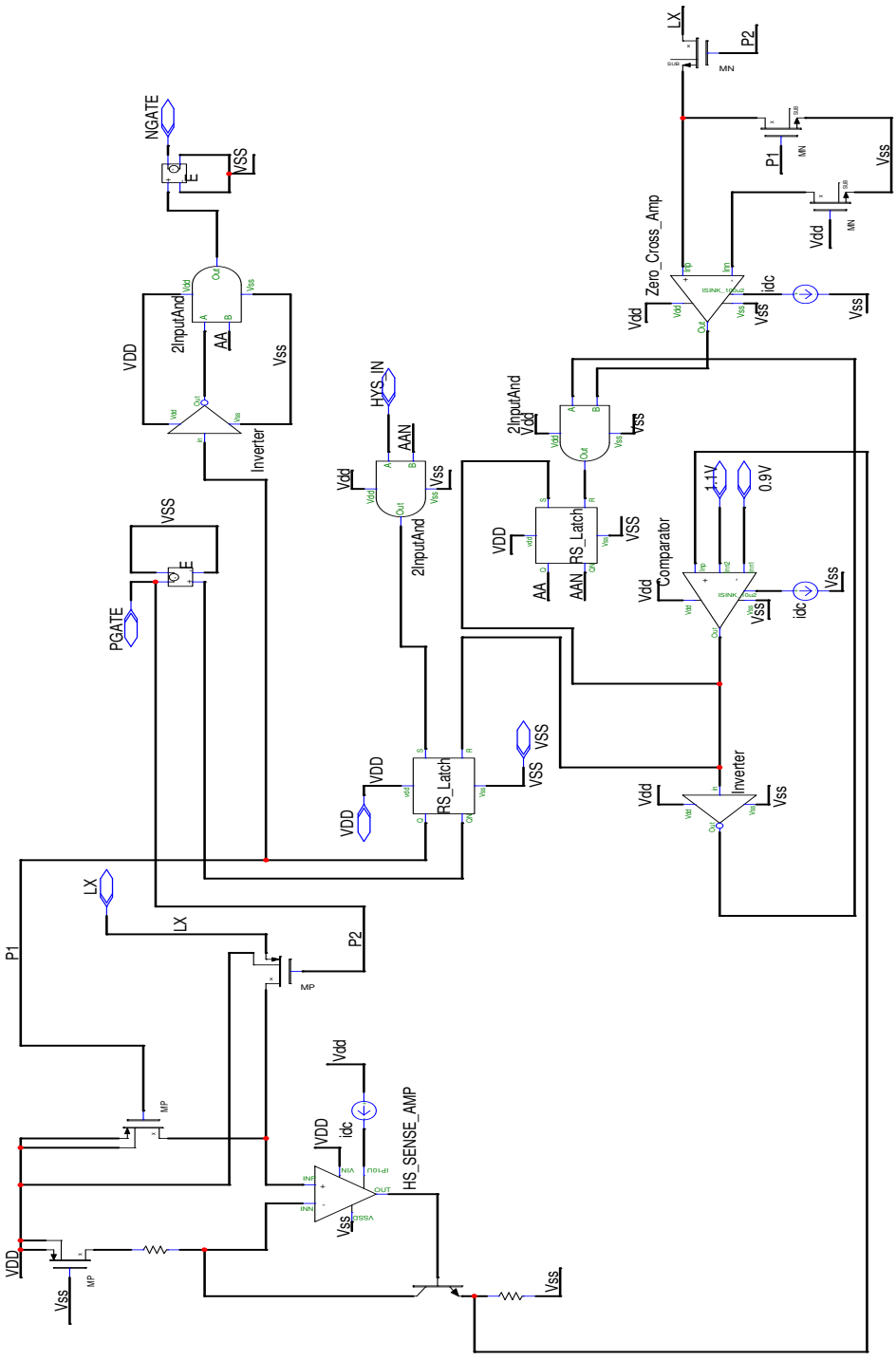


Figure 7.4: The schematic of hysteretic regulator

Each current supply uses five hysteretic regulators to regulate the output voltage of the current supply.

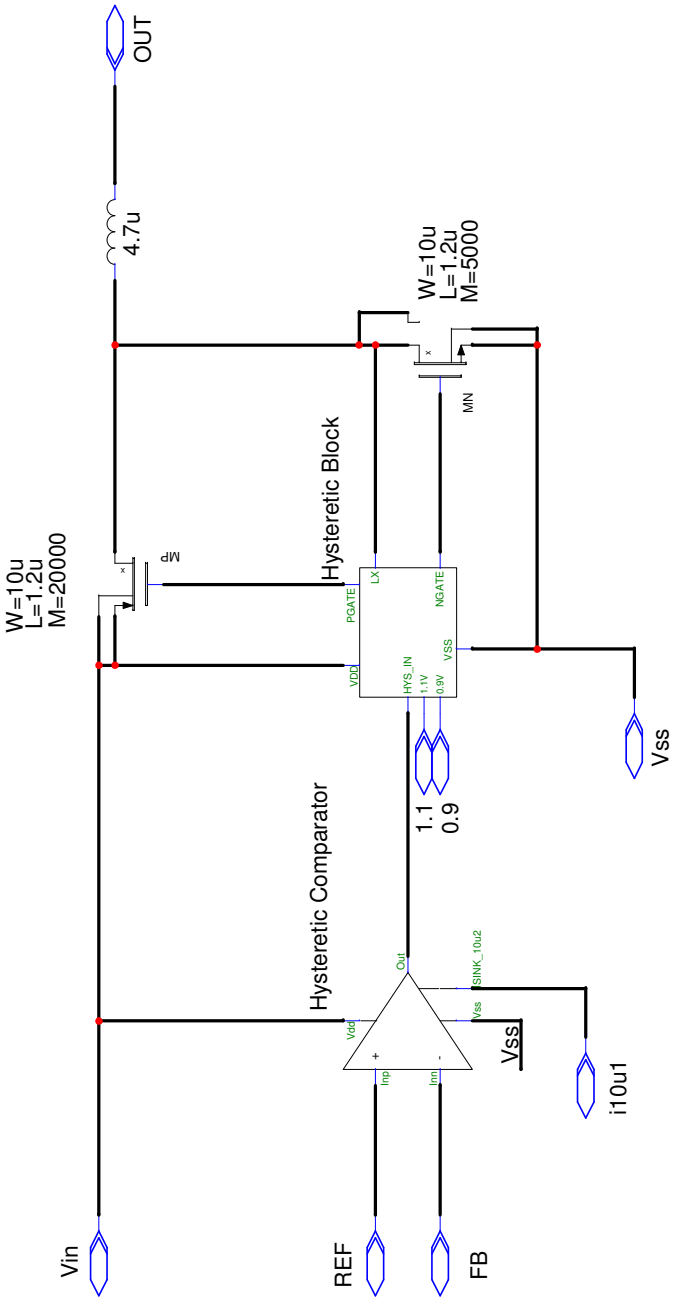


Figure 7.5: Simplified schematic of the hysteretic block

Hysteretic Comparator

The hysteretic comparator monitors the output voltage and compares the sampled voltage to a reference voltage and determines whether or not the PMOS POWER FET should turn on for the next cycle. The schematic of the hysteretic comparator is shown in figure 7.6. The comparator has a built in hysteresis that will be used by to regulate the system. The input stage is composed of the PMOS level shifters, so the input stage can have an input common mode range (ICMR) all the way down to ground. The input differential pair is made up of NPNs that convert the differential input voltage to current, and resistors that convert this current to a voltage load the NPNs. Basically, the signal is amplified by the relationship

$$\frac{V_{out}}{V_{in}} = gm_{NPN} * Resistor \tag{7.1}$$

This voltage is further amplified by the next gain stage to drive the digital logic gates. In order to introduce hysteresis into this comparator, an offset current is injected into the summing nodes of the first stage, and this offset current is converted to an offset voltage (hysteretic voltage), which can be described by the equation

$$V_{Hysteretic} = \frac{I_{offset}}{gm_{npn}} \tag{7.2}$$

The two offset switches control the amount of current and consequently the built in hysteresis of the comparator.

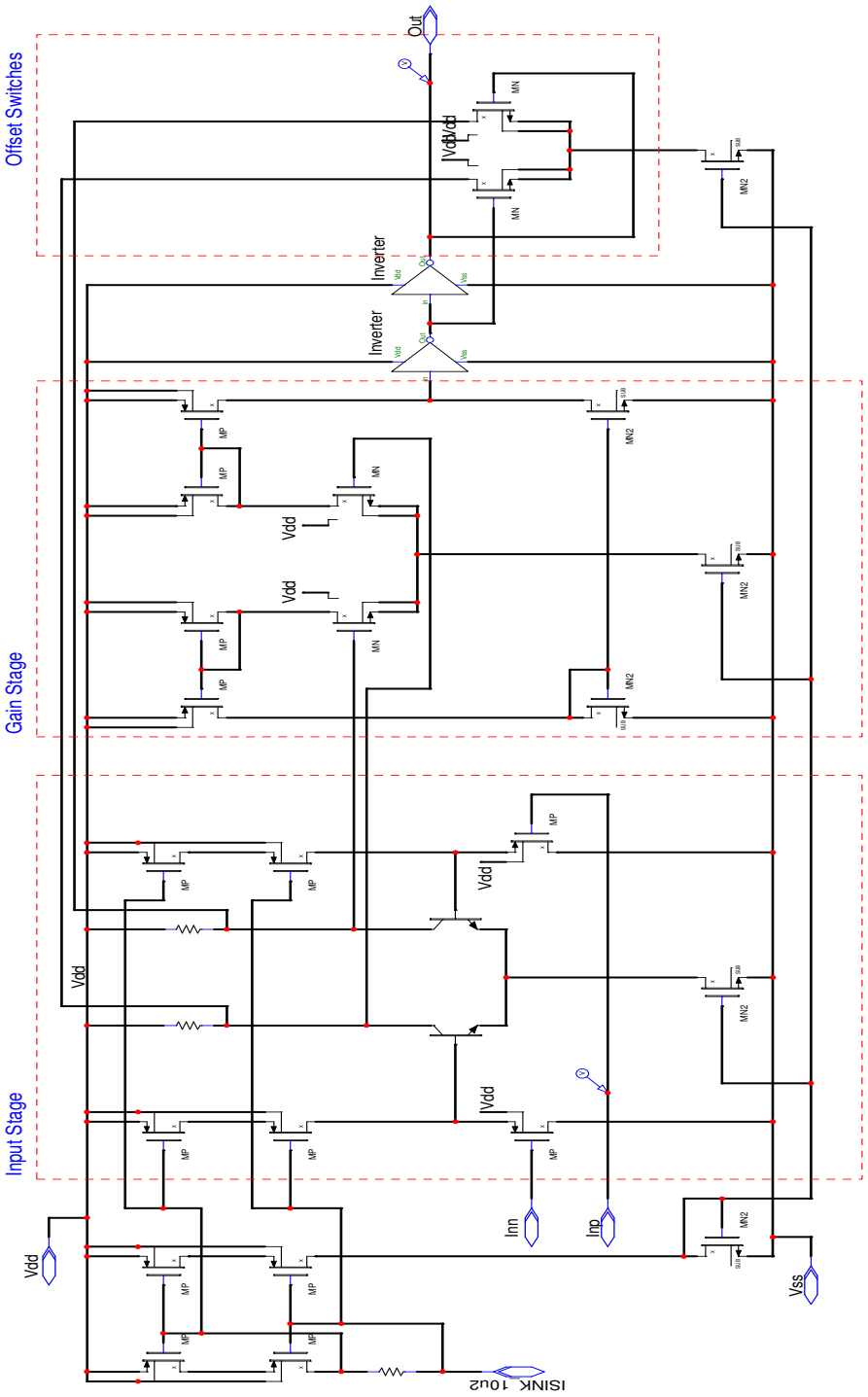


Figure 7.6: Hysteretic comparator

In order to test the hysteresis of the comparator, a test circuit is designed that will be used to measure the hysteresis. A simplified schematic of this circuit is shown in figure 7.7.

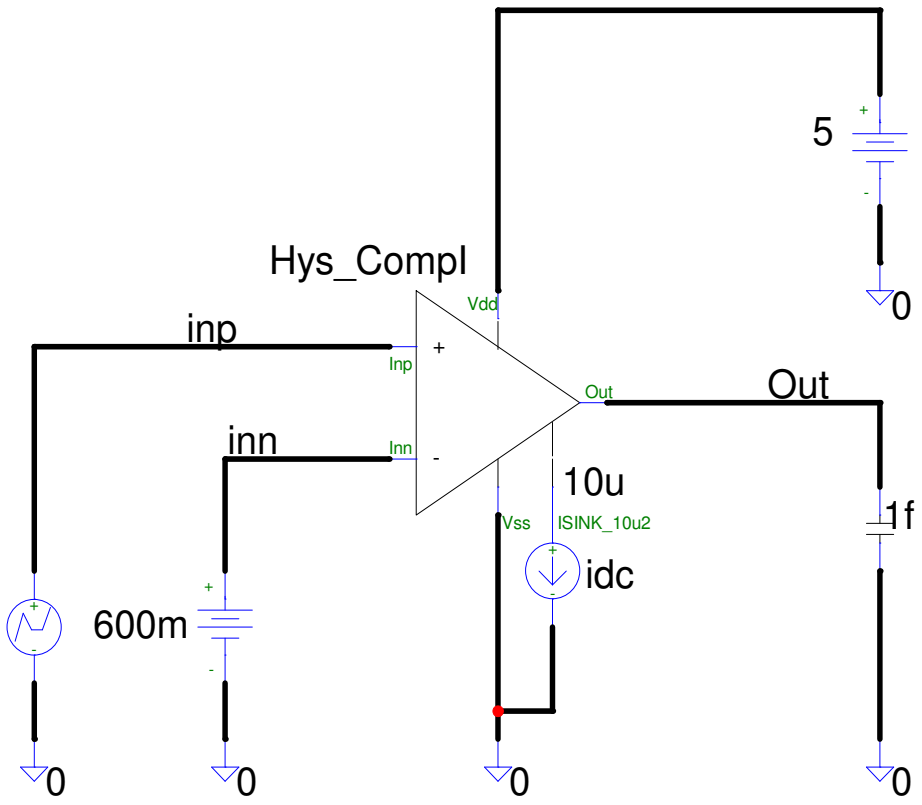


Figure 7.7: A test circuit to measure the hysteresis

The comparator is powered up and biased at the right conditions, with a 600mV reference at its inverting input. The voltage at the non-inverting input is ramped up linearly from 500mV to 700mV, and then it is ramped down linearly from 700mV to 500mV. The voltage at the output is monitored and it is sketched vs. the non-inverting input, and in figure 7.8, the intended waveform is drawn. The waveform of figure 7.8 shows that the amount of hysteresis that is built in the comparator.

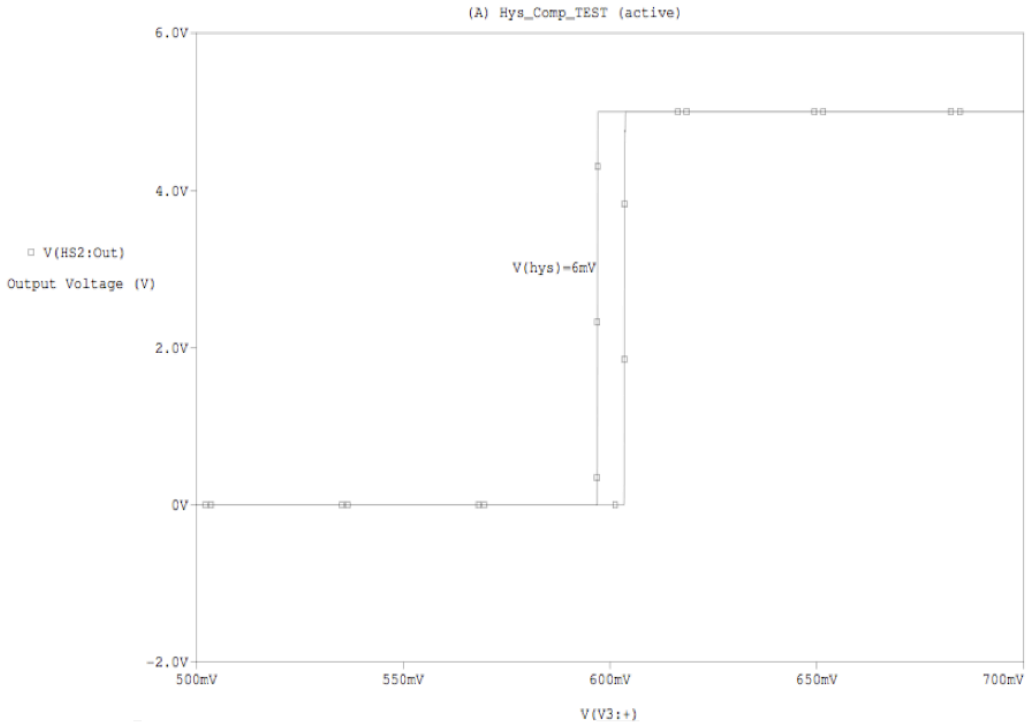


Figure 7.8: The hysteretic window of the hysteretic comparator

High-side Current Sense Amplifier

The high-side current sense amplifier measures the current that is passing through the high-side switch by the voltage that is created as the inductor current is converted to a voltage by passing through the resistance of the high-side switch. This voltage is amplified and made available to the current limit comparator. Figure 7.9 shows the simplified block diagram of a current sense amplifier and how it works. The current sense amplifier can be described with the following set of equations:

$$V_{diff} = R1 * ILOAD \tag{7.3}$$

$$ILOAD * R1 = IOUT * R3 \tag{7.4}$$

$$VOUT = IOUT * R4 \tag{7.5}$$

$$VOUT = \frac{R1*R4}{R3} ILOAD \tag{7.6}$$

Basically, the ILOAD is sensed and amplified by the gain factor shown in equation. The information signal VOUT is used by the system to do what is necessary such as current limiting, signal processing, or etc.

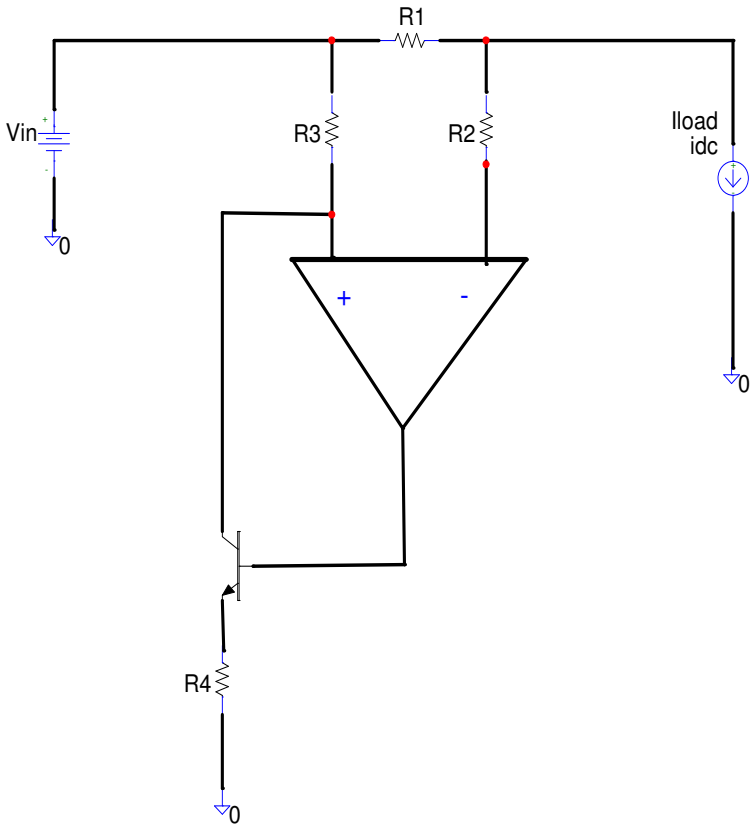


Figure 7.9: Simplified block diagram of a current sense amplifier

In figure 7.10, the detailed schematic of current sense amplifier is shown. Transistors Q1-Q6 form the input stage of the amplifier. The input stage is loaded by the current mirror Q7 and Q8. Transistors Q10 and Q11 form a current mirror which supply the bias current to the current sense amplifier.

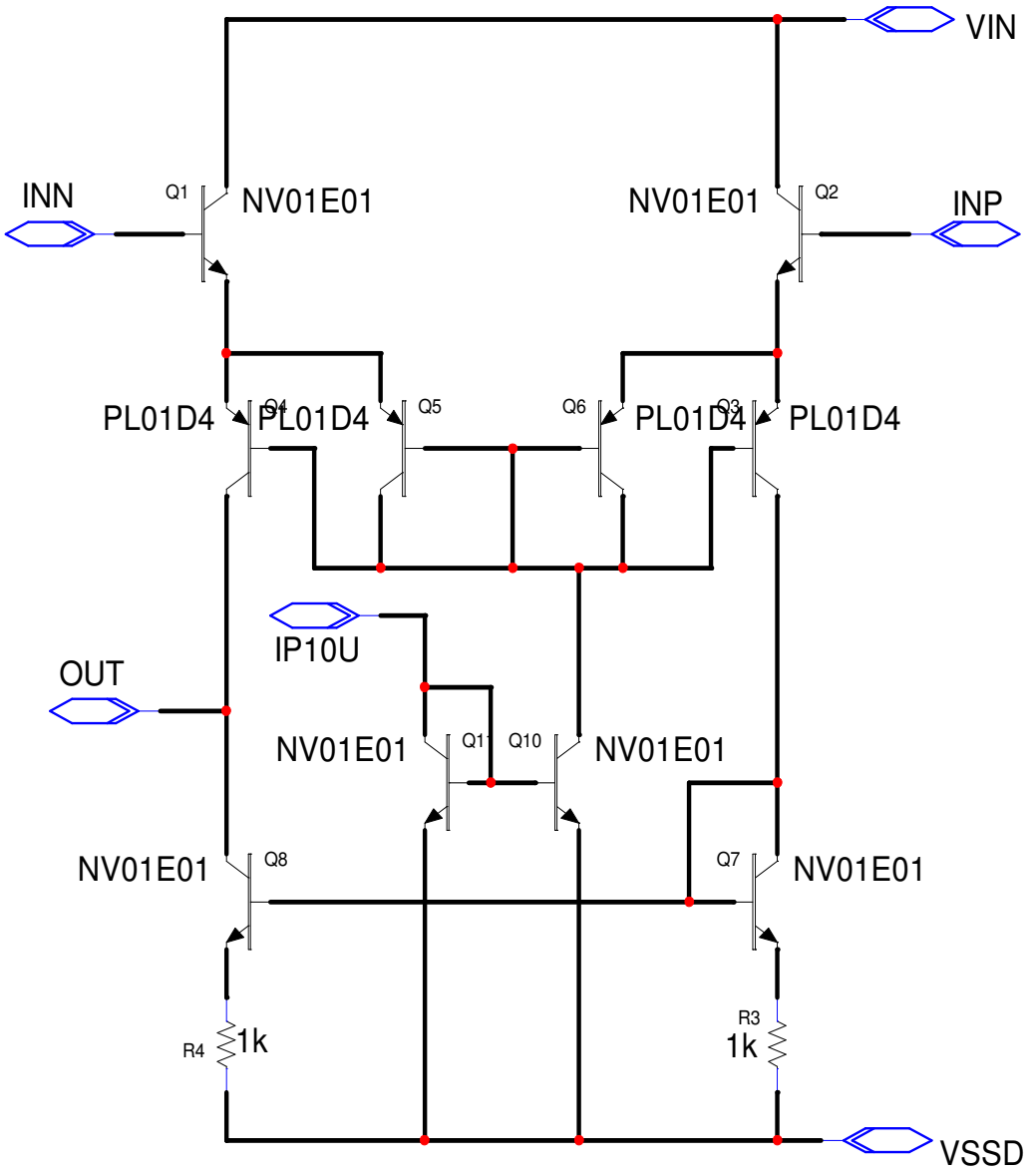


Figure 7.10: High-side current sense amplifier

In order to test the high side current sense amplifier, the test circuit in figure 7.11 is set up. A load current is run through a resistor and by the actions of negative feedback, the high side current sense amplifier will create an output voltage. By following the design equations above, the output voltage can be calculated to be

$$VOUT = \frac{0.1\Omega * 10000\Omega}{2000\Omega} * 1Amp = 500mV \quad (7.7)$$

The waveform on figure 7.12 shows that the calculated value matches up, precisely, with the simulated value.

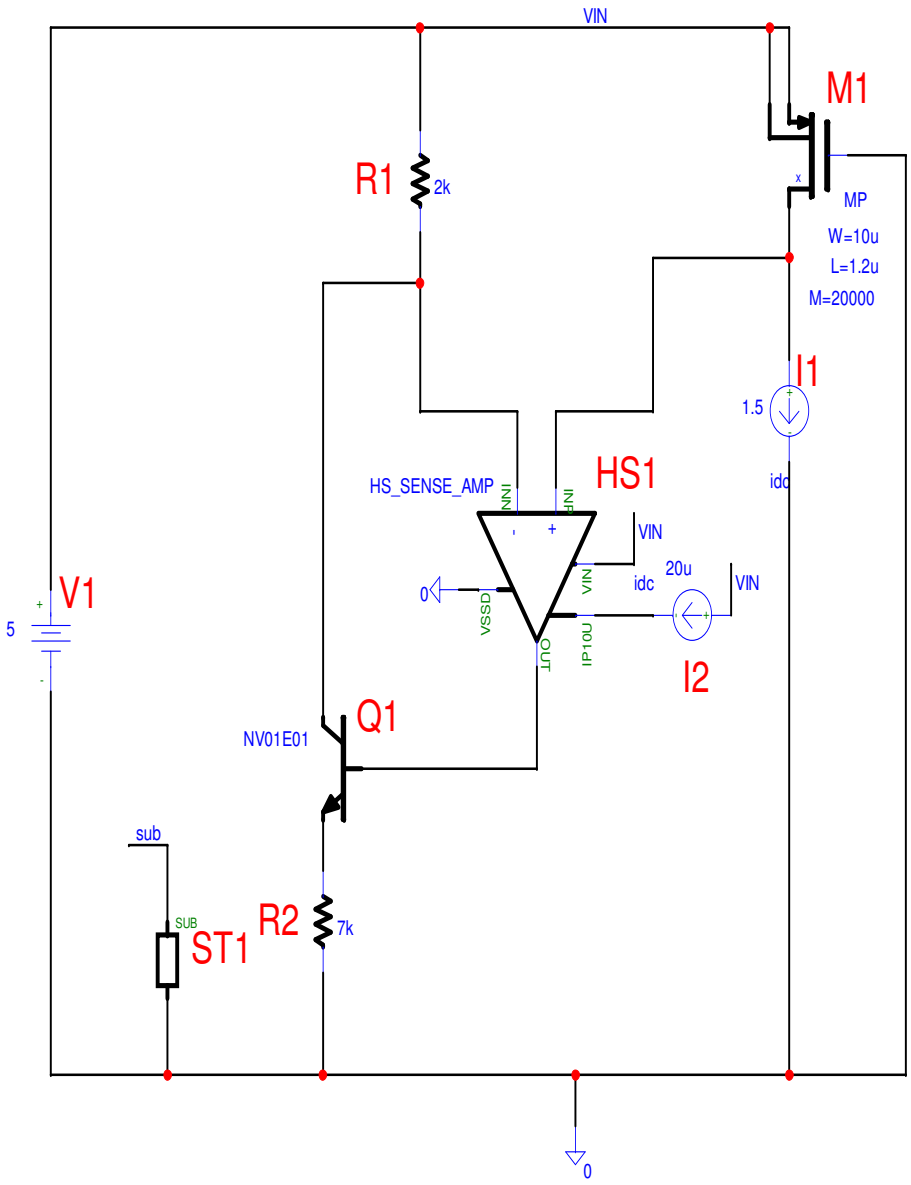


Figure 7.11: Test circuit for the current sense amplifier

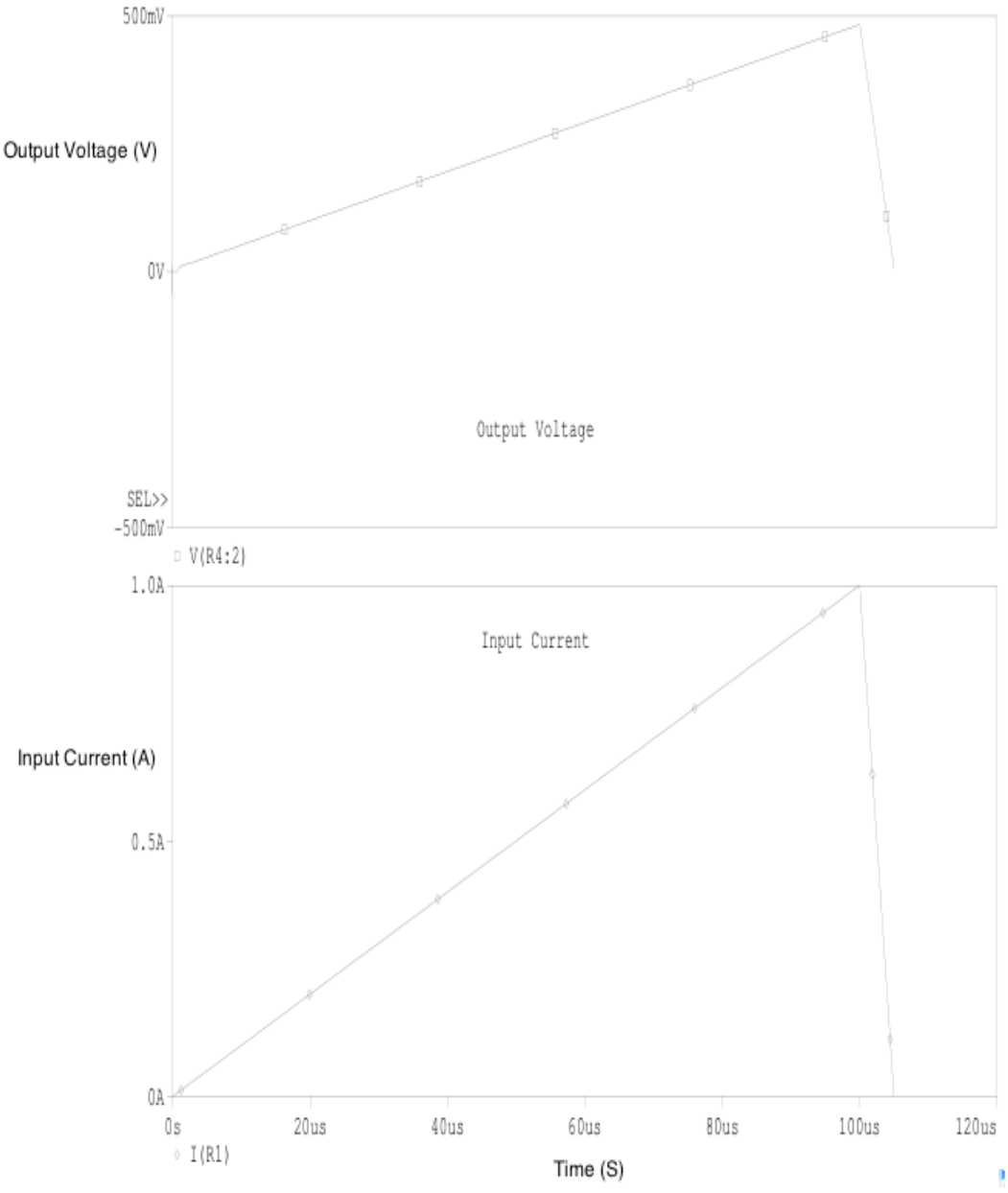


Figure 7.12: The waveforms for the current sense amplifier

Current Limit Comparator with Hysteresis

This comparator will use the signal from the high-side current sense amplifier to turn off the high-side switch for a predetermined inductor current threshold.

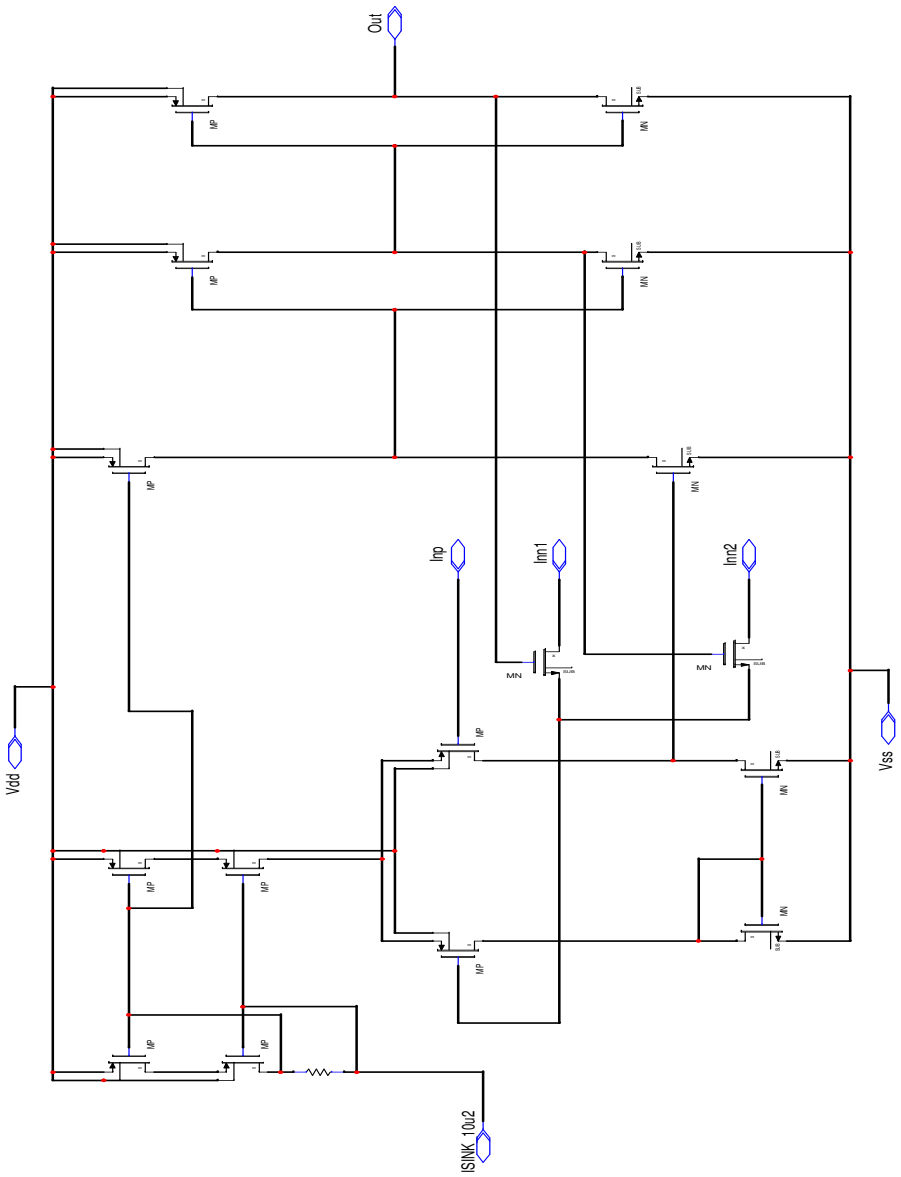


Figure 7.13: Current limit comparator with hysteresis

Low-Side Zero Crossing Amplifier

After the high-side switch is turned off the inductor current will ramp down through the low-side switch. The switch will remain open until the inductor current has reached the zero current thresholds. This amplifier will detect the zero crossing point and turn off the low-side switch. The zero crossing amplifier is composed of two amplifiers that monitor the threshold voltage differentially which are more accurate and less prone to noise generated signals. Since there are two amplifiers that reinforce each other, the gain of the overall system is doubled. Each amplifier has the transconductance (g_m), and then the signal is amplified by the following relation:

$$V_{out} = I_{out} * R_{POWER_{SWITCH}} * \left(gm_{AMP_1} + gm_{AMP_2}\right) * (R_{ds\_M4} || R_{dS\_M2}) \quad (7.8)$$

where gm_{AMP1} and gm_{AMP2} is the transconductance of amplifier 1 and 2,

R_{ds_M4} and R_{ds_M2} is the drain to source small signal resistance of transistor M4 and M2, and

$R_{POWER\text{-}Switch}$ is the resistance of the NMOS power transistor in the hysteretic converter.

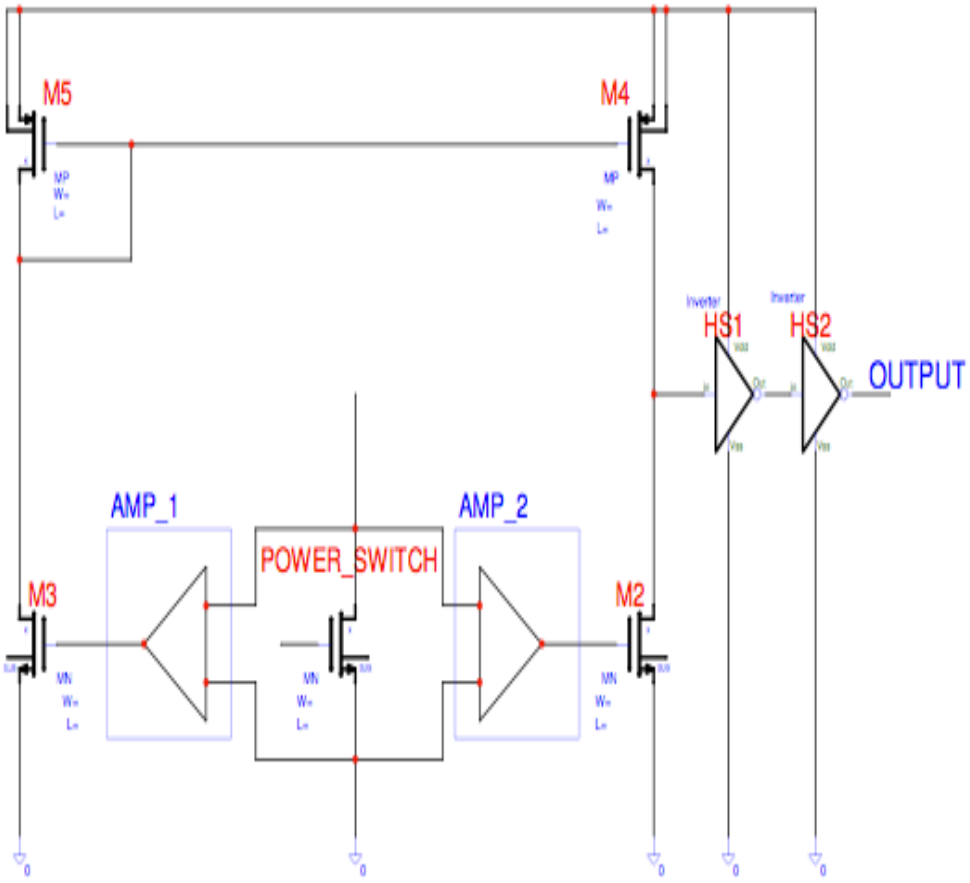


Figure 7.14: Block diagram of zero crossing amplifier

The V_{out} should be big enough to drive the two-stage inverter; otherwise another gain stage must be inserted before the inverter chain. Figure 7.15 shows the detailed schematic of zero crossing amplifier. Transistors Q4, Q5, and Q6 make up Amp_1. The second amplifier is composed of transistors Q1, Q2, and Q3. Current mirrors M23, M24, M26, M25, M22, and M21 form the gain stages of the zero crossing amplifier.

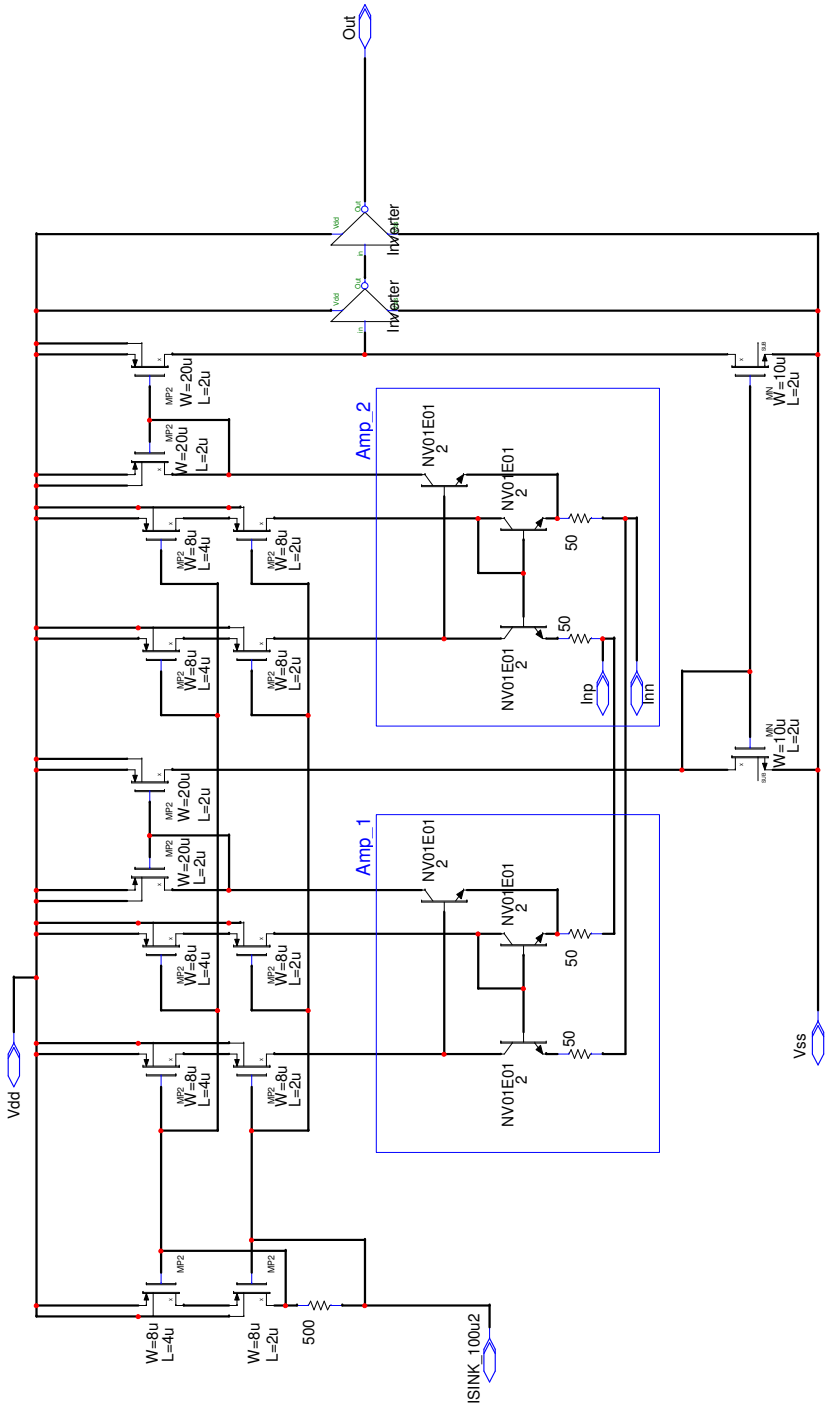


Figure 7.15: Low-side zero crossing amplifier

In order to check the performance of the zero crossing amplifier, a test circuit was set up and is shown in figure 7.16. The inputs of the amplifier are connected across a resistor R1, which represents the drain to source resistance of a power MOSFET. A current, which has the shape of a saw-tooth, is run through the resistor. As the waveform in figure 7.17 shows, the zero crossing amplifier reacts sharply, when the voltage across the resistor is at zero.

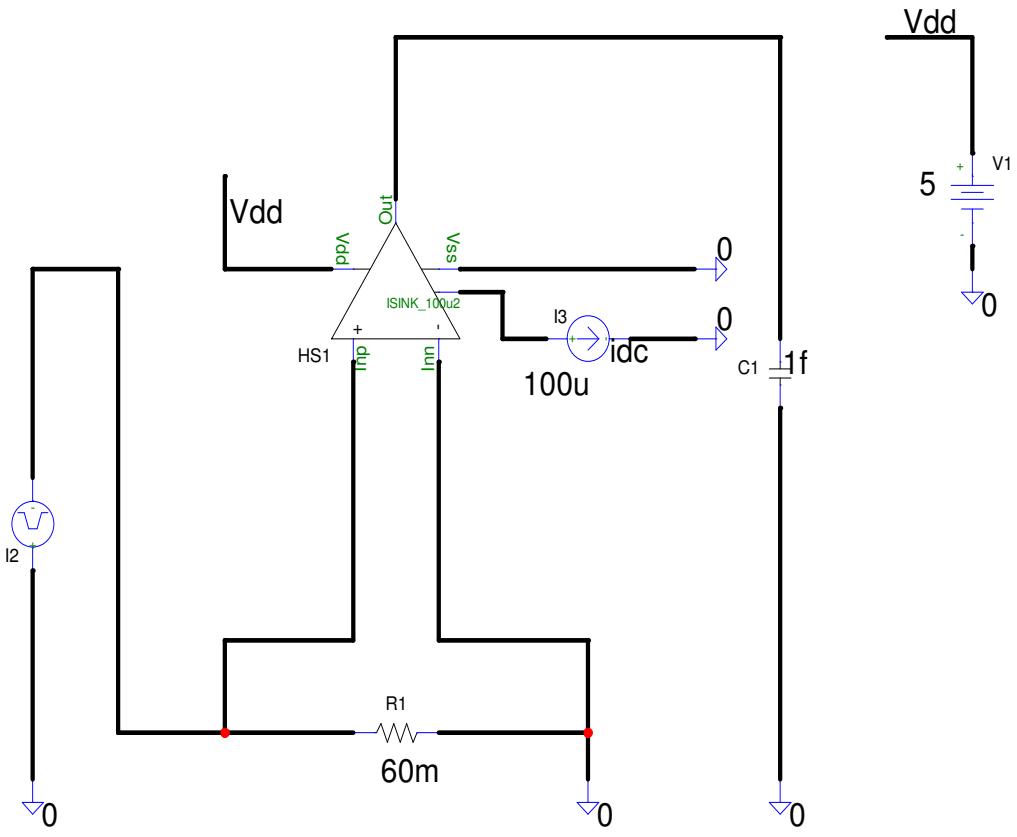


Figure 7.16: Test set up for zero crossing amplifier

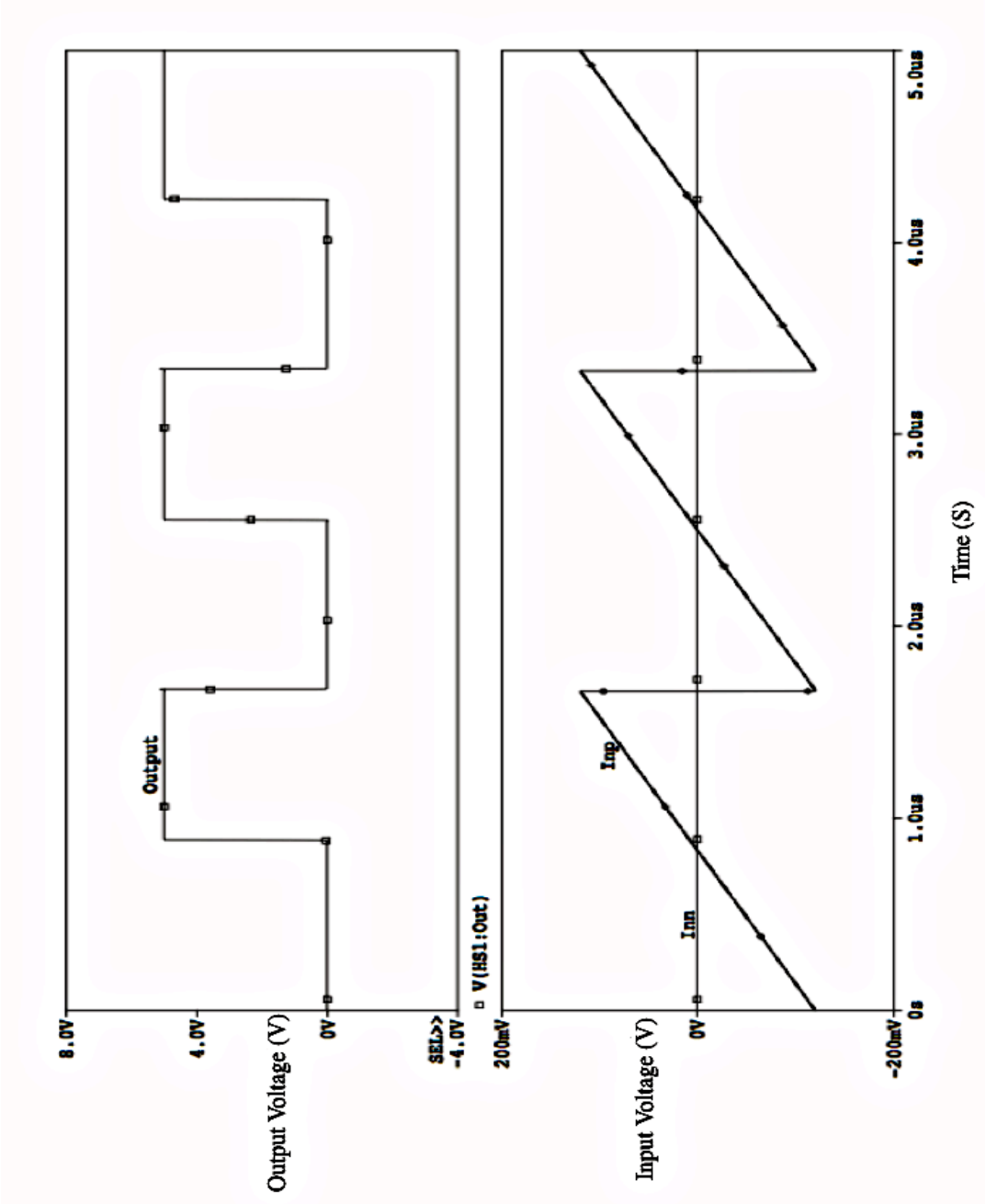


Figure 7.17: Waveform of the Zero-Crossing amplifier performance

NMOS and PMOS Power Switches

The high-side switch is made up of large number of PMOS FETs that are group together to create a switch with 60mΩ of resistance. The low-side switch is made up large number of unit size NMOS FETs.

NMOS and PMOS Drivers

The NMOS and PMOS drivers are just chains of inverters that are sized in a way to drive the big power switches. The schematic of the PMOS and NMOS Drivers is shown in figure 7.18.

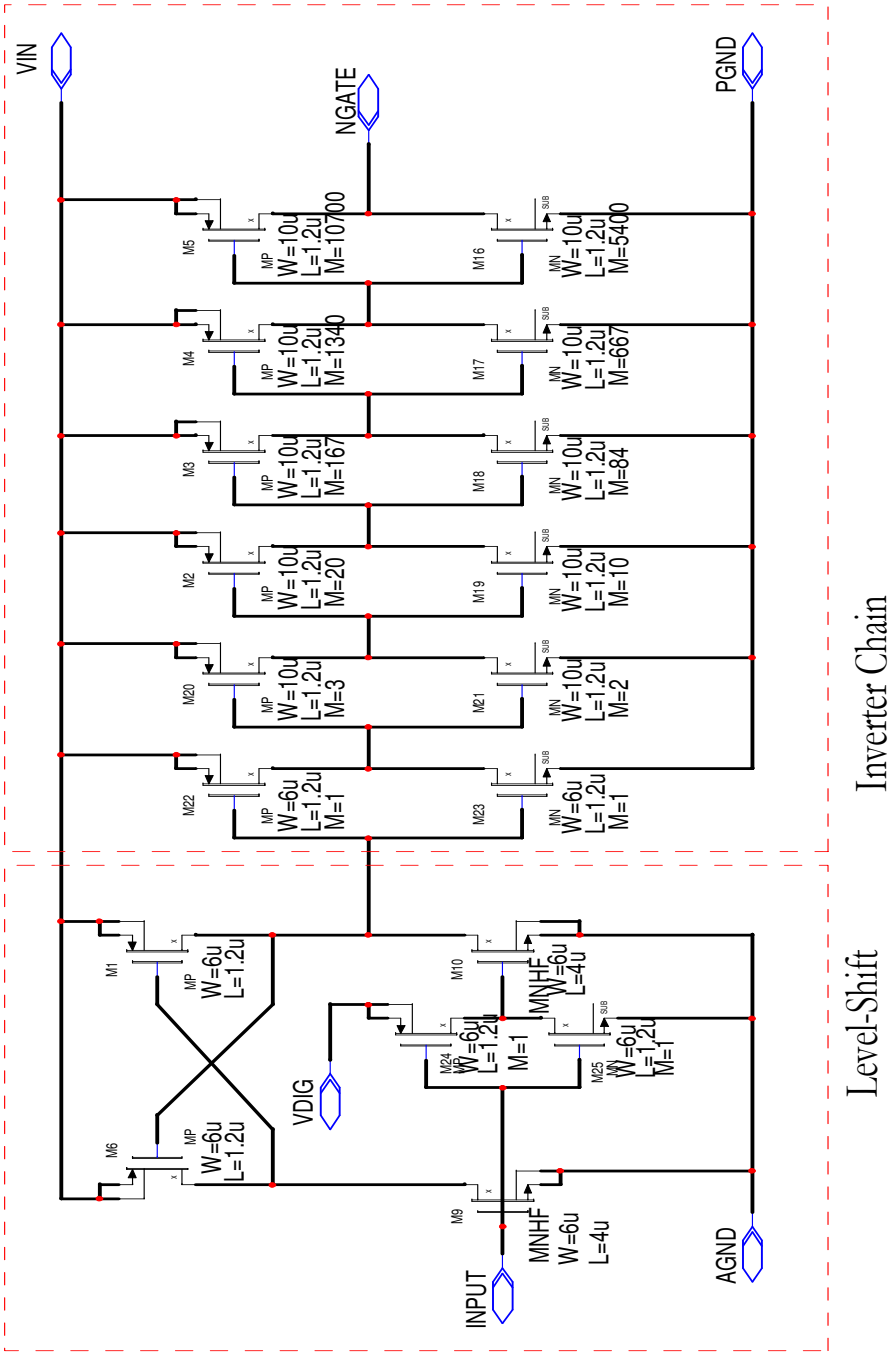


Figure 7.18: Schematic of PMOS and NMOS drivers

The Bandgap Complex

The bandgap complex is used to create an ultra stable reference voltage to the voltage-to-current converter that supplies the current to the magnetic lenses. This complex is made up of three blocks that are:

- Secondary bandgap
- Amplifier
- Primary bandgap

Figure 7.19, shows the simplified block diagram of the bandgap complex. This complex is composed of three blocks that are the primary bandgap, the amplifier, and the secondary bandgap. The Secondary bandgap provides all the reference voltages and the bias current to all other blocks, except the reference voltage to the current regulator. The amplifier, which acts as the supply voltage to the primary bandgap, amplifies the reference voltage and provides an ultra stable voltage supply to the primary bandgap. The power supply rejection ration (PSRR) of the amplifier attenuates all disturbances on the supply lines, so the primary bandgap has more immunity to the disturbances.

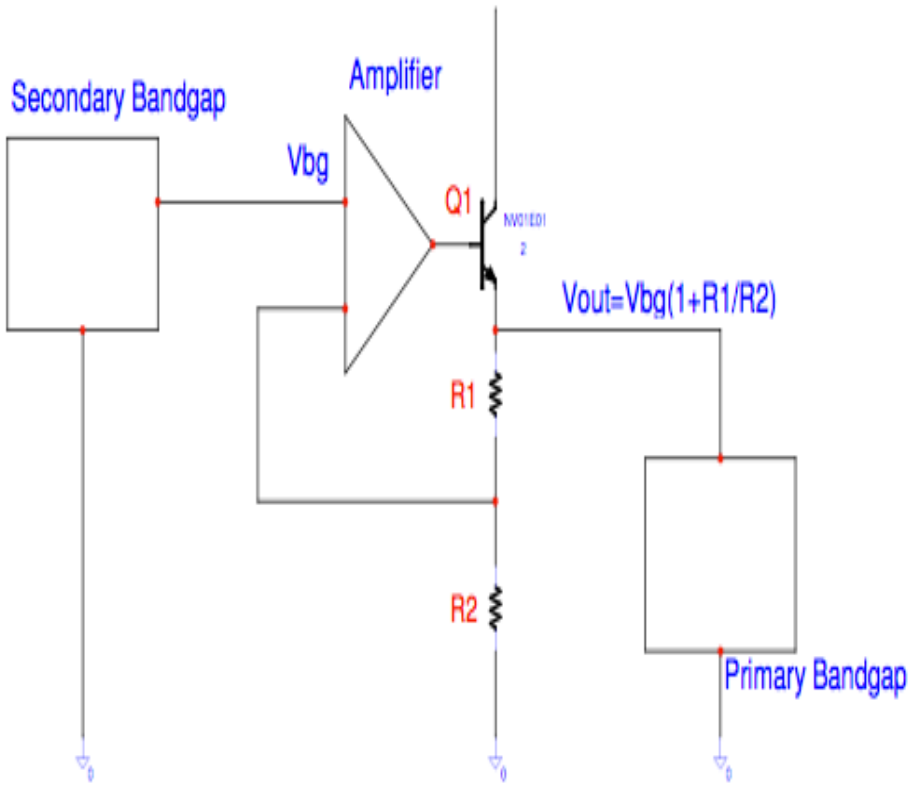


Figure 7.19: A simplified block diagram of the bandgap complex

The real bandgap complex is as shown in figure 7.20, and the waveforms of this complex are shown in figure 7.21.

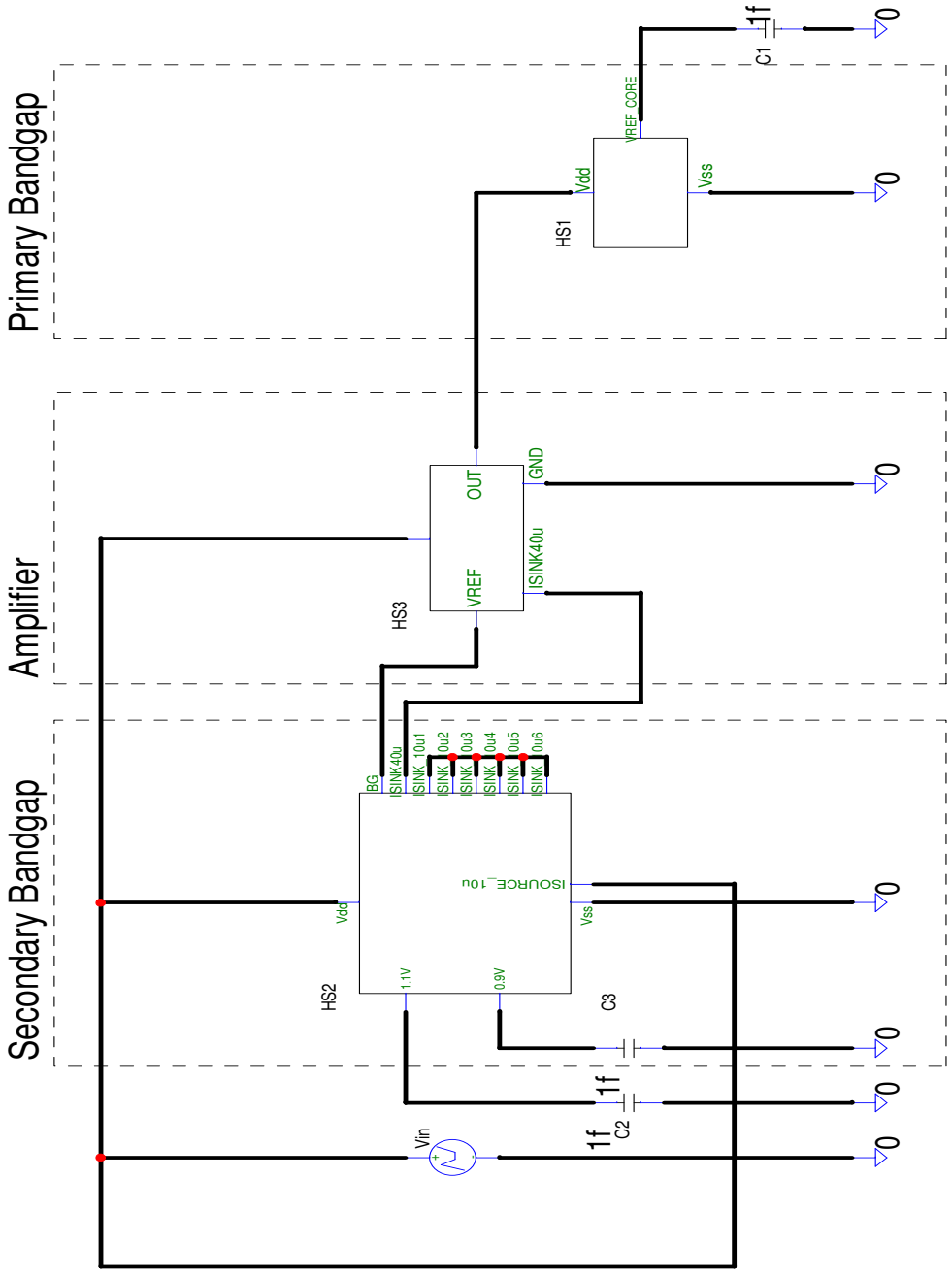


Figure 7.20: The real schematic of the bandgap complex

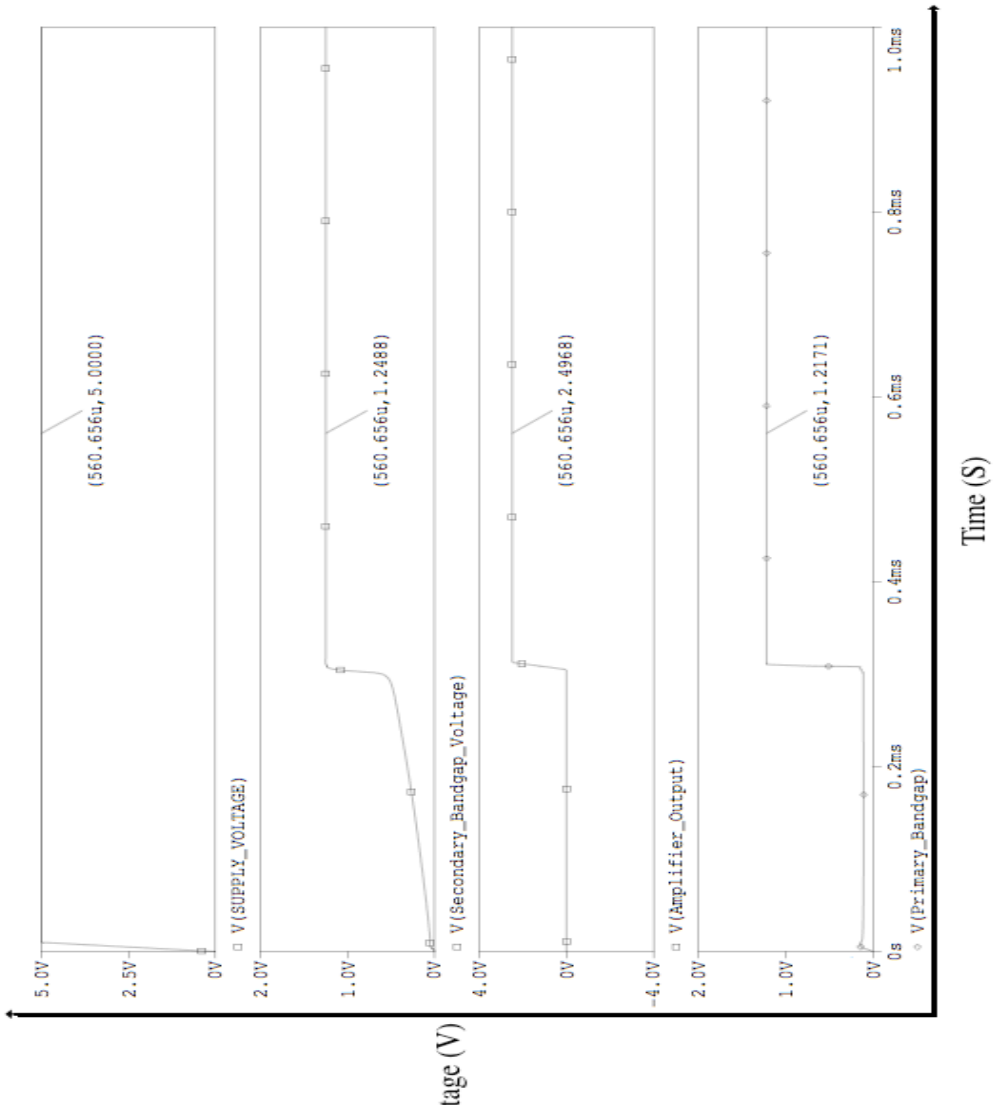


Figure 7.21: Waveforms of the bias circuitry

Secondary Bandgap

The secondary bandgap and bias circuitry will supply all the reference voltages and bias currents to all the blocks except the reference voltage for the current regulator. Figure 7.22, shows the detailed schematic of the secondary bandgap and bias circuitry. This bandgap is a typical bandgap that creates stable reference voltages and currents. The bandgap's performance can be described by the following design equations:

$$V_T ln \frac{I_{CQ1}}{I_{sQ1}} - V_T ln \frac{I_{CQ2}}{I_{sQ2}} - IR_{17} = 0$$

$$I = \frac{V_T ln8}{I_{R17}}$$

$$V_{OUT} = V_{be} + \frac{R_{18}}{R_{17}} * 2 * V_T ln8 \qquad (7.9)$$

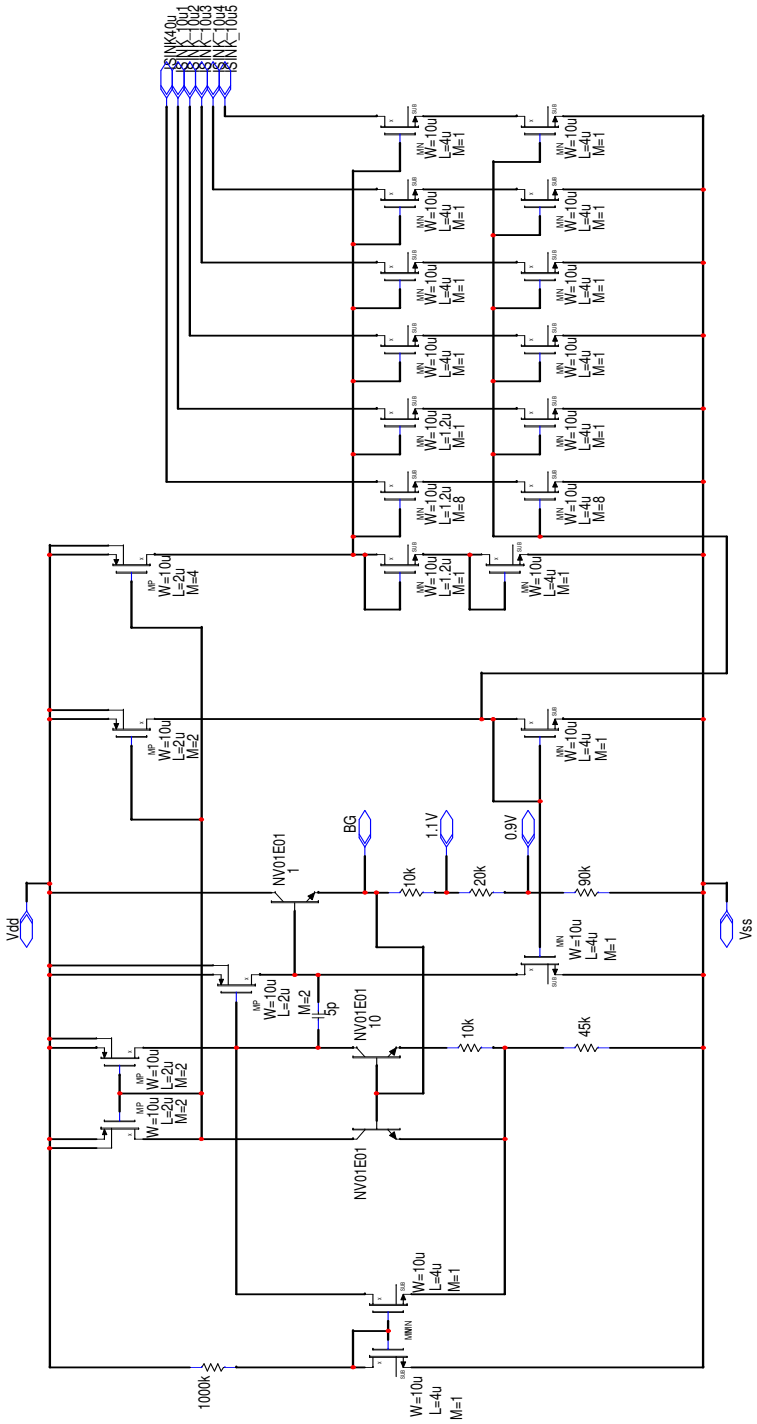


Figure 7.22: Schematic of secondary bandgap and bias circuitry

Also, the bias current can be described by the following equation:

$$I_{bias} = \frac{V_{BG} - V_{be}}{R19 + R37 + R36} \quad (7.10)$$

where V_{BG} is the bandgap voltage, and

V_{be} is the base-emitter voltage.

The bandgap voltage vs. temperature is plotted in Figure 7.23. As the figure shows, the bandgap shows respectable stability over a long range in temperature. Also, transistors Q3, Q5, R14, and R13 form the start up circuitry so that the bandgap always starts up.

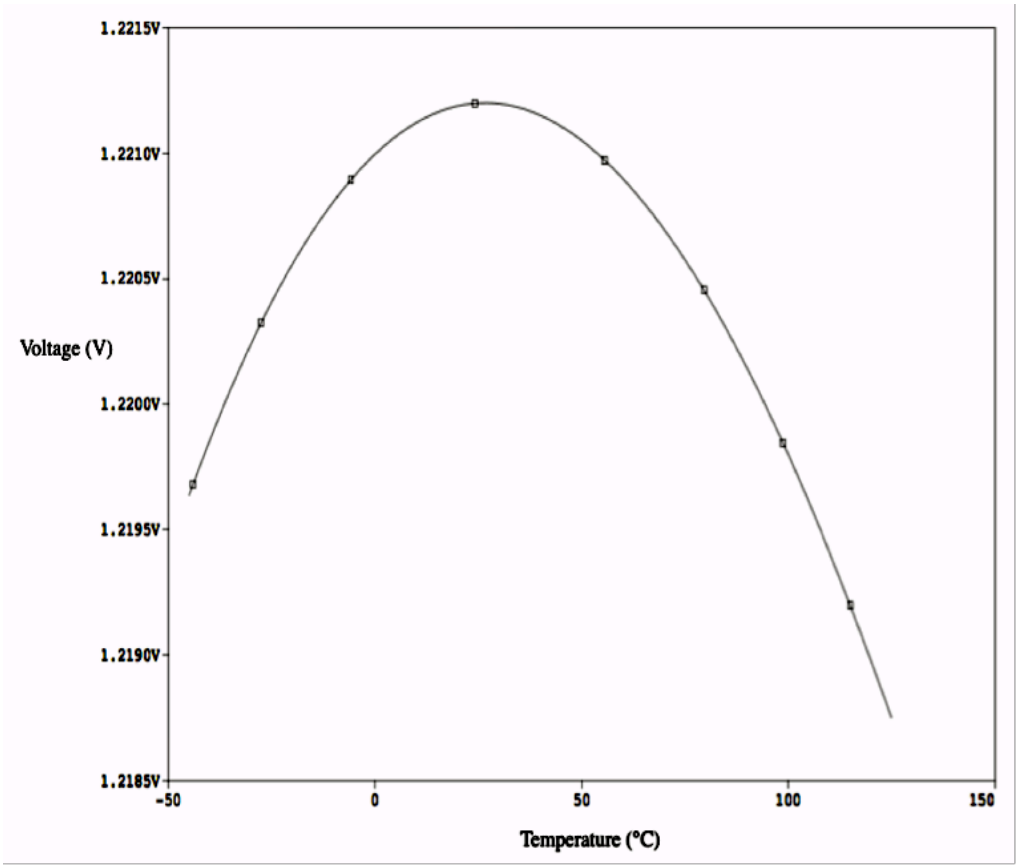


Figure 7.23: Secondary bandgap's reference voltage vs. temperature

The purpose of the secondary bandgap is to create the reference voltage and bias current for all other blocks and it is used as a reference to an amplifier that supplies the voltage to primary bandgap. The block diagram of

this complex is shown in figure 7.19. Due to the ultimate stability requirements of the current source, the reference voltage that provides the reference voltage to current regulator must not see variations in its supply voltage. The secondary bandgap comes up first; which provides the reference to the amplifier that supplies the primary bandgap. The secondary bangap is a first order circuit and the primary bandgap is a second order one.

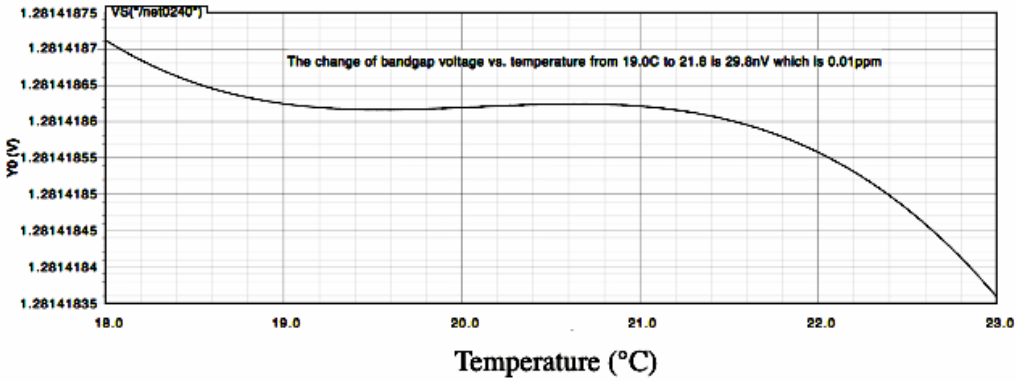


Figure 7.24: Zoomed in primary bandgap voltage vs. temperature

The Amplifier

The sole purpose of the amplifier is to provide an extremely stable, low output impedance voltage supply to the primary bandgap. The ultra stability of the current that is to be produced requires a really stable reference voltage. Bandgaps and analog circuitries are susceptible to the integrity of their supply voltages. All the noise and disturbances must be filtered out as much as possible so they do not jeopardize the integrity of the system. In addition, the ability of systems to filter out the noise worsens as frequency is increased. For these reasons, the amplifier is used to filter out the noise as much as possible. Figure 7.25 shows the schematic of the amplifier in this architecture. The amplifier is mainly composed of bipolar transistors to

achieve as much gain as possible with fewer numbers of gains stages. Transistors Q1 and Q2 form the input stage of this amplifier. They form the differential pair that converts the differential voltage to a current. Transistors Q12, Q11, Q14, Q13, Q7, Q8 and resistors R1 and R2 form the gain block of this amplifier. The source follower Q9 is used to create low output impedance and buffer the gain stage from the being loaded by the primary bandgap. Also, Figure 7.26 shows the output voltage of the amplifier as the function of Temperature. Notice that output voltage is 2.5V, which is the double that of the bandgap voltage, which is 1.25V.

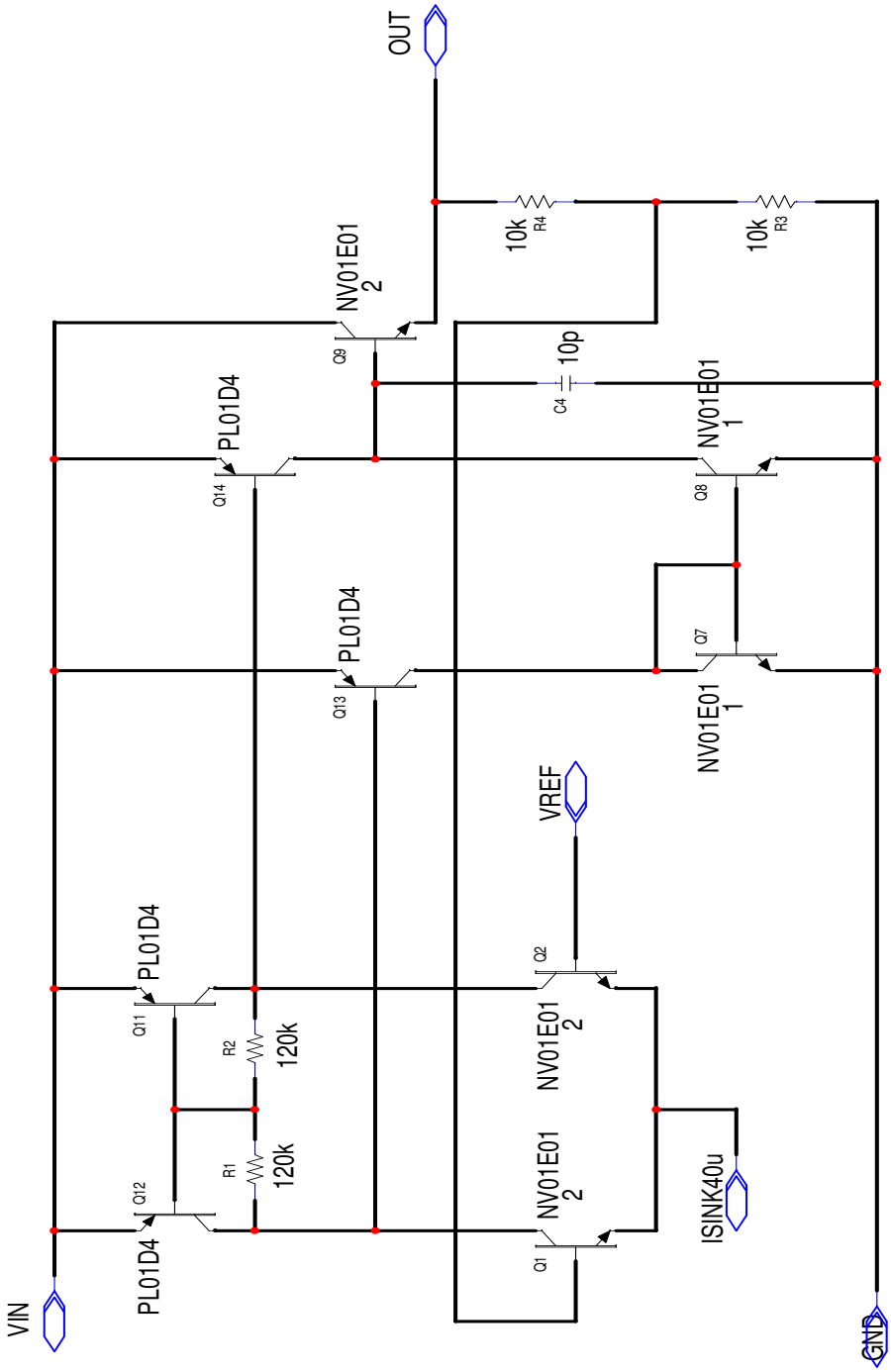


Figure 7.25: Schematic of amplifier

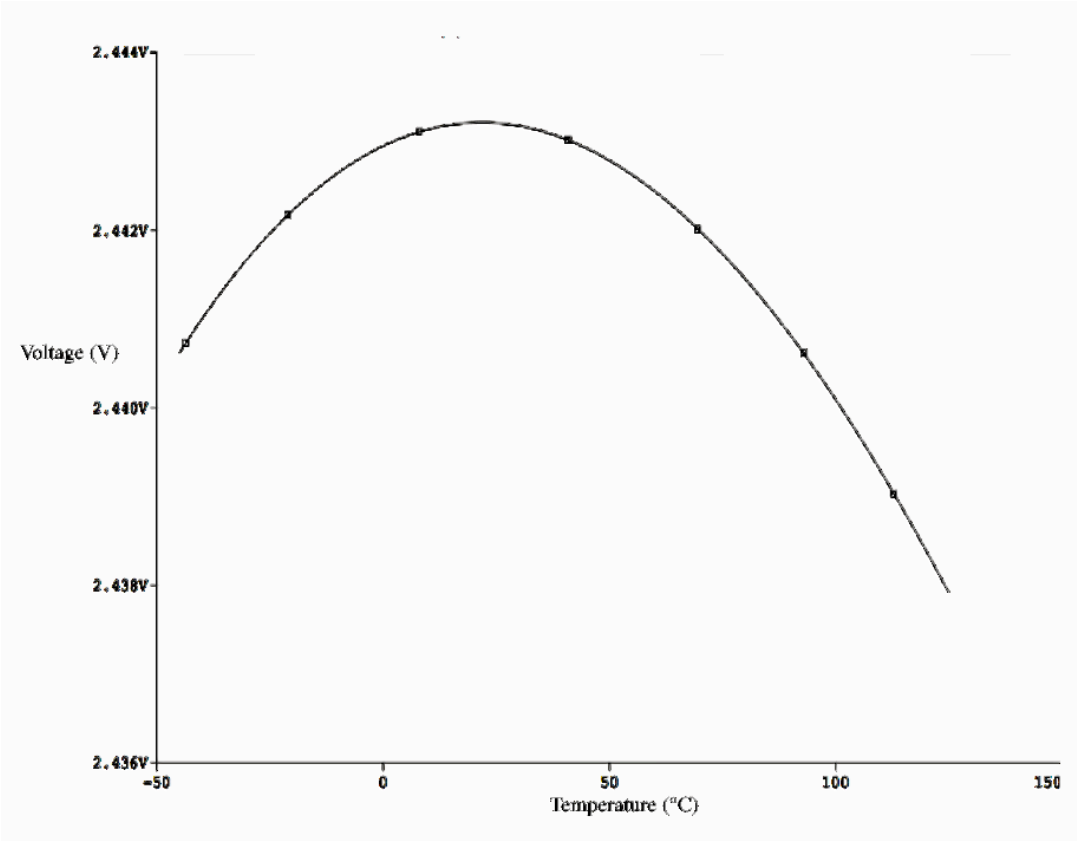


Figure 7.26: The output voltage of the amplifier vs. temperature

Primary Bandgap

The primary bandgap creates a stable reference voltage to the current regulator, which in turn is converted to a current.

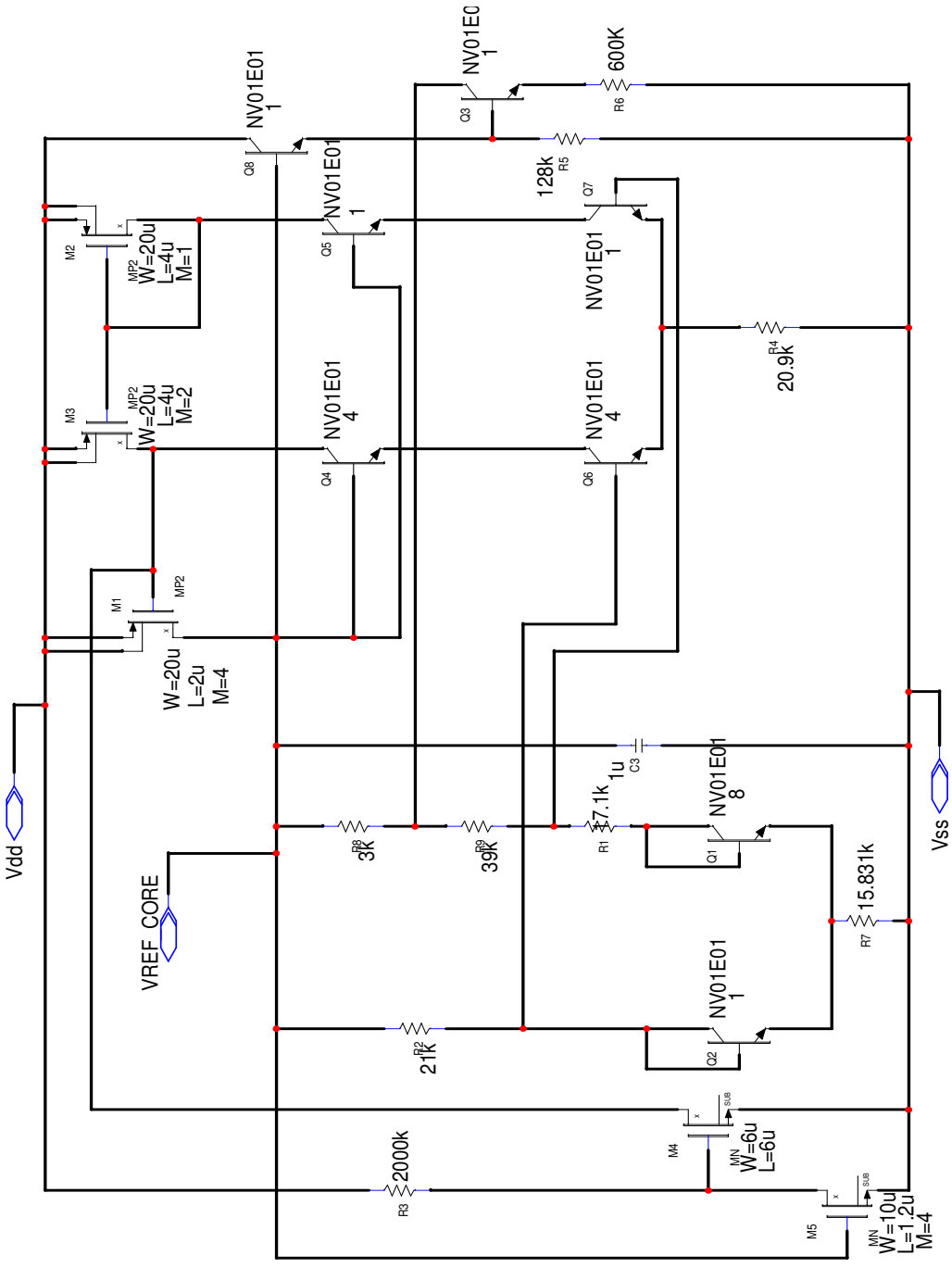


Figure 7.27: Schematic of primary bandgap

Filter

An LC filter is placed after the hysteretic regulator to block the passage of higher frequency ripples to the analog circuitry. This is a second order passive low pass filter that has the second order pole at

$$Pole = \frac{1}{2\pi\sqrt{LC}} = 30\ KHz \qquad (7.11)$$

Figure 7.28 shows the schematic of the LC filter that is only composed of an inductor and a capacitor.

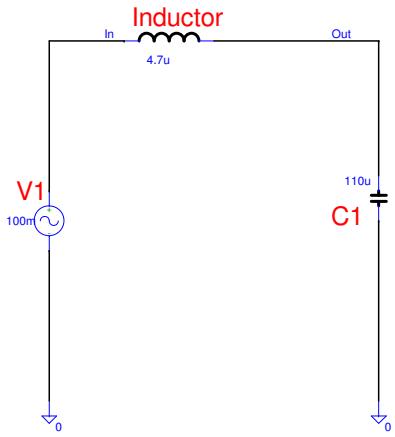


Figure 7.28: Schematic of the passive low pass filter

Linear Regulator

A linear regulator is placed after the LC filter and before the magnet load. The purpose of this linear regulator is to further filter the low frequency ripples and create a stable voltage. The detailed schematic of this linear regulator is shown in figure 7.29. The schematic of linear regulator and hysteretic regulator is shown on figure 7.30.

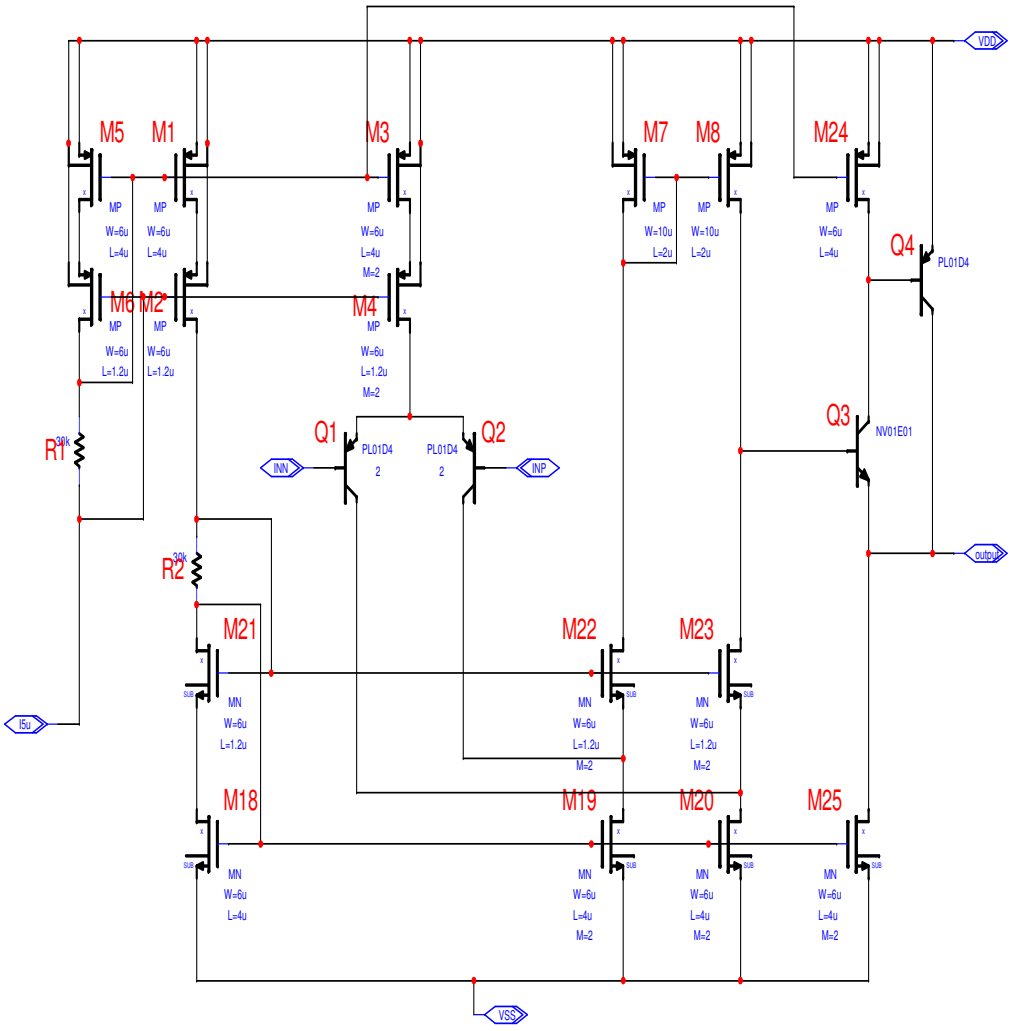


Figure 7.29: Schematic of linear regulator

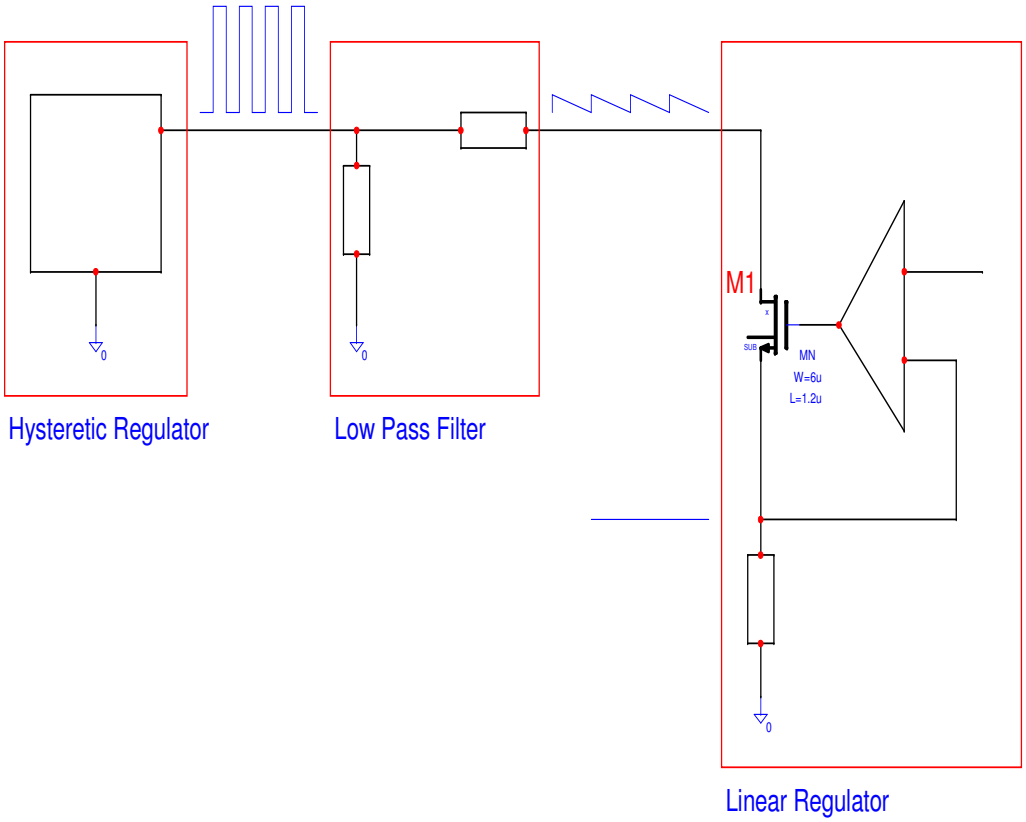


Figure 7.30: Block diagram of hysteretic regulator, low pass filter, and linear regulator

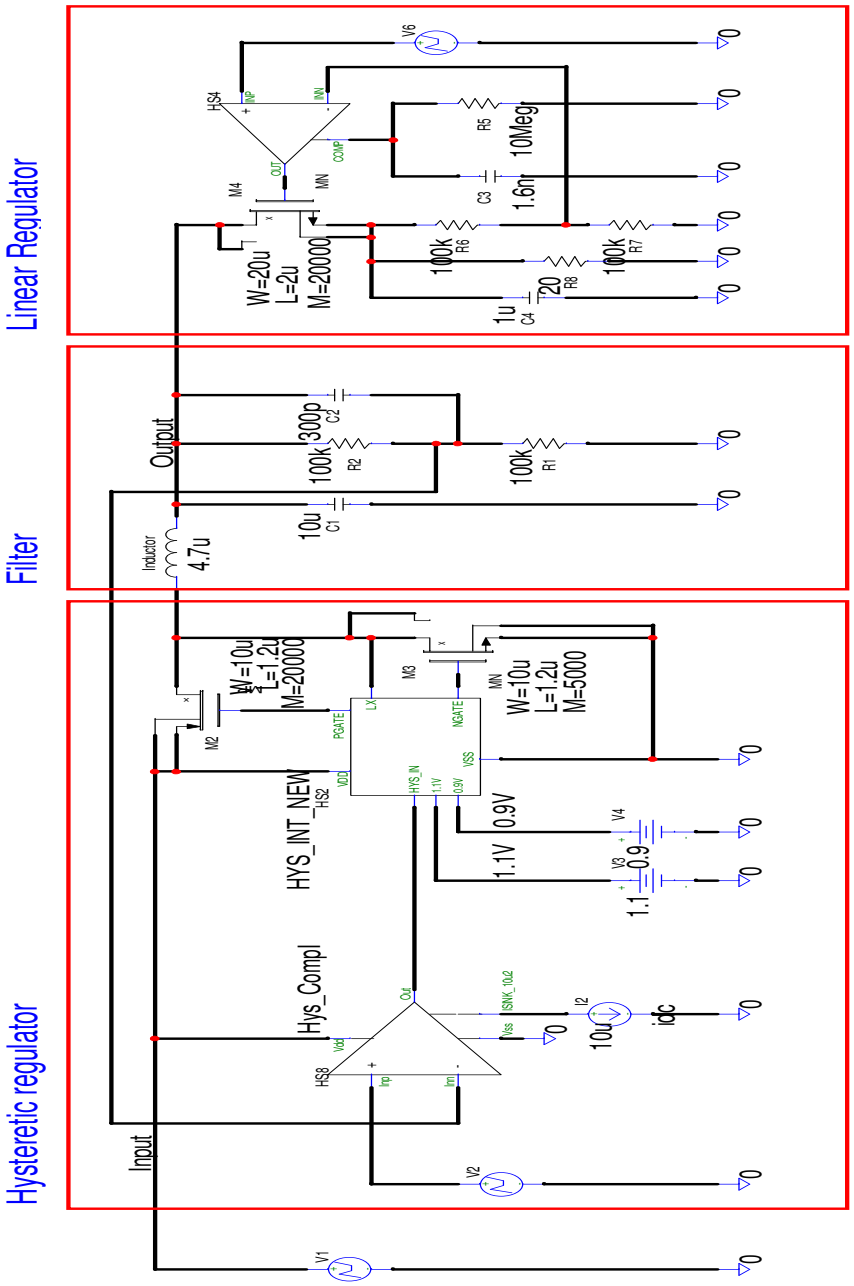


Figure 7.31: Schematic of hysteretic regulator, low pass filter and linear regulator

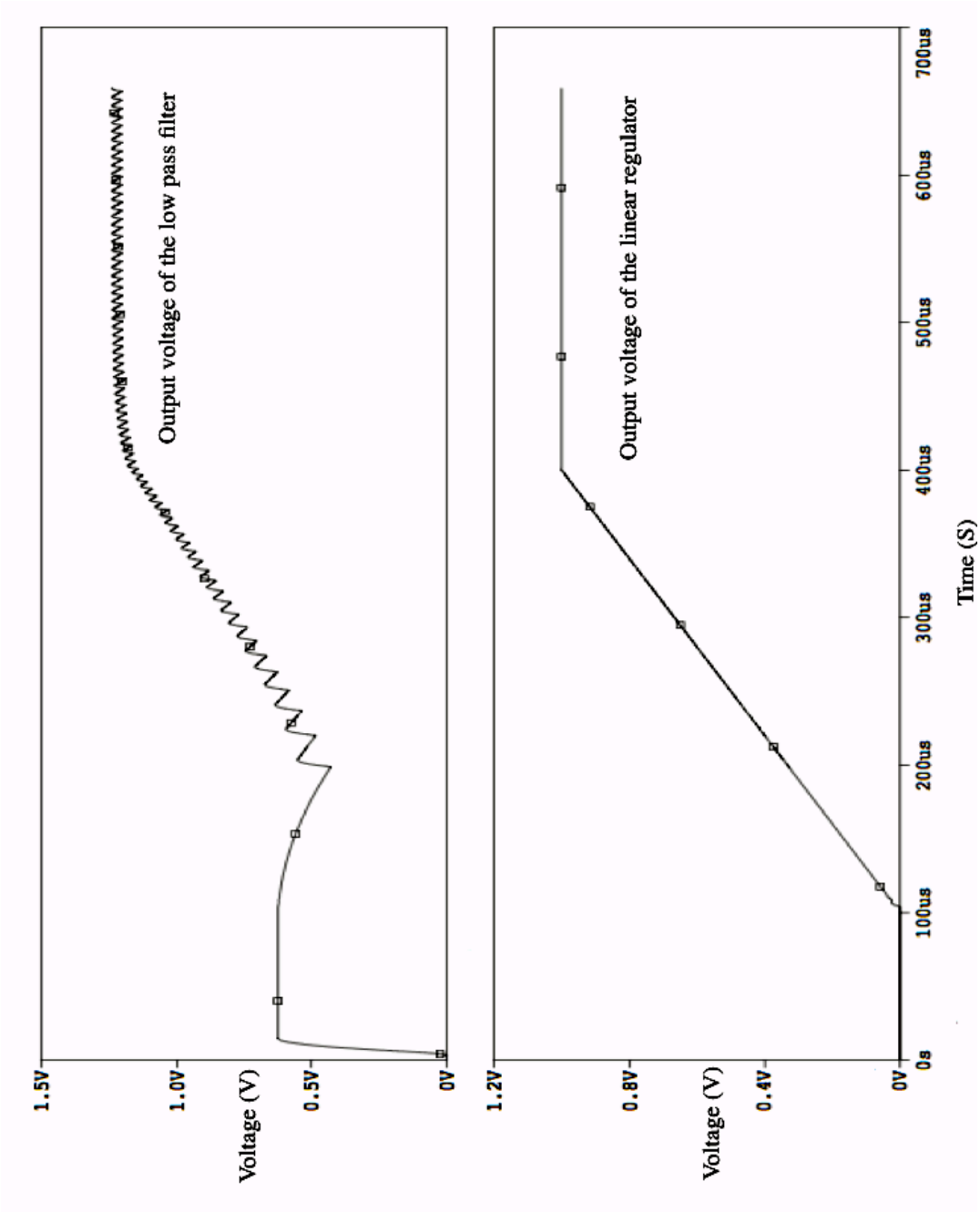


Figure 7.32: The output voltage of the low pass filter and linear regulator

Current Regulator

This is the circuit that creates the extremely accurate current to the magnetic lenses. It is made up of a very high gain, low offset and low output impedance amplifier that drives a big NFET. The simplified block diagram of the current regulator is shown in figure 7.33. The detailed schematic of the linear regulator is shown in figure 7.34.

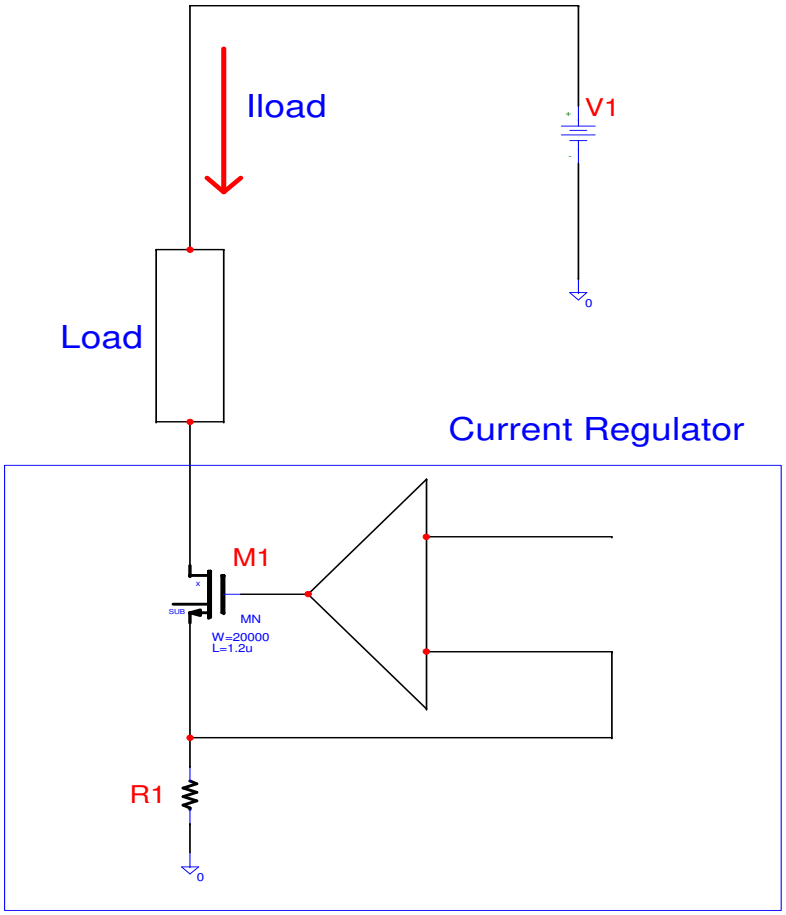


Figure 7.33: Block diagram of current regulator

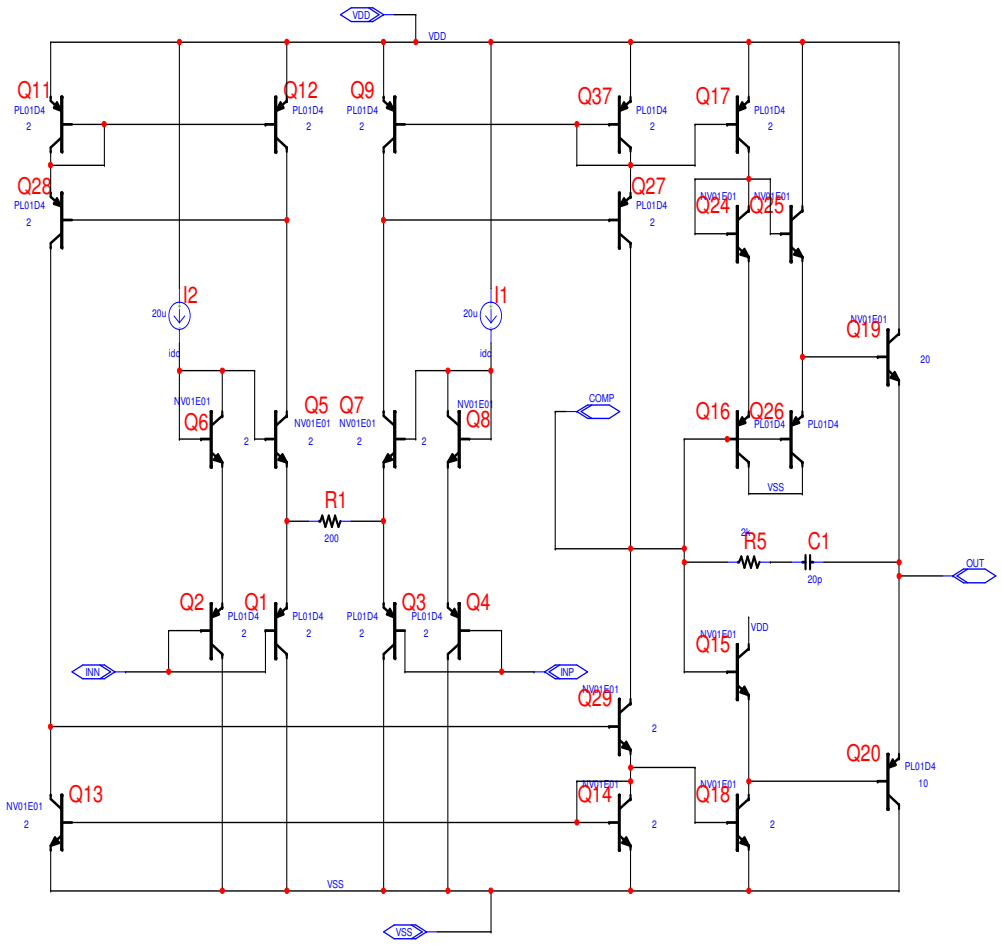


Figure 7.34: Schematic of current regulator

Voltage Adjust Circuitry

There are two reasons for voltage adjust circuitry in this current regulator system. The first one is that the current must remain absolutely constant. A MSOFET's drain current is a function of its V_{GS} and its V_{DS}. The current in a MOSFET can be described by

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \quad (7.12)$$

where

W = width of MOSFET transistor

L = length of the MOSFET transistor

μ = mobility of charge carriers

C_{ox} = oxide capacitance per unit area

V_{th} = threshold voltage

V_{GS} = gate to source voltage

V_{DS} = drain to source voltage

λ = channel modulation

It can be seen that the current will be changed when its drain to source voltage changes. So, it is paramount to control the V_{GS} as well as V_{DS}. The first function of the voltage adjust circuitry is to guarantee that V_{DS} is kept as constant as possible. The other function of the voltage adjust circuitry is to keep the V_{DS} as low as possible, but still keep the transistor in saturation, so the power loss through thermal radiation is minimized. Since the power that is wasted through heat is

$$Power\ Loss = I_{LOAD} * V_{DS} \quad (7.13)$$

the power loss is low if V_{DS} kept low. In this way, the heat that is generated in the system is kept as low as possible. Since heat can have a huge negative impact on the system, then this is an important design consideration. Figure 7.35 shows how voltage adjust circuitry accomplishes this task.

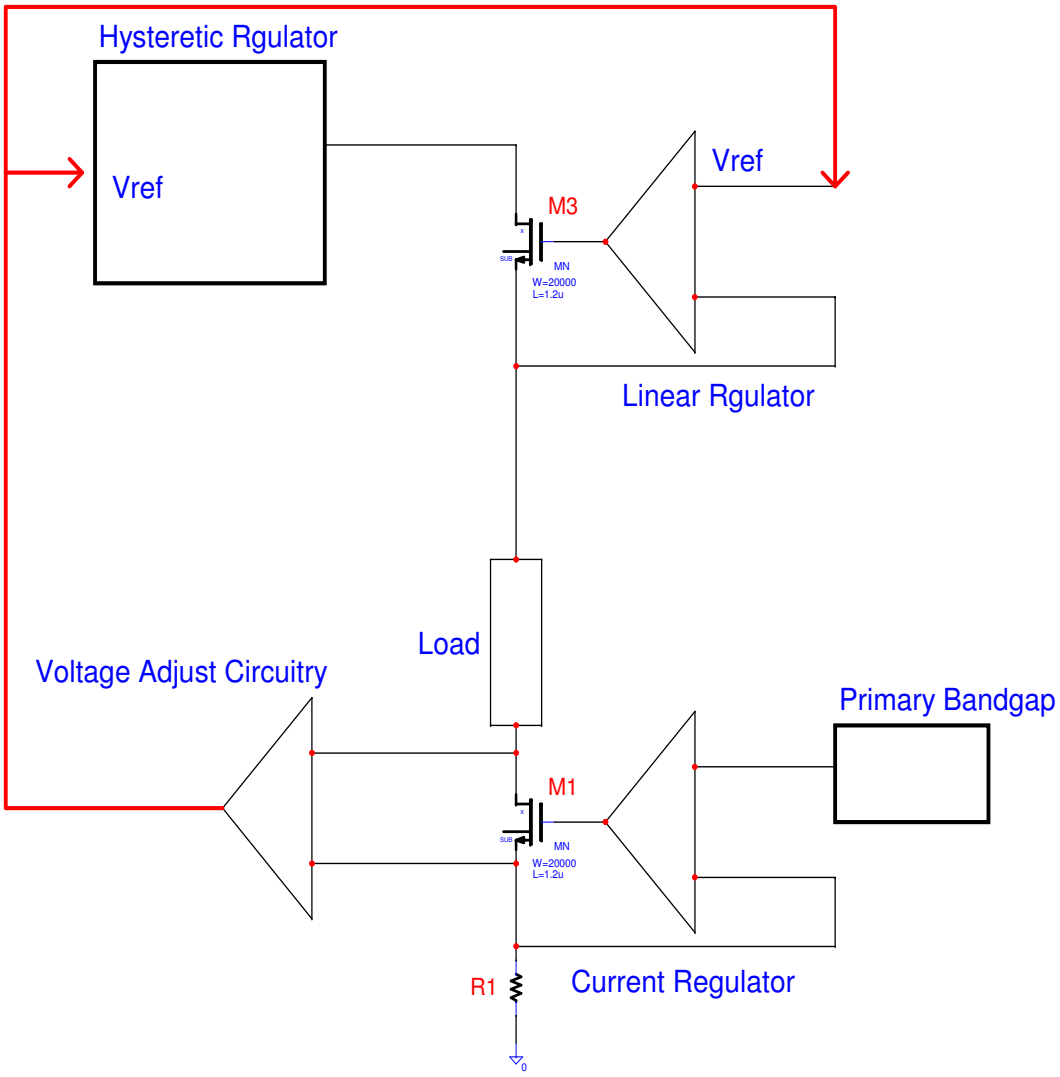


Figure 7.35: Block diagram of the current supply system

The voltage adjust circuitry monitors the V_{DS} of the power MOSFET M1, and it will change the reference voltage to the hysteretic regulator and linear regulator. That means the output voltage will vary to make the V_{DS} of the MOSFET M1 constant. In a way, the output impedance of the current source is increased by the open loop gain (A_{ol}) of the voltage adjust circuitry amplifier.

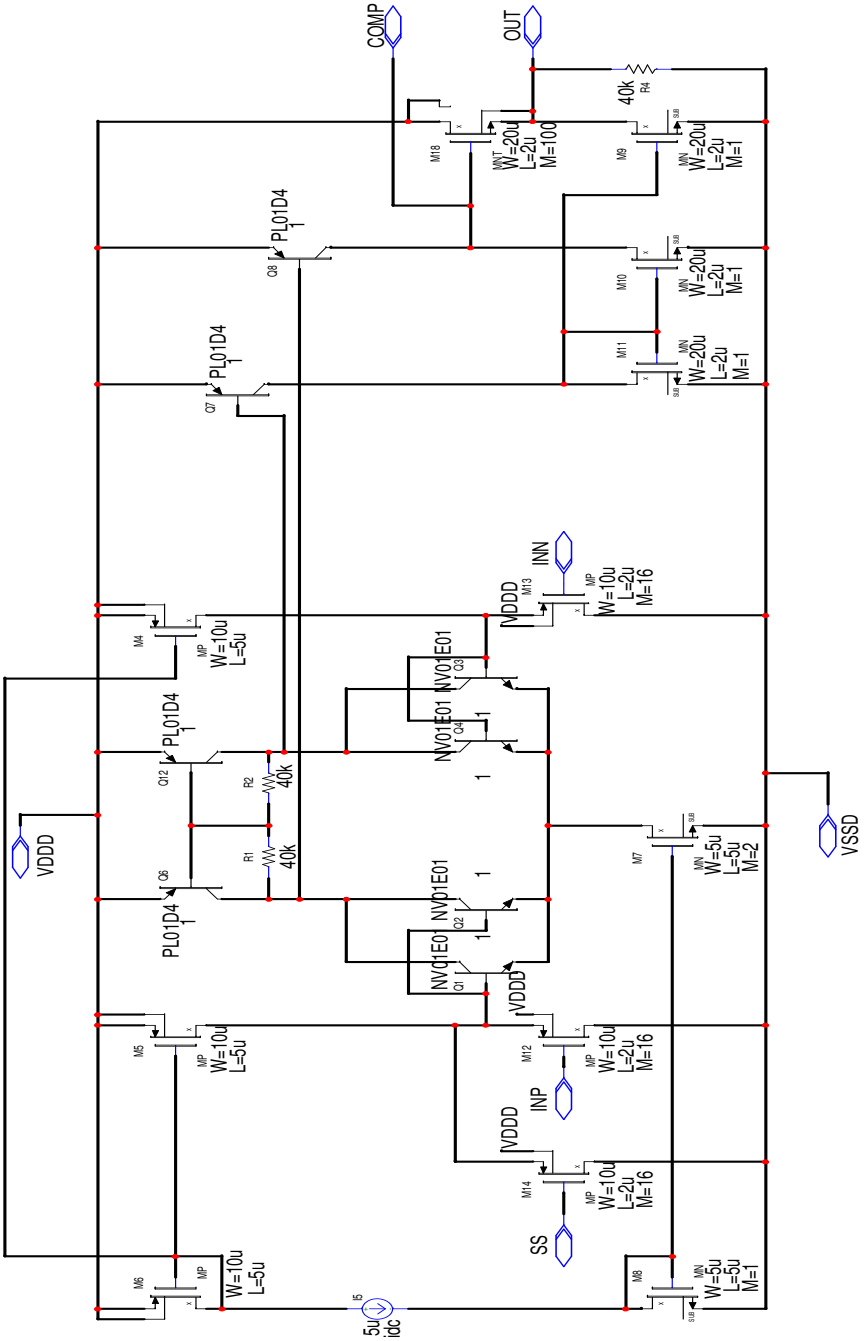


Figure 7.36: Schematic of voltage adjust circuitry

The Complete Current Supply System

The schematic of the complete current supply system is shown in figure 7.37. A 10mH inductor with a series resistance of 0.5 ohms was used to simulate the magnetic lens which serves as the load for this current supply system. All the blocks are shown on this picture. The hysteretic converter block, itself, is composed of five hysteretic converter sub-blocks. The system performs as expected, by regulating the current within the range of expected stability. The waveforms of this block are shown in figure 7.38 and 7.39. In figure 7.39 the maximum change in current versus time and at three different supply voltages that vary from 2.5 to 5.5 volts for a 1 amp output is 10.9 na that corresponds to 0.0109 ppm. Figure 7.40 shows the change of output current vs. temperature.

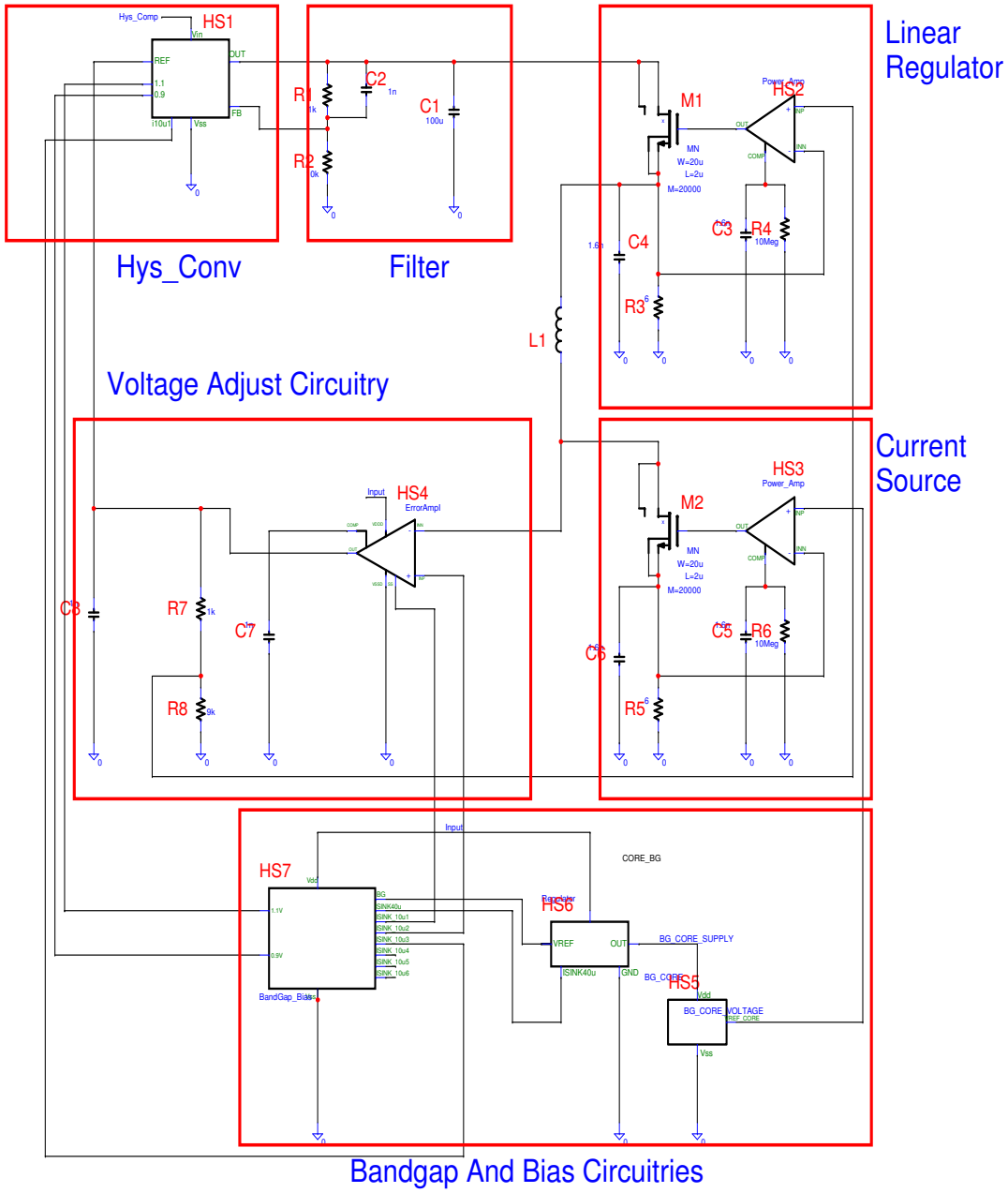


Figure 7.37: Complete schematic of the current supply circuitry

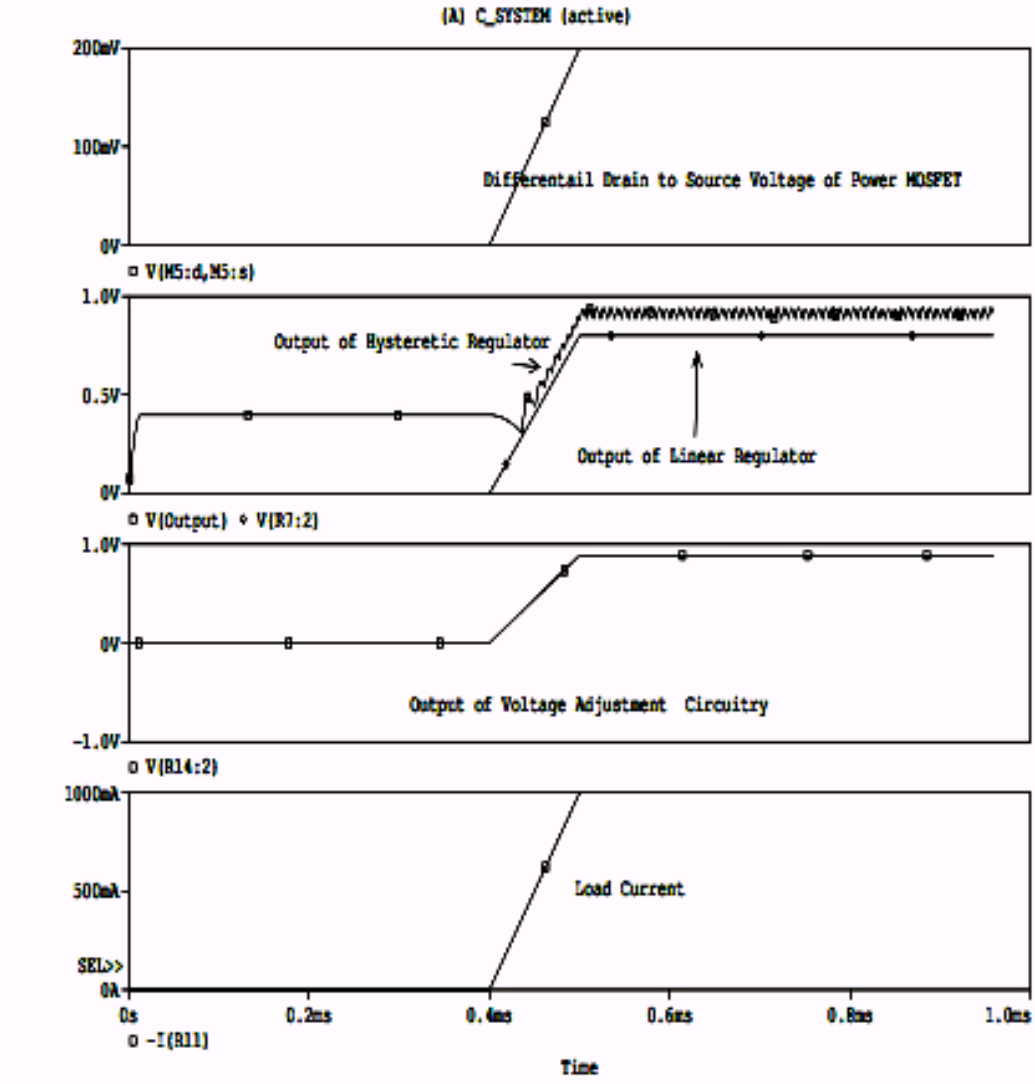


Figure 7.38: The waveforms of the overall current supply system

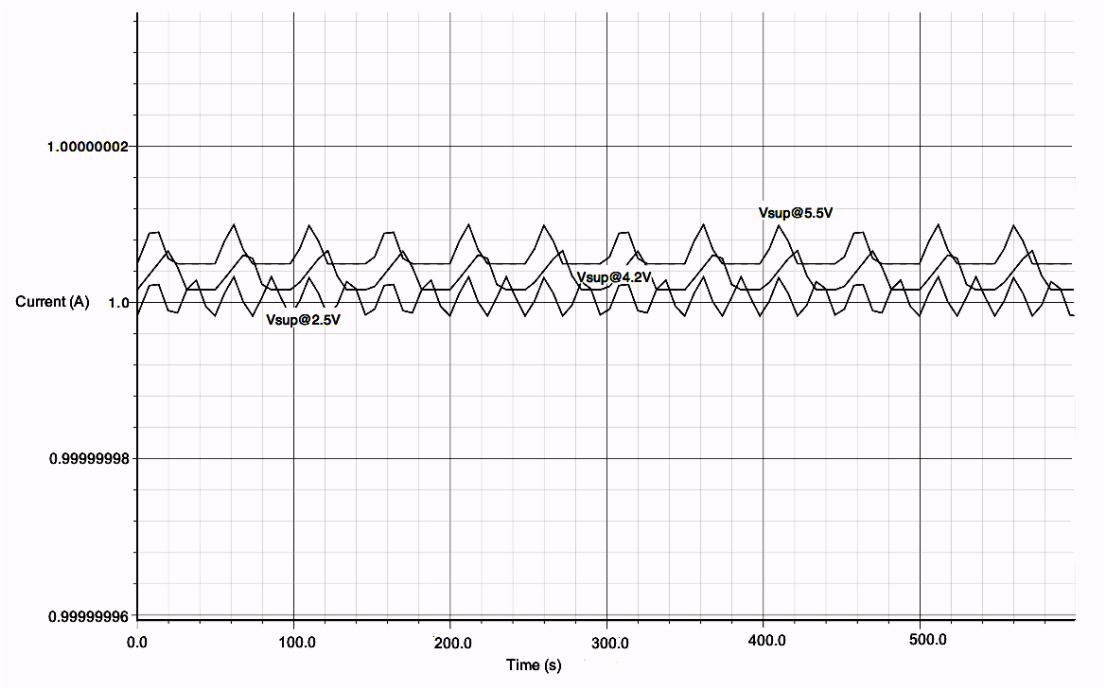


Figure 7.39: Output current vs. time at three different input supplies

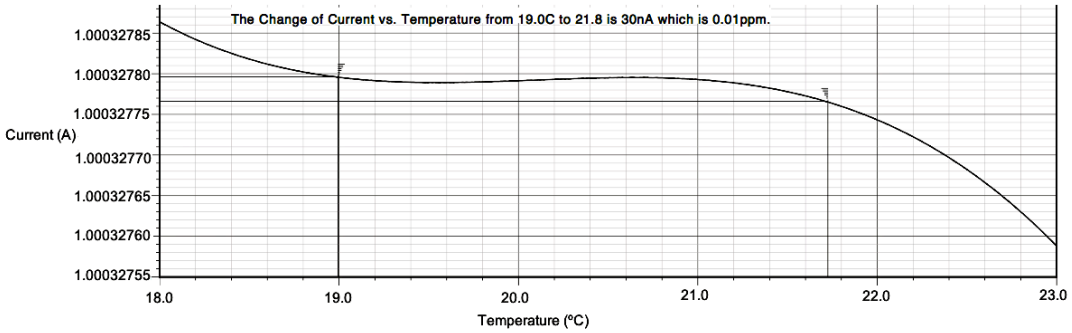


Figure 7.40: Change of output current vs. temperature

Figure 7.41 shows how the system reacts when the supply voltage varies. Output of the linear regulator, output of the low pass filter, and output current is shown.

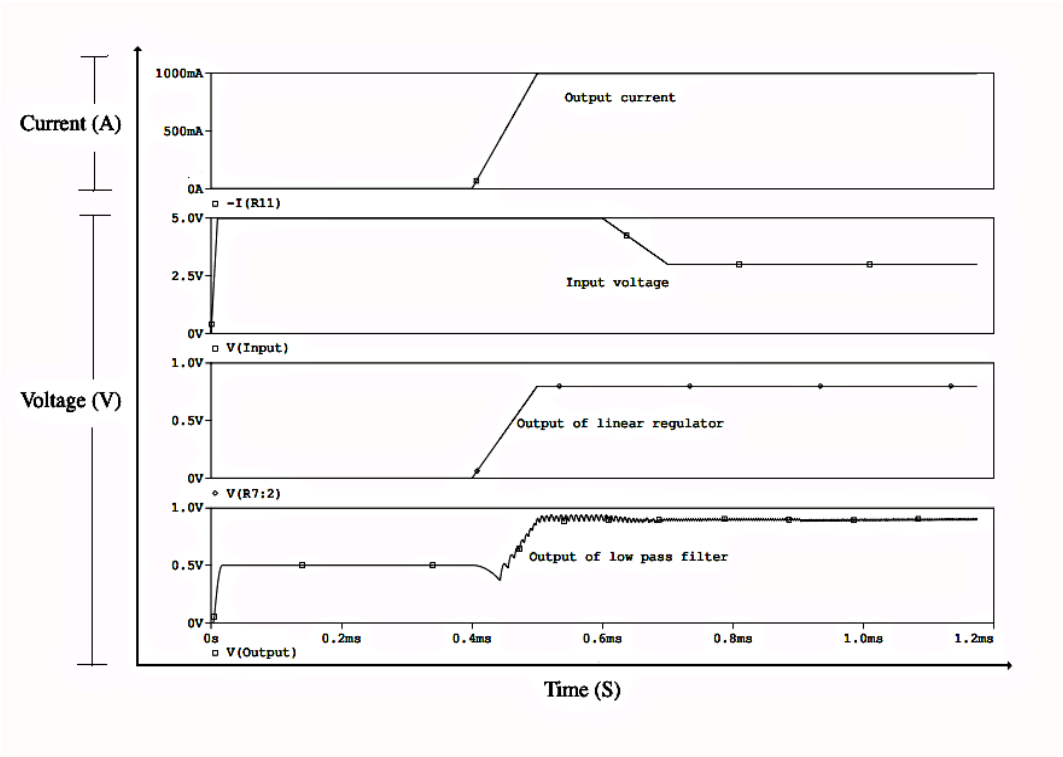


Figure 7.41: Variation of output voltages and current vs. input voltage supply

The waveforms in figures 7.42 and 7.43 show the system response during the load transient. In the first figure, the load is stepped up from 700mA to 1A to show how fast the system recovers to a large step load. The second figure shows how the system reacts and recovers in a small step load. In both cases, the current supply recovers from fast transients in less than 10us without any sustained oscillations that shows high bandwidth and good stability.

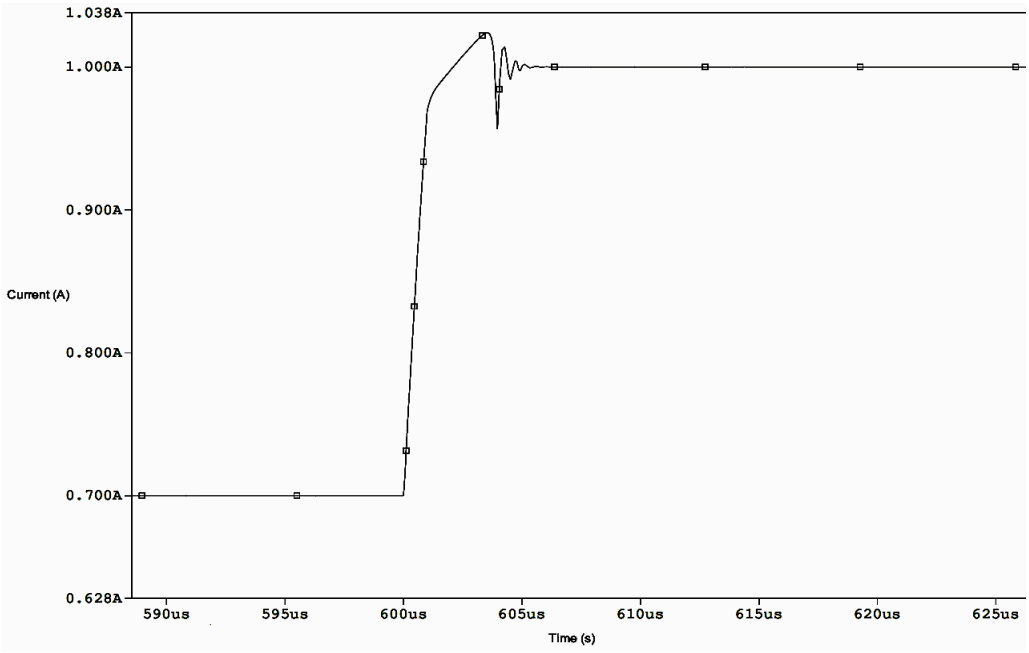


Figure 7.42: Load transient from 0.70A to 1.00A

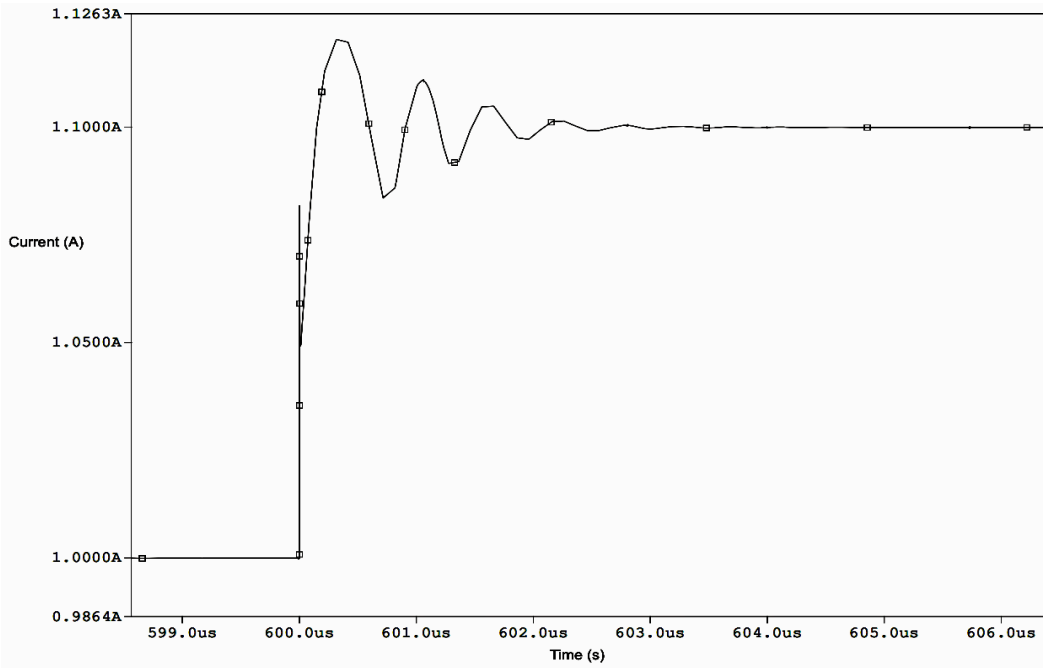


Figure 7.43: Load transient from 1.00A to 1.10A

Chapter 8

Summary & Conclusion

The challenges and difficulties of this design will be discussed at this point. This chapter starts with a discussion of the problems that must be taken into account in constructing this high stability current supply system. The right technology, the right circuitries, and the right physical structures of the overall system are of paramount importance. This summary will conclude with the potential of future research and the recommendations for improving the future undertakings of building an ultra high stability current supply.

Technology

At the present time, there are many technologies available that can be selected to build this current supply. The technologies are:

- CMOS process
- BIPOLAR process
- BICMOS process.

CMOS technology is the most widely used process for the manufacturing of circuits and systems. The advantage of a purely CMOS technology are its availability and its low cost, but this technology does not have the variety and the quality of devices that are needed for building high stability circuitries. A CMOS process does not have the N-buried layer, a highly rich N-type dopant layer that is needed to isolate the sensitive circuitries as needed (39). That means the NMOS power transistors cannot become isolated and their switching noise is coupled to the substrate that is common to all circuits.

On the design of this current supply, the hysteretic converter has a number of n-channels of power transistors that, if are not isolated, can jeopardize the ultimate stability that is required. The other disadvantage of a CMOS technology is the lack of available bipolar transistors. Compared to MOSFET transistors, bipolar transistors have higher transconductance, lower offset voltage, lower noise voltage, and superior device matching (39). These advantages of bipolar transistors make them more suitable in the design of sensitive circuitries, such as amplifiers and the voltage reference cells. These drawbacks of a purely CMOS technology makes it unsuitable for the design of this ultra stable current supply system.

Bipolar technology is suitable for building good quality analog circuitries with excellent performance. It is important that in this particular design, sensitive analog circuitries have as many bipolar transistors as possible. There are, however, disadvantages to a bipolar process that must be taken in account. Bipolar transistors tend to be larger than CMOS transistors that can make a system design with large number of transistors impractical. In this current supply design the digital blocks, the bias circuitries, and the comparators can be fabricated using MOSFETs. This will save a big area and cost in design of the overall system. The other advantage of MOSFET transistors is their distinct advantages when it comes to the design of power transistors. Bipolar transistors suffer from emitter debiasing, thermal runaway, and secondary breakdown, which makes them unsuitable for power transistor design (39). The current supply that is designed for this thesis has a total of ten power transistors. The designs of these power transistors play a crucial role for selecting the proper technology.

Since both CMOS and bipolar transistors have their own distinct advantages that, together, are important for the success of this design, the

BiCMOS technology is chosen as the proper technology. In a BICMOS process, both CMOS devices and bipolar devices are available. This technology allows the capability of isolating all the noisy power and digital circuitries from the quiet analog circuitries. This makes the design of this ultra accurate current supply practical and achievable. CMOS transistors will be used in places that are suitable for them like the digital circuitries, the comparators, the drivers, the power transistors, and all the current mirrors. The bipolar transistors will be used in all the sensitive analog circuitries such as the bandgap, and all the amplifiers that are used in this system.

System and Circuit Design

The system selected for this current supply, as shown in figure 7.1, plays a fundamental role in the success of this design. The main block of this system is the current regulator that sources current to the load. The integrity of this system depends upon how accurately this current regulator is functioning. An ideal current source has extremely high output impedance and its current must remain as constant as possible throughout the specified temperature range. To make sure these objectives were met, two key decisions were made. The first one was to use a switching converter that would lower the input voltage to a level so that less heat will be radiated away through the current source. The second one was to use a mechanism that would keep the drain to source voltage of the NMOS power FET in the current source as constant as possible. In order to accomplish the second objective, the voltage adjust amplifier block was added.

The Integrated circuits are sensitive to heat and heat production. Transistors and their performances are a strong function of temperature and the surrounding heat generation. For example: the leakage current of junction diodes varies, the base to collector current gain (β) of bipolar transistors

change, the base to emitter voltage (V_{be}) of bipolar transistors change, the threshold voltage (V_{th}) of MOSFET transistors change, and the value of passive elements like resistors and capacitors change as a function of temperature. The accumulated effect of all these changes can be deleterious to reach the ultimate stability in the current that is required. For these reasons, the system must be designed in a way to minimize the heat production. The hysteretic block will lower the input voltage with an efficiency of up to 95%. This is the optimum efficiency that can be obtained with the present technologies. The other advantage of a hysteretic converter, as compared to a fixed frequency (PWM) switching converter, is that it does not require any compensation for stability. This will render the system unconditionally stable to all conditions and variables. This introduces a degree of freedom that is particularly invaluable to the system design. For one, a higher order filter can be used to attenuate the noise, rather than the second order filter that is normally applied.

One of the core disadvantages of a switching power supply in general and a hysteretic converter in particular is their inherent noise production. The outputs of the power stages of these converters inject a substantial amount of noise, through unwanted current injection, in the substrate. This is the same substrate that is common to all other circuit blocks of this current supply system. If proper measures are not taken, then sensitive blocks might not function optimally. To mitigate this issue the circuits must have architectures that are robust and insensitive, as much as possible, to the noise generation. Bipolar transistors have a degree of immunity to noise and fast transient disturbances that MOSFET transistors do not. The other way to protect the sensitive circuitries from the substrate noise is to isolate them at the device level. It is the reason, as explained above, that a BICMOS technology was

selected. A BICMOS technology provides a reasonable degree of isolation from substrate noise by providing an N-buried layer and deep N-well.

The hysteretic converter, not only, introduces noise to the substrate by its inherent switching activity, but also through the ripple on the current regulator. The second order passive filter that follows the converter will not block all the switching noise. The solution to this problem is either adding more passive filters or a linear regulator that can attenuate as much of the noise as possible. The level of stability that is required by this current supply justifies the implementation of this expensive solution. The linear regulator must have a bandwidth wide enough to attenuate the supply noise as much as possible. The device of choice is, again, bipolar transistors since they have higher bandwidths, more inherent gain, and less susceptibility to noise and latch-ups. Also, as explained in chapter 6, the architecture of this linear regulator must be able to cancel the supply noise that is superimposed on the gate electrode of the power NMOS. The output voltage of the linear regulator is the input voltage of the current regulator. Any noise and disturbances at this point could reduce the current stability.

The current regulator is at the heart of this current supply system. This block must have high bandwidth, high gain, low offset, and low noise. The bipolar transistors are, again, the device of choice for the design of this block. In order to increase the output impedance of the current regulator to extremely high levels, another block voltage adjust amplifier (VAA) is added. Any changes in the drain to source voltage (V_{ds}) of the power NMOS in the current regulator can cause variations in load current that can be catastrophic. The VAA will maintain a constant V_{ds} across the NMOS power FET of the current regulator. VAA will also maintain a low thermal generation by keeping the V_{ds} of the power FETs of the linear regulator and the current regulator as low

as possible. Finally, a second order bandgap with extremely high stability with respect to temperature and supply is designed. The main bandgap uses bipolar core architecture with curvature correction to meet the 0.01 ppm that is required in this design. In order to increase the PSRR to values large enough for this current supply design, a secondary bandgap is designed that powers the amplifier that supplies the primary bandgap. In this way, the primary bandgap voltage, to a large degree, is isolated from supply and any variation imposed on it.

The layout of this design will play a fundamental role in its success. The placements of each block at the right place and orientation will be of paramount importance in the final achievement of this plan. The digital blocks and the hysteretic converter need to be separated and placed in their own isolation pocket. They will be isolated by a reversed biased junction diode that surrounds the whole structure. For example, the isolation can be achieved by putting the noisy devices in a pocket of N-buried layer surrounded by a deep N-well and N+ connected to the highest voltage. On the other hand, the analog circuitries sit in their own pockets isolated in the same manner explained above. The analog circuitries are, further, divided into sensitive and non-sensitive blocks. The linear regulator and the current regulator are considered as power stages, and they produce more heat than the other analog circuitries. For that matter, they are separated from the other circuitries as much as possible. The voltage references are the most vital part of this design, so they are located away from noise and heat generating blocks as much as possible as shown in Figure 8.1. These sensitive analog blocks are further isolated from the rest of analog circuitries by another level of isolation as shown.

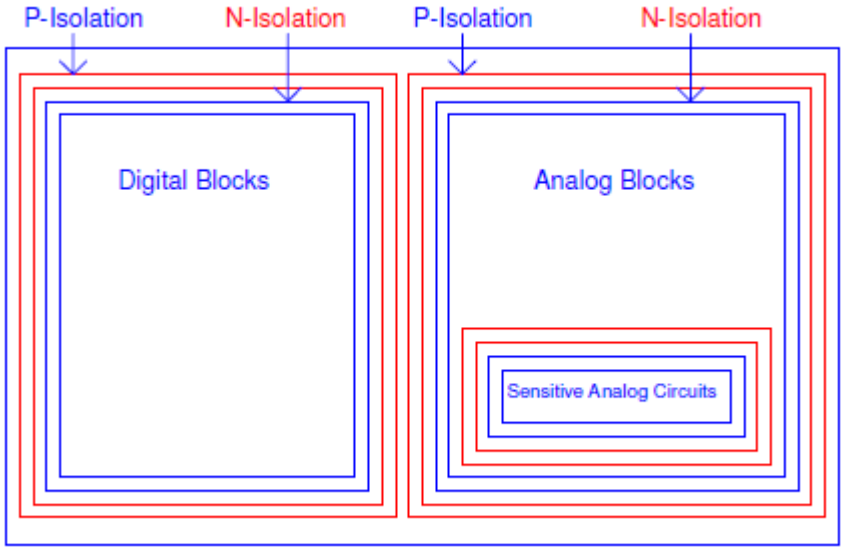


Figure 8.1: The placement of analog and digital blocks

In this thesis, an ultra stable current supply was designed and simulated. The success of this current supply was based on selecting the proper system, the most robust and precise circuit architectures, and the most optimum device configurations and layout. The goal of the system design was based on high efficiency for low thermal generation, ease of compensation, a stable and noiseless supply voltage for the load, and a current source with output impedance as high as possible. On the circuit level, the most crucial circuit blocks were designed with bipolar transistors since they provide more gain, less offset voltage, and superior device matching at the layout level compare to MOSFET transistors. The simulations results indicated the performance of this current supply exceeds the 0.01ppm that was required. In the future, the stability constraints can go beyond the requirement of this thesis. The future design for a more stable system must take advantage of technologies where the offset voltage, noise transmissions through capacitive coupling, and better device matching is possible. At the circuit level, a third

order bandgap, amplifiers with active offset cancellation circuitries for better matching, and faster transistors with more intrinsic gain are of importance.

The stability of the current is based on the stability of the bandgap. The stability of this bandgap changes by only 30nV in the temperature range of 19^{o}C to 21.8^{o}C (41). This means a stability of 0.0086 ppm/^{o}C, which is within the range that is required for this design. It is important to keep the ambient temperature within the boundary that gives the best stability for this bandgap that is between the points specified above and shown in figure 8.2. Since a temperature control of only plus or minus 1.0 ^{o}C around 20.5 ^{o}C is needed the system can be kept in the temperature-controlled environment (41). The waveform in figure 8.3 shows the line regulation of this system. The current supplied is measured at three input voltages of 2.5V, 4.2V, and 5.5V. The supply current is run for 600s and the stability variations are less than 20nV, which supersedes requirement of this system. These figures demonstrate the system is functional, stable, and meets the criterion and objective that were set from the beginning.

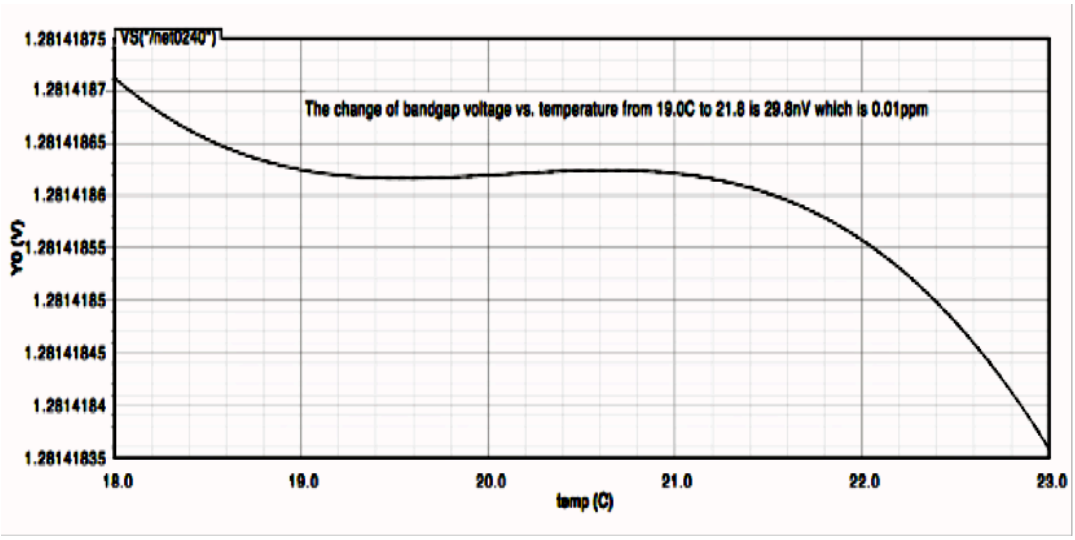


Figure 8.2: Zoomed in bandgap voltage vs. temperature

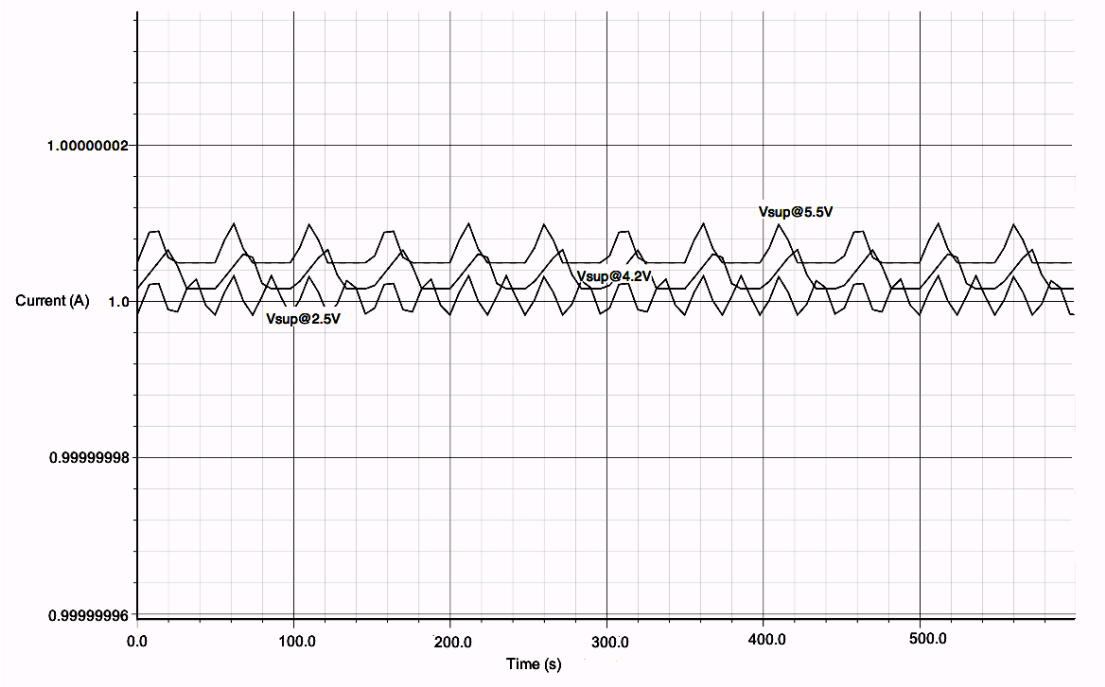


Figure 8.3: Output current vs. time at three different input supplies

Figure 8.4 shows the change of output current vs. temperature. Between 18 degree C to 21.8 degree C the output current change is 30nA. That means the stability of the output current is less than 0.01ppm.

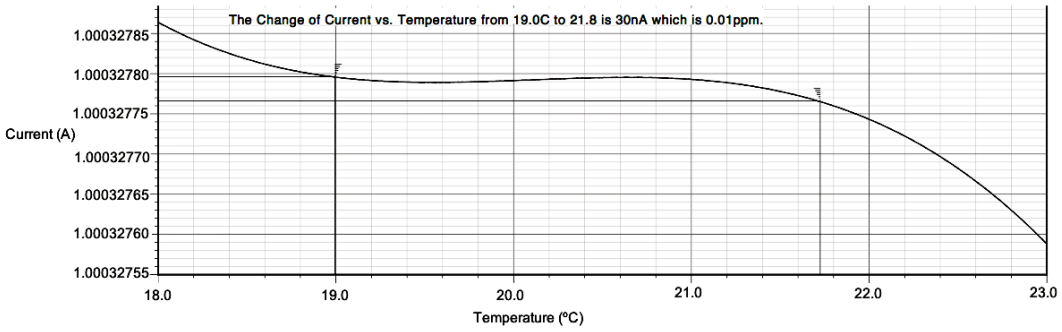


Figure 8.4: The change of output current vs. temperature

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