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A 512-Channel Neural Signal Acquisition ASIC for High-Density Electrophysiology

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Abstract—The complexity of information processing in the brain requires development of technologies that can provide spatial and temporal resolution by means of dense electrode arrays paired with high-channel count signal acquisition electronics. In this work, we describe a highly flexible neural readout application-specific integrated circuit (ASIC) that successfully integrates 512 channels on a dense 8.2mm x 6.8mm 2D layout. Each DC coupled channel features a gain and bandwidth programmable analog front-end, and 14b 30kS/s analog-to-digital conversion. The chip was fabricated in a 0.18 μ m 1.8V CMOS technology and dissipates a total of 125mW. The chip is bump-bonded on a base circuit board, creating an ultralight 350mg flexible module, which can be used in a single or multi-module system with a variety of electrode arrays.

Index Terms—Brain-machine interface, biomedical electronics, in vivo, high channel count, neural readout.

I. INTRODUCTION

Large-scale, high-density neural recording is a key requirement in understanding how brains process information, and how dysfunction can disrupt this process. The nature of this job is inherently distributed; multiple brain regions contribute to any given function through complex, distributed neural circuits with activity patterns at the millisecond timescale. A large number of recording sites featuring high anatomical spatial coverage and millisecond temporal resolution is necessary for any new technology developed to tackle this problem.

Significant progress has been made in increasing the number of electrodes in silicon and polymer probes [1] [2], therefore increasing the requirement for high-channel count neural readout electronics. Current state-of-the-art commercial ASICs feature up to 64 recording channels [3] [4], each with an AC-coupled front-end with limited scalability due to the large capacitors required for a 1Hz high pass cutoff. In [5] and [6] up to 384 readout channels are demonstrated, monolithically fabricated with electrodes and circuits on a silicon substrate. Although monolithic fabrication allows increased channel count, the readout cannot be integrated with other probes or electrode technologies.

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This work achieves readout and digitization of 512-channels, the highest number of simultaneous recording channels integrated onto a single chip. The prototype borrows a 2D layout approach that has previously led to major developments in particle physics and X-ray microscopy, allowing much higher density of electronics than standard 1D layouts. It features a DC-coupled programmable analog front-end and in-pixel digitization, as well as programmable clock distribution, and data encoding and serialization, making it a complete high-density neural readout solution, compatible with various high density electrode arrays, in standalone or multi-module configuration.

The system design is presented in II, with details on the circuit design for each channel discussed in Sections II-A and II-B. Bench and in-vivo measurement results are presented in Section III.

II. SYSTEM ARCHITECTURE AND CIRCUIT DESIGN

The proposed chip architecture of this work is shown in Fig. 1 as part of the whole neural data acquisition system. Each module consists of 4 shanks of 128 passive electrodes. A flexible ribbon cable connects the neural probes with a 10mm $\times$ 17mm base circuit board. The chip is bump-bonded on an interposer board, which is then bump-bonded to the electrode array. Its output is routed to an ultralight 0.5mm-pitch connector, to be sent to an FPGA for processing. The whole system is designed to not exceed a weight budget of 350mg for each module, therefore allowing for up to 8 modules to be stacked together inside the headstage, resulting in a total of 4096 electrodes which can be processed by a single FPGA.

Figure 2 shows the floorplan and power distribution scheme. Each chip contains 512 channels, organized as 32 rows by 16 columns. Each channel includes the electrode pad, and one column of additional power pads is placed between every two electrode pad columns. These additional power pads achieve ultra-low resistance power routing, easy decoupling, and reduced on-board power regulation requirements, at the cost of chip area.

Each pixel consists of a front-end neural amplifier with programmable gain, a programmable anti-aliasing filter, a

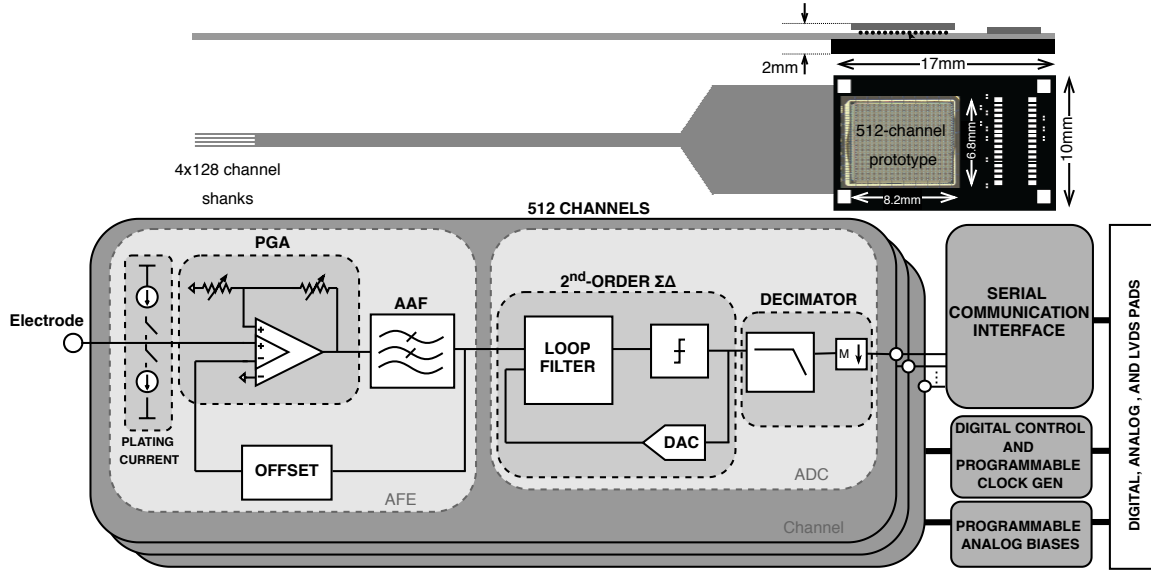


Fig. 1. High-level system architecture of the proposed neural readout ASIC.

buffer, and a 14b $\Sigma\Delta$ ADC, including the digital decimation filter.

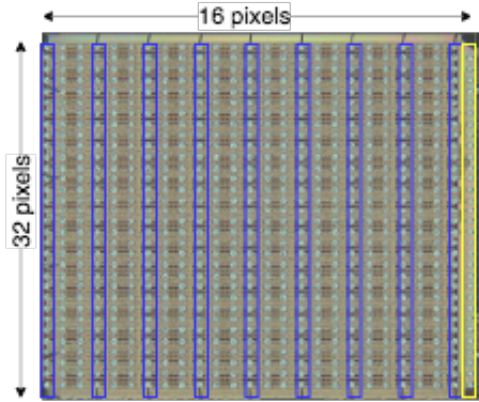


Fig. 2. Die photo of the chip. Power pad columns (blue) are placed between every two electrode pad columns. Output pads are highlighted in yellow.

A. Analog Front-End

The Analog Front End (AFE) consists of a DC-coupled amplifier with programmable gains of 5,10,20,50,100 or 200. The electrode signal presents to the non-inverting input of the amplifier. In order to compensate for electrochemical offsets, once the amplifier output exceeds a programmable threshold, the output is pulled by putting sufficient charge on a capacitor connected to the inverting input so that the output voltage is zero. Electrode plating currents are provided through programmably gated current mirrors. A DAC common to all channels sets the value of the plating current. The amplifier is followed by an anti-aliasing filter (AAF) with a programmable cutoff frequency.

B. Sigma-Delta ADC

To determine ADC specifications, a spike sorting algorithm was applied to publicly available rat neural recordings, which were reconstructed to create a *golden* data set. The golden data was then digitized in software with various levels of non-idealities. It was determined that a 14b ADC causes a sufficiently small error in neural clustering produced by spike sorting. Linearity requirements are relaxed, and bandwidth requirements are limited to less than $\leq 10\text{kHz}$ due to the nature of intracortical signals. A 256-times oversampled 2nd-order $\Sigma\Delta$ topology was chosen to meet these specifications, while achieving also low power and area.

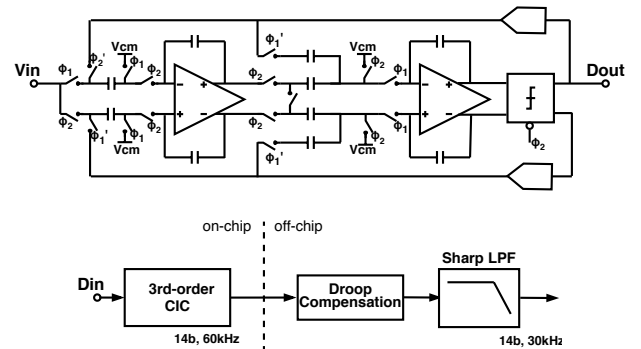


Fig. 3. Simplified schematic of the modulator (top) and block diagram of the decimator (bottom).

The modulator is implemented as a discrete-time, switched-capacitor topology, in a single-ended-to-differential configuration to maintain reasonable linearity while maximizing dynamic range. The decimation filter was separated into two components, a pre-filter which was implemented in the pixel

and a post-filter implemented off-chip. This allowed a tradeoff between on-chip filter area and data communication bandwidth requirements because as the modulated signal is decimated bandwidth is traded for resolution. The decimation pre-filter is implemented as a Cascaded Integrator Comb (CIC) filter, using a computationally efficient implementation of a narrow-band FIR lowpass filter that does not require multipliers, which greatly relaxes the area and power dissipation requirements [7].

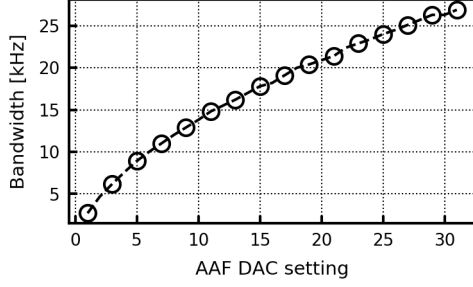


Fig. 4. Measured system bandwidth vs. AAF DAC value.

C. Digital services

Two 14-bit words, representing the sample from two channels, are encoded in a 32-bit DC-balanced output word. The chip serializes the data output on two LVDS channels, each carrying the data from $16 \text{ rows} \times 16 \text{ columns}$ of pixels, at a rate of $32 \times 128 \times f_s$, where f_s is the sampling frequency. Chip programming is performed via a 2-wire interface, with token passing to control multiple chips in multi-module assemblies.

III. SILICON MEASUREMENT RESULTS

The design was fabricated in a $0.18\mu\text{m}$ CMOS process. A microphotograph of the prototype is shown in Fig. 2. Each channel occupies 0.099mm^2 , including the area of the power pads. The total chip area is 55.8mm^2 . Both standalone bench testing and *in vivo* testing were performed, and the results are presented in Sections III-A and III-B, respectively.

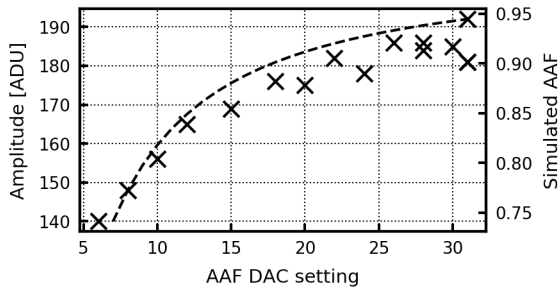


Fig. 5. Simulated amplitude for a 0.2mV 10kHz input sinusoid, compared to simulated AAF response. The AFE gain setting is 50. ADU size is $61\mu\text{V}$.

A. Standalone Measurements

For standalone testing, the peripheral power pads and 32 electrodes are wirebonded onto a custom board. Figure 4 shows excellent bandwidth programmability of the AAF filter.

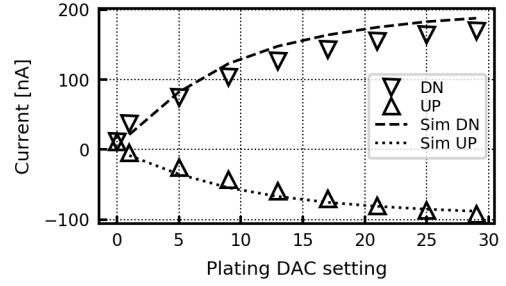


Fig. 6. Simulated and measured plating current programmability.

Figure 5 shows the measured signal amplitude compared against the simulated AAF response, for various AAF DAC settings. For a AAF DAC value of 20, the measured gain is 53.4, very close to the expected value. The plating current DAC was also measured to be comparable with simulation results (Fig. 6). Figure 7 shows signal amplitude over frequency for a 0.2mV input sinusoid. The response is compared to the theoretical response of the AAF and digital CIC filter with gain scaling, and follows the expected roll-off. It also reveals a 15% lower gain comparing to the expected value, in this particular gain setting.

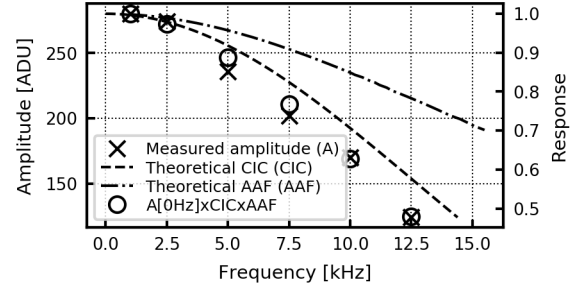


Fig. 7. Measured amplitude for a 0.2mV input sinusoid. The AFE gain setting is 100. ADU size is $61\mu\text{V}$.

Figure 8 shows the input-referred noise (IRN) histogram. Measured noise is $5.4\mu\text{V}$ in the $0.3\text{-}10\text{kHz}$ action potential (AP) band, and $3.1\mu\text{V}$ in the $0.5\text{Hz-}1\text{kHz}$ local-field potential (LFP) band. For our application, the AP band of interest is the $0.3\text{-}6\text{kHz}$ band, which yields an IRN of $4.8\mu\text{V}$. At a 1.8V supply voltage, the total power consumption is $244\mu\text{W/channel}$, including all digital backend and I/O circuits.

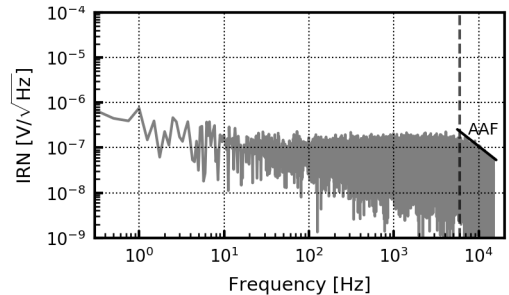


Fig. 8. Measured noise spectrum in AP band of interest ($0.3\text{-}6\text{kHz}$).

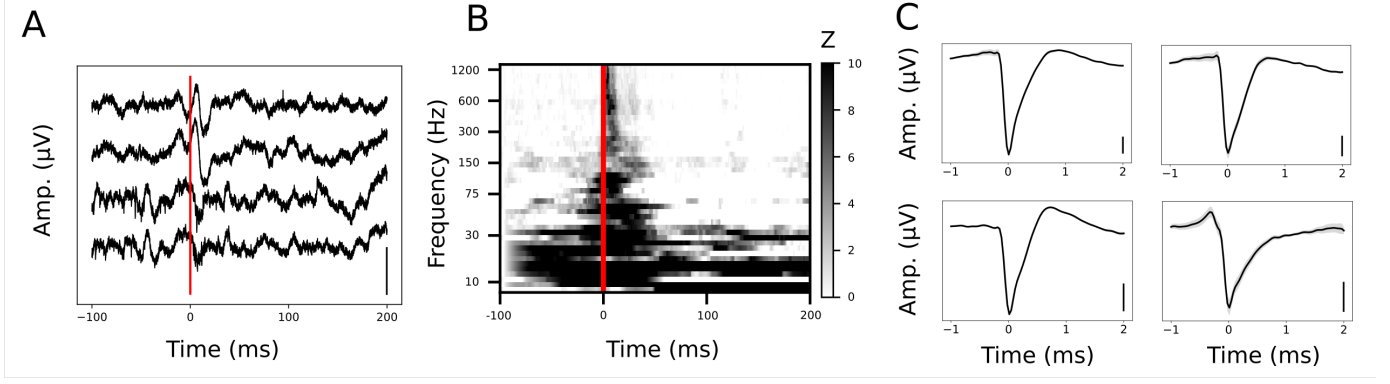


Fig. 9. Chip readout of *in vivo* electrophysiological signals. A) High pass filtered ($f_c = 300$ Hz) signals from 4 channels during the presentation of an auditory stimulus indicated by the red vertical line at time 0. The scale bar is 500 μ V. B) Median spectrogram across 60 trials of auditory presentation showing a broadband increase in amplitude relative to a baseline window. The auditory presentation is indicated by the red vertical line at time 0. The amplitude is normalized by z-scoring (Z) relative to baseline. The colorbar ranges from 0 to 10 Z. C) Four putative single unit waveforms generated by using an automated spike-sorting algorithm. The average waveform is plotted in black and the 95% standard error is plotted as a gray shaded region about the average. Scale bars are 100 μ V.

B. *In vivo* Electrophysiology

We performed an acute craniotomy experiment on a Sprague Dawley rat, which was anesthetized by intraperitoneal injections of Ketamine and Xylazine. A silicon laminar probe was inserted into the primary auditory cortex and a Pt reference wire was inserted into a contralateral frontal region. Auditory stimulus included a white noise burst lasting 100ms played every 1 second for 60 repetitions [8]. The chip readout was sent to an FPGA and main controller unit for digital processing and finally sent to a computer for visualization and data saving. The recordings are post-processed and passed through spectral and spike sorting analysis pipelines. The spectral analysis involves computing the constant-Q wavelet transform for each trial for center frequencies ranging from 8.3 Hz to 1200 Hz. The magnitude of the transform is taken and then normalized by z-scoring relative to baseline. The baseline period lasts 200 samples or ~ 6.67 ms, and starts 100 ms prior to the upcoming stimulus presentation. High pass filtering at 300 Hz, whitening, and spike sorting were performed [9] [10], along with manual curation to identify putative single units.

The prototype was able to readout *in vivo* electrophysiological signals including action potentials measured from laminar polytrodes inserted into cortex. The filtered measured signals from 4 channels are shown in Fig. 9A. Evoked potentials were strongly driven by auditory stimuli across the neural frequency spectrum as expected (Fig. 9B). Spike sorting revealed isolated putative single units (Fig. 9C). These results demonstrate that the proposed design can readout spikes and field potentials that are modulated by a sensory input.

The chip performance summary is shown in Table I, compared to the two most widely adopted state-of-art commercial neural signal acquisition systems.

TABLE I
PERFORMANCE SUMMARY

	[4]	[5]	<i>This work</i>
Recording channels	64	384	512
Total area [mm^2]	28.7	45.2	55.8
Area/channel [mm^2]	0.448 ^a	0.12	0.099
ADC resolution	16	10	14
ADC f_s [kHz]	30	30	30
IRN (LFP) [μ V]	2.4 ^b	10.32	3.1
IRN (AP) [μ V]	2.4 ^b	6.36	5.4
Power/channel [μ W]	351	49.06	244
Supply voltage [V]	3.0	1.2/1.8	1.8
Technology	0.35 μ m	0.13 μ m SOI	0.18μm

^aIncludes I/O and digital interface. ^bUnspecified frequency range.

IV. CONCLUSION

We report a massive 512-channel signal acquisition ASIC which features programmable gain, filtering, and 14b $\Sigma\Delta$ digitization, including digital decimation filtering in each channel. The chip occupies a 55.8 mm^2 area, measures an IRN of 4.8 μ V in the AP band of interest (0.3-6kHz), and dissipates 244 μ W/channel from a 1.8V supply. We present *in vivo* measurements of action potentials using silicon laminar probes on anesthetized rats. This work demonstrates a flexible signal acquisition modular system with potential for ultra high-density neural recording.

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REFERENCES

- [1] G. Buzsáki et al., "Tools for probing local circuits: high-density silicon probes combined with optogenetics," *Neuron*, vol. 86, no. 1, pp. 92-105, Apr. 2015.
- [2] J. E. Chung et al., "High-Density, Long-Lasting, and Multi-region Electrophysiological Recordings Using Polymer Electrode Arrays," *Neuron*, vol. 101, no. 1, pp. 21-31.e5, Jan. 2019.
- [3] J. Du, et al. "Multiplexed, high density electrophysiology with nanofabricated neural probes," *PloS one*, Oct 2011
- [4] Intan Technologies. "RHD Electrophysiology Amplifier Chips," intantech.com: https://intantech.com/products_RHD2000.html, Oct 2021
- [5] C. M. Lopez et al., "A 966-electrode neural probe with 384 configurable channels in 0.13 μ m SOI CMOS," in 2016 IEEE International Solid-State Circuits Conference (ISSCC), Jan. 2016.
- [6] N. A. Steinmetz, et al. "Neuropixels 2.0: A miniaturized high-density probe for stable, long-term brain recordings." *Science*, Apr 2021
- [7] Hogenauer, E., "An Economical Class of Digital Filters for Decimation and Interpolation", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, Vol. ASSP-20, No. 2, April 1981
- [8] V. L. Baratham. "Columnar localization and laminar origin of cortical surface electrical potentials," *bioRxiv*, Jan. 2021.
- [9] J. E. Chung et al., "A Fully Automated Approach to Spike Sorting," *Neuron*, vol. 101, no. 1, pp. 1381-1394, 2017.
- [10] A. P. Buccino "SpikeInterface, a unified framework for spike sorting," *Elife*, Nov. 2020.