Title
ON USING HIGH SPEED DIGITAL INTEGRATED CIRCUITS FOR NUCLEAR INSTRUMENTATION

Authors
Althaus, R.F.
Lee, K.L.
Kirsten, F.A.
et al.

Publication Date
1973-05-01

Presented at International Conference
on Instrumentation for High Energy Physics,
Frascati, Italy, May 8-12, 1973

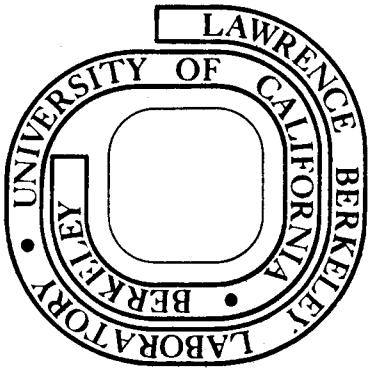
LBL-1750

ON USING HIGH SPEED DIGITAL INTEGRATED CIRCUITS FOR NUCLEAR INSTRUMENTATION

R. F. Althaus, K. L. Lee,
F. A. Kirsten, and L. J. Wagner

May 1973

Prepared for the U.S. Atomic Energy Commission
under Contract W-7405-ENG-48



LBL-1750

DISCLAIMER

ON USING HIGH SPEED DIGITAL INTEGRATED CIRCUITS FOR NUCLEAR INSTRUMENTATION*

R. F. Althaus, K. L. Lee, F. A. Kirsten and L. J. Wagner
Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

1. - Summary

Commercially available high speed digital integrated circuits (I.C.'s) now have performance characteristics and economy that make them attractive as central logical elements around which state-of-the-art instruments for High Energy Physics can be developed. In work reported five years ago[1] commercial I.C.'s were shown to offer advantages of economy and packaging density, which were valued in some large system arrays, but their performance was below that of the 200 MHz commercially available counting equipment. No longer must speed, or resolution, be compromised for these advantages. Circuits now configured around the Motorola** MECL III line of integrated circuits provide 300 MHz speed, 1.2 ns maximum rise- or fall-time, coincidence recognition for 1 ns overlap, and inherent coincidence time resolution edges of less than 40 ps (1000:1 count rate).

Two modular packaging schemes using MECL III I.C.'s have been developed at the Lawrence Berkeley Laboratory. The first to be described, called the FLOGIC System, achieves high packaging density by means of logic cards that are interconnected in a custom design unique to each experiment. The FLOGIC System is most suitably used where many channels of instrumentation are required and the configuration of these channels, once established, is not subject to frequent unprescribed change. The second scheme uses the NIM Standard[2] hardware. This scheme offers the convenience and versatility of standardized hardware and signal levels.

2. - THE FLOGIC System

The FLOGIC System is modular at the printed circuit card level. Small (55mm X 114mm) printed circuit cards containing I.C. gates and registers are interconnected to perform the logical functions desired for a specific application. Achieving this modularity in a manner consistent with the performance characteristics of the MECL I.C.'s and with economically practical hardware were the dichotomous objectives of this system. Subminiature coaxial connectors, as a natural first consideration for interconnection, match the performance characteristics, but are prohibitively expensive and leave the distribution of d.c. power as a separate consideration.

Unique utilization of standard commercial component parts provides performance at an attractive cost. Interconnection is accomplished by means of DIAD connectors, an adaptation of the Termi-twist/Termi-point printed circuit card-edge connector series manufactured by AMP.* The overall system is packaged in bins available from Data-Tech.** Power can be provided by any modular floating 5.2V power supply; a floating supply is used to shift the usual MECL III logic signal levels of -0.8V and -1.6V to approximately 0V and -0.8V, compatible with the NIM standard.

2.1 - MECL III FLOGIC cards

Figure 1 shows a MECL III FLOGIC card in which you can see the strip-line input and output fast signal lines required by the nominally 1 ns signal transition speed of the I.C.'s. Output signal strip-lines have a characteristic impedance (Z_o) of 50Ω; they are the four wide strip-lines on the card. Pulldown resistors of 180Ω for each of these outputs are located adjacent to the I.C. Inputs, the eight narrow strip-lines, are run at 100Ω Z_o to conserve on printed surface area; these lines are shunted with 100Ω resistors at the card-edge to terminate the 50Ω input coax, and are terminated at the I.C. with a 100Ω strip-line match. As a shadow, you can see the plane conductor surface on the reverse side of the card that serves as reference for the strip-lines. The lower portion of this plane surface is at common potential, but the upper portion is at -4.4V, V_{ee}, as required for the stud connection on the I.C. A row of capacitors provides a.c. signal continuity across these two plane surfaces. The remaining trace is the +0.8V, V_{cc} conductor.

2.2 - DIAD Connectors

Figure 1 also shows the interconnecting hardware. Inexpensive Termi-point clips are solder-mounted onto the small printed pads shown at the top of the figure to produce DIAD connectors as shown in front and rear views in Fig. 2. The pads have a plane surface on one side, to which the coax braid is referenced. On the other side, to which the Termi-point clips are soldered, a strip-line is printed as the signal conductor. A capacitive mismatch at the clip end of the DIAD, caused by the very presence of the clips, is used to advantage. It is trimmed, by voiding a section of the rear plane surface, to just combine with a small inductive lump in the rearward pin extension of the Termi-twist connector socket contact and a capacitive lump at the forward extension of the contact (due to dielectic effects of the connector block) to provide a C-L-C lumped constant section of 50Ω line with transit

*Work done under the auspices of USAEC
**Motorola Semiconductor Products, Inc.
Phoenix, Arizona, U.S.A.

*AMP Incorporated, Harrisburg, Pennsylvania, U.S.A.
**Data Technology, Corp., Palo Alto, California, U.S.A.

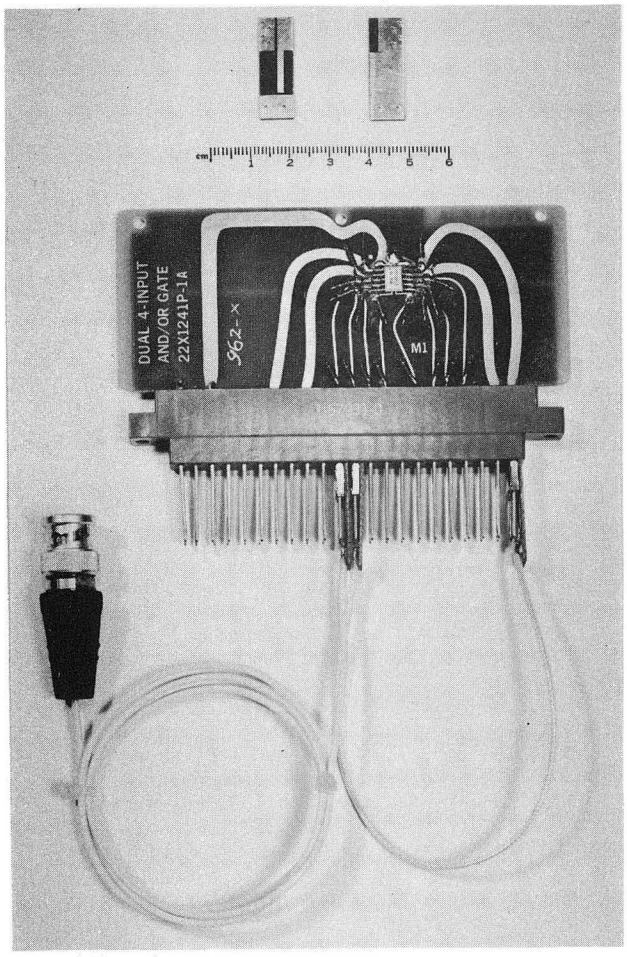


Fig. 1. MECL III Flogic System Components

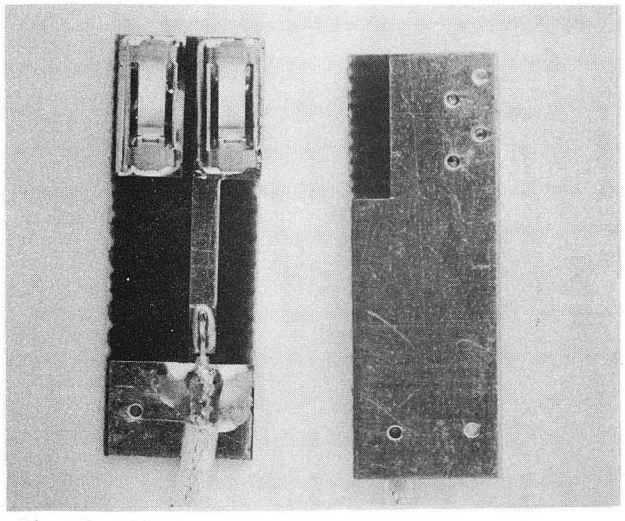


Fig. 2. DIAD Connector for MECL III FLOGIC System

time short enough to be inconsequential to the 1.2 ns rise-time signal out of the MECL III I.C.'s, when driving a 50Ω load. Tests show this compensated DIAD connector to pass a 200 ns 10-90% rise-time signal with undetectable deterioration of 10-90% rise-time, whereas an uncompensated version, with the same Termi-point clip, deteriorates the 200 ps 10-90% rise-time to 700 ps.

2.3 - A FLOGIC Instrumented Experiment

An experiment implemented early in the development of the MECL III FLOGIC System is shown in Fig. 3. This Figure, in addition to showing MECL III FLOGIC in use, demonstrates the compatibility of MECL III FLOGIC with the earlier FLOGIC work by this group (op.cit.) utilizing MECL II I.C.'s. When so configured, the system speed is limited by the slower MECL II components and commensurate liberties can be taken with matching the strip-line impedance from the MECL III FLOGIC cards. The modularity of the system is emphasized in the figure by cross-hatching the sections of the diagram at FLOGIC card boundaries.

In this experiment the input signals are received from discriminators which transmit standard NIM fast signal levels. At the inputs, eight "A" Gamma counter signals are ANDED with the corresponding eight "B" Gamma counter signals. Three distinct logical operations are performed:

1) $A_i \cdot B_i$ --- a single-shot output pulse is provided as shown at the top center for each $\Gamma(A_i) \cdot \Gamma(B_i)$ coincidence "hit".

2) $(A_i \cdot B_i) \cdot (A_{(i+1)} \cdot B_{(i+1)})$ --- a coincidence "hit" on any two adjacent Γ-Γ counters is recognized, as shown in the upper-right of the figure.

3) $\Sigma(A_i \cdot B_i)>1$, $\Sigma(A_i \cdot B_i)>2$, $\Sigma(A_i \cdot B_i)>3$ --- three outputs provide the analog OR'd sums of $A_i \cdot B_i$ "hits", as shown in the right-hand outputs.

Top and bottom views of this system bin are shown in Figures 4 and 5 respectively. Notice that only two-thirds of bin capacity is required to provide the logic for this experiment. Notice also that the hardware is particularly well suited for providing specialized circuitry; cards can be easily bread boarded and installed in the card-edge connectors. Following this experiment, the interconnections can be removed, and the cards and chassis will then be available for the next experiment. (New front and rear panels will have to be provided.)

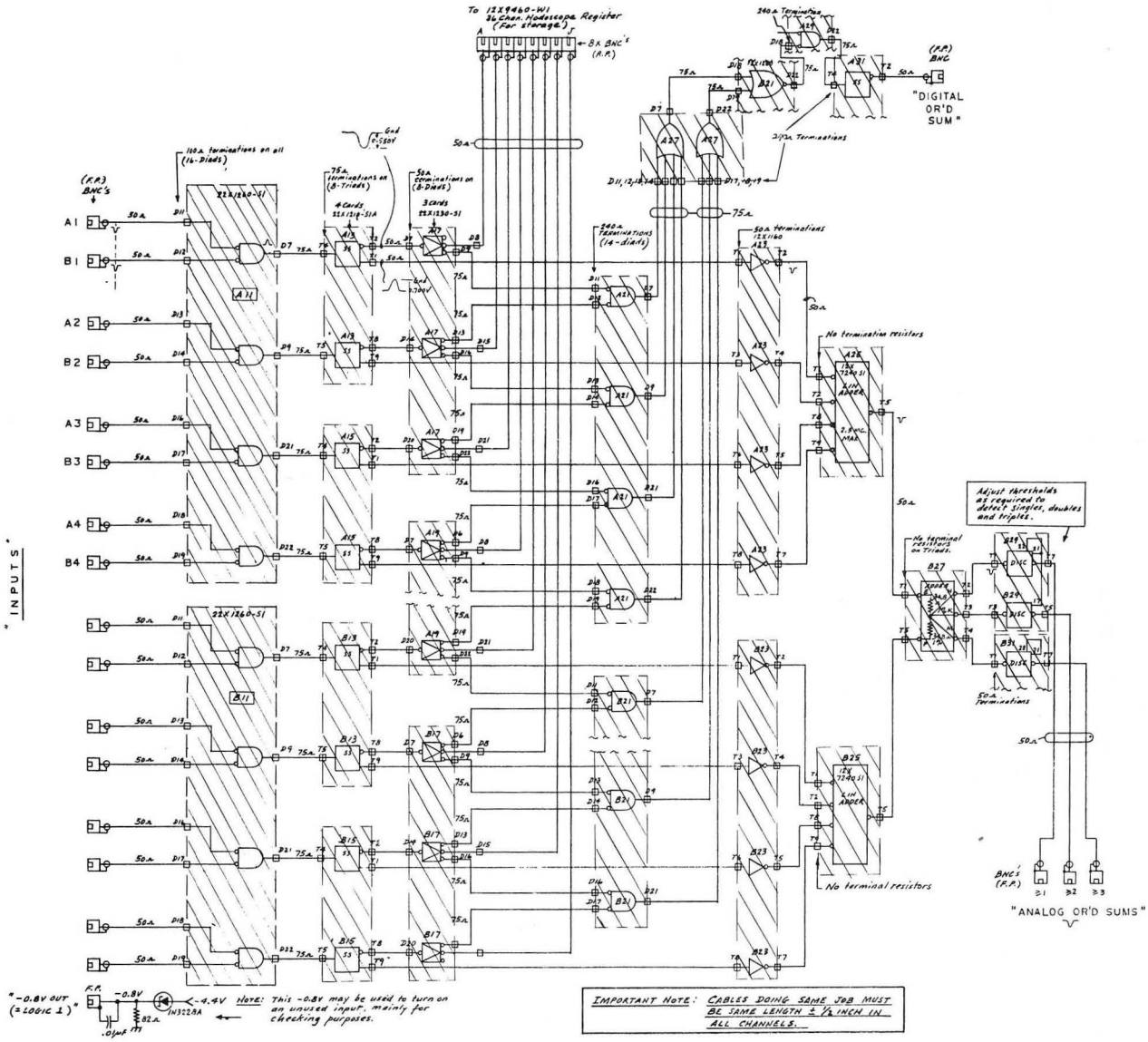


Fig. 3. Γ-Γ Experiment, FLOGIC Circuits Diagram

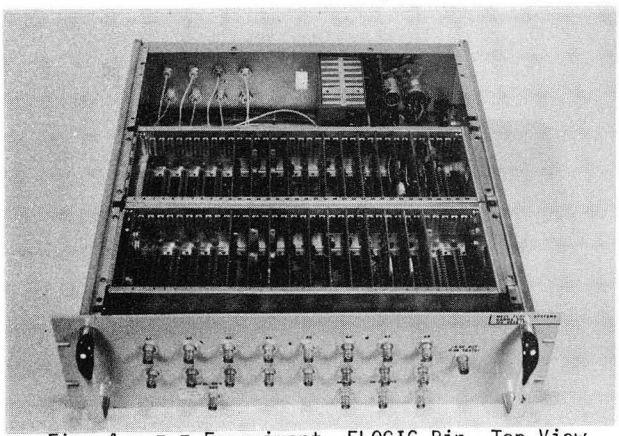


Fig. 4. Γ-Γ Experiment, FLOGIC Bin, Top View

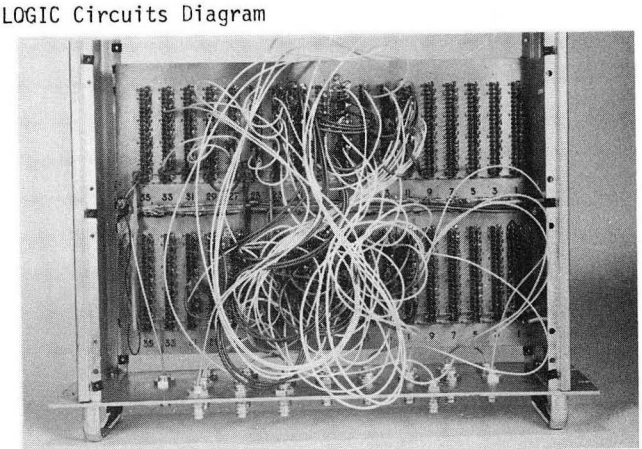


Fig. 5. Γ-Γ Experiment, FLOGIC Bin, Bottom View

3.0 - NIM Standard MECL III Fast Logic Modules

A series of 300 MHz Nuclear Instrumentation modules utilizing MECL III I.C.'s has been built that offers NIM standardized signal levels and hardware packaging conveniences to the user. A circuits building block concept has been employed in the design of these modules. Four functional circuits, Input Level Shifter, Pulse Standardizer, Retriggerable One-Shot, and Output Level Shifter are the structural elements which are appropriately combined and supplemented with special function circuits to generate the various NIM fast logic modules.

The performance specifications for the MECL III Fast Logic Modules: repetition rates to > 300 MHz; output rise-time, < 0.9 nsec; output fall time, $\leq$ 1.2 nsec; minimum coincidence overlap, 0.7 nsec above threshold; and coincidence resolution edges for 1000:1 count rate, $\leq$ 40 ps are in keeping with the capabilities of the MECL III I.C.'s. Additional specifications include: signals standardized to NIM levels, inputs protected against short transients to +100V (d.c. to +3.5V) and power requirements satisfied by the standard NIM type IV (+6V, +12V) power supply. MECL III Fast Logic Modules designed to date are displayed in Fig. 6.

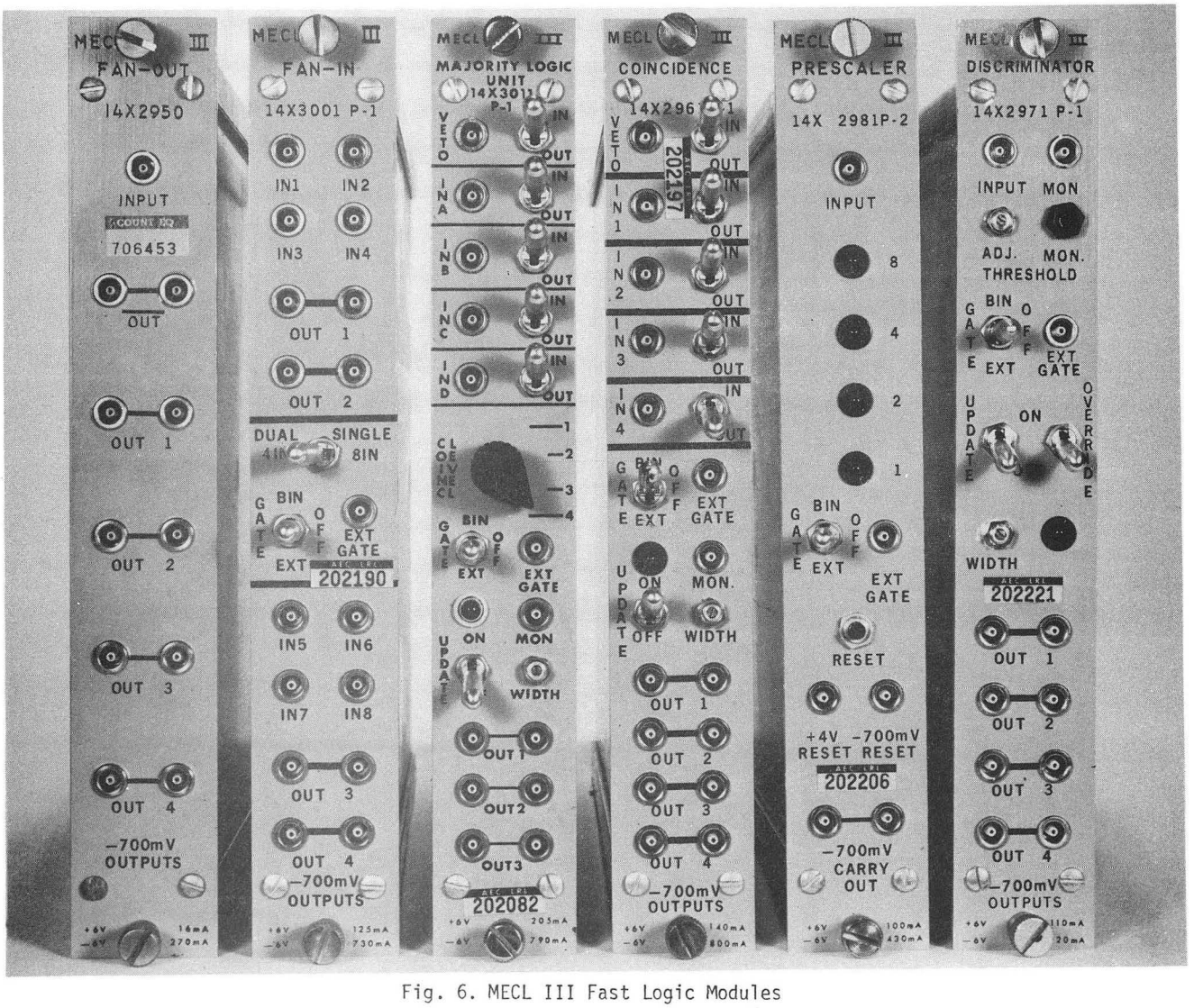


Fig. 6. MECL III Fast Logic Modules

3.1 - Circuit Building Blocks

The details of the four basic circuits used as building blocks in the design of MECL III Fast Logic Modules are presented in an earlier report.[3] The general characteristics of the circuit building blocks are:

3.1.1 - Input Level Shifter Active semiconductor junctions provide level shift between the center of the NIM fast signal levels and the center of the unique MECL III signal levels associated with the -6V V_{EE} used in these modules. Except under extreme overload conditions, when these junctions turn off to protect the MECL III I.C.'s, these active junctions pass 1 ns signals with negligible deterioration.

3.1.2 - Pulse Standardizer A pulse standardizer uses the regenerative characteristics of a MECL III flip-flop and the stability characteristic of coaxial cables to provide output pulses of precise shape; independent of input rise-time and input width.

3.1.3 - Retriggerable One-Shot Output pulse widths over the range of 3 ns to 100 ns are achieved by the use of a wide-range active current pump and a charging capacitor. The charging cycle is initiated by "dumping" the capacitor with a standardized input pulse to a clamped level; thus stability and retriggerability are achieved.

3.1.4 - Output Level Shifter NIM outputs are provided from the collector of a transistor current switch. Twice NIM standard currents are switched into two parallel outputs; allowing one either to drive two circuits or to clip the output signal with a shorted transmission line on one output.

3.2 - Recent Module Developments

The Discriminator and the Majority Logic Unit shown in Fig. 6 have recently been developed to fill out the selection of MECL III Fast Logic Modules. The building block approach is evident in the block diagrams of these modules, Figures 7 and 8. Clearly from these block diagrams, there is but one functional element in each that distinguishes between the two devices.

To show the actual circuits used as building blocks, the schematic of the MECL III discriminator is presented as Fig. 9. In the S-2 (lower) portion of this schematic, the two 12" cables and flip-flop, M3, identify the Pulse Standardizer section. Current pump Q15 and capacitor C35 identify the Retriggerable One-Shot section. Output Level Shifters are evidenced by the current switching output transistors. Details on the theory of operation of these circuits can be obtained from the original works (op.cit.). The discriminator input circuit is modified from the standard building block circuit to provide the exceptional speed and the critical offset balance required in a 50 mV broadband discriminator. The Schmitt tunnel diode discriminator is, of course, unique to this module.

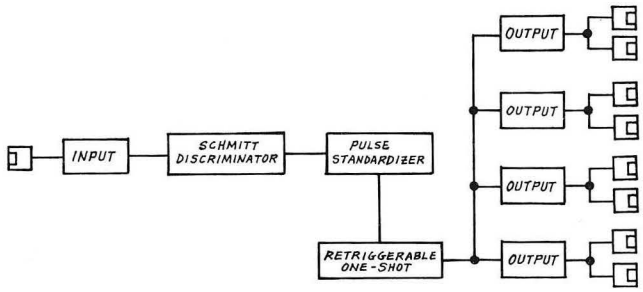


Fig. 7. MECL III Fast Logic Discriminator Block Diagram

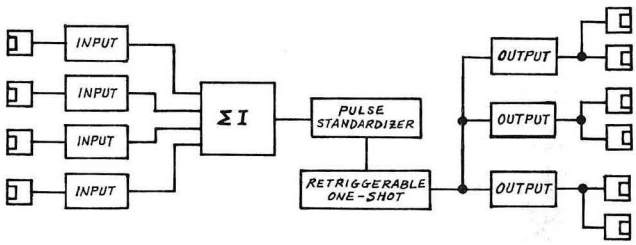


Fig. 8. MECL III Fast Logic Majority Logic Block Diagram

Figure 10 shows the standard Input Level Shifter building block circuit as the input to the MECL III Majority Logic Unit. The two input diodes and the base-emitter junction of the first transistor comprise the protection and active level shift components. A clever utilization of the MECL III output transistor as one-half of a current switch in the majority logic summing section (M1a and Q6, for example) is shown in this figure. Beyond Q10, the circuits are of the common building block variety.

3.3 - Input Circuit Component Selection Although it is the intent of this paper to present only the concepts of the utilization of MECL III for High Energy Physics Instrumentation, a particularly significant detail has come to light that should be mentioned for the benefit of those contemplating the use of the input level shifters in this or in similar applications. It has been found that the diodes used for input protection and level shift have I-V characteristics that vary from production batch to production batch: within any given batch they appear to be fairly consistent. Therefore the self-explanatory nomogram, Fig. 11, has been designed to aid in the proper selection of resistors which, with these diodes, establish input offset and provide signal level shift.

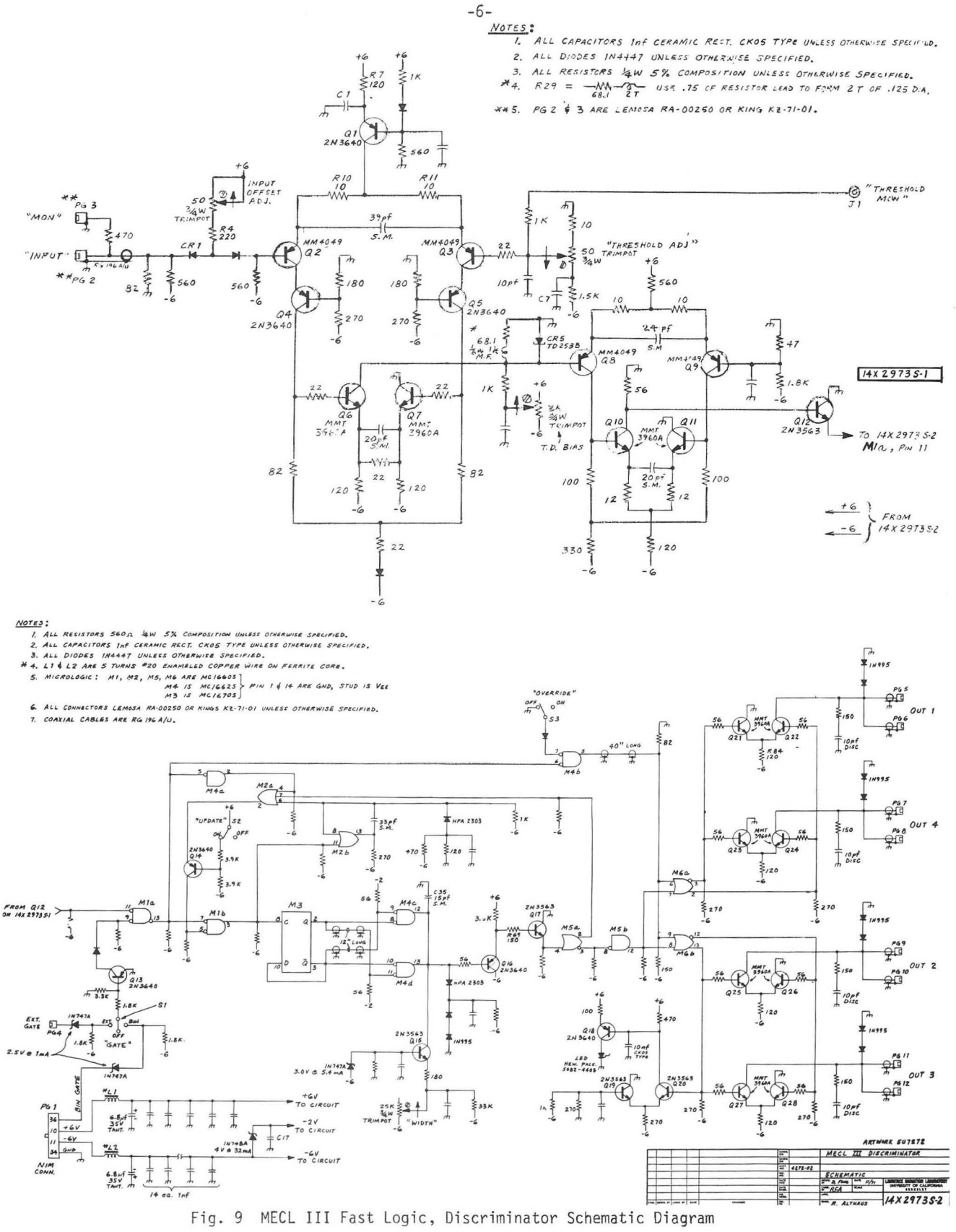


Fig. 9 MECL III Fast Logic, Discriminator Schematic Diagram

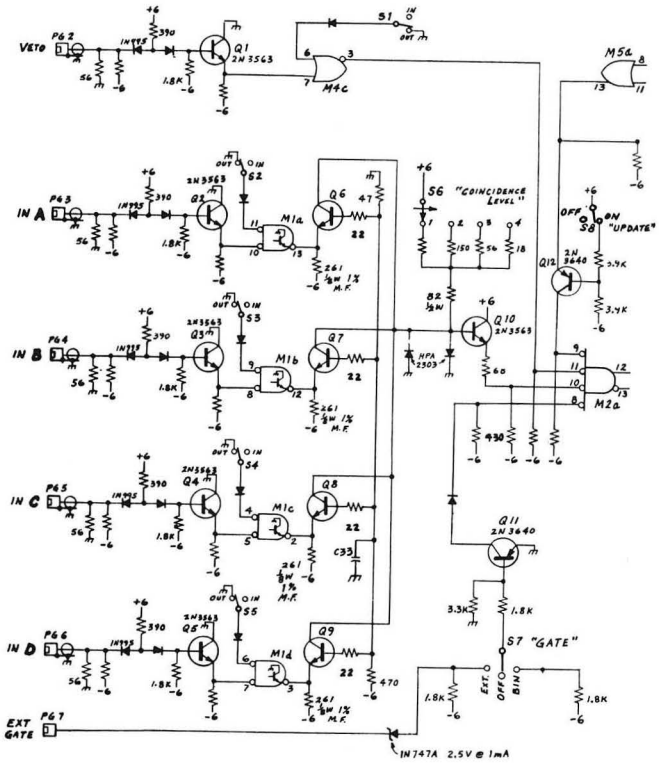


Fig. 10. MECL III Fast Logic, Majority Logic Input Section Schematic Diagram

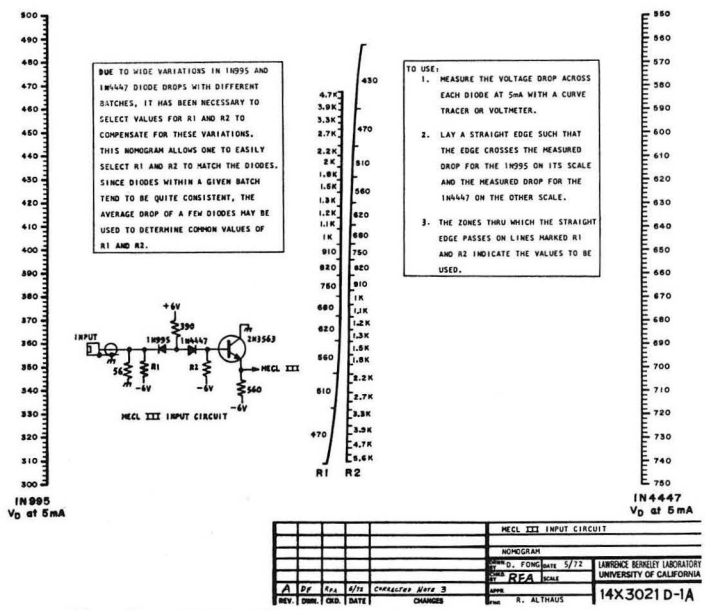


Fig. 11. MECL III Fast Logic, Input Section - Resistor Selection Nomogram

REFERENCES

1) F. A. Kirsten and D. A. Mack, System of Fast Integrated Circuit Logic for Physics Instrumentation, International Symposium on Nuclear Electronics, Versailles, France, Sept. 1968, pp 55-1 to 55-12.

2) AEC Committee on Nuclear Instrument Modules, Standard Nuclear Instrument Modules, TID 20893 (Rev. 3), U.S. Atomic Energy Commission, December 1969.

3) R. F. Althaus and L. W. Nagel, NIM Fast Logic Utilizing MECL III Integrated Circuits, IEEE Trans. on Nuclear Science, NS-19, No. 1, Feb. 1972, pp 520-525.

TECHNICAL INFORMATION DIVISION
LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720