DC Link Capacitor Ripple Constraints Limit the Benefits of Utility-Owned Four-Wire Power Converters

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Suggested Citation

M. Deakin, X. Deng, S. Odhano, and R. Heidari, "DC Link Capacitor Ripple Constraints Limit the Benefits of Utility-Owned Four-Wire Power Converters," in *Proceedings of the PowerUp Conference*, 2026.

BibTeX Entry

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@inproceedings{deakin2026dclink,
  author = {Deakin, Matthew and Deng, Xu and Odhano, Shafiq and Heidari, Rahmat},
  title = {{DC} Link Capacitor Ripple Constraints Limit the Benefits of Utility-
      Owned Four-Wire Power Converters},
  booktitle = {Proceedings of the PowerUp Conference},
  year = {2026},
}
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DC Link Capacitor Ripple Constraints Limit the Benefits of Utility-Owned Four-Wire Power Converters

Matthew Deakin, Xu Deng, Shafiq Odhano and Rahmat Heidari

***Abstract*—Utilities are increasingly interested in power converters to increase the headroom of their assets by actively controlling power flows on their network. In this work we demonstrate that thermal limits of dc link capacitors can result in substantially diminished benefits of these converters under unbalanced operation, due to constraints on neutral current and double-line frequency power ripple. Considering nine voltage source converter topologies with varying ripple capabilities, the upper bound (in terms of additional headroom released) increases by more than 80% compared to a no-ripple case for the application of phase current unbalance mitigation.**

***Index Terms*—Phase balancer, voltage source converter, dc link ripple, capacitor sizing, distribution network**

I. Introduction

Power converters are achieving ever-increasing power density and cost-effectiveness, driven by a huge range of applications including electric vehicles, motor drives, and battery storage systems. Distribution system operators are therefore exploring how these next-generation power converters could be exploited to avoid disruptive and costly traditional reinforcement as electrification continues to gather pace. Power converter-based technologies which are being explored by utilities include back-to-back soft open points, STATCOMs, and hybrid transformers.

As a result of these new applications, there has recently been interest in more accurate algebraic modeling of power converters. Aspects considered include physics-based loss modeling [1], consideration of controls on power quality impacts of power converters [2], or dc link capacitor ripple on operational constraints under unbalanced operation [3], [4].

This work focuses on the latter consideration of low-frequency dc link ripple (e.g., ripple components with frequency $< 50\omega$ rad/s, for fundamental grid angular frequency ω) under the injection of unbalanced currents. Low-frequency dc link ripple is caused by neutral return current, and double line frequency power oscillation as a result of time-varying active power injection.

The contribution of the work is to use analytic bounds on minimum and maximum dc link ripple values to conduct a parameter sweep that evidence, for a range of common voltage source converter (VSC) topologies, that dc link ripple substantially and consistently impacts on the benefits of VSCs for applications requiring unbalanced injections. As compared to recent works [3], [4], we consider benefits for a variety of topologies, considering the full range of capacitor sizes.

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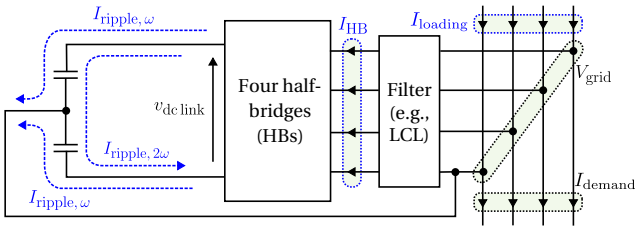

Fig. 1. A four-leg, four-wire VSC converter with split dc link. Quantities in blue are variables considered to change significantly with half bridge currents I_{HB} assigned by the VSC controller. For the purposes of this paper, the impact of the filter on current and voltage at line frequency is neglected, so the voltage and current at the input and output of the filter are equal.

a) Notation: Upper case variables represent phasors. Superscript $(\cdot)^*$ represents complex conjugate and $|\cdot|$ the magnitude of a complex number. The (angular) line frequency of the grid is ω. ϕ is used as a (subscripted) index for vectors which collect per-phase (or per-leg) quantities.

II. Voltage Source Converter Modelling with DC Link Ripple Constraints

Fig. 1 shows a model of a grid-connected four-wire, four-leg VSC with split dc link (the parallel fourth leg and split dc link splits the neutral current to reduce stress on each of those return paths). There are a range of topologies for the filter block (see, e.g., [5]): for the purposes of this work, we assume the filter is primarily introduced to mitigate high-frequency ripple components, with little voltage drop or current transfer between phases, so the voltage drop between the half-bridges and grid at low frequency is negligible. Similar topologies to Fig. 1 are also common, such as three-leg, four-wire topologies (i.e., with only three half bridges [3]), or for four-leg four-wire topologies with monolithic dc link (i.e., the dc link has only a single capacitor between upper and lower rails, with no midpoint [4]).

A. Basic Voltage Source Converter Constraints

For any four-wire VSC topologies, current injections into the half bridge legs, I_{HB}, must be limited according to the thermal rating of semiconductor devices $I^{\text{Max}}_{\text{HB},\phi}$, i.e.,

$$|I_{\text{HB},\phi}| \leq I^{\text{Max}}_{\text{HB},\phi} \quad \forall\, \phi \in \Phi\,, \tag{1}$$

where Φ represents the set of half-bridge legs. If there is no dc-side source capable of providing active power, then

$$\sum_{\phi} V_{\text{grid},\phi} I^*_{\text{HB},\phi} = 0\,, \tag{2}$$

where V_{grid} is the vector of grid voltages at the point of common coupling. For the purposes of this work, this grid

voltage is assumed to be dominated by a nominal positive sequence voltage only, i.e.,

$$V_{\text{grid}} = V_{\text{grid}}^{\text{phase}} \, [1,\, \alpha^{-1},\, \alpha^{-2},\, 0\,]^{\intercal} \,, \tag{3}$$

where $\alpha = e^{2\pi/3}$ is the 120° phase rotation operator and $V_{\text{grid}}^{\text{phase}}$ is the nominal phase voltage.

B. Voltage Source Converter Capacitor Ripple Constraints

For VSCs injecting line-frequency currents, low-frequency ($< 50\omega$) dc link (capacitor) ripple is dominated by line frequency neutral return current and double-line frequency power ripple. Line frequency neutral current occurs only when the dc link has a split-capacitor topology, so that neutral current can return through the midpoint between the capacitors (shown as $I_{\text{ripple},\,\omega}$ on Fig. 1). Assuming dc link capacitors of equal capacitance and balanced charge, then the line-frequency neutral current ripple is shared between capacitors equally [3],

$$I_{\text{ripple},\,\omega} = \frac{1}{2} \sum_{\phi} I_{\text{HB},\,\phi} \,. \tag{4}$$

Double-line frequency power ripple occurs as a result of non-cancellation of active power ripple across phases under unbalanced power injections. The general form for this power ripple $P_{\text{ripple},\,2\omega}$ is [4]

$$P_{\text{ripple},\,2\omega} = \left| \sum_{\phi} V_{\text{grid},\,\phi} I_{\text{HB},\,\phi} \right| \,, \tag{5}$$

so, for a known dc link voltage $v_{\text{dc link}}$, the current ripple is

$$|I_{\text{ripple},\,2\omega}| = \frac{\left| \sum_{\phi} V_{\text{grid},\,\phi} I_{\text{HB},\,\phi} \right|}{v_{\text{dc link}}} \,. \tag{6}$$

The impact of ripple currents on the thermal load of the capacitor is modeled via its equivalent series resistance (ESR), r, so that for each harmonic k,

$$\begin{aligned} \text{Thermal Load} &= r \sum_{k} |I_{\text{ripple}}(k\omega)|^2 \\ &= c_{\text{Sw.}} + r \left(|I_{\text{ripple},\,\omega}|^2 + |I_{\text{ripple},\,2\omega}|^2 \right) \,, \end{aligned} \tag{7}$$

where $c_{\text{Sw.}}$ represents losses due to high-frequency (low-energy) switching ripple from high frequency half-bridge pulse width modulation (PWM), and the line and double-line frequency components $I_{\text{ripple},\,\omega}$, $I_{\text{ripple},\,2\omega}$ are from (4), (6). For a given maximum thermal load, the maximum allowed ripple currents through the capacitor can be limited. Defining

$$(I_{\text{ripple}}^{\text{Max}})^2 = \frac{\text{Thermal Limit} - c_{\text{Sw.}}}{r} \tag{8}$$

then assigning Thermal Limit as the upper bound for (7) yields

$$|I_{\text{ripple},\,\omega}|^2 + |I_{\text{ripple},\,2\omega}|^2 \leq (I_{\text{ripple}}^{\text{Max}})^2 \,. \tag{9}$$

The voltage ripple at a given frequency ω can be determined according to the fundamental capacitor relation $C = Q/V$ for the known current ripple, with constraints included for each frequency [3]. For the remainder of this work, we focus on thermal constraints of the form (9).

C. Maximum DC Link Ripple Current Design

Considering (9), it is possible to determine an upper bound on the maximum theoretical ripple capacity $I_{\text{ripple}}^{\text{Max}}$ for a given converter leg capacity $I_{\text{HB}}^{\text{Max}}$. Considering the grid voltage (3), the negative sequence current injection is the only injection which will increase the value of the current ripple (6). The maximum value of the double-line frequency current ripple $I_{\text{ripple},\,2\omega}$ will take value of the kVA rating of the converter divided by the dc link voltage. For a sinusoidal pulse width modulation (SPWM) scheme, the dc link voltage should be a minimum of $2\sqrt{2}$ that of $V_{\text{grid}}^{\text{phase}}$; a dc link voltage $v_{\text{dc link}} = 3V_{\text{grid}}^{\text{phase}}$ has headroom of 6%. Therefore, noting that a fourth leg does not contribute to active power ripple (as it is at 0 V, from (3)), and considering (1) and (6), the maximum value of $|I_{\text{ripple},\,2\omega}|$ takes value

$$|I_{\text{ripple},\,2\omega}| \leq \frac{1}{3} \sum_{\phi=\{1,\,2,\,3\}} I_{\text{HB},\,\phi}^{\text{Max}} \,, \tag{10}$$

for any permissible value of I_{HB} (1).

The maximum line-frequency ripple $|I_{\text{ripple},\,\omega}|$ occurs when all legs inject currents I_{HB} with identical phase angle, so for any I_{HB},

$$|I_{\text{ripple},\,\omega}| \leq \frac{1}{2} \sum_{\phi} I_{\text{HB},\,\phi}^{\text{Max}} \,. \tag{11}$$

To consider the maximum ripple $I_{\text{HB}}^{\text{Max}}$ across all I_{HB}, note that (9) can considered a weighted squared 2-norm of the zero- and negative-sequence current injections (from (10), (11)). However, given that sequence components are orthogonal, the maximum ripple current $I_{\text{ripple}}^{\text{Max}}$, is the maximum of the individual ω, 2ω ripple currents. As a result, we can write down that

$$0 \leq I_{\text{ripple}}^{\text{Max}} \leq \frac{1}{2} \sum_{\phi} I_{\text{HB},\,\phi}^{\text{Max}} \,. \tag{12}$$

Given (12), it is possible to consider how dc link capacitors impact on converter benefits across the full range of reasonable capacitor thermal capacities.

D. Operational Constraints for three-leg, four-leg, and reconfigurable VSCs

The operating constraints considered in this work are for three different half-bridge configurations, as follows.

a) Three-leg VSC: The VSC's operational constraints are given by (1), (2), (3), (4), (6), and (9), with the set of leg phases $\Phi = \{1,\, 2,\, 3\}$. All three legs have the same capacity, $I_{\text{HB},\,\phi}^{\text{Max}} = I_{\text{HB}}^{\text{Total}}/3$.

b) Four-leg VSC: A four-leg VSC has the same operational constraints as for a three-leg VSC, but has $\Phi = \{1,\, 2,\, 3,\, 4\}$. Each leg is assumed to have the same current carrying-capacity, $I_{\text{HB},\,\phi}^{\text{Max}} = I_{\text{HB}}^{\text{Total}}/4$, with the fourth leg enabling reduced line frequency (neutral) current ripple $I_{\text{ripple},\,\omega}$.

c) Reconfigurable VSC: Finally, to consider other possible half-bridge capacity sizes, we consider the VSC leg capacity convex relaxation introduced for reconfigurable VSCs [6]. This relaxation provides a continuous approximation of a (discrete) power multiplexer that enables the output of half

bridges to be connected to different phases [7]; therefore, on a per-unit basis, this relaxation provides an upper bound to VSC performance under any leg sizing. This topology still considers constraints (2), (3), (4), (6), and (9), but replaces (1) with the convex relaxation

$$\sum I_{\mathrm{HB}} \leq I_{\mathrm{HB}}^{\mathrm{Total}} . \tag{13}$$

E. Application: Phase Current Balancing

Typically, thermal constraints on distribution system assets are binding on a per-phase basis. Therefore, by balancing the unbalanced demand I_{demand} (imbalance caused by, for example, single-phase domestic loads), the per-phase asset loading I_{loading} can be reduced, increasing the headroom of a distribution system asset. The benefit of a VSC at a time τ for a VSC is

$$\mathrm{Benefit}_{\tau} = \left(\max_{\phi} |I_{\mathrm{loading},\,\phi}^{\mathrm{No\ VSC}}| \right) - \left(\max_{\phi} |I_{\mathrm{loading},\,\phi}^{\mathrm{With\ VSC}}| \right) . \tag{14}$$

For demand I_{demand} at time τ, the objective is to minimize the maximum phase current (i.e., maximising the benefit (14)), as

$$\min_{I_{\mathrm{HB}}} \quad \left(\max_{\phi} |I_{\mathrm{loading},\,\phi}^{\mathrm{With\ VSC}}| \right) + \lambda \|I_{\mathrm{HB}}\|_2 , \tag{15}$$

with constraints on I_{HB} described in Section II-D for each of the three VSC topologies considered; regularization parameter $\lambda \ll 1$ ensures a unique solution in I_{HB} is found (and can be considered a proxy as a secondary objective to minimize converter losses).

By solving (15) at each time period τ, the additional headroom can be found using each solution $I_{\mathrm{HB}}(\tau)$ to find

$$\begin{aligned} \text{Additional Headroom} = &\left(\max_{\phi,\,\tau} |I_{\mathrm{loading},\,\phi,\,\tau}^{\mathrm{No\ VSC}}| \right) \\ &- \left(\max_{\phi,\,\tau} |I_{\mathrm{loading},\,\phi,\,\tau}^{\mathrm{With\ VSC}}| \right) . \end{aligned} \tag{16}$$

III. Results

To study how dc link ripple affects the benefits provided by a VSC, we use two weeks of data for a 500 kVA secondary substation based in the UK [8] (id: no. 110568). Fig. 2 shows the first full day of demand I_{demand}, showing that the additional headroom at peak demand on this day could be 60 A (greater than 20% headroom released). Phase angles of the demand currents have an average of 120° lag between phases, with a small random angle offset at each time τ (normally distributed with zero mean and standard deviation $\pi/15$) to account for time-varying demand power factors. The optimization problems are solved with cvxpy [9], [10].

To study the impact of dc link ripple constraints, we consider three-, four-, and relaxed reconfigurable-leg cases (Section II-D) across VSCs with total leg capacities $I_{\mathrm{HB}}^{\mathrm{Total}}$ of:

- 150 A, with split dc link (Case (i), 36 kVA);
- 150 A, with monolithic dc link (Case (ii), 36 kVA);
- 30 A, with split dc link (Case (iii), 7.2 kVA).

An example of the solution of (15) across time for Case (i) is shown in Fig. 3. This shows how a case with no ripple capabilities (left subfigure) is restricted to inject only balanced currents, as the VSC does not have the ripple capacity required to inject zero- or negative-sequence currents. In contrast, when there is a large dc link ripple capability (right subfigure), the VSC is able to inject unbalanced currents that track the unbalance seen in the load. As a result, when the unbalanced load peaks at 18:00, the VSC can draw power from phase b and inject it into phase c, effectively mitigating the high currents, as in Fig. 2 (right subfigure).

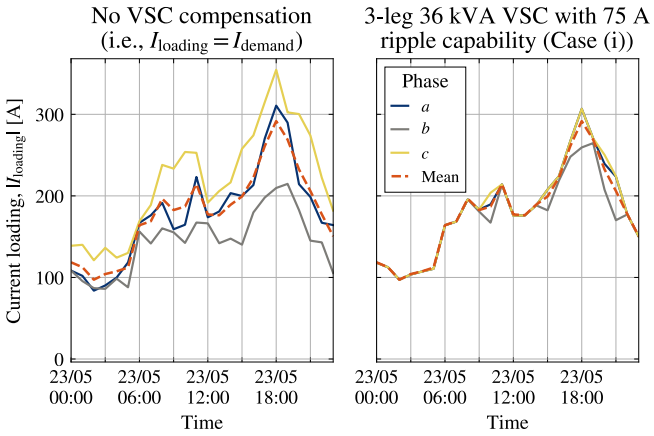

Fig. 2. Loading I_{loading} for the first full day of data, in the case of no VSC injections (left), and a 36 kVA 3-leg VSC with split dc link (Case (i)) and a 75 Arms capacitor ripple current capabilities (right).

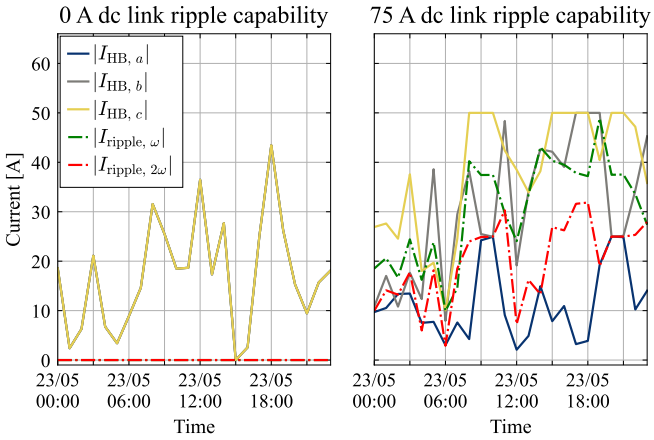

Fig. 3. Injected currents for a 36 kVA three-leg VSC with split dc link (Case (i)), considering 0 A dc link ripple current capabilities (left) vs full dc link ripple capability of 75 A (right).

A. Benefits for a Large VSC with Split DC Link (Case (i))

Fig. 4 shows the Benefit (14) and Additional Headroom (16) for the full range of dc link ripple capabilities (12). It can be seen that, as expected, the benefits increase monotonically as the dc link ripple capability $I_{\mathrm{ripple}}^{\mathrm{Max}}$ increases. Furthermore, the change in capability plateaus as this value reaches the maximum ripple value of 75 A. Across all VSC configurations of Case (i), the dc link ripple $I_{\mathrm{ripple}}^{\mathrm{Max}}$ more than doubles the Additional Headroom benefit, showing how small dc link ripple capabilities severely restrict the benefits of the VSC.

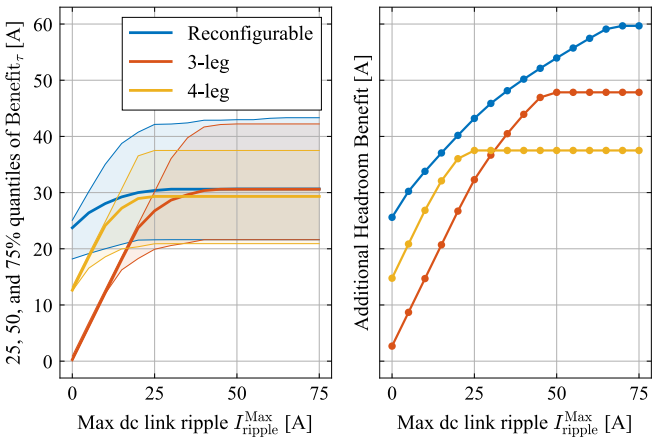

Fig. 4. Results for parameter sweep of the maximum dc link ripple $I^{\text{Max}}_{\text{ripple}}$ for Case (i), considering quartiles of the Benefit (14) across time τ (left) and for the Additional Headroom (16) across all τ (right).

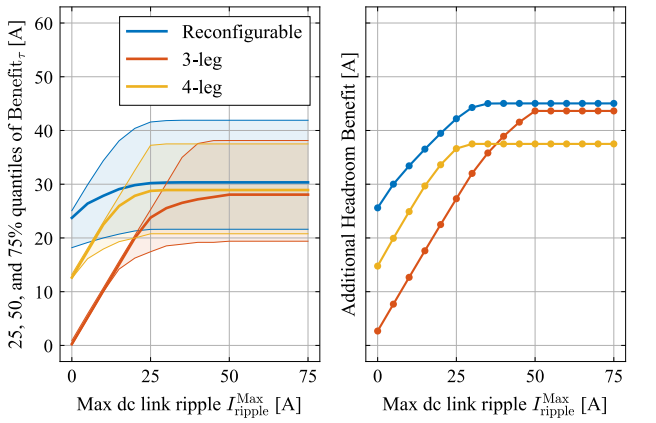

Fig. 5. Results for parameter sweep of the maximum dc link ripple $I^{\text{Max}}_{\text{ripple}}$ for Case (ii), considering quartiles of the Benefit (14) across time τ (left) and for the Additional Headroom (16) across all τ (right).

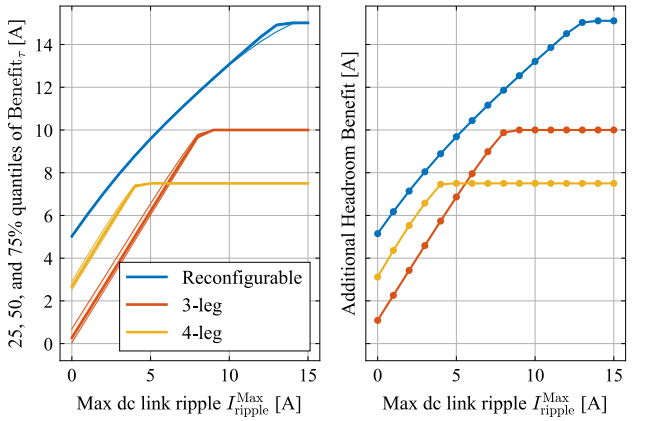

Fig. 6. Results for parameter sweep of the maximum dc link ripple $I^{\text{Max}}_{\text{ripple}}$ for Case (iii), considering quartiles of the Benefit (14) across time τ (left) and for the Additional Headroom (16) across all τ (right).

Comparing the three half-bridge configurations (Section II-D), it can be seen that, as expected, the relaxed reconfigurable VSC topology has the greatest Benefit and Additional Headroom. The 3-leg converter initially has low benefits, as it can only inject balanced power, whilst the 4-leg converter can use the neutral-connected leg to inject zero sequence current. However, as the dc link ripple capability $I^{\text{Max}}_{\text{ripple}}$ increases, the benefits of the 3-leg VSC surpass the 4-leg design, as the 3-leg VSC can exploit the dc link midpoint for neutral return (noting the 50 A legs for 3-leg design, versus 37.5 A for the 4-leg design).

B. Benefits for a Large VSC with Monolithic DC Link (Case (ii)) and Small VSC with Split DC Link (Case (iii))

Qualitatively, results for Case (ii) mirror those of Case (i), as shown in Fig. 5. The main difference between is that the Additional Headroom is somewhat reduced, and that the dc link capacitor ripple $I^{\text{Max}}_{\text{ripple}}$ does not increase beyond 50 A. This is because there is no neutral return for a monolithic dc link capacitor, so the applicable upper capacitor limit is limited by (10) (i.e., 50 A) rather than (12). The difference between the minimum and maximum Additional Headroom is smaller than Case (i), but still 80% or greater across the three half-bridge configurations.

Finally, Fig 6 shows the results for Case (iii), whereby the VSC capacity on each leg is significantly smaller than the unbalance in the network. As a result, all three half-bridge configurations show benefits that show a smaller spread across the time-varying benefits (left subfigure), as the VSC saturates its outputs at most time periods. In this case, the Additional Headroom benefit (right subfigure) shows an even greater difference in benefits than either of the other two Cases.

IV. Discussion and Conclusions

Conventional VSC models only consider per-phase current and power constraints (1), (2), therefore requiring only two model parameters. In this work, we provide evidence that neglecting capacitor ripple constraints risks an inadequate model for VSCs injecting unbalanced currents, with the *minimum* difference in converter overall benefits across nine topologies having value of 80%. This suggests that these more detailed converter models are necessary.

Nevertheless, the assumptions considered in this work could be further studied to consider how they interact with the ripple constraints considered. This includes dc link voltage ripple; the effect dc link-connected active power sources; impacts of different output filter topologies; or alternative topologies such as multilevel converters. This would enable a more comprehensive study of the tradeoff between complexity and fidelity for different applications.

Conversely, utilities could develop libraries of example mission profiles for these emerging use-cases, which are non-trivial due to these converter's multiport structure. These would enable power converter topology and design to be co-optimized, improving competitiveness against alternative solutions. We conclude that utility-owned power converters are of particular interest (as compared to customer-owned converters), given their topology, design, and control can be influenced by system operators, ultimately enabling detailed converter models to be accurate and of high value.

AI Usage Disclosure Statement

AI was not used in the research or writing of this paper.

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I. Review #11A

A. Paper summary

This paper studies DC link capacitor sizing of three-leg and four-leg voltage source converters in four-wire distribution systems. The main contribution are analytic bounds that map thermal capacitor limits and switch thermal limits to ripple current limits. Then various common topologies are studied using feeder data to determine the benefit (measured as balancing load demand between phases) under various ripple current (i.e., capacitor size / ESR) limits.

B. Comments for authors

This is a very interesting topic that is often overlooked and needs further study to ensure that VSCs are sized appropriately to fully leverage their control capabilities in four-wire distribution. The main contribution are analytic bounds that map thermal capacitor limits and switch thermal limits to ripple current limits. Then various common topologies are studied using feeder data to determine the benefit (measured as balancing load demand between phases) under various ripple current (i.e., capacitor size / ESR) limits. Overall the contribution is good for a note paper but I have some concerns around the clarity of the presentation.

1) In Section II-A through II-C, it is not quite clear what data is used as a starting point for the calculations and what bound on which signal results from the calculations. My understanding is that, as a starting point, the thermal limit of the semiconductors $I_{\text{HB}}^{\max}$ is used. Then a maximum set for the thermal load on the capacitor is introduced after (7). However, because that thermal limit is never explicitly established the remaining derivation is somewhat unclear. I had to read it twice and now my understanding is that the authors use $c_{\text{sw}} + r$ (sum of squared ripple current) $\leqslant$ thermal limit. Then, $I_{\text{ripple}}^{\max}$ in (8) would be $(I_{\text{ripple}}^{\max})^2 = (\text{thermal limit})/r - c_{\text{sw}}$? Why not explicitly state this? Also, why is there a full stop in c_{sw}.? Then, in Section II-C, one basically sees that the 1/2 times the sum of thermal limits of the semiconductors need to be larger than $I_{\text{ripple}}^{\max}$ so that the converter can operate at the ripple current limit without the switches becoming the limiting factor. If this is correct, why not directly state it? Either way, this part of the presentation lacks clarity and precision.
2) The basic principle of the reconfigurable VSC from [6] used to enable the relaxation in (13) is unclear. The reader should not have to read [6] in detail to understand this result and the related results in Sec. III.
3) The abstract is inaccessible to non-experts and likely not understandable for a broader audience. It uses a lot of jargon that has not been introduced (soft open point, unconstrained DC ripple, etc.).
4) Why is there a connection between DC neutral for four-legged converters as well? Does that not significantly limit the capabilities of the four-legged converter? Without the DC midpoint grounding, the DC current ripple will heavily depend on the modulation scheme used for the four legs. However, it appears that this would be the more relevant case for the four-legged topology. I would have expected a DC midpoint point to neutral connection only for the three-legged converter.
5) I agree that thermal phase current limits are often the most crucial aspect in distribution systems as discussed in Section II-E. However, another way to look at it is the capability of the converter to correct three-phase voltage unbalance by compensating three-phase unbalanced load.
6) Overall this paper seems to be based on the premise that electrolytic capacitors are used for the DC link, i.e., that ESR is significant. Large film capacitors with negligible ESR are becoming available whose rating may suffice for distribution system applications.

C. Summarize your recommendation in one to two sentences

A solid paper on an interesting topic, but the presentation lacks clarity in some parts.

— Dominic Groß

II. Review #11B

A. Paper summary

This paper examines the impact of neutral current and double-frequency power ripples under unbalanced operation on the capacity of the dc-side capacitor to offer headroom benefits.

B. Comments for authors

Strengths:

+ Practical consideration in VSC design given (high) likelihood of distribution-level phase imbalance.
+ Use of real-world data for substation based in the UK
+ Parametric sweep offers information regarding sensitivity and saturation of benefits

Weaknesses:

- There are a few inconsistencies in notation, specifically with respect to subscript ϕ and summation over ϕ. Sometimes they appear, e.g., (5) and (6), other times not, e.g., (4). Notation section further mentions that summations with no index are across ϕ.
- I find (14) unintuitive as it tries to /minimize/ the benefit as defined in (13). One generally would hope to maximize benefit.
- Fig. 5 is not referenced in the paper body, and it has identical caption as Fig. 4, yet the plots look different from Fig. 4.

C. Summarize your recommendation in one to two sentences

While there are a few minor errors / inconsistencies throughout the manuscript, overall I expect the main contribution to be of interest to those working at the intersection of power electronics and power systems. I recommend acceptance.

— Anonymous reviewer

III. Review #11C

A. Paper summary

This work uses analytic bounds on minimum and maximum dc link ripple values to conduct a parameter sweep that evidence, for a range of common VSC topologies, that dc link ripple impacts the benefits of VSCs for applications requiring unbalanced injections.

B. Comments for authors

Please consider the following comments/suggestions:

- Make sure all terms are defined in the text (e.g., $I^*_{HB,\phi}$ is not defined)
- The work considers a good set of reconfigurable leg cases and leg capacity architectures, which allows drawing broad conclusions.
- Their conclusion "neglecting capacitor ripple constraints risks an inadequate model for VSCs injecting unbalanced currents" is very relevant for the community.
- The manuscript is well-written.

C. Summarize your recommendation in one to two sentences

Not provided by the reviewer.

— Patricia Hidalgo-Gonzalez

IV. Brief response to reviewers (optional)

We thank the reviewers for their time and efforts to review the paper. The "summary of changes" outlines the changes we have made to address the reviewer comments.

V. Brief summary of changes made to the final paper

We thank the reviewers and editors for their detailed review and constructive comments.

For the final version of the manuscript we have made the following changes.

- We have added authorship, affliliations, and funding.
- An additional equation has been added to streamline the derivation of the thermal limit considered in the results (comment 11A-1).
- Further detail has been added before (13) to briefly introduce the concept of a reconfiguable VSC (comment 11A-2).
- We have removed the STATCOM and Soft Open Point mentions in the abstract and reworded the sentence with regards to unconstrained dc link ripple (comment 11A-3).
- A sentence has been added to clarify the purpose of the parallel dc link capacitor and fourth leg (comment 11A-4)
- We have made explicit the index over summations, even when they are over ϕ (comment 11B-1).
- We have clarified the sense of the optimization objective (comment 11B-2).
- The appropriate link to Fig. 5 has been added to the text (comment 11B-3).
- We have indicated that indexes are subscripted (comment 11C).
- We have added the citations for cvxpy, which are used to solve the optimization problems.