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Radiation Analysis on Spin Transfer Torque Random Access Memory and Design of a Radiation Hardened Sense Circuit

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical Engineering

by

Saba Mohammadi

Dissertation Committee:
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DEDICATION

To my loving parents, Fatemeh and Mohsen.
I owe my education and success to their sacrifices.

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ABSTRACT OF THE DISSERTATION

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Spin transfer torque (STT-RAM) is a fast, scalable and non-volatile memory technology. These characteristics make STT-RAM one of the best candidates among memories that can be used for space applications. However, understanding of radiation effects on memory cells and the related circuitry is necessary to avoid failure in high radiation environment. Energetic gamma and neutron particles may strike on sensitive circuit nodes and induce a current by electron/hole pair generation. Radiation induced current potentially leads to read/write failures. In this work, we analyzed the effect of radiation on the STT-RAM sense circuit and proposed a radiation hardened circuit. The sense circuit is implemented in 45 nm $CMOS$ technology. Simulation results show that the proposed circuit is immune to radiation pulses up to 400 $Krad$.

Chapter 1

Introduction

Nowadays to increase the performance of computer systems, multi-core processors are integrated on a single chip. Having multiple cores that have access to the shared memory requires high speed memory technology. To increase the speed of memory, one solution is to investigate the increase in clock frequency, which is not efficient in terms of power. Also as the technology scales down, especially above 10 nm, conventional on-chip memory technologies (SRAM, DRAM,) lack reliability and consume large power due to leakage current. So, the need for a fast and nonvolatile memory technology is vital.

Another important issue with the memory technologies that work based on storing electric charge is their vulnerability to radiation. In particular, for space applications and environment with high dose of heavy ions and charged particles, a radiation hard memory technology is required.

Spin Transfer Torque Random Access Memory (STT-RAM) is an emerging non-volatile technology that has attracted a lot of attention in recent years. Non-volatility and low leakage power of STT-RAM, makes it a great candidate to be used for on chip cache memory. STT-RAM works the best for space applications, because of the intrinsic radiation hardness

of its memory cells[4].

1.1 Limitations of Current Memory Technologies

Studying the currently used memory technologies, researchers found a vital need for a non-volatile, power efficient and fast memory. In this section, we discuss why STT-RAM is a superior technology compared to previously used memories.

Conventional memory technologies such as SRAM, DRAM and NAND flash, are used in many applications. These technologies are called capacitive memories since they store data in the form of electric charge. SRAM is a volatile memory which is mostly used in on chip caches, because of its low access time. As the technology scales down, the amount of charge that can be stored in a device decreases. This makes it easier for a bit to flip and leads to reliability issues. The lack of reliability raises severe problems in computer systems, particularly in space applications where a high dose of radiation is present in the environment. DRAM is another capacitive memory that is vulnerable to radiation. DRAM is vastly used in the main memory because of its relatively high speed and low price. However, the leakage current of DRAM cell makes it a power hungry memory that requires periodic power consuming refreshments. Non-volatile NAND flash is also susceptible to radiation induced reliability issues. this memory is usually used for storage purposes where high speed is not expected.

In a marked contrast to previously mentioned memories, STT-RAM is a non-volatile technology. After a successful write in STT-RAM cells, the data remains for a long time without the need to be refreshed [2]. STT-RAM has low latency and is a $CMOS$ compatible technology. It is considered as a reliable memory technology due to its intrinsic radiation hardness[4].

Table 1.1 compares the memory technologies with the emerging nonvolatile STT-RAM. STT-

	latency	volatility	power consumption	physical nature
DRAM	medium(100 ns)	volatile	high	capacitive
SRAM	low(10 ns)	volatile	varying with frequency	capacitive
NAND Flash	high(100μs)	non-volatile	low	capacitive
Hard Disc	very high	non-volatile	high	magnetic
STT-RAM	low(100ps)	non-volatile	low	magneto-resistive

Table 1.1: Memory Technologies

RAM has the fast speed feature of SRAM and DRAM but is not a volatile memory. Also, STT-RAM is more power efficient than NAND Flash memory and hard disc SSD. The high speed and insurance along with its high performance is the key to consider STT-RAM as the next promising memory technology.

1.2 Contributions

One of the most challenging reliability issues for space applications, is to protect te memory cells against high energy particles of the environment. Memory is required to tolerate the high energy alpha or gamma radiations and not to lose the stored data if hit by the particles.

Although an STT-RAM cell itself is believed to be invulnerable to radiation [4], its $CMOS$ sense circuit is susceptible to radiation. The $CMOS$ sense circuit is necessary to integrate STT-RAM cells with other components of a computer system and to read the state of data cells. The circuitry is required to be protected against high energy particles that can generate electron hole pairs and inject a radiation induced current into the circuit.

In this work, we analyzed the impact of radiation on STT-RAM read circuit. We defined single event upset (SEU) in STT-RAM sense circuit and explained how the radiation induced current may cause an SEU. A rad-hard sense circuit is a read circuit which can sense the state of MTJ cells precisely when exposed to radiation induced pulses. Such a circuit decreases the probability of having an SEU in the sense cycles.

Previous works [3][6][7] suggested solutions to protect the sense circuit against radiation effect. Although the suggested circuits are efficient in terms of dynamic power consumption, the latency is still high, because of their two stage read operation.

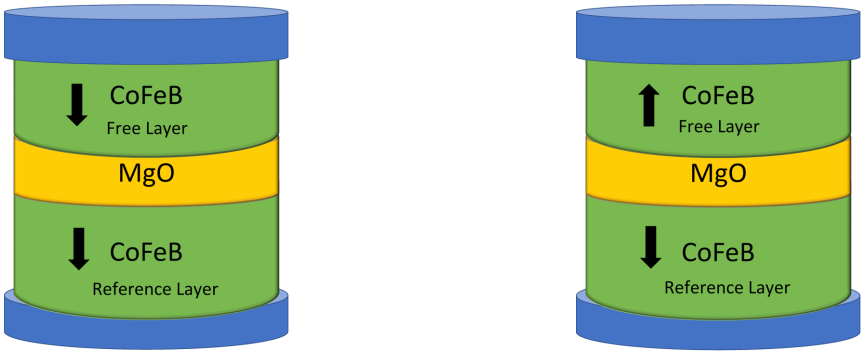
Considering the limitations of previous circuits and the power and area overhead which these circuits induce, we propose our own rad-hard sense circuit. In the following chapters, the topology and functionality of two types of conventional sense circuits are presented. The effect of radiation on conventional sense circuits is simulated. Our own proposed sense circuit and the effect of radiation on this circuit is described. We compared the proposed circuit to the conventional circuit and previous works in terms of power, speed and radiation hardness.

Chapter 2

Physics of STT-RAM

In magnetic based memories, the spin of electrons specifies the stored data[8][15]. Spin is a quantum mechanical property of electrons. STT-RAM also has a magneto resistive nature. It stores the data in the form of resistance value of the memory cell. Memory elements of STT-RAM are called Magnetic Tunnel Junction (MTJ). Fig. 2.1 shows the physical structure of MTJ. MTJ consists of two ferromagnetic layers and a dielectric layer in between. The ferromagnetic layers are usually cobalt-iron-boron, and the thin dielectric layer is usually magnesium-oxide (MgO). These sandwiched layers establish the MTJ with nanoscale dimensions. One of the ferromagnetic layers has fixed magnetic orientation, and is called the reference layer or pinned layer. The other one is called the free layer, and its magnetic orientation changes according to the direction of applied switching current [8] [15]. When the magnetic orientation of free and fixed layers are aligned (parallel state), the resistance of MTJ is low, otherwise the MTJ is in high resistance state (anti-parallel state). The tunneling magnetic resistance (TMR) of a MTJ is defined as :

$$TMR = \frac{R_{high} - R_{low}}{R_{low}} \tag{2.1}$$



(a) (b)

Figure 2.1: Magnetic tunnel junction multilayer in (a) parallel state and (b) anti-parallel

Where R_{high} is the resistance value of MTJ in anti-parallel state and R_{low} is the resistance value in parallel state. TMR is an important property of MTJ, which is usually described in percentages. Higher TMR increases the sense margin and makes it easier to detect the state of MTJ.

2.1 Write Operation

In order to write in magnetic memories, the spin direction of electrons should be altered. This can be done in various ways. In older magnetic RAM technologies, writing to a bit was done by passing current through a wire near to the memory bits. This current carrying wire produces a magnetic field that can change the spin orientation of free layer. Although this is a fast writing process, it is not power efficient. The current passing though the wire should be large enough to generate the required switching magnetic field. Hence, a wide wire is required. This makes the chip size very large. To ease the scaling down of the chip, one way is to reduce the size of memory cells. However, as the technology scales down, the memory cells become closer and the switching magnetic field affects the neighbor cells.

STT-RAM adopts another method to write in data cells, which decreases the required write current. In this method, a polarized current is passed through the MTJ cells directly. In

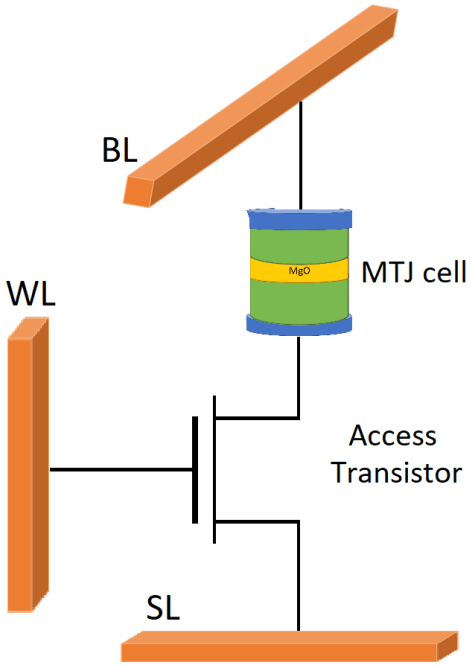


Figure 2.2: MTJ cell architecture

usual electric current, electrons have an arbitrary distribution of spin, in a way that the overall current is unpolarized. By passing the current through a thick magnetic material, we can have a spin polarized current. The spin polarized current alters the magnetization orientation of the free layer and writes the data into the memory cells. The critical current or switching current is defined as the amount of current passing through the MTJ that can change the state of MTJ. The basic cell architecture of STT-RAM is shown in Fig. 2.2. Each cell is connected to an access transistor that selects the desired bit. A bit line (BL) is connected to the other port of MTJ and a source line (SL) is connected to the source node of access transistor. The write process is done by applying the desired voltages to BL and SL.

2.2 Read Operation

As mentioned before, STT-RAM stores the data in the form of resistance value of MTJ cells. Therefore, reading data is basically measuring the value of a resistor. We should note that, only the relative value of MTJ resistance (high or low resistance) is determinative and the exact value is not important.

There are various sense circuits to measure the resistance of MTJ. In hybrid circuits, the resistance value is determined by comparing the discharge time constant of the sense circuit[3]. Another way to sense the data stored in MTJ cell, is to pass a small current (smaller than critical switching current) through it, and measure the resultant voltage.

2.3 MTJ Circuit Model

To analyze the radiation effect on STT-RAM and perform simulations we need an accurate and efficient circuit model for MTJs. The precision of the model is vital because it helps to optimize the STT-RAM circuits in terms of area and power consumption. Otherwise, if the model does not exactly express the characteristics of MTJ, designers have to consider a margin for the modeling error. In addition, a compact and fast circuit model reduces run time and makes simulations faster.

MTJ characteristic curves, show two major characteristics of this element that must be considered in the model:

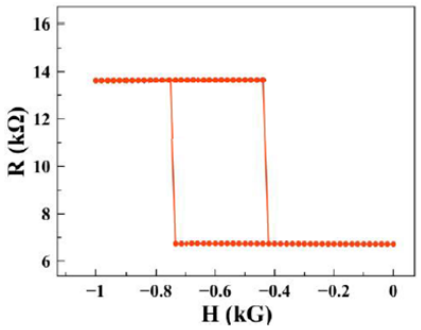


Figure 2.3: Magneto-resistance of a nanopillar MTJ vs. applied magnetic field

Hysteresis

The resistance of the MTJ changes with the magnetic field as shown in Fig. 2.3. The magnetic hysteresis behavior of the curve is the key to store data in MTJ. A higher magnetic field is required to switch from parallel state to anti-parallel state.

Bias dependent resistivity

Fig. 2.4 shows the resistance of MTJ versus the bias current. The is a nonlinearity in the high resistance value which is measured experimentally. This bias dependence can be approximated in the model by a Gaussian function.

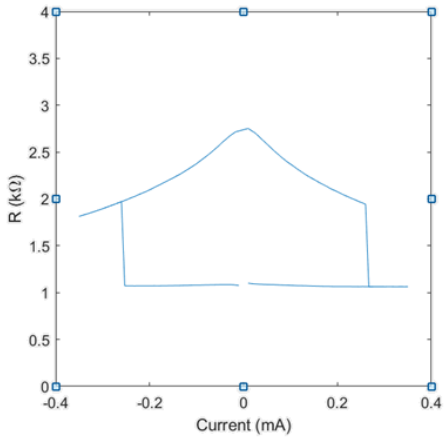


Figure 2.4: Resistivity of MTJ vs. bias current

There are three types of circuit models for an MTJ, macro models , micromagnetic models and behavioral models.

Macro models are circuits that represent the same functionality as of an MTJ. In these models, capacitors, resistors and controlled voltage sources are adopted to mimic the properties of MTJ. Macro models can be used in any circuit simulator such as Spice or Spectre. However, the number of required circuit elements increases with the precision of the MTJ characteristics[10].

Macro-models represent the characteristics of MTJ by solving the Landau-Lifshitz-Gilbert (LLG) equations. These models are beneficial because they consider the movement of individual magnetizations. This makes the micromodels very accurate, specially for smaller technologies. However, for an array of memory cells, the simulation time is long[10].

Behavioral models are a piece of hardware language code such as Verilog-A which describe the characteristics of MTJ. The Verilog-A code is compatible with Spectre and can be realized with a symbol in the circuit environment. These models have longer simulation time and might not be appropriate for simulating large arrays of memory [10].

Considering the mentioned pros and cons, we used the behavioral compact model of CoFeB/MgO/ CoFeB PMA MTJs presented in [18]. In this work, a compact model is programmed with Verilog-A language and a symbol is created in Spectre simulator (Cadence Platform). They have done DC simulations, to verify the static behavior of the model. Transient simulations also performed to ensure that the dynamic behavior of the model and experimental measurements are the same.

Using this model, we have simulated the sense circuit in Spectre Cadence, which will be discussed in the following chapters.

Chapter 3

Sense Circuits

3.1 Pre-Charged Hybrid Spintronics Sense Circuit

A typical hybrid/spintronic sense circuit for STT-RAM is shown in Fig. 3.1. This circuit adopts two MTJ cells in a complementary configuration to store one bit of data[3]. The hybrid/spintronic sense circuit measures resistance value of MTJs by measuring the time constant of the pre-charged circuit.

Read operation in this circuit is done in two stages. In the first stage, called pre-charge state, the sense enable signal (SE) is driven with a low voltage, to turn transistors P_1 and P_4 on. The capacitor present at nodes A and B are charged to V_{dd} voltage. In the second stage, SE signal goes high, turning N_3 on, and P_1 and P_4 off. In this stage, the capacitance at nodes A and B are discharged, because there is a current path to the ground through N_1, N_2 and N_3. Therefore, voltage of nodes A and B will be reduced with a time constant τ equal to:

$$\tau_A = R_A \times C_A \tag{3.1}$$

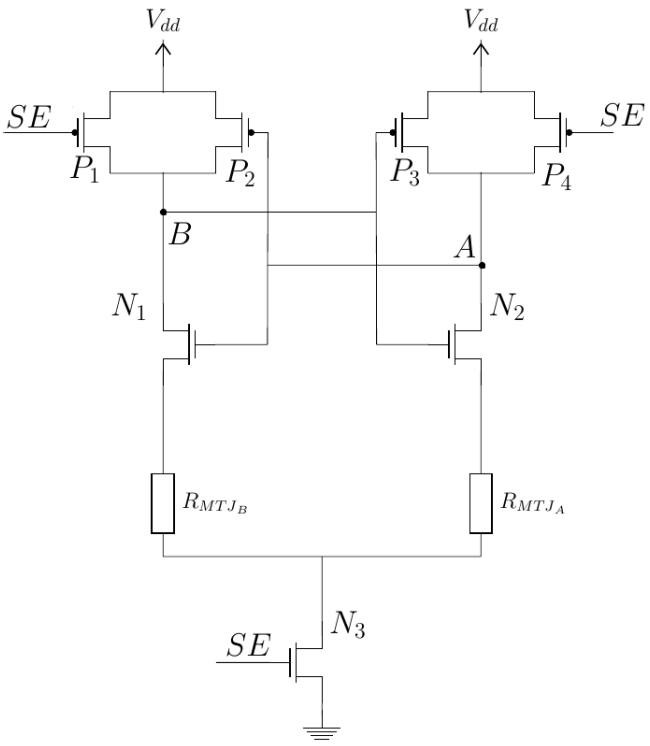


Figure 3.1: Hybrid/Spintronics sense circuit

Where R_A and C_A are the resistor and the capacitor present at node A, respectively. The resistance value R_A seen from node A is:

$$R_A = r_{o,P3} \mid\mid r_{o,N2}(1 + g_{mN2}(R_{MTJ_A} + 2r_{o,N3})) \tag{3.2}$$

Where $r_{o,P3}$, $r_{o,N2}$ and $r_{o,N3}$ are the output resistances of transistors P_3, N_2 and N_3, respectively. Also g_{mN2} is the small signal transconductance of N_2. The same equation applies to node B, where R_{MTJ_A} will be replaced by R_{MTJ_B}. The overall capacitor value seen from node A is also determined by adding the gate-drain, gate-source and the drain-bulk capacitance of the connected transistors:

$$C_A = C_{DB,P3}+C_{DB,P4}+C_{DB,N2}+C_{GD,N1}+C_{GD,N2}+C_{GD,P2}+C_{GD,P3}+C_{GD,P4}+C_{GS,N1}+C_{GS,P2} \tag{3.3}$$

C_A is not dependent on the value of R_{MTJ} and is the same for both nodes.

As an example, if MTJ_A is in anti-parallel state (high resistance) and MTJ_B is in parallel state (low resistance), the sense operation is done by comparing the discharge time constant of the two nodes:

$$R_A \geq R_B \Rightarrow \tau_A \geq \tau_B \tag{3.4}$$

As node B has smaller time constant, it will be discharges faster than node A. In other words, gate voltage of P_3 reaches to the threshold voltage more rapidly and turns transistor P_3 on. Node A will be charged again to V_{dd} and node B discharges to ground.

3.2 1T1MTJ Sense Circuit

One of the most popular sense circuits for STT-RAM technology is the circuit called 1T1MTJ (one transistor, one MTJ)[16]. The sense circuit is shown in Fig. 3.2. A bit of data is stored in the form of the resistance value of the MTJ cell. This circuit consists of two parallel branches, one connected to the data cell (R_{data}) and the other one to the reference cell (R_{ref}). The resistance value of the reference MTJ is set to:

$$R_{ref} = \frac{1}{2}(R_{low} + R_{high})$$

N_1 and N_2 are the access transistors connected to the word line. The world line signal (WL) turns on the access transistors to select the desired cell. Driving the RE signal with a high state, N_3 and N_4 transistors turn on and identical sense currents pass through the load transistors, N_7 and N_8. These identical currents passed through reference branch and data branch, leading to a voltage drop at the input nodes of the sense amplifier (SA). The sense amplifier evaluates the state of R_{data} by comparing the two inputs, V_{ref} and V_{data}. Neglecting

process variations, the voltage at the input of the sense amplifier can be obtained by:

$$V_{ref} = V_{DS,N4} + I_{ref} * R_{ref} + V_{DS,N2}$$

and

$$V_{data} = V_{DS,N3} + I_{data} * R_{data} + V_{DS,N1}$$

where $V_{DS,N1}$ and $V_{DS,N2}$ are the drain-source voltages of the access transistors and $V_{DS,N3}$ and $V_{DS,N4}$ are the drain-source voltages of N_3 and N_4 transistors, respectively. Since the sizes of N_1 and N_2 are chosen equally and the current passing through them is identical, the drain-source voltages are equal.

$$V_{DS,N1} = V_{DS,N2}$$

in the same manner,

$$V_{DS,N3} = V_{DS,N4}$$

So the differential input at the input nodes of the sense amplifier is determined by:

$$V_{data} - V_{ref} = I_{data} * R_{data} - I_{ref} * R_{ref}$$

$$I_{data} = I_{ref} = I_{sense}$$

So

$$V_{data} - V_{ref} = I_{sense} * (R_{data} - R_{ref})$$

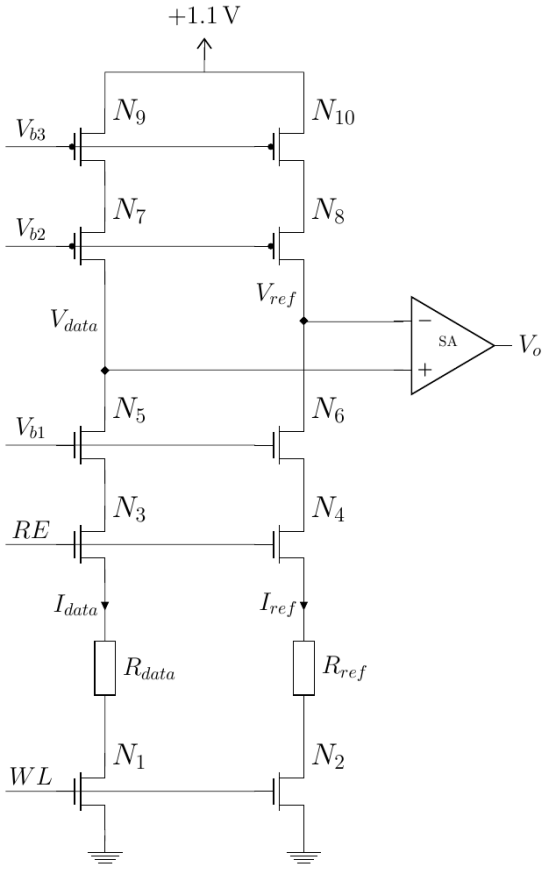


Figure 3.2: Conventional 1T1MTJ sense circuit

$$R_{ref} = \frac{R_{low} + R_{high}}{2}$$

if $V_{data} - V_{ref} > 0$, then $R_{data} - R_{ref} > 0$ and so

$R_{data} = R_{high}$.

else if $V_{data} - V_{ref} < 0$, then $R_{data} - R_{ref} < 0$ and so

$R_{data} = R_{low}$.

The circuit is simulated in 45 nm technology for the case where the data bit is zero. TMR value is set to 100%. R_{high} and R_{low} resistances are 8 $K\Omega$ and 4 $K\Omega$, respectively. The waveforms are shown in Fig. 3.3 for four read cycles. The read enable signal (RE) is set to

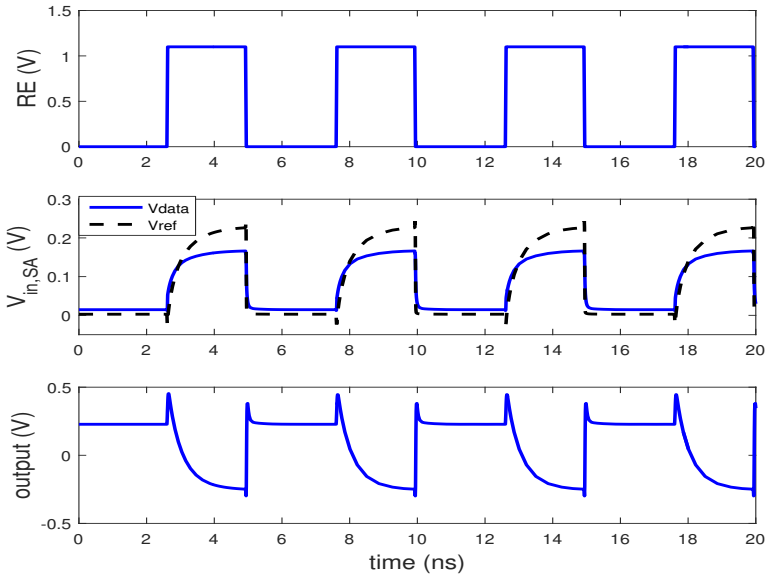


Figure 3.3: Read operation waveforms for 1T1MTJ sense circuit (MTJ State = 0)

1 for each 2.5 ns read cycle to turn on transistor N_3 and pass the current to MTJs. The voltages across data (V_{data}) and reference (V_{ref}) branches are measured and compared. As waveforms show, in all four cycles, V_{data} is lower than V_{ref}, which means the MTJ state is low, or the data bit is zero. This is an example of the normal functionality of 1T1MTJ sense circuit. In the next chapter the effect of radiation on this circuit is analyzed.

Chapter 4

Radiation Effect

Capacitive memories such as SRAM and DRAM are sensitive to radiation effects. As the technology scales down, and the frequency increases, these memories become more vulnerable to radiation. On the other hand, STT-RAM is considered as a promising technology for space applications because of its robustness against radiation. Previous research works [4][5] have experimentally shown that the MTJ cell itself has intrinsic radiation hardness due to its magnetic characteristics. It is shown [13] that both the TMR value and high/low resistance values of MTJ remain the same after irradiating the samples up to 64 *krad* for eight hours. However, the sense circuit is susceptible to radiation. When a high energy particle hits a reversed bias p-n junction in the circuit, it can generate electron-hole pairs and induce a current pulse [16]. This radiation induced current may lead to an error during read/write cycles and degrade the reliability of STT-RAM. Depending on the amount of radiation induced current, the error is either a volatile single event effect (VSEU) or a non-volatile single event error (NVSEU). VSEU happens when the radiation induced current at the sensitive node is less than the critical current required to switch the MTJ state. VSEU error can be corrected by performing another read operation. NVSEU is a permanent error and happens when the radiation induced current is larger than the critical switching current of

the MTJ and causes a bit flip. To compensate a NVSEU, another write operation is required [7]. In this chapter, MTJ sense circuits are simulated under radiation effect.

The radiation effect is modeled by a current pulse injected into the incident node of a circuit in [12]. They modeled the radiation induced current in the form of a double exponential pulse with its magnitude proportional to the amount of collected charge on that node.

$$I = \frac{Q}{\tau_1 - \tau_2}(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}})$$

Where Q is determined by the number of electron-hole pairs generated by the particle:

$$Q = n \times d_r \times V \times q$$

where n is the number of electron-hole pairs per rad in one $(cm)^3$, d_r is the radiation dose, V is the volume and q is the charge of an electron. The collected charge is determined for different radiation dose by the number of electron-hole pairs generated[1]. Fig. 4.1 shows the radiation induced current pulse simulated for radiation dose range of 100 $krad$ to 400 $krad$.

4.1 Radiation Effect on Hybrid/Spintronics Sense Circuit

Previous works [3],[7] presented rad-hard hybrid spintronics/CMOS circuits. In [3] they analyzed the effect of radiation on hybrid spintronics/CMOS sense circuit which deploys two MTJ cells in a complementary circuit to save one bit of data. In this work, four transistors are added to sense the radiation induced pulse and shunt the excess current to the ground. This circuit is simulated in $40nm$ technology and is tested for up to $80fC$ injected charge to

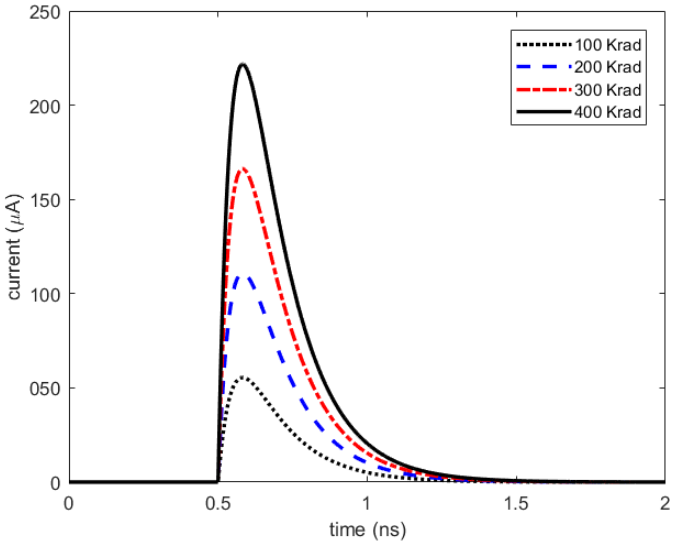


Figure 4.1: Radiation induced current pulse

the sensitive nodes. The paper reports that the circuit has radiation hardness for injected charge of less than $50fC$ at the cost of 60% area overhead and performance degradation. Also for injected charges more than $50fC$, the radiation tolerance of the rad-hard circuit is approximately the same as the conventional circuit.

Another approach to refine the circuit in high radiation environment is presented in [7]. In this work, the pre-charged hybrid spintronics/CMOS unit is duplicated to sense the data accurately. An XOR gate compares the output of two units and recognizes whether an SEU happened or not. If the outputs are not the same, an SEU occurred. This technique imposes more than 100% area and power overhead.

Another circuit is presented in [6]. In this work, the power and area overhead is reduced compared to aforementioned papers. However, the pre-charged sense circuit used in this study, slows down the sense speed.

4.2 Radiation Effect on 1T1MTJ Sense Circuit

In order to analyze the effect of radiation on a CMOS sense circuit, an understanding of the CMOS transistor characteristics is vital. The drain-source voltage of a $MOSFET$ transistor is a function of drain current as shown in Fig. 4.2. When the access transistor is biased in the saturation region, the drain-source voltage varies with the current because of channel length modulation effect. Hence, when the drain current jumps in a very short period of time, we will have a step change in the drain-source voltage.

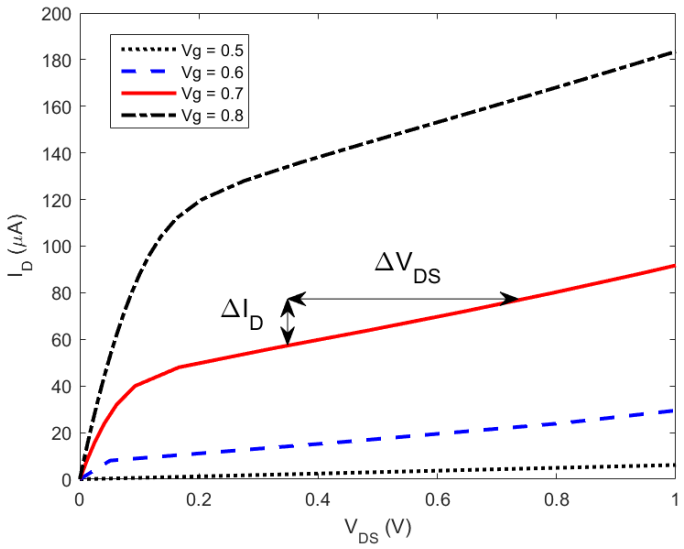


Figure 4.2: Variations of drain-source voltage vs. the drain current

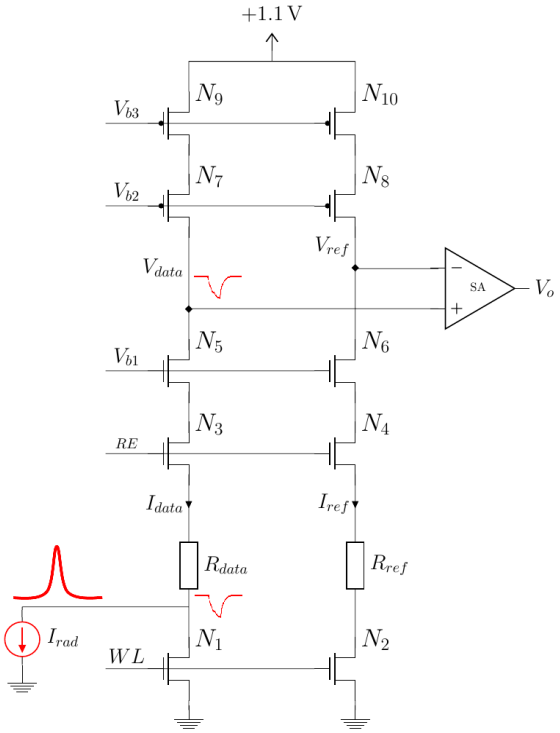
The same phenomena happens in the circuit shown in Fig. 4.3, when a high energy particle hits the drain of the access transistor N_1, and injects radiation induced current I_{rad} into this node. At this point two scenarios are possible. The first scenario is shown in Fig. 4.3a which represents the radiation effect when the injected current is positive. The current passing through MTJ does not changed since the MTJ is in series with a current source realized by N_7. However, the drain current of N_1 is increased, which leads to an increase in the drain voltage of N_1 and consequently V_{data}. In this case, we have a positive step change in V_{data} for a short period of time. This can cause a read failure when the actual data is zero (0 to

1 read error). Another scenario is shown in Fig. 4.3b where the injected current pulse is negative and likewise the MTJ current is fixed. The drain current of N_1 is reduced. The drain voltage of N_1 is decreased, leading to a drop in V_{data}. In this scenario, the 1 data can be sensed as zero (1 to 0 read error).

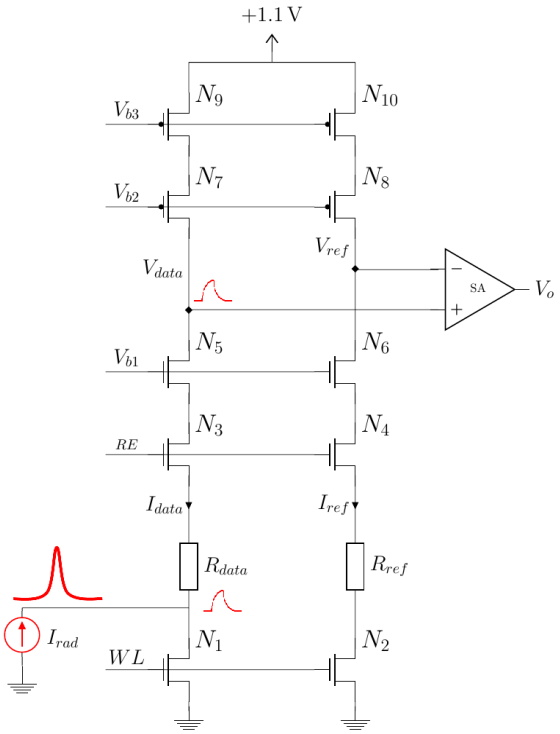
We should note that the drain of the access transistor is considered as the most sensitive node. Although the high energy particles can hit any reversed bias p-n junction in the circuit, the probability of hitting the access transistor is the highest, since the number of access transistors is as high as the number of memory bits [16].

The conventional 1T1MTJ sense circuit is simulated in $45nm$ technology and the MTJ is represented by a behavior model, developed with VerilogA code for Spectre simulation[14]. The radiation induced current is injected in order to analyze the radiation effect. Fig. 4.5 expresses the sense failure due to the radiation. The radiation induced pulse causes a step rise in V_{data}, making it higher than V_{ref}. The output has changed to $+0.2V$ for a short period of time. If a clock pulse arrives in this period of time, the output can be interpreted as 1 and a read error occurs.

According to previous discussions, the key point here is that, the radiation induced current, changes the current passing through access transistors, and so changes their drain-source voltage. Hence, to detect the error, we need to monitor the V_{DS} of the access transistor. But in an array of cells shown in Fig. 4.4, we do not have any external access to the drain node of N_1. For a 1×8 memory architecture we cannot probe the drain of access transistors. It is not possible to connect the drain of access transistors to a line to probe them, since in that case, all the MTJ cells will be in parallel. The MTJ cells store data by their resistance value. If they are connected together in parallel, the data will be lost. The only access point is the bit-line where all MTJ cells are connected. In the next chapter a solution is proposed to negate the effect of V_{DS} without any access to the drain node.



(a)



(b)

Figure 4.3: Radiation effect on 1T1MTJ sense circuit

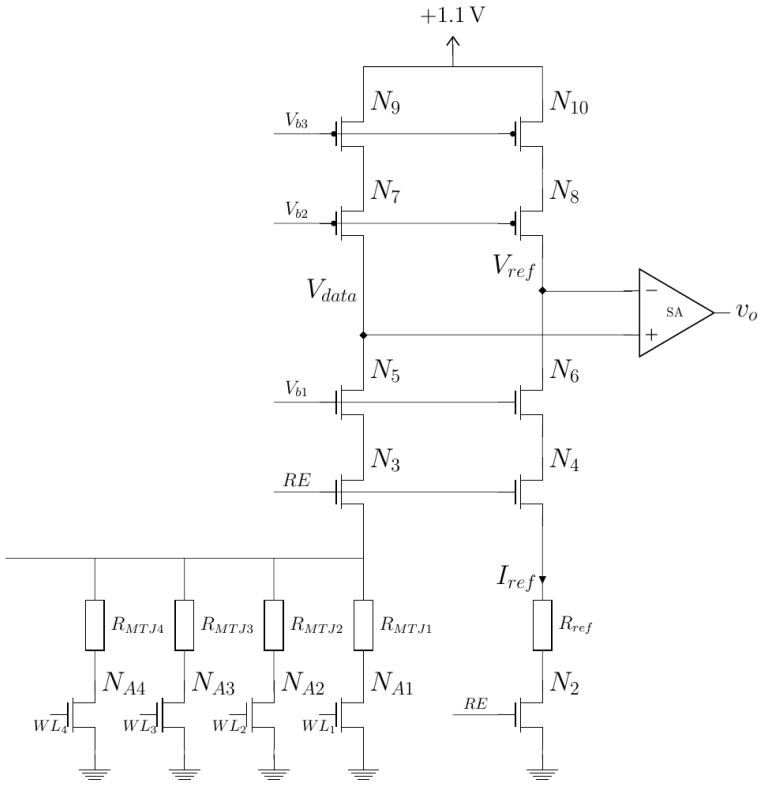


Figure 4.4: Array of memory cells

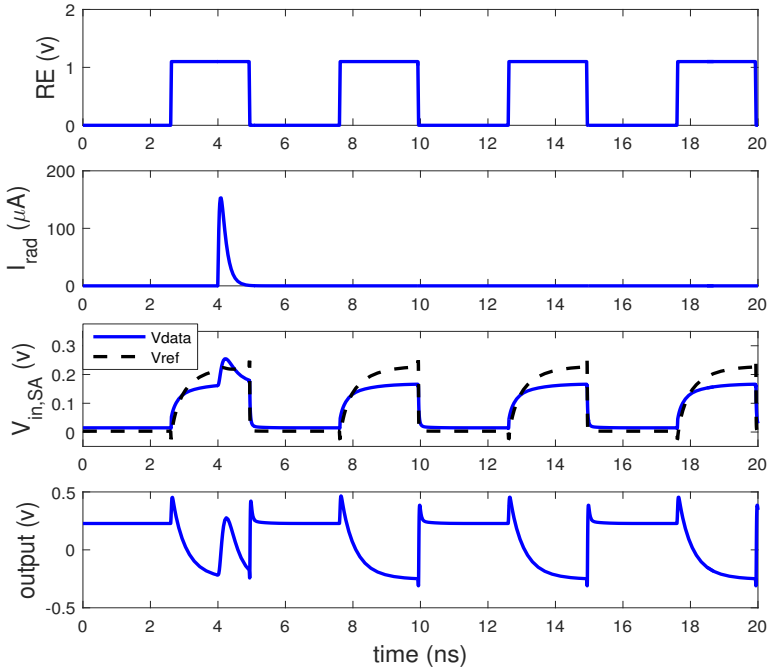


Figure 4.5: Radiation induced read error in conventional 1T1MTJ circuit

Chapter 5

Proposed Rad-Hard Sense Circuit

5.1 Rad-Hard Sense Circuit Design

In this work, a new sense circuit is designed which is power efficient, fast, and radiation hardened by its architecture. As discussed in previous chapters, variable V_{DS} of the access transistor is the major flaw of the 1T1MTJ sense circuit in the presence of high radiation. We have eliminated this effect in our proposed rad-hard sense circuit. Fig. 5.1 shows the schematic of the proposed circuit. The reference MTJ is put in the path of the access transistor. Thus, any change in V_{DS,N_1} will have the same effect on both V_{data} and V_{ref}. In addition, it is necessary to add the transistor N_2 in series with R_{ref}. Otherwise, in an array of cells, all the MTJ cells will be in parallel. In this circuit, considering the radiation induced current injected to the drain node of N_1, the voltage of input nodes of the sense amplifier is:

$$V_{ref} = V_{DS,N_1} + I_{sense} * R_{ref} + V_{DS,N_2}$$

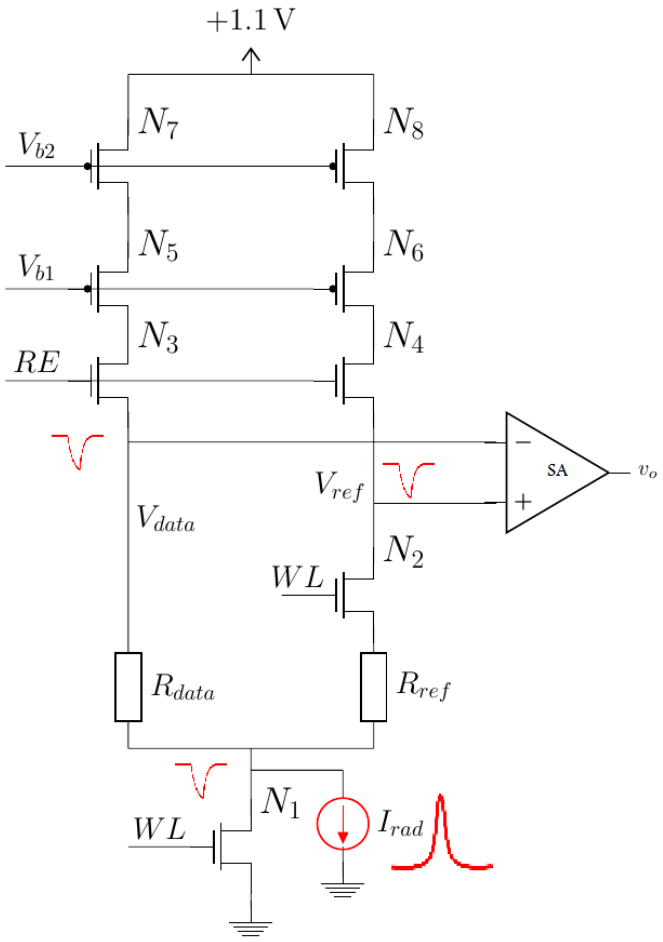


Figure 5.1: Proposed reference branch

where V_{DS,N_2} is the drain-source voltage of N_2 when it is turned ON, passing current I_{sense} and also no radiation hits N_2.

$$V_{data} = V_{DS,N_1} + I_{sense} * R_{data}$$

We choose R_{ref} and the size of N_2 in a way that:

$$I_{sense} * R_{ref} + V_{DS,N_2} = I_{sense} * \frac{R_L + R_H}{2}$$

In this way, comparing V_{data} and V_{ref} we can find the state of MTJ.

Although this circuit eliminates the effect of radiation on N_1, since a new transistor N_2 is

added, it is possible that the particles hit the drain node of N_2 and change its drain-source voltage. If this happens, the value of V_{ref} will be wrong and the comparison result is not valid anymore. We solved this problem by adding the second reference branch as shown in Fig. 5.2. The reference branches are identical. The two reference branches should be placed far from each other in the layout. In this way, it is very unlikely that the particle hits these two nodes at the same time. If one of the references is hit by particles, the other one would be error free. In other words, to cause a read failure, the particles have to hit the drain nodes of N_2 and N_3 simultaneously, which is a multi bit upset (MBU) and is less probable.

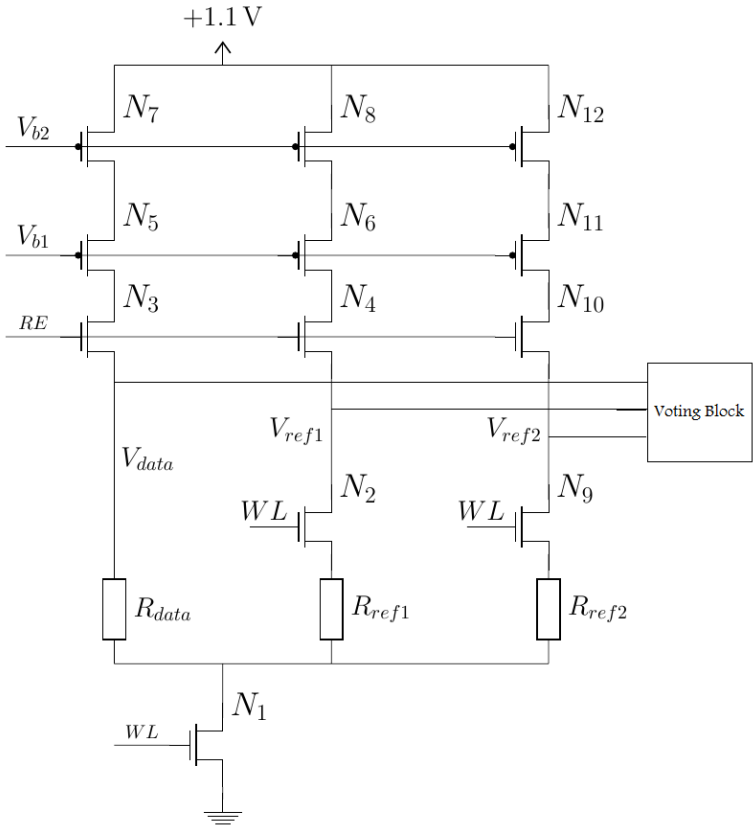


Figure 5.2: Proposed rad-hard sense circuit

We added a logic unit that detects, if any radiation error has occurred. In the case of an error, the logic unit detects which reference branch is error free and compares voltage V_{data} to the V_{ref} of the error free reference branch. The error free reference voltage is always the same regardless of R_{data} value. The logic unit is simply composed of a comparator to check

if $V_{ref,1}$ is hit or not, by comparing it to the ideal value of V_{ref} when no radiation is present. If error happened at $V_{ref,1}$, we assume that the $V_{ref,2}$ is error free. So the multiplexer choses the $V_{ref,2}$ to be compared with V_{data}. Otherwise, $V_{ref,1}$ is error free and $V_{ref,1}$ is passed by the multiplexer to the comparator.

The logic block is also implemented in CMOS $45nm$ on the same chip. The V_{data} and V_{ref} voltages are compared by a two-stage open-loop comparator. The output of the two comparatprs are latched. The CML XNOR gate decides whether there is an error in $V_{ref,1}$ and sets the $error_{ref,1}$ to select between the multiplexer inputs. A Current Mode Logic (CML) buffer is included after the multiplexer. The output is fed to a D-flipflop to test the functionality of the proposed circuit. For this work, we do not consider the radiation effect on the logic block transistor nodes, since there are only a limited number of transistors used in this block compared to the high density memory. Therefore, the logic circuit nodes are not considered as sensitive nodes in this paper, since the probability of them being hit by particles is very small compared to the large number of access transistors.

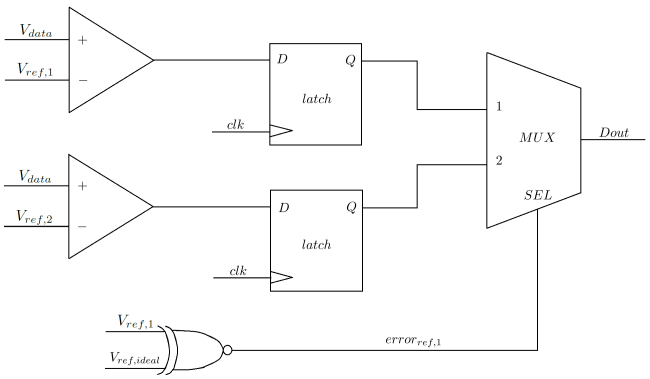


Figure 5.3: Voting block to detect and correct the error

Proposed circuit is protected against an SEU caused by high energy particles. It can also detect an MBU by just adding another comparator to compare $V_{ref,1}$ and $V_{ref,2}$. In this way, if the two reference voltages are the same, and $error_{ref,1}$ is equal to 1, an MBU has occured.

5.2 Radiation Analysis of Proposed Rad-Hard Sense Circuit

The proposed circuit is simulated and tested under the radiation effect. Fig. 5.4 shows the waveforms when no radiation is present in the environment. In this simulation, the proposed read circuit is connected to two MTJ cells. The first cell (MTJ_1) is in the low state while MTJ_2 is in the high state. MTJ_1 is sensed in the first and third cycles and MTJ_2 is sensed in the second and fourth read cycles. As the waveforms in Fig. 5.4 show, for odd cycles where MTJ_1 is being sensed by activating its word-line signal, V_{data} is lower than V_{ref}, which sets the output signal to $-0.2V$. Similarly, for even cycles, where we sense MTJ_2, V_{data} is higher than V_{ref} which will set the output voltage to $+0.2V$.

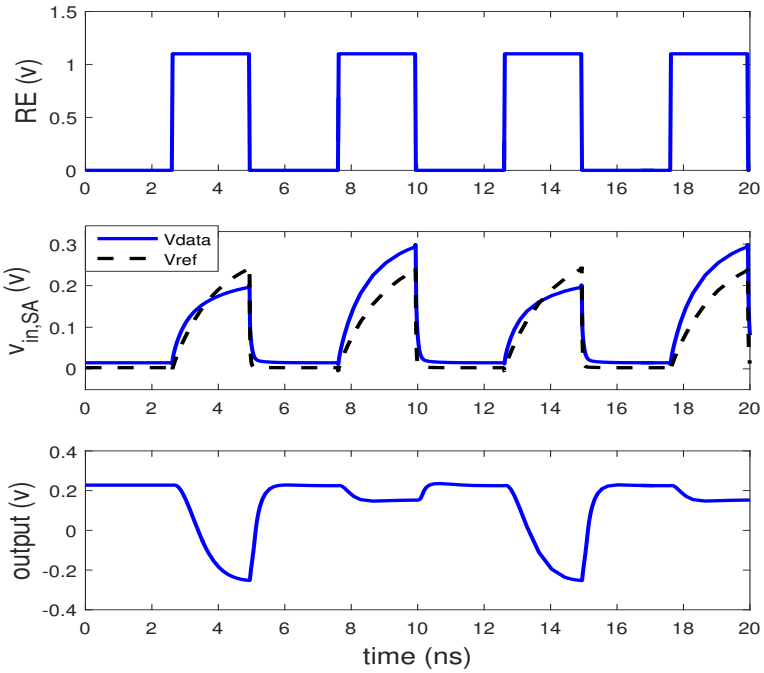


Figure 5.4: Read operation waveforms for the proposed circuit (MTJ_1 state = 0 , MTJ_2 state = 1)

We analyzed the effect of injected radiation current on our proposed circuit. The sensitive nodes of the circuit are the drain nodes of the access transistors and also the transistors in the reference branches. The first case is simulated by injecting the current into the

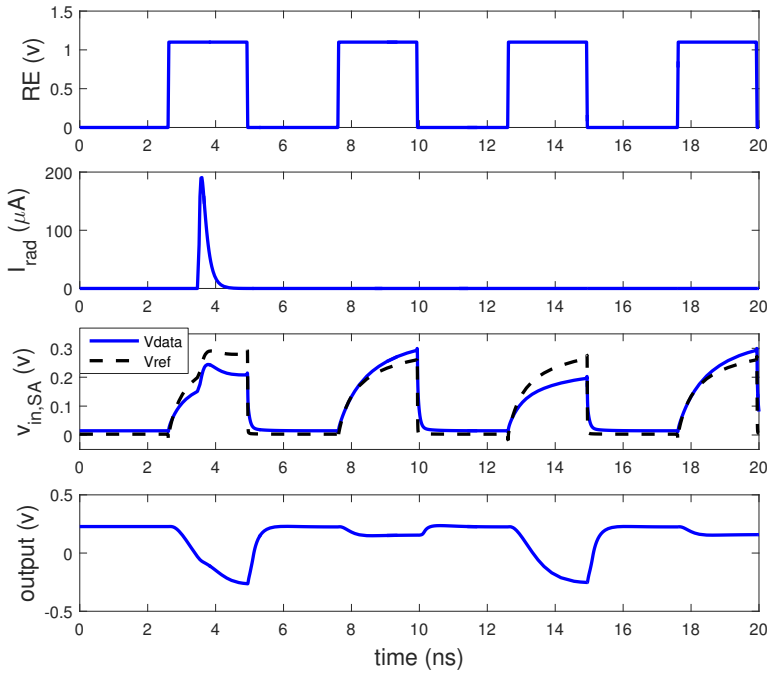


Figure 5.5: Read operation waveforms for the proposed circuit under radiation (radiation at access transistor)

drain of the access transistor, N_1. Resulted Waveforms are shown in Fig. 5.5. Injecting current to the drain of N_1 will result in an increase in both V_{data} and $V_{ref_{1,2}}$ simultaneously. Although V_{data} is raised, it is still lower than V_{ref} and this does not affect the result of our comparison.Therefore, the output remains error-free. Comparing the waveforms in Fig. 5.5 and Fig. 4.5, we can observe the robustness of the proposed circuit against a radiation pulse. In both conventional (Fig. 4.5) and proposed (Fig. 5.5) circuits, injecting I_{rad} leads to a voltage step increase in V_{data}. However, in Fig. 5.5, the output is not affected, where in Fig. 4.5 the output is impacted.

Another case is when the particle hits one of the reference branches. We simulated this by injecting I_{rad} to the drain node of N_2. As depicted in Fig. 5.6, the $error_{ref,1}$ signal indicates which reference branch voltage should be compared to V_{data}. For the first sense cycle, the $error_{ref,1}$ signal is in the high state, which implies that the reference voltage V_{ref_1} is affected by the radiation, while V_{ref_2} has remained untouched where it can be used for comparison. As shown in Fig. 5.6, although $V_{ref,1}$ is lower than V_{data}, the output signal is in the low

state. For the rest of the read cycles, $error_{ref,1}$ is in the low state and $V_{ref,1}$ is chosen to be compared with V_{data}.

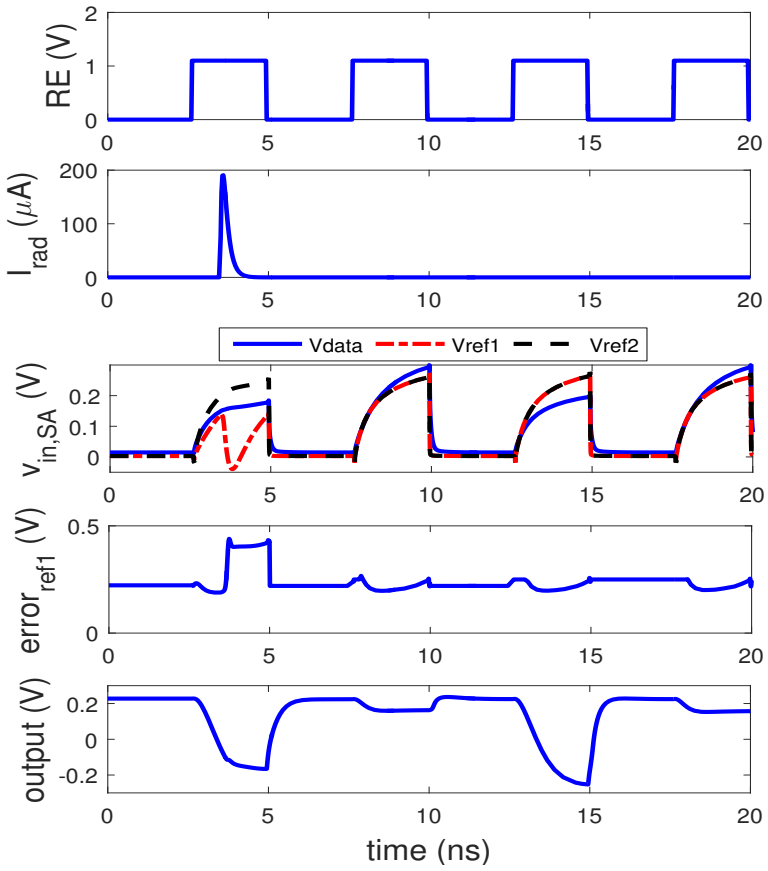


Figure 5.6: Read operation waveforms for the proposed circuit under radiation (radiation at reference branch)

Chapter 6

Conclusion

6.1 Evaluation

The proposed rad-hard sense circuit is simulated for an array of 8 memory bits as shown in Fig. 6.1. This circuit is immune to radiation induced SEU. Also our logic block can detect an MBU (when both reference branches are incident). The circuit is tested for radiation dose up to 400 $krad$ which is equivalant to $50fC$ collected charge at sensitive nodes. This circuit has 50% power overhead compared to the conventional 1T1MTJ circuit. This is expected since we have to drive three branches instead of two. Table.6.1 compares our proposed rad-hard circuit to previous works in terms of area and power overhead per bit and also the speed of recovery after a radiation incident. The number of transistors per cell is three, which is comparable to previous works. The power overhead is at the same range of previous works [3] [7], which when compared to their original circuit have about 50% power overhead. The most important feature of our circuit is its recovery time after a radiation incident, which is near zero for up to 400 $krad$ dose of radiation. Although the proposed circuit is superior to existing solutions in term of radiation hardness, it requires additional MTJ cells and

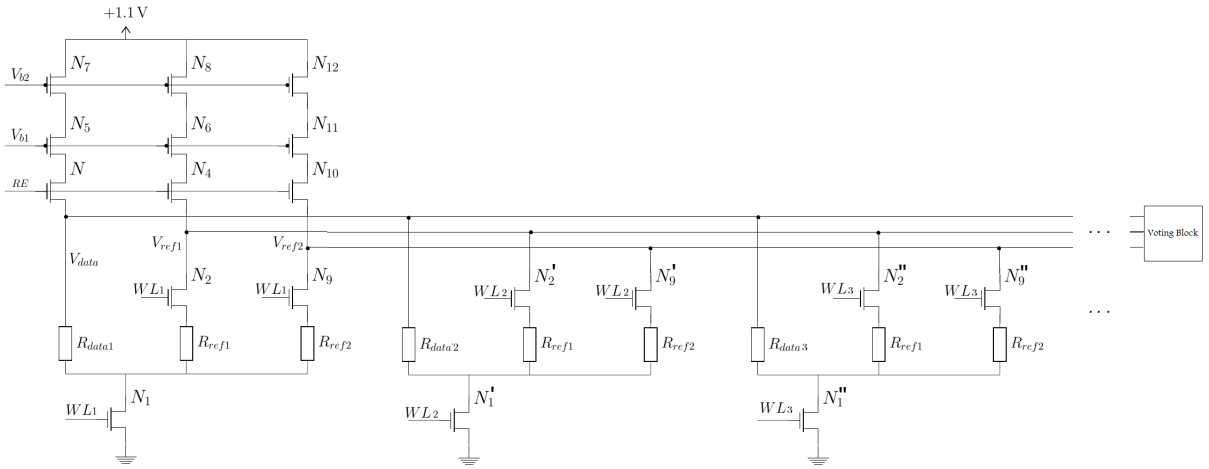


Figure 6.1: Proposed circuit for an array of memory cells

transistors. Our proposed design has the potential to be improved in terms of sense-margin and sensitivity to process variations [11] [9].

In this project, we analyzed the effect of radiation on 1T1MTJ sense circuit of STT-RAM technology. Simulations verified the analytic arguments for a simulated circuit in the 45 nm technology. We presented our rad-hard sense circuit that eliminates the SEU and also detects the MBU. The circuit is tested for radiation induced collected charges up to $50fC$. Simulation results show that the circuit is radiation hard at the cost of 50% power overhead. The robust proposed circuit can be used in the future to design more advanced memory technologies for space applications and other situations where rad-hard circuit operation is critical.

Table 6.1: Comparison between STT-RAM sense circuits

sense circuit	# transistors per bit	# MTJs per bit	power overhead	recovery delay(ns)
conventional	1	1	-	∞
[3]	1	2	53%	0.1
[7]	2	4	more than 100%	0.52
[6]	4	2	57%	0.36
proposed	3	3	50%	0

6.2 Future Works

In this research we analyzed the STT-RAM sense circuits from the perspective of radiation effect. There are some other important features of the sense circuits which require further investigation and research.

Most memories used in today's applications are two dimensional and have multiple bits in each line. In future we will extend our solution for a $8M \times 8$ array of memory. Having eight bits in each line, the throughput of memory increases eight times.

Also our proposed sense circuit is immune to radiation pulses, we will perform Monte-Carlo simulations to verify that the random behavior of the radiation pulses will not affect the performance of our circuit. We will simulate the circuit for a random distribution of radiation time and dosage.

As mentioned in previous chapters, the whole circuitry around the MTJs should be protected against radiation. In future, we will investigate the effect of radiation on write circuits and we will present a rad-hard write circuit for this memory.

There are previous works on the effect of process variations on 1T-1MTJ sense circuit [9]. We will persue these solutions to improve our sense circuit reliability. Also the effect of temperature variation on the MTJ cells and also the circuit should be studied in future.

Appendix A

Compact model of MTJ

Title: Compact model of Perpendicular Magnetic Anistropy (PMA) MTJ based on Spin transfer torque mechanism

Version: Beta.4.0

Date:24 May 2014

Language: VerilogA

Property: IEF, UMR8622, Univ.Paris Sud-CNRS

Authors: You WANG,Yue ZHANG, Weisheng ZHAO, Yahya Lakys, Dafine Ravelosona, Jacques-Olivier Klein and Claude Chappert

In this model, it takes into account the static, dynamic and stochastic behavoirs of PMA MTJ nanopillar:

- MTJ resistance calculation based on brinkman model
- TMR dependence on the bias voltage

- Spin polarity calculation model for magnetic tunnel junction
- Critical current calculation
- Dynamic model
- Stochastic model
- Resistance variation
- Temperature evaluation

The model files can be found here: `https://www.researchgate.net/profile/You_Wang15/publication/309414922_PMAMTJ40_5breakdown/data/580f584308aee15d4911edda/PMAMTJ40-5breakdzip`

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