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Authors
Jing, T.
Delgado, J.C.
Bertomeu, J.
et al.

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Physics Division

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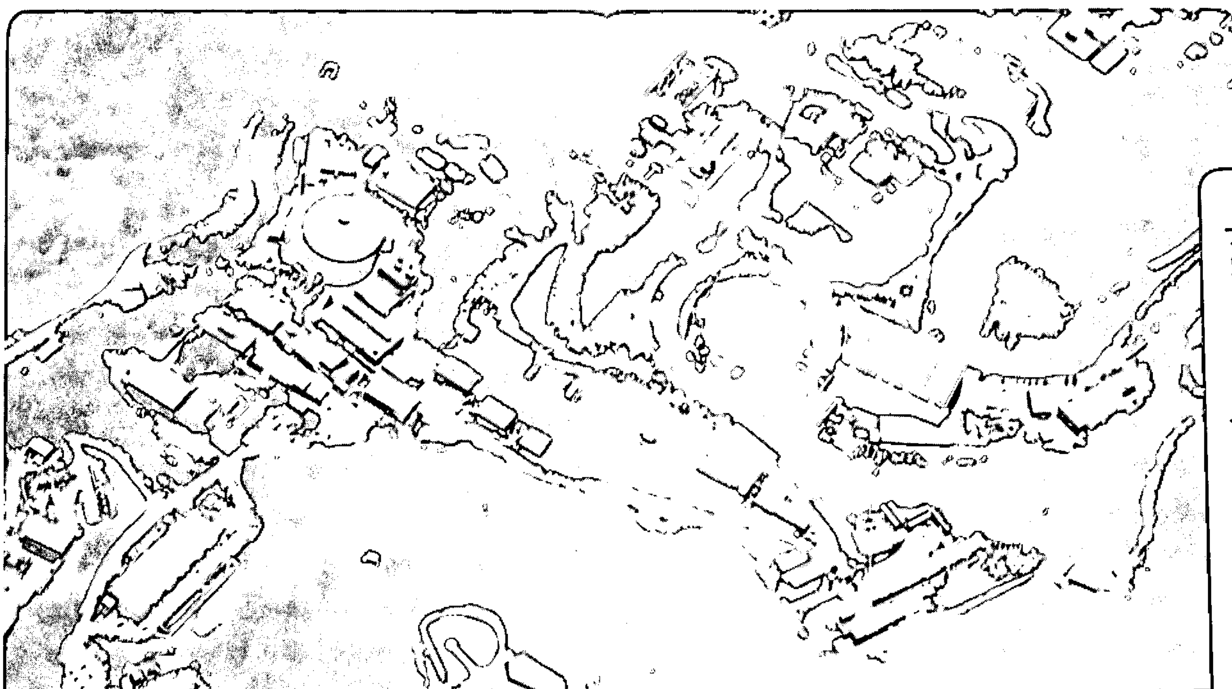
April 1994



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CHARGE COLLECTION IN a-Si:H/a-$Si_{1-x}C_x$ MULTILAYERS PHOTODETECTORS

T. Jing, J. C. Delgado*, J. Bertomeu*, J. Drewray. W.S. Hong, H. Lee,

S.N. Kaplan, A. Mireshghi, V. Perez-Mendez

Lawrence Berkeley Laboratory,

University of California,

Berkeley, CA 94720 USA

* Department de Fisica Aplicada i Electronica,

Universtat De Barcelona, Spain

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* Department de Fisica Aplicada i Electronica,

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ABSTRACT

Amorphous semiconductors have been used as thin film transistor(TFT), solar cell, phototransistors. In this paper we study the charge collected properties of a-Si:H/a-$Si_{1-x}C$:H_x multilayer pin photodiode. In a-Si:H pin photodiode, the photogenerated carriers can be totally collected under strong electric field under reverse bias. However, our measurements show that in the a-Si:H/a-$Si_{1-x}C$:H_x multilayer pin photodiode photogenerated electrons and holes drift toward the electrodes under a certain bias, the total collected charge shows no saturation with bias and exhibits a continuous increase with reverse bias. We classify that the device works at two regions. In region I, the device behaves like a photodiode. This charge collection efficiency drop from theoretical value may indicate charge capture or confinement at the interfaces and trapping at the a-Si:H potential wells. These tcharges trapped or confined can be released at the interface and quantum well at higher electric field. In region II, above a critical bias voltage, the device works as a breakdown diode with a series photosensitive resistor which contributes higher collection efficiency, namely optical gain greater than unity.

Keywords: amorphous silicon, multilayers, charge collection, photodiode

1. INTRODUCTION

Amorphous silicon multilayer structures have been extensively studied since 1983.[1-3] The well-defined periodic potential structure can be designed and fabricated by amorphous semiconductor heterojunction multilayers, which have shown some new aspects of amorphous material whose properties are different from the constituent bulk material. In particular, ultrathin multilayers consisting of hydrogenated amorphous silicon (a-Si:H) and hydrogenated silicon-based compounds such as silicon carbide (a-$Si_{1-x}C_x$:H), silicon nitride (a-Si1-xNx:H), silicon oxide (a-$Si_{1-x}O_x$:H), and silicon germanium (a-$Si_{1-x}Ge_x$:H) have been studied.[4-8] The existence of quantum size effects in an a-Si:H potential well has been demonstrated by resonant tunneling of electrons through a-Si:H/a-Si_3N_4:H double-barrier diodes[4,9] and recently by subband optical transitions observed in the differential absorption spectra of a-Si:H/quart and a-Si:H/a-$Si_{1-x}C_x$:H systems.[10,11] Therefore, unique optical and electrical properties currently observed for the multilayer structures are basically understood by quantum size effects which are well established in crystalline superlattices.

In this paper we are primarily concerned with electron transport in a-Si:H/a-$Si_{1-x}C_x$:H multilayers. Relevant electrical properties of a semiconductor device can be investigated by injecting excess carriers with an electron (or light) beam and measuring the induced current or charge.[12] The ratio η between this current or charge and the carrier generation rate represents the fraction of the injected carriers that is collected and is defined as charge collection efficiency of the device. The value of n for a photodetector with blocking contact (photodiode) is normally less than unity. In the photoconductor, the η replaced by optical gain G is larger than unity as long as the photocarrier recombination time is longer than the carrier transit time.[13] Our pin a-Si/a-$Si_{1-x}C_x$:H device has both the characteristics of photodiode at low bias voltage and the characteristics of the photoconductor at higher bias. This optical gain was previously reported to be as an avalanche phenomenon.[14] We will show that the I-V characteristics do not supports the avalanche assumption.

Semiconductor superlattice structures fabricated from alternating layers of crystalline III-V materials exhibit many interesting transport and optical properties that are associated with quantum size effects. These superlattices can only be fabricated from materials that have a nearly perfect match in their lattice constants and that can be grown epitaxially on top of one another. Otherwise the density of defects is too great to have advantages. Amorphous superlattices are not inherently restricted by the lattice matching condition because of the disordered arrangement of atoms and the fluctuations of the bond angle. Therefore, a more flexible fabrication of superlattice structures is permitted in amorphous system than in crystalline ones.

2. EXPERIMENTAL DETAILS

a-Si:H/a-$Si_{1-x}C_x$:H multilayer pin diode is schematically shown in figure 1. The p and n layers provide the built-in potential of the junction but contribute virtually nothing to the collection of the carriers. Therefore the doped layers need to be thin to avoid unnecessarily reduction of the charge collection by absorbing the incident light. The device was deposited in a RF capacititively coupled reactor with automated substrate holder.[15] The sample was prepared at a substrate temperature of 300^0C and a RF (13.56 MHz) power of 5 W (27 mW cm^{-2}). The gas pressure was maintained at 20 pa, and pure silane (20 sccm) and a mixture of silane (1 sccm) and methane (19sccm) were repetitively used in a-Si:H and a-$Si_{1-x}C_x$:H deposition. The plasma was maintained during the gas switching process, and the substrate was removed from the plasma influence until conditions were stable.[15] The carbon content in a-$Si_{1-x}C_x$:H alloy was found to be 0.36 by XPS. The cross-section of the this artificially induce periodic structure was observed by using Transmission electron Microscope (TEM). Fig.2 shows a very good periodicity, but non-strictly abrupt interfaces with a thickness of around 10 Å.

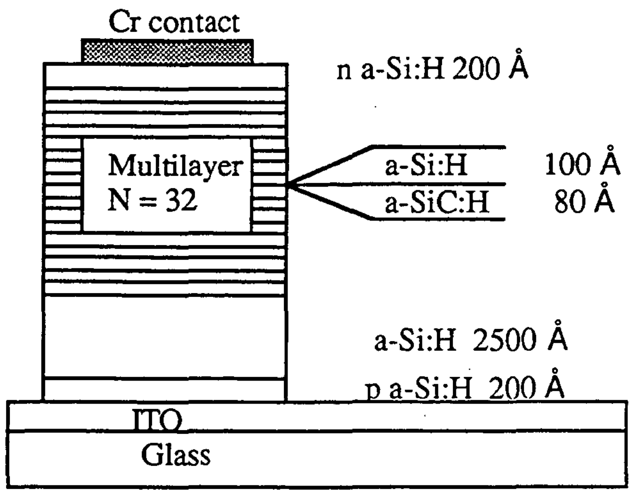

Figure 1 Schematic structure of pin a-Si:H/a-$Si_{1-x}C$:H_x multilayers.

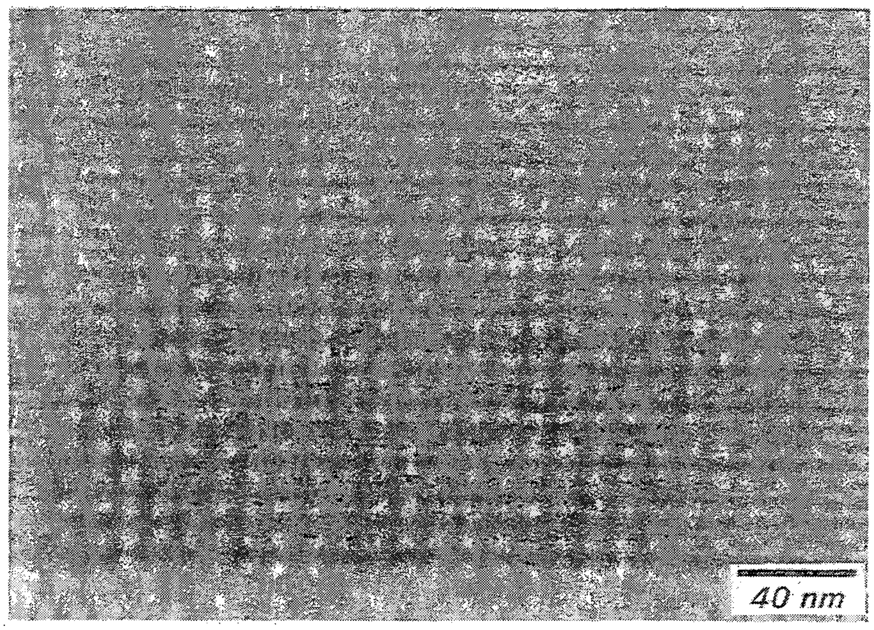

Figure 2. TEM photograph of a-Si:H/a-SiC:H multilayers (a-Si:H layers in dark).

The charge collection measurement was performed by measuring the optically induced charges. A short light pulse was illuminated on the p-side of the diode, the induced charges were integrated by a charge-sensitive preamplifier. A quasi-Gaussian shaping amplifier was connected to the preamplifier output. The shaping time (5 μs) is much longer than the carrier transit time at the order of nano-second, so signal loss (ballistic deficit) is negligible.

3. RESULTS AND ANALYSIS

3.1 SIGNAL SIZE DEPENDENCE ON A BIAS AND I-V CHARACTERISTICS

Charge collection corresponding to a single pulse was recorded as a function of the diode bias, as shown in figure 4. The reverse current was also plotted against the applied bias.

The initial efficiency at zero bias is only 20% which is less than the normal a-Si:H diode because the built-in potential may deplete only first 250nm a-Si:H layer, then be hindered by multiple a-$Si_{1-x}C_x$:H barriers, refer to Fig.3. These barrier heights or band offsets were reported to be ~ 0.2 - 0.4 eV.[16] With increasing bias, the depletion region reaches into the multilayer, hence more charges are collected similar to a-Si:H pin diode. In region I, the device behaves as a photodiode as shown in figure 4. The diode exhibits a small, essentially voltage-independent saturation current (thermal generation current).[17] In region II, above 60 V, the device works as a breakdown diode with a series photosensitive resistor (or photoconductor). As shown in Fig.4, after a critical voltage V_{br}, the current through the diode increases sharply. This is because when a high bias is applied to the diode, the thin barrier (p layer) separating the conduction band and valence band becomes narrower, tunneling of electrons will occur, as shown in Fig.3. These tunneling electrons from the p-side valence band to i-layer conduction band further to n-side conduction band constitute a reverse current from n to p; this is the Zener effect.[18] Since a-$Si_{1-x}C_x$:H layers are highly resistive, the device works as a series resistor R which limits the reverse current to a safe level. As shown in the Fig.4, the measured current is well described by calculating the reverse current,

$$I = (V - V_{br}) / R. \qquad (1)$$

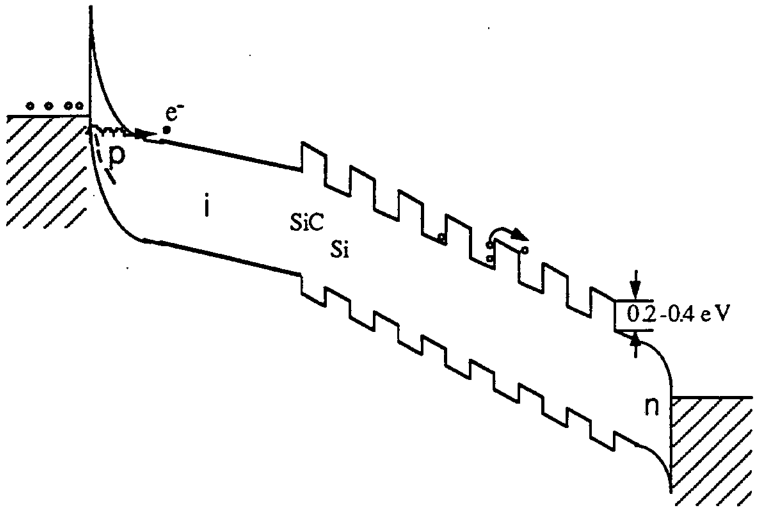

Figure 3. Energy band diagram of pin a-Si:H/a-$Si_{1-x}C_x$:H multilayers.

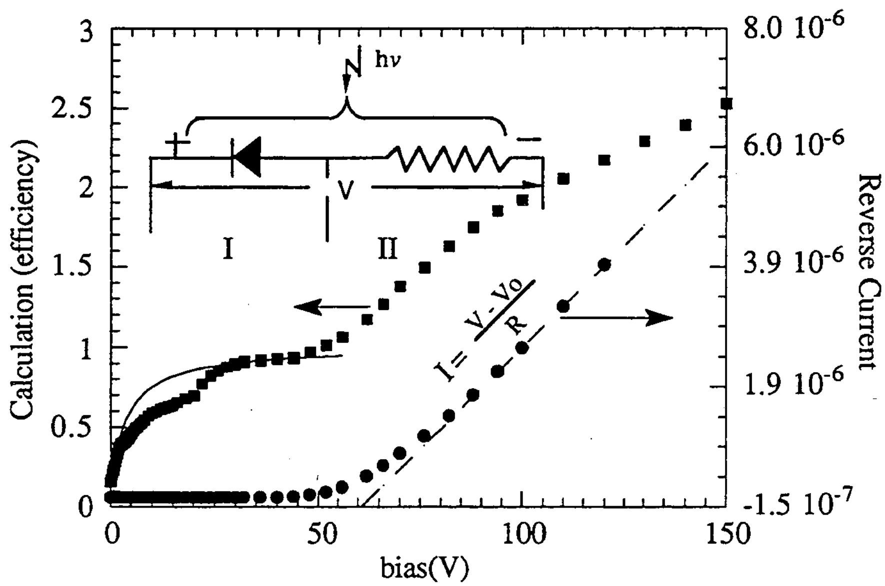

Figure 4. The charge collection efficiency with applied bias and I - V curve of the device.

3.2 CHARGE COLLECTION AS a PHOTODIODE

If the pin diode is biased at a constant voltage V, the electrons and holes generated in the optical interaction will drift toward the positive and negative electrodes, including a current given by the Ramo theorem:[19]

$$i(t) = \frac{q}{d}\,[v_e(t)n_e(t) + v_h(t)n_h(t)], \tag{2}$$

Where q is the electron charge, d the thickness of the diode, v_e and v_h the velocities of electrons and holes and $n(t)$ their corresponding concentrations at instant t. To a first approximation, the carrier velocity follows a linear relationship with the electric field:

$$v_e(t) = \mu_e E(x), \quad v_h(t) = \mu_h E(x), \tag{3}$$

μ being the carrier mobility. $E(x)$, being the electric field distribution will be substituted by the average electric filed E in the following. This is a reasonable assumption for a thin device.

On the other hand, the mean carrier concentration decreases due to the deep trapping or recombination during the transit and its decrease is characterized by a lifetime τ, following an exponential decay law:

$$n_e(t) = n_0 e^{-t/\tau_e}, \quad n_h(t) = n_0 e^{-t/\tau_h}, \tag{4}$$

In this way, the current in eq.(2) becomes,

$$i(t) = \frac{q n_0 E}{d}\,[\mu_e e^{-t/\tau_e} + \mu_h e^{-t/\tau_h}], \tag{5}$$

and the total charge induced on the electrode during some measurement time T_m after charge injection is simply an integral of eq.(5) for electrons and holes, namely,

$$Q_e = \int_0^{T^*} i(t)\, dt = \frac{qn_0E}{d}\,[\mu_e\tau_e(1 - e^{-T^*_e/\tau_e}) + \mu_h\tau_h(1 - e^{-T^*_h/\tau_h})] \tag{6}$$

T^* is either the measurement time T_m or the times when the electrons or holes complete through the depletion layer whichever is shorter.

Because small carrier diffusion lengths are an inherent property of amorphous semiconductors, the most important feature is the built-in drift field E_0, which provides a mean of carrier transport across the device. When the external bias is applied to the device, the internal field will be modified. It is difficult to predict the precise distribution of the electric field inside the device because of its nonhomogenerous structure; however in order to make a correlation of results possible we shall assume that the resulting average field is given by

$$E = E_0 + V_d/d, \tag{7}$$

V_d is the applied bias voltage. Obviously, eq.(7) is an oversimplification, justifiable only by the fact it leads to resonablely consistent results.

When strongly absorbed radiation, 560nm light in this case, is incident on the p-side of a diode, the signal is virtually induced by the electrons only. Because the transit distances are so short that the transit time for hole T^*_h is nearly zero, the second term of the eq.(6) can be neglected. Hence, the charge collection efficiency is

$$\eta = \frac{Q_e + Q_h}{Q_{gen}} = \frac{Q_e}{qn_0} = \frac{\mu_e\tau_e E}{d}\,(1 - e^{-T^*_e/\tau_e}), \tag{8}$$

Because the transit time T_r for electrons is shorter than the measurement time Tm, the T^*_e should be

$$T^*_e = T_r = d/v = d/\mu_e E, \tag{9}$$

Combining eq.(7),(8) and (9),

$$\eta = \frac{\mu_e \tau_e (E_0 + V_d/d)}{d} [1 - e^{-d/\mu_e \tau_e (E_0 + V_d/d)}], \tag{10}$$

The efficiency calculated by eq.(10) is plotted as solid line in Fig. 4. One should notice that the efficiency drop in the range 7 - 20 voltage may be due to the carrier confinement effect at a-Si:H/a-$Si_{1-x}C_x$:H interface or quantum well, seen in Fig.3.

3.3 CHARGE COLLECTION AS A PHOTOCONDUCTOR

As discussed above, in region II, the device works as photosensitive resistor, thus the collection efficiency can be larger than unity, as shown in Fig.4. For the photoconductor, the collection efficiency is normally called optical gain which is proportional to the applied bias when the bias is in the appropriate range (in this case between 60 to 80 voltage). The optical gain is given by,

$$G = \tau / t_{tr}(V), \tag{11}$$

τ is the carrier recombination time, $t_{tr}(V)$ carrier transit time which is proportional to 1/V at low bias for first order. At the higher bias, optical response begins non-linearly. The reason is that optical gain increase is limited by space charge accumulation at high field strength,[20] as shown in Fig.4.

4. CONCLUSIONS

We have observed the charge collection efficiency feature of a pin a-Si:H/a-SiC:H multilayer photodetector under a pulsed stimulating light. The device has two working regions. In the region I, from 0 to 56 V (the critical bias), as we have shown, that the device works as photodiode. The charge loss (the difference between the calculated curve and the measurement data, as shown in Fig.4, from bias 6 to 20 voltage) may be due to the carrier confinement effect at a-Si:H/a-$Si_{1-x}C_x$:H interface or quantum well. At higher bias, the diode tends to collect all of the generation carriers, because the carriers have obtained kinetic energies high enough from the high electric force to overcome the quantum well or interface confinement and can surpass barriers. In region II, above the critical voltage, the device behaves as a breakdown diode(Zener effect) with a series photosensitive resistor. This assumption was supported by the linearity of the optical gain increase with bias. The linearity of the reverse current above the critical bias voltage confirmed our conclusion. The critical voltage is associated with the p-layer doping level and p-layer thickness. By optimizing these parameters and the multilayer structure, the device can be designed to have an appropriate critical voltage and a low level of dark current, the higher optical gain can be expected.

5. ACKNOWLEDGMENTS

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