Title

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Reducing C_{OSS} Switching Loss in a GaN-based Resonant Cockcroft-Walton Converter Using Resonant Charge Redistribution

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***Abstract*— By applying resonant charge redistribution (RCR) to the parasitic capacitances of a switched-capacitor converter, Coss-related dynamic switching losses can be significantly reduced. The proposed technique demonstrates adiabatic mitigation of all primary loss mechanisms in a transformer-less resonant Cockcroft-Walton (CW) converter's forward power path, with only the gate drivers exhibiting conventional hard-charged CV^2f losses. Two inductors are used: a large primary inductance directly in the forward power path to mitigate transient inrush currents, and a second small inductance to perform C_{OSS} charge redistribution prior to initialization of subsequent phases. The second inductor can be small while still exhibiting high Q-factor as it only interacts with switch parasitics. A discrete 1:5 prototype using GaN-FETs and diodes achieves a power density of 181.8 kW/liter (2.98 kW/inch^3) and a peak efficiency of 96.2% with RCR contributing a measured 61% reduction in total losses at light load for a 0.74% increase in solution volume.**

Keywords—Resonant Converter, ZVS, Soft-Switching

I. Introduction

Within the past several years there has been increasing interest in hybridized switched-capacitor power converters with record breaking power densities having been demonstrated [1,2]. Recent work ([1-7]) has focused on developing topologies and switching regimes that eliminate the transient inrush currents associated with fly capacitor voltage mismatch, described analytically as the slow-switching-limit (SSL) in [8]. Here a topology is adopted that also eliminates transient inrush currents but in addition attempts to achieve complete soft-switching of all active devices by addressing the C_{OSS}-related dynamic switching loss inherent in all of the aforementioned designs. Output capacitance loss, or C_{OSS} loss, can easily account for over 50% of total converter loss at lighter loads, greatly incentivizing its mitigation. To minimize this loss mechanism and enable further power-density improvements, we propose the introduction of a short tertiary resonant phase designed only to interact with non-ideal switching device C_{OSS} capacitances. It serves to redistribute charge losslessly and appropriately amongst them such that all switches nominally exhibit zero-voltage-switching (ZVS). A similar approach has been used in low power piezoelectric energy harvesting for the past several years (termed 'bias-flip' by [9]). However, that approach focused on adiabatically redistributing the charge stored on the single intrinsic capacitance of the harvester's power source. In contrast, this work instead applies this principle to the much more complex parasitic capacitance network of the converter itself.

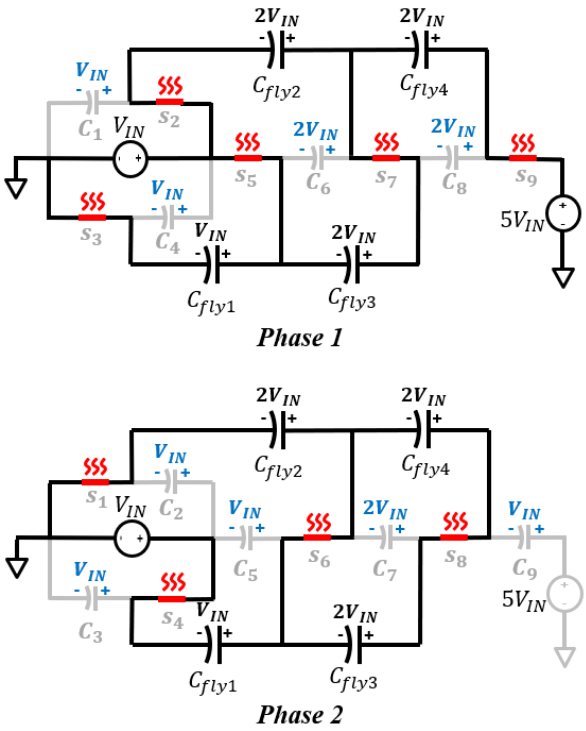

Fig. 1. C_{OSS} switching loss depicted as radiated heat in a conventional 1:5 Cockcroft-Walton (CW) converter.

Other work has focused on developing active snubber circuits, or zero-voltage-transition (ZVT) methods which similarly produce ZVS conditions using assistive LC networks [10]. However, these techniques have historically been primarily applied to simpler converter architectures such as buck, boost, flyback, or for power factor correction (PFC).

ZVS has been used extensively in power converter design for many years, but to the authors' knowledge has not been demonstrated in totality when applied to non-isolated complex switched-capacitor structures. Prior art, such as that demonstrated in [6], does achieve ZVS conditions, but across a limited number of switches. This work aims to achieve ZVS

conditions across all devices in a hybridized switched-capacitor converter, drastically reducing C_{OSS}-related CV^2f switching loss. The approach described herein has significant potential for expansion to an arbitrary number of phases and conversion ratios.

In this paper, Section II discusses switching loss, the proposed RCR mitigation method, its applications to a complex switched-capacitor topology, optimization constraints, and the non-ideal effects of non-linear C_{OSS} capacitance. Section III demonstrates a discrete prototype which achieves a 61% reduction in light-load losses with no optimization techniques applied. Section IV concludes this paper.

II. Steady-State Analysis

A. Switching Loss

Switching loss is a major loss mechanism in any switching converter arising as a result of energy being expended while reconfiguring the converter to a new state or phase of operation. This loss mechanism tends to be dominant at light-load, where conduction losses are small, and at high switching frequencies where it scales proportionally. The term 'switching loss' encompasses several different mechanisms including gate-drive loss, reverse recovery loss, finite transition time conduction loss, and output capacitance loss (C_{OSS} switching loss) [11]. Gate drive loss is that incurred by the gate driver in actuating the primary switching device, often by charging or discharging C_{GS}, and typically incurs CV^2f hard-charging losses. Several methods have been proposed to address this loss mechanism using resonant and soft-charging techniques within the gate-driver itself (e.g. [12]). Reverse recovery and finite transition time conduction losses can be avoided through use of devices with no intrinsic body diode (e.g. gallium nitride) and complete ZCS/ZVS respectively. The term C_{OSS} switching loss is primarily used to refer to CV^2f losses incurred through the hard turn-on of a device under non-ZVS conditions. Here, all energy stored in C_{OSS} is dissipated internally in the device's channel. Figure 1 depicts where C_{OSS} switching loss would occur in an example 1:N Cockcroft-Walton (CW) converter with FET switches, where N=5 and $C_{OSS} = C_{DS} + C_{DG}$. To highlight this loss mechanism, light-load operation is assumed, which results in no voltage ripple across the fly capacitors and as such the SSL considerations addressed in [1-7] can temporarily be ignored. By modelling switches in the on-state as a short circuit and switches in the off-state as their intrinsic C_{OSS} capacitance (C_{1-9}) one can see $C_{OSS}V^2f$ loss occurring at each phase transition. Provided the fly capacitors are significantly larger than the non-ideal switch capacitances, this power loss can be estimated using;

$$P_{C_{OSS}} \cong \left(\sum_{i=1}^{5} C_i {V_{IN}}^2 + \sum_{n=6}^{N+3} C_n (2V_{IN})^2 + C_{N+4} {V_{IN}}^2\right) f_{SW} \qquad (1)$$

where the effective C_{OSS} capacitance for each switch (C_1-C_{N+4}) can be estimated from datasheet provided characterization curves across a specified voltage range.

B. Resonant Charge Redistribution (RCR)

To efficiently transport energy, hybridized switched-capacitor converters utilize high-Q inductor-capacitor (LC) circuits to perform adiabatic energy transfer, such as the simple example depicted in Fig. 2. Here the polarity of the C_{EFF} voltage can be reversed without incurring conventional CV^2f hard-charging losses. In this example, the introduction of a diode removes the turn-off sensitivity of the switch allowing it to remain on after the RCR cycle has completed.

C. Proposed Solution

Fig. 3 depicts a 1:5 CW converter with all switches open. Here we have chosen an inductively loaded topology using the inductor L_P to mitigate SSL losses, as in [1], however; RCR will also work for conventional hard-charged topologies such as that depicted in Fig. 1. S_{5-9} can be actively controlled using split-phase or N-phase switching [6,7], or diodes may be used for simplicity in step-up applications.

To apply RCR a small inductor, L_r, is added between nodes V_A and V_B. This element serves to appropriately redistribute the charge stored on all parasitics of the primary circuit components during the deadtime interval between major (or 'primary') phases. Also depicted is switch S_r which controls this transfer. S_r can be relatively small and so its associated capacitance will be ignored.

Figures 4 and 5 depict the operation of such a converter. RCR acts between primary phases resulting in parasitic capacitors being pre-charged to an appropriate voltage before initialization of the subsequent primary phase. In an ideal case this results in perfect elimination of C_{OSS} losses at light-load. With increasing load, ripple across the fly capacitors results in this method deviating from ideal with this topology, but RCR still provides a net benefit until voltage ripple exceeds $|V_{IN}|$. As illustrated in Fig. 5, the deadtime between primary phases must be greater than or equal to the RCR duration for *complete* pre-charging of C_{OSS} parasitics (i.e., $t_{DT} \geq t_r$). Should $t_{DT} \gg t_r$, complete RCR will occur, but as the deadtime becomes non-negligible relative to the primary phase durations the converter enters discontinuous conduction (DCM) or a pulse-frequency-

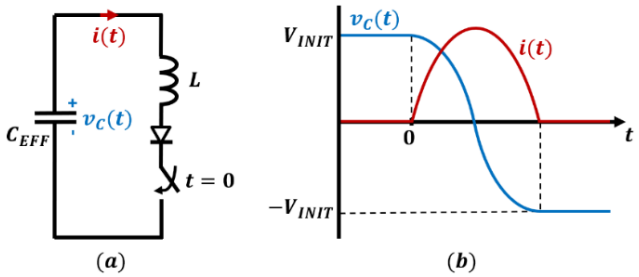

Fig. 2. A simple LC circuit exemplifying adiabatic energy transfer. (a) schematic, (b) voltage and current waveforms.

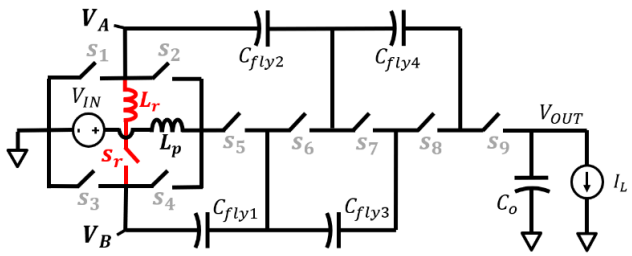

Fig. 3. A 1:5 CW converter including the proposed RCR circuit between nodes V_A and V_B.

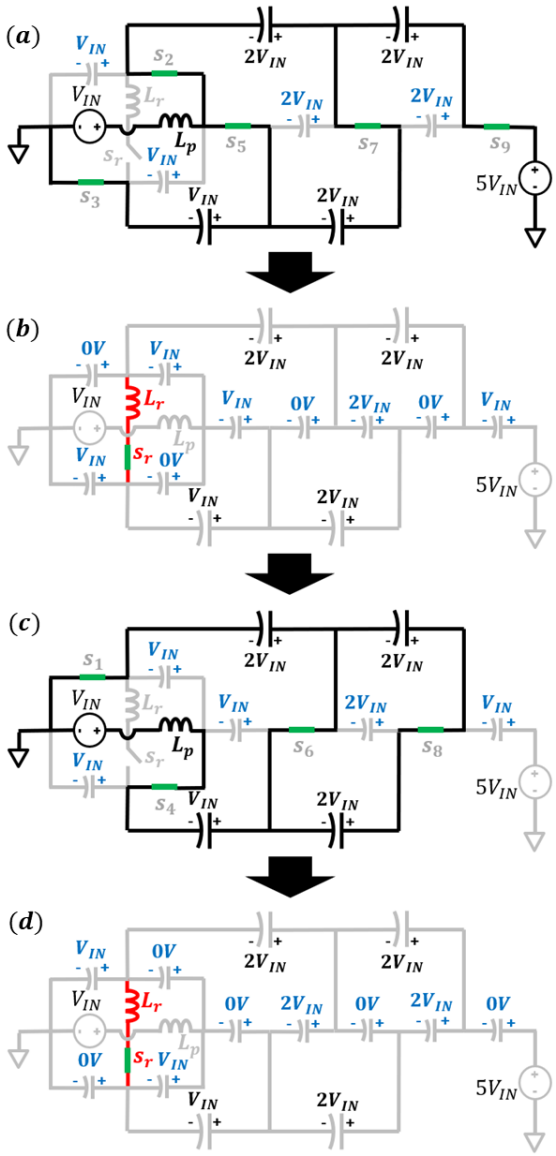

Fig. 4. Phase progression for a 1:5 CW using RCR in between major phases. The major phases, (a) and (c), are simplified and do not show the ZVS required to achieve full SSL loss mitigation. (b) and (d) depict the deadtime intervals and desired C_{OSS} voltages after perfect RCR has occurred.

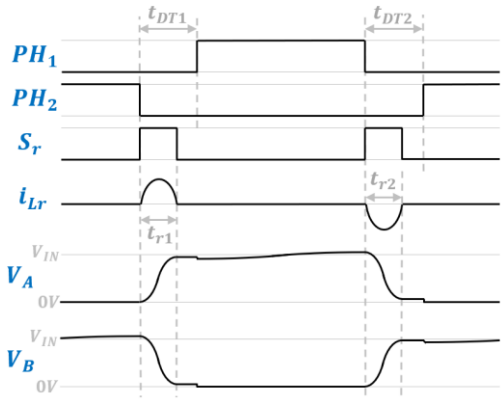

Fig. 5. Waveforms depicting RCR between nodes V_A and V_B.

modulation (PFM) mode of operation. Note that even if $t_{DT} < t_r$, active RCR will still affect a net performance benefit as some charge is still redistributed.

It can be difficult to recognize appropriate large-signal applicability of RCR and to deduce the required deadtime duration when considering the complex capacitor array of a switched-capacitor converter. To clarify, Fig. 4 (b) and (d) are redrawn as Fig. 6 with all large capacitors replaced with low impedance DC voltage sources. As a result, nodes V_A and V_B (Fig. 3) can be absorbed into super-nodes V_X and V_Y respectively by only considering the displacement current and shorting the voltage sources. Fig. 6 can be further simplified into Fig. 7 yielding an AC model. Since RCR occurs quickly during the deadtime between phases, L_p presents as a high impedance and so this branch can be ignored. To deduce the natural resonant frequency of the RCR, one must calculate the effective capacitance seen by inductor L_r, where it becomes apparent from Fig. 7 that;

$$C_{EFF} = \frac{C_3(C_1 + C_9)}{C_1 + C_3 + C_9} + \frac{C_2(C_4 + C_5)}{C_2 + C_4 + C_5} + C_6 + C_7 + C_8 \qquad (2)$$

Since switch parasitic capacitance (C_{1-9}) is typically orders of magnitude smaller than the fly capacitors, a small value of L_r may also be chosen. The choice of L_r directly affects the RCR duration which can be approximated as a resonant LC half-period:

$$t_r \cong \pi\sqrt{L_r C_{EFF}} \qquad (3)$$

As such, L_r is chosen to be small to keep dead-time short, while conversely being large enough to maintaining a Q-factor in relation to C_{EFF} that achieves the desired RCR efficiency improvements.

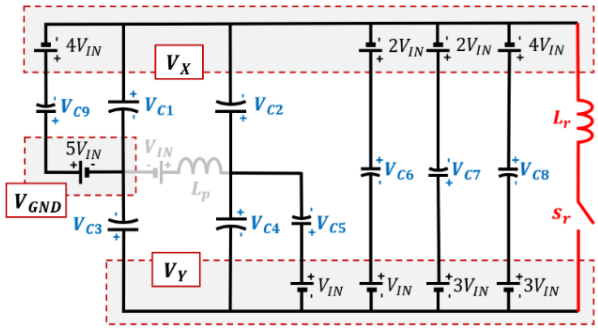

Fig. 6. Simplified model of a 1:5 CW converter during RCR operation. Large capacitors are depicted as DC voltage sources as they offer very low impedance relative to C_{1-9}.

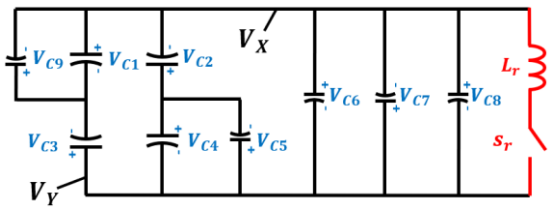

Fig. 7. Further simplified AC model with all DC sources shorted.

In order to achieve the correct charge redistribution for a 1:5 converter, we require;

$$C_1 + C_9 = C_3 \quad (4)$$

$$C_4 + C_5 = C_2 \quad (5)$$

These conditions equate to having two identical effective capacitances in series such that the RCR voltage polarity reversal is split evenly between them. Once these equalities are satisfied, by separately applying the voltages depicted in Fig. 4 (a) and (c) to $V_{C,1-9}$ of Fig. 6 one can see that when S_r closes the RCR circuit causes$(V_A - V_B) = \pm V_{IN}$ to complete a magnitude reversal, similar to Fig. 2, resulting in the desired voltages depicted in Fig. 4 (b) and (d) respectively being applied to $V_{C,1-9}$ before initialization of the next major phase. In this ideal case all C_{OSS} switching loss has been eliminated. To satisfy the C_{OSS} equalities, devices can either be sized appropriately or dummy capacitance can be added. Alternatively, the C_{OSS} constraints can be approximated or neglected, in which case imperfect RCR ensues while still imparting partial benefit.

D. Non-linear C_{OSS} Capacitance

In practice C_{OSS} is often highly non-linear, dropping off steeply with applied voltage bias. This results in a deviation from the ideal RCR behavior predicted by Fig. 7. If the input voltage range is large, t_r can vary significantly. To address this, t_{DT} can be selected as a best-fit duration or it can be dynamically adjusted as a function of input voltage to track t_r.

Provided the net non-linear characteristics are symmetric about the parasitic C_{OSS} network's equilibrium point, complete RCR can still be achieved despite high degrees of non-linearity in C_{OSS} values. This is illustrated in Fig. 8 where RCR is performed between two arbitrarily chosen opposing non-linear capacitors representing a lumped C_{OSS} network. In this example, voltage and current waveforms are non-sinusoidal but still give complete charge redistribution, provided both capacitors are identical. It is noted that for the same quantity of charge conducted, it is possible for non-linear capacitance characteristics to reduce RMS current and subsequent conduction losses relative to 'ideal' sinusoidal charge transfer.

Through strategic placement of additional dummy switches, as depicted in Fig. 9, Fig. 7 can achieve complete symmetry and ideal RCR if non-linear C_{OSS} characteristics are common to all switching devices. However, selecting appropriate large-signal placement of these devices may prove challenging. Additionally, these solutions also deviate from the ideal case when accounting for fly capacitor voltage ripple with increased load. As such this concept is not explored further here. Although, we note that applying RCR to more symmetric topologies such as the multi-phase variant of the 'stacked-ladder' topology presented in [13] is expected to yield inherently improved performance.

III. Discrete Prototype

A prototype measuring 25.3mm×13.5mm×4.2mm and depicted in Fig. 10 was constructed using the components listed in Table I. Large GaN-FETs were chosen for S_{1-4}; since C_{OSS}-related losses are to be significantly reduced with RCR, optimal switch sizing shifts towards larger devices for reduced conduction losses. Diodes were selected for switches S_{5-9},

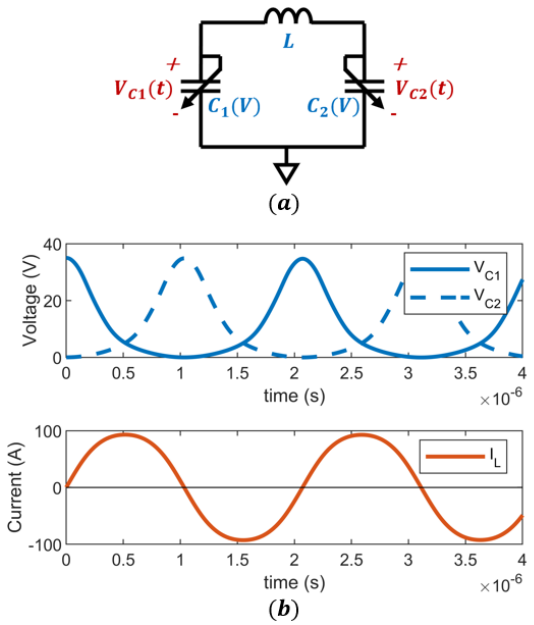

Fig. 8. (a) schematic and (b) simulated waveforms illustrating symmetric resonant charge transfer between two opposing identical non-linear capacitors which represent a lumped parasitic C_{OSS} network. In this example, one capacitor is pre-charged to 35V, the other to 0V.

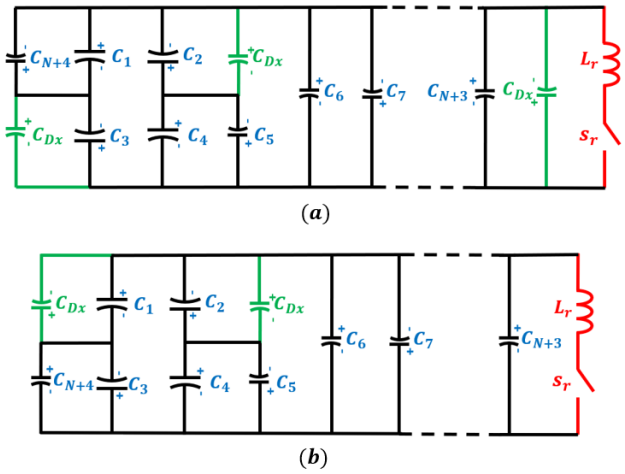

Fig. 9. AC model placement of dummy non-linear C_{OSS} capacitors (green) for (a) odd, and (b) even conversion ratios of a similar inductively loaded CW converter.

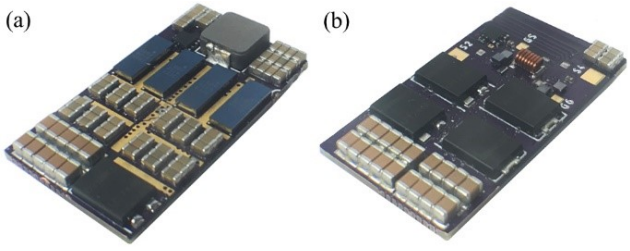

Fig. 10. Photograph of prototype measuring 25.3 x 13.5 x 4.2 mm^3. (a) Top. (b) Bottom.

limiting performance, but simplifying design as diodes automatically perform near-ZVS [4,5]. A fully active design would require split-phase switching on several switches, adding to the control complexity, but saving on diode forward voltage losses and volume when operating at lower voltages. An active design would also allow for step-down conversion.

The converter was operated in resonant mode, with primary phase durations adjusted until ZCS conditions were met. As such, there is zero current in L_p when performing RCR of the switch parasitics during the deadtime between primary phase transitions. The precise duration of major phases is dictated by the choice of fly capacitors and primary inductance L_p and is beyond the scope of this work. In brief, L_p influences both switching loss, due to its effect on switching frequency, total converter volume, and the Q-factor of the primary resonant dynamics. Here L_p is chosen to be 100nH.

No steps were taken to satisfy the capacitor equalities described in Section II. As such, the RCR benefit seen with this prototype is regarded as worst-case with significant improvement expected in future revisions.

Figures 11 and 12 depict how the gate driving circuitry and RCR circuit were implemented. Similar to Fig. 2, diodes D_1 and D_2 are used here to relax the turn-off constraints of S_{11} and S_{10} respectively, which when combined constitute the effective switch S_r depicted in Fig. 3. S_{10} or S_{11} turns on immediately after a primary phase has ended, which in turn commences the RCR during the following deadtime interval. While not demonstrated with this prototype, it is possible to synthesize appropriate control signals for U5 and U6 using neighboring gate driver signals.

TABLE I. COMPONENT SELECITON

Type	Details	Part Number
L_P	100nH 45A 3.6mΩ	IHLP2020BZERR
S_{1-4}	40V 90A 1.5mΩ	EPC2024
C_{OUT}	28x 0.1uF 250V	CGA4J3X7T2E104M125AE
S_{5-9}	Schottky 60V 8A	DST860S
$C_{FLY,1-4}$	9x 0.1uF 100V	GCJ188R72A104KA01D
C_{IN}	26x 0.1uF 100V	GCJ188R72A104KA01D
U_{1-4}	Gate Driver	LMG1205YFXR
$R_{G,1-4}$	0Ω 0201	ERJ-1GN0R00C
$C_{BP,1-6}$	25V 0.1uF 0201	GRM033C81E104KE14
S_{10-11}	60V 1.7A 45mΩ	EPC2035
D_{1-2}	0402 40V	DB2G40800L1
L_r	19.4nH 2.9A	0806SQ-19NJLB
U_{5-6}	Inverter	SN74LVC1G04YZVR

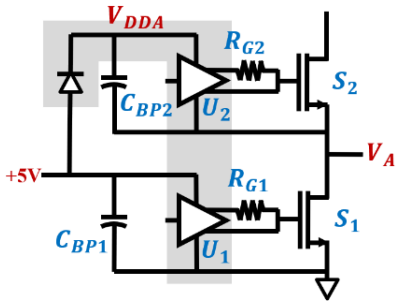

Fig. 11. Implementation of S_{1-2} (and likewise S_{3-4}). Grey region indicates elements within the LMG1205 gate driver.

Figure 13 shows the converter volume breakdown and illustrates significant potential for increased density using improved assembly methods and substrates or monolithic integration.

The converter was tested over an input voltage range of 24V-32V and achieved a maximum output power of 261.7W. The resulting maximum power density was 181.8kW/liter with a switching frequency, f_{SW}, of approximately 840kHz. For V_{IN}=32V and a 261.7W load, the output voltage is 5.8% lower than the ideal 1:5 conversion ratio, dropping to 150.75V due to internal converter losses.

The next set of figures show measured results emphasizing the improvement due to RCR. Figure 14 depicts measured efficiency curves for the same converter with and without RCR enabled. Up to a 61% reduction in total losses is observed when using RCR. Similar efficiency curves are observed in Fig. 15 for several different input voltages all with RCR enabled.

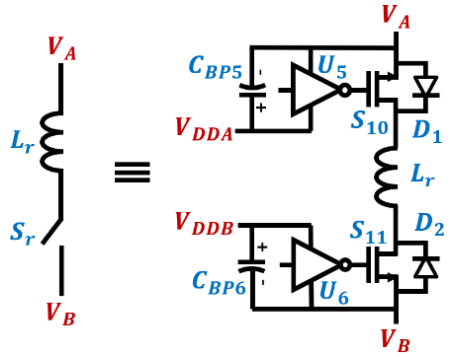

Fig. 12. Implementation of RCR circuit. Diodes D_1 and D_2 act to relax the turn-off timing constraints on S_{11} and S_{10} respectively.

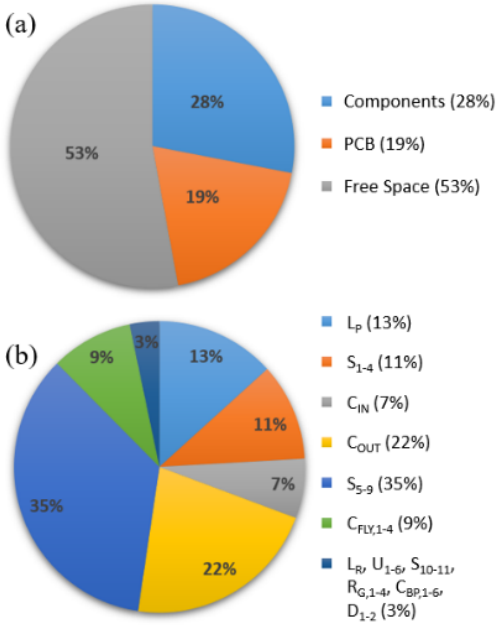

Fig. 13. (a) Converter volume breakdown. (b) Component volume breakdown.

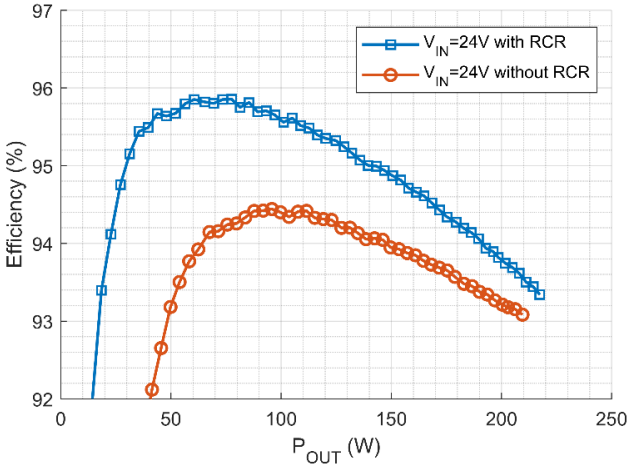

Fig. 14. Measured efficiency versus output power with and without RCR.

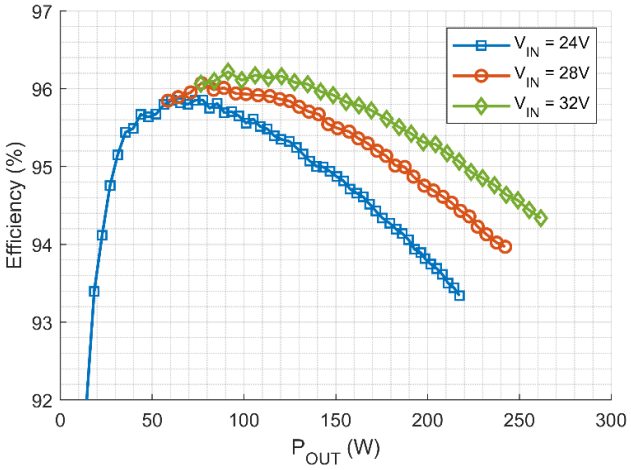

Fig. 15. Measured efficiency versus output power for several different input voltages all using RCR.

Figures 16 and 17 show measured voltage waveforms of nodes V_A and V_B over a full converter switching period. RCR is disabled in Fig. 16 resulting in significant ringing throughout the converter as C_{OSS} energy is dissipated. Also noted is apparent peak positive clipping of nodes V_A and V_B. This is likely due to ringing inducing reverse conduction in the GaN-FETs and results in the output voltage being driven much higher than anticipated at light-load as stored C_{OSS} energy is driven onto the output. This effect is depicted clearly in Fig. 18 where at light-load the converter with disabled RCR sees an effective conversion ratio of 1:6.9 as opposed to its nominal 1:5. This light-load output voltage peaking increases voltage stress and devices must be rated at much higher voltages than their expected range if this is to be tolerated. To resolve this in practice, an output shunt resistor may be included to ensure a load is always present, but this ultimately degrades efficiency. Conversely, Fig. 17 depicts V_A and V_B waveforms with greatly diminished ringing with RCR enabled.

Figures 19 and 20 show closeup measured waveforms of a major phase transition with both RCR enabled and disabled for comparison. Note that V_A and V_B are equal to V_{DS1} and V_{DS3}, respectively. With RCR disabled, V_A and V_B transition to their new bias points abruptly once the next phase commences. With

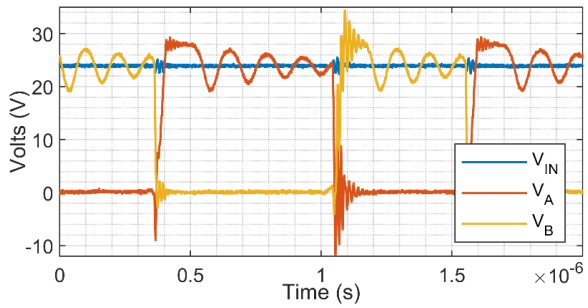

Fig. 16. Measured waveforms **without RCR**. Ringing indicates significant C_{OSS} energy dissipation. R_{LOAD}=3.2kΩ.

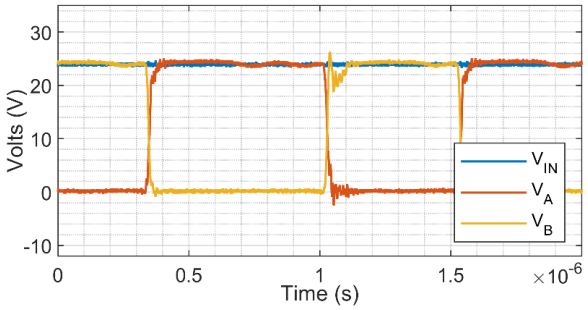

Fig. 17. Measured waveforms **with RCR** enabled show significantly reduced ringing. R_{LOAD}=3.2kΩ.

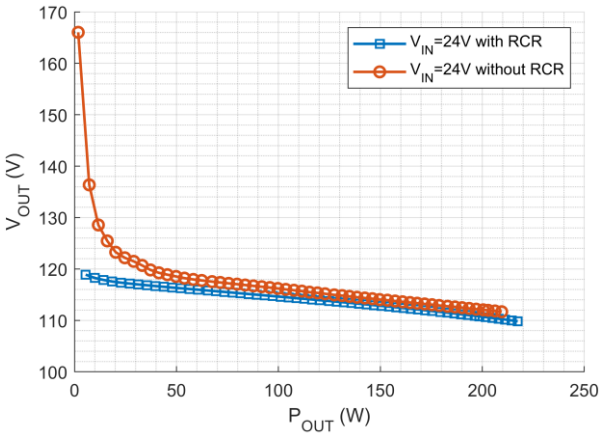

Fig. 18. Measured V_{OUT} for swept load with both RCR enabled and disabled.

RCR enabled, L_r acts during the deadtime to smoothly redistribute charge across all C_{OSS} capacitors such that the C_{OSS} of all switches with upcoming ON states are discharged to near 0V. As such, ZVS is achieved and results in minimal loss being incurred upon initialization of the subsequent major phase.

IV. Conclusion

This work proposes the use of resonant charge redistribution (RCR) to significantly reduce switching losses in a hybridized switched-capacitor DC-DC converter. Preliminary analysis is presented with a subsequent prototype demonstrating up to a 61% reduction in total losses with the RCR circuitry occupying a near-negligible 0.74% of the total solution volume. This result is achieved despite taking no steps to address identified capacitor constraints for optimal performance, leaving room for significant improvement.

Application of RCR moves the envelope with respect to sizing and optimization of primary switching devices, allowing increased switch sizes for reduced conduction loss without incurring additional switching loss.

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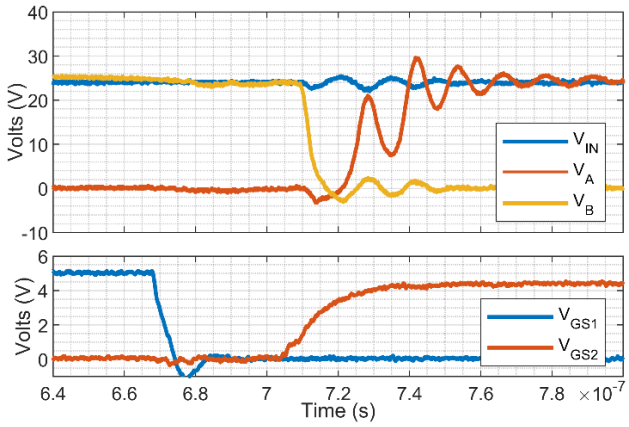

Fig. 19. Close-up of transition between the two major phases **without RCR** enabled. Abrupt charge redistribution between parasitic C_{OSS} capacitors results in switching loss and ringing. R_{LOAD}=640Ω.

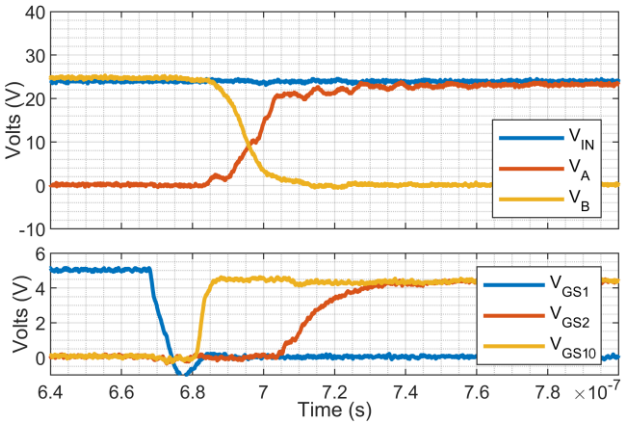

Fig. 20. Close-up of transition between two major phases **with RCR** enabled. L_r facilitates smooth redistribution of charge before the subsequent phase begins. Node voltages V_A and V_B are equivalent to the V_{DS} voltages of S_1 and S_3 respectively, illustrating near ZVS upon commencement of the subsequent phase. All other switches are shifted in voltage due to C_{FLY} offsets and experience similar near-ZVS due to RCR. R_{LOAD}=640Ω.