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Steady-State Analysis of Series-Capacitor Buck Converters in Discontinuous Capacitor Voltage Mode

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***Abstract*—The series-capacitor buck (SCB) converter is a compact and highly-efficient alternative to the multi-phase buck converter and has recently been demonstrated in data center applications. To achieve high power density, it is desirable to reduce the total flying capacitance in this topology. However, for sufficiently small flying capacitances, a discontinuous capacitor voltage mode (DCVM) manifests, leading to an imbalance in inductor currents. This work provides a detailed derivation of the relationship between the critical capacitance describing the onset of DCVM and converter operating parameters. Moreover, the inductor current imbalance is characterized through the development of a clamped steady-state model. To recover balancing when flying capacitance below the critical value is used, a technique to drive the branches with modified duty cycles in a constant power regime is proposed. Experimental validation of the steady-state model and recovery of inductor current balancing are demonstrated on a 4-branch SCB prototype.**

I. Introduction

Hybrid switched-capacitor (SC) converters enable highly energy-dense and efficient power conversion solutions, primarily due to their high utilization of capacitive energy storage components [1], [2]. The series-capacitor-buck (SCB) converter [3]–[6] shown in Fig. 1 is one such hybrid SC converter that has recently been adopted in data center applications, both as a stand-alone high step-down solution [7], and embedded within 48:1 hybrid switched-capacitor converters [8]–[12]. Relative to the multi-phase interleaved buck converter, the SCB converter offers decreased switch voltage rating, which enables use of lower-voltage switches with higher figure-of-merit [13]; extended duty cycle, which enables a large conversion ratio with sufficient duty cycle resolution; and decreased total inductor volt-seconds, which allows for decreased inductive energy storage volume. Additionally, the SCB converter exhibits automatic balancing of inductor currents under small-ripple conditions, eliminating the need for active current-balancing control [4], [7].

Pushing the limits of power density in hybrid SC converters requires decreasing passive energy storage (for the same processed power) or increasing power processing capability (for the same passive energy storage). The effects of these modifications for inductive energy storage components are well understood. Namely, as inductance is decreased or the operating voltage (V_{in} for a fixed conversion ratio) is increased, inductor current ripple increases, eventually driving the converter into either a diode-clamped discontinuous conduction mode

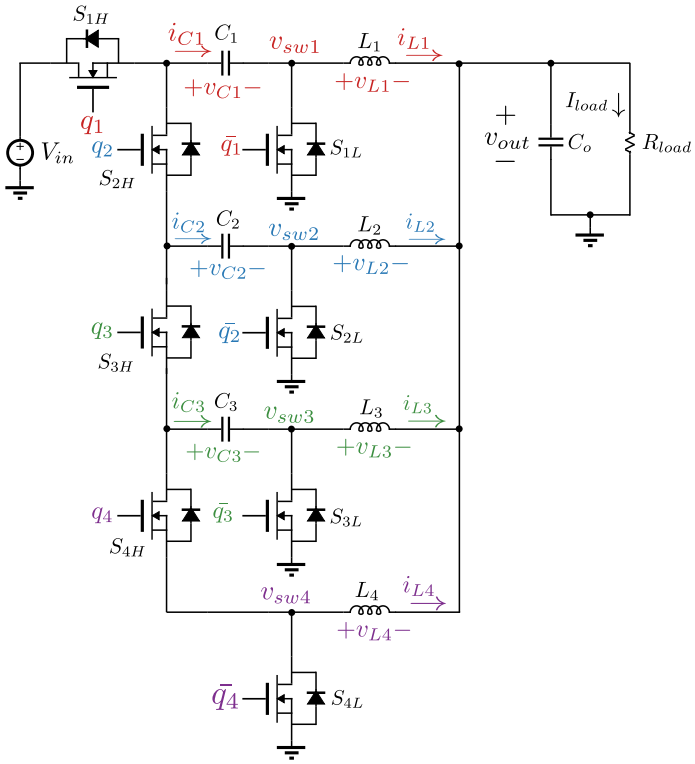

Fig. 1: Schematic of a 4-branch series-capacitor-buck converter [4]–[6]

(DCM), or a synchronously-rectified forced continuous conduction mode. The duals of these effects for capacitive energy storage components are less often discussed. As capacitance is decreased or load current is increased, capacitor voltage ripples increase until clamping occurs through the reverse-conduction of a typically employed voltage-unidirectional low-side switch, driving the converter into a discontinuous capacitor voltage mode (DCVM) [14], [15].

The consequences of DCVM operation for the series-capacitor-buck converter are the subject of this work. In particular, the automatic balancing of inductor currents observed under small flying capacitor voltage ripple conditions is lost, posing additional converter failure mechanisms through inductor saturation or thermal runaway of the branches processing increased current.

The remainder of this paper is organized as follows: In section II, the origin of inductor current imbalance is identified and explained through the concept of effective duty cycle.

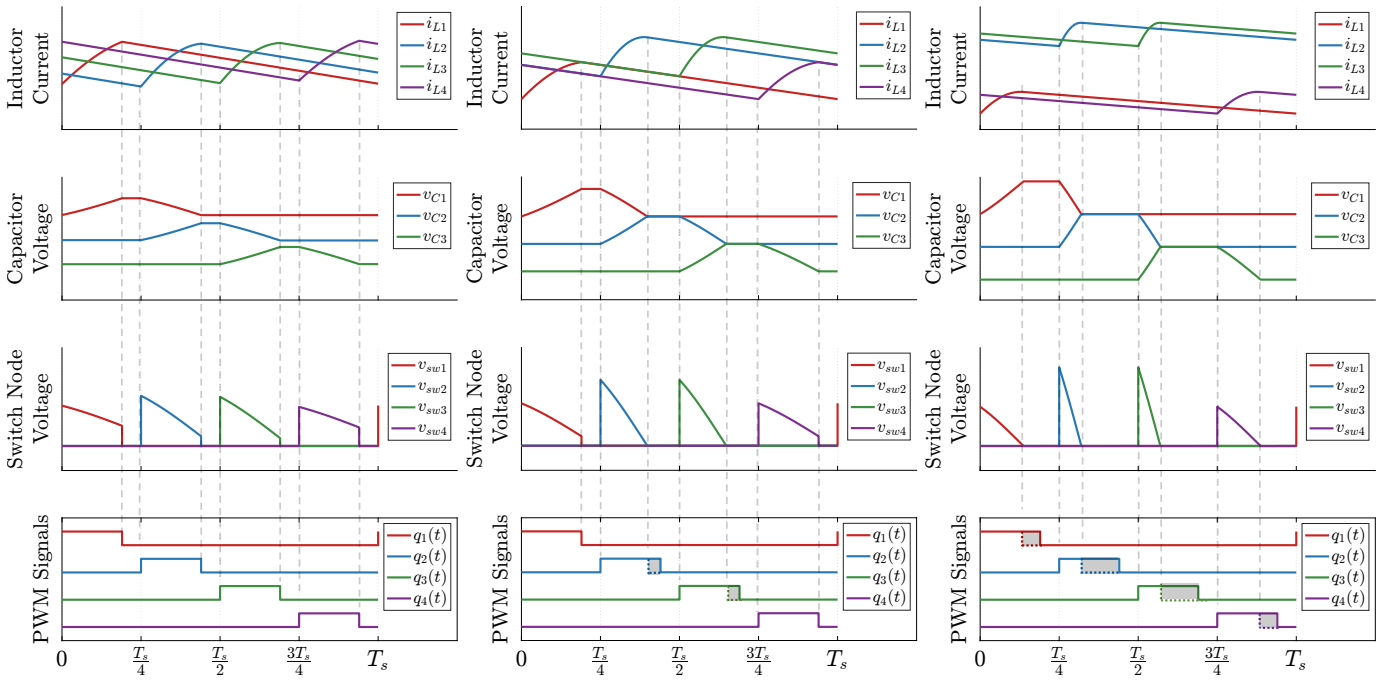

Fig. 2: Simulated inductor currents (top), flying capacitor voltages (middle), switch node voltages (middle), and PS-PWM control signals (bottom) for three modes of operation. (a) Standard CCVM operation. (b) DCVM operation with inner branches exhibiting decreased effective duty cycle. (c) DCVM operation with all branches exhibiting decreased effective duty cycle

To characterize the imbalance, the steady-state solution in DCVM is found by imposing a "clamping condition." A modified duty cycle scheme is proposed to recover inductor current balancing despite the presence of voltage clamping conditions. In section III, experimental results from a 4-branch SCB converter hardware prototype are presented. The experimental results show agreement with the proposed model and demonstrate that the modified duty cycle control scheme recovers inductor current balancing.

II. Modeling

An N-branch, N-phase SCB converter has N uniformly phase-shifted complementary switch pairs, each driven by a pulse-width modulated control signal with duty cycle $0 \leq D \leq \frac{1}{N}$ (PS-PWM) [4], as shown in Fig 2(a). Inductor current, capacitor voltage, and switch node voltage waveforms for an exemplar 4-branch SCB operating in continuous capacitor voltage mode (CCVM, the dual of continuous conduction mode) are shown in Fig. 2(a). With sufficiently large flying capacitance, the midrange values (average of maximum and minimum values) of the flying capacitor voltages balance to $V_{ck} = \frac{N-k}{N} V_{\text{in}}$ for $k = 1, 2, 3$ and the average inductor currents are $I_{Lk} = \frac{I_{\text{load}}}{4}$ for $k = 1, 2, 3, 4$.

A. Origin of Inductor Current Imbalance

Imbalance in the inductor currents arises when flying capacitor voltage ripples are sufficiently large to cause the capacitor voltages to clamp to each other or the supply rails (i.e., V_{in} and ground). Two critical capacitances define the onset of clamping. Below a first critical threshold $C_{\text{crit},1}$, neighboring flying capacitor voltages become equal before the end of the $q(t) = 1$ switching phase, causing the switch nodes of the inner (2 through N-1) branches to clamp to ground through reverse conduction of their low-side switches. This shortens the $q(t) = 1$ state and lengthens the $q(t) = 0$ state, resulting in a decreased effective duty cycle $D_{eff} < D$ for the inner branches (Fig. 2(b)). When the flying capacitance is further decreased below a second critical threshold $C_{\text{crit},2}$, the outer (1 and N) branches exhibit decreased effective duty cycle due to v_{C1} clamping to V_{in} and v_{CN-1} to ground (Fig. 2(c)).

In Fig. 2(b) and (c), the decreased effective duty cycles of inner branches with respect to outer branches causes the observed imbalance in steady-state inductor currents. By applying steady-state charge balance to the outermost capacitors (C_1 or C_{N-1}), a relationship between the steady-state inductor currents is derived as

$$\begin{aligned} \langle i_{\text{C,outer}} \rangle_{T_s} &\approx D_{\text{eff,outer}} I_{\text{L,outer}} - D_{\text{eff,inner}} I_{\text{L,inner}} = 0 \\ \implies \quad I_{\text{L,outer}} &= \frac{D_{\text{eff,inner}}}{D_{\text{eff,outer}}} I_{\text{L,inner}} < I_{\text{L,inner}} \end{aligned} \tag{1}$$

B. Steady-State Model in DCVM

The extent of imbalance and the critical values of flying capacitance below which imbalance occurs are important in the design of a compact a reliable converter, particularly if flying capacitors are implemented with technologies that exhibit degradation over time, such as class II multi-layer ceramic chip capacitors [16], [17]. In this section, analytic

expressions for the critical capacitances are derived, along with the resulting steady-state solution in this regime of operation.

If the voltages of neighboring flying capacitors clamp in steady-state (Fig. 3), their midrange values may be related to their ripples as

$$\frac{1}{2}\Delta v_{Ck-1,pp} + \frac{1}{2}\Delta v_{Ck,pp} = V_{Ck-1} - V_{Ck} \tag{2}$$

Assuming small inductor current ripple, this clamping condition may be solved for the effective duty cycle of the k^{th} branch ($k = 2, 3, ..., N-1$) as

$$D_{\text{eff},k} = 2\frac{C_{k-1}C_k}{(C_{k-1}+C_k)I_{Lk}T_s}(V_{Ck-1} - V_{Ck}) \tag{3}$$

This formulation for the effective duty cycle of an inner branch may be generalized to include the cases where v_{C1} clamps to V_{in}, $v_{\text{C}N-1}$ clamps to ground, or clamping is absent as follows.

$$D_{\text{eff},k} = \begin{cases} D_k, & C_{\text{eff},k} \geq C_{\text{thresh},k} \\ \frac{C_{\text{eff},k}}{I_{\text{Lk}}T_s}2\Delta V_k, & C_{\text{eff},k} < C_{\text{thresh},k} \end{cases}$$

$$\text{where} \quad C_{\text{eff},k} = \begin{cases} C_1 & k = 1 \\ C_{k-1}||C_k & k = 2, 3, ..., N-1 \\ C_{N-1} & k = N \end{cases}, \tag{4}$$

$$\Delta V_k = \begin{cases} V_{\text{in}} - V_{\text{C1}} & k = 1 \\ V_{\text{C}k-1} - V_{\text{C}k} & k = 2, 3, ..., N-1 \\ V_{\text{C}N-1} & k = N \end{cases},$$

$$\text{and} \quad C_{\text{thresh},k} = \frac{I_{\text{Lk}}D_kT_s}{2\Delta V_k}$$

in which D_k is the driven duty cycle of the k^{th} complementary switch pair, $C_{\text{eff},k}$ is the effective series capacitance during the k^{th} primary switching phase, and $C_{\text{thresh},k}$ is the capacitance threshold for clamping of the k^{th} branch.

The generalized formulation (4) highlights the difference between inner and outer branches. If one assumes equal duty cycles $D = D_1 = D_2 = ... = D_N$ driving all branches and equal flying capacitances $C = C_1 = C_2 = ... = C_{N-1}$ that are sufficiently large for CCVM operation, then the differences between neighboring flying capacitor voltages balance to $\frac{V_{\text{in}}}{N}$ (i.e. $\Delta V_k = \frac{V_{\text{in}}}{N}$ for $k \in \{1, 2, ..., N\}$), and the load current splits equally between the inductors. Thus, the clamping threshold C_{thresh} is the same for all branches. However, two capacitors charge in series during the primary switching phase of the inner branches while only one charges for the outer branches, making $C_{eff} = \frac{C}{2}$ for the inner branches and $C_{eff} = C$ for outer branches. This disparity in effective capacitance causes the inner branches to exhibit decreased effective duty cycle at larger values of C than the outer branches, and in turn, the inductor currents to imbalance as predicted by (1).

The final step in finding the steady-state state solution in DCVM operation is to substitute the effective duty cycles described by (4) into a system of inductor volt-second and capacitor charge balance equations.

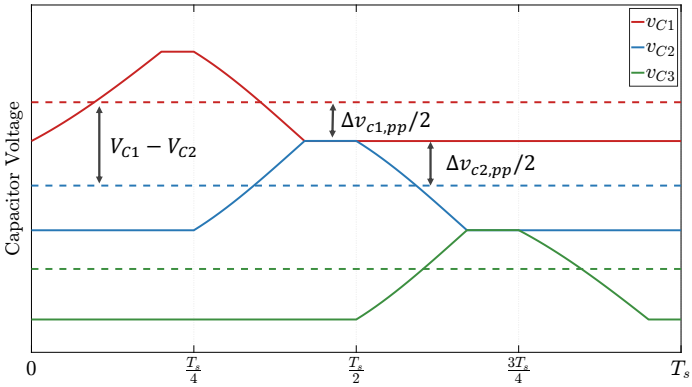

Fig. 3: DCVM clamping condition

$$\begin{aligned} \langle v_{\text{Lk}} \rangle_{T_s} &= D_{\text{eff},k}\Delta V_k - V_{\text{out}} = 0, k \in \{1, ..., N\} \\ \langle i_{\text{Ck}} \rangle_{T_s} &= D_{\text{eff},k}I_{\text{Lk}} - D_{\text{eff},k+1}I_{\text{Lk}+1} = 0, k \in \{1, ..., N-1\} \\ \langle i_{\text{Co}} \rangle_{T_s} &= I_{\text{L1}} + I_{\text{L2}} + ... + I_{\text{LN}} - \frac{V_{\text{out}}}{R_{\text{load}}} = 0 \end{aligned} \tag{5}$$

Under the assumptions of equally driven duty cycles, equal flying capacitances, and only the inner branches exhibiting clamping (i.e. $C_{\text{crit},2} < C < C_{\text{crit},1}$, as in Fig. 2(b)), the solution of (5) subject to (4) is given by

$$\begin{aligned} V_{\text{C},N-1} &= \frac{V_{\text{in}} - (N-2)K}{2} \\ I_{\text{L1}} &= I_{\text{LN}} = \frac{CK}{DT_s} \\ V_{\text{C}k} &= V_{\text{C}N-1} + (N-k-1)K \\ k &= 1, 2, 3, ..., N-2 \\ I_{\text{L2}} &= I_{\text{L3}} = ... = I_{\text{L}N-1} = \frac{Cf_sK^2}{V_{\text{out}}} \\ V_{\text{out}} &= DV_{\text{C}N-1} \\ K &= \frac{DI_{\text{load}}T_sV_{\text{in}}}{2CV_{\text{in}} + (N-2)DI_{\text{load}}T_s} \end{aligned} \tag{6}$$

where the solution is parameterized in terms of K, the steady-state difference between neighboring flying capacitor midrange voltages.

The solution with all branches exhibiting clamping (i.e. $C < C_{\text{crit},2}$, as in Fig. 2(c)) is given by

$$\begin{aligned} V_{\text{C}N-1} &= \frac{V_{\text{in}}}{2(N-1)} \\ I_{\text{L1}} &= I_{\text{LN}} = \frac{I_{\text{load}}}{2(N-1)} \\ V_{\text{C}k} &= V_{\text{C}N-1} + (N-k-1)K \\ k &= 1, 2, 3, ..., N-2 \\ I_{\text{L2}} &= I_{\text{L3}} = ... = I_{\text{L}N-1} = \frac{I_{\text{load}}}{N-1} \\ V_{\text{out}} &= \frac{CK^2}{I_{L2}T_s} \\ K &= \frac{V_{\text{in}}}{N-1} \end{aligned} \tag{7}$$

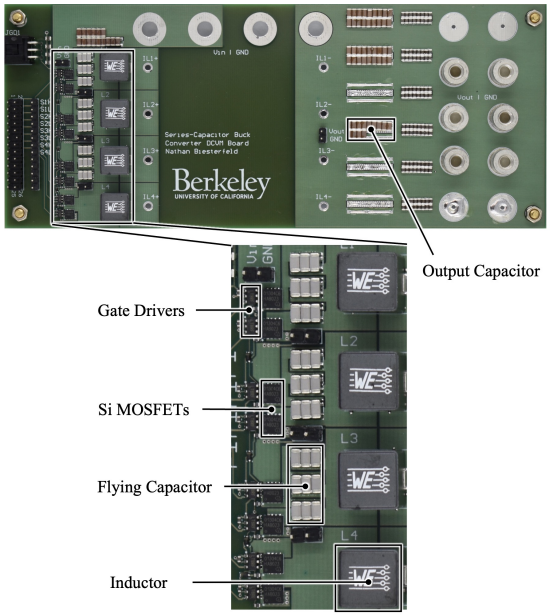

Fig. 4: 4-branch series-capacitor-buck converter hardware prototype with key components labelled

TABLE I: Component Details

Component	Description	Part Number
$S_{1-4H,L}$	40V Si MOSFET	IQE013N04LM6CG
$C_1 - C_4$	Flying Capacitor	GRM31C5C1E474JE01L
L	Inductor	7443330470
C_o	Output Capacitor	C3216X5R1A686M160AC
Gate Driver	8V, 4A	LTC4440-5

Critical values of flying capacitance are given by

$$C_{\text{crit},1} = \frac{DI_{\text{load}}T_s}{V_{\text{in}}} \tag{8}$$

$$C_{\text{crit},2} = \frac{DI_{\text{load}}T_s}{2V_{\text{in}}} \tag{9}$$

The steady-state solution with a reverse conduction voltage $-V_{\text{diode}}$ for all switches is included in the Appendix.

TABLE II: Operation Parameters

Parameter	Value
V_{in}	48 V
D	0.2
f_s	100 kHz
I_{load}	60 A

C. Recovery of Inductor Current Balancing via a Modified Duty Cycle Scheme

In an aggressive design where the flying capacitance C is designed to only slightly exceed $C_{\text{crit},1}$, degradation of capacitance over time, or a momentary increase in load current can invoke DCVM operation. A conventional closed-loop controller designed to match V_{out} to a reference would increase the driven duty cycle of all switch pairs, but only the outermost branches would exhibit the increased duty cycle (due to clamping of the inner branches), further exacerbating the inductor current imbalance.

Instead, inductor current balance may be maintained in the presence of clamping by driving the outer branches with the decreased effective duty cycle exhibited by the inner branches. When the switches are controlled in this manner, all branches exhibit the same, decreased effective duty cycle, so $I_{Lk} = \frac{I_{\text{load}}}{N}$ and $V_{\text{out}} = \frac{D_{eff}V_{\text{in}}}{N}$, just as if the converter were operating in CCVM. However, by driving the outer branches with decreased duty cycle, V_{out} is decreased due to v_{sw1} and v_{swN-1} exhibiting a decreased average voltage.

Under the proposed modified duty cycle scheme, output voltage is proportional to duty cycle (see (6)) and duty cycle is inversely proportional to load current (see (4)), so the output voltage is inversely proportional to the output current. Thus, operation in DCVM with this scheme corresponds to a constant-power regime. This behavior is beneficial, as it provides both an increased degree of short circuit and overload protection, and a soft limit to the maximum power demands of certain PoL applications, including those employing dynamic voltage scaling (DVS) (e.g., [18]).

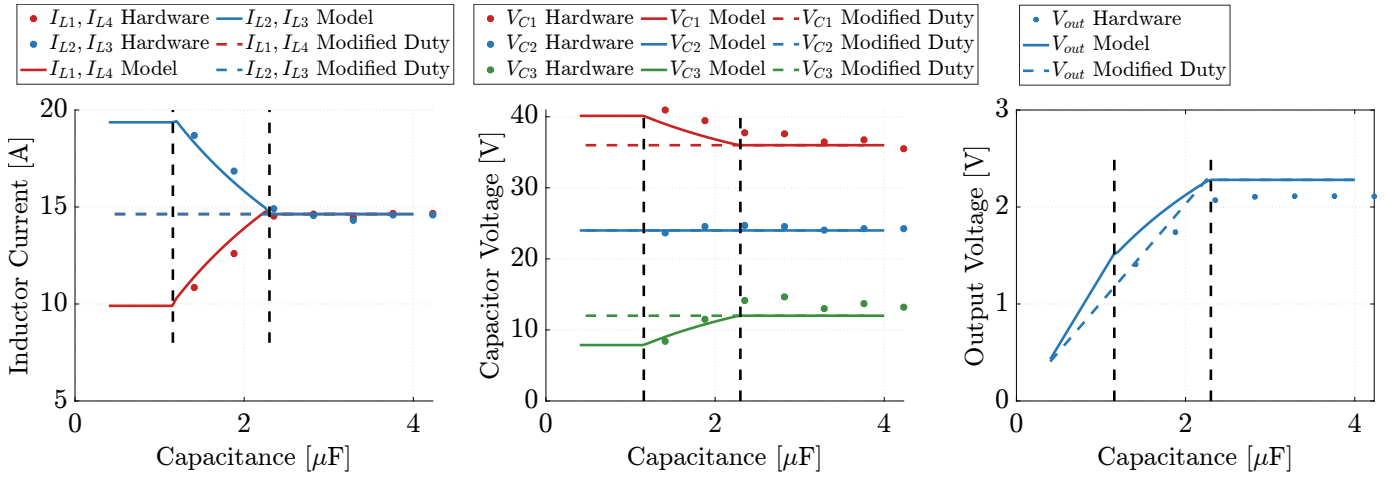

Fig. 5: Average inductor currents (left), midrange flying capacitor voltages (middle), and output voltage (right) measured on hardware, predicted by the steady-state DCVM model of section II-B, or for the modified duty cycle scheme of section II-C for several values of the flying capacitance.

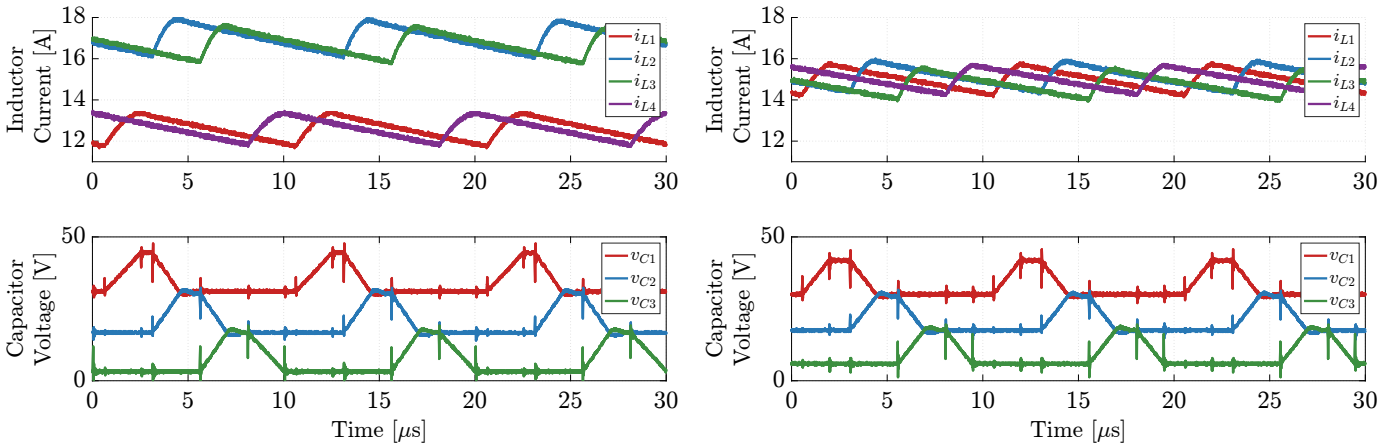

Fig. 6: Recovery of inductor current balance in DCVM via modified duty cycles. (a) imbalanced inductor currents under equal driven duty cycles (b) recovered inductor current balancing via duty cycle modification

III. Experimental Validation

The steady-state DCVM model and modified duty cycle scheme developed in section II are validated on the 4-branch series-capacitor buck prototype in Fig. 4 with the components summarized in Table I. The converter is operated according to the parameters in Table II.

A. Steady-State DCVM Model

The steady-state DCVM model is validated by measurement of the average inductor currents, midrange flying capacitor voltages, and output voltage across seven discrete values of flying capacitance (3x-9x $0.47\,\mu F$). The results are compared to the steady-state DCVM model (6),(7), with and without modified duty cycle, in Fig. 5.

All measurements follow the trends predicted by the steady-state DCVM model. As the flying capacitance decreases below $C_{\text{crit},1}$, the inner inductor currents increase, the outer inductor currents decrease, V_{C1} increases, V_{C3} decreases, and V_{out} decreases.

Discrepancy between model and hardware, particularly in the midrange flying capacitor and output voltages, is primarily due to the DCVM model not accounting for parasitic resistances in the circuit.

B. Recovery of Inductor Current Balancing in DCVM

Measured flying capacitor voltage and inductor current waveforms for equal driven duty cycles $D = 0.2$ and for flying capacitance $C = 1.88\,\mu F$ are shown in Fig. 6a. As discussed in section II-A, the voltages of neighboring flying capacitors clamp together before the end of each primary switching period, leading to a mismatch in effective duty cycle that causes the observed inductor current imbalance.

Recovery of inductor current balancing is demonstrated by decreasing the duty cycle of the outer branch PWM signals $q_1(t)$ and $q_4(t)$ to $D_{outer} \approx 16\%$ to match the inner branches. As a result, the inductor currents remain balanced despite clamping of flying capacitor voltages due to each branch exhibiting the same effective duty cycle (Fig. 6b).

It should be noted that while the decrease in duty cycle of outer branches was performed manually, a DCVM active balancing controller based on models dual to well-developed DCM averaged-switch models could, in principle, be employed.

IV. Conclusions

This work identifies mismatched effective duty cycles resulting from different effective series capacitances between inner and outer branches as the origin of inductor current imbalance in DCVM operation of the SCB converter. The imbalance is characterized by development of a DCVM steady-state model, and critical capacitances describing the onset of capacitor voltage clamping are presented. Recovery of inductor current balancing via a modification to the branch duty cycles is discussed, and the work is validated on a hardware prototype.

V. Appendix

The steady-state DCVM solution described by (6)-(9) is easily modified to account for the voltage drop across switches in reverse conduction, $-V_{\text{diode}}$. Following the same steps of formulating the effective duty cycle in terms of inductor currents, capacitor voltages, and V_{diode}, and then substituting into the system of steady-state balance equations, it can be shown that

$$
\begin{aligned}
V_{\text{C}N-1} &= \frac{V_{\text{in}} - (N-2)K}{2} \\
I_{\text{L1}} = I_{\text{L}N} &= \frac{C(K + \frac{1}{2}V_{\text{diode}})}{DT_s} \\
V_{\text{C}k} &= V_{\text{C}N-1} + (N-k-1)K \\
k &= 1, 2, 3, ..., N-2 \\
I_{\text{L2}} = I_{\text{L3}} = ... = I_{\text{L}N-1} &= \frac{Cf_s(K + V_{\text{diode}})(K + \frac{1}{2}V_{\text{diode}})}{V_{\text{out}} + DV_{\text{diode}}} \\
V_{\text{out}} &= DV_{\text{C},N-1} \\
K &= \frac{DI_{\text{load}}T_s(V_{\text{in}} + 2V_{\text{diode}}) - CV_{\text{diode}}(V_{\text{in}} + (N-1)V_{\text{diode}})}{2C(V_{\text{in}} + (N-1)V_{\text{diode}}) + (N-2)DI_{\text{load}}T_s}
\end{aligned}
\tag{10}
$$

for $C_{crit2} < C < C_{crit1}$. For $C < C_{crit2}$,

$$\begin{aligned} V_{\mathrm{C}N-1} &= \frac{V_{\text{in}}}{2(N-1)} - \frac{N-2}{4(N-1)} V_{\text{diode}} \\ I_{\mathrm{L}1} &= I_{\mathrm{L}N} = \frac{I_{\text{load}}}{2(N-1)} \\ V_{\mathrm{C}k} &= V_{\mathrm{C}N-1} + (N-k-1)K \\ k &= 1, 2, 3, ..., N-2 \\ I_{\mathrm{L}2} &= I_{\mathrm{L}3} = ... = I_{\mathrm{L}N-1} = \frac{I_{\text{load}}}{N-1} \\ V_{\text{out}} &= \frac{C}{I_{L2} T_s}(K + \frac{V_{\text{diode}}}{2})(K + V_{\text{diode}}) - D V_{\text{diode}} \\ K &= \frac{V_{\text{in}} + \frac{1}{2} V_{\text{diode}}}{N-1} \end{aligned} \tag{11}$$

where

$$C_{crit1} = \frac{2 I_{\text{load}} D T_s}{2V_{\text{in}} + N V_{\text{diode}}} \tag{12}$$

$$C_{crit2} = \frac{D I_{\text{load}} T_s (V_{\text{in}} + (\frac{3}{2}N - 1) V_{\text{diode}})}{(V_{\text{in}} + (N-1)V_{\text{diode}})(2V_{\text{in}} + N V_{\text{diode}})} \tag{13}$$

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