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Digital Switching CMOS Power Amplifier for Multiband and Multimode Handset Applications

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Lawrence E. Larson

2013
The dissertation of Toshifumi Nakatani is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego
2013
To my parents and brother,
and
to my beloved wife, Yoko.

両親、弟へ
そして
親愛なる妻、陽子へ
EPIGRAPH

“The more I learn, the more I realize I don’t know. The more I realize I don't know, the more I want to learn.”

— Albert Einstein
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ABSTRACT OF THE DISSERTATION

Digital Switching CMOS Power Amplifier for Multiband and Multimode Handset Applications

by

Toshifumi Nakatani

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2013

Professor Peter M. Asbeck, Chair

This thesis is directed towards the development of a digitally-assisted radio frequency power amplifier (RF PA) which is one of the potential solutions to realize a multiband and multimode transmitter with high efficiency for handset applications. To improve efficiency and linearity in multiple conditions, PA circuits and digital signal processing (DSP) algorithms are co-designed. In the dissertation, a proposed architecture employs a current-mode class-D (CMCD) configuration for high efficiency, and a polar modulation scheme driven by digital inputs. Detail design, fabrication and experimental results are given for circuit implementation and DSP of this architecture.

First, a multiband watt-class complementary metal–oxide–semiconductor (CMOS) PA is demonstrated using 0.15 μm CMOS integrated circuits (ICs), off-chip inductor and balun. To obtain high breakdown voltage, stacked field effect transistors (FETs) are used. The CMCD PA is tuned by band-switching capacitors, operating in the 0.7-1.8 GHz frequency band. The overall efficiencies of 27.1 / 25.6 % are achieved at 30.2 / 28.9 dBm CW output powers and 0.85 / 1.75 GHz carrier frequencies, respectively.
Next, to achieve wide output power dynamic range, an architecture consisting of small segmented unit-cells is introduced into the PA, where multiple three-state unit-cells are used and the state of each unit-cell is controlled to provide a specific output power. The overall dynamic ranges are expanded to approximately 90 dB and 85 dB at and 0.85 / 1.75 GHz, respectively.

The dissertation then presents digital modulation algorithms. The digital compensation techniques are developed to maintain linearity of an envelope modulator of the polar transmitter. A new digital pulse width modulation algorithm is also shown to partially suppress spurious signals associated with the digital input envelope signal. When wideband code-division multiple access (WCDMA) modulation is implemented, spur suppression of 9-10 dB is achieved while maintaining adjacent channel leakage power ratios within 3rd generation partnership project specifications.
Chapter 1

Introduction

1.1 Power Amplifiers for Handset Applications

1.1.1 Present Status of Handset Transmitters

The rapid growth in data communication using mobile phones has led to a demand for high data rates. In order to satisfy this demand, a typical mobile terminal, such as a cell phone, needs transceivers to address the proliferation of bands in present and emerging wireless systems. At present, multiple power amplifiers (PAs) are used in the same terminal in order to accommodate the different frequencies, bandwidths, peak output powers and modulation schemes required. Figure 1.1 shows photos of a commercial handset inside, where (a) five PAs and (b) radio frequency (RF) transceiver integrated circuit (IC) are mounted. Total area occupied by PAs is larger than that of the transceiver IC.
Figure 1.1: Photos of (a) power amplifier and (b) transceiver of commercial handset inside.
Figure 1.2 shows an example of RF transceiver block [1]. One or two paths are selected among many possible transmission and reception paths for a specified environment (area and operator). A received signal at the antenna is demodulated in the transceiver IC and provided to the modem IC, while a modulated RF signal is generated in the transceiver IC based on data from the modem IC. A PA is placed at each transmission path and works to amplify the RF signal only when the specific transmission path is selected.

Table 1.1 shows a representative progression of commercial RF transceiver ICs [2]. As the generation of the IC increases, the number of the air interfaces and global navigation systems also increases, while the size of the IC decreases by using advanced
semiconductor and package technologies. However, the number of PAs increases or does not change.

Table 1.1: Transition of commercial RF transceiver IC [2].

<table>
<thead>
<tr>
<th>Generation</th>
<th>3rd</th>
<th>4th</th>
<th>5th</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>RTR6285</td>
<td>RTR8600</td>
<td>WTR1605</td>
</tr>
<tr>
<td>Air Interface</td>
<td>GSM UMTS</td>
<td>GSM UMTS CDMA LTE</td>
<td>GSM UMTS CDMA LTE TD-SCDMA</td>
</tr>
<tr>
<td>Global Navigation Satellite System</td>
<td>GPS</td>
<td>GPS GLONASS</td>
<td>GPS GLONASS BeiDou</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18um</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Package</td>
<td>Plastic</td>
<td>Plastic</td>
<td>Wafer level</td>
</tr>
<tr>
<td>Size</td>
<td>64 mm²</td>
<td>48 mm²</td>
<td>25 mm²</td>
</tr>
</tbody>
</table>

The objective of this research is to explore a new architecture towards a golden single PA that can satisfy present and future needs, where it is important to realize multiband and multimode operation with low direct current (DC) power consumption.

1.1.2 Requirements for Power Amplifiers

In this section, requirements for PAs are briefly explained. As mentioned below, each standard has different requirements, which result in placing multiple PAs in the handset.

Figure 1.3 shows the transmitter (Tx) frequency bands specified in 3rd generation partnership project (3GPP) standards [3]-[5]. Even if the band VII (2.5-2.57 GHz) for worldwide interoperability for microwave access (WiMAX) application is excluded, PAs needs to cover in 0.7-2.0 GHz. In this dissertation, the bands in ranges from 0.7 to 1.0 GHz and from 1.4 to 2.0 GHz are called “low band” and “high band”, respectively.
The signal waveforms of 3GPP standards are categorized into roughly two, i.e. (a) constant and (b) non-constant envelopes, as shown in Figure 1.4. When the constant envelope signal, such as global system for mobile communications (GSM), is delivered, a PA can operate exclusively at its peak output power, where the PA tends to achieve maximum efficiency. On the other hand, in case of non-constant envelope, such as wideband code division multiple access (WCDMA) and 3rd generation long term evolution (3G LTE), the peak output power of the PA corresponds to the instantaneous peak of the envelope shown in in Figure 1.4 (b). Therefore, the PA on average works in back-off, where the efficiency is relatively lower. The degree of the back-off is called “peak-to-average power ratio (PAPR)”. Furthermore, linearity of the PA is required for this non-constant RF signal amplification.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>Low band 698-915 MHz</th>
<th>High band 1428-1980 MHz</th>
<th>WiMAX, etc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>1</td>
<td>1.5</td>
<td>2</td>
</tr>
</tbody>
</table>
Figure 1.4: (a) Constant envelope and (b) non-constant envelope modulated waveforms.

Figure 1.5 shows the output power dynamic range and bandwidth of the different standards. Since GSM uses constant envelope signal, i.e. PAPR of 0 dB, the required power dynamic range is 30 dB for the average power control, where the peak output power is 33 dBm at the antenna. If a loss between the PA and antenna is 2 dB, the output power of 35 dBm (3 W) is needed at the PA output. For WCDMA, not only the average power control (74 dB), but also modulation power control (40 dB) are required, and corresponding minimum output power, i.e. minimum resolution, is approximately -85 dBm at the PA output, while the PAPR is 3 dB and the required peak output power is approximately 30.5 dBm. The required bandwidths of the GSM and WCDMA are 0.2 MHz and 5 MHz, respectively. The required peak and minimum output powers of 3G LTE are approximately 31.5 dBm and -75 dBm, respectively, but the maximum signal bandwidth is 20 MHz. To cover all standards, the power dynamic range of 120 dB and the signal bandwidth of 20 MHz are needed.
Figure 1.5: Output power dynamic range and signal bandwidth of different standards.

A number of additional specifications are required from standards to be satisfied:

1) Error vector magnitude (EVM) [6], [7] is used to evaluate the signal integrity;
2) adjacent channel leakage power ratio (ACLR) [6], [7] is a spectral mask requirement to avoid blocking the spectrum of neighboring channels;
3) spurious emissions are also a spectral mask to prevent interference with other terminals and systems, whose frequency band is far from the Tx channel.

Other performance metrics are also critical, like area, cost and so on. As one of these factors, energy efficiency is quite important for PAs. If the RF output power, $P_{out}$, is delivered and the DC power, $P_{DC,f}$, is consumed at the final stage of the PA, the drain (output) efficiency [6], [7] is defined as

$$\eta \equiv \frac{P_{out}}{P_{DC,f}}$$

(1-1)
This is useful metric for evaluating output transistors. An alternative often used definition of the efficiency is power-added efficiency (PAE) [6], [7], which is written as

\[ PAE \equiv \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}_f}} \]

where \( P_{\text{in}} \) is the drive power of the amplifier. The efficiency of the definition is degraded from the drain efficiency as the power gain of the PA is reduced, especially when it is less than 10 dB.

Figure 1.6 shows the efficiency of a typical PA and the power probability distributions of the (a) constant and (b) non-constant modulated signals. The gray curve is the efficiency of the PA corresponding to constant amplitude cosine waves of a particular output power. When the envelope is constant, the efficiency is relatively high. In case of non-constant envelope, not only the peak efficiency but also back-off efficiency affects the total efficiency. Therefore, it is important to improve efficiency in back-off.

![Figure 1.6](image_url)

Figure 1.6: Efficiency of typical PA and power probability distributions of modulated signals, which are (a) constant envelope and (b) non-constant envelope.
One more factor, which is not specified in 3GPP standard, is receive band noise (RxBN). In full frequency-division duplex (FDD) system, transmitter and receiver work simultaneously, while both tend to share one antenna through a duplexer. If the transmitter delivers the modulated signal with large noise at the receive band, it degrades the signal-to-noise ratio of the receive signal because the isolation between transmitter and receiver ports of the duplexer is finite. If that occurs, once the handset receives a call far from the base station, it is likely that the call will be dropped once the handset starts to transmit due to “self-jamming” (which is a relatively bad customer experience).

Figure 1.7 shows a spectral mask of GSM / WCDMA Tx at (a) antenna and (b) PA output, where the Tx band is in a range from 1.805 GHz to 1.88 GHz. Isolation between PA, antenna and receiver are calculated based on the attenuations of an EPCOS duplexer [8]. The gray spectral mask is the spurious emission specified in 3GPP standard, where the minimum requirement is approximately -126 dBm/Hz at the antenna. However, in order for receiver to be able to entirely neglect the effect of the noise from the PA, the required noise level is -180 dBm/Hz, which is the black line. The requirement of the RxBN is 54 dB lower than the spurious emission specification. If the duplexer suppresses the noise from PA by 50 dB, the RxBN of -130 dBm/Hz is needed.
1.2 Basic Concept for Multiband and Multimode Power Amplifiers

1.2.1 Digitally-assisted RF Power Amplifiers

Figure 1.8 shows block diagrams of commercial PA modules for (a) GSM and (b) WCDMA applications [9]. The function of the PAs is merely to amplify the RF input signals. In Figure 1.8 (a), GaAs HBT based PAs are used and the bias and logic control are provided by the complementary metal–oxide–semiconductor (CMOS) controller. In
Figure 1.8 (b), the bias circuit is integrated, but a voltage of dynamic bias control is applied from the outside of the chip to enhance the PAE in back-off. However, there are two drawbacks in these approaches: First, the number of control lines of PAs is limited because the states of the PAs are controlled from outside of the chips. If many control lines are applied, more precise adjustment should be possible, but the number of the bonding pads increases, resulting in large chip size. Second, they use linear PAs, such as class-C and class-AB [7], whose performance tends to be sensitive to the threshold voltage of the main transistor. Since the variation of the threshold voltage is relatively large due to manufacturing, temperature and aging, the control capability of the linear PA is limited.

![Block diagrams of commercial PA modules for (a) GSM and (b) WCDMA applications][9]
A digitally-assisted PA is one of the potential solutions to realize multi-standard transmitters [10]-[13]. Co-design of digital signal processing (DSP) algorithms and PA characteristics can lead to improved efficiency and linearity in multiple configurations, where the signals applied to PA do not need to be same as the signal delivered and can be reformatted to be suitable for the PA to operate efficiently. It is attractive to integrate both DSP and PA into one die because 1) a higher clock rate can be maintained compared with multi-chip solutions, 2) many control lines can be readily accommodated, and 3) it is relatively easy to manage delay time between control lines.

Figure 1.9 shows examples of digitally-assisted PAs reported on (a) [10] and (b) [11], where the PAs are directly driven by digital pulses generated in a DSP. In Figure 1.9 (a), an oversampling modulator delivers 1bit band-pass delta-sigma modulated RF signal into the PA. The delivered signal integrity is highly dependent on the precision of the clock signal and insensitive to the process variation and aging. In Figure 1.9 (b), the PA is segmented into unit-cells and the number of active unit-cells is selected by the DPS. With increasing the number of active unit-cells, higher output power is provided.

It is relatively easy to realize these scenarios using Silicon technology instead of compound devices because large digital libraries are available. One of the challenges for this approach is to implement watt-level Silicon PAs because they have typically lower power handling capability, i.e. lower breakdown voltage and current driving, compared with GaAs/GaN devices with same \( f_t \).
1.2.2 Watt-level CMOS Power Amplifiers

Many Silicon CMOS PAs have been previously demonstrated [14]-[16]. CMOS devices are well-suited for digitally controlled amplifiers because their currents can be easily controlled by full-swing digital input signals and there are no undesirable currents, as occur from input diode turn-on with SiGe/GaAs hetero-junction bipolar transistors (HBTs) and GaAs field-effect transistors (FETs).

Figure 1.10 shows the output power vs operating frequency of published CMOS PAs reported in [17]. (DAT is “distributed active transformer” proposed by California
Institute of Technology [15]) From the survey, PAs with the output power of 35 dBm (3W) has been realized in the range from 0.7 GHz to 2 GHz.

Several multiband CMOS PAs have also been reported [17]-[22]. In [17], high-Q varactor based tunable matching networks are integrated and output power of 27-28 dBm is achieved at 0.9, 1.8, 1.9 and 2.0 GHz. In [19], fixed off-chip matching networks of a class-E amplifier are used to cover 0.8-2.0 GHz. In [20], band-switching feedback and output resonator circuits adjust the output impedance to 50 Ω over 0.9-3.0 GHz. In [21], by applying an integrated band-switching output capacitor of a voltage-mode class-D (VMCD) amplifier, a 3 dB bandwidth from 0.45-0.73 GHz with an output power of 20 dBm is achieved. In [22], a quad-band PA for 1.9, 2.3, 2.6 and 3.5 GHz is implemented by changing the number of active transistors.
To date, however, a few watt-class CMOS PAs have demonstrated non-constant envelope signals, such as WCDMA. Also, the peak output powers of the reported multiband CMOS PAs were less than 28 dBm.

1.3 Fundamental Techniques for Digitally-assisted Power Amplifiers

1.3.1 Switching-mode RF Amplifiers

One of attractive configurations is a switching-mode amplifier for these digitally-assisted PAs using CMOS FETs. The switching-mode amplifier basically consists of main transistor and resonator as shown in Figure 1.11. The main transistor acts as a switch instead of a current source, and is supposed to be driven by pulse signals. Thanks to the resonator, there is ideally no overlap between the output voltage across the transistor and the current flowing through the transistor, which results in the drain efficiency of 100%. Power amplifiers classified as class-D and -E operates as switching-mode RF amplifiers [7].

Figure 1.11: Simple configuration of switching-mode RF amplifiers.
CMOS PAs suffer from low power handling capability. A relationship between ideal peak voltage and current of a current-mode class-D amplifier, which is one of switching-mode amplifier, is written as (See Chapter 3):

\[ V_{\text{peak}} = \pi \cdot \frac{P_{\text{out}}}{I_{\text{peak}}} \]

(1-3)

On the other hand, that of a conventional class-B linear amplifier [7], [23] can be expressed as:

\[ V_{\text{peak}} = 8 \cdot \frac{P_{\text{out}}}{I_{\text{peak}}} \]

(1-4)

Figure 1.12 shows the peak voltage vs peak current of switching-mode (black) and linear-mode (grey) amplifiers when the output power of 35 dBm is delivered. From the results, the switching-mode amplifier can relaxed the trade-off between peak voltage and peak current, which is appropriate for Silicon PAs.

![Figure 1.12: Peak voltage vs peak current of switching-mode and linear-mode amplifiers when output power of 35 dBm is delivered.](image-url)
Figure 1.13 shows the waveform and simple circuit configuration of the class-D (or VMCD) amplifier, which is a straightforward approach. Switches Q1 and Q2 are switching alternatively, which results in a square voltage waveform. Using a series LC resonator, the current waveform becomes a half sine wave without overlapping the voltage.

Figure 1.13: Waveforms and circuit configuration of class-D (or VMCD) amplifier.

The class-D amplifier is very simple, but a big jump of its voltage at switching timing may cause over-and under-shoots. To avoid the issue, the class-E amplifier was proposed by Sokal, et al. [24]. Figure 1.14 shows the waveforms and circuit configuration. By applying a shunt capacitor and shifting the resonance frequency of the series resonator to be slightly higher than the resonance frequency of the carrier frequency, the output voltage and its derivative become zero when the switch turns on.

Figure 1.14: Waveforms and circuit configuration of class-E amplifier.
Figure 1.15 shows the waveforms and circuit configuration of the current-mode class-D (CMCD) amplifier [25]. The voltage and current waveforms are a dual of the (voltage-mode) class-D amplifier. The output voltage of the CMCD amplifier is also zero when the switch turns on (although the derivative is relatively high). A benchmarking of the switching-mode RF amplifiers will be carried out in Chapter 2.

![Waveforms and circuit configuration of current-mode class-D (CMCD) amplifier](image)

Figure 1.15: Waveforms and circuit configuration of current-mode class-D (CMCD) amplifier.

### 1.3.2 Transmitter Architectures for Non-constant Envelope Modulation Using Switching-mode Amplifier

Unlike linear amplifiers, the output power of switching-mode amplifiers ideally does not change even if the RF input power increases because the transistor works as a switch. In this section, possible architectures for non-constant envelope modulation using switching-mode amplifiers are introduced.

Figure 1.16 shows a simple block diagram of an out-phasing modulator originally proposed by Chireix [26]. At time, $t$, two constant amplitude and different phase modulated (PM) signals, $S_1(t)$ and $S_2(t)$, are applied to two PAs, respectively, where $S_1(t)$ and $S_2(t)$ can be written as
\[ S_1(t) = \cos(\omega t + \cos^{-1} A(t)) \]  
\[ (1-5) \]
\[ S_2(t) = \cos(\omega t - \cos^{-1} A(t)) \]  
\[ (1-6) \]
where \( A(t) \) is the amplitude modulated (AM) signal and \( \omega \) is the angle frequency. So that if the gain of the PA is \( G \), the combined output is calculated from
\[ S_{out}(t) = G[S_1(t) + S_2(t)] \]
\[ = 2G \cdot A(t) \cdot \cos \omega t \]  
\[ (1-7) \]
As a result of the process, an amplified original modulated signal is reproduced using constant envelope amplifiers.

Figure 1.17 shows a simple block diagram of a polar (envelope elimination and restoration: EER) modulator originally proposed by Kahn [27]. A PM signal is applied into the RF input of the PA and an AM signal is supplied to the DC input of the PA. The PA works as a multiplier. Since the output power is basically proportional to the square of the DC supply voltage or current, it is relatively easy to apply the switching-mode
amplifier to the polar modulator. The architecture shown in Figure 1.9 (b) is alternative demonstration of the polar modulator.

Figure 1.17: Simple block diagram of polar (EER) modulator.

Figure 1.18 shows a simple block diagram of an RF digital modulator [28]. The idea of this architecture is to directly generate RF modulated signals from DSP using a sampling frequency much higher than the RF carrier frequency. The signal applied to the PA has constant envelope, but has a modulation of its pulse widths or duty cycles so that the output power becomes also modulated. The resulting spectrum contains the desired output components, although it also has quantization noise, pushed into spectral regions outside the desired channel. An output filter is necessary to remove the out-of-band components. An appropriate architecture will be also discussed in Chapter 2.
1.4 Objectives and Organization of Dissertation

The objective of this work to explore an innovative multiband and multimode PA for handset applications, using an architecture suitable for fully digital control. The contributions of this dissertation are to establish a new switching-mode amplifier-based transmitter architecture; develop fundamental circuit configurations and DSP algorithms to satisfy requirements from standards; and validate these novel techniques using test chips and instruments as a preliminary demonstration toward realizing a single golden PA. The experimental results should be useful as a guide for future handset transceiver products.

This dissertation consists of seven chapters. The chapters are organized as follows (after this introduction chapter):

The second chapter starts by proposing a new digitally-assisted RF power amplifier architecture, where a CMCD configuration for high efficiency in the RF power amplifier, and a polar modulation scheme driven by digital inputs, are applied. Challenges of the proposed architecture are summarized, based on measured results using
discrete devices and simulated results. Subsequent sections of the thesis cover circuit implementation (Chapters 3, 4 and 5) and digital signal processing (Chapter 6) for this architecture. In addition, an overview of the chipset development is introduced that will assist in understanding the subsequent chapters, since the functions of test chips increase step-by-step over a couple of generations.

The third chapter is dedicated to demonstrate a watt-class PA using bulk CMOS technology. The circuit design of a CMCD PA is examined, in which stacked FETs are used to obtain high breakdown voltage. A buck converter with the maximum switching frequency of up to 200 MHz is employed as an envelope modulator of the polar transmitter. Finally, the implementation, board design and experimental results are presented and discussed.

The fourth chapter focuses on multiband functionality implemented for the proposed PA. A band-switching resonator, operating in the 0.7-1.8 GHz frequency band, is used for the digital polar transmitter, where one demonstration is carried out using on-chip 9 V\textsubscript{p-p} band-switching capacitor and together with an off-chip inductor, and a fully integrated variable resonator is used for another. In addition, for the off-chip inductor demonstration, a doughnut-shaped Guanella reverse balun is applied to achieve a 1-to-4 impedance transformation with less than 1 dB insertion loss and 0.5-2.1 GHz frequency band. In the measurement, only by changing the resonance frequency of the output resonator, watt-level CMOS power amplifiers are successfully demonstrated in the low and high cellular frequency bands.

The fifth chapter looks at a new polar transmitter architecture to achieve wide output power dynamic range, where a structure consisting of small segmented unit-cells
is introduced into the power amplifier and envelop modulator. Multiple three-state unit-cells are used for the driver and final stages of the CMCD PA and the state of each unit-cell is controlled to provide a specific output power. To improve the efficiency in power back-off, a new operation mode analogous to switched capacitor operation is realized using the proposed envelope modulator. Lastly, experimental results are shown, where a very wide power dynamic range is achieved compared with existing polar transmitters.

The sixth chapter describes the development of digital modulation algorithms to generate non-constant envelope RF signal using the proposed polar transmitter. The digital compensation techniques are developed to maintain linearity of an envelope modulator. In addition, a new digital pulse width modulation algorithm is also shown to partially suppress spurious signals associated with the digital input envelope signal. Multiband operation and wide average power control are demonstrated using test chipsets discussed in previous chapters.

The seventh chapter concludes the whole dissertation, and future directions in multiband and multimode PA work are suggested.
Chapter 2

Digital Switching CMOS Power Amplifier Architecture

2.1 Introduction

As described in Chapter 1, new architectures using digitally-assisted techniques should be explored to realize a multi-standard PA. For more flexible digital control, it is desirable to integrate the PA and DSP into Silicon. It is appropriate for the operation of Silicon PAs to be switching-mode because the requirements of the peak voltage and current for the PA are relaxed, and efficiency is increased. However, the switching-mode amplifier has a limited sensitivity to variations in input amplitude and often requires other means, such as DC control, load impedance control and digital modulation, to change output amplitude.

This thesis describes a compatible digitally-controlled polar modulation approach for waveforms with time-varying envelopes. The polar transmitter architecture is a promising candidate for linear amplification with highly efficient non-linear switching-mode amplifiers. In previous works [29]-[31], linear regulators or switching-linear hybrid regulators are used as envelope modulator inputs, and flexibility is sacrificed. In
[13], [32] and [33], DC-DC converters have been used to provide envelope modulation, where the digital inputs, such as $\Delta \Sigma$ and $\Delta$ modulations and pulse width modulation (PWM), are applied with operating frequency in the range from 4 MHz to 250 MHz. However, the RF output power is only up to 0.3 W (25 dBm).

In this work, the proposed polar transmitter employs a CMCD RF PA, which is suitable for watt-level Silicon PAs, and a buck converter envelope modulator, using digital pulse width modulation (DPWM) based on up to 200 MHz pulse repetition rate synchronized by up to 12 GHz clock.

Challenges of the polar modulation transmitter using switching-mode PA and envelope modulator have been summarized by Raab [34] and following papers [35]-[37]. These challenges include the following: 1) time misalignment between envelope and carrier; 2) finite bandwidth of the envelope modulator; 3) hardware imperfection including feed-through of the PA. For the time misalignment of AM-PM paths, some high performance calibration algorithms have been reported [38]-[41] (and, as a result, this challenge is outside of the scope of this thesis.) However, to address the finite bandwidth of AM path, one must overcome the trade-off between spurious products and nonlinearity due to memory effects. Also, the feed-through of the PA, which limits the minimum output power, is one of the remaining major issues. It is difficult to improve these nonlinearities even if memory-less digital pre-distortions (DPDs) [42]-[45] are applied.

In this chapter, challenges of the proposed transmitter (including multiband PA and RxBN in addition to these issues) are summarized. The solutions for these challenges are discussed in the following chapters.
To begin, the details of the proposed digital polar transmitter will be explained, including selection of switching-mode amplifier architecture. Then challenges of the proposed architecture will be discussed from the circuit design and digital signal processing points of view. Finally, an experimental chip set fabrication for prototype demonstration will be described.

2.2 Proposed Digital Switching CMOS Power Amplifier

2.2.1 Selection of Switching-mode Amplifier Configuration

In this section, three major switching PAs introduced in Chapter 1 are compared for Silicon PAs. Figure 2.1 shows circuit schematics of (a) CMCD, (b) VMCD and (c) class-E. For fair comparison, the configurations of VMCD and Class-E are changed to correspond to differential circuits. Load impedances and DC supplies are selected for peak voltage of 5V at the output power of 34 dBm and carrier frequency of 0.8 GHz.

In Figure 2.1 (a), the on-resistance and output capacitance of the switch (shown in the gray line) are selected to correspond to an n-channel metal–oxide–semiconductor (NMOS) gate width of 20 mm (Jazz 0.18 µm technology), which is large enough for DC current of 1.6 A. The loaded quality factor of the parallel resonator is designed to be 2.
Figure 2.1: Circuit configuration of differential switching-mode amplifiers. (a) CMCD, (b) VMCD and (c) class-E.
The output capacitance of the switch used for the CMCD PA implementation is found to be too large for VMCD PA use because the drain efficiency is significantly degraded due to output capacitor loss. In Figure 2.1 (b), the capacitance is optimized to obtained highest efficiency in the condition of constant capacitance × on-resistance product, where the capacitance is 1/3 times (5 pF), while the on-resistance is 3 times (105 mΩ). The loaded quality factor of the series resonator is 0.8, in order for the inductor to be less than 1.3 nH.

In Figure 2.1 (c), the on-resistance and output capacitance of the switch are the same as those of Figure 2.1 (a) (although the peak current of the switch is approximately 1.5 times higher). Using a 25.5 pF capacitor between two switches, wider bandwidth of the class-E amplifier is obtained compared with only shunt capacitors. The loaded quality factor of the series resonator is 2.2, in order for the inductor and capacitor to be less than 1.3 nH and 80 pF, respectively.

Figure 2.2 shows simulated (a) drain efficiency and (b) peak voltage of the three types of switching-mode amplifier, where the DC supply voltage (or DC supply current) is set to correspond to output power of 34 dBm over frequency. The carrier frequency is in the range from 0.65 to 0.95 GHz. From these results, the VMCD amplifier suffers from low drain efficiency due trade-off between $R_{on} I^2$ and $C_p V^2$ losses. In addition, VMCD PA needs over 5 V DC supply voltage. Therefore, a boost converter is needed. Regarding as the class-E amplifier, the peak voltage achieves almost 7 V at 0.95 GHz and higher break down switch is needed. The CMCD amplifier has lower peak voltage and higher efficiency, which are attractive for Silicon PA implementation.
Figure 2.2: Simulated (a) drain efficiency and (b) peak voltage over frequency of three switching-mode PAs in the condition that the output power is 34 dBm.

Results of comparing the switching-mode amplifiers are summarized in Table 2.1. The CMCD amplifier has relatively low output capacitance loss and peak voltage sensitivity over frequency. These properties are suitable for Silicon PAs, which tend to
have large parasitic capacitance and low breakdown voltage compared with compound semiconductor devices. In addition, no p-channel metal-oxide-semiconductor (PMOS), whose on-resistance tends to be higher than that of same size NMOS, is needed for the CMCD amplifier. Therefore, the CMCD configuration is used in this work.

Table 2.1: Benchmark of switching-mode amplifier.

<table>
<thead>
<tr>
<th></th>
<th>CMCD</th>
<th>VMCD</th>
<th>Class-E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low CV$^2$ Loss</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>(Zero Voltage Switch)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No P-ch FET</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>$V_{\text{peak}}$ Sensitivity</td>
<td>Low</td>
<td>fixed</td>
<td>High</td>
</tr>
</tbody>
</table>

2.2.2 Selection of Transmitter Architecture for Non-constant Envelope Signal

In order to deliver a non-constant envelope signal from a CMCD amplifier, we compared three types of transmitter architectures introduced in Chapter 1. Figure 2.3 shows block diagrams of (a) polar transmitter, (b) outphasing transmitter and (c) pulse density modulation (PDM) transmitter [46], respectively. In this study, an ideal current source is used for the polar and PDM transmitters. For the outphasing transmitter, a constant DC voltage is supplied through large inductors (to optimize linearity) and an ideal adaptive Chireix power combiner [47], [48] is applied (to optimize high efficiency) although the circuit configuration is complicated. In the following simulation, the FET model of Jazz 0.18 μm technology and ideal passive components are used.

Figure 2.4 shows the linearity of three transmitters, where the inputs of (a) polar, (b) outphasing and (c) PDM transmitters are DC current, cosine of outphasing angle and
pulse density, respectively. The output power of the polar transmitter is linear, while the outphasing transmitter shows some non-linearity due to the mismatch of two paths in the adaptive Chireix combiner. The PDM transmitter also shows some non-linearity because some expected pulses disappear at the transition from “00” state to “10” state.

Figure 2.3: Block diagram of transmitter architecture for switching-mode amplifier. (a) polar transmitter, (b) outphasing transmitter and (c) pulse density modulation transmitter.
Figure 2.4: Simulated output powers of (a) polar, (b) outphasing and (c) PDM transmitters. ($f_c = 0.85$ GHz)
Figure 2.5: Simulated (a) drain efficiency and (b) driver and final stage efficiency vs output power. ($f_c = 0.85$ GHz)

Figure 2.5 shows the simulated (a) drain efficiency and (b) driver and final stage efficiency vs output power of the transmitters with a CMCD PA (where the driver and final stage efficiency is defined as the ratio between the RF output power and the sum of driver and final stage DC power consumptions). The polar transmitter maintains high drain efficiency in back-off, while the drain efficiency of the PDM transmitter decreases because the transmitter delivers some amount of power in the out-of-band frequency. The drain efficiency of the outphasing transmitter is also degraded because the effective
load impedance increases. In this case, the corresponding loaded quality factor of the CMCD PA increases, while the unloaded quality factor is maintained. As a result, the output loss and the efficiency are degraded. The driver and final stage efficiency of the polar transmitter is highest in the range from 5 dB to 15 dB back-off.

From the preliminary simulation, we decided to use the polar transmitter due to high linearity and efficiency although an envelope amplifier is needed to amplify the envelope signal, and its efficiency is an important consideration for the overall system. In the next section, an envelope amplifier controlled by digital input is discussed.

### 2.2.3 Envelope Amplifier Investigation

Envelope signal generation for a digitally-driven polar transmitter has been discussed in [28]. Figure 2.6 shows the proposed architecture, where an envelope amplifier with serial input is driven by a non-return-to-zero (NRZ) binary pulse sequence and the amplified signal is delivered to the PA after being smoothed by an envelope inductor ($L_{env}$). In order for the applied signal to follow the expected envelope waveform, encoding algorithms were studied using Matlab simulation and it was shown that the RxBN of a DPWM is better than that of a low-pass ΔΣ modulation. (This discussion will be revisited in Chapter 6.) The switching frequency of the DPWM pulses was 62.5 MHz.

In this work, we start our investigation from the architecture.

The difference between analog PWM and DPWM is briefly explained in the following. Figure 2.7 shows block diagrams and waveforms of (a) analog PWM and (b) DPWM. In Figure 2.7 (a), the modulated pulses are generated from the comparison between the analog input and a triangle wave. This method requires generation of an analog modulation signal and also an analog triangle wave. On the other hand in Figure
2.7 (b), DPWM pulses can be digitally generated from $2^{N_{be}}$ bit data using the oversampled clock ($f_0$), which is $2^{N_{be}}$ time faster than the PWM switching frequency ($f_{sw}$). Clocks at such high speeds should be available due to the steadily progressing CMOS technology.

Figure 2.6: Block diagram of digital polar transmitter, where envelope amplifier is driven by DPWM signal following envelope data.

Figure 2.7: Block diagrams and waveforms of (a) analog PWM and (b) DPWM.
For the envelope amplifier, there are two types of non-inverting step-down switching-mode DC-DC converters. Figure 2.8 illustrates circuit schematics of (a) buck converter [49] and (b) single-ended primary-inductor converter (SEPIC) [49], respectively. In order to achieve higher output impedance at the carrier frequency, additional inductor is applied for the SEPIC, while no additional component is needed for the buck converter. Since the SEPIC is a kind of buck-boost converter, the supply voltage of the SEPIC is half of that of the buck converter. In the following simulation, ideal switches with $R_{on} = 65 \, \text{m}\Omega$ and $C_d = 100 \, \text{pF}$ and ideal inductors of 250 nH with series resistance of 100 m$\Omega$ are used. The load resistance representing the PA is 2.5 $\Omega$ and the switching frequency of the pulse width modulated signal applied to the converters is 50 MHz.

![Circuit schematic of (a) synchronous buck converter and (b) synchronous SEPIC.](image)

Figure 2.8: Circuit schematic of (a) synchronous buck converter and (b) synchronous SEPIC.

Figure 2.9 shows the simulated regulator efficiency vs output power of the switching-mode regulators. From the results, the buck converter achieves significantly higher efficiency at the peak output current, while the efficiency of the SEPIC goes down as the output current is increased due to inefficiency of the boost-mode operation. In
addition, there are many components in the SEPIC, which causes the degradation of the peak efficiency. Therefore, we decided to use the buck converter for the proposed architecture.

![Graph of simulated regulator efficiencies of buck converter and SEPIC.](image)

Figure 2.9: Simulated regulator efficiencies of buck converter and SEPIC. \( f_{sw} = 50 \text{ MHz} \)

### 2.2.4 Proposed Baseline Transmitter Architecture

Based on the several preliminary simulations discussed in the previous sections, we proposed a watt-class CMOS amplifier, whose block-level architecture is shown in Figure 2.10. A DSP is used to provide a DPWM waveform to the buck converter which encodes the output AM. The buck converter in turn supplies AM current to the CMCD PA. The DSP also provides a constant amplitude PM signal to the CMCD amplifier. An overall RF modulated signal is provided from the CMCD PA. One of the merits of the proposed architecture is high ideal efficiency due to “zero voltage switching” characteristics of the PA. It is important because CMOS devices have small power handling capability and high parasitic components. Additionally, the polar modulation
scheme improves the linearity of the inherently non-linear switching-mode PA. Finally flexible control results from fully digital input.

![Diagram of proposed baseline architecture of digital polar transmitter.](image)

**Figure 2.10:** Proposed baseline architecture of digital polar transmitter.

### 2.3 Challenges of Circuit Design of Proposed Architecture

#### 2.3.1 Multiband Operation of Watt-level CMOS Amplifier

A challenge of multiband operation of watt-level CMOS amplifier is discussed based on [50], where CMCD amplifiers were implemented with GaInP/GaAs HBTs. Figure 2.11 (a) shows the schematics of CMCD amplifier for simulation. An input balun generates differential input signals and an output balun converts the balanced output to single-ended output signal. Input and output matching networks are applied for each transistor to increase tuning flexibility. Figure 2.11 (b) shows a photograph of the
CMCD amplifier prototype. The input and output matching network are tuned for maximum efficiency.

Figure 2.11: (a) Schematic and photograph of the CMCD amplifier [50]. The overall amplifier employed external matching and baluns.

Figure 2.12 shows the measured collector efficiency, gain vs. frequency of the GaInP/GaAs HBT CMCD amplifier. The bases of the HBTs are biased to a turn-on
voltage of 1.2V for operation as switches. The collector bias is set to 3.4V. The CMCD amplifier shows a wide operating bandwidth. The collector efficiency is higher than 70% in the range from 0.65 GHz to 0.95 GHz. However, the required RF frequency band is from 0.7 GHz to 2.0 GHz and obviously wider bandwidth is needed. One of the possible solutions is to apply a variable resonator, which will be discussed in Chapter 4.

![Graph showing collector efficiency and gain vs. frequency.](image)

Figure 2.12: Measured collector efficiency, gain vs. frequency of CMCD amplifier, showing the operation bandwidth of 300 MHz for collector efficiency greater than 70% [50]. ($V_b = 1.2$ V, $V_{cc} = 3.4$ V)

### 2.3.2 Wide Power Dynamic Range of Polar Modulation Transmitter

The power dynamic range of a polar modulation transmitter is described using preliminary measured results of a CMCD PA designed by Dr. T.-P. Hung. Figure 2.13 shows the photo of the CMCD PA using Eudyna GaAs p-HEMT, where two discrete FETs are used as switches and two coaxial cable baluns are applied for the single-end to differential conversion. The resonance frequency of the output resonator is adjusted to be 1 GHz using the chip inductor and capacitor.
Figure 2.13: Photo of GaAs pHEMT CMCD PA designed by Dr. T.-P. Hung.

Figure 2.14 shows the DC voltage vs DC current of the final stage of the GaAs HEMT CMCD PA. A DC offset is apparent in the figure, which requires the calibration for the polar modulation. The gate Schottky diode causes the DC offset. Similar offset should appear when a bipolar transistor, such as SiGe HBT, is used as the switch in place of the HEMT. However, the offset should be negligible when CMOS devices are applied.

Figure 2.14: DC voltage vs DC current of final stage of GaAs HEMT CMCD PA. ($f_c = 1.0 \text{GHz}$)
Figure 2.15 shows the output power vs DC current of the GaAs HEMT CMCD PA. From the results, with decreasing DC current, the output power reaches a floor due to the leakage power from the input to the output, which is so-called “feed-through”. In order to satisfy the required power dynamic range, the feed-through needs to be reduced.

![Figure 2.15: Output power vs DC current of GaAs HEMT CMCD PA. \( f_c = 1 \text{ GHz} \)](image)

Figure 2.16 shows the efficiency vs output power of the GaAs HEMT CMCD PA. The drain efficiency of the CMCD PA is kept high in back-off, although the PAE is degraded. The constant input power required by the switching-mode PA causes the PAE degradation. Therefore, another challenge is to reduce the input power in back-off, while maintaining the switching-mode operation of the PA. These challenges will be investigated in Chapter 5.
2.3.3 High Switching Frequency Buck Converter as Envelope Modulator

In order to generate the envelope signal, a switching frequency in the range from several 10 MHz to 200 MHz is needed for the buck converter [28]. Challenges of the high switching frequency buck converter are evaluated in the following by measuring a discrete buck converter.

Figure 2.17 shows (a) circuit schematic and (b) photo of a buck converter using discrete devices. It is an asynchronous buck converter, consisting of PMOS and Schottky diode. Since the maximum voltage provided by the pulse pattern generator (Agilent 81442A) is 1.8 V, a high speed comparator (Maxim MAX999 [51]) is used as a 1.8 V-to-5 V level shifter. In addition, a driver amplifier (TI TPS2828 [52]) is inserted before the large PMOS. The air core inductor and 10 Ω load resistor are placed at the output. The size of the designed PCB is 35 mm × 25 mm.
Figure 2.17: (a) Circuit schematic and (b) photo of discrete buck converter.

Figure 2.18 shows the measured voltage waveform when the switching frequency is (a) 781.25 kHz and (b) 12.5 MHz. The duty cycle of the input signal is 50 %. In Figure 2.18 (a), the measured drain voltage becomes the expected waveform. However, with increasing switching frequency, the drain voltage waveform is corrupted as shown in Figure 2.18 (b). This occurs because it takes a while for Schottky diode to turn on. From these results, the switching speed of the discrete buck converter is limited due to
the delay at the diode. Therefore, it is important to use a synchronous buck converter. It is also effective to integrate dead-time generator, driver stages and final stage into one die.

The design of high speed buck converters will be explained in Chapters 3 and 5.

Figure 2.18: Measured output voltage waveforms of discrete buck converter when switching frequency is (a) 781.25 kHz and (b) 12.5 MHz.
2.4 Challenges of Digital Signal Processing for the Proposed Architecture

2.4.1 Wideband Envelope Signal Generation

In this section, challenges of digital envelope signal generation are described. At first, the clock image associated with the DPWM is discussed.

Figure 2.19 shows a simulation block diagram of a primitive digital polar modulation system. The system consists of DSP and analog blocks. In DSP block, I and Q inputs are converted into envelope and phase data. Envelope information is quantized into $N_{be}$ bits and transferred into the DPWM signal. The RF PM signal is generated using phase information and carrier frequency signal. In the analog block, within the PA, the AM data is combined with the PM data after smoothing by the customary inductor ($L_{env}$) at the output of the buck converter. In simulation, the PA effect is represented by simple multiplication. The envelope waveform and spectrum are measured at the output of the inductor and PA, respectively. The AM-AM characteristics are obtained after out-of-band noise is suppressed by the band-pass filter (BPF).

![Figure 2.19: Block diagram of primitive digital polar modulator system.](image-url)
Figure 2.20 shows the envelope current waveform when (a) $L_{env} = 10$ nH and (b) $L_{env} = 100$ nH. The blue curve is an ideal waveform and the red curve is the waveform of the primitive digital polar transmitter. WCDMA modulation (HPSK) with 3.3 dB PAPR is applied, using a symbol rate of 3.84 MS/s. The carrier frequency is 0.75 GHz. The number of bits of DPWM ($N_{be}$) is 6. When $L_{env}$ is small, large switching noise is shown. On the other hand, when $L_{env}$ is large, the waveform is distorted.

![Envelope current waveform of primitive digital polar modulator](image)

(a)

(b)

Figure 2.20: Envelope current waveform of primitive digital polar modulator when (a) $L_{env} = 10$ nH and (b) $L_{env} = 100$ nH. ($f_c = 0.75$ GHz, $f_{sw} = 46.08$ MHz, $N_{be} = 6$ bit)

Figure 2.21 shows the spectra when $L_{env}$ changes from 1 nH to 1000 nH. The black broken curve indicates the ideal WCDMA spectrum as a reference and the gray solid lines are 3GPP specs. With increasing $L_{env}$, the clock images decrease, while the adjacent channel leakage ratio (ACLR) is degraded.
Figure 2.21: Spectra of primitive digital polar modulator when $L_{env} = 1\sim1000$ nH. ($f_c = 0.75$ GHz, $f_{sw} = 46.08$ MHz, $N_{be} = 6$ bit)

Figure 2.22 shows the AM-AM input-output relationship when $L_{env} = (a)$ 10 nH and (b) 100 nH. The AM-AM relationship shows a correlation between the ideal envelope and the delivered (and possibly distorted) envelope signals, where ideally the distribution is located on the line from left-bottom to right-top. If the distribution makes a thin curve instead of a line, the system is non-linear but it is easily compensated by a memory-less digital pre-distortion (DPD). If the distribution is broadly spread, it indicates the system is distorted due to memory effects and memory DPD is needed. In Figure 2.22 (a), the system is relatively linear. However in Figure 2.22 (b), the simulated results show strong memory effect due to the large $L_{env}$. From these investigations, larger $L_{env}$ is appropriate to suppress the clock image, while it causes signal distortion. To overcome the trade-off, some techniques will be discussed in Chapter 6.
Figure 2.22: AM-AM characteristics of primitive digital polar modulator (a) $L_{\text{env}} = 10$ nH and (b) $L_{\text{env}} = 100$ nH. ($f_c = 0.75$ GHz, $f_{sw} = 46.08$ MHz, $N_{be} = 6$ bit)
2.4.2 Receive Band Noise Reduction

Lastly, a challenge for reducing the RxBN is described. Figure 2.23 shows calculated spectra of a primitive digital polar modulator, where the span is 300 MHz. The carrier frequency is changed to 1.75 GHz. The gray line shows the target spec of the RxBN when WCDMA band III is used. From the results, the noise floor of the simulated spectra is approximately 15 dB higher than the target spec even if the envelope inductor and switching frequency are optimized.

![Spectra of primitive digital polar modulator, where a span is 300 MHz.](image)

Figure 2.23: Spectra of primitive digital polar modulator, where a span is 300 MHz. ($L_{env} = 1\text{~}1000 \text{ nH}, f_c = 0.75 \text{ GHz}, f_{sw} = 46.08 \text{ MHz}, N_{bc} = 6 \text{ bit}$)

2.5 Chip Set Fabrication

In the following chapters, several chip sets of the proposed digital polar transmitter will be demonstrated, where the functions of the transmitters increase step by step. The purpose of the 1st generation transmitter is to realize a watt-class CMOS PA in
the low band. A low / high band-switching option is added for the 1.5th generation transmitter. Finally, on-chip transformer balun and wide power dynamic range function are implemented for the 2nd generation transmitter. The features of these generations are summarized in Table 2.2.

Table 2.2: Purpose of each generation of digital polar transmitter.

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st generation</td>
<td>Single-band watt-class CMOS PA</td>
</tr>
<tr>
<td>1.5th generation</td>
<td>Multiband watt-class CMOS PA</td>
</tr>
<tr>
<td>2nd generation</td>
<td>Multiband and wide power dynamic range PA</td>
</tr>
</tbody>
</table>

In this work, digital polar transmitters consist of a CMCD PA chip and a buck converter chip. Some off-chip components are used for 1st and 1.5th generation transmitters. Two types of printed circuit boards (PCBs) are designed for evaluation. The configuration of each generation is summarized in Table 2.3. Details of these configurations will be explained in Chapters 3, 4 and 5, respectively.

Table 2.3: Configuration of each generation of digital polar transmitter.

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>PA</th>
<th>Buck converter</th>
<th>Inductor</th>
<th>Balun</th>
<th>PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st generation</td>
<td>1st generation</td>
<td>1st generation</td>
<td>off-chip</td>
<td>off-chip</td>
<td>1st generation</td>
</tr>
<tr>
<td>1.5th generation</td>
<td>1.5th generation</td>
<td>2nd generation</td>
<td>bonding wire</td>
<td>off-chip</td>
<td>1st generation</td>
</tr>
<tr>
<td>2nd generation</td>
<td>2nd generation</td>
<td>2nd generation</td>
<td>on-chip</td>
<td>on-chip</td>
<td>2nd generation</td>
</tr>
</tbody>
</table>

2.6 Summary

A digitally-controlled polar transmitter with a CMCD CMOS PA is proposed as baseline architecture of this work, where a buck converter driven by the DPWM envelope signal is employed as an envelope amplifier. Challenges of the proposed architecture are
discussed from both circuit design and digital signal processing points of view. Finally, the overview of chip set fabrication is summarized.

2.7 Acknowledgements

The author is very grateful to Panasonic Corporation for valuable discussions and funding support, and to Dr. Jeremy Rode, Mr. Donald Kimball, Professor Lawrence Larson, and Professor Peter Asbeck for their valuable discussions and suggestions.

Some of the material in Chapter 2 is as it appears in "Digital-controlled polar transmitter using a watt-class current-mode class-D CMOS power amplifier and Guanella reverse balun for handset applications", T. Nakatani, J. Rode, D. F. Kimball, L. E. Larson, and P. M. Asbeck, published in IEEE Journal on Solid-State Circuits, vol. 47, no. 5. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.
Chapter 3

Watt-level CMOS Power Amplifier

3.1 Introduction

One of the challenges for the digitally-assisted RF PA is to implement a watt-level Silicon PA. A requirement of the peak voltage with moderate load resistance is still high although it is relaxed using a CMCD amplifier. To tolerate the high voltage swing without using any optional technologies, such as LDMOS, one of the possible solutions is a stacked FET [53], [54]. Several PAs using the stacked FETs have been reported for the envelope modulated supply voltage. In [55], a self-biased second gate configuration is used to improve the efficiency in up to 10 dB back-off. In [56], the load shared configuration between the driver and final stages are used and the driver stage provides the power in the deep back-off. However, the output power and efficiency of the first configuration decreases rapidly in the back-off of over 10 dB because the upper-tied FET turns off. The RF bandwidth of the second configuration is limited.

In this work, several second gate bias circuits are studied using the CMCD amplifier which is inherently a differential configuration. It is shown the resonant
frequency shift of the output resonator causes efficiency degradation in back-off and a bias circuit is proposed to improve the resonant frequency shift.

Furthermore, the proposed digital polar transmitter employs a buck converter with several-watt power and up to 200 MHz switching frequency. By applying a synchronous buck converter configuration and integrating driver and final stages into one die, the drain voltage waveform can be improved dramatically. However, for a specific output frequency, the buck converter suffers from the effect of ground bounce and Vdd sag due to an inductance of a bonding wire between chip and printed circuit board (PCB).

In this work, an on-chip RC “snubber” circuit [57], [58] is used to kill the resonance between the bonding wire and on-chip capacitor, where small snubber cells are distributed in the chip layout.

This chapter begins with theoretical designs of the CMCD PA and buck converter. Then, actual circuit designs of the CMCD PA with stack FETs and the buck converter with RC snubber will be discussed. After chip set and PCB fabrication is explained, the proposed digital polar transmitter will demonstrate at the carrier frequency of 0.75 GHz. It is noted that the design of an on-board balun used in the measurement will be described in Chapter 4.

3.2 Theoretical Design and Analysis

3.2.1 Load Impedance and Output Resonator of CMCD PA

The circuit configuration and the ideal current/voltage waveforms of the CMCD amplifier are shown in Figure 3.1. By driving switches Q1 and Q2, alternatively with switching frequency \( f_c \), the current through each switch is a square wave, while the
voltage across each switch is a half sine wave. DC current $I_{dd}$ is supplied from two current sources to maintain the circuit symmetry for simple calculation. A parallel resonator consisting of capacitor $C_{res}$ and inductor $L_{res}$ is used for harmonic termination, and only the fundamental component of the differential voltage reaches the load $R_L$.

![Circuit diagram](image)

Figure 3.1: (a) Circuit configuration and (b) current/voltage waveforms for each switching device of the CMCD amplifier.

The current through switch Q1 is written as

$$ I_1 = \frac{I_{dd}}{2} + \sum_{k=1}^{\infty} \frac{2I_{dd}}{\pi(2k-1)} \cdot \sin\{2\pi(2k-1)f_c t\} $$

(3-1)

The current through the load impedance is calculated as

$$ I_L = I_{dd} - I_1 = -\sum_{k=1}^{\infty} \frac{2I_{dd}}{\pi(2k-1)} \cdot \sin\{2\pi(2k-1)f_c t\} $$

(3-2)
The load impedance from switches Q1 and Q2 at the frequency \( f \), including the parasitic resistance of the resonator, can be expressed as

\[
Z_L(f) = \frac{1}{\frac{Q_u}{Q_a} \frac{1}{R_L} + j(2\pi f C_{res} - 1/2\pi f L_{res})} = \frac{(1 - Q_L/Q_u)R_L}{1 + j(f/f_{res} - f_{res}/f) \cdot Q_L}
\]

(3-3)

where \( Q_u \) and \( Q_L \) are the unloaded and loaded Qs, and \( f_{res} \) is the resonance frequency of the output resonator. From Eqs. (3-2) and (3-3), the voltage shown at the load impedance is calculated as

\[
V_L = Z_L(f) \odot I_L = -\frac{2R'_L I_{dd}}{\pi} \sum_{k=1}^{\infty} \frac{\sin\{2\pi(2k-1)f_c t\} - n(k) \cdot Q_L \cdot \cos\{2\pi(2k-1)f_c t\}}{(2k-1) \cdot \left[1 + \{n(k) \cdot Q_L\}^2\right]}
\]

(3-4)

where \( \odot \) is Volterra operator, \( R'_L = (1 - Q_L/Q_u)R_L \), and \( n(k) = (2k-1)f_c / f_{res} - f_{res} / \{(2k-1)f_c\} \) \( (k = 1,2, \ldots) \), is a factor describing the harmonic response of the resonator and \( k \) designates the odd harmonic index [50]. From Eqs. (3-2) and (3-4), the load current and voltage at the fundamental frequency are written as

\[
I_L(f_c) = -\frac{2I_{dd}}{\pi} \sin(2\pi f_c t)
\]

(3-5)

\[
V_L(f_c) = -\frac{2R'_L I_{dd}}{\pi} \cdot \frac{\sin(2\pi f_c t) - n(1) \cdot Q_L \cdot \cos(2\pi f_c t)}{1 + \{n(1) \cdot Q_L\}^2}
\]

(3-6)

From Eqs. (3-5) and (3-6), the output power delivered to \( R_L \) is calculated as
\[
\begin{align*}
P_{\text{out}} &= \left(1 - \frac{Q_L}{Q_u}\right) \cdot f_c \int_0^1 I_L(f_c) \cdot V_L(f_c) \cdot dt \\
&= \frac{2R_L I^2_{dd}}{\pi^2} \cdot \left(1 - \frac{Q_L}{Q_u}\right)^2 \cdot \frac{1}{1 + \{n(1) \cdot Q_L^2\}^2} 
\end{align*}
\]

(3-7)

Next, from Figure 3.1 (b) and Eq. (3-4), the DC component of \(V_1\) is calculated as

\[
\begin{align*}
V_1(\text{DC}) &= f_c \cdot \int_{\nu_2 f_c}^{\nu_f} V_L \cdot dt \\
&= \frac{2R'_L I^2_{dd}}{\pi^2} \cdot \sum_{k=1}^{\infty} \frac{1}{(2k - 1)^2} \cdot \frac{1}{1 + \{n(k) \cdot Q_L^2\}^2} 
\end{align*}
\]

(3-8)

The DC power consumption is calculated as

\[
\begin{align*}
P_{\text{DC}} &= I_{dd} \cdot V_1(\text{DC}) \\
&= \frac{2R_L I^2_{dd}}{\pi^2} \cdot \left(1 - \frac{Q_L}{Q_u}\right) \cdot \sum_{k=1}^{\infty} \frac{1}{(2k - 1)^2} \cdot \frac{1}{1 + \{n(k) \cdot Q_L^2\}^2} 
\end{align*}
\]

(3-9)

From Eq. (3-7) and (3-9), the drain efficiency (\(\eta = \frac{P_{\text{out}}}{P_{\text{DC}}}\)) can be can be expressed as follow

\[
\eta = \frac{\left(1 - \frac{Q_L}{Q_u}\right)}{\sum_{k=1}^{\infty} \frac{1}{(2k - 1)^2} \cdot \frac{1}{1 + \{n(k) \cdot Q_L^2\}^2}} \cdot \frac{1}{1 + n(1)^2 Q_L^2} 
\]

(3-10)
A. Load Impedance

The output balun transforms the load impedance to 50 Ω as shown in Figure 3.2. When the turns-ratio of the balun is 1-to-N, the corresponding impedance transformation ratio becomes 1-to-$N^2$.

![Circuit schematic of the CMCD amplifier with output balun.](image)

Figure 3.2: Circuit schematic of the CMCD amplifier with output balun.

The load resistance can be calculated from

$$\frac{R_L}{N^2} = \frac{50}{N^2}$$

From Eqs. (3-7) and (3-11), the output power of an ideal CMCD amplifier, operating with $f_c$ equal to $f_{res}$ and infinite loaded Q, can be simply expressed as

$$P_L = \frac{100 I_{dd}^2}{\pi^2 N^2}$$

From (3-12), peak and DC voltages across the switches can be written as
\[ V_{\text{peak}} = \pi \cdot V_{\text{DC}} = \frac{\sqrt{25P_L}}{N} \]

(3-13)

Figure 3.3 shows the voltage vs. \( N^2 \), required for 35 dBm output power using Eq. (3-13). In general, there is a trade-off between peak voltage and balun performance in the choice of impedance ratio. With increasing \( N^2 \), the balun bandwidth and insertion loss tend to degrade.

Figure 3.3: Calculated peak and DC voltage of the switching FETs vs. balun impedance ratio required to achieve \( P_{\text{out}} = 35 \) dBm.

We find for the case of \( N^2 = 4 \), the peak voltage is 9 V, which is low enough to be supported by a stack of two FETs, consisting of one nominally 1.8 V NMOS together with one nominally 3.3 V NMOS. Here we use the fact that the peak AC drain-source voltage that can be supported by the FETs is more than twice the nominal DC power supply voltage [59] although the ruggedness needs to be confirmed by stress testing.
Maximum peak voltage in the load mismatch condition will be discussed in Section 3.2.3. The corresponding DC drain-source voltage is 2.8 V and no boost converter is needed to supply DC current from a battery.

**B. Output Resonator**

The output resonator is designed to optimize drain efficiency. Figure 3.4 shows the calculated output resonator capacitance dependence of the drain efficiency of a CMCD PA using Eq. (3-10), and values of $Q_u = 5, 10$ and $20$.

![Figure 3.4: Drain efficiency vs resonator capacitance according to analytical model of CMCD amplifier ($R_L = 12.5 \, \Omega$, $Q_u = 5, 10$ and $20$).](image)

For small values of the resonator capacitance, harmonic leakage dominates the efficiency, while for large values, the resonator loss is the dominant factor. The frequency of operation for this work is chosen to be $f_{res} = f_c = 0.75$ GHz which is located between 3GPP standard bands XII and XIII. To anticipate future multi-band operation, a switched capacitor array, which is frequently used in voltage controlled oscillators
(VCOs) [60]-[63], was also used in the resonator resulting in a simulated \( Q_u \) at 0.75 GHz of approximately 20. From the results, it is seen that \( C_{res} = 13.5 \) pF is optimum to achieve the highest efficiency (although actual \( Q_u \) and \( C_{res} \) of the demonstrated PA is approximately 6 and 26 pF respectively, which slightly degrades the drain efficiency).

## 3.2.2 Buck Converter Design Considerations

The circuit configuration and the voltage waveform example of the buck converter are shown in Figure 3.5. Switches, Q3 and Q4, are driven alternatively with switching period \((1/f_{sw})\), using a digital pulse width modulated (DPWM) voltage \((V_{PW})\), generated based on an ideal envelope signal \((v_{env}(t))\). The supply voltage is \(V_{dd}\). An output inductor \((L_{env})\) is used to suppress clock images, and only baseband components is delivered to the load \((R_{PA})\), which is the DC current input of the CMCD amplifier. The output impedance of the buck converter at the RF carrier frequency is designed to be high enough to work as a current source.

![Figure 3.5](image-url)

**Figure 3.5:** (a) Circuit configuration of buck converter and (b) voltage waveforms of digital pulse width modulation signal.
When the digitized voltage of $v_{env}(t)$ is $V_{env}(t_n)$, the pulse width at the time $t_n$ can be written as

$$PW_n = \frac{V_{env}(t_n)}{V_{dd}} \cdot \frac{1}{f_{sw}} = \frac{D_n}{f_{sw}}$$

(3-14)

$V_{PW}$ is expressed as

$$V_{PW}(t) = 0 \left( t_n - \frac{1}{2f_{sw}} \leq t < t_n - \frac{PW_n}{2}, t_n + \frac{PW_n}{2} \leq t < t_n + \frac{1}{2f_{sw}} \right)$$

$$= V_{dd} \left( t_n - \frac{PW_n}{2} \leq t < t_n + \frac{PW_n}{2} \right)$$

(3-15)

From Fourier series expansion, $V_{PW}$ can be calculated from

$$V_{PW}(t) = D_n \cdot V_{dd} + \sum_{m=1}^{\infty} \frac{2V_{dd}}{m\pi} \cdot \sin(m\pi \cdot D_n) \cdot \cos(2\pi mf_{sw} t)$$

(3-16)

The output current $I_{out}$ is written as

$$I_{out}(t) = \frac{1}{R_{PA} + j2\pi f_{sw} L_{env}} \circ V_{PW}(t)$$

(3-17)

If $D_n$ is constant, the DC component of the output current is calculated as

$$I_{out}(DC) = D_n \cdot V_{dd}/R_{PA}$$

(3-18)
From Eq. (3-14), the input current is expressed as

\[
I_{in}(t) = 0 \quad \left( t_n - \frac{1}{2f_{sw}}, t_n \right)
\]

\[
= I_{out}(t) \quad \left( t_n - \frac{PW_n}{2}, t_n + \frac{PW_n}{2} \right)
\]

(3-19)

The DC component of the input current is calculated from

\[
I_{in}(DC) = \frac{D^2 \cdot V_{dd}}{R_{PA}} + \sum_{m=1}^{\infty} \frac{4V_{dd}}{m^2 \pi^2} \cdot \frac{R_{PA} \sin^2\left(m\pi D_n\right)}{R_{PA}^2 + (2\pi m f_{sw} L_{env})^2}
\]

(3-20)

From Eqs. (3-18) and (3-20), the efficiency of the buck converter is obtained from

\[
\eta_{BC} = \frac{R_{PA} \cdot I_{out}^2(DC)}{V_{dd} \cdot I_{in}(DC)} = \frac{1}{1 + \sum_{m=1}^{\infty} \left( \frac{\sin(m\pi D_n)}{m\pi D_n} \right)^2 \cdot \frac{4R_{PA}^2}{R_{PA}^2 + (2\pi m f_{sw} L_{env})^2}}
\]

(3-21)

**A. Envelope Inductor**

If \( D_n \) includes an AC component \( A_{env} \cos(2\pi f_{env} t_n) \), where \( f_{env} \ll f_{sw} \), from Eq. (3-17), the output current at \( f_{env} \) is expressed as

\[
I_{out}(f_{env}) \approx \frac{V_{dd} \cdot A_{env} \cos\left(2\pi f_{env} t_n\right)}{R_{PA} + j2\pi f_{env} L_{env}}
\]

(3-22)

The output power at \( f_{env} \) is calculated from
\[
P_{\text{out}}(f_{\text{env}}) \approx \frac{V_{\text{dd}}^2 A_{\text{env}}^2}{2R_{\text{PA}}} \cdot \frac{1}{1 + (2\pi f_{\text{env}} L_{\text{env}}/R_{\text{PA}})^2}
\]

(3-23)

3 dB bandwidth of the buck converter is expressed as

\[
BW = \frac{R_{\text{PA}}}{2\pi L_{\text{env}}}
\]

(3-24)

Figure 3.6 shows \(\eta_{\text{BC}}\) and \(BW\) vs \(L_{\text{env}}\) using Eqs. (3-21) and (3-24), where \(f_{\text{sw}} = 47\) MHz and \(R_L = 12.5\ \Omega\). From Eq. (3-8), when \(f_c = f_{\text{res}}, Q_u = \infty\) and \(Q_L\) is large enough, \(R_{\text{PA}}\) is approximately calculated as

\[
R_{\text{PA}} \approx 2R_L/\pi^2 + R_{\text{SW}}
\]

(3-25)

where \(R_{\text{SW}}\) is the parasitic series resistance of the PA FET switch. If the \(R_{\text{SW}}\) is small enough, \(R_{\text{PA}}\) is equal to 2.53 \(\Omega\). In Figure 3.6 (a), the duty cycles are 25%, 50% and 75%. From these results, the DC efficiency is improved with increasing output inductance, while the 3 dB bandwidth decreases. By selecting 100 nH, the DC efficiencies are higher than 97 % and the bandwidth is 4 MHz, which is approximately twice the baseband signal bandwidth of WCDMA signal. Generally speaking, three times or wider bandwidth of baseband bandwidth is needed as an envelope bandwidth, but the non-linearity can be compensated using DSP algorithm like pre-emphasis.
Figure 3.6: Calculated (a) DC efficiency and (b) 3 dB bandwidth vs output inductance according to analytical model of buck converter ($R_{PA} = 2.53 \, \Omega$, $f_{sw} = 47 \, MHz$, $D_n = 25\%$, 50\% and 75\%).

In order to generate 20 MHz LTE signal, four times higher switching frequency is needed. Figure 3.7 shows $\eta_{BC}$ and $BW$ vs $L_{env}$ when $f_{sw} = 188 \, MHz$. In this case, it is appropriate to use the output inductor of approximately 25 nH, where the DC efficiency is higher than 97\% and the bandwidth is 16 MHz.

Figure 3.7: Calculated (a) DC efficiency and (b) 3 dB bandwidth vs output inductance according to analytical model of buck converter ($R_{PA} = 2.53 \, \Omega$, $f_{sw} = 47 \, MHz$, $D_n = 25\%$, 50\% and 75\%).
3.2.3 Peak Voltage Variation Due to Load Mismatch of Digital Polar Transmitter

In actual handsets, the load impedance of the PA is affected by human body interaction [64]. In this section, the output peak voltage variation of the proposed digital polar transmitter due to the load impedance mismatch is analyzed.

Figure 3.8 shows the circuit schematic of the proposed digital polar transmitter for this analysis. For simplicity, it is assumed that \( f_c = f_{res} \) and \( Q_u = \infty \).

![Circuit schematic of the proposed digital polar transmitter for peak voltage analysis in load mismatch condition.](image)

The load impedance seen from Q1 and Q2 is approximated as

\[
Z_L = R_{LM} + jX_{LM} \quad (f = f_c) \\
= 0 \quad (f = 3f_c, 5f_c, \ldots)
\]

If the characteristic impedance is \( R_L \) and the reflection coefficient is \( |\Gamma| e^{j\theta} \), the load impedance at \( f_c \) can be calculated from
\[ R_{LM} + jX_{LM} = \frac{1 + |\Gamma|e^{j\vartheta}}{1 - |\Gamma|e^{j\vartheta}} R_L \]

(3-27)

The relationship between the amplitude of the reflection coefficient, \(|\Gamma|\), and voltage standing wave ratio, \(VSWR\), is expressed as

\[ |\Gamma| = \frac{VSWR - 1}{VSWR + 1} \]

(3-28)

From Eq. (3-4), the voltage shown at the load impedance is written as

\[ V_L = -\frac{2I_{dd}}{\pi} \{ R_{LM} \sin(2\pi f_c t) + X_{LM} \cos(2\pi f_c t) \} \]

(3-29)

From Eqs. (3-8), (3-18) and (3-29), the DC voltage supplied from the buck converter is calculated from

\[ V_1(DC) = \frac{2R_{LM}I_{dd}}{\pi^2} = D_n \cdot V_{dd} \]

(3-30)

From Eqs. (3-29) and (3-30), the peak voltage is obtained from

\[ V_{peak} = \pi \cdot D_n \cdot V_{dd} \cdot \sqrt{1 + \left( \frac{X_{LM}}{R_{LM}} \right)^2} \]

(3-31)
From the equation, if the load impedance at \( f_c \) have only real component, the peak voltage is determined only by changing the duty cycle of the buck converter. Also, from Eqs. (3-5) and (3-29), the output power is calculated from

\[
P_{\text{out}} = \frac{\left(\pi \cdot D_n \cdot V_{dd}\right)^2}{2R_{LM}}
\]

(3-32)

Figure 3.9 shows the reflection coefficient phase dependence of the peak voltage of the proposed digital polar transmitter, where \( VSWR = 3 \) and \( R_L = 12.5 \, \Omega \). The black curve is the peak voltage in the condition that \( D_n \cdot V_{dd} = 2.8 \, \text{V} \), which is the voltage to provide the output power of 3 W at \( VSWR = 1 \). The gray curve is the peak voltage when the output power is 3 W.

![Graph showing peak voltage vs phase of reflection coefficient](image)

Figure 3.9: Calculated peak voltage vs phase of reflection coefficient of proposed digital polar transmitter. \( (VSWR = 3, R_L = 12.5 \, \Omega) \)

From these results, the maximum peak voltage is approximately 15 V. If the transmitter is controlled in the condition that \( D_n \cdot V_{dd} \leq 2.8 \, \text{V} \) and \( P_{\text{out}} \leq 3 \, \text{W} \), the maximum peak voltage is less than 14 V. Furthermore, Breakdown due to load mismatch
can be avoided using a voltage peak control system [65] (not included in this work). In this work, the circuit design will carry out where the peak voltage of the PA is assumed to be 9 V.

3.3 Circuit Design

3.3.1 CMCD PA with Stacked FETs

A. Study on Efficiency Degradation in Back-off

Figure 3.10 (a) shows a circuit schematic of CMCD amplifier for 9 V peak voltage, where a two-stacked FET switching stage consisting of a 3.3 V NMOS and a 1.8 V NMOS in series is used. The stacked FET is designed using Jazz 0.18 µm CMOS technology, where the gate widths of both upper and lower FETs ($W_{gl}$ and $W_{gh}$) are 7.4 mm and 5.4 mm, respectively. In order to prevent breakdown, the second gate voltage ($V_{g2}$) needs to be designed carefully to control voltage distribution of two FETs at the peak voltage. As a preliminary study, ideal components are used for $L_{res}$ (=1.77 nH) and $C_{res}$ (= 20 pF), and the corresponding $f_{res}$ is 0.75 GHz. $R_L$ is 12.5 Ω.

Figure 3.10 (b) shows the drain efficiency ($\eta$) vs output power ($P_{out}$) of the CMCD PA with the fixed second gate bias condition. $f_c$ is 0.75 GHz and $I_{dd}$ is swept from 50 mA to 1.07 A. From the results, $\eta$ decreases by approximately 15 % at 20 dB back-off.
One of possible mechanisms of the efficiency degradation is the resonance frequency shift of the CMCD PA as shown in Figure 3.11. The supply voltage of the polar transmitter is reduced with decreasing output power. When $V_{d2}$ is higher than $V_{g2} - V_{th}$ in the left side, both 3.3 V and 1.8 V NMOSs turn off. The output capacitance is approximately $C_{d2}$, where $f_{res}$ is adjusted to $f_c$ like the broken gray curve in Figure 3.11 (a). However, when $V_{d2}$ is less than $V_{g2} - V_{th}$, the 3.3 V NMOS turns on as shown in Figure 3.11 (b). The output capacitance increases by the second gate-source capacitance, $C_{gs2}$. As a result, the resonance frequency shifts to lower like the black curve in Figure 3.11 (a) and the efficiency decreases.

Figure 3.12 shows the simulated drain efficiency vs output power when $C_{res}$ is tuned at each output power. As a reference, the drain efficiency without tuning $C_{res}$ is also shown. The drain efficiencies with tuned $C_{res}$ become flat as expected. From the
results, increasing $C_{res}$ is the major contribution of the efficiency degradation as assumed. Therefore, it is important to reduce the variation of the output capacitance.

Figure 3.11: Assumptions of back-off efficiency degradation mechanism of CMCD PA with stacked FET, which are (a) resonance frequency shift and (b) increasing output capacitance of stacked FET in back-off ($V_{d2} < V_{g2} - V_{th}$).

Figure 3.12: Simulated drain efficiencies vs output power of CMCD PA with tuned and fixed resonators. ($f_c = 0.75$ GHz, $L_{res} = 1.77$ nH, $C_{res} = 14.8$ pF, $R_L = 12.5$ Ω)
B. Investigation of Second Gate Bias Circuits

To reduce the output parasitic capacitance, three additional second gate bias circuits are investigated. Figure 3.13 (a) uses a “cross coupled” configuration between the second gate and output. Figure 3.13 (b) shows a circuit schematic of “pulse injection”, where the input pulses are injected into the second gate. Basic idea of “cross couple” and “pulse injection” configurations is to apply lower voltage to the second gate and prevent the upper-tied FET from turning on when the stacked FET is open. Figure 3.13 (c) is a circuit schematic of “common-mode floating”, where two second gates are connected to each other and isolated from AC ground using a large resistor to reduce the effect of $C_{gs2}$.

Figure 3.14 shows the simulated output capacitance vs DC supply voltage of the stacked FET with different second gate bias circuits. “Fixed bias” means the configuration shown in Figure 3.10 (a). From these results, the capacitance of “fixed bias” increases by approximately 18 pF. Using “cross-couple” configuration, the output capacitance decreases with the low DC supply voltage, but increases with the high DC supply voltage. The output capacitance of “pulse injection” is relatively lower, however, the configuration actually suffers from higher feed-through (not shown). Finally, we decided to use “common-mode floating” configuration, whose output capacitance is lowest. Although the output capacitance still changes, we can compensate the remained PA non-linearity arising from the variation using digital pre-distortion if needed.
Figure 3.13: Circuit schematic of three possible second gate bias circuits, i.e. (a) cross-coupled, (b) pulse injection and (c) common-mode floating, to reduce output parasitic capacitance of stacked FETs.
Figure 3.14: Simulated output capacitance vs supplied DC voltage of stacked FET with different second gate bias circuits. \( W_{gl} = 7.2 \text{ mm}, \ W_{gh} = 5.4 \text{ mm} \)

The mechanism of parasitic capacitance reduction at low output voltage \( (V_{d2} < V_{g2} - V_{th}) \) is analyzed when “common-mode floating” configuration is applied. By inserting a large resistance between the gate and AC ground as shown in Figure 3.15, the second gate is isolated from AC ground. Therefore, \( C_{gs2} \) becomes equivalently halved. In this configuration, the differential impedance of the second gate is grounded due to the virtual ground and the bias circuit does not affect the RF switching operation.

Figure 3.15: Mechanism of parasitic capacitance reduction at low output voltage \( (V_{d2} < V_{g2} - V_{th}) \) when “common-mode floating” configuration is applied.
Figure 3.16 shows the initially simulated voltage waveform of a two-stacked FET CMCD PA at 0.75 GHz. L-foundry 0.15 μm CMOS technology PDK is used for simulation. The first drain voltage, second drain voltage and second gate voltage are plotted. The supplied DC current is 1.1 A and the load impedance is 12.5 Ω. In this case, the peak voltage of the HVNMOS is less than 5.8 V and that of the LVNMOS is less than 3.3 V, in keeping with the design considerations of Section 3.2.1.

![Simulated voltage waveforms of differential two-stacked FET](image)

**Figure 3.16:** Simulated voltage waveforms of differential two-stacked FET ($f_c = f_{res} = 0.75$ GHz, $I_{dd} = 1.1$ A, $R_L = 12.5$ Ω). Here $V_{d1}$ is at the drain of the bottom FET, $V_{d2}$ is at the drain of the top FET, while $V_{g2}$ is at its gate.

### C. Advanced Self-Biasing Technique

Even if the “common-mode floating” second gate bias circuit is used, the output capacitance of the CMCD PA with still changes and the efficiency is degraded in back-off. It is possible to apply an advanced self-biasing technique [66] to the proposed digital polar transmitter, where the second gate bias voltage is adaptively controlled by analog circuit to maximize the efficiency. In this section, the effect of the technique is studied using preliminary simulation.
Figure 3.17 shows the (a) drain efficiency and (b) driver and final stage efficiency vs output power when a different second gate bias voltage is supplied, where the driver and final stage efficiency includes not only final stage but also driver stage DC power consumption.

Figure 3.17: (a) Drain efficiency and (b) driver and final-stage efficiency of CMCD PA with different second gate voltages. ($f_c = 0.75$ GHz, $L_{res} = 1.77$ nH, $C_{res} = 20$ pF)
The results indicate the drain efficiency can be improved by maximum 10 % at the output power of 25 dBm. However, the efficiency is improved only in the range from 20 dBm to 30 dBm and the amount of the improvement is limited. If the driver stage DC power dissipation is taken into account, the improvement becomes smaller. In the demonstration, this advanced self-biasing circuit is not implemented because the design of the bias circuit is complicated and the bandwidth of the envelope signal might be limited due to the RC constant of the bias circuit (although it is an interesting topic for future research).

### 3.3.2 High Switching Frequency Buck Converter

#### A. Final Stage Inverter Design

In this section, it is briefly explained how series resistance \((R_{BC})\) and output capacitance \((C_d)\) of the final inverter affect the efficiencies of the buck converter at the peak and in back-off.

Figure 3.18 shows an equivalent circuit of a buck converter, where it is assumed that the high-side and low-side switches have same on-resistances. The supply voltage, duty cycle of DPWM and load resistance are \(V_{dd}\), \(D_n\) and \(R_{PA}\), respectively. The DC output current and regulator efficiency can be expressed as

\[
I_{\text{out}}' \approx \frac{D_n \cdot V_{dd}}{R_{BC} + R_{PA}}
\]

(3-33)

\[
\eta_{BC} \approx \frac{R_{PA} \cdot I_{\text{out}}'^2}{R_{PA} \cdot I_{\text{out}}'^2 + R_{BC} \cdot I_{\text{out}}'^2 + C_d \cdot V_{dd}^2 \cdot f_{sw}}
\]

(3-34)
where the leakage of harmonics in Eq. (3-21) is neglected. The second and third terms of the denominator are well-known conduction and output capacitance losses [67].

\[ V_{dd} \]
\[ Q3 \]
\[ Q4 \]
\[ R_{BC} \]
\[ L_{env} \]
\[ I'_{in} \]
\[ I'_{out} \]
\[ C_d \]
\[ R_{PA} \]

Figure 3.18: Equivalent circuit of buck converter including \( R_{BC} \) and \( C_d \).

Figure 3.19 shows the simulated efficiency vs output current of the buck converter with different gate widths, where \( V_{dd} = 3.3 \) V, \( f_{sw} = 200 \) MHz, \( L_{env} = 100 \) nH and \( R_L = 2.5 \) \( \Omega \). The high-side and low-side switches are 3.3 V PMOS and 3.3 V NMOS respectively and the ratio of gate widths is 1.8:1.

![Efficiency vs Output Current](image)

Figure 3.19: Simulated efficiency vs output current of buck converter with different gate width (\( V_{dd} = 3.3 \) V, \( f_{sw} = 200 \) MHz, \( L_{env} = 100 \) nH, \( R_L = 2.5 \) \( \Omega \))

When the gate width is narrow, the regulator efficiency is relatively flat over the output current, but the peak efficiency is low. Here, the regulator efficiency is dominated
by the conductive loss, which is proportional to the square of the output current. With increasing gate width, the peak efficiency is improved, but the back-off efficiency decreases due to increasing effect of the output capacitor loss, which is constant for the output current. Finally, it was decided to use the PMOS gate width of 18.2 mm for the demonstration.

**B. RC Snubber Circuit**

If only a large bypass capacitor is used and a specific switching frequency is provided, the output voltage waveform of the buck converter is corrupted as shown in Figure 3.20. This is caused by a resonance between the capacitor and bonding wire. The waveform degradation may cause the efficiency degradation.

Figure 3.20: Circuit schematic and output voltage waveform of buck converter with only bypass capacitor.

Figure 3.21 shows the circuit schematic and output voltage waveform of the buck converter with on-chip RC snubber, consisting of large capacitor and resistor in series. The RC snubber is placed between the Vdd and ground. In the RC snubber, the resistor
works to suppress the resonance. As a result, a pulse-shaped voltage waveform is obtained.

Figure 3.21: Circuit schematic of buck converter with RC snubber.

The resonance is analyzed using the output impedance of the final stage inverter. When the high-side switch is closed and the low-side switch is open, the output impedance at the frequency $f$ can be expressed as

$$Z_{out}(f) = j \frac{2\pi f \cdot L_w (2\pi f \cdot L_w - \frac{1}{2\pi f} \cdot C_{bp} - jR_{sb})}{4\pi f \cdot L_w - \frac{1}{2\pi f} \cdot C_{bp} - jR_{sb}}$$

(3-35)

where $L_w$ is the bond wire inductance, $C_{bp}$ is the bypass capacitance and $R_{sb}$ is the snubber resistance. If $R_{sb} = 0 \ \Omega$, $Z_{out}$ becomes infinity at the frequency $f_{res_{bc}} = (2L_w C_{bp})^{1/2}/2\pi$. When the switching frequency is close to $f_{res_{bc}}$, a ripple emerges in the output voltage.

Figure 3.22 shows the output impedance $|Z_{out}|$ over frequency calculated using Eq. (3-26), where $L_w$ is 0.25 nH, $C_{bp}$ is 1 nF, and corresponding $f_{res_{bc}} = 225$ MHz. Here, the quality factor of RC snubber is defined as $Q_c = \frac{1}{2\pi f_{res_{bc}}} C_{bp} R_{sb}$. By changing $R_{sb}$, $|Z_{out}|$
with different values of $Q_c$ is calculated. When $Q_c$ is very small, $|Z_{out}|$ increases continuously due to the inductance of the bonding wire, which results in large over-shoot and under-shoot of the output voltage. When $Q_c$ is very large, $|Z_{out}|$ has a peak at the $f_{res,bc}$, which causes the ripple of the output voltage. When $Q_c$ is approximately unity, $|Z_{out}|$ is relatively flat over frequency.

![Figure 3.22](image)

Figure 3.22: Calculated (a) output impedance and (b) its quality factor of buck converter with RC snubber circuit over frequency. ($L_w = 0.25$ nH, $C_{bp} = 1$)

Figure 3.23 shows the simulated peak voltage and regulator efficiency vs $Q_c$ of 3-stage buck converter, where $f_{sw} = 200$ MHz, $D = 50\%$ and $V_{dd} = 3.3$ V. Dead time ($t_d$) of 150 psec is applied to input pulses between high-side and low-side, which reduces the shoot-through current and improves the efficiency of a buck converter with driver stages. The black curve is peak voltage and the gray curves are final-stage and 3-stage efficiencies. From the results, the peak voltage can be minimized when $Q_c$ is adjusted to be from 1 to 2. In addition, the efficiency decreases with increasing $Q_c$. Therefore, it should be best balance in the case of $Q_c = 1$. 
Figure 3.23: Simulated peak voltage and efficiency vs $Q_c$ of buck converter. ($L_w = 0.25$ nH, $C_{bp} = 1$ nF, $f_{sw} = 200$ MHz, $V_{dd} = 3.3$ V, $D = 50\%$, $t_d = 150$ psec)

3.4 Chip and Evaluation Board Fabrication

3.4.1 Differential Stacked FET for On-wafer Measurement

One of drawbacks of a CMOS PA is breakdown voltage. Not only DC evaluation but also AC evaluation is needed when the voltage swing is near the breakdown voltage. It is difficult to measure the AC voltage waveform using a test chip mounted on PCB because parasitic components, such as bonding wire inductance and impedance mismatch of transmission lines on PCB, affect the waveform. To prevent the issue, on-wafer measurement is carried out.

Figure 3.24 and Figure 3.25 show circuit schematic and layout of differential stacked FET for on-wafer measurement, respectively. In order to set each output port to be $50\,\Omega$, i.e. differential load resistance of $100\,\Omega$, the size of FETs are $1/8$ times smaller than that of on-board test chip. It consists of 16 unit cells. The second gate voltage is
supplied through 20 kΩ resistor. 100 Ω poly resistor is inserted between two input ports for impedance matching.

Figure 3.24: Circuit schematic of differential stacked FET for on-wafer measurement.

Figure 3.25: Layout of differential stacked FET for on-wafer measurement.
3.4.2 1st Generation CMCD PA

The implemented PA consists of on-chip and on-board DC and RF blocks, as shown in Figure 3.26. The driver stages, stacked differential switching stages and an output capacitor stage are integrated into silicon. The total output capacitance increased to 26 pF due to the parasitic capacitances of the switching FETs, routing, and pads. The 1.65 nH air core inductor and Guanella reverse balun (GRB) are used as off-chip components. Detail of the GRB will be described in Chapter 4.

Figure 3.26: Circuit schematic of proposed CMCD PA.

Figure 3.27 shows the circuit schematic of the driver stage, consisting of a differential inverter. The RC snubber (de-Qed bypass capacitor) is also applied to reduce the over-shoot/under-shoot and ripple of the output voltage waveform as discussed in Section 3.3.2. $Q_c$ of the RC snubber are 1–2 in the range from 0.8 GHz to 2.0 GHz.
To anticipate future wide power dynamic range operation, final and driver stages are segmented into small unit cells for layout. Figure 3.28 (a) shows the layout of the unit-cell amplifier. The RC snubber is also included in each unit-cell to reduce the effect of the parasitic inductance of the routing. Figure 3.28 (b) shows a chip photo of CMCD PA; the die size was $1.7 \times 1.5 \text{ mm}^2$. The chip is fabricated using L-foundry 0.15 µm CMOS technology. Multiple wires are supposed to be used for RF output and ground to reduce parasitic inductance.
Figure 3.28: (a) Layout of unit cell amplifier and (b) chip photo of CMCD PA. (1.7 × 1.5 mm²)
3.4.3 1st Generation Buck Converter

Figure 3.29 shows the circuit schematic of the high switching frequency buck converter. Two inverter stages are included to drive the buck converter output FETs. The DC voltage is 3.3 V and the off-chip air-core inductor of 100 nH is used for WCDMA signal. High speed pulse pattern generator can provide only 2 V<sub>pp</sub> square wave to 50 Ω load while 3.3 V<sub>pp</sub> square wave is supposed to be applied into the input of the designed buck converter. Off-chip input termination resistor of 82 Ω is used to obtain a voltage swing as large as possible, which is ideally 2.5 V<sub>pp</sub>.

![Circuit schematic of high switching frequency buck converter.](image)

Figure 3.29: Circuit schematic of high switching frequency buck converter.

Similar to CMCD PA, the buck converter is also segmented into small unit cells. Figure 3.30 (a) shows the layout of the unit cell amplifier of buck converter. The RC snubber is accommodated in each unit cell. The chip pictured in Figure 3.30 (b) is implemented in the same 0.15 μm CMOS technology as the CMCD PA. The die size was 1.1 × 1.5 mm<sup>2</sup>.
Figure 3.30: (a) Layout of unit cell amplifier and (b) chip photo of buck converter. (1.1 × 1.5 mm²)
3.4.4 1st Generation PCB

Figure 3.31 shows photos of the 1st generation PCB for 1st and 1.5th generation digital polar transmitters. The dielectric constant is 3.48 (FR4) and the thickness is 0.508 mm. Parameters of the PCB are summarized in Table 3.1. The digital pulse width modulation (DPWM) envelope signal is applied to “AMin” and the differential PM signal is provided to “PMin+” and “PMin-”. The envelope modulated delivered from the buck converter is supplied to the CMCD PA through the red DC cable. The RF modulated signal is delivered from “MODout” after conversion to single-end in the Guanella reverse balun (GRB). Design of GRB will be discussed in Chapter 4.

Figure 3.31: Photo of PCB for 1st and 1.5th generation digital polar transmitters.

Table 3.1: Parameters of PCB.

<table>
<thead>
<tr>
<th># of layer</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant</td>
<td>3.48</td>
</tr>
<tr>
<td>Board thickness</td>
<td>20 mill (0.508 mm)</td>
</tr>
<tr>
<td>Metal</td>
<td>Copper immersed gold</td>
</tr>
<tr>
<td>Metal thickness</td>
<td>2 oz/ft² (70 um)</td>
</tr>
<tr>
<td>Board size</td>
<td>70 mm x 80 mm</td>
</tr>
<tr>
<td>Drill Diameter</td>
<td>0.3 mm / 2.5 mm</td>
</tr>
</tbody>
</table>
Figure 3.32 shows the photo of the Aluminum base for 1st and 1.5th generation digital polar transmitters. The Aluminum base has a hole below the GRB not to touch the bottom side of the balun with the base. Another hole is made below the envelope inductor to reduce the output capacitor of the buck converter.

The calculated thermal resistances of the CMCD PA chip and Aluminum base are approximately 1 °C/W and 2 °C/W, respectively [23], [68]. Even if the output power is 2W and the drain efficiency is 33 %, the generated heat is 4 W and the junction temperature increases by only 12 °C. It should be small enough since typical junction temperatures of commercial Silicon ICs are in the range from 140 °C to 175 °C.

![Figure 3.32: Photo of Aluminum base for 1st and 1.5th generation digital polar transmitters.](image-url)
3.5 Experimental Results

3.5.1 Differential Stacked FET (On-wafer)

Figure 3.33 shows the on-wafer measurement setup for the differential stacked FET. An RF differential pulse signal with 50% duty cycle is applied from a pulse pattern generator. The voltage waveform at one output port is measured by 6 GHz digital oscilloscope through bias-T and the other port is terminated by 50 Ω. The voltage from power supply changes from 0 V to 9V.

![Diagram of measurement setup](image)

Figure 3.33: On-wafer measurement setup for differential stacked FET.

Figure 3.34 shows the measured and simulated DC I-V curves of the differential stacked FET. The symbols are measured results and the curves are simulated results. The stacked FET tolerates up to 9 V when it turns off. By increasing $V_{g1}$ to 1.8 V, it maintains the triode region when the DC current is 64 mA and more. If the device size is 8 times, the DC current capability becomes more than 0.5 A. Some amount of error between measurement and simulation appears when they are in the saturation region, but this should have small impact to performance of a switching-mode PA.
Figure 3.34: Measured and simulated DC I-V curves of differential stacked FET, where $V_{g2} = 3.0$ V. (Symbols: measurement and curves: simulation)

Figure 3.35 shows the measured and simulated output voltage waveform of the differential stacked FET, where the carrier frequency is (a) 0.5 GHz and (b) 1.0 GHz. In Figure 3.35 (a), the output voltage waveform is like pulse wave which is expected. In addition, it is confirmed that the designed stacked FET tolerates the voltage swing of approximately 8 V<sub>pp</sub>, which is the maximum value of oscilloscope although it is 1 V lower than the required peak voltage. In Figure 3.35 (b), the waveform looks a half-sine wave at 1.0 GHz. The parasitic components in the chip seem to affect the load impedance of the stacked FET at the harmonic frequency.
Figure 3.35: On-wafer voltage waveform measured results of differential stacked FET, where $f_c =$ (a) 0.5 GHz and (b) 1.0 GHz, and $V_{g_2} = 2.8$ V.

3.5.2 1st Generation CMCD PA

Figure 3.36 shows the measured and initially simulated output power of the 1st generation CMCD PA over frequency. From the results, the output power of 30.8 dBm is achieved at 0.75 GHz. Also, the measured output power is in good agreement with the simulated result. The DC current for the measurements is supplied from an external source, with values 0.5 A and 0.8 A. In the initial simulation, a DC current of 1.2 A was applied to reach a 9 V peak voltage. However, bond wire inductance changed the load impedance to be higher than 12.5 $\Omega$, and the peak voltage reached 9 V at approximately 0.8 A DC current. In addition, unexpected oscillations occurred when higher DC current
was supplied. Therefore, measured results were not obtained at 1.2 A DC current. One possible reason for the oscillation is feedback of even harmonics to the driver amplifier input due to on-chip ground bounce. If the PM signal generator is integrated into the same die, this effect can be mitigated.

![Graph](image_url)

Figure 3.36: Measured and initially simulated output power of 1st generation CMCD PA over frequency (single-tone output), where $V_{g2} = 2.8$ V.

Figure 3.37 shows the measured and initially simulated driver and final-stage efficiency (including losses in the driver and final stages) of the single band CMCD PA over frequency. Peak driver and final-stage efficiency at 0.75 GHz frequency achieved 49 % (51 % drain efficiency) at 31 dBm output power. The measured efficiency is lower than the value from theoretical analysis shown in Figure 3.4. A portion of this difference can be accounted for by series resistances (0.65 $\Omega$ including on-resistance of the stacked FETs and routing resistances) and by the output balun loss (0.67 dB), leading to loss factors [50] of approximately 80 % and 85 %, respectively. The power consumption of the driver stage (approximately 120mW at 0.75 GHz) also contributes to reducing the
efficiency. There is a discrepancy between the measured and initially simulated efficiency because no RF MIM capacitor model nor layout parasitic extraction (LPE) were applied. Comparison between measured results and more accurate simulation will be discussed in Chapter 4.

![Figure 3.37: Measured and initially simulated efficiency (including driver and PA) over frequency of 1st generation CMCD PA, where $V_{g2} = 2.8$ V.](image)

Figure 3.37 shows the measured and calculated output power vs DC current; and Figure 3.39 shows the driver and final stage efficiency vs output power. The theoretical output powers are calculated from Eq. (3-7) and GRB loss, and the driver and final-stage efficiencies are from Eq. (4-3), driver stage power consumption and GRB loss, where $Q_u = 6$, $Q_L = 1.3$, $R_L = 12.5 \ \Omega$. From the results, it can be seen that it is possible to theoretically predict the characteristics of the CMCD PA except feed-through and shifting the resonance frequency due to the stacked FET.
Figure 3.38: Measured and calculated output power vs DC current of 1st generation CMCD PA, where $V_{g2} = 2.8$ V, $f_c = 0.75$ GHz, $Q_u = 6$, $Q_L = 1.3$, $R_L = 12.5$ Ω and $Loss_{GRB} = 0.68$ dB.

Figure 3.39: Measured and calculated driver and final stage efficiency vs DC current of 1st generation CMCD PA, where $V_{g2} = 2.8$ V, $f_c = 0.75$ GHz, $Q_u = 6$, $Q_L = 1.3$, $R_L = 12.5$ Ω, $Loss_{GRB} = 0.68$ dB, $R_{SW} = 0.65$ Ω and $P_{drv} = 0.12$ W.
3.5.3 1st Generation Buck Converter

Figure 3.40 and Figure 3.41 shows the measured and initially simulated DC output current and efficiency vs duty cycle of the buck converter, respectively. The symbol corresponds to the measured results and the curve corresponds to the simulated results. The supply current is 3.3 V and the switching frequency changes from 47 MHz to 200 MHz. When the switching frequency is 47 MHz, the measured peak DC current of 1.05 A and the efficiency of 85 % are achieved. The measured DC current and efficiency are lower than the simulation because simulation does not take additional parasitic resistance and capacitance of on-chip metal layer, bonding wire, air-core inductor and so on.

Figure 3.40: Measured and initially simulated DC output current vs duty cycle of 1st generation buck converter, where \( V_{dd} = 3.3 \) V and \( f_{sw} = 47 \) MHz, 125 MHz and 200 MHz.
Figure 3.41: Measured and initially simulated regulator efficiency vs duty cycle of 1st generation buck converter, where $V_{dd} = 3.3$ V and $f_{sw} = 47$ MHz, 125 MHz and 200 MHz.

### 3.5.4 1st Generation Digital Polar Transmitter (Single-tone)

Single-tone outputs of the 1st generation digital polar transmitter are produced using inputs with fixed DPWM duty ratio and no phase modulation. Measured and calculated output powers vs duty ratio are shown in Figure 3.42. The carrier frequency is 0.75 GHz and the switching frequency of DPWM is 47 MHz. Peak output power is 30 dBm. The measured output power is proportional to the square of the duty ratio in range 5-30 dBm (although it decreases somewhat from this relationship at lower powers due to PA nonlinearity). Theoretical curve of the output power is calculated from Eqs. (3-7), (3-25) and (3-33), where $R_{BC} = 0.3 \, \Omega$. The calculated output power is approximately 1.8 dB higher than the measured output power. One of the possible reasons is that the resistance of the CMCD PA seen from the buck converter is slightly different from the theoretical value.
Figure 3.42: Measured and calculated output power vs duty cycle of 1st generation digital polar amplifier with CW output (single-tone), where $V_{g2} = 2.8$ V, $f_c = 0.75$ GHz, $f_{sw} = 47$ MHz, $V_{dd} = 3.3$ V, $Q_u = 6$, $Q_L = 1.3$, $R_L = 12.5$ Ω, $Loss_{GRB} = 0.68$ dB, $R_{SW} = 0.65$ Ω and $R_{BC} = 0.3$ Ω.

Figure 3.43 (a) shows overall efficiency vs output power. Peak overall efficiency is 40.6 %. DC power dissipation of the buck converter and the driver stage are included in the overall stated efficiency. The peak PAE drops to 36.4 % due to the 20 dBm driver stage input as mentioned above, although in a realistic application scenario, the input power would be considerably lower.

Figure 3.43 (b) shows a comparison between measured efficiency and theoretical curves of class-A and B amplifier. From the results, the efficiency of the digital polar transmitter is higher than that of an ideal class-A amplifier in all output power ranges and higher than that of an ideal class-B amplifier up to 20 dB power back-off.
Figure 3.43: (a) Measured overall efficiency vs output power of 1st generation digital polar amplifier (linear scale); (b) comparison between measured efficiency and theoretical curve of class-A and B amplifier (log scale), where $V_{g2} = 2.8$ V, $f_c = 0.75$ GHz, $V_{dd} = 3.3$ V and $f_{sw} = 47$ MHz.
3.6 Summary

A digital polar transmitter with a watt-class CMOS power amplifier is demonstrated, implemented with a 0.15µm RF CMOS process. Current-mode class-D configuration and stacked FETs are used to obtain high efficiency and high breakdown voltage in the output stage, which is measured to have 31 dBm output power with 51% drain efficiency under single tone testing. A three-stage buck converter with RC snubber was applied as envelope modulator, whose measured efficiency was 85% when 1.05 A DC current is delivered with a 47 MHz driving frequency and 95% duty cycle. The measured output power and efficiency of the digital polar transmitter, consisting of CMCD PA and buck converter, achieved 30 dBm and 40.6%.

3.7 Acknowledgements

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Chapter 4

Multiband Digital Switching Power Amplifier

4.1 Introduction

To cover wide frequency range (0.7-2.0 GHz), there are two options, i.e. broadband and tunable matching networks. The bandwidth of the CMCD amplifier is limited by the on-resistance \((R_{on})\) and shunt capacitance \((C_p)\) of the switches. Therefore, it is appropriate to apply a tunable matching network when a transistor with relatively high \(R_{on}\) and \(C_p\), such as CMOS, is used.

In order to realize a CMCD amplifier with a tunable matching network, a band-switching resonator used for VCOs [60]-[63] is one of possible candidates. These resonators usually consist of two capacitors and a switch between the capacitors to supply bias voltages flexibly. However, these resonators were not designed to tolerate a large voltage swing higher than the breakdown voltage of a FET.

In this work, a band-switching resonator is proposed for 9 V peak voltage swing using stacked FET switch and well-concerned bias circuit.
An on-board balun is used for 1st and 1.5th generation digital polar transmitters. 1-to-4 differential-to-single-end impedance transformation and ideally open common-mode impedance are required to the balun. In addition, the balun needs to cover the low and high bands of cellphone application. Several types of baluns have been reported. In [70], a balun consisting of a pair of wire wound around a ferrite core was used and the operation frequency of the balun is low (30 MHz). With increasing the operation frequency of this type of balun, the allowable peak power tends to decrease. In [71], a second-order Lattice balun made by chip inductors and capacitors was applied. The bandwidth of the balun is a little narrower than requirement (ideally 0.5-1.8 GHz) and the impedance transformation ratio is 1-to-1. In [72] and [73], coaxial cable balun and Marchand reverse balun are used and the ideal bandwidths are infinite. However, the impedance transformation ratios are 1-to-1 and 1-to-2, respectively.

In this work, we propose Guanella reverse balun (GRB), which has infinite ideal bandwidth and 1-to-4 impedance transformation ratio. The ideal input common-mode impedance is open. Using a doughnut shape layout with low parasitic components, the significantly wide bandwidth is achieved.

On the other hand, on-chip balun is also an important research objective. Power mixer and CMCD PA with on-chip 1-to-4 baluns [74], [75] have been reported, where symmetry transformer balun and step-up transformer balun [76] are used. However, both cover only a fixed frequency range.

In this work, by adjusting the resonance frequency of the balun together with the band-switching capacitor, an integrated multiband PA is realized.
This chapter begins with analysis of effects of $R_{on}$ and $C_p$ to the bandwidth and system design of multiband CMCD PA. Next, design and modeling of the circuit blocks are explained, where we focus on tunable resonators using on-board and on-chip baluns. Finally, measured output powers and efficiencies are discussed and accurate simulation is discussed.

4.2 Theoretical Design and Analysis

4.2.1 Variable Resonator for Multiband CMCD PA

Figure 4.1 shows the circuit configuration of the multiband CMCD amplifier. A variable parallel resonator consisting of variable capacitors ($C_{res}$) and inductor ($L_{res}$) is used to adjust the resonance frequency and for harmonic termination, and only the fundamental component of the differential voltage reaches at the load. Our CMCD PA uses 1-to-4 balun as an appropriate tradeoff between the peak voltage and output loss.

Figure 4.1: Circuit configuration of the multiband CMCD amplifier.
The WCDMA frequency bands are roughly categorized into two groups: low band (0.698-0.915 GHz) and high band (1.71-1.98 GHz) excluding Band VII and XI. Here we focus on 0.85 GHz and 1.75 GHz as the resonance frequencies of the variable resonator. When switch Q1 is open and switch Q2 is closed, the resonator is the parallel circuit of $C_{res}$, $L_{res}$ and the fixed parasitic capacitance between the output and ground ($C_p$). The resonance frequency is written as

$$f_{res} = \frac{1}{2\pi \sqrt{L_{res}(C_{res} + C_p)}}$$

(4-1)

Figure 4.2 shows the required $C_{res}$ for 0.85 and 1.75 GHz vs $L_{res}$ of the variable resonator and the drain efficiencies of the CMCD PA vs $L_{res}$ calculated using Eqs. (4-1) and (3-10). In Figure 4.2 (a), $C_p$ is assumed to be 5 pF. With increasing $L_{res}$ of the resonator, the area of $C_{res}$ can be reduced, but the required capacitance ratio between low and high band conditions increases. When $L_{res}$ is 0.5 nH, the required capacitance ratio is 5.6, which is lower than that of the fabricated BSC of approximately 6 as shown in Figure 4.35. In Figure 4.2 (b), unloaded quality factors of 8.5 and 7.5 at 0.85 and 1.75 GHz are used, where a bonding wire inductor supposed to be applied. With decreasing $L_{res}$, the drain efficiencies decrease. When $L_{res}$ is 0.5 nH, the calculated drain efficiencies are 76 \% and 64 \%, which are lower than the optimal value (around 82 \%) but still high.
Figure 4.2: (a) Required capacitances and (b) drain efficiencies of CMCD PA vs inductance of band-switching resonator ($f_{\text{res}} = f_c = 0.85 \text{ GHz} / 1.75\text{GHz}$, $Q_u = 8.5 / 7.5$).

Figure 4.3 (a) shows the simplified overall circuit configuration of the multiband CMCD amplifier. Band-switching capacitors (BSCs) are used to change the resonance frequency of the output resonator since it is difficult to cover the entire band using the fixed value LC resonator. In our design, the BSCs consist of 64 cells (21-74 pF). In order to provide the bias voltage independent of the instantaneous power supply voltage, the switch is inserted between two capacitors. When the switch is closed, the capacitors
dominate the resonance frequency. When the switch is open, the frequency is decided by the off-capacitance of the switch. The 0.5 nH inductor is provided to adjust the resonance frequency, together with the BSCs. Figure 4.3 (b) shows the simulated output power vs frequency under ideal conditions when the number of BSCs turned on is 64 (C64), 32 (C32), 16 (C16), 8 (C8) and 0 (C0). The supplied DC current is 1.12 A, as required for 35 dBm peak output power.

Figure 4.3: (a) Circuit configuration and (b) frequency response of multi-band CMCD amplifier.
4.2.2 Bandwidth Degradation of CMCD PA

The variable resonator needs to tune the resonance frequency rather precisely because the parasitic components of the PA degrade its bandwidth. In this section, the effects of the series resistance and output capacitance of the stacked FETs are theoretically estimated.

Figure 4.4 shows the voltage waveform at the resonance frequency of the CMCD amplifier along with the voltage drop from the series resistance \( R_{SW} \) of the stacked FET. The constant DC current \( (I_{dd}) \) flows through \( R_{SW} \) of Q1 and Q2 alternatively. Therefore, the voltage waveform is shifted up by \( I_{dd} R_{SW} \) from the ideal waveform. The series resistance degrades the drain efficiency although it does not change the output power.

From Eq. (3-9), the DC power consumption is expressed as

\[
P_{DC} = \frac{2R'_{L}I_{dd}^{2}}{\pi^{2}} \cdot \sum_{k=1}^{\infty} \frac{1}{(2k-1)^{2}} \cdot \frac{1}{1+n(k)^{2}Q_{k}^{2}} + R_{SW}I_{dd}^{2}
\]

(4-2)

From Eqs. (3-7) and (4-2), the drain efficiency may be calculated from

\[
\eta = \frac{\left(1 - \frac{Q_{L}}{Q_{n}}\right) \cdot \frac{1}{1+n(1)^{2}Q_{L}^{2}}}{\sum_{k=1}^{\infty} \frac{1}{(2k-1)^{2}} \cdot \frac{1}{1+n(k)^{2}Q_{k}^{2}} + \frac{\pi^{2}R_{SW}}{2 \cdot R_{L} \cdot \left(1-Q_{L}/Q_{n}\right)}}
\]

(4-3)
Figure 4.4: Voltage waveform of CMCD amplifier with on-resistance of stacked FET ($R_{on}$) at resonance frequency.

Figure 4.5 shows the voltage waveform of the CMCD amplifier, for a case where the switching frequency is higher than the resonance frequency. In case that $C_p$ is zero, $V_2(\pi) = -V_1(\pi)$. However, in case $C_p > 0$ and $f_c > f_{res}$, $C_p$ at the $V_1$ side stores a positive charge when the phase is just below $\pi$. The capacitor is discharged to ground and $V_2$ starts from $-V_1(\pi) + \Delta V$ when the phase is just above $\pi$, where $\Delta V$ can be calculated from

$$
\Delta V = \frac{C_p}{2C_{res} + C_p} \cdot V_1(\pi) \quad (f_c \geq f_{res})
$$

$$
= 0 \quad (f_c < f_{res})
$$

$$
(4-4)
$$

These phenomena can be expressed as adding a square wave with $\Delta V$ height to $V_1$ and $V_2$ respectively. The load voltage and current at the fundamental frequency are written as
\[ V_L(f_c) = -\frac{2R'_L I_{dd}}{\pi} \cdot \frac{\sin(2\pi f_c t) - n(1) \cdot Q_L \cdot \cos(2\pi f_c t)}{1 + n(1)^2 Q_L^2} - \frac{4\Delta V}{\pi} \sin(2\pi f_c t) \]

(4-5)

\[ I_I(f_c) = -\frac{2I_{dd}}{\pi} \sin(2\pi f_c t) - \frac{4\Delta V}{\pi R'_L} \cdot \left\{ \sin(2\pi f_c t) + n(1) \cdot Q_L \cdot \cos(2\pi f_c t) \right\} \]

(4-6)

From Eqs. (4-5) and (4-6), the output power is calculated from

\[ P_{out} = \frac{2 \cdot R'_L \cdot I_{dd}^2}{\pi^2} \left( 1 - \frac{Q_L}{Q_u} \right)^2 \left( \frac{1 + 2\alpha}{1 + n(1)^2 Q_L^2} + \alpha^2 \right) \]

(4-7)

where \( \alpha = 2 \Delta V / \{ I_{dd} R_L (1 - Q_L/Q_u) \} \) is the voltage ratio between the additional square wave and fundamental square wave of the CMCD amplifier, which is current times load resistance including the parasitic resistance of the resonator. From Eqs. (4-2), (4-5) and (4-6), the DC power consumption is expressed as

\[ P_{DC} = \frac{2R'_L I_{dd}^2}{\pi^2} \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2} \cdot \frac{1}{1 + n(k)^2 Q_L^2} + \frac{R_{SW} I_{dd}^2}{2} + \Delta V I_{dd} \]

(4-8)

From Eqs. (4-7) and (4-8), the drain efficiency is derived as

\[ \eta = \frac{\left( 1 - \frac{Q_L}{Q_u} \right) \left( \frac{1 + 2\alpha}{1 + n(1)^2 Q_L^2} + \alpha^2 \right)}{\sum_{k=1}^{\infty} \frac{1}{(2k-1)^2} \cdot \frac{1}{1 + n(k)^2 Q_L^2} + \frac{\pi^2}{2} \left( \frac{R_{on}}{R_L (1 - Q_L/Q_u)} + \alpha^2 \right)} \]

(4-9)
Figure 4.5: Voltage waveform of CMCD amplifier with parasitic capacitance ($C_p$) where $f_c > f_{res}$.

Figure 4.6 shows the effect of $R_{SW}$ and $C_p$ of the CMCD PA on (a) the output power and (b) the drain efficiency, as calculated using Eqs. (4-7) and (4-9) with $f_{res} = 0.85 / 1.75$ GHz and $Q_u = 8.5 / 7.5$, respectively; $L_{res} = 0.5$ nH, $I_{dd} = 1.12$ A (corresponding to the ideal output power of 35 dBm), $R_{on} = 0.5$ Ω (obtained from a designed circuit in the following section), and $C_p = 5$ pF. The figure shows that, while the maximum output power does not change appreciably, the parasitics cause narrower bandwidth, so that to maintain maximum power and efficiency, the resonant frequency must be set with high precision.
Figure 4.6: Effects of $R_{SW}$ and $C_p$ of CMCD amplifier: (a) output power and (b) drain efficiency ($f_{res} = 0.85$ GHz / 1.75 GHz, $Q_u = 8.5 / 7.5$, $L_{res} = 0.5$ nH, $I_{dd} = 1.12$ A)
4.3 Circuit Design

4.3.1 Variable Resonator Using Off-chip Inductor

A. Band-Switching Capacitor (BSC)

Figure 4.7 shows a basic concept of a BSC for the variable resonator of the multiband CMCD PA. In order to provide a switch control voltage independent of the instantaneous power supply voltage, the switch is inserted between two metal-insulator-metal (MIM) capacitors. When the switch is closed as shown in Figure 4.7 (a), the MIM capacitors dominate the resonance frequency. In this case, AC voltage swing with a half of the peak voltage (4.5 V for our design) and DC bias voltage ($V_{c,DC}$) are applied to each MIM capacitor. When the switch is open as shown in Figure 4.7 (b), the frequency is decided by the off-capacitance of the switch and the AC voltage swing is applied to the switch (9 V for our design). Since the switches need to tolerate 9 V peak voltage, two 3.3 V NMOSFETs are connected in series.

![Diagram of BSC](image)

Figure 4.7: Basic concept of BSC for variable resonator of multiband CMCD PA.
Three types of BSCs using two stacked FET switches are compared, where Figure 4.8-Figure 4.10 (a) and (b) are circuit configurations and simulated voltage waveforms, respectively. In order for the switches to be closed / open, the supply voltage (3.3 V) / 0 V are applied to the gates of the FETs through resistors. In the simulation, the switches are open and 9 V peak voltage is applied.

In Figure 4.8 (a), the bodies of the FETs are tied to GND and the drains / sources are 0 V biased through resistors. $V_{ds}$ is the drain-source voltage of a FET, $V_{gd}$ and $V_{gs}$ are the gate-drain and gate-source voltages, and $V_{bd}$ and $V_{bs}$ are the body-drain and body-source voltages. In Figure 4.8 (b), the carrier frequency and the DC supply current of the CMCD PA are 1.85 GHz and 1.24 A, respectively, where the peak voltage is approximately 9 V. From the results, the body-drain becomes higher than the threshold voltage ($\sim 0.7$ V) of the parasitic NPN bipolar junction transistor (BJT) of the FET and the BJT turns on in almost half of the period, which causes the efficiency degradation.

In Figure 4.9 (a), large resisters are inserted to the body to prevent the base current of the parasitic BJT. However, the FET itself turns on because $V_{gd}$ and $V_{gs}$ become higher than the threshold voltage ($\sim 0.7$ V) of the FET alternatively as shown in Figure 4.9 (b). It also causes the efficiency degradation.

To overcome the issue, the drain, source and body of the FET are biased to the supply voltage (3.3 V) through the resistors when the switches are open as shown in Figure 4.10 (a). Using the configuration, $V_{gd}$ and $V_{gs}$ are much lower than 0.7 V as shown in Figure 4.10 (b).
Figure 4.8: (a) Circuit configuration and (b) voltage waveforms of BSC with two stacked FET switches where bodies of FETs are tied to ground, where $f_c = 1.85$ GHz and $I_{dd} = 1.24$ A.
Figure 4.9: (a) Circuit configuration and (b) voltage waveforms of BSC where drains, sources and bodies of switches are tied to ground through large resistors, where $f_c = 1.85$ GHz and $I_{dd} = 1.24$ A.
Figure 4.10: (a) Circuit configuration and (b) voltage waveforms of BSC where drains, sources and bodies of switches are tied to supply voltage through large resistors when switches are open, where $f_c = 1.85$ GHz and $I_{dd} = 1.24$ A.
The preliminary simulated output power and drain efficiency of the multiband CMCD PA are summarized in Table 4.1. From these results, we decided to use the circuit configuration shown in Figure 4.10 for the 1.5th generation CMCD PA.

Table 4.1: Preliminary simulated output power and drain efficiency of multiband CMCD PA, where \( f_c = 1.85 \text{ GHz} \), \( I_{dd} = 1.24 \text{ A} \), \( V_{gg2} = 2.9 \text{ V} \) and BSC is open.

<table>
<thead>
<tr>
<th></th>
<th>( P_{out} ) (dBm)</th>
<th>( \eta ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 4.8</td>
<td>33.4</td>
<td>58.9</td>
</tr>
<tr>
<td>Figure 4.9</td>
<td>28.8</td>
<td>32.3</td>
</tr>
<tr>
<td>Figure 4.10</td>
<td>33.8</td>
<td>66.2</td>
</tr>
</tbody>
</table>

**B. Variable Resonator Using Bonding Wire Inductor**

As discussed in Section 4.2.1, the required inductance of the variable resonator is 0.5 nH. When an off-chip air-core inductor with such a small-value is used, the load impedance of the CMCD PA is transformed to significantly higher than 12.5 \( \Omega \) due to series parasitic inductance of output bonding wires. Therefore, it is important to place the inductor of the resonator close to the BSC. In this work, we success to realize a variable resonator for the CMCD PA using a bonding-wire inductor. In addition, the quality factor of the bonding wire is finite [77], especially when its length is very short. In order to improve the quality factor, we decided to use several bonding wires in parallel.

Figure 4.11 shows shape of a bonding wire, whose inductance is simulated using the bonding wire model of Agilent Advanced Design System (ADS). The simulated inductance of the bonding wire is 1.5 nH, and the unloaded quality factors are 31 (0.85 GHz) and 45 (1.75 GHz), respectively. By changing the shapes, bonding wires with different inductances and quality factors are obtained.
Figure 4.11: Shape of bonding wire inductor, where simulated inductance is approximately 1.5 nH.

To simulate the loss of the variable resonator, a simple model is used as shown in Figure 4.12. By increasing the number of the bonding wire connected between the output pads in parallel ($N_{bw}$), (where the inductance of each wire is adjusted to be $N_{bw} \times 0.5$ nH,) the loss of the variable resonator is reduced. It is because the structure decreases the effect of the parasitic resistance ($R_l$), originated in the contact resistance between wire and pad and series resistance of the metal layer (although the unloaded quality factor of the bonding wire does not change). The series resistance of the capacitor ($R_c$) is calculated from

$$ R_c = \frac{1}{2\pi f_{res} C_{res} Q_c} $$

(4-10)

where $Q_c$ is the unloaded quality factor of the capacitor.
Figure 4.12: Simple model of variable resonator.

Figure 4.13 shows the simulated equivalent efficiencies calculated from the losses of the variable resonator model. Based on the measurement, $C_{res}$ are 66 pF (closed) and 13 pF (open), where corresponding $f_{res} = 0.85$ GHz and 2 GHz. The frequency is slightly higher than the target frequencies because the parasitic capacitance of the stacked FET ($C_p = 4$ pF) is not taken into account. $Q_c$s are 12 (closed) and 9 (open), and $R_l$ is 0.2 $\Omega$. From the results, the efficiency degradation is small enough when the number of the bonding wires is three.

Figure 4.13: Simulated efficiency vs number of bonding wires of variable resonator, $f_{res} = 0.85$ GHz and 2 GHz.
4.3.2 On-board Guanella Reverse Balun (GRB)

Figure 4.14 (a) shows an equivalent circuit of GRB. Here the differential port of the original Guanella balun [16] is exchanged for the single-end. The balun circuit is based on the combination of two 1-to-1 transformers whose differential impedance is 25 \( \Omega \) and whose common-mode impedance is infinite. At the input, the transformers are connected in parallel, providing a differential input impedance of 12.5 \( \Omega \), and infinite common mode input impedance. At the output, the transformers are connected in series, providing a single-ended impedance of 50 \( \Omega \). The balun design provides infinite bandwidth if it is implemented with ideal transformers. To realize this balun, 25 \( \Omega \) coupled transmission lines on the PCB were used, as shown in Figure 4.14 (b). For differential signals applied between top and bottom lines, a plane of symmetry at the midpoint between lines becomes a virtual ground. The 25 \( \Omega \) coupled transmission line can be seen to consist of two 12.5 \( \Omega \) microstrip transmission lines on virtual ground.

![Diagram of GRB and 25 \( \Omega \) coupled transmission line](image)

Figure 4.14: (a) equivalent circuit of GRB and (b) representation of 25 \( \Omega \) coupled transmission line.
The layout of the doughnut-shape GRB is shown in Figure 4.15. Using a doughnut shape, it is possible to minimize the parasitic components at the connections of the two transmission lines, which cause narrow bandwidth and loss, because the inputs or outputs of the transmission lines face each other. Nevertheless, vias connecting top and bottom metals have extra parasitic inductance. To extend the bandwidth, a 4 pF chip capacitor was mounted on the bottom layer. The outer radius of the doughnut-shaped balun is 11.8 mm. The size of the balun can be reduced using a circuit board with higher permittivity and permeability.

![Figure 4.15: (a) Top metal and (b) bottom metal layouts of GRB.](image)

**4.3.3 Fully Integrated Variable Resonator**

**A. Study of DC Current Supply Circuit Configuration**

In the 1st and 1.5th generation CMCD PAs, DC current is supplied from two current sources realized by two air-core inductors, but it is desirable to use one current source for a fully integrated CMCD PA.
Figure 4.16 shows DC current supply circuits of (a) one side and (b) center tap, where $R_s$ is parasitic resistance of $L_{res}$. In Figure 4.16 (a), when node-P is shorted, the voltage drop from node-N to node-P is 0 V. In case that node-N is shorted, the voltage drop from node-P to node-N is $I_{dd} R_s$. Since the IR drop generates a common-mode voltage, it does not affect the output power and efficiency directly. However, the voltage headroom of the amplifier is consumed. In addition, if the output impedance of the current source is not high enough, not only common-mode output current is generated but also the loss of the differential output signal increases.

On the other hand, in Figure 4.16 (b), when either node-P or node-N is shorted, the voltage drop is $I_{dd} R_s / 2$ and no additional headroom is needed. The loss of the differential signal also supposed to be small because the current source is connected at the virtual ground of the differential signal. Therefore, the center-tap configuration is used for the demonstration.

![Figure 4.16](image-url)

Figure 4.16: Configuration of DC current supply circuit with one current source and voltage waveform of CMCD amplifier. (a) one side and (b) center tap.
**B. On-chip Transformer Balun**

In this section, a design of on-chip baluns is discussed, where the balun works as not only differential-to-single-end converter but also an inductor of a resonator.

Three different on-chip 1-to-4 baluns are compared, where their occupied areas are approximately 0.2 mm$^2$. Figure 4.17 shows (a) layout and (b) EM-simulated self-inductances / quality factors / coupling coefficient of an on-chip GRB, where Agilent Momentum is used for EM simulation. In the simulation, 6 μm thick Al metal layer is used with the line width of 25 μm and the space of 5.5 μm. The on-chip GRB consists of two 1-to-1 transformers instead of coupled transmission lines as shown in Figure 4.14. The structure has relatively high coupling coefficient, but the self-inductance (1.5 nH) is much higher than the target (0.5 nH).

Figure 4.18 shows (a) layout and (b) simulated results of a symmetry interwound transformer balun [76], where the primary inductor is single spiral and the secondary is double spiral. To increase the coupling coefficient, the single spiral is inserted between the double spirals. The occupied area is reduced and the secondary quality factor of the balun is relatively high, but the coupling coefficient decreases and the self-inductance (0.8 nH) is still slightly higher.

Figure 4.19 shows (a) layout and (b) simulated results of a symmetry step-up transformer balun [76], where a triple spiral is applied as the primary inductor. As a result, the coupling coefficient increases and the self-inductance becomes approximately 0.5 nH.
Figure 4.17: (a) Layout and (b) simulated results of on-chip GRB.
Figure 4.18: (a) Layout and (b) simulated results of on-chip interwound transformer balun.
Figure 4.19: (a) Layout and (b) simulated results of on-chip step-up transformer balun.
The equivalent efficiencies are also evaluated using these on-chip baluns. The simulation setup is shown in Figure 4.20 and the simulated results are summarized in Table 4.2. In the simulation setup, the capacitances ($C_{res}$) are adjusted for the resonance frequency ($f_{res}$) to be 0.85 GHz and 1.75 GHz, where the unloaded quality factors are set to be 12 and 9, respectively. From the results, the efficiencies of the interwound and step-up transformer baluns are twice higher than that of the GRB. From $C_{res}$ and $f_{res}$, the equivalent $L_{res}$ is also calculated and we find the step-up structure has $L_{res}$ of approximately 0.5 nH. By decreasing the size of other baluns, the equivalent $L_{res}$ may be reduced, but the efficiency tends to be degraded. Therefore, the step-up structure is selected for the demonstration.

![Figure 4.20: Layout of on-chip step-up transformer balun.](image)

<table>
<thead>
<tr>
<th>Type of balun</th>
<th>Size $X \times Y$ (um$^2$)</th>
<th>$C_{res}$ (pF) / $Q_c$</th>
<th>Equivalent $L_{res}$ (nH)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guanella Reverse</td>
<td>300 x 620</td>
<td>43.0 / 12, 12 / 9</td>
<td>0.82 / 0.69, 16.9 / 28.9</td>
<td></td>
</tr>
<tr>
<td>Interwound Transformer</td>
<td>460 x 460</td>
<td>38.5 / 12, 9.5 / 9</td>
<td>0.91 / 0.87, 33.9 / 48.0</td>
<td></td>
</tr>
<tr>
<td>Step-up Transformer</td>
<td>460 x 460</td>
<td>73.0 / 12, 18 / 9</td>
<td>0.48 / 0.46, 32.5 / 55.6</td>
<td></td>
</tr>
</tbody>
</table>

**C. Revision of BSC**

In the measurement of the 1.5th CMCD PA, unexpected leakage current flows from 3.3 V DC voltage supply when the BSC is open. The mechanism of the current...
leakage is explained using Figure 4.21. Figure 4.21 (a) shows the structure of the switch used in the BSC of the 1.5th CMCD PA, where the switch turns off and the supply voltage (3.3 V) is applied to the body and deep N-well. The Silicon substrate is grounded and a parasitic PNP BJT exists. Here, if the large voltage swing is applied to the body, the voltage difference between the body (emitter) and deep N-well (base) becomes higher than the threshold voltage of the BJT and current flows from body to substrate (collector).

Figure 4.21 (b) shows the route of the current. From 3.3 V power supply, current flows to the parasitic BJT through inverter and resistor. The measured current was approximately 500 μA and it can cause the breakdown of the FET switch and the loss of the PA.

Figure 4.22 shows the improved BSC, where the body is biased to the ground, while the drain and source are still tied to the supply voltage when the switches are open. (a) is the circuit configuration and (b) is the voltage waveforms ($V_{ds}$, $V_{gd}$, $V_{gs}$, $V_{bd}$ and $V_{bs}$). The carrier frequency and DC current of the CMCD PA are 1.85 GHz and 1.24 A, respectively, where the peak voltage is approximately 9 V. From the results, the amplitude of $V_{ds}$ is less than 4 V and no FET switch turns on because the $V_{gs}$ and $V_{gd}$ are less than 0.7 V.

Figure 4.23 shows the simulated leakage current vs output power, where a parasitic PNP BJT is modeled. From the results, the simulated leakage current can be suppressed using the new bias condition (although the simulated leakage current is smaller than the measurement due to inaccurate model parameters of PNP BJT.
Figure 4.21: (a) Parasitic BJT of switch and (b) route of leakage current used in BSC of 1.5th CMCD PA.
Figure 4.22: (a) Circuit configuration and (b) voltage waveforms of BSC where body is biased to ground, while drain and source of switches are tied to supply voltage through large resistors when switches are open, where \( f_c = 1.85 \) GHz and \( I_{dd} = 1.24 \) A.
Figure 4.23: Simulated leakage current vs output power when all unit-cells are open, where $f_c = 1.85$ GHz and $I_{dd} = 1.24$ A.

Using the new bias condition, the ON/OFF capacitance ratio and unloaded quality factor of the BSC are also improved. Figure 4.24 shows the simulated (a) capacitance and (b) quality factor over frequency when all BSC unit-cells are open. The solid line is the new bias condition ($V_b = 0$ V) and the broken line is the previous bias conditions ($V_b = 3.3$ V). From these results, the capacitance is 0.9 times lower and the quality factor is 1.1 times higher.
Figure 4.24: Simulated (a) capacitance and (b) quality factor over frequency when all BSC unit-cells are open.
D. Revision of Variable Resonator

Even if the capacitance ratio of the BSC increases using the new bias condition, the resonance frequency is still shifted lower than the original design due to the parasitic capacitance of the bonding pads and routing. Therefore, circuit design of variable resonator is revised.

The revision of the variable resonator is summarized in Table 4.4. By reducing the number of the BSC unit-cells from 64 to 48, the minimum / maximum resonance frequencies are shifted to 0.94 / 1.68 GHz from 0.84 / 1.54 GHz.

Table 4.3: Revision of variable resonator circuit.

<table>
<thead>
<tr>
<th></th>
<th>$L_{\text{res}}$ (nH)</th>
<th>Num. of BSC Cell</th>
<th>$C_{\text{res}}$ (pF)</th>
<th>$C_p$ (pF)</th>
<th>$f_{\text{res}}$ (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>All Closed</td>
<td>All Open</td>
<td>All Closed</td>
<td>All Open</td>
</tr>
<tr>
<td>1.5th Generation CMCD PA</td>
<td>0.5</td>
<td>64</td>
<td></td>
<td>61.6</td>
<td>10.4</td>
</tr>
<tr>
<td>2nd Generation CMCD PA</td>
<td>0.5</td>
<td>48</td>
<td></td>
<td>46.2</td>
<td>7.0</td>
</tr>
</tbody>
</table>

Finally, Figure 4.25 shows the circuit schematic of the variable resonator for the 2nd generation CMCD PA. Whole resonator and balun are integrated into Silicon.

Figure 4.25: Circuit schematic of band-switching capacitor and conceptual layout of on-chip transformer balun for 2nd generation CMCD PA.
4.4 Chip and Board Fabrication

4.4.1 Band-Switching Capacitor for On-wafer Measurement

Since the parasitic components of the BSC significantly affect the performance of the CMCD PA, 1/8 size BSC is fabricated for on-wafer measurement to evaluate the capacitances and unloaded quality factors when the switches are closed and open. Figure 4.26 shows the circuit schematic. The BSC consists of small unit-cells and the number of unit-cells is 8. Since the BSC is inserted between parallel lines, the transition loss can be evaluated directly. Large resistors are inserted between the input ports and grounds to avoid from the breakdown of MIM capacitor in fabrication. Figure 4.27 shows (a) unit-cell and (b) entire layouts of the BSC for on-wafer measurement. The length of the metal layer is routed to be as short as possible.

Figure 4.26: Circuit schematic of BSC for on-wafer measurement.
Figure 4.27: (a) Unit-cell and (b) entire layouts of BSC for on-wafer measurement.
4.4.2 Guanella Reverse Balun

To supply DC current to CMCD PA, a bias circuit including choke inductors and DC block capacitors are needed for on-board balun as shown in Figure 4.28. Air-core inductors and chip capacitors are used and the inductance and capacitance values are experimentally designed not to affect the loss and impedance of the balun in the cellphone frequency bands. Although the cable to supply DC current to CMCD PA caused low common-mode impedance of the balun at the specific frequency, the air-core inductor of 27 nH improved it.

Figure 4.28: Additional circuits for implementing with CMCD PA.

Figure 4.29 shows the photos of a fabricated GRB, where (a) is top view and (b) is bottom view. Roger 4305B ($\varepsilon_r = 3.48$) with 0.508 mm (20 mil) thickness is used. In the measurement, 50 $\Omega$ transmission lines are de-embedded using a port extension.
technique, especially carefully for the input because the differential impedance is 12.5 $\Omega$ instead of 100 $\Omega$.

Figure 4.29: Photos of fabricated GRB. (a) Top metal. (b) Bottom metal.

4.4.3 1.5th Generation CMCD PA

Figure 4.30 shows the circuit schematic of the overall transmitter, which consists of 1.5th generation CMCD PA and 2nd generation buck converter. These circuits are fabricated as two individual chips. A differential RF carrier signal is delivered from the
CMCD PA and a GRB is provided for differential-to-single and 1-to-4 impedance conversion. The buck converter supplies the DC current to the CMCD PA. The 1.5th generation CMCD PA contains not only a driver stage and stacked switching stage, but also BSCs and bond wire inductors, which work together as a band-switching resonator. The BSCs consist of 64 cells (21-74 pF) including $C_p$. The number of closed BSCs is binary-controlled from outside of the chip to cover the entire band. Three parallel bond wires are used as inductors and the total inductance is around 0.5 nH. The unloaded quality factors of the variable resonator are 8.5 (0.85 GHz) and 7.5 (1.75 GHz), which limit system efficiency.

Figure 4.30: Circuit schematic of multiband digital polar transmitter with band-switching resonator.
Figure 4.31 shows the die photos for the 1.5th generation CMCD PA chip. The chip was fabricated using the L-Foundry 0.15 \( \mu \)m RF CMOS process containing six nominal and one 6 \( \mu \)m thick Al metal layers. The die size is \( 1.7 \times 1.5 \) mm\(^2\). The differences between the 1st and 1.5th generation chips are the thick metal layer and extra pads for the bond wire inductor.

![Chip photo of 1.5th generation CMCD PA (1.7 mm \times 1.5 mm)](image)

Figure 4.31: Chip photo of 1.5th generation CMCD PA (1.7 mm \times 1.5 mm)

Figure 4.32 shows the photo of the bonding wire inductors. The length of each wire is around 2.3 mm (90 mil). Since the loops does not overlap each other, mutual couplings should be very small.
4.4.4 2nd Generation PCB (1)

In this section, an off-chip circuit design related with the multiband operation of the digital polar transmitter is discussed. Other topics of the 2nd generation digital polar transmitter will be described in Chapter 5.

A. Implementation of DC Supply from Buck Converter

A CMCD PA requires high common-mode load impedance at the even-harmonic frequencies, which is directly affected by the output impedance of the buck converter. Ideally the output impedance is very large due to the envelope inductor. However, an actual inductor has a self-resonance frequency, and a power supply cable used to connect buck converter to CMCD PA also have parasitic components. These parasitic components can degrade the output impedance.
Figure 4.33 shows the possible configurations of the output inductor of the buck converter. In Figure 4.33 (a), a large air core inductor is placed at the output of the buck converter and the inductor is connected to the CMCD PA directly. In Figure 4.33 (b), two air core inductors are placed at near the CMCD PA and buck converter, respectively. The configuration can minimize the effect of the cable.

Figure 4.33: Configurations of DC power supply: (a) single inductor and (b) two inductors in series.
Figure 4.34 shows the simulated impedance of the inductors using the S-parameters provided from the Coil Craft. For simplicity, the cable impedance is neglected. From the results, the impedance of two series inductors at the frequency of 1.8 GHz is very small due to a resonance between two inductors. The frequency is the second harmonic of 0.9 GHz carrier frequency and the resonance causes the efficiency degradation.

![Impedance Graph]

Figure 4.34: Simulated impedance of the inductors using the S-parameters.

4.5 Experimental Results

4.5.1 Band-Switching Capacitor (On-wafer)

Figure 4.35 shows the measured characteristics of the BSC cell. Capacitances with the switch closed and open are shown in Figure 4.35 (a), and Figure 4.35 (b) shows the measured quality factors (when the one port is grounded). The number of unit cells is eight for on-wafer evaluation and the parasitics of the pads are de-embedded. From these results, the capacitances are 7.7 pF (closed, 0.85 GHz) and 1.3 pF (open, 1.75 GHz) and the quality factors are 12 and 9, respectively, as mentioned in the previous section. From
Eq. (4-1), the resonance frequency is decided by the capacitances although actually they include shunt capacitances between the bottom plate of the MIM capacitor and the ground, which are 0.5 pF (0.85 GHz) and 0.3 pF (1.75 GHz).

Figure 4.35: Measured characteristics of 9 V BSC cells: (a) capacitance and (b) quality factor (the number of unit cell is 8 and pads are de-embedded).
Figure 4.36 shows comparison between electromagnetic (EM) simulated and measured (a) capacitances and (b) quality factors. The simulated capacitance and quality factor is calculated from the S-parameters of EM simulation, which includes pads (See Appendix A). The simulated results are in good agreement with the measured results.

(a)

(b)

Figure 4.36: Comparison between simulated and measured capacitance and Q of BSC (the number of unit cell is 8 and pads are included).
4.5.2 Guanella Reverse Balun

Figure 4.37 shows measured differential-mode insertion loss and input return loss of the GRB. In the low band (0.7-1.0 GHz), < 0.95 dB insertion loss and > 13.5 dB return loss were achieved. In the high band (1.6-2.0 GHz) < 0.9 dB and > 15 dB are obtained. The insertion loss over a narrow region in the vicinity of 1.1 GHz is degraded to approximately 2.5 dB because of radiation loss. This resonance frequency is designed to be out-of-band for cellular applications.

![Figure 4.37: Measured insertion loss and input return loss of GRB over frequency. (Input: $Z_0 = 6.25 \Omega$ each side, Output: $Z_0 = 50 \Omega$)](image)

Figure 4.38 shows measured input impedances of the GRB for the differential and common-modes. The common-mode impedance of each port for amplifier operation, given the 6.25 $\Omega$ differential-mode impedance, is > 150 $\Omega$ and > 60 $\Omega$ in the low and high bands respectively.
Figure 4.38: Measured differential and common mode impedances over frequency of GRB. (Input: $Z_0 = 6.25 \, \Omega$ each side, Output: $Z_0 = 50 \, \Omega$)

4.5.3 1.5th Generation CMCD PA

Figure 4.39 shows the CW measured and simulated output power and “driver and final-stage efficiency”, which is defined as the ratio between the output power and the DC power dissipation of the driver and final stages, of the CMCD PA module (with external power supply). All switched capacitances are closed for the low band and open for the high band. The DC currents are 0.5 A and 1.0 A. The symbols are measured results and the lines are transient simulated results using SPICE FET models with chip parasitic extraction, EM simulations of S-parameters of MIM capacitors, routing and pads, bond wire model, and equivalent circuits of the on-board balun (See Appendix A). The measured results are in good agreement with the simulations. By increasing DC current, the peak output powers of 31 / 30 dBm are achieved at 0.8 / 1.65 GHz respectively, where the drain efficiencies are 35 / 31 %, and the driver and final-stage efficiency are 33 / 29 % (although they are not shown in the figure).
Figure 4.39: Measured and simulated (a) output power, and (b) driver / final-stage efficiency of 1.5th generation CMCD PA over frequency when one-tone signal is delivered. (symbol: measurement, line: simulation, $P_{in} = 20 / 24$ dBm, $V_{gg2} = 2.8 / 2.9$ V)
Figure 4.40 shows the measured and simulated output power vs DC current, where the carrier frequencies are (a) 0.85 GHz and (b) 1.65 GHz (instead of 1.75 GHz due to shifting the peak frequency lower in the high band). From the results, the peak output powers are 30.7 dBm and 30.0 dBm, respectively, and a multiband CMOS PA with over 1 W output power is realized. The measured output powers in back-off are also in good agreement with the simulation.

![Figure 4.40: Measured and simulated output power vs DC current of 1.5th generation CMCD PA at (a) 0.85 GHz and (b) 1.65 GHz. (symbol: measurement, line: simulation, $P_{in} = 20/24$ dBm, $V_{gg2} = 2.8/2.9$ V)](image)

Figure 4.41 shows the driver and final-stage efficiency vs output power at the frequencies of (a) 0.85 GHz and (b) 1.75 GHz. From the results, the peak driver and final-stage efficiencies of 34 % and 30 % are achieved, respectively. There is a discrepancy between the measured and simulated efficiencies at the peak output in the high band. One of possible reasons is the effect of the ground bouncing, but more studies are required.
Figure 4.41: Measured and simulated driver / final-stage efficiency vs output power at (a) 0.85 GHz and (b) 1.65 GHz. (symbol: measurement, line: simulation, $P_{in} = 20 / 24$ dBm, $V_{ggs} = 2.8 / 2.9$ V)

The theoretical (a) output power and (b) drain efficiency over frequency are compared with the measured and simulated results, as shown in Figure 4.42. The theoretical curves are calculated using Eqs. (4-7), (4-9) and measured balun losses ($Loss_{GRB}$), where the DC current is 1.0 A. $C_p$ of 11 pF is used instead of 5 pF based on both simulation and measurement. $C_{res}$ are 62 pF / 10 pF, and $Q_u$ is 8.5 / 7.5 when the BSC is closed and open, respectively. $L_{res}$ is 0.5 nH and $R_{SW} = 0.65$ Ω. The input impedances ($R_L$) are obtained from measured impedance of the GRB and simulated bonding wire inductance. From the results, the theoretical frequency dependences are similar to the measured and simulated results and errors of the output power and drain efficiency are less than 3 dB and 10 %, respectively. Possible reasons of the difference are the losses due to the interconnects and pads of the chip and the bonding wires, but the calculated results should be useful for 1st order estimation.
Figure 4.42: Comparison between theory, simulation and measurement, where (a) output power and (b) drain efficiency of 1.5th generation CMCD PA are calculated using Eqs. (4-7) and (4-9), respectively. (solid line: theory, broken line: simulation, symbol: measurement, C64 / C0, $I_{dd} = 1.0$ A, $P_{in} = 20 / 24$ dBm, $V_{ggs} = 2.8 / 2.9$ V)

### 4.5.4 1.5th Generation Digital Polar Transmitter (Single-tone)

Figure 4.43 shows the measured frequency dependence of (a) output power and (b) overall efficiency of the 1.5th generation digital polar transmitter with 50% and 75% duty cycle and 47 MHz fixed clock DPWM ($f_0 = 3000$ MHz, $N_{be} = 6$). The DPWM signal was generated from the pulse pattern generator, and the RF carrier signal (without PM) was applied from the vector signal generator. The numbers of closed BSC cells are
64 (C64), 32 (C32), 16 (C16), 8 (C8) and 0 (C0) for the different cases. DC power dissipations of the buck converter and of the driver stage are included in the overall efficiency. By adjusting the resonance frequency of the CMCD, the output power is 23.5-26.1 dBm in the 0.7-1.8 GHz range at 50 % duty cycle. With increasing frequency, the overall efficiency decreases due to the power consumption of the driver stage. When the duty cycle is 75 %, the output power increases approximately 29 dBm and the overall efficiency becomes 23-28 %.

![Figure 4.43](image)

Figure 4.43: Measured CW performance of 1.5th generation digital polar transmitter over frequency. (a) Output power and (b) overall efficiency ($P_{in} = 20 / 24$ dBm, $V_{g2} = 2.8 / 2.9$ V, $V_{dd} = 3.3$ V, $f_{sw, ave} = 47$ MHz).
Figure 4.44 shows the output power at (a) 0.85 GHz (C64 between Band V and Band VIII) and (b) 1.75 GHz (C0, Band III) when the duty cycle of DPWM is swept. The envelope modulation is generated based on $f_{sw\_ave}$ of DPWM = 47 MHz ($N_{be} = 6$) and 188 MHz ($N_{be} = 4$) with $f_0 = 3000$ MHz. Theoretical curves, calculated from Eqs. (3-7), (3-25) and (3-33), are also shown for reference. In $f_{sw\_ave} = 47$ MHz, the output powers are 30.2 / 28.9 dBm respectively at 87.5% duty cycle. When $f_{sw\_ave}$ increases, the linearity of the output power is degraded because the buck converter cannot deal with very narrow pulses. The measured output powers are approximately 0.5 dB and 1.5 dB lower than the theoretical curves at 0.85 GHz and 1.75 GHz respectively, which are similar to the results of only CMCD PA.

![Graph](image)

**Figure 4.44:** Measured and calculated CW output power of 1.5th generation digital polar transmitter over frequency, where $f_c$ = (a) 0.85 GHz / (b) 1.75 GHz, $P_{in} = 20 / 24$ dBm, $V_{gg2} = 2.8 / 2.9$ V, $V_{dd} = 3.3$ V, $f_{sw\_ave} = 47$ MHz / 188 MHz, $Q_u = 8.5 / 7.5$, $Q_L = 2.5 / 2.0$, $R_L = 9.2 / 15.2$ Ω, $Loss\_GRB = 0.73$ dB / 0.84 dB, $R_{SW} = 0.65$ Ω and $R_{BC} = 0.3$ Ω.
Figure 4.45 shows the overall efficiency at (a) 0.85 GHz and (b) 1.75 GHz. In $f_{sw\text{ ave}} = 47$ MHz, the overall efficiencies are 27.1 / 25.6% respectively at 87.5% duty cycle. The peak PAE drops to 24.5 / 18.3% due to 20.0 / 23.5 dBm external input power required, as needed to maintain proper switching operation of the CMCD in the test-bench, although in a realistic application scenario the input power would be considerably lower, since it would come from an on-chip digital buffer. When $f_{sw\text{ ave}}$ increases, the peak overall efficiencies are 24 / 22 % respectively at 75% duty cycle. There is a trade-off between the linearity / efficiency and the RX band noise / peak spurs.

![Figure 4.45: Measured CW overall efficiency of 1.5th generation digital polar transmitter over frequency, where carrier frequencies are (a) 0.85 GHz and (b) 1.75 GHz. ($P_{in} = 20 / 24$ dBm, $V_{gg2} = 2.8 / 2.9$ V, $V_{dd} = 3.3$ V, $f_{sw\text{ ave}} = 47$ MHz / 188 MHz).]
4.5.5 2nd Generation Digital Polar Transmitter (Single-tone 1)

A. Frequency Dependence

Figure 4.46 shows (a) output power and (b) overall efficiency of the 2nd generation digital polar transmitter over frequency \( f_c \) with 75% and 100% duty cycle and 47 MHz \( (= f_{sw}) \) fixed clock DPWM. The numbers of closed SC cells are 48 (C48), 24 (C24), 13 (C13) and 0 (C0) for the different cases. DC power dissipations of the buck converter \( (V_{dd} = 3.6 \text{ V}) \) and of the driver stage (1.8 V) are included in the overall efficiency. RF carrier power \( (P_{in}) \) of 10-11 dBm is applied to maintain proper switching operation (in a way that would not be necessary in a fully digital chipset.) By adjusting the resonance frequency of the CMCD, the output power is 26.8-29.0 dBm at 100 % duty cycle in the 0.75-2 GHz range. With decreasing frequency, the overall efficiency decreases due to the increased loss of the transformer balun. The peak output power and overall efficiencies are 27.5 / 29.0 dBm and 13.2 / 22.2 % at 0.85 / 1.75 GHz, respectively.

In order to confirm if the discussion in Section 4.4.4 is valid, characteristics of the digital polar transmitter are evaluated using the DC supply shown in Figure 4.33 (b) instead of Figure 4.33 (a). Figure 4.47 shows the measured (a) output power and (b) overall efficiency over frequency. From the results, the output power and overall efficiencies are degraded at 0.9 GHz (and 1.85 GHz). Low common-mode impedance of the DC supply at 1.8 GHz (2nd harmonic frequency) should cause these degradations (, and the impedance can be low at 3.5 GHz although no simulated results are available).
Figure 4.46: (a) Output power and (b) overall efficiency of 2nd generation digital polar transmitter over frequency. ($P_{in} = 10 / 11$ dBm, $V_{gg2} = 2.8 / 2.9$ V, $V_{dd} = 3.6$ V, $f_{swave} = 47$ MHz)
Figure 4.47: (a) Output power and (b) overall efficiency of 2nd generation digital polar transmitter over frequency using DC supply circuit shown in Figure 4.33 (b). ($P_{in} = 10 / 11$ dBm, $V_{gg2} = 2.8 / 2.9$ V, $V_{dd} = 3.6$ V, $f_{sw,ave} = 47$ MHz)
B. Leak Current through Triple-well Substrate Due to High Voltage Swing

In order to confirm the effect of the BSC circuit revision discussed in Section 4.3.3, leakage currents from the body / deep N-well of the BSC through Silicon substrate are evaluated using of the 1.5th and 2nd digital polar transmitters.

Figure 4.48 shows the leakage current vs output power with different carrier frequencies, where the body of the BSC is tied to (a) $V_{dd}$ (1.5th generation digital polar transmitter) and ground (2nd generation digital polar transmitter) when the BSC is open. The numbers of BSC cells are 64 and 48, respectively. From the results, peak leakage current of the 1.5th generation transmitter is achieved to higher than 450 uA, while that of the 2nd generation digital transmitter is significantly reduced to less than 140 uA although the current still increases as the output power increases. In order to completely suppress the leakage current, it is considered to use SOI substrate.

![Leakage current vs output power](image)

Figure 4.48: Leakage current vs output power of CMCD PA where body of BSC is tied to (a) $V_{dd}$ and (b) ground when the BSC is open. The numbers of BSC cells are 64 and 48.
4.6 Summary

In this paper, a multiband digital polar modulation transmitter with a band-switching resonator has been demonstrated. The designed 1.5th transmitter comprises a 0.7-1.8 GHz CMCD CMOS PA with over 1W output power, and a buck converter with over 2.5 W output power and up to 200 MHz clock rate. At 0.85 / 1.75 GHz, 30.2 / 28.9 dBm CW output powers and 27.1 / 25.6% overall efficiency are achieved, respectively, when the duty ratio is 87.5% and the switching frequency of the buck converter is 46 MHz. The 2nd generation transmitter, whose output balun is integrated, achieved 27.5 / 29.0 dBm CW output powers and 13.2 / 22.2 % overall efficiency at 0.85 / 1.75 GHz.

The peak efficiency of the fabricated PA is a little lower compared with commercial single-band PAs. It is because the quality factors of the BSC are approximately 10. However, if high resistivity silicon-on-insulator (HRSOI) technology, which has been already used for several products, is applied, the quality factors increase up to 30 and significant efficiency improvement is expected.

4.7 Acknowledgement

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Some of the material in Chapter 4 is as it appears in "Digital-controlled polar transmitter using a watt-class current-mode class-D CMOS power amplifier and Guanella
Chapter 5

Wide Power Dynamic Range Digital Switching Power Amplifier

5.1 Introduction

The next challenge is to establish the very large dynamic range of power control needed for use in handsets (up to 74 dB for WCDMA) with low DC power consumption. This is considered to be a major problem for polar modulation transmitters since these transmitters suffer from the feed-through of the constant envelope RF phase modulation signal.

In order to improve the feed-through issue, several approaches have been reported. In [19], [78] and [79], RF input power controls, such as input attenuator or quadrature modulation, are applied. These techniques are reliable, but flexibility and efficiency in back-off are sacrificed. In [11], [19], [75], [79]-[82], PA is partitioned into multiple unit cells and the output power is controlled by changing the number of active unit cells. However, the power dynamic range of this technique is only 40-50 dB. In [83], a variable attenuator with the dynamic range of 55 dB is reported. However, the
minimum loss of 0.6 dB causes the peak efficiency degradation and the 1 dB compression is only 21 dBm.

In this work, by combining the DC power controlling with unit-cell switching, extremely wide power dynamic range polar transmitter is demonstrated. Using the proposed architecture, it is possible to adjust the DC current density of each unit cell appropriately and maintain the operation point to be the triode region, which leads relatively high drain efficiency in back-off. In addition, a third state (attenuation) of the unit-cell operation is added into conventional two states (switching and open). This arrangement has negligible effect on peak output power and efficiency, because attenuation is done with the same FETs that are employed for output drive under high power operation.

Even if the wide dynamic range and high efficiency RF PA is realized, the DC power consumption of the buck converter as the envelope modulator degrades the overall efficiency. In order to improve the back-off efficiency of the buck converter, many techniques are reported. In [84]-[87], several adaptive dead-time control techniques are proposed. However, it is difficult to reduce the input DC current to less than the product of the output capacitance \((C_{\text{out}})\), supply voltage \((V_{dd})\) and switching frequency \((f_{\text{sw}})\) in back-off. In [88] and [89], PWM / pulse density modulation (PDM) dual-mode operation is reported. (It is noted that pulse frequency modulation is same as pulse density modulation). Using the PDM, the DC power consumption decreases in back-off, but the bandwidth of the envelope signal is limited.

In this work, a new operation mode, so called “charge sampling” [90], is introduced to the buck converter, which is a kind of switched capacitor techniques, such
as charge pumps [91], [92]. The operation mode reduces the DC power in back-off and the degradation of the peak efficiency can be omitted because it is possible to realize the charge-sampling mode using the same FETs for the DPWM mode.

Chapter 5 begins with studies of the architectures for wide power dynamic range polar transmitter. Next, the back-off efficiency improvement of the buck converter is discussed. After that, the design and implementation of the 2nd generation polar transmitter, incorporating new CMCD PA and buck converter, is explained, and the measured results are discussed.

5.2 Theoretical and Circuit Design of CMCD PA

5.2.1 Unit-cell Switching Technique

A. Basic Concept

Figure 5.1 shows a simple configuration of a wide power dynamic range CMCD PA, where DC current control and unit-cell switching technique are combined. According to the required output power, DC current supplied and state of each unit-cell amplifier are selected. When the output power is peak, all unit-cells are active and large DC current is supplied. With decreasing active unit-cells and supplied DC current, the output power goes down. Finally, by controlling that only one unit-cell is active and no DC current is supplied, the delivered RF power becomes extremely small. Using these operations, feed-through is improved because equivalent transistor size of final stage is reduced. In addition, it is possible to decrease the DC power dissipation of not only final state but also driver stage in back-off.
Figure 5.1: Efficiency improvement in back-off and feed-through reduction using unit-cell switching.

Major difference of conventional unit-cell switching PA, so called “digital PA”, is the operation point of each FET of unit-cell in back-off. Figure 5.2 shows the dynamic load lines of (a) conventional unit-cell switching and (b) combination of DC control and unit-cell switching when the number of switching unit-cell is changed. In both cases, the FETs of the unit-cells work as switches when all unit-cells are activated like solid black lines. In Figure 5.2 (a), with decreasing the number of active unit-cells, the DC current of each FET increases due to the load modulation effect and exceeds $I_{d_{\text{max}}}$ like gray broken lines, which results in the operation point of the FET turning on becomes the saturation region [79]. In this case, the FETs work as a current source and the efficiency is degraded. On the other hand, in Figure 5.2 (b), both supply voltage and number of unit-
cells are decreased and the FETs still work as switch. Therefore, the PA can maintain relatively higher efficiency.

Figure 5.2: Dynamic load lines of (a) conventional unit-cell switching and (b) combination of DC control and unit-cell switching when number of active unit-cells is changed.
**B. Derivation of Output Power and Efficiency**

Figure 5.3 shows equivalent circuits of driver and final stages of the proposed wide power dynamic range CMCD PA. A resonator consists of $L_{\text{res}}$ and $C_{\text{res}}$, where the unloaded quality factor is $Q_u$, and the load resistance is $R_L$. $N$ is the number of unit cells, which represent as a pair of switch with a series resistance $N R_{\text{on0}}$. $n$ is the number of switching unit cells and $N-n$ is the number of constant-open unit cells. $R_{\text{metal}}$ is the series resistance of the metal layer including the series resistance of the on-chip balun. For simplicity, DC current ($I_{dd}$) is supplied from an ideal buck converter, to which a pulse width modulated signal with the duty cycle ($D$) is applied.

![Diagram showing equivalent circuits of driver stage and final stage of unit-cell controlled CMCD PA.](image)

Figure 5.3: Equivalent circuit of driver stage and final stage of unit-cell controlled CMCD PA.

In this architecture, controlling the number of switching unit cells is equivalent to changing the series resistance of each switch. The series resistance can be expressed as
$R_{SW} = \frac{N}{n} \cdot R_{on} + R_{metal}$

(5-1)

where it is assumed the operation point of switch is the triode region. When the carrier frequency ($f_c$) is identical to the resonant frequency, $f_{res}$, of $L_{res}$ and $C_{res}$, from Eq. (3-7), the output power of the CMCD amplifier can be written as

$$P_{out} = \frac{2R_L I_{dd}^2}{\pi^2} \cdot \left( 1 - \frac{Q_L}{Q_a} \right)^2$$

(5-2)

Eq. (5-2) indicates the output power does not change directly by controlling $R_{sw}$ in the condition with constant $I_{dd}$. On the other hand, by controlling $R_{sw}$, $I_{dd}$ change due to the load modulation effect of the buck converter, where $I_{dd}$ is written as

$$I_{dd} = \frac{D \cdot V_{dd}}{R_{PA}}$$

(5-3)

where the load impedance from the buck converter is calculated from

$$R_{PA} = \frac{2}{\pi^2} \cdot \left( 1 - \frac{Q_L}{Q_a} \right) \cdot R_L + \frac{N}{n} \cdot R_{on} + R_{metal}$$

(5-4)

From Eq. (4-2), the DC power consumption of the final stage is calculated from
\[ P_{DC}(P_{out}, n) = P_{out} \sum_{k=1}^{\infty} \frac{1}{(2k-1)^2} \cdot \frac{1}{1+n_h(k)^2 Q_k^2} + \left( \frac{N}{n} R_{out} + R_{metal} \right) I_{dd}^2 \]  

(5-5)

where \( n_h(k) = (2k-1) f_c / f_{res} - f_{res} / \{ (2k-1) f_c \} \) \( (k = 1, 2, \ldots) \), is a factor describing the harmonic response of the resonator. In Figure 5.3, the driver stage is represented as \( N \) isolated inverter with the load capacitor \((C_{drv}/N)\). The power consumption of the driver stage can be calculated from

\[ P_{DRV}(n) = \frac{n}{N} \cdot C_{drv} \cdot V_{drv} \cdot f_c \]  

(5-6)

where \( V_{drv} \) is the supply voltage of the driver stage. The driver and final stage efficiency is obtained from

\[ \eta_{D+F} = \frac{P_{out}}{P_{DC}(P_{out}, n) + P_{DRV}(n)} \]  

(5-7)

In Eq. (5-7), \( P_{DC} \) is a function of \( P_{out} \) and \( n \), while \( P_{drv} \) is a function of only \( n \). At peak output power, \( n \) is set to be \( N \). With decreasing \( P_{out} \), \( P_{DC} \) is also decreased, where \( P_{drv} \) dominate \( \eta_{D+F} \). In this situation, by decreasing \( n \), \( P_{drv} \) can be reduced although \( P_{DC} \) is slightly increased. By making a balance between \( P_{DC} \) and \( P_{drv} \), \( \eta_{D+F} \) can be maximized.

**C. Simulated Results**

Theoretical limits of power dynamic range and driver and final stage efficiency are simulated, where 10 bit unit-cell architecture (7 bit unary-cell and 3 bit binary-cell) is
employed [19], [79]. For simplicity, it is assumed that $R_{metal}$ is 0 Ω and $Q_u$ is infinite. To confirm the validity of the calculation, simulation is also done using 0.15 μm CMOS technology, where ideal inductor and capacitor are used as the output resonator. Instead of the buck converter, voltage supply and buck converter inductor, $L_{env}$, are used, where the supply voltage is $D V_{dd}$. Parameters used for simulation are summarized in Table 5.1.

Table 5.1: Parameters of unit-cell switching digital polar transmitter.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty cycle ($D$)</td>
<td>1/64 - 1</td>
</tr>
<tr>
<td>BC supply voltage ($V_{dc}$)</td>
<td>3.3 V</td>
</tr>
<tr>
<td>FET on-resistance ($R_{on0}$)</td>
<td>0.39 Ω</td>
</tr>
<tr>
<td>Number of unit cells ($N$)</td>
<td>1023</td>
</tr>
<tr>
<td>Driver supply voltage ($V_{av}$)</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Driver load capacitance ($C_{drv}$)</td>
<td>80 pF</td>
</tr>
<tr>
<td>Metal resistance ($R_{metal}$)</td>
<td>0 Ω</td>
</tr>
<tr>
<td>Resonator unloaded Q ($Q_u$)</td>
<td>infinite</td>
</tr>
<tr>
<td>Carrier frequency ($f_c$)</td>
<td>1.65 GHz</td>
</tr>
<tr>
<td>Load resistance ($R_L$)</td>
<td>12.5 Ω</td>
</tr>
<tr>
<td>Resonant frequency ($f_{res}$)</td>
<td>1.65 GHz</td>
</tr>
<tr>
<td>Resonator Inductance ($L_{res}$)</td>
<td>0.5 nH</td>
</tr>
<tr>
<td>BC inductance ($L_{env}$)</td>
<td>100 nH</td>
</tr>
</tbody>
</table>

Figure 5.4 shows the calculated and simulated $P_{out}$ vs $D$ of the unit-cell switching CMCD PA. The curves are calculated using Eqs. (5-2)-(5-4) and the symbols are the simulated results, where $n = 1, 15, 127$ and 1023. From the results, $P_{out}$ is in the range from 35 dBm to -45 dBm, and the corresponding power dynamic range of 80 dB is achieved.

More insight of the relationship is analyzed. Figure 5.5 shows the calculated and simulated $P_{out}$ vs $I_{dd}$. The black curve is calculated using Eq. (5-2). From the results, it is confirmed that $P_{out}$ is almost independent of $n$. Simulated results are slightly lower than the theoretical curve because the output capacitance of the stacked FETs increases and $f_{res}$ is shifted in back-off.
Figure 5.4: Calculated and simulated output power vs equivalent duty cycle. (curves: Eqs. (5-2)-(5-4), symbols: simulation where \( n = 1, 15, 127 \) and 1023)

Figure 5.5: Calculated and simulated output power vs DC current. (black curve: Eq. (5-2), symbol: simulation where \( n = 1, 15, 127 \) and 1023)
Figure 5.6 shows the calculated and simulated $I_{dd}$ vs $D$ of the unit-cell switching CMCD PA. The theoretical curves are calculated using Eq. (5-3) and (5-4). The simulated $I_{dd}$ is in good agreement with the theoretical curve in the high duty-cycle region when $n$ is large, while in the low duty-cycle region when $n$ is small. When $n$ is large, $R_{PA}$ is dominated by the first term of Eq. (5-4). In this case, simulated $R_{PA}$ decreases from an ideal value in back-off due to shifting the resonant frequency, which causes the DC current error. When $n$ is small, $R_{PA}$ is dominated by the second term of Eq. (5-4). In this case, simulated $R_{PA}$ increases from an ideal value in high current region because the operation point of the stacked FET moves from triode region to saturation region.

Next, Figure 5.7 shows the calculated and simulated $\eta_{D+F}$ vs $P_{out}$. From the results, the optimal efficiency of each output power is higher than the curve proportional to square root of $P_{out}$ (ideal class-B curve) up to 45 dB back-off. When the operation point of the stacked FET is the saturation region (where $n$ is small and $D$ is high), the simulated $\eta_{D+F}$ is lower than the theoretical curve. It indicates the combination of DC current control and unit-cell switching is desirable to keep high efficiency in back-off because it is possible to maintain the operation point of the stacked FET to be the triode region.

Finally, Figure 5.8 shows the calculated and simulated $P_{DC} + P_{drv}$ vs $P_{out}$. From the results, when $P_{out}$ is lower than -20 dBm, $P_{DC} + P_{drv}$ is lower than 20 mW, which is comparable with DC power consumption of other circuit blocks.
Figure 5.6: Calculated and simulated DC current vs equivalent duty cycle. (curves: Eqs. (5-3) and (5-4), symbols: simulation where $n = 1, 15, 127$ and $1023$)

Figure 5.7: Calculated and simulated driver and final stage efficiency vs output power. (curves: Eq. (5-7), symbols: simulation where $n = 1, 15, 127$ and $1023$)
Figure 5.8: Calculated and simulated driver and final stage DC power consumption vs output power. (curves: sum of Eqs. (5-5) and (5-6), symbols: simulation where \( n = 1, 15, 127 \) and 1023)

5.2.2 Additional-state for Unit-cell Switching

A. Basic Concept

Increasing the number of bit (NOB) of DPWM signal is another choice to expand power dynamic range. Figure 5.9 shows the output power vs duty cycle when the NOB increases up to 10 bit. Even if precise control of buck converter is realized, the minimum output power is limited due to the feed-through. The output power can decreases up to -60 dBm and the maximum power dynamic range is 95 dB. As discussed in Chapter 1, the required total power dynamic range is 114 dB (modulation: 40dB, average power control: 74 dB). Therefore, additional 20 dB dynamic range is needed.
Figure 5.9: Power dynamic range when DPWM number of bit is increased. (curves: Eqs. (5-2) and (5-3), symbols: simulation where \( n = 1, 15, 127 \) and 1023)

Figure 5.10 shows a concept of a variable attenuator for power dynamic range extension. Shunt resistors are added at the output. By decreasing the resistance, the output power can be reduced. If the stacked FET of unit-cell is closed instead of open, it works as a shunt resistor due to the on-resistance. Since a part of the PA circuit block is used as the attenuator without additional components at the output, the degradation of the peak output power and efficiency can be neglected.

Figure 5.10: Concept of variable attenuator for power dynamic range extension.
\section*{B. Derivation of Output Power}

Figure 5.12 shows an equivalent circuit of three-state unit-cell switching CMCD PA, where no DC current is supplied. Here, only one unit-cell is switching alternatively ("state-1"), some unit-cells are constant open ("state-2"), and rest of them is constant closed ("state-3"). By contrast, the reported power amplifiers in [11], [19], [75], [79]-[82] have only state-1 and state-2. The FET switches are "closed", where they act as resistors, partially shunting the output signal to ground. Thus the output current can be attenuated and the dynamic range can be extended, in a manner controlled by the number of unit-cells in state-3 as shown in Figure 5.11.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure5.12}
\caption{Equivalent circuit of three-state unit-cell switching CMCD PA.}
\end{figure}
Figure 5.13 shows a simple equivalent half-circuit of the three-state unit-cell switching CMCD PA, where no DC current is supplied and the state of some unit-cells is state-3 (call “attenuation mode”). The left side drawn by gray lines indicates the active unit cell. A part of RF carrier signal delivered from the driver stage goes to the output through the parasitic capacitance between the input and output. In addition, the non-linear capacitance and resistance, whose values are changed alternatively by the input voltage, generates small voltage fluctuation. Although the leakage and fluctuation are the feed-through, the current is expressed as $i_{FT}$, which is less sensitive for the resistance of the right side because the output impedance of the left side is very high.

![Figure 5.13: Simple equivalent half-circuit of three-state unit-cell switching CMCD PA in attenuation mode.](image)

The half output voltage can be calculated as

$$
\frac{v_L}{2} = N \frac{R_{on0}}{m} \left( 1 - \frac{Q_u}{Q_L} \right) \frac{R_L}{2} \cdot i_{FT}
$$

$$
\frac{v_L}{2} = \frac{N}{m} \frac{R_{on0}}{R_{on0} + \left( 1 - \frac{Q_u}{Q_L} \right) \frac{R_L}{2}} \cdot i_{FT}
$$

(5-8)
where \( m \) is the number of state-3 unit-cell. From the output voltage of the half-side circuit, the total output power can be calculated from

\[
P_{\text{out}}(m) = \frac{v_L^2}{R_L/2} = \left( \frac{N}{m} \frac{R_{\text{on0}}}{m} + \left( 1 - \frac{Q_L}{Q_u} \right) \frac{R_L}{2} \right)^2 \cdot \left( 1 - \frac{Q_L}{Q_u} \right)^2 \cdot \frac{R_L}{2} \cdot i_{FF}^2
\]

\[
= \left( \frac{N}{m} \right)^2 \cdot \frac{R_{\text{on0}}}{m} + \left( 1 - \frac{Q_L}{Q_u} \right) \frac{R_L}{2} \right)^2 \cdot P_{\text{out}}(N)
\]

\( (5-9) \)

C. Simulated Results

Figure 5.14 shows the calculated and simulated output power vs number of state-3 unit-cells. The black curve is calculated using Eq. (5-9) where \( P_{\text{out}}(N) = -79 \) dBm. The symbols are simulated results. From the results, the theoretical slope of the output power is almost same as the simulation when the large number of unit-cells is state-3. The theoretical power dynamic range is extended by approximately 25 dB and the simulated power dynamic range also increases by more than 21 dB. With decreasing the number of state-3 unit-cells, there is a discrepancy between theory and simulation. One of the possible reasons of the difference is the resonance frequency shift due to the parasitic capacitance of the state-2 unit-cells with no DC supply. With increasing the number of state-3 unit-cells, decreasing the parasitic capacitance results in approaching the simulated results to theoretical curve.
Figure 5.14: Calculated and simulated output power vs number of constant closed unit-cells. \((N = 1023, R_{on0} = 0.39 \, \Omega, R_L = 12.5 \, \Omega, Q_c = 0.21, Q_u = \text{inf}, P_{out}(N) = -79 \, \text{dBm}, f_c = 0.85 \, \text{GHz}, V_{drv} = 1.8 \, \text{V}, V_{g2} = 2.8 \, \text{V})\)

5.3 Circuit Design of Buck Converter

5.3.1 Unit-cell Switching Technique

In this section, the efficiency improvement of the buck converter in back-off is discussed. One of simple ideas is a unit-cell control technique which has been applied to the CMCD PA. Using the technique, the DC power consumption of the driver stage supposed to be reduced although the output capacitance loss remains.

Figure 5.15 shows a block diagram of a unit-cell switching buck converter. Driver and final stages are partitioned into \(L\) unit cells, where \(l\) unit cells are switching and \(L-l\) unit cells are constant open. Digital pulse width modulated voltage with a dead time is provided to the unit-cell selectors and enable voltages are applied to the active unit cells. The DC current \((I_{out})\) is supplied to the CMCD PA, whose input impedance is \(R_{PA}\), through the envelop inductor \((L_{env})\).
In this system, there are many controllable parameters, i.e., duty cycle \((D)\) the number of active buck converter unit cells \((l)\), and \(R_{PA}\) which is the function of the number of active PA unit cells \((n)\). To evaluate the regulator efficiency in back-off, the combination of \(n\) and \(I_{out}\) is constrained for simplicity. Figure 5.16 shows the constrained \(I_{out}\) vs \(n\). The switching frequency, \(f_{sw}\), of the DPWM signal is 46 MHz. The dead times at the rising and falling edges \((T_{d,r} \text{ and } T_{d,f})\) are 90 psec and 150 psec respectively, where these dead times are optimized for the peak efficiency. The supply voltage \((V_{dd})\) is 3.6 V and \(L\) is 1024. At first, when \(l = 1024\), simulated \(I_{out}\)s are on the black solid curve, where \(D = 3.125\%\) fixed. Next, when \(l = 1, 16\) and 128, simulated \(I_{out}\)s are also on the black solid curve, but \(D\) is adjusted every time \(n\) is changed.
Figure 5.16: Constraint of $I_{out}$ vs $n$ of unit-cell switching buck converter. ($f_{sw} = 46$ MHz, $V_{dd} = 3.6$ V)

Figure 5.17 shows the simulated DC power dissipation in the buck converter ($P_{\text{reg}}$) vs $I_{out}$. $P_{\text{reg}}$ is defined as “input DC power minus output DC power” of the buck converter. With decreasing $l$, $P_{\text{reg}}$ decrease from 97 mW to 44 mW (55%) at $I_{out} = 40$ mA, and from 97 mW to 3 mW (97%) at $I_{out} = 0.3$ mA.

Figure 5.17: Simulated $P_{\text{reg}}$ vs $I_{out}$ of unit-cell switching buck converter. ($f_{sw} = 46$ MHz, $V_{dd} = 3.6$ V)
Actually, simulated $P_{\text{reg}}$s in Figure 5.17 are much lower than expected. Ideally, $P_{\text{reg}}$ should be higher than the output capacitance loss ($C_d V_{dd} f_{sw}$) which is approximately 40 mW (where the output capacitance ($C_d$) is 65 pF). To study the reason, the drain voltage waveforms of the buck converter are compared between $l = 1024$ and 16 as shown in Figure 5.18 (where $D = 3.125 \%$ and 6.25%, respectively, $I_{out} = 4.5$ mA and $n = 16$). When $l = 1024$, the peak-to-peak voltage is 3.6 V$_{\text{p-p}}$ as expected. On the other hand, when $l = 16$, the peak-to-peak voltage decreases, which results in smaller output capacitance loss. The waveform indicates that there is a possibility to reduce $P_{\text{reg}}$ more using this phenomenon. In the next section, a smarter controlling algorithm of a buck converter will be discussed.

Figure 5.18: Simulated drain voltage waveform of unit-cell switching buck converter when $l =$ (a) 1024 and (b) 16, where $D = 3.125 \% / 6.25 \%, f_{sw} = 46$ MHz, $V_{dd} = 3.6$ V, $I_{out} = 4.5$ mA, and $n = 16$. 
5.3.2 Charge Sampling Operation

**A. Basic Concept**

If it is possible to control amount of charge stored in the output capacitor of the buck converter and deliver all stored charge to the PA, the DC power dissipation in the buck converter is significantly reduced. To realize the function, a new digital control technique is introduced like a “charge-sampling” switched capacitor [90].

Figure 5.19 shows the equivalent circuit and output voltage waveform of the buck converter in charge-sampling (CS) mode. The supply current to the PA is determined by the amount of charge stored in parasitic capacitance $C_d$ during a period. By increasing the equivalent on-resistance of the high-side switch, the output voltage no longer can reach $V_{dd}$. Subsequently, during a relatively long dead time at falling edge, the stored charge flows to the PA. After the drain voltage is small enough, the low-side turns on and current flows from GND as needed. Overall efficiency is improved because the output capacitance loss is ideally zero (although the conductive loss increases). The high-side on-resistance is changed by controlling the number of the active unit-cells. Low-side unit cell control is also needed to achieve a proper balance between the conductive loss and the loss due to the charge injection of the NMOS switches.

**B. Derivation of DC Output Current**

Figure 5.20 shows ideal operations of charge sampling techniques, where a charge is provided form (a) variable current source (original charge sampling for A/D converter [90]) and (b) constant voltage source with variable series resistor (proposal for DC regulator).
Figure 5.19: New operation of buck converter: charge sampling mode.

Figure 5.20: Ideal operation of charge sampling technique, where charge is provided form (a) variable current source (original charge sampling for A/D converter) and (b) constant voltage source with variable series resistor (proposal for DC regulator).
In Figure 5.20 (a), a sample hold circuit captures amount of current from a variable current source with the current of $I_{in}$. It is assumed that the $R_{onP}$ is large enough. If the variation of $I_{in}$ is small enough in the period of sampling, the charge stored at $C_d$ in the charging period can be expressed as

$$Q(t) \approx \int_{0}^{t} I_{in} \cdot dt = I_{in} \cdot t$$

(5-10)

The average output current can be calculated from

$$V_{out} \approx C_d \cdot Q(t = D/ f_{sw}) = \frac{C_d \cdot D}{f_{sw}} \cdot I_{in}$$

(5-11)

If $D$ is constant, the output voltage is proportional to the input current.

In Figure 5.20 (b), the mechanism of the charge sampling is applied into the DC regulator. From Thevenin-Norton’s theorem, the parallel connection of the current source and resistor can be converted to the series connection of the voltage source and resistor. If the circuit topology of the buck converter is applied, $V_{dd}$ needs to be constant, but the $R_{onP}$ can be changed using the high-side unit-cell switching. In this case, $Q$ is calculated from

$$Q(t) \approx \int_{0}^{t} \frac{V_{dd} - Q(t)/C_d}{R_{onP}} \cdot dt$$

$$\therefore Q(t) = C_d \cdot V_{dd} \left\{ 1 - \exp\left(\frac{t}{R_{onP}C_d}\right) \right\} \approx \frac{V_{dd} \cdot t}{R_{onP}}$$

(5-12)
where it is assumed that $Q(0) = 0$ and the output current is small enough. The current instead of the voltage is delivered from the proposed circuit, which is obtained from

$$I_{out} = Q(t = \frac{D}{f_{sw}}) \cdot f_{sw} = \frac{V_{dd} \cdot D \cdot f_{sw}}{R_{onP}}$$

(5-13)

From the results, you can see the output current is approximately inversely proportional to $R_{onP}$ in the ideal condition.

**C. Simulated Results**

Figure 5.21 shows the simulated $P_{reg}$ vs $I_{out}$ of the charge-sampling buck converter, where the simulated results of the unit-cell switching buck converter are shown for comparison. The same constraint of $I_{out}$ vs $n$ is applied as shown in Figure 5.16. The duty cycle of the input pulse in the charge-sampling mode is 1.5625% (1/64). The dead time at the falling edge ($T_{d_f}$) is optimized to minimize $P_{reg}$. In addition, the size of the low-side FET is optimized to make a balance between the effects of charge injection and on resistance. From the results, $P_{reg}$ decreases from 44 mW to 24 mW (45%) at $I_{out} = 40$ mA, and from 3 mW to 1.5 mW (50%) at $I_{out} = 0.3$ mA.

Figure 5.22 shows optimal $T_{d_f}$ vs $n$ of the charge-sampling buck converter. The optimal $T_{d_f}$s are in the range from 2.5 nsec to 20 nsec, which is relatively long. When the function of the charge sampling is implemented, the delay elements may occupy large area. Therefore, for the demonstration, we decided to use the dead time of 1.5 nsec constant, where it is confirmed that degradation of $P_{reg}$ is small enough even if $T_{d_f} = 1.5$ nsec.
Figure 5.21: Simulated $P_{\text{reg}}$ vs $I_{\text{out}}$ in charge sampling mode and unit-cell switching mode, where $f_{sw} = 46$ MHz and $V_{dd} = 3.6$ V.

Figure 5.22: Optimal $T_{d,f}$ vs $n$ of charge-sampling buck converter.
5.4 Chip and Board Fabrication

5.4.1 2nd Generation CMCD PA

A. Block Diagram

Figure 5.23 shows the block diagram of the 2nd generation CMCD PA. If the PA is portioned into 1023 unit-cells to realize 10 bit control, the numerous control lines occupy large area. Therefore, binary unit cells are used for 3 LSB, while unary cells are used for 7 MSB to achieve better DNL and INL. 3 bit digital input (B1~3) control the state of the binary unit-cells, and 7 bits of remained 10 bits (B4~10) are used to choose the state of the unary unit-cells, where a binary-to-thermometer decoder, which consists of 3 bit and 4 bit recursive decoders and 7 bit matrix decoder [93], is employed. At first, the digital inputs (B1~10) are registered to the latch, and delivered ENABLE signals (EN1~127, EN1/2, EN1/4, EN1/8) are also synchronized by the latch using external clock. All unit cells except 1/8 unit cell have three operation states, where one more control line is used to change from state1-to-2 to state2-to-3. The envelope modulated current from the buck converter is multiplied with the PM RF carrier in the unit amplifiers. Finally, the RF modulated signal is delivered through the on-chip variable resonator for multiband operation (See Chapter 4).
Figure 5.24 shows the block diagram of the buffered synchronized delay block. It consists of the 8-stage inverter. The delay time of the former 4-stage is approximately same as the delay time of the recursive decoder. The delay time of the latter 4-stage is approximately same as the delay of the matrix decoder.
C. 7bit Binary-to-Thermometer Decoder

To realize a binary-to-thermometer decoder with small number of bits, it is easy to use the recursive way. 3 bit recursive decoder is expressed as

\[(C_1, C_2, C_3) = BTD_2(B_4, B_5) \ OR \ B_6\]

\[(5-14)\]

\[C_4 = B_6\]

\[(5-15)\]

\[(C_5, C_6, C_7) = BTD_2(B_4, B_5) \ AND \ B_6\]

\[(5-16)\]

where \(BTD_2(B_4, B_5)\) is the 2 bit decoding function. Similarly, 4 bit recursive decoder is written as

\[(R_1 \sim R_6) = BTD_3(B_7 \sim B_9) \ OR \ B_{10}\]

\[(5-17)\]

\[R_7 = B_{10}\]

\[(5-18)\]

\[(R_8 \sim R_{15}) = BTD_3(B_7 \sim B_9) \ AND \ B_{10}\]

\[(5-19)\]
where $BTD_3(B7\sim B9)$ is the 3 bit decoding function.

Figure 5.25 (a) shows the 3 bit recursive decoder, which is flattened from Eqs. (5-17)-(5-19) to reduce the delay. At the output of C4, two inverters are inserted before the buffer to have approximately same delay with other outputs. Similarly, Figure 5.25 (b) shows 4 bit recursive decoder, which is flattened from Eqs. (5-17)-(5-19).

Figure 5.25: (a) 3 bit and (b) 4 bit recursive decoders.
Figure 5.26 shows the block diagram of the matrix decoder to simplify the design of large decoder. The least-significant and most-significant thermometer words (C1~C7 and R1~R15) are provided from two small decoders. In each cell, ENABLE signal is given by the following function:

$$EN = nextROW \lor (COL \land ROW)$$

(5-20)

The design is completed by imposing that the first row is always on, and that the last row and column are always off.

Figure 5.26: 7 bit binary-to-thermometer matrix decoder.
**D. 3-state Unit-cell Amplifier**

Figure 5.27 shows a block diagram of a PA unit-cell. Each final stage FET in the PA unit-cell can be operated in three states. The 3 states are controlled by two digital inputs, A and B. Both A and B are high in state-1. A is low and B doesn't care in state-2. A is high and B is low in state-3. When the required output power decreases from peak, all unit-cell’s Bs are high and As change from high to low in order. Once all Bs except one small unit-cell are low, As of these unit-cells turn to be low. To attenuate the output power, Bs are set to be high in order.

![Diagram of PA unit-cell and its 3-state operation](image)

Figure 5.27: Configuration of PA unit-cell and its 3-state operation.

**E. On-chip Differential Line**

In the 1.5th generation CMCD PA, the space between the output metal lines was 5 μm to minimize parasitic inductance for the differential signal. However, with approaching two lines, parasitic resistance for the differential signal increases due to the
proximity effect. For the 2nd generation CMCD PA, the line space is re-designed using EM simulated results.

Figure 5.28 shows the layout of the differential output metal line for the EM simulation, where 2 input ports and 2 output ports are placed. 6 μm Aluminium layer is employed and the line length is 1350 um. The total line width is 55 um and the space between two lines is changed in the range from 5 um to 25 um. From simulated mixed-mode S-parameters [95], differential-mode Y-parameters are calculated and differential series resistances ($R_{ds}$) are obtained from

$$R_{ds} = \text{Re}(-1/Y_{dd21})$$

(5-21)

![Figure 5.28: Layout of differential output metal line for EM simulation.](image)

Figure 5.29 shows the simulated $R_{ds}$ over frequency, where $S = 5$μm, 15 μm and 25 μm. When $S = 5$ μm, $R_{ds}$ is small in the low frequency, but rapidly increases in the RF frequency. When $S = 15$ μm, $R_{ds}$ is the smallest in the RF frequency. From the results, $S$ is changed to be 15 μm for the 2nd generation CMCD PA.
Figure 5.29: Simulated differential series resistances over frequency, where \( S = 5 \, \mu m, 15 \, \mu m \) and \( 25 \, \mu m \).

**F. Fabricated Chip**

Figure 5.30 shows the die photo of 2nd generation CMCD PA using L-foundry 0.15 \( \mu m \) CMOS process containing 6 \( \mu m \) thick Al metal layers. The die sizes are \( 2.55 \times 1.54 \, mm^2 \). To prevent digital noise to analog block, the digital and analog power supplies and grounds are separated [94].

Figure 5.30: Die photo of 2nd generation CMCD PA \((2.55 \times 1.54 \, mm^2)\).
5.4.2 2nd Generation Buck Converter

A. Block Diagram

Figure 5.31 (a) shows the block diagram of the 2nd generation buck converter, where DPWM signal is applied to buck converter unit-cells through variable dead-time generator, level shifter and driver stage. The envelope current is delivered from the unit-cells to the CMCD PA through the envelope inductor. Similarly to the 2nd generation CMCD PA, where the buck converter is segmented into 3LSB binary and 7MSB unary unit cells. For charge-sampling mode, the state of the high-side and low-side switches in each unit cell needs to be controlled independently, where available states are switching and constant open. The number of digital control bits for high-side and low-side unit cells is 5 bits each due to limited number of pads for the digital control (although it is possible to design the circuit more flexibly when all DSP circuits are integrated into die). Therefore, the mapping between decoder outputs and controlled unit-cells is changed as shown in Figure 5.31 (b), where unit-cells are coarsely selected when the number of active unit cells is many. With decreasing the number of active unit-cells, fine tuning is available. For variable dead time generator, two more digital bits are assigned.
Figure 5.31: (a) Block diagram of 2nd generation buck converter and (b) unit-cell control map using 5 bit digital input.


**B. Variable Dead-time Generator**

Figure 5.32 shows the voltage waveforms required for the charge-sampling mode and delivered from conventional dead-time generators [96], [97]. Short pulse width signal (first waveform) and dead time longer than the pulse width are used for the charge-sampling mode. In this case, required high-side and low-side gate voltages become like the second and third waveforms. Now we focus on how to generate the third waveform. Conventional dead-time generators use the delayed input signal (forth waveform) and AND gate for low-side control signal. If the dead time is longer than twice of the input pulse width, the waveform is degraded like the fifth waveform. In order to generate required voltage waveform, a new dead-time generator is needed.

![Diagram of voltage waveforms and gate voltages](image)

Figure 5.32: Voltage waveforms required for charge-sampling mode and delivered from conventional dead-time generators.

Figure 5.33 shows (a) the block diagram of the proposed pulse-edge-switching variable dead-time generator and (b) the circuit schematic of the negative edge D-flip
flop with reset. The negative edge D-flip flop with reset provides low voltage at the falling edge of the reset and high voltage at the rising edge of the clock. By applying the inverted input pulse to the reset and the delayed pulse to the clock, the required low-side gate voltage can be generated.

Figure 5.33: (a) Block diagram of pulse-edge-switching variable dead-time generator and (b) circuit schematic of negative edge D-flip flop with reset.

Figure 5.34 shows (a) the 2 bit recursive decoder to select the dead time. The output is expressed as
\[ DT_1 = BDT_1 \text{ OR } BDT_2 \]  

(5-22)

\[ DT_2 = BDT_2 \]  

(5-23)

\[ DT_3 = BDT_1 \text{ AND } BDT_2 \]  

(5-24)

Figure 5.34 (b) shows the chart between the decoder output and dead time. The dead time changes from 0.15 nsec to 1.5 nsec. By taken into account the effect of parasitic components and process variation, several dead times can be selected.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|}
\hline
DT1 & DT2 & DT3 & Dead time \\
\hline
High & High & High & 0.15 ns \\
High & High & Low & 0.30 ns \\
High & Low & Low & 0.75 ns \\
Low & Low & Low & 1.50 ns \\
\hline
\end{tabular}
\caption{Dead time chart for decoder outputs.}
\end{table}

\[ \begin{align*}
\text{Figure 5.34: } & (a) \text{ 2 bit recursive decoder and (b) chart between decoder output and dead time.} \\
\end{align*} \]

C. 5 bit Binary-to-Thermometer Decoder

Figure 5.35 shows the block diagram of the 5 bit matrix decoder. The basic configuration is same as the matrix decoder for the 2nd generation CMCD PA. C1~C3 and R1~R7 are generated from the 2 bit and 3 bit recursive decoders, respectively.
Figure 5.35: Block diagram of 5 bit matrix decoder.

**D. 4-state Unit-cell Amplifier**

Figure 5.36 shows the configuration of the buck converter unit cell. Each high-side and low-side switches in a buck converter can operate in four states: 1) normal switching, 2) low-side switching, 3) high-side switching and 4) constant open. The 4 states are also controlled by two digital inputs, C. and D. In state-1 (both C and D high), the final stage is driven by DPWM signal and other states are used to control the on-resistance of the high-side switch and relax the charge injection of the low-side switch for charge-sampling mode.
Figure 5.36: Configuration of buck converter unit-cell and its 4-state operation.

**E. Fabricated Chip**

Figure 5.37 shows the die photo of 2nd generation buck converter, which is also fabricated using 0.15 μm CMOS process. It should be easy to integrated both PA and buck converter into one die in the future. The die sizes are 1.39 × 1.38 mm². Since all circuit blocks can be seen as digital circuit, all grounds are connected with each other and 1.8 V power supply is shared between dead time generator and decoder.
5.4.3 2nd Generation PCB (2)

Figure 5.38 shows the block diagram of the 2nd generation PCB. To control resonance frequency of variable resonator, state of unit-cells and dead time of variable dead-time generator, 16 bit digital inputs for CMCD PA and 12 bit digital inputs for buck converter are applied from data pods of pulse pattern generator. Since the high-state of the data pod is 3.3 V, level shift circuits, consisting of resistive divider, are inserted for 1.8 V digital inputs.

Figure 5.39 shows the photo of the final version PCB for 2nd generation digital polar transmitter, where analog and digital grounds are combined to obtain. The size of the board is 2.5 inch \( \times \) 4 inch (63 mm \( \times \) 100 mm). A cross-talk between analog and digital signals, such as interference due to digital noise, should be small by preventing a cross-section between analog and digital signal lines [98].
Figure 5.38: Block diagram of 2nd generation PCB.

Figure 5.39: Photo of fabricated PCB for 2nd generation digital polar transmitter.
5.5 Experimental Results

5.5.1 2nd Generation Digital Polar Transmitter (Single-tone 2)

A. State-1 to State-2

Figure 5.40 shows the output power, $P_{\text{out}}$, vs the duty cycle, $D$, of the 2nd generation digital polar transmitter at (a) 0.85 GHz and (b) 1.75 GHz when all band-switching capacitors are closed and open, respectively. The PA unit cells change from state-1 (active) to -2 (constant open), where $n$ is the number of state-1 unit cells. The state of all buck converter unit cells is state-1 (both high-side and low-side active). The supply voltage of the buck converter, $V_{\text{dd}}$, is 3.6 V, the DPWM switching frequency, $f_{\text{sw}}$, is 47 MHz, the PA driver supply voltage, $V_{\text{drv}}$, is 1.8 V, the input power of the PM signal, $P_{\text{in}}$, is 10 / 11 dBm, and the 2nd gate voltage of the final stage, $V_{\text{g2}}$, is 2.8 / 2.9 V. A power dynamic range of 82 dB (-54~28 dBm) and 78 dB (-49~29 dBm) are achieved in the low and high bands, respectively. It is noted that most part of the output power at $D = 1.5625 \% (= 1/64)$ is feed-through and it is difficult to reduce the power less than the value using the DC current control.

Calculated output powers using Eqs. (3-7), (3-25) and (3-33) are compared with the measured results as shown in Figure 5.41, where $Q_a = 9.8 / 8.1$, $Q_L = 3.2 / 2.2$, $R_L = 12.5 / 17 \, \Omega$, and $R_{\text{BC}} = 0.3 \, \Omega$ at 0.85 GHz / 1.75 GHz, respectively. The series resistances of the stacked FET ($R_{\text{SW}}$) are obtained from measured results. The simulated losses of the on-chip balun are 2.8 dB and 1.4 dB, respectively. From the results, the output power is well estimated at 0.85 GHz, while there are some discrepancies at 1.75 GHz, where the loss due to interconnects and pads may causes the error.
Figure 5.40: Measured output power vs duty cycle from state-1 to -2 at (a) $f_c = 0.85$ GHz and (b) $f_c = 1.75$ GHz. ($V_{dd} = 3.6$ V, $f_{sw} = 47$ MHz, $V_{drv} = 1.8$ V, $P_{in} = 10 / 11$ dBm, $V_{g2} = 2.8 / 2.9$ V)
Figure 5.41: Comparison between measured and calculated output power from state-1 to state-2 at (a) $f_c = 0.85 \text{ GHz}$ and (b) $f_c = 1.75 \text{ GHz}$. ($V_{dd} = 3.6 \text{ V}, f_{sw} = 47 \text{ MHz}, V_{drv} = 1.8 \text{ V}, P_{in} = 10 / 11 \text{ dBm}, V_{g2} = 2.8 / 2.9 \text{ V}$)
Figure 5.42 shows the overall efficiency vs $P_{out}$ at (a) 0.85 GHz and (b) 1.75 GHz. Here, $D$ is higher than 3.125 % ($= 2/64$) not to take the effect of the feed-through into account. The overall efficiencies are higher than an ideal class-A curve in all output power ranges and higher than an ideal class-B curve in the range higher than -5 dBm and 3 dBm, respectively. The corresponding back-offs are 33 dB and 26 dB. The proposed transmitter maintains high efficiency over significantly large dynamic range.

One of curious topics of the proposed architecture is which is better for the efficiency to change the output power using “DC current control” and “unit-cell switching”. The overall efficiencies are compared in Figure 5.43, where the carrier frequencies are (a) 0.85 GHz and (b) 1.75 GHz. $n$ for the DC current control and $D$ for the unit-cell switching are selected as both peak overall efficiencies are similar. In relatively high output power region, the DC current control is better to achieve higher efficiency, while the unit-cell switching is superior in lower output power region.

Figure 5.45 shows the measured total DC power consumption vs $P_{out}$ at (a) 0.85 GHz and (b) 1.75 GHz. $D$ is also higher than 3.125 %. The minimum DC power consumptions are approximately 85 mW and 97 mW, which are almost dominated by the buck converter power consumption (approximately 73 mW). In the high output power region, the DC power consumption of the final stage almost decides the total power. When $n$ is large, the total DC power is saturated in back-off due to the driver stage output power. When $n$ is small, the total DC power increases in relatively high output region because the stacked FETs enter into the saturation. The quiescent power consumption of 100 mW is comparable to a traditional linear PA [19]. So it is important to reduce the DC power consumption of the buck converter in deep back-off.
Figure 5.42: Measured overall efficiency vs output power from state-1 to -2 at (a) $f_c = 0.85$ GHz and (b) $f_c = 1.75$ GHz. ($V_{dd} = 3.6$ V, $f_{sw} = 47$ MHz, $V_{drv} = 1.8$ V, $P_{in} = 10 / 11$ dBm, $V_{g2} = 2.8 / 2.9$ V)
Figure 5.43: Efficiency comparison between DC current control and unit-cell switching at (a) $f_c = 0.85$ GHz and (b) $f_c = 1.75$ GHz. ($V_{dd} = 3.6$ V, $f_{sw} = 47$ MHz, $V_{drv} = 1.8$ V, $P_{in} = 10 / 11$ dBm, $V_{g2} = 2.8 / 2.9$ V)
Figure 5.44: Measured total DC power consumption vs output power from state-1 to -2 at (a) $f_c = 0.85 \text{ GHz}$ and (b) $f_c = 1.75 \text{ GHz}$. ($V_{dd} = 3.6 \text{ V}, f_{sw} = 47 \text{ MHz}, V_{drv} = 1.8 \text{ V}, P_{in} = 10 / 11 \text{ dBm}, V_{g2} = 2.8 / 2.9 \text{ V}$)
**B. State-2 to State-3**

Figure 5.45 shows the measured (a) output power and (b) total DC power consumption when the PA unit-cells change from state-2 to state-3. Only one PA unit cell are switching although the buck converter does not work anymore. The simulated results are normalized to the measured powers when no unit-cell is state-3. With increasing number of state-3 PA unit-cells, $l$, the power dynamic ranges are extended by 9 / 7 dB to 91 / 85 dB at 0.85 GHz and 1.75 GHz. The measured dynamic ranges improvement is somewhat lower than predicted by simulation, due to low input-output isolation of the PA chip and PCB. In this mode, the total DC power consumption is less than 1 mW since no DC power is consumed in the buck converter. The DC power consumption of the selector in the PA unit-cell is also decreased. The DC power is very small compared with the reported value [19].

![Figure 5.45: Measured (a) output power and (b) total DC power consumption vs number of state-3 PA unit-cells at 0.85 GHz and 1.75 GHz. ($n = 1, V_{drv} = 1.8 \text{ V}, P_{in} = 10 / 11 \text{ dBm}, V_{g2} = 2.8 / 2.9 \text{ V}$)](image-url)
Figure 5.46 shows the output power vs $I$ at (a) 0.85 GHz and (b) 1.75 GHz, where $n = 0$ to evaluate the isolation between input and output. The gray solid curves are measured results and the black broken curves are the output power when $n = 1$ for confirmation. It is supposed that the output power with $n = 0$ is much smaller than $n = 1$. However, actually both results are almost same, which is one of the reasons why the dynamic range improvement of the proposed technique is smaller than the simulation. The possible reasons of the isolation degradation are the coupling of interconnects in the chip, the leakage through Si substrate, and the leakage through the ground of the PCB. By adding more buffer amplifier to isolate the input and output, and integrated the phase modulator into the chip, the leakage should be improved.

![Graph](a)

![Graph](b)

Figure 5.46: Isolation between input and output at (a) $f_c = 0.85$ GHz and (b) $f_c = 1.75$ GHz.

### 5.5.2 2nd Generation Digital Polar Transmitter (Single-tone 3)

**A. Charge Sampling Mode**

In order to reduce the total DC power consumption of the buck converter when the state of the CMCD PA is from state-1 to state-2, the charge-sampling mode is applied.
Figure 5.47 shows the measured total DC power consumption vs $P_{out}$ at 1.75 GHz, where the DC current of the charge-sampling mode is constrained to be that of the DPWM mode with $D = 3.125 \%$, as explained in Section 5.3.2. From the results, the minimum total DC power consumption is reduced to be a factor of 0.7 (67 mW).

![Figure 5.47: Measured total DC power consumption vs output power when charge-sampling mode is applied to buck converter. ($f_c = 1.75$ GHz, $V_{dd} = 3.6$ V, $f_{sw} = 46.875$ MHz, $V_{drv} = 1.8$ V, $P_{in} = 10 / 11$ dBm, $V_{g2} = 2.8 / 2.9$ V)](image)

5.6 Summary

In this paper, a wide power dynamic range polar modulation transmitter has been demonstrated. By using a novel attenuation mode for the basic unit amplifier cells, 91 dB and 85 dB CW power dynamic range is demonstrated and the measured total DC power consumption less than 1 mW is achieved in the range from -65 dBm to -50 dBm. In addition, by applying charge-sampling operation in the buck converter, the measured overall DC power in the range from -40 dBm to -10 dBm is reduced by a factor of approximately 0.7.
The measured dynamic ranges improvement is somewhat lower than predicted by simulation, due to low input-output isolation of the PA chip and PCB. The isolation should be improved by designing the layout carefully and integrating the PM signal generator into the chip.

5.7 Acknowledgements

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Chapter 6

Wideband Digital Envelope Modulation Processing

6.1 Introduction

Polar transmitters using switching-mode envelope modulators suffer from a trade-off between artifacts from the use of purely digital envelope input signals and non-linearity due to the limited bandwidth of the AM path. In the reported papers [13], [33], [99] and [100], the switching frequency is set to be high enough for the signal bandwidth, and the cut-off frequency of the envelope reconstruction filter is designed to be between them. However, recent wireless standards require a significantly wide signal bandwidth, while the maximum switching frequency of the regulator is limited due to the minimum rising / falling times and expected efficiency.

We succeed to relax the trade-off by applying the pre-emphasis algorithm to the digital signal processing. The basic idea of the proposed algorithm has been reported in Dr. J. Rode’s dissertation [28]. In this work, the algorithm is expanded and the new algorithm is demonstrated using the fabricated digital polar transmitters described in Chapters 3, 4 and 5.
Even if the output filter of the envelope modulator can be designed aggressively using a pre-emphasis algorithm, the presence of clock images associated with the digital envelope input still remains [101], [102]. Many techniques to avoid clock images have been reported. In [103], phase chopping is applied for a spur-free output. However, this technique is only useful for a constant envelope signal like GSM. In [104], an auxiliary branch of an envelope modulator, which works with the opposite phase of the main branch, is connected in parallel to cancel the ripple of output signal. However, two large output inductors are needed. In [33] and [105], ΔΣ and Δ modulations and random carrier frequency modulation (RCFM) are applied to decrease peak out-of-band spurs. However, in order to meet ACLR specifications, ΔΣ modulation requires high average frequency, which causes large DC power consumption. Δ modulation needs an analog feedback circuit, which limits maximum bandwidth. RCFM increases the noise floor coming from quantization noise. Other dithering techniques like random pulse position modulation and random pulse width modulation [106] also have a similar trend.

In this work, a new dithered DPWM technique is compared with the normal DPWM and 1 bit ΔΣ modulation, and demonstrated to reduce clock images and quantization noise using the fabricated digital polar transmitter.

This chapter begins with design of the proposed digital polar modulation algorithm including a signal pre-emphasis for envelope inductor and time quantization. Next, a novel dithering algorithm is explained to reduce the peak spurious products. After that, measurement setups to emulate the proposed modulators and experimental results are described.
6.2 Design of Digital Polar Modulator

6.2.1 Average Output Power vs Mean Square Duty Cycle

Before discussing algorithms for the digital signal processing of the envelope modulation, the relationship between the duty cycle of the DPWM signal and the RF analog output power will be represented, where the DPWM signal is expressed as a sequence of zero and one and the duty cycle is defined as the percentage of the one in a certain period. The RF analog output power is calculated using the RF output voltage and load resistance. In case the envelope of the RF analog signal is modulated, variation in the duty cycle is calculated from an IQ digital input as mentioned in the following section, and the mean square duty cycle needs to be scaled by the average output power.

Figure 6.1 shows the simple circuit schematic of the digital polar transmitter. DSP provides a sequence consisting of zero and one, which is converted to the pulse voltage waveform ($V_{pw}$). $V_{pw}$ delivered from the inverter stage of the buck converter is transformed smooth current ($I_{dd}$), by the output inductor. $I_{dd}$ and the phase modulated RF carrier voltage are multiplied in the CMCD PA and the desired RF modulated signal is generated.
Figure 6.1: Simple circuit schematic of proposed digital polar transmitter.

From Eq. (3-16), $V_{pw}$ can be written as

$$V_{pw}(t) \equiv D(t_n) \cdot V_{dd}$$

(6-1)

where $f_{sw}$ is the switching frequency, $V_{dd}$ is the supply voltage of the buck converter and it is assumed that the harmonics of the DPWM signal can be neglect. From Eqs. (5-3) and (5-4), $I_{dd}$ can be simplified as

$$I_{dd}(t) = \frac{V_{pw}(t)}{2R_L \cdot \frac{1}{\pi^2} \left(1 - \frac{Q_L}{Q_u}\right) + R_{SW} + R_{BC}}$$

(6-2)

where $Q_L$ and $Q_u$ is the loaded and unloaded quality factors of the resonator of the CMCD PA, $R_{SW}$ is the parasitic resistance of the CMCD PA and $R_{BC}$ is the parasitic resistance of
the buck converter. From Eq. (5-2), the instantaneous output power can be calculated from

\[ P_{ou}(t) = \frac{2R_L I_{dd}^2(t)}{\pi^2} \left(1 - \frac{Q_L}{Q_u}\right)^2 \]

(6-3)

where it is assumed that the carrier frequency \( f_c \) is equal to the resonance frequency of the output resonator \( f_{res} \). From Eqs. (6-1)-(6-3), the average output power can be obtained from

\[ P_{ou}(t) = \frac{2R_L I_{dd}^2(t)}{\pi^2} \left(1 - \frac{Q_L}{Q_u}\right)^2 V_{dd}^2 \cdot D^2(t_n) \]

\[ \left\{ \frac{2R_L}{\pi^2} \cdot \left(1 - \frac{Q_L}{Q_u}\right) + R_{SW} + R_{RC} \right\} \]

(6-4)

Using Eq. (6-4), the required mean square duty cycle can be calculated from the average output power. A scaling block is inserted at the input of the AM path. If peak value of digital envelope input is unity, the scale factor is equal to the square root of the mean square duty cycle.

### 6.2.2 Digital-to-Pulse-Width Converter (DPWC)

From this section, algorithms of the digital signal processing are investigated. First function is the digital-to-pulse-width converter (DPWC). Figure 6.2 shows an example of a 2 bit DPWC to understand the function, where the high resolution input is converted to a 2 bit digital code word in a quantizer and the DPWC delivers a 4 series
sequence including the number of “1” corresponding to the digital code. In this example, the input binary data is “10” and the output sequence is “0110”, where the pulse width is equivalent to the number “1” and the pulse period is the length of the sequence. Therefore, the duty cycle, which is the ratio of the pulse width and period, is basically proportional to the input data.

![Figure 6.2: 2 bit digital-to-pulse-width converter (DPWC).](image)

There are different implementations of DPWC. To prevent the noise of the pulse position variation, the center of the pulse width is basically synchronized to the center of the pulse period. Figure 6.3 shows three implementations of DPWC, where \( N_{be} = 4 \). The vertical axis is the input data, which is converted into the quantized pulse width as represented at the horizontal axis. The horizontal axis indicates whole sequence and the first several bits are “0”. And then, in the duration between the black solid line and the gray solid line “1” is provided and the rest bits are “0” again. If the gray line is located at the left of the black line, the sequence is all “0”.

Digital to Pulse Width Clock (\( f_0 \))

\[ f_s = f_0 / 2^{N_{be}} \]

Full scale: 4

\( N_{be} = 2 \text{ bit} \)

2.1
Figure 6.3: Different implementations of DPWC when \( N_{\text{he}} = 4 \). (a) \( 2^{N_{\text{he}}-1} \) level/symmetry, (b) \( 2^{N_{\text{he}}-1}+1 \) level/symmetry and (c) \( 2^{N_{\text{he}}+1} \) level/asymmetry.
In Figure 6.3 (a) and (b), the pulse widths increase symmetry and the pulse center of each pulse width is completely synchronized. Both quantizing implementations are 8 \( (2^{N_{be} - 1}) \) and 9 \( (2^{N_{be} - 1} + 1) \) levels, respectively, where the number of bits substantially decreases by 1 bit. In Figure 6.3 (c), the quantization is 17 levels \( (2^{N_{be}} + 1) \), but the pulse width increases alternatively and the pulse center varies within 0.5 bit.

For this work, these digital functions are emulated using Matlab. Figure 6.4 shows a block diagram of a digital polar modulator. Most of the digital circuits of the modulator operate at a frequency of \( f_s = f_0 / 2^{N_{be}} \). To meet the measurement setup described in Section 6.4.1, the carrier frequency \( (f_c = 0.75 \text{ GHz}) \) is chosen to be a quarter of the digital clock frequency \( (f_0 = 3 \text{ GHz}) \). To prevent the effect of the PM signal, no quantization and ideal phase modulation are applied to the PM path. Quantization of the PM path will be discussed in Section 6.2.5.

Figure 6.4: Block diagram of a digital polar transmitter with scaling, quantization and DPWC of envelope path.
After scaling, AM data is digitally converted to DPWM pulses, where $N_{be} = 6$ bit. The pulse repetition rate ($f_{sw} = f_s$) is 46.875 MHz. The envelope current ($I_{dd}$) delivered from the inductor is emulated using the following equations:

$$I_{dd}(t_m) = \frac{V_{PW}(t_m) + V_{ind}(t_{m-1})}{f_0 \cdot L_{env} + R_{out}}$$

(6-5)

$$V_{ind}(t_m) = f_0 \cdot L_{env} \cdot I_{dd}(t_m)$$

(6-6)

$$R_{out} = \frac{2R_L}{\pi^2} \left(1 - \frac{Q_L}{Q_a}\right) + R_{SW} + R_{BC}$$

(6-7)

The RF modulated signal is obtained from the product of the envelope current and the PM signal.

Figure 6.5 shows the simulated spectra of the modulator at 24 dBm average output power using different DPWCs. WCDMA modulation (HPSK) with 3.3 dB PAPR is applied, using a symbol rate of 3.9 MS/s (rather than 3.84 MS/s) for coding simplicity. Preliminarily $L_{env}$ is 10 nH to avoid distortion due to the limitation of the envelope bandwidth. 65 level / asymmetry implementation has the lowest digital noise. The digital noises of 32 and 33 level / symmetry implementations are almost same. From the results, we decide to use the 65 level / asymmetry implementation (although a 64 level / asymmetry might be almost the same noise level).
6.2.3 Pre-emphasis Algorithm

There is a trade-off between signal bandwidth and switching image noise for the design of the output inductor. In order to reduce switching image noise, the output inductor may be used to roll off the higher frequency parts of the output signal, but then it may cause the ACLR of the RF output spectrum to degrade. In this case, a pre-emphasis algorithm is useful to improve the trade-off. Figure 6.6 shows a block diagram of a digital polar modulator with the pre-emphasis.
Figure 6.6: Block diagram of a digital polar transmitter with pre-emphasis of envelope path.

The pre-emphasized voltage $V_{pe}$ to drive the buck converter is calculated from the inverse transfer function of the LR load. $V_{pe}$ is given by:

$$V_{pe}(t) = \frac{L_{env}}{R_{out}} \frac{dV_{env}(t)}{dt} + V_{env}(t)$$

(6-8)

where $V_{env}$ is the desired envelope voltage. Correspondingly, the z transform $Y$ of the predistorted envelope signal shown in Figure 6.6 may be obtained from the envelope transform $X$ through

$$Y = \left\{ \frac{L}{R} \frac{f_0}{64} (1 - z^{-1}) + 1 \right\} \cdot X$$

(6-9)

Figure 6.7 shows the simulate spectra of the digital polar modulator with and without pre-emphasis of the envelope path. By increasing $L_{env}$ to be 100 nH, the clock
images of the DPWM signal decreases by approximately 17 dB. From the results, the distortion at the adjacent channels is significantly improved using the pre-emphasis.

Figure 6.7: Simulated spectra of digital polar transmitters with and without pre-emphasis of envelope path. \((f_s = 46.875 \text{ MHz}, N_{le} = 6, L_{env} = 100 \text{ nH}, f_c = 0.75 \text{ GHz})\)

Figure 6.8 shows the AM-AM characteristics of the digital polar transmitter (a) with pre-emphasis and (b) without pre-emphasis. In Figure 6.8 (a), large memory effect is shown due to the output inductor. Using pre-emphasis, the memory effect is amazingly improved as shown in Figure 6.8 (b). In addition, the EVM decreases from 9.5% to 0.8%. 
Figure 6.8: AM-AM characteristics of digital polar transmitters (a) without pre-emphasis and (b) with pre-emphasis. ($f_s = 46.875$ MHz, $N_{be} = 6$, $L_{env} = 10$ nH, $f_c = 0.75$ GHz)
6.2.4 Time Quantization Noise Shaping Algorithm

Typically a 10-12 bit DAC is used for handset transmitters [19]. However, only 6 bit resolution is available for a DPWM demonstration with the test bench used in this work, due to a trade-off between the signal bandwidth and available clock source frequency. In order to minimize the near-band quantization noise (such as EVM and ACLR) in communication signals such as WCDMA, an algorithm is developed to spectrally shape the time-quantization noise generated by rounding pulse transitions to the nearest clock cycle.

The proposed algorithm shown in Figure 6.9 is very similar to ΔΣ modulation, except that the noise shaping loop operates on time delays instead of amplitudes [107]. A quantizer rounds the input signal to meet the nearest possible transition of the DPWM signal. The difference between the desired signal and the rounded signal is computed. This time-quantization error is then integrated to create a running sum of the time-error in the system. This running sum of the time-error is added to the next incoming signal before rounding during its corresponding clock cycle.

In Figure 6.9, a time decay with an appropriately chosen time constant is also added to the error feedback to enable the algorithm to decay the accumulated error at the same rate as the LR circuit. The slew rate of the output current from the buck converter is limited due to finite supply and ground voltages. The above pre-emphasis approach cannot work beyond this slew rate limitation. Failure of the output current to accurately track the signal envelope not only causes an instantaneous error, but also causes a signal error to persist beyond the point of rapid slewing. The computed pre-distorted signal does not accurately represent the output and produces an error that decays at the L/R time
constant of the envelope path. The error can cause substantial near band spectral noise to be generated.

Figure 6.9: Block diagram of a digital polar transmitter with noise shaping of envelope path.

Figure 6.10 shows the simulated spectra with and without the noise shaping, and for comparison, the ACLR requirements of the standard (gray line). The green is no noise shaping, the blue is simple noise shaping and the red is noise shaping with decay. Using the noise shaping, near-band noise seems to be pushed to the outside. The decay function works to push the noise more aggressively. There is a trade-off between the ACLRs and the out-of-band noise, such as spurious emission and RxBN. For the demonstration of this chapter, the noise shaping with decay is applied.

Figure 6.11 is the normalized current waveform of the buck converter including proposed compensations (shown in the light gray line); it follows closely the ideal envelope current waveform (black line), although it also contains ripple from the clock images.
Figure 6.10: Simulated spectra of digital polar transmitters with noise shaping and decayed noise shaping. ($f_s = 46.875$ MHz, $N_{be} = 6$, $L_{env} = 100$ nH, $f_c = 0.75$ GHz, with pre-emphasis)

Figure 6.11: Current waveforms of a buck converter. ($f_s = 46.875$ MHz, $N_{be} = 6$, $L_{env} = 10$ nH, $f_c = 0.75$ GHz)
6.2.5 Quantization of PM Path

For demonstration, the PM data also needs to be quantized. In this section, the minimum requirement of PM data resolution is investigated. Figure 6.12 shows block diagram of the digital polar transmitter with PM path quantization, where $N_{bp}$ bit quantizer is inserted before the phase modulator. In addition, delays that are integer multiples of $1/f_0$ can be inserted in the AM path for time-alignment of AM and PM paths.

Figure 6.13 shows the simulated spectra of the digital polar transmitter with the phase quantization. $N_{bp}$ changes from 6 bit to 10 bit. With an increasing $N_{bp}$, the noise floor is improved. Since $N_{be}$ is 6 bit, it is considered that the digital noise is low enough when $N_{bp}$ is much higher than 6 bit.

![Block diagram of a digital polar modulator with digital compensation for AM path.](image-url)
6.3 Spurious Signal Reduction for DPWM

6.3.1 Slew Rate Related Dithering (SRRD)

To reduce the peak amplitude of spurious associated with the envelope clock replicas, RCFM [105] is a good candidate, in which switching between different clock frequencies randomly for the DPWM signal is used to reduce the peak amplitude of the spurs. However, the conventional RCFM increases the amount of noise compared with DPWM due to time quantization errors, especially in adjacent channels.

One of ideas for new RCFM is the switching frequency changes proportional to the slew rate of the signal. Figure 6.14 shows the conceptual input and output voltage waveforms of (a) conventional DPWM and (b) slew-rate related dithering (SRRD). The conventional DPWM uses a constant switching frequency. A signal with a high slew rate
contains higher frequency components. Therefore, if a higher switching frequency is applied in the high slew rate term and lower frequency is used in the low slew rate term to maintain the average frequency, it might be possible to obtain better signal integrity.

Detail of the proposed SRRD is explained. First, the average pulse period is decided ($2^{N_{be}}$). Next, the dithering range ($2^{N_{be}}-2^{N_{be}-2}+1 \sim 2^{N_{be}}+2^{N_{be}-2}-1$) is selected. The slew rate ratio is calculated from

$$SR = 0.5 \times \frac{dI_{dd}}{dt} \bigg/ \text{mean} \left( \frac{dI_{dd}}{dt} \right)$$

(6-10)

and $SR$ is clipped to be from 0 to 1. Pulse periods are calculated from

$$T_{PW} = 2^{N_{be}}-2^{N_{be}-2} + \text{int}(2^{N_{be}-1} \times SR)$$

(6-11)

PWM pulse sequence is generated using $T_{PW}$.

Figure 6.15 shows the simulated envelope spectra of (a) conventional DPWM and (b) SRRD using single-tone. The blue spectrum is ideal and the red spectrum is pulse-modulated. The average sampling frequency is approximately 47 MHz. Using SRRD, the noise around the desired signal is reduced and the spurious products due to the clock are pushed out to higher frequency. However, the peak of the spurs is reduced by only a few dB.
Figure 6.14: Conceptual input and output voltage waveforms of (a) conventional DPWM and (b) slew-rate related dithering (SRRD).
6.3.2 Minimum Quantization Error Dithering (MQED)

In order to reduce the peak amplitude of spurs without increasing near band noise, another approach to carrier frequency modulation is proposed, whose principle is presented in Figure 6.16 and Figure 6.17. If conventional DPWM is used, only a limited number of amplitudes can be selected (e.g., 2, 3, 4 and 5 are shown in Figure 6.16). Even if RCFM is applied, a large time quantization error occasionally appears, when the period is short (e.g., the period is 2 and the required output level is 0.75), and the resulting noise is spread over frequency. However, if these periods can be selected appropriately in accordance with the required output level, the time quantization error can be reduced (e.g., when the required output level is 0.75, a period of 4 and a width of 3 are selected). As a result, the equivalent number of timing bits increases (except for the first and last steps).
Furthermore, even if two combinations of period and width have the same width / period value (e.g., 2/4 and 4/8), their timing is generally different at the center of each period, and appropriate choices can result in a reduced quantization error. For example, Figure 6.17 shows a representative required envelope signal, along with output pulses with periods of 4 and 8 that could be chosen to encode it. The width / period for both pulse waveforms is 0.5. The quantities $e(4)$ and $e(8)$ are the errors between the required envelope signal and 0.5 at the centers of the pulses. In this case, it would be more accurate to select a period of 4 because $e(4)$ is smaller than $e(8)$.
Figure 6.17: MQED principle: time-alignment between ideal envelope and DPWM pulse.

Figure 6.18 shows a block diagram of a digital polar modulator employing a MQED technique. For this work, these digital functions are emulated using Matlab. The Matlab signals are subsequently uploaded to a pulse pattern generator, operating with a clock frequency ($f_0$) for the AM signal. The PM signal is generated based on Matlab inputs transferred to an arbitrary waveform generator and a vector signal generator. The input IQ data is first converted to polar format, and the PM carrier signal is generated using an 8 bit DAC and an analog quadrature modulator. The clock frequency of the DAC is $f_0/64$ due to the limitation of the instrument used.

AM data is pre-emphasized and quantized by using several pulse periods ($M_p$) ranging from $2^{N_{be}} - 2^{N_{be} - 2} + 1$ to $2^{N_{be} + 2^{N_{be} - 2}} - 1$, $N_{be} = 1, 2, \ldots$. Here $N_{be}$ is the average number of bits of DPWM. After that, the residual quantization errors ($e$) are calculated using all sets of pulse width ($W_p$) and $M_p$. Finally, a set of $W_p$ and $M_p$ with minimum $e$ is selected and a PWM pattern is generated from them. In addition, the minimum $e$ is fed back for noise shaping.
Figure 6.18: Block diagram of a digital polar modulator for MQED.

Figure 6.19 shows the simulated spectra of the MQED when a single-tone is generated. The average sampling frequency is approximately 47 MHz. From the results, the peak of the spurious products is approximately 15 dB lower than that of the DPWM. In the next section, a comparison using WCDMA modulation will be carried out.
### 6.3.3 Comparison between MQED, DPWM and 1 bit $\Delta \Sigma$ Modulation

To evaluate the proposed modulation technique, the spectra of the ideal PA outputs are simulated using Matlab; MQED, DPWM and 1bit DSM are applied. WCDMA modulation (HPSK) with 3.3 dB PAPR is chosen as the modulation to be represented. The source clock frequency, $f_0$, is 2949.12 MHz. The carrier frequency, $f_c$, is 1.75 GHz and the RX band is 1.84 GHz (selected to correspond to UMTS band III). Ideal CMCD PA and buck converter models with 6.9 dB loss at the output are assumed, in order to match the measured power. To avoid the effect of the clock image in the PM path, 750 MHz clock frequency is used for the PM signal.

Figure 6.19: Simulated envelope spectrum of MQED when single-tone is generated. ($f_s \sim 47$ MHz, $N_{be} = 6$ bit)

![Simulated envelope spectrum of MQED](image)

**Figure 6.19:** Simulated envelope spectrum of MQED when single-tone is generated. ($f_s \sim 47$ MHz, $N_{be} = 6$ bit)

\[
fs=46.875\text{MHz}, \quad R_{mqn}=31/64 \\
V=0.5 \cdot \sin(2\pi \times 1.01 \cdot t) + 0.5 \\
\text{# of transition} = 47028
\]
for a 1bit DSM, the choice was 117.965 MHz (under-clocked) in order to maintain $f_{sw,ave} < 50$ MHz, corresponding to almost the same peak DC power consumption of the buck converter as the average output power is swept. Figure 6.20 (a) shows that the near band noise of MQED is higher than that of the DPWM due to the noise spread effect of the dithering, at the output power of 20 dBm.

The trend of the noise far away from the carrier frequency is different among the three modulation approaches. The RX band noise of the UMTS band III, which is located at 95 MHz higher than the carrier frequency, is considered here as an example. From Figure 6.20 (b), the RX band noise of the MQED is lower than that of DPWM, but higher than that of the 1 bit DSM because the second images of the average switching frequency show up in the RX band. Even if the average switching frequency is adjusted for the RX band to fall between the images, the noise level of the MQED is higher than -100 dBm/Hz.

Figure 6.21 shows ACLR2 and RxBN vs average output power. The MQED keeps the near band noise lower over a wider range of average output power by increasing the effective number of bits, where ACLR2 (whose specification is harder to meet than ACLR1) is plotted. The noise of the 1 bit DSM is much higher due to the under-clocking. The RX band noise of the MQED is found to be about 7 dB higher than that of 1 bit DSM. This is because the MQED algorithm tends to spread the quantization error effects away from average switching frequency into neighboring spectral regions. This suggests that with MQED the noise level should be very low if the Rx band is inside the first images.
Figure 6.20: Simulated spectra with (a) 40 MHz span and (b) 500 MHz span of digital polar transmitters when $f_{sw_{ave}} < 50$ MHz. ($P_{out} = 20$ dBm, $f_c = 1.75$ GHz)
Figure 6.21: ALCR2 and RxBN of UMTS band III (95 MHz offset) vs average output power of digital polar transmitters when $f_{sw,ave} < 50$ MHz. ($f_c = 1.75$ GHz)

Figure 6.22 shows the simulated output spectra and the average output power dependence of the noise levels when the average switching frequency is constrained to be less than 200 MHz (and thus higher than for Figure 6.20). This places the Rx band within the first images. $N_{be}$ (the average number of bits of the MQED and DPWM) is decreased to 4, and the $f_0$ of the 1 bit DSM is scaled to be 491.52 MHz. In this case, the big difference between the MQED and DPWM is spurs. Peak spurs are improved by 7-9 dB using the MQED, and the requirement for the duplexer can be relaxed.

From Figure 6.23, the ACLRs of the MQED are lower than in other cases, in the 0-30 dBm average output power dynamic range, and the RxBN of the MQED and DPWM are reduced to -98 dBm/Hz or lower although that of 1 bit DSM is still around -90 dBm/Hz.
Figure 6.22: Simulated spectra in (a) 40 MHz and (b) 500 MHz span of digital polar transmitters when $f_{sw, ave} < 200$ MHz. ($P_{out} = 20$ dBm, $f_c = 1.75$ GHz)
Figure 6.23: ALCR2 and Rx band noise of UMTS band III (95 MHz offset) vs average output power of digital polar transmitters when $f_{sw, ave} < 200$ MHz. ($f_c = 1.75$ GHz)

6.4 Measurement Setups

6.4.1 Fully Digital Polar Modulator

In this section, a measurement setup is explained using a dual-channel pulse pattern generator (PPG), where one channel generates DPWM signal and another channel provides PM signal. This configuration is appropriate to demonstrate the proposed digital polar transmitter with fully digital inputs. Using the setup, WCDMA performance of the 1st generation digital polar transmitter is evaluated.

Figure 6.24 shows the concept of phase modulation, which is different from conventional IQ modulator [78] and phase locked loop (PLL) modulator [11]. PM data is converted to delay time and the delay time is added to the carrier signal with a frequency
of $f_c$. As the phase is increased, the delay time decreases. The resolution of the delay time ($\Delta t_d$) is $1/(2N_{bp} f_0)$.

Figure 6.24: Concept of phase modulation using a delay controller.

**A. Setup for Low Band**

The measurement setup for a demonstration of the 1st generation digital polar transmitter is shown in Figure 6.25. An $f_0 = 3$ GHz clock is generated with a PPG, which provides the DPWM signals to the buck converter, the PM signals at the carrier frequency to the CMCD amplifier, and $f_0/64$ frequency pulses to an arbitrary waveform generator (AWG). The $f_0/64$ frequency pulses work not only for clock synchronization but also as a trigger for AM and PM data. The PM signals have 2 bits of delay control (MSBs) generated by the PPG and an additional 6 bits of control through the AWG. All data is generated in Matlab and uploaded from a PC. The digital PM signals driving the CMCD PA were considerably low-pass filtered by our experimental setup, so we used an RF amplifier to boost their amplitude to 20 dBm. This maintained a proper switching operation of the CMCD but decreased its PAE (in a way that would not be necessary in a fully digital chipset).
Figure 6.25: Measurement setup of fully digital polar modulator with 3 GHz envelope source clock.

Details for generating a PM signal are shown using Figure 6.26. Phase input is in a range from 0 to 360 degrees. The relative phase of the PM signal delivered from the PPG is decided by the combination between the output sequence of the PPG and the output voltage of the AWG (i.e. the delay input of the PPG). The delay sensitivity of the PPG is 0.5 nsec/V and the corresponding AWG voltage range is from -333 mV to 333 mV.

![Diagram of measurement setup](image)

Figure 6.26: Relationship between phase input and PPG / AWG output.
B. Issue of PM Signal Generation in High Band

The maximum carrier frequency of the measurement setup is 0.875 GHz due to the 3.5 Gbps dual channel PPG. It is possible that the PPG controls only 1 bit of MSB and the remaining LSB is generated in AWG in order for higher carrier frequency. However, in this case, the delivered PM signal is corrupt as mentioned below.

Figure 6.27 shows the voltage waveform of the PM signal with \( f_c = (a) 0.75 \text{ GHz} \) and \( (b) 1.65 \text{ GHz} \). In Figure 6.27 (a), sequences of “0011” with -45 deg. phase and “1001” with +45 deg. delay are delivered alternatively, where both sequences should be same. From the measured waveform, the pulse widths at the transition points of two sequences are distorted from 50 % duty cycle, but no pulse disappears.

In Figure 6.27 (b), sequences of “10” with -90 deg. phase and “01” with +90 deg. delay are delivered alternatively. From the measured waveform, one pulse disappears. Possible reasons are the large rising / falling time of the control voltage delivered from the AWG and the limited bandwidth of the delay control input.

The missing pulse significantly affects the RF spectrum of the PM signal. Therefore, another setup is needed to evaluate the digital polar transmitter in both low and high bands, which will be discussed in the next section.
6.4.2 Quasi-digital Polar Modulator for Multiband Operation

For the multi-band operation, setups of quasi-digital polar modulator are applied, where a conventional IQ modulator is used for PM signal generation. Two different setups are employed with the DPWM source clocks of 3 GHz and 12 GHz. Using these setups, WCDMA modulation characteristics of the 1.5th and 2nd generation digital polar transmitters are evaluated.

Figure 6.27: Measured voltage waveforms of PM signals, where (a) $f_c = 0.75$ GHz and (b) $f_c = 1.65$ GHz.
Figure 6.28 shows a basic concept of quasi-digital PM signal generation. First, an analogue PM signal is generated using an IQ modulator, where the baseband clock frequency is \( f_s \) and the carrier frequency is \( f_c \). The analogue PM signal is applied a driver inverter integrated into the CMCD PA chip after amplified to relatively large. In this case, the inverter is overdriven and delivers PM modulated pulses, which is good enough for a switching-mode amplifier like the CMCD PA.

![Basic concept of quasi-digital PM signal generation](image)

Figure 6.28: Basic concept of quasi-digital PM signal generation.

**A. Setup with 3 GHz Envelope Source Clock**

Figure 6.29 shows the measurement setup of quasi-digital polar modulator with 3 GHz source clock. A PPG applies DPWM AM pulses into the buck converter and the external clock into an AWG, which also works as a trigger. The AWG delivers I and Q baseband voltages to a vector signal generator (VSG). The VSG provides a constant envelope PM signal to the CMCD PA through an RF amplifier and a 180 degree hybrid coupler. The \( f_0 \) of the PPG changes to 2.94912 GHz to easily generate data with a
symbol rate of 3.84 MS/s, easily although a higher clock rate is desired for high resolution AM data.

Figure 6.29: Measurement setup of quasi-digital polar modulator with 3 GHz envelope source clock.

Here, a small issue still remains for PM signal generation,. The delivered signal envelope is not completely constant as shown in Figure 6.30 (a). The reason for the dents is the slew rate limitation of AWG as shown in Figure 6.30 (b). I and Q signals sometimes have a big jump when the sampling clock is low. However, the AWG does not enable handling the big jump and it causes dents of $I^2+Q^2$. The dents cause spurs at a 46.08 MHz offset from the carrier in the RF spectrum. An improved setup will be described in the next section.
Figure 6.30: (a) WCDMA PM voltage waveform at sampling clock of 46.08 MHz and (b) voltage waveform of I, Q and $I^2+Q^2$ delivered from AWG with 46.08 MHz clock.

**B. Setup with 12 GHz Envelope Source Clock**

Figure 6.31 shows a measurement setup of a quasi-digital polar modulator with 12 GHz source clock, where high speed PPG and VSG with an AWG function are used for DPWM AM and PM signal generations. The $f_0$ of the PPG is 11.79648 GHz and the $f_s$ of the VSG is 92.16 MHz. By increasing the sampling clocks, the resolution of DPWM AM
data is increased, and the envelope of the PM signal can be more flat. In addition, the VSG has steep filters at IQ DAC, and the clock images of the PM signal are suppressed. The digital sampling clocks of both instruments are synchronized by a 10 MHz reference and a trigger signal from the PPG is used to synchronize AM and PM data. The trigger level of the PPG is ±0.5 V, but the input level of the VSG is TTL (0.8 / 1.5 V). Therefore, a bias-T is inserted as a level shifter. Digital control states are provided from multi-channel pulse pattern generator. In this work, the control is only used statically when the average output power and operation band are changed.

Figure 6.31: Measurement setup quasi-digital polar modulator with 12 GHz envelope source clock.

Figure 6.32 shows the voltage waveform of I, Q and I²+Q² delivered from VSG with 92.16 MHz clock. From the results, I²+Q² becomes relatively constant compared with Figure 6.30 although small ripples still remain.
Figure 6.32: Voltage waveform of I, Q and I^2+Q^2 delivered from VSG with a 92.16 MHz clock.

6.5 Experimental Results

6.5.1 1st Generation Digital Polar Transmitter (Modulation)

A. WCDMA Modulation

The measured ACLR values are sensitive to the parameters used for digital compensation as described in Section 6.2. The measurement setup in Figure 6.25 is used as explained in Section 6.4.1. In this work, the compensation is done manually as a preliminary demonstration rather than with an adaptive system.

Figure 6.33 shows the ACLRs vs. an estimated L_{env}/R_{out} constant for the pre-emphasis of the 1st generation digital polar transmitter, where some amount of delay is applied to the AM path. When L_{env}/R_{out} = 31 nsec, the ACLRs achieve good balance. L_{env} and R_{out} are expected to be approximately 79 nH and 2.53 Ω.
Figure 6.33: Measured impact of digital control parameters for ACLR optimization: estimated $L_{env}/R_{out}$.

Figure 6.34: Measured impact of digital control parameters for ACLR optimization: relative delay of AM path.
Figure 6.34 shows an ACLR vs. relative delay of the AM path where $L_{env}/R_{out} = 31$ nsec. At -4 nsec, the ACLRs have almost their minimum values. The compensation control was easily done by changing only two parameters.

Figure 6.35 shows the measured and theoretical average output power vs root square mean (RMS) duty cycle of the 1st generation digital polar transmitter using a WCDMA modulation signal. The theoretical curve is calculated using Eq. (6-4), where $R_L = 12.5 \ \Omega$, $Q_L = 1.2$, $Q_u = 5$, $V_{dd} = 3.3 \ \text{V}$, $R_{SW} = 0.65 \ \Omega$ and $R_{BC} = 0.3 \ \Omega$. A loss of the GRB (0.68 dB) is also applied to the calculated output power. The difference between the results of both is approximately 1.6 dB at an RMS duty cycle of 69 %.

Figure 6.35: Measured and theoretical output power vs RMS duty cycle of 1st generation digital polar transmitter. ($f_0 = 3 \ \text{GHz}$, $f_c = 0.75 \ \text{GHz}$, $N_{be} = 6$, $f_{sw} = 46.875 \ \text{MHz}$, $L_{env}/R_{out} = 31$ nsec, $V_{dd} = 3.3 \ \text{V}$, $N_{bp} = 8$)

Figure 6.36 shows the overall PA efficiency, as a function of the average output power. At 24 dBm, the overall efficiency was 26.5 %. (As for the single-tone case, the PAE taking into account the 20 dBm input was lower, at 16.1 %, although in real
application scenarios the number would be much closer to the drain efficiency). Higher efficiency can be expected using a high resistivity silicon-on-insulator substrate due to smaller FET parasitic capacitance and higher capacitor quality factor.

Figure 6.36: Measured overall efficiency vs average output power of 1st generation digital polar transmitter. \((f_0 = 3 \text{ GHz}, f_c = 0.75 \text{ GHz}, N_{be} = 6, f_{sw} = 46.875 \text{ MHz}, L_{en}/R_{out} = 31 \text{ nsec}, V_{dd} = 3.3 \text{ V}, N_{bp} = 8)\)

Figure 6.37 shows the ACLR vs average output power. In the range 16 to 24 dBm, the ACLRs were within 3GPP specifications without AM-AM and AM-PM digital predistortion. Non-linearity in the low power region is one of the reasons for ACLR degradation.
Figure 6.37: Measured ACLR vs average output power of 1st generation digital polar transmitter. ($f_0 = 3$ GHz, $f_c = 0.75$ GHz, $N_{be} = 6$, $f_{sw} = 46.875$ MHz, $L_{em}/R_{out} = 31$ nsec, $V_{dd} = 3.3$ V, $N_{bp} = 8$)

Figure 6.38 shows the measured spectrum at 24 dBm average output. Figure 6.38 (a) covers a span of 24.68 MHz, showing the low ACLR values, while Figure 6.38 (b) shows a broader 500 MHz span. As seen in the figure, the output exhibits, in addition to the WCDMA signal, have many undesirable clock images separated by the 46.875 MHz DPWM frequency. The highest of these is at a level of about -20 dBc. These images can be removed from the bands of interest by use of a higher PWM frequency. Accordingly, the buck regulator design of the present chip allows higher input clock frequencies to be used, but the test bench available was only able to support the experimentally used frequency at the necessary pulse width resolution. Alternatively, the clock images could be suppressed with multi-phase inter-leaved digital modulation as reported in [108]. The harmonics of the carrier at the output are considerably smaller than these spurs because
the load impedances provided within the CMCD PA are close to open and short at even and odd harmonics, respectively.

![Figure 6.38: Measured output spectrum at 10 dB / division ($P_{ave} = 24$ dBm, PAPR = 3.3 dB). (a) 24.68 MHz span. (b) 500MHz span. ($f_0 = 3$ GHz, $f_c = 0.75$ GHz, $N_{be} = 6$, $f_{sw} = 46.875$ MHz, $L_{env}/R_{out} = 31$ nsec, $V_{dd} = 3.3$ V, $N_{bp} = 8$)](image)
6.5.2 1.5th Generation Digital Polar Transmitter (Modulation)

A. WCDMA Modulation (Multiband Operation)

Next, the WCDMA modulation measured results of the 1.5th generation digital polar transmitter is explained, where we focus on the carrier frequencies of 0.85 GHz and 1.75 GHz to confirm the multiband operation. The measurement setup in Figure 6.29 is used as explained in Section 6.4.2.

Figure 6.39 shows the measured and theoretical output power vs RMS duty cycle of the 1.5th generation digital polar transmitter (a) at 0.85 GHz using C64 and (b) at 1.75 GHz using C0. In the measurement, no dithering is applied for the DPWM; \( f_{sw} \) for the DPWM are 46.08 MHz \( (N_{be} = 6) \) with \( f_0 = 2949.12 \text{ MHz} \). The PAPR of the modulation signal is 3.3 dB. The theoretical output power is calculated using (a) \( R_L = 9.2 \Omega, Q_L = 2.5, Q_u = 8.5, V_{dd} = 3.3 \text{ V}, R_{SW} = 0.65 \Omega, R_{BC} = 0.3 \Omega \) and (b) \( R_L = 15.2 \Omega, Q_L = 2.0, Q_u = 7.5, V_{dd} = 3.3 \text{ V}, R_{SW} = 0.65 \Omega, R_{BC} = 0.3 \Omega \). Losses of the GRB \( (0.73 / 0.84 \text{ dB}) \) are also applied to the calculated output power. The difference between both results is approximately 0.6 / 1.7 dB at the RMS duty cycle of 53 %.

Figure 6.40 shows the average output power dependence of the measured ACLR and overall efficiency (a) at 0.85 GHz using C64 and (b) at 1.75 GHz using C0, where \( f_{sw} \) for the DPWM are 46.08 MHz \( (N_{be} = 6) \) with \( f_0 = 2949.12 \text{ MHz} \). From the results, the ACLRs are within 3GPP specifications at 0.85 GHz in the range 10 to 26 dBm, while from 12 to 20 dBm at 1.75 GHz without AM-AM and AM-PM DPD. The cause of non-linearity in the high band is largely the non-linearity of the switching stage parasitic capacitance. In the low band, the capacitance of the BSC (which is linear) is relatively
large and mitigates the shift of the resonance frequency of the PA for low instantaneous output power. The peak overall efficiencies are 26 % and 19 % at 26 dBm / 0.85 GHz and 25 dBm / 1.75 GHz, respectively.

Next, $f_{sw}$ for the DPWM increases to 184.32 MHz ($N_{he} = 4$) with $f_0 = 2949.12$ MHz. The measured ACLRs and overall efficiencies vs average output power are shown in Figure 6.41. For high values of average switching frequency, the linearity is degraded due to the rising / falling-time limitations of the buck converter. DPD may help to improve the ACLR in the wide output power range. The peak overall efficiencies are 21 % and 16 % at 26 dBm / 0.85 GHz and 24 dBm / 1.75 GHz, respectively.

Figure 6.39: Measured and theoretical output powers vs RMS duty cycle of 1.5th generation digital polar transmitter: (a) C64, $f_c = 0.85$ GHz, $L_{env}/R_{out} = 35$ nsec and (b) C0, $f_c = 1.75$ GHz, $L_{env}/R_{out} = 40$ nsec. (DPWM, $f_0 = 2949.12$ MHz, $N_{he} = 6$, $f_{sw} = 46.08$ MHz, $V_{dd} = 3.3$ V, $N_{bp} = 8$)
Figure 6.40: Measured ACLRs and overall efficiencies of 1.5th generation digital polar transmitter with WCDMA signals: (a) C64, $f_c = 0.85$ GHz, $L_{env}/R_{out} = 35$ nsec and (b) C0, $f_c = 1.75$ GHz, $L_{env}/R_{out} = 40$ nsec. (DPWM, $f_0 = 2949.12$ MHz, $N_{be} = 6$, $f_{sw} = 46.08$ MHz, $V_{dd} = 3.3$ V, $N_{bp} = 8$)

Figure 6.41: Measured ACLRs and overall efficiencies of 1.5th generation digital polar transmitter with WCDMA signals: (a) C64, $f_c = 0.85$ GHz, $L_{env}/R_{out} = 35$ nsec and (b) C0, $f_c = 1.75$ GHz, $L_{env}/R_{out} = 40$ nsec. (DPWM, $f_0 = 2949.12$ MHz, $N_{be} = 4$, $f_{sw} = 184$ MHz, $V_{dd} = 3.3$ V, $N_{bp} = 8$)
B. Effect of MQED

Figure 6.42 shows the measured spectra of a digital polar transmitter with DPWM and MQED modulations, covering (a) a 40 MHz span and (b) a 500 MHz span. The average $f_{sw}$ for the envelope modulation is 46.08 MHz ($N_{be} = 6$). The carrier frequency is 1.75 GHz and the output power is 20 dBm. The resolution bandwidths are 100 kHz and 3 MHz, respectively. In Figure 6.42 (a), compared with the simulated near band spectra shown in Figure 6.20 (a), there is considerable spectral regrowth caused by the non-linearity of the devices which dominates the ACLRs. Therefore, the measured ACLRs for MQED encoding are almost the same as those for conventional DPWM except in the case of ACLR2s. The ACLR2s of MQED are 1-2 dB higher due to the spreading of the spurious noise into the alternate channel band, although the values are within the 3GPP specifications.

In Figure 6.42 (b), measured spectra over a wider span are similar to the simulations of Figure 6.20 (b). The RxBN values estimated for UMTS band III are less than -90 dBm/Hz. Peak spurs from DPWM are suppressed by over 3.2 dB using 46 MHz switching frequencies of the buck converter.
Figure 6.42: Measured spectra of 2nd generation digital polar transmitter with DPWM and MQED modulations: (a) span 40 MHz and (b) span 500 MHz, $f_{\text{sw, ave}} \sim 46$ MHz. ($P_{\text{out}} = 20$ dBm, $f_c = 1.75$ GHz)
Figure 6.43 shows the measured spectra, for the envelope modulation switching rates of 184.32 MHz ($N_{he} = 4$), which is four times higher than Figure 6.42. In Figure 6.43 (a), almost the same amount of near-band spectral regrowth is measured between the MQED and DPWM, which is different from Figure 6.42 (a). Unfortunately, the ACLR improvement of the MQED as shown in Figure 6.22 disappears due to the device non-linearity. However, the effect of the DPD is limited by the original signal in the measured examples, and the proposed MQED should still have some advantages.

In Figure 6.43 (b), measured spectra over a wider span are similar to the simulations of Figure 6.22 (b). The RxBNs estimated for UMTS band III are less than −100 dBm/Hz. Peak spurs from DPWM are suppressed by over 9.0 dB using 184 MHz switching frequencies of the buck converter. Spurs emerge at around 46 / 92 MHz offset frequency from the carrier due to unexpectedly small envelope variations of the PM signal caused by experimental slew rate limitations of the instrument for the IQ baseband signal generation.

In Figure 6.44, the measured spectra are compared with the required spectral mask at the output of PA explained in Chapter 1. The red and blue spectra are the results when the MQED and DPWM are applied, respectively. The black broken dot line is a target spectral mask. By applying the proposed algorithm, the spectrum delivered from the PA is satisfied with required spectral mask except receive band noise.
Figure 6.43: Measured spectra of a polar transmitter with DPWM and MQED modulations: (a) span 40 MHz and (b) span 500 MHz, $f_{sw, ave} \sim 184$ MHz. ($P_{out} = 20$ dBm, $f_c = 1.75$ GHz)
Figure 6.44: Comparison between measured spectrum and required spectral mask.

6.5.3 2nd Generation Digital Polar Transmitter (Modulation)

A. WCDMA Modulation (Wide Power Dynamic Range)

Finally the WCDMA modulation measured results of the 2nd generation digital polar transmitter is explained. By changing the number of active CMCD PA and buck converter unit-cells, the power dynamic range performance is evaluated. The setup in Figure 6.31 is applied as described in Section 6.4.2.

Figure 6.45 shows the measured average output power vs the theoretical average output power at the carrier frequency of (a) 0.85 GHz and (b) 1.75 GHz, where only the DPWM mode is used for the envelope signal generation. Parameters for calculation are (a) $R_L = 12.5 \, \Omega$, $Q_L = 3.2$, $Q_u = 9.8$, $V_{dd} = 3.6 \, V$, $R_{SW} = 57.0/n+0.13 \, \Omega$, $R_{BC} = 0.3 \, \Omega$ and (b) $R_L = 17.0 \, \Omega$, $Q_L = 2.2$, $Q_u = 8.1$, $V_{dd} = 3.6 \, V$, $R_{SW} = 55.9/n+0.13 \, \Omega$, $R_{BC} = 0.3 \, \Omega$, where n is the number of active unit-cells. As n decreases, $R_{out}$ increases. However, the decay factor of the noise shaping does not change from the values when $n = 1023$ for
loop convergence. From these results, the measure average output powers are almost proportional to the theoretical average output powers although some amount of offset remains. The offsets are approximately 1 dB and 3 dB at 0.85 GHz and 1.75 GHz, respectively.

Figure 6.46 shows the overall efficiency vs average output power of the WCDMA signal at (a) 0.85 GHz and (b) 1.75 GHz. The overall efficiency is almost in line with an ideal class-B curve in a range higher than 0 dBm average output power.

Figure 6.47 shows the ACLR vs the average output power of the WCDMA signal at (a) 0.85 GHz and (b) 1.75 GHz. In the range -2 to 26 dBm, the ACLRs are within 3GPP specs without digital pre-distortion at 0.85 GHz, and at 1.75 GHz, the range is from -2 to 18 dBm.

Figure 6.48 shows the compared results between measured ACLRs and Matlab simulated ACLRs at 1.75 GHz, where $N_{be}$ is (a) 6 bit and (b) 8 bit. In Figure 6.48 (a), it is found the measured ACLR2s with $n = 2$ and $4$ are almost the same as simulation, which indicates the quantization noise of the envelope signal limits the ACLR2s. By increasing the number of bits, the measured ACLR2s are improved significantly and at -9 dBm, the ACLR1 and ACLR2 are satisfied with 3GPP specifications without DPD.
Figure 6.45: Measured average output power vs theoretical average output power of a 2nd generation digital polar transmitter: (a) C64, \( f_c = 0.85 \) GHz, \( L_{env}/R_{out} = 37 \) nsec and (b) C0, \( f_c = 1.75 \) GHz, \( L_{env}/R_{out} = 35 \) nsec. (DPWM, \( f_0 = 2949.12 \) MHz, \( N_{be} = 6, f_{sw} = 46.08 \) MHz, \( V_{dd} = 3.6 \) V, \( N_{bp} = 8 \))

Figure 6.46: Measured overall efficiency vs average output power of a 2nd generation digital polar transmitter: (a) C64, \( f_c = 0.85 \) GHz, \( L_{env}/R_{out} = 37 \) nsec and (b) C0, \( f_c = 1.75 \) GHz, \( L_{env}/R_{out} = 35 \) nsec. (DPWM, \( f_0 = 2949.12 \) MHz, \( N_{be} = 6, f_{sw} = 46.08 \) MHz, \( V_{dd} = 3.6 \) V, \( N_{bp} = 8 \))
Figure 6.47: Measured ACLR vs average output power of a 2nd generation digital polar transmitter: (a) C64, $f_c = 0.85$ GHz, $L_{env}/R_{out} = 37$ nsec and (b) C0, $f_c = 1.75$ GHz, $L_{env}/R_{out} = 35$ nsec. (DPWM, $f_0 = 2949.12$ MHz, $N_{be} = 6$, $f_{sw} = 46.08$ MHz, $V_{dd} = 3.6$ V, $N_{bp} = 8$)

Figure 6.48: Measured and simulated ACLRs vs measured average output power of a 2nd generation digital polar transmitter with $N_{be} = 6$ and $N_{be} = 8$: (DPWM, $f_0 = 2949.12$ / 11796.48 MHz, $f_{sw} = 46.08$ MHz, $V_{dd} = 3.6$ V, $N_{bp} = 8$)
B. Spurious Related PM path Imperfection

In Figure 6.43 (b), unexpected spurious are emerged near the desired signal due to the imperfection of the PM path as explained in Section 6.4.2. It is confirmed that the spurious are suppressed using the measurement setup in Figure 6.31.

Figure 6.49 shows the measured spectra of the 2nd digital polar, covering 200 MHz span. The average $f_{sw}$ and $N_{be}$ for the envelope modulation are 184.32 MHz and 6, where the corresponding $f_0$ is approximately 11.8 GHz. The carrier frequency is 1.75 GHz and the output power is 16 dBm. The resolution bandwidth is 3 MHz. From the result, no spurious products are shown except the clock images of the envelope signal.

Figure 6.49: Measured spectra of 2nd generation polar transmitter with DPWM modulation, where span is 200 MHz, $f_{sw, ave} \sim 184$ MHz, $P_{out} = 16$ dBm, and $f_c = 1.75$ GHz.
6.6 Summary

A digital compensation algorithm is introduced to maintain linearity with the digital polar modulation, which is effective for a wide power dynamic range technique. In addition, a new digital pulse width modulation algorithm is also shown to partially suppress spurious signals associated with the digital input envelope signal.

Using the 1st generation digital polar transmitter, 26.5 % overall efficiency is achieved at 0.75 GHz and 24 dBm average output, along with ACLRs that satisfied 3GPP specifications. The out-of-band peak spurs of the 1.5th generation digital polar transmitter are reduced by 9-10 dB using the proposed dithering technique, in bands corresponding to UMTS band III. By applying an 8 bit resolution envelope signal, in the range -7 to 18 dBm, the ACLRs of the 2nd generation digital polar transmitter are within 3GPP specs without digital pre-distortion.

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Chapter 7

Conclusion and Future Work

7.1 Dissertation Summary

To make a transceiver simpler and more compact in a handset, it is important to develop a single transmitter that can work in multi-standard operation with high efficiency. In this dissertation, the design of digitally-assisted watt-level CMOS PA have been investigated, including octave frequency band operation, several decade output power control and adaptive DSP algorithm to maintain signal integrity. The study of the characteristics of single components and individual circuit blocks in theoretical analysis, simulation and experiment has led to solutions for integration and better performance of the whole transmitter.

The dissertation began by proposing a new digitally-assisted RF PA architecture for multiband and multimode operation, where a CMCD configuration for high efficiency in the RF PA, and a polar modulation scheme driven by digital inputs, were applied. Challenges of circuit implementation and DSP were summarized for the proposed architecture, based on measured results using discrete devices and simulated results.
First challenges of circuit implementation were a watt-class CMOS PA and a high
switching frequency buck converter. Stacked FETs were used for the CMCD PA to
obtain high breakdown voltage. An on-chip RC snubber circuit was employed for the
buck converter to reduce the over- and under-shoots of the output voltage. The designed
digital polar transmitter was demonstrated using 0.15 μm CMOS technology, and peak
output power and overall efficiency for a single-tone signal were 30 dBm and 40.6 %
respectively, at 0.75 GHz carrier frequency.

A second challenge was multi-band functionality. To operate in the 0.7-1.8 GHz
frequency band, two types of variable resonators, 1) hybrid of on-chip band-switching
capacitor (BSC) and bonding wire inductor, and 2) full on-chip integration, were
developed. A broadband on-board doughnut-shaped Guanella reverse balun was also
designed. By combining the hybrid variable resonator and on-board balun, overall
efficiencies of 27.1 / 25.6% were obtained at 30.2 / 28.9 dBm CW output powers and
0.85 / 1.75 GHz carrier frequencies, respectively. By applying the fully integrated
variable resonator, overall efficiencies of 13.2 / 22.2 % were achieved at 27.5 / 29.0 dBm
output powers.

A third challenge was to achieve wide output power dynamic range. An
architecture consisting of small segmented unit-cells is introduced into the PA and buck
converter. Multiple three-state unit-cells were used for the driver and final stages of the
CMCD PA and the state of each unit-cell was controlled to provide a specific output
power. To improve the efficiency in power back-off, a new operation mode analogous to
switched capacitor operation was realized using the proposed envelope modulator. The
overall dynamic range was expanded to approximately 90 dB and 85 dB at 0.85 GHz and 1.75 GHz carrier frequencies, respectively.

A challenge of the DSP was to overcome a trade-off between ACLR and spurious products. Digital compensation techniques were developed to maintain linearity of an envelope modulator, which is strongly related with ACLR. A new DPWM algorithm was also shown to partially suppress spurious signals associated with the digital input envelope signal. When WCDMA modulation was implemented, spur suppression of 9-10 dB was achieved while maintaining ACLRs within 3GPP specifications. In addition, by combining the algorithm with unit-cell switching architecture, ACLR requirements were satisfied in the range from -7 to 18 dBm at 1.75 GHz.

7.2 Future Works

7.2.1 Output Power and Efficiency Improvement

In this work, a novel octave frequency range watt-class CMOS PA has been demonstrated. However, the efficiency was lower than that of commercial PAs. One of the major reasons is the low quality factor of the variable resonator, which is less than 10, due to losses on the conductive substrate of bulk Silicon technology. Recently, a PA using high-resistivity Silicon-on-insulator (HRSOI) substrate and laterally diffused metal oxide semiconductor (LDMOS) FET, which is compatible with standard CMOS process, has been reported [109]. The quality factor of the BSC can be improved to approximately 30 using the HRSOI substrate and the resonance frequency shift of the CMCD PA in back-off could be improved by applying the LDMOS. Therefore, those technologies promise higher efficiency CMOS PAs.
7.2.2 Wideband Envelope Signal Generation

In this work, 200 MHz switching frequency buck converter has been developed as an envelope modulator. However, as the switching frequency increases, the efficiency and controllable current dynamic range were sacrificed. One of possible solutions for wider bandwidth envelope signal is two-point modulation [28], [110], where two different envelope modulation procedures are combined to make a balance between efficiency and signal integrity. If the proposed architecture is utilized, a combination of DC current control and unit-cell switching can be employed although time-alignment and gain-adjustment of the two paths will be required.

7.2.3 Wideband PM Signal Generation

In this work, the PM signal was close to ideal since it was delivered from test bench instruments. However, it is actually one of big challenges to generate wideband PM signal in a transceiver IC [111]. Conventional PLLs suffer from a trade-off between bandwidth and jitter. Possible candidates of wideband PM signal generators are variable delay circuit [112] and digital quadrature modulator [113]. Research in these areas just started.

7.2.4 Modulation Scheme for Very Low Average Output Power

In this work, an 85-90 dB power dynamic range transmitter has been developed. Signal modulation at very low output powers remains as a future work. It is possible just to apply unit-cell switching like DPAs [11], [79], but they may require approximately 120 dB dynamic range. On the other hand, as the average output power decreases, the requirements of receive band noise (RxBN) and spurious emission are substantially
relaxed because they are specified by absolute values rather than by values that scale with output power. In this situation, a 1 bit RF pulse modulation technique, such band-pass delta-sigma modulation and band-pass pulse width modulation, could be applicable. This might lead to easier implementation in the low output power region.

7.2.5 DSP Algorithm for Receive Band Reduction

In this work, DSP algorithms have been studied to generate linear envelope signal with low spurious products. However, the RxBN of the delivered signal is still higher than the requirement. The noise is generated from the interaction of the AM and PM signals. One approach to avoid the issue is to reshape both signals by limiting their bandwidth, preventing the signals from spreading to the Rx band frequency. Another possible approach is to cancel the noise in the receiver using an adaptive noise cancelling algorithm [114].
Appendix A

Co-simulation of Circuit and EM Simulators

For RF simulation including large size devices, co-simulation of circuit and electro-magnetic (EM) simulators are needed. Here, we introduce two cases: band-switching capacitor and current-mode class-D power amplifier. The simulated results have been compared with the measurement in Chapter 4.

A. Band-switching Capacitor (BSC) for On-wafer Measurement

Figure A 1 show layouts of the BSC for accurate simulation. MIM capacitors, pads and interconnects are simulated by an EM simulator (Agilent Momentum). FET switch is simulated using a circuit simulator (Cadence Virtuoso), where simulation program with integrated circuit emphasis (SPICE) model with layout parasitic extraction (LPE) is applied. S-parameters of the passive components and eight FET switches are combined using a circuit simulator (Agilent Advance Design System: ADS).
Figure A 1: EM simulation and LPE layouts of BSC for on-wafer measurement.

**B. Current-mode Class-D Power Amplifier (CMCD PA)**

For CMCD PA, SPICE models with LPE are applied for the stacked FETs and the switches of the BSC. MIM capacitors, Interconnects and bonding pads are simulated by Momentum, where some of them are shown in Figure A 2-Figure A 4. The frequency range of the EM simulation is up to 20 GHz for 9th harmonics. As bonding wires, ADS models are used and a shape of a bonding wire is introduced in Figure A 5. Equivalent circuits are used for GRB, based on measured S-parameter fitting as shown in Figure A 6 and Figure A 7. Finally, all of them are combined in Cadence Virtuoso and characteristics of CMCD PA are simulated using transient engine of Agilent GoldenGate.
Figure A 2 shows the output parallel line of the differential stacked FETs. In the layout, the differential FETs and drivers are segmented into 128 unit-cells and sixteen unit-cells form two rows. This parallel line combines the outputs of sixteen unit-cells and delivers to bonding pads of chip through the BSC block.

![Figure A 2: EM simulation layout of output parallel line of differential stacked FETs (1/8 size, 34 ports).](image)

Figure A 3 shows EM simulation and LPE layouts of the 1/8 size BSC block for the CMCD PA. The upper layout is used for the EM simulation of the MIM capacitor, where sixteen MIM capacitors are placed. The lower layout is for the LPE of the FET switch. A differential signal is applied from the left side and delivered to the right side.

Figure A 4 shows EM simulation layout of the output combiner and bonding pads. There are eight differential inputs and one differential output. Two bonding wire inductors supposed to be connected to four inner pads and one bonding wire inductor is placed between the differential output.
Figure A 3: EM simulation and LPE layouts of BSC block of CMCD PA, where upper is MIM capacitors and lower is a FET switch (1/8 size, 4 ports).
Figure A 4: Simulation model of output combiner and pads. (32 ports)
Figure A 5 shows a shape of the bonding wire for the output of the CMCD PA. A CMCD PA chip with a bonding wire supposed to be placed at the left side and the on-board GRB is located at the right side.

![Figure A 5: Shape of bonding wire at output of CMCD PA.](image)

Figure A 6 shows equivalent circuits of the on-board GRB for (a) low band and (b) high band. It is difficult to pursue an accurate EM simulation of the balun because the size of the balun is large enough for the wavelength of the RF signals and the setting of the ports in the EM simulation significantly affect the results. Therefore, the equivalent circuit models, fit to the measured results, are used for the CMCD PA simulation.

Figure A 7 shows comparison between the simulated and measured (a) differential $S_{11}$ and (b) $S_{21}$ of the GRB. From the results, simulated results are in good agreement with the measured results except the $S_{11}$ in the high band. Both simulated and measured impedance are approximately 12.5 $\Omega$ in the high band and the difference between them won’t affect the overall CMCD PA simulation.
Figure A 6: Equivalent circuit models of GRB. (a) low band model (0.7~1 GHz) and (b) high band model (1.4~2 GHz).
Figure A 7: Fitting results of GRB, where (a) $S_{11}$ and (b) $S_{21}$ are shown. (Input: $Z_0 = 6.25 \, \Omega$ each side, Output: $Z_0 = 50 \, \Omega$)
Appendix B

Alternative Techniques for Wide Power Dynamic Range PAs

Here, we would like to discuss about alternative approaches to improve the power dynamic range and the efficiency in back-off of the digital polar transmitter although they are not used for the demonstration of this work.

A. Cross-coupling Switching PA

Figure B 1 shows the circuit schematic of a cross-coupling CMCD PA for feed-through cancellation. In order to reduce the leakage current through the parasitic capacitance between the input and output of each stacked FET, an opposite phase current is applied through an additional capacitor ($C_{XC}$). By adjusting $C_{XC}$ to be same as the parasitic capacitance of the stacked FET, the leakage can be minimized.
Figure B 1: Circuit schematic of cross-coupling CMCD PA for feed-through cancellation.

Figure B 2 shows the output power vs DC current of CMCD PA when the carrier frequencies \( f_c \), are (a) 0.85 GHz and (b) 1.75 GHz. The stacked FETs are designed using L-foundry 0.15 \( \mu \)m CMOS technology and all passive components are ideal elements. The black curve is the simulated output power with \( C_{xc} = 5 \) pF and the gray broken curve is the results without the cross coupling capacitors. From the results, the power dynamic range improves by approximately 10 dB and 15 dB at 0.85 GHz and 1.75 GHz, respectively, using the cross-coupling configuration.

One of drawbacks of the technique is that the equivalent output shunt capacitance increases. Table B 1 shows the simulated equivalent output capacitance and the required capacitance ratio of BSC to cover in the range from 0.85 GHz to 1.75 GHz. Using the cross-coupling technique, the equivalent shunt capacitance increases by approximately 0.75 \( C_{xc} \). As a result, the required capacitance ratio increases from 5.8 to 7.8. It is difficult to realize such a large capacitance ratio using a bulk CMOS technology. Therefore, we decided not to use this technique for the demonstration.
Figure B 2: Output power vs DC current of CMCD PA using cross-coupling configuration at (a) $f_c = 0.85$ GHz and (b) $f_c = 1.75$ GHz. ($C_{XC} = 5$ pF, $L_{res} = 0.5$ nH, $R_L = 12.5 \ \Omega$, $V_{g2} = 2.8 / 2.9$ V).

Table B 1: Equivalent output shunt capacitances, and required capacitance ratio of BSC.

<table>
<thead>
<tr>
<th></th>
<th>$C_p$ (pF)</th>
<th>$C_{res}$ (pF)</th>
<th>Cap. Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>No XC</td>
<td>5.4</td>
<td>64.7</td>
<td>11.1</td>
</tr>
<tr>
<td>$C_{xc}=5pF$</td>
<td>8.4</td>
<td>61.7</td>
<td>8.1</td>
</tr>
</tbody>
</table>
**B. Charge Reuse Technique for Driver Stage of PA**

Unit-cell switching technique is effective to improve the driver and final stage efficiency because the DC power consumption of the driver stage can decrease. However, if the DC power consumption of each unit-cell can be reduced, the unit-cell switching is more effective especially in the high band. An inter-stage matching inductor [115]-[117] is one of possibilities. However, the bandwidth of the matching network is limited and the occupied area should be huge if all unit-cells have individual inductors. In this work, another new technique like a switched capacitor is studied.

Figure B 3 shows the (a) circuit schematic and (b) timing chart of a new driver stage. Each inverter of the differential driver stage has a certain dead time at both rising and falling edges. In the dead time, the output ports are shorted by an additional switch. In the meanwhile, half of the charge stored in the parasitic output capacitance of one side moves to the other side. We can say that the driver stage reuses the charge at the rising and falling edge.

Figure B 4 shows the current flow of the charge reuse driver stage. In Figure B 4 (a), a charge $Q_1 = C_{drv} V_{drv} / 2$ is stored to one side capacitor and a charge $Q_2$ of another side is discarded to the ground. In Figure B 4 (b), half of $Q_1$ moves from the left inverter to the right inverter. In Figure B 4 (c), the rest half of $Q_1$ is discarded, but additional charge from the DC supply to the right inverter is only $C_{drv} V_{drv} / 4$. Using this structure, the DC power consumption of the driver stage ideally becomes half.
Figure B 3: (a) Circuit schematic and (b) timing chart of charge reuse driver stage.
Figure B 4: Current flow of charge-reuse driver stage.
Figure B 5 shows the simulated output power vs DC current of CMCD PA using three types of driver stages at the carrier frequency of (a) 0.85 GHz and (b) 1.8 GHz. The light gray broken line is the normal inverter, the bold gray broken line is the driver stage with the inter-stage inductor of 0.6 nH ($Q = 20$ at 2 GHz) and the black solid line is the charge reused driver stage with 1 mm NMOS inter-stage switch and optimal dead time. In this simulation, single FETs are used as the final stage and ideal inductor and capacitor are used for the output resonator. The load resistors are 5 $\Omega$ and 10 $\Omega$ at 0.85 GHz and 1.8 GHz, respectively. From the results, the linearity of the charge reuse driver stage is relatively better than others and the feed-through is lower than that of the inter-stage inductor at 0.85 GHz and 1.8 GHz.

Figure B 5: Simulated output power vs DC current of CMCD PAs using three types of driver stage at the carrier frequencies of (a) 0.85 GHz and (b) 1.8 GHz. ($f_{res} = f_c$, $L_{res} = 0.4$ nH, $Q_u = \infty$, $R_L = 5 / 10$ $\Omega$, $V_{drv} = 1.8$ V, inductor used for inter-stage matching is 0.6 nH with the Q of 10 at 2 GHz and gate width of FET used for charge reuse is 1 mm)
Figure B 6 shows the driver and final stage efficiency vs output power. From the results, the efficiencies of the charge reuse driver stage are improved from those of the normal at 0.85 GHz and 1.8 GHz. The efficiency of the inter-stage inductor is highest at 1.8 GHz, but lowest at 0.85 GHz. The charge reuse driver stage is useful to improve the efficiency of the CMCD PA in the wide frequency range.

![Graphs showing driver and final stage efficiency vs output power](image)

Figure B 6: Simulated driver and final stage efficiency vs output power of CMCD PA using three types of driver stage at the carrier frequencies of (a) 0.85 GHz and (b) 1.8 GHz. ($f_{\text{res}} = f_c$, $L_{\text{res}} = 0.4 \text{ nH}$, $Q_u = \infty$, $R_L = 5 \div 10 \ \Omega$, $V_{\text{drv}} = 1.8 \text{ V}$, inductor used for inter-stage matching is 0.6 nH with the Q of 10 at 2 GHz and gate width of FET used for charge reuse is 1 mm)

One of drawbacks of this technique is that precise dead-time control is required. Figure B 7 shows the optimal dead time used for the simulation. From the results, the optimal dead times are in the range from 50 psec to 100 psec. Since the dead time is too small to generate using a 0.15 μm CMOS technology, we decided not to use this technique for the demonstration.
C. Output Capacitance Reduction of Buck Converter Using Inductor

The output capacitance loss is one of big causes for the DC power dissipation of the buck converter in back-off. In this section, one of the ideas to reduce the output capacitance, which is investigated in the early stage of this work, is summarized although the technique was not used for the demonstration.

Figure B 8 shows the circuit schematics to reduce the output capacitance. In Figure B 8 (a), the body is connected to the ground through a large resistor. Since the drain-body capacitance is replaced with the series connection of the drain-body-source capacitances, the total output capacitance decreases. In Figure B 8 (b), the body-source capacitance is resonated by the additional inductor at the switching frequency of the buck converter. Therefore, the total output capacitance at the switching frequency can be reduced.
Figure B 8: Circuit schematics to reduce output capacitance using (a) large resistors and (b) impedance matching inductor.

Figure B 9 shows $P_{\text{reg}}$ vs $I_{\text{out}}$ of the buck converter with the body resistor and inductor. For simplicity, only final stage is simulated, where the FET model of Jazz 0.18 μm BiCMOS technology and ideal passive components are used. $V_{dd}$ is 3.3 V, $R_{PA}$ is 1 Ω, $f_{sw}$ is 200 MHz and no dead time is applied. From the results, using the resistor or inductor, $P_{\text{reg}}$ in back-off improves from 180 mW to 160 mW (11 % improvement). Difference between the resistor and inductor is small.

The effect of the proposed technique is confirmed, but the improvement is not so large. In addition, the body diode may not work to prevent breakdown when the over- and under-shoot are emerged in the actual situation. Therefore, we decided not to apply the technique for the demonstration.
Figure B 9: Simulated regulator DC power dissipation vs DC output current of buck converter with body resistor and inductor.
Appendix C

PCB Design for Digital and RF Analogue Mixed Signal

In this work, the unit-cell control of the CMCD PA is used statically to extend the power dynamic range. However, this technique can be also applied to the signal modulation. In this case, unit-cells need to be switched by the frequency of the envelope modulation. Here, PCB design including off-chip circuit and layout is discussed for several hundred MHz digital clock frequency.

A. Resistive Divider for Level Shifter

Block diagram and measurement setup of 2nd generation digital polar transmitter have been shown in Figure 5.38 and Figure 6.31, where digital data and clock are provided from data and clock pods of the pulse pattern generator incorporated into the logic analyzer. Maximum clock rate is 300 MHz (half channel) / 180 MHz (full channel) and data rate is half of clock rate. The voltage swing of the data pod is 3.3 V, but the voltage swing of decoders in chips is supposed to be 1.8 V. Also, the low and high voltages of the LVPECL clock pod are 1.6 V and 2.3 V, respectively. Therefore, the level shift circuit is needed.
The resistive divider circuit is one of good candidates to generate 1.8 V swing pulse from 3.3 V pulse as shown in Figure C 1 (a). The ratio of these resistances are decided by voltage ratio, but the absolute values are depends on the signal integrity. The output resistance of the data pod is approximately 32.5 Ω and the input capacitance of the chip is approximately 0.75 pF (~1.4 kΩ at 150 MHz). Therefore, 250 Ω and 350 Ω are used. Figure C 1 (b) shows the simulated voltage waveform at the chip input. The pulse waveform seems to be sharp enough.

Figure C 1: (a) Resistive divider circuit for data pod and (b) simulated voltage waveform at chip input loaded by pad, I/O and latch.

Since the output level of the clock pod is LVPECL (1.6 V / 2.3 V) and the voltage swing is 0.7 V, the level shifter is used for clock pod as shown in Figure C 2 (a). The bias voltage of 0.8 V is supplied through 2 kΩ, which is higher than the load resistance of the clock pod (215 Ω). Figure C 2 (b) shows the simulated voltage waveform, where the black curve is the voltage at the chip input and the gray curve is at the output of the clock distribution circuit. From the results, the 1.8 Vpp pulse signal seems to be reproduced.
Figure C 2: (a) Resistive divider circuit for data pod and (b) simulated voltage waveform at chip input loaded by pad, I/O and latch.

**B. PCB Ground**

One of puzzling issues for mixed signal evaluation boards is ground. Preliminary, we fabricated an evaluation board with the ground separated between analog and digital blocks as shown in Figure C 3. RF analog ground is significantly large and digital round is relatively small. Using the PCB, the signal integrity supplied from the clock pod is evaluated. Green dots indicate probing point on PCB and no chip is mounted for simplicity. G2U and G2T are analog ground and G1U, G3U, G1T and G3T are digital ground. Smaller number is nearer to clock pod and move to chip side with increasing number.
Figure C 3: Probing point to test signal integrity from clock pod.
Figure C 4 shows measured signal waveform before DC block capacitance. The blue curve is a reference waveform, which is measured without connecting to the PCB. The other voltages are measured between probing points specified in the legend. With increasing number of probing point, signal looks to be corrupt. Especial voltage between S2T and G3T is small and strange shape because G3T takes a roundabout way with the ground of the clock pod.

Figure C 4: Measured clock waveforms between probing points shown in Figure C 3. (a) CMCD PA side and (b) buck converter side. ($f_{\text{clock}} = 300$ MHz).

To obtain a better waveform, both grounds are combined using copper tape and soldering. Figure C 5 shows the measured waveform. Since G3U and G3T are almost same voltages as G2U and G2T, respectively in this condition, G2U and G2T are used as the ground. From the results, better waveforms are obtained compared with the case of the separated ground.
Figure C 5: Measured waveforms when analog and digital grounds are combined. (a) CMCD PA side and (b) buck converter side.
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