UNIVERSITY OF CALIFORNIA SAN DIEGO

Highly Integrated Hybrid DC-DC Converters for High Performance Power Delivery Systems: Design, Analysis and Implementation

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2023

The Dissertation of Tianshi Xie is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2023

DEDICATION

To my beloved family: my wife Jingxiang Tian, my daughter Ada Xie, my father Jiadong Xie and mother Yanling Liu.

In memory of my grandfather Zhiyuan Xie, a pioneer in Nuclear Medicine in China

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C. Hardy, H. Pham, M. Jatlaoui, F. Voiron, T. Xie, P. Chen, S. Jha, P. Mercier, H. Le, " A Scalable Heterogeneous Integrated Two-Stage Vertical Power-Delivery Architecture for High-Performance Computing," in 2023 IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2023.

T. Xie, J. Zhu, D. Maksimovic and H. -P. Le, "A Highly Integrated Hybrid DC–DC Converter With nH-Scale IPD Inductors," in IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 705-719, March 2023, doi: 10.1109/JSSC.2022.3227163.

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T. Xie, M. R. Oltra, and H. Le, "A 5kV/15W Dual-Transformer Hybrid Converter with Extreme 2000X Conversion Ratios for Soft Mobile Robots," in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2020.

T. Xie, R. Das, G.-S. Seo, D. Maksimovic, and H.-P. Le, "Multiphase Control for Robust and Complete Soft-charging Operation of Dual Inductor Hybrid Converter," in 2019 IEEE Applied Power Electronics Conference and Exposition (APEC).

ABSTRACT OF THE DISSERTATION

Highly Integrated Hybrid DC-DC Converters for High Performance Power Delivery Systems: Design, Analysis and Implementation

by

Tianshi Xie

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2023

Professor Hanh-Phuc Le, Chair

As the development of technology, devices, particularly semiconductor, have scaled down dramatically enabling the high performance of computing systems. However, when examine the entire electronics system, the total dimension is not equally scaled. It is found that magnetic devices are the bottleneck for the dimensional scaling. In this dissertation, several commonly employed methods for reducing the usage of inductors are discussed and compared, including high switching frequency converter, switched-capacitor converter, hybrid converter and resonant converter. Each of these converters has been proved that partially meet the requirement of miniaturized system with fine regulation and high energy efficiency. In the following chapters,

three approaches that address the problem from circuit operation, circuit technique and circuit topology are proposed.

The first one is multi-phase operation of a hybrid converter, as discussed in Chapter. 3. With multi-phase operation instead of dual-phase which is more commonly used, the effective frequency over the output inductors is 3 times higher leading to smaller inductors. While retaining the benefits of using a Dickson-Star hybrid converter, such as high conversion ratio, soft-charging of flying capacitors, the multi-phase operation has also been proved to gain the robustness on the flying capacitor mismatch. A demonstration PCB has been made to show the experimental results. The peak efficiency was captured at 40 V-1.8 V/4 A with a number of 92.4 %.

Secondly, an auxiliary circuit assisted Zero-Voltage-Switching 3-Level Buck (ZVS-3LB) converter is introduced in Chapter. 4 with its fundamental operations, design analysis and key experimental results. By inserting an auxiliary ZVS circuit with around 20% area overhead, the converter achieves maximum 30% loss reduction compared with a conventional 3-level buck converter when the output current is below 1.5 A. A peak efficiency of 92.4% is reached for 20 V/5 V conversion at 1 A load. As another significant benefit, ZVS operation allows the switching frequency to reach a multiple Mega-Hertz range as a result of low switching loss, making the topology a good candidate for minimizing inductor usage.

Furthermore, an Integrated Transformer-less Stacked Active Bridge (ITSAB) converter that uses only nano-Henry scale inductors at 2-5 MHz switching frequency is proposed in Chapter. 5. Since it is derived from a Dickson-Star Switched Capacitor converter, the proposed converter inherits the benefit of low voltage stress on switches while enjoying an efficient fine regulation by phase shift, similar to a Dual Active Bridge (DAB) converter. The converter is optimized, designed and fabricated in 1.7 mm $\times$ 1.9 mm area of a 130 nm BCD process. The active die is flip-chipped on a 6.5 mm $\times$ 6.5 mm package substrate together with power capacitors and two 10 nH IPD inductors for demonstration, illustrating the feasibility of passive components integration, resulting in a peak efficiency of 91.2% and a peak power density of 1.36 W/mm^3

from 9.6-12 V input to 2.15-3.3 V output. Another demonstration is constructed on the same package substrate but with discrete air-core inductors. It achieves a peak efficiency of 92.4% and a peak power density of 0.62 W/mm^3, while delivering a max power of 7.5 W. To achieve the performance, a detailed loss analysis and a unique optimization methodology for the converter, together with the design of key sub-blocks, including gate drivers (GDs), phase shift modulator (PSM), and ramp generator (RG), are provided in this chapter.

Additionally, a revised prototype of ITSAB converter that is capable of higher output current is presented in Chapter. 6. It has been demonstrated 5.2 A output current with 10 nH inductors. The chip is fabricated with the same technology. The necessary techniques to achieve such high output current, including the 3D integration and switch partitioning, are addressed.

In last, a conclusion and future works, such as CC-CV mode, bidirectional conversion are presented.

Chapter 1

Demand for Miniaturized and Efficient Power Delivery Network

Pushed by the famous Moore's Law (Fig. 1.1), technology has been continuously evolving and brought unprecedented change to modern human life. Albeit the physics limitation, the performance trend predicted by the Moore's Law is well maintained with transistor structure innovation, multi-threading operation, 3D integration and many more technology. However, the trend of another vital metrics does slowdown (Fig. 1.2), which is the microprocessor typical power. It hits the limitation that is usually rephrased as power wall. In other words, with this power limitation, the High Performance Computing (HPC) unit can't really work as designed despite the growth of number of transistors.

What's more, as indicated in [3], the power consumption of a major supercomputer in the year of 2035 would reach the power level of a nuclear power plant, if the same energy efficiency of computing is maintained, as shown in Fig. 1.3. Apparently, this is insane. Therefore, many improvements that prioritize energy efficiency must be done. From the power delivery point of view, the improvements could include new converter topology, innovation in integration and packaging.

On the other hand, when reviewing the history of electronic devices, there is a noticeable trend of dimension shrinking. A computer, for example, changes from a gigantic machine when it was first invented, to a portable device that is used in everyday life. That being said, to satisfy

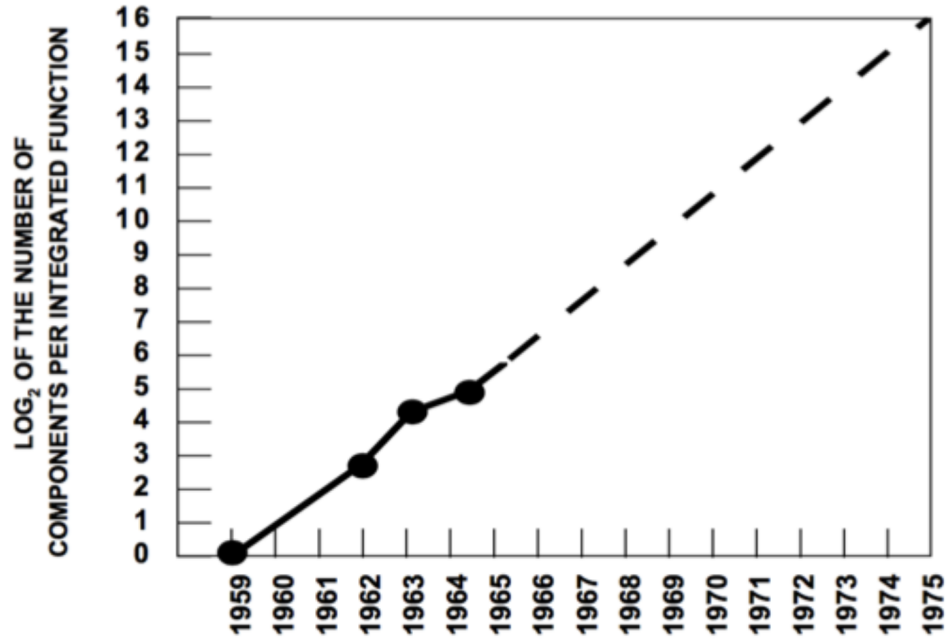


Figure 1.1. Moore's Law [1]

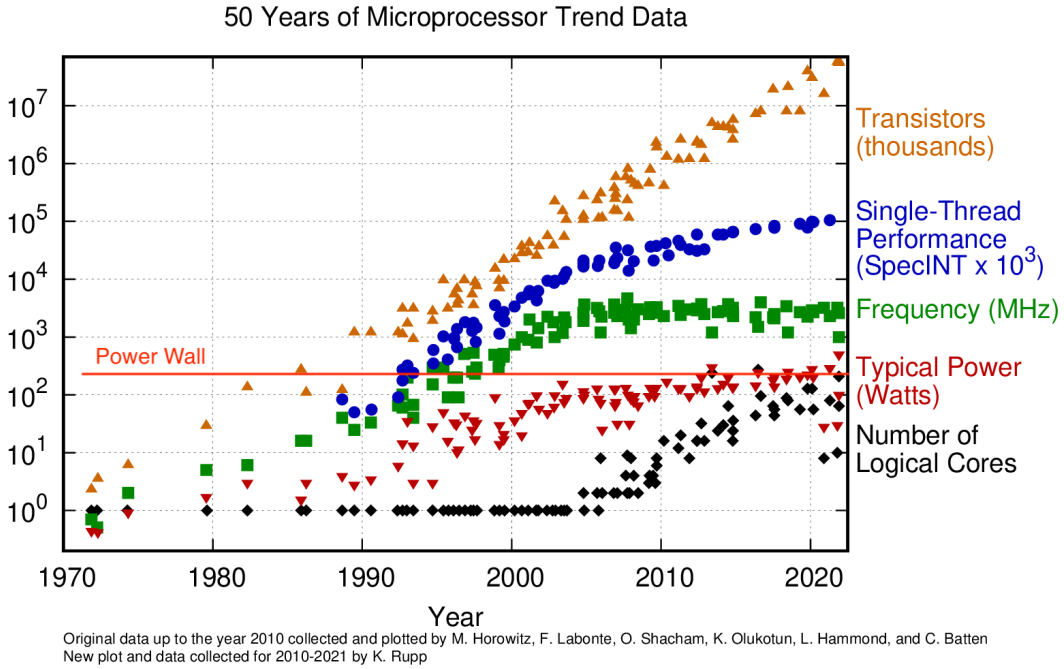


Figure 1.2. Collected data showing trend in microprocessor technology [2]

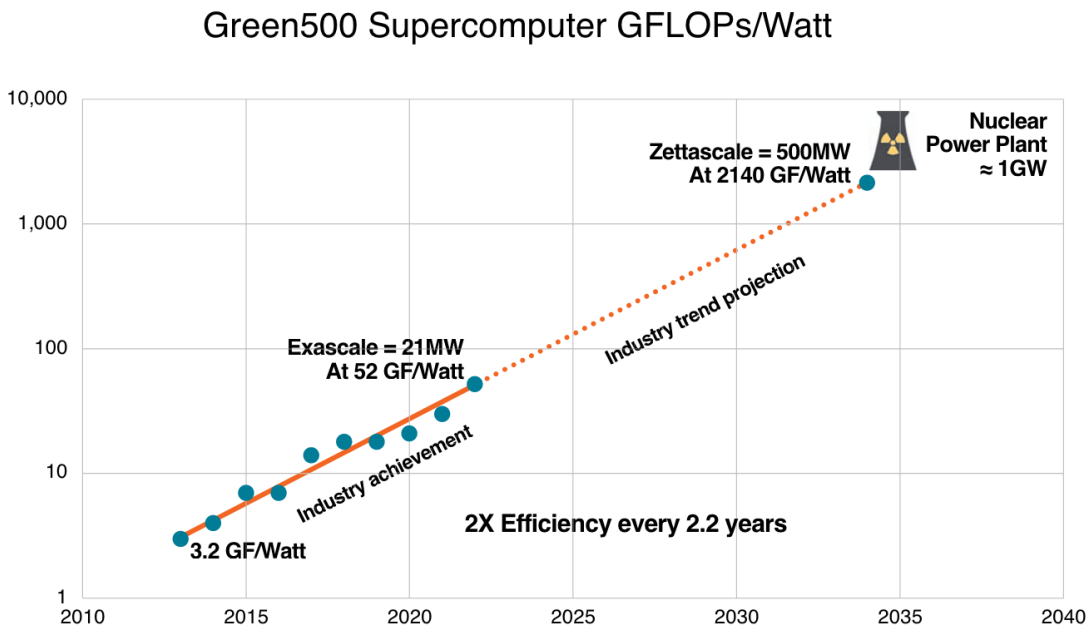


Figure 1.3. Trend in power efficiency of top performing super-computers [3]

the aforementioned computation capability, the required power density within these electronic devices has been continuously increasing [4, 5], making the power delivery design increasingly challenging. Active devices, who are benefited from semiconductor technology scaling, decline in dimension without losing in performance, whereas passive devices, particularly the magnetic components, do not keep up with the rate of scaling and miniaturization [6]. As a consequence, as implied in the main board of a major brand smart phone (Fig. 1.4), inductors dominate the size of modern power converter implementations. In other words, to diminish the board dimension and increase the power density, it is important to reduce the number of inductors used on board and the individual inductor size.

From the survey of inductance vs. volume for Coilcraft XEL series inductors depicted in Fig. 1.5, the dimension of an inductor linearly changes with its inductance. Therefore, the desired high power density converter design prioritizes a small inductance for power delivery.

In addition to improving the quality of inductors, significant efforts have been invested in coming up with new converter topologies and different operating principles to reduce the required inductance [7–11]. The most straightforward approach to minimize inductance is operating

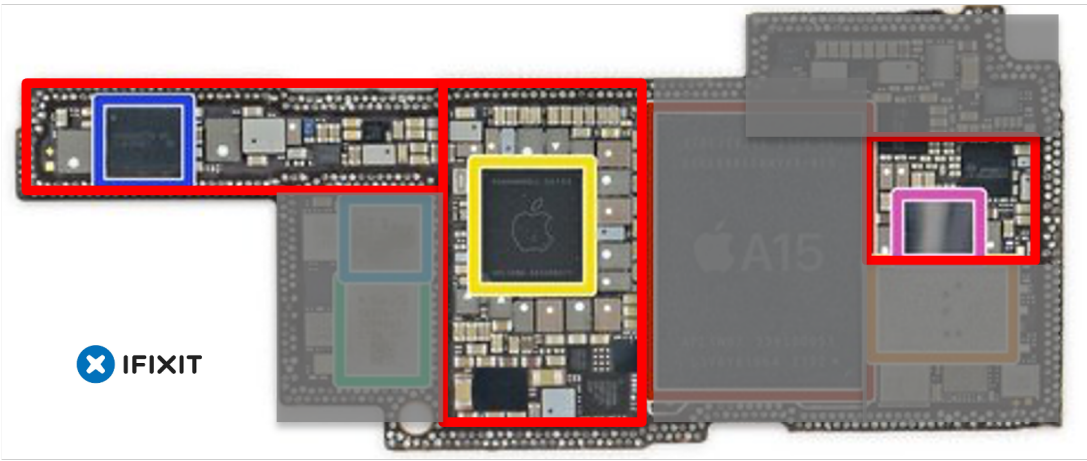


Figure 1.4. iPhone 13 Pro (2021) main board, the highlighted parts are power management circuits and obviously a lot of inductors occupy the area

a power converter at very high frequency (VHF) [12, 13]. However, the benefit of reduced inductance comes with increased switching losses leading to reduced efficiency. Alternatively, Switched capacitor (SC) converters, which require no inductors, are good candidates for realization of fully integrated power converters [14–16]. However, drawbacks of an SC converter include significantly degraded efficiency when operating away from the nominal conversion ratio, and large output noise with variable frequency that could cause EMI issues in the system. Therefore, new topologies that efficiently utilize inductors are emerging, such as hybrid converters [7, 9–11, 17, 18]. With the help of capacitors that blocks high DC voltage, the inductors are magnetized with much lower voltage such that smaller inductors can be employed. Nonetheless, most of the previously proposed hybrid converters are based on discrete-circuit realizations, still requiring inductances in the range of 100 nH or larger. In an another effort to use less inductance, resonant or quasi-resonant converters are employed. Unfortunately, output regulation is often challenging for converters with a resonant tank while satisfying high efficiency and small size requirements. The quasi-resonant converter demonstrated in [8] was a successful demonstration of this type of converter, capable of regulation at relatively low switching frequency. However, its efficiency is relatively low, and more importantly, the 36 nH inductor used is still large, which makes it difficult for on-chip realization. Further increasing the switching frequency to achieve a

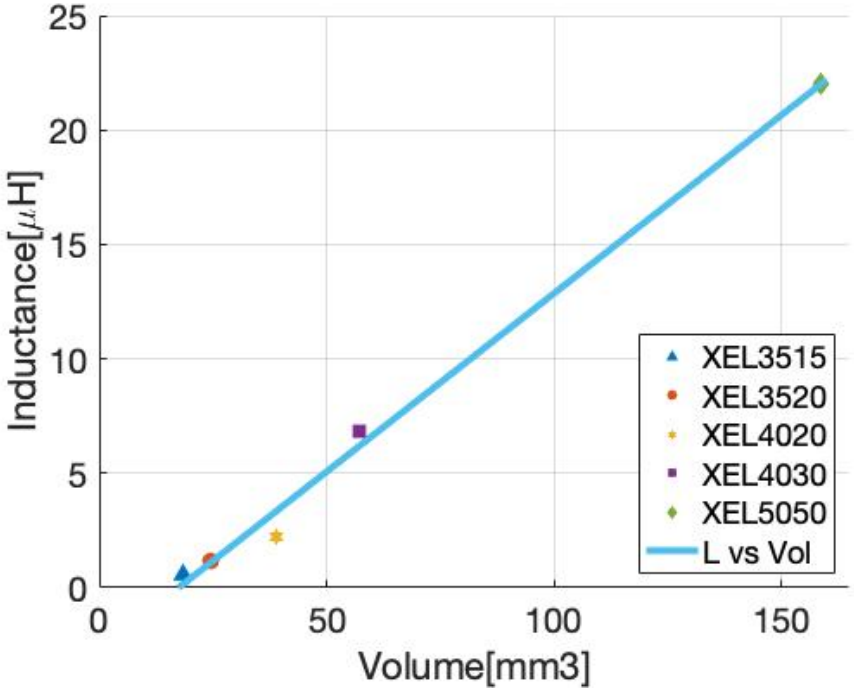


Figure 1.5. A survey of inductance vs. volume for Coilcraft XEL series inductors.

smaller inductor would face significant challenge in maintaining high efficiency [6]. In the next chapter, detailed analysis and comparison between these topologies would be addressed.

Chapter 2

Overview of the Converters with Reduced Magnetic Devices

As illustrated in Chapter 1, magnetic components are the bottleneck to reduce the overall dimension and to improve the power density. To reduce the usage of magnetic parts, several applicable methods have been analyzed and implemented in prior arts. In this chapter, they are evaluated and commented.

2.1 High frequency Switched-inductor Converter

As for a buck converter, the inductor current ripple is inversely proportional to the switching frequency f and the inductor value L:

$$\Delta i_L \propto \frac{V_{in}}{fL} \tag{2.1}$$

To achieve the same current ripple, if a smaller inductance is selected, the switching frequency must be increased. In most cases, a smaller inductance leads to a lower profile inductor and hence a miniaturized power module. However, as analyzed in [13], if considering maintaining a consistent quality factor Q and an acceptable temperature rise ΔT, a cored inductor will cease scaling down once hit the temperature rise limit, while a coreless inductors can keep declining in size but with a lower rate when approaching the temperature rise limit. In other words, if

using an coreless inductor, it is a viable method to shrink the overall converter size by increasing switching frequency.

On the other hand, even though the analysis above implies nearly the same the loss over inductors after scaling as a result of consistent Q, increasing switching frequency results in poor efficiency at light load due to excessive switching loss. To deal with this design challenge, several approaches have been published.

Reported in [19], the solution of actively tuning switching frequency at light load has been effectively proved for USB-C application. The idea can be summarized as Fig. 2.1. However, the reduced switching loss comes with the penalty of the circuit complexity and dynamic performance.

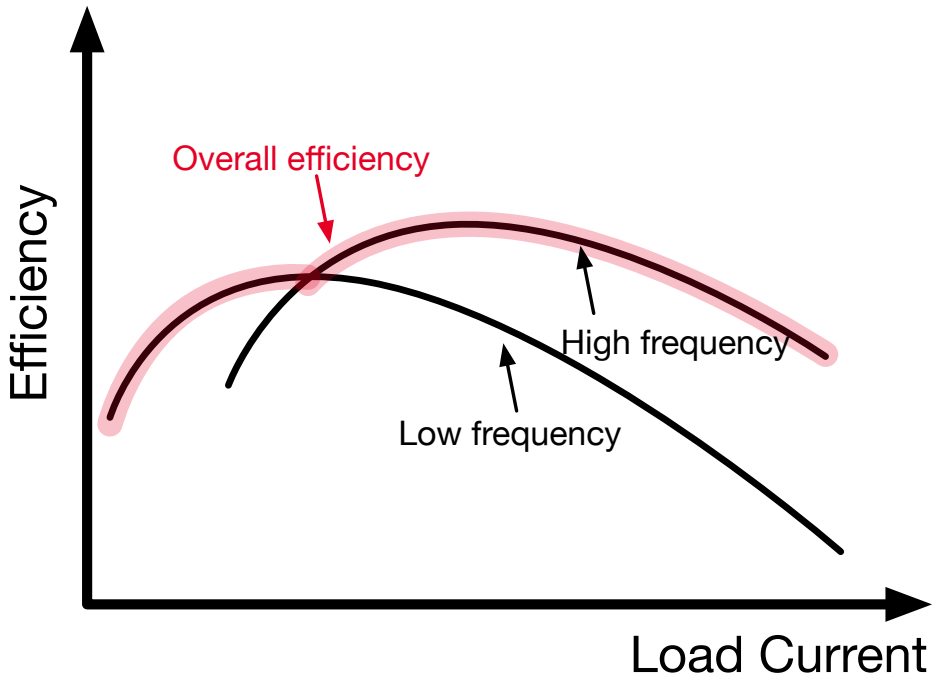


Figure 2.1. The concept of variable switching frequency that improves light load efficiency

Boundary Conduction Mode (BCM) operation, as shown in Fig. 2.2 is another way to achieve soft-switching at light load as demonstrated in[20–22]. However, the limited ZVS range and high conduction loss resulted from large current ripple remain problems.

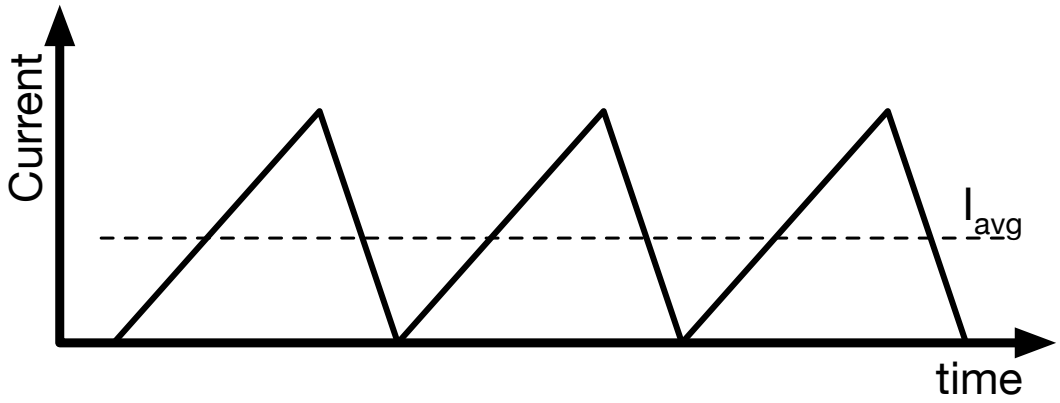


Figure 2.2. BCM operation that enables soft-switching

In addition to these methods, using auxiliary passive components to generate required charge for ZVS is another viable method [23, 24]. Through an inductor, the parasitic capacitors associated with the switchihng node will be softly charged/discharged once the auxiliary current is higher than the main inductor current and hence the converter achieves soft-switching. Despite the switching loss is effectively reduced as reported in these works, a lack of precise timing control causes more charge delivered from auxiliary circuit than required for ZVS and therefore hurts efficiency.

2.2 Switched-capacitor Converter

Switched-capacitor (SC) topology is a potential candidate for Point-of-Load (PoL) converter [25] due to the fact of zero inductor and hence possible fully integration of the converter. As discussed in numerous publications, a SC converter can be modeled as a DC transformer (DCX) with an output resistance as shown in Fig. 2.3.

The regulation of the converter is to modulate the output resistance R_{out} by tuning one or combination of the listing parameters: switching frequency f_s[15], size of the power switches and the effective flying capacitance C_{fly}[26].

The calculation of the output resistance is evaluated by charge flow analysis described in [27]. Take one-capacitor 2:1 switched capacitor (SC) converter as an example. The charge flow

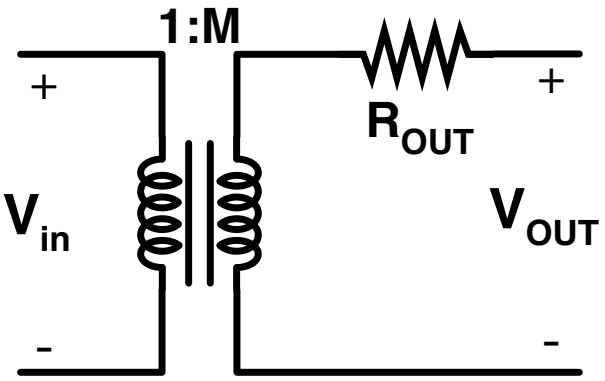


Figure 2.3. Switched-capacitor converter model

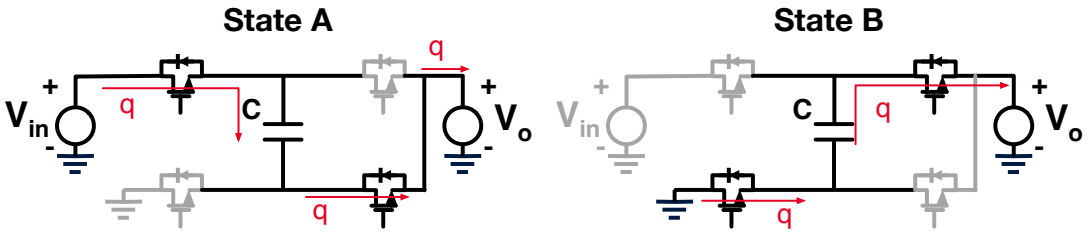


Figure 2.4. Charge flow analysis of 2:1 switched-capacitor converter

can be depicted as in Fig. 2.4. The charge transferred through the capacitor is the same during state A and state B, which is q, while the total charge flows to the output is $2q$. The conversion ratio M, slow switching limit (SSL) resistance R_{SSL} and fast switching limit (FSL) resistance R_{FSL} are as follows.

$$\begin{aligned} M &= \frac{q_{IN}}{q_O} = \frac{q}{2q} = \frac{1}{2}, \\ R_{SSL} &= \frac{1}{4 f_s C}, \\ R_{FSL} &= 2R_{ON} \end{aligned} \tag{2.2}$$

where q_{IN}, q_O, f_s, C and R_{ON} are input and output charge, switching frequency, capacitance and ON resistance of each switch, respectively. The total output resistance R_{out} is therefore expressed as,

$$R_{OUT} = \sqrt{{R_{SSL}}^2 + {R_{FSL}}^2} \tag{2.3}$$

The value of (2.3) is sketched in Fig. 2.5. It indicates the output resistance of a SC

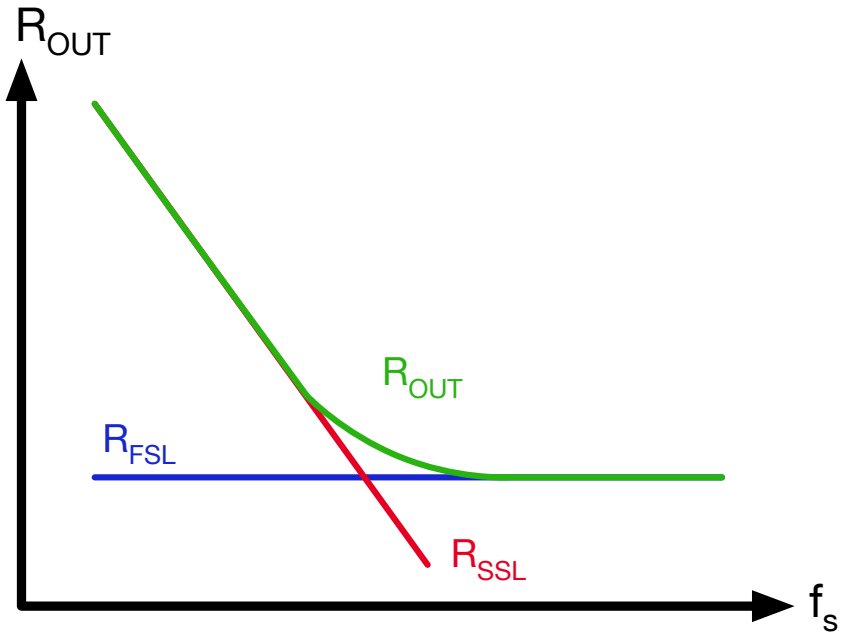


Figure 2.5. Output resistor R_{OUT} of a SC converter

converter is bounded by R_{SSL} at low switching frequency while limited to R_{FSL} at high switching frequency. This feature implies a narrow regulated output voltage range. Moreover, the efficiency drops quickly when the output voltage is away from the nominal value which is slightly lower than $M * V_{IN}$. Because a larger R_{OUT} and hence higher conduction loss is inevitable when the converter is regulated to lower output voltage, whereas a smaller R_{OUT} and hence worse switching loss is required for higher output voltage. A more completed loss analysis including the influence of bottom plate capacitors is given in [16]. The output voltage range problem can be alleviated by reconfigurable topology [16]. But it inevitably increases the complexity of the gate drivers and control logic.

2.3 Hybrid Converter

Intrinsically, R_{SSL} of an SC converter represents the total charge sharing loss of capacitors. To alleviate this type of loss, the most straightforward method is to add inductors in series with these capacitors during charging and discharging. Indeed, if the inductor is selected properly,

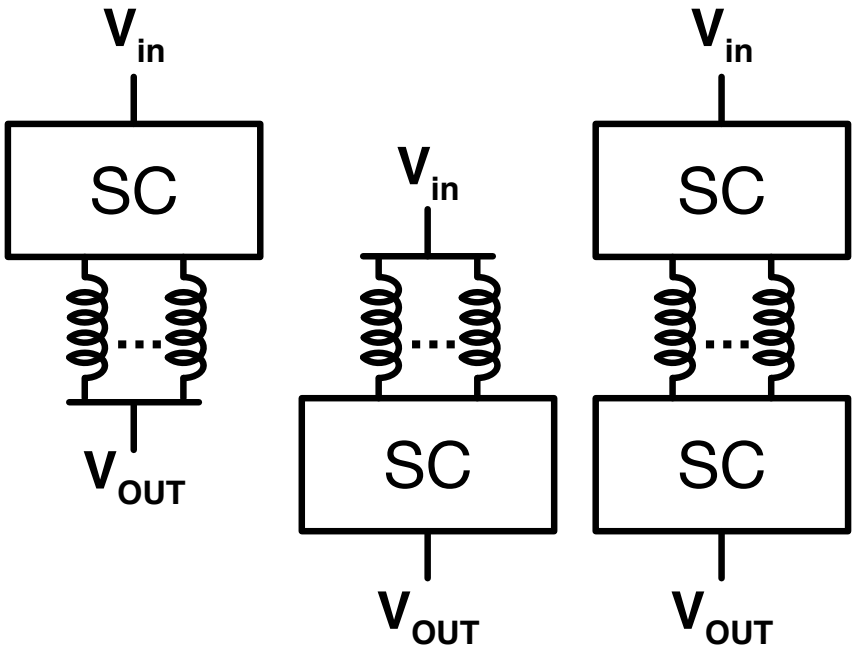


Figure 2.6. Various type of hybrid converter

the total loss would be reduced. No charge sharing loss would be observed and the current spikes during charging and discharging are limited. The term soft-charging is used to describe this circumstance. The converter with both inductor and capacitor is called hybrid converter, which has been demonstrated a good candidate for high-conversion-ratio and high-power-density applications in many publications [17, 28–30].

A hybrid converter can have three types of combinations as shown in Fig. 2.6. The first one is to place the inductor at the output, which is called inductor-last hybrid hybrid converter. The advantage of this type of arrangement is continuous output current and hence smaller output capacitor is required. The next one is to connect the inductor to the input, which is called inductor-first topology [31]. The benefit of this kind of connection is light inductor current. It's particularly suitable for step-down converter as the input current of it is less than the output one, so that less conduction loss on the inductor compared with putting the inductor at the output node. Emerging more recently, the last type is called inductor-middle hybrid converter [32]. As the inductor is away from high current output node, similar to the inductor-first topology, the

conduction loss is reduced. Meanwhile, the circuit can be reconfigured to different structures that provides wide output range without compromising performance.

In order to have a fair comparison between a hybrid converter and a conventional switched-inductor converter, let's only consider the inductor-last topology and assume they have the same switching frequency at the switching node and the same current ripple over the inductors, as well as the identical input and output voltages. Thus, for a n-level dickson-star hybrid converter [17] and a synchronous buck converter, their duty ratios and inductor voltages as well as the required inductance are listed in Table 2.1.

Table 2.1. Comparison between synchronous buck converter and n-level dickson-star hybrid converter

Topology	**Duty ratio**	**Voltage over inductor(s)**	**Inductance**
Buck	D	V_L	L
Hybrid (n-level)	$n*D$	$\frac{V_L}{n}$	L

From the well-know Steinmetz equation for calculating magnetic core loss,

$$P_{core} = V_{core} C_M f^{\alpha} \Delta B^{\beta} \tag{2.4}$$

the inductor loss for these two converters are the same, given the fact that ΔB, determined by volt*sec value, and switching frequency f are identical. In other words, using a hybrid topology won't reduce the volume of inductors. Nevertheless, the capacitors have three orders of magnitude higher energy per unit volume than a ferrite magnetic material [5], which means for a practical application, e.g. power supplies for servers, one hybrid converter can substitute multiple stages of conventional switched-inductor converters [17], in other words, it greatly reduces the usage of inductors.

To further decrease the inductor ripple and hence inductance value required, a multi-phase operation can be applied [18]. The detailed operation and its analysis as well as the experimental

results of this converter will be addressed in Chapter. 3.

2.4 Resonant Converter

Resonant converter can be viewed as a special case of a hybrid converter. The sinusoidal current and voltage help achieve Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS). As a matter of fact, a resonant converter can use very switching frequency without worrying about switching loss and hence passive components, especially magnetic devices, are miniaturized.

Traditionally, the magnetized or leakage inductance of a transformer resonates with an added capacitor. Even though the transformer provides the additional conversion ratio and isolation between input and output, which is crucial for high power applications such as data center power supplies and EVs, the dimension of the magnetic parts makes it difficult to be implemented onto size-limited applications such as mobile phones, USB-C chargers, *etc*.

Alternatively, inductors are inserted into conventional switched-capacitor converters to resonate with existing capacitors. One example is shown in Fig. 2.7 which combines 2:1 switched-capacitor converter with an resonant inductor. Despite the topology is identical to a 3-level buck converter, the resonant operation determines a different sinusoidal shape of the current and the voltage which helps achieving zero-voltage-switching (ZVS) and zero-current-switching (ZCS) and results in higher efficiency.

However, a successful soft-switching operation requires precise timing control. Moreover, similar to traditional transformer-included resonant converter, because inductance L and capacitance C are fixed so as the resonant frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$, the converter in Fig. 2.7 can't be regulated by varying frequency while achieving ZVS and ZCS similar to the traditional transformer-included resonant converters. But it's still a good candidate for fixed conversion ratio application [33].

Meanwhile, to gain the regulation capability of a resonant converter, many demonstrations

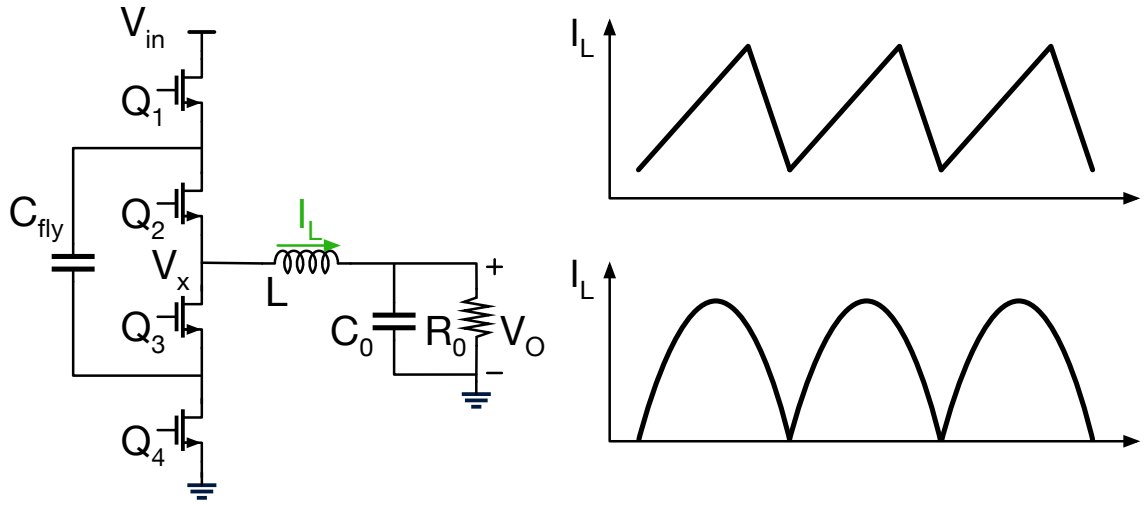


Figure 2.7. 3-level buck converter and its 1)inductive operation (top), 2)resonant operation (bottom)

have been published. The work in [8] has presented precisely on-time control which means modulating the time of resonant. However, the efficiency is therefore sacrificed. Another approach is adding a regulated converter stage to a fixed conversion ratio resonant converter stage. One good example is [34]. A multi-phase buck converter is plugged between input and the resonant stage. It has been proved an outstanding efficiency but as additional stage is added, more inductors are presented which offsetting the motivation of using a resonant converter.

Chapter 3

Multi-phase Dual-inductor Hybrid Converter

As discussed in Chapter. 2, the required inductor can't be reduced solely by replacing the conventional switched-inductor converter, e.g. buck converter, with a hybrid converter unless the effective switching frequency over the inductors is increased. Modified from the Dual-Inductor Hybrid (DIH) converter [35], rather than dual-phase operation, the Multi-Phase Dual-Inductor Hybrid (MP-DIH) converter [18] achieves 3x higher effective frequency on the inductors while reserves other benefits such as soft-charging, high conversion ratio, *etc*. In this chapter, the detailed operation and experimental results of it would be given.

3.1 Operation of MP-DIH Converter

The proposed MP-DIH converter operation can be applied to any DIH converter topology that has an even number of levels. The number of non-overlapped phases equals the number of the converter's levels (ignoring the zero level). In this work, a six-level version of the topology shown in Fig. 3.1 is demonstrated as a proof of concept. This 6-to-1 MP-DIH converter has two inductors L_{1-2}, five capacitors C_{1-5}, and eight switches S_{1-8}. Its operation can be explained using the illustrations of states and operational waveforms in Fig. 3.3. In State 1, a charge drawn from the input by C_1 and L_1 is stored in C_1. It is then sequentially transferred to C_2, C_3, C_4, and C_5 in other odd states with the operation of $L_1$and L_2. In each odd state other than State 1 and

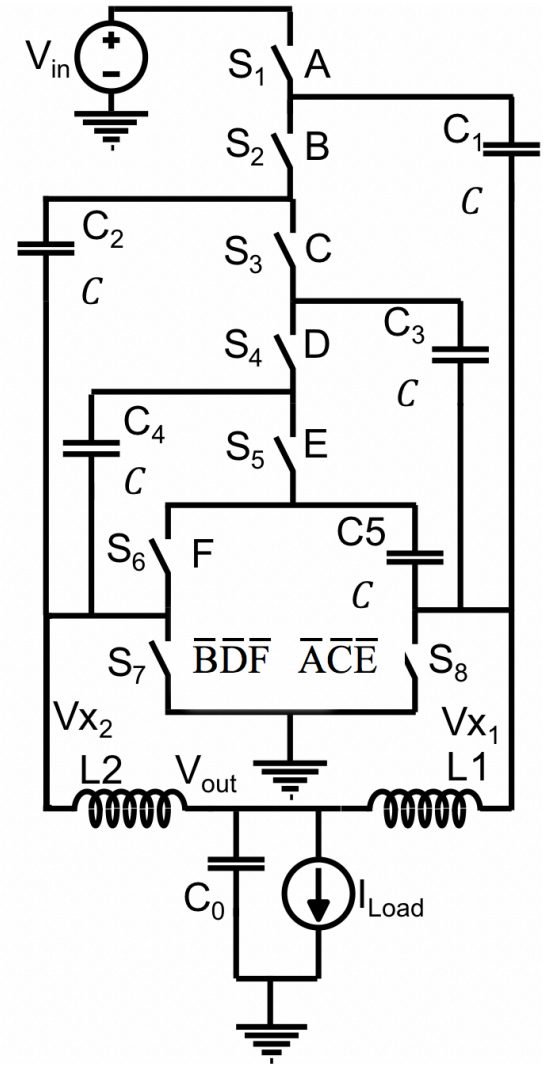
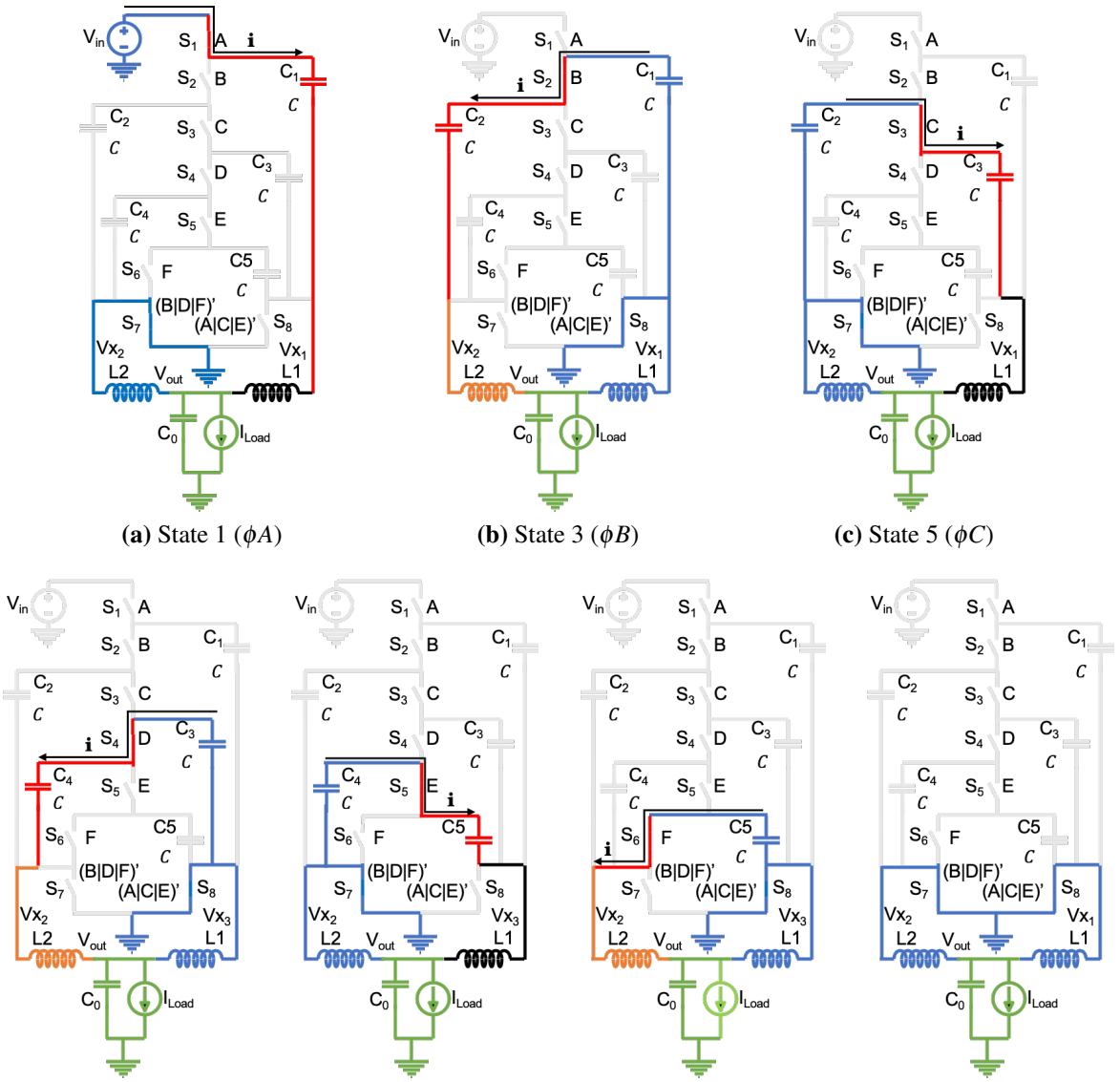


Figure 3.1. Topology of the Multi-Phase Dual-Inductor Hybrid (MP-DIC) converter

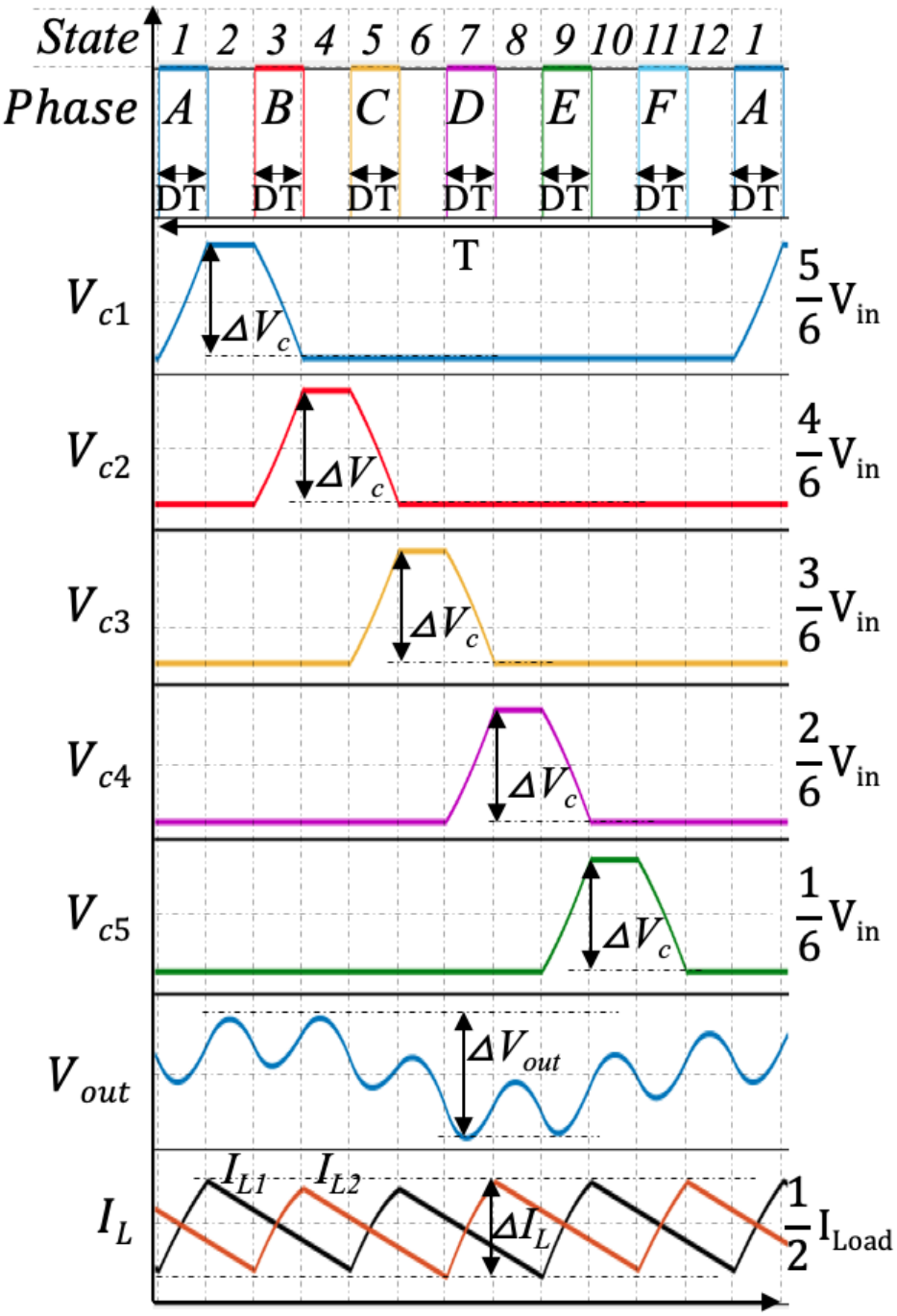
11, two capacitors and one inductor form a conducting branch where the inductor enables a soft charge transfer from the higher-level capacitor to the lower-level one, e.g. from C_1 to C_2 using L_1 in State 3. In State 1 and 11, C_1 receives the charge from the source and C_5 delivers the charge to the load, respectively. These odd states are also labeled as the six identical non-overlapped phases A-F evenly distributed over an operational cycle T. For even states, all the capacitors are



(a) State 1 (ϕA) **(b)** State 3 (ϕB) **(c)** State 5 (ϕC)

(d) State 7 (ϕD) **(e)** State 9 (ϕE) **(f)** State 11 (ϕF) **(g)** State 2, 4, 6, 8, 10, and 12

Figure 3.2. Operating states of the proposed MP-DIH converter



(a) Operational waveforms

Figure 3.3. Operational waveforms of the proposed MP-DIH converter

inactive and open-circuited. Inductor L_1 (L_2) free-wheels the stored charge to the output when S_8 (S_7) is activated during even states and during odd states when L_2 (L_1) is getting charged. The operational PWM signals, related capacitor voltage and inductor current ripple waveforms are shown in Fig. 3.3a.

To simplify the analysis on the steady-state voltages V_{C1} to V_{C5} of the capacitors C_{1-5}, we first assume small voltage ripples across the capacitors and inductor volt-second balance. Similar to a regular 6-to-1 Dickson SC converter, C_{1-5} have their steady-state voltages gradually decreased by $\frac{V_{in}}{6}$ from $V_{C1} = \frac{5V_{in}}{6}$ to $V_{C5} = \frac{V_{in}}{6}$. Switching nodes V_{X1} and V_{X2} swing from 0 to $\frac{V_{in}}{6}$ in states 1,5,9 and 3,7,11, respectively. Therefore, each inductor blocks only $\frac{V_{in}}{6}$ and is effectively switched at a frequency three times higher than that of S_{1-6}. This creates an opportunity to select an inductor of lower inductance, and thus lower equivalent series resistance (ESR) for the same size, while sacrificing switching loss for only $S_{7,8}$, i.e. $S_{7,8}$ is operated at 3X the fundamental switching frequency.

As can be seen in Fig. 3.5, on top of the high-frequency ripple, associated with switching nodes $V_{X1,2}$, $I_{L1,2}$ and V_{out} also have a low-frequency ripple at the operational frequency of the high-side switches, i.e. $\frac{1}{T}$. This phenomenon is caused by the different impedance and as a result, different voltage swing seen by the inductors in States 3, 5, 7, and 9 compared with States 1 and 11 [36]. Particularly, L_1 (L_2) only sees one capacitor C_1 (C_5) when it gets charged in State 1 (11), while in all other odd phases the inductors see two capacitors in series at switching nodes $V_{X1,2}$. Since the voltage swing difference created by equivalent capacitor mismatch only causes a small predictable perturbation in the fundamental operations of the converter, it does not alter either the charge balance of C_{out} and C_{1-5} or the volt-second balance of the inductors achieved in the entire period.

General steady-state values of the output and flying capacitor voltages for an MP-DIH converter are given as:

$$V_{out} = \frac{DV_{in}}{2} \quad \text{and} \quad V_{C_k} = \frac{(N-k)V_{in}}{N} \tag{3.1}$$

where, k=1, 2,...., N-1

One can calculate from this analysis that for an N-level N-phase operation, the maximum duty cycle D is limited to $\frac{1}{N}$ due to non-overlapping phase distribution. In other words, the conversion ratio $\frac{V_{in}}{V_{out}}$ is limited to $2N$. However, the converter is still capable of supporting a wide range of conversion ratios from a 40V-54V input supply to an output voltage up to 3.33V-4.5V, covering the 1V-2V range typically required in data center and telecommunication systems. It is also noted that, for the same voltage conversion ratio as a three-level Buck converter the voltage stress across each high-side switch of the MP-DIH converter is $\frac{2V_{in}}{N}$, significantly lower than the three level Buck converter's switch stress of $\frac{V_{in}}{2}$ [37–39]. This difference brings advantages in both switching loss and conduction loss, i.e. allowing switches with lower breakdown voltage and on resistance, promising a higher efficiency for a larger conversion ratio.

Table 3.1. Parts List

Item	Design Selection
Flying Capacitors C_{1-5}	2.2, 1.5, 1.5, 1, 1μF, X7R, 1812/1210, TDK
Output Capacitor C_0	6.8μF, X5R, 0603, 10V, TDK
Inductors L_1, L_2	1.5μH, IHLP-5050CE-01
High Side Switches, S_{1-6}	EPC2014C
Low Side Switches, $S_{7,8}$	EPC2023
$S_{7,8}$ Paralleled Diodes, $D_{7,8}$	CRS08, 30 V, 1.5 A
Gate Drivers	LM5113, LM5114
Signal Isolators	Si8422, Silicon Labs
Microcontroller	TMS320F28377 Delfino, TI

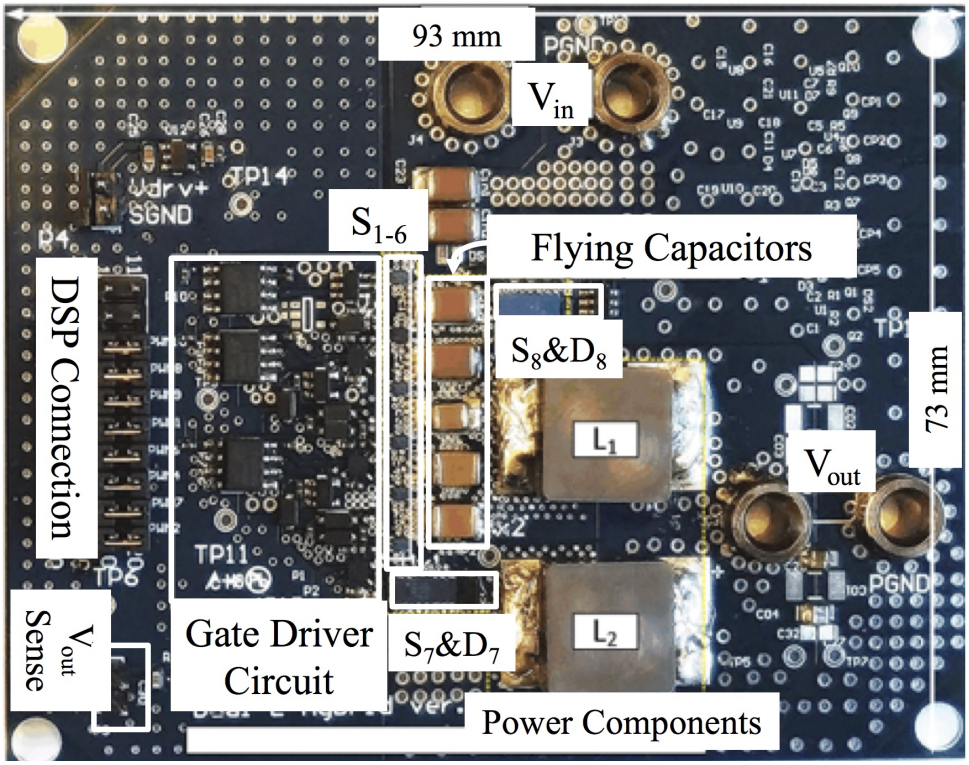


Figure 3.4. Prototype Board

3.2 Experimental Results

To verify the feasibility of this novel topology and operation, a 48V 20W prototype has been implemented using the components listed in Table 3.1. With a switching frequency of 150 KHz applied to S_{1-6} , $S_{7,8}$ and $L_{1,2}$ are switched effectively at 450 KHz, as described in Section 3.1. The operational waveforms of I_{L1}, I_{L2}, V_{X1}, V_{X2}, and V_{out} are captured in Fig. 3.5, while capacitor voltages V_{C1-5} for one operational cycle with 12 states shown in Fig. 3.6. These measured waveforms verify intended converter operations and analysis of Section 3.1.

As shown in Fig. 3.7 and Fig. 3.8, the converter is also demonstrated to maintain efficiency higher than 90% over most of the 1A-8A load range for wide ranges of input voltages, 40V-54V, and output voltages, 1.4V-2V, with a peak efficiency of 92.4% at 40V-1.8V/4A and 92.1% at 48V-1.8V/4A.

At a mid load of 4A for 48V-to-1.8V conversion, the converter is analyzed to have switch-

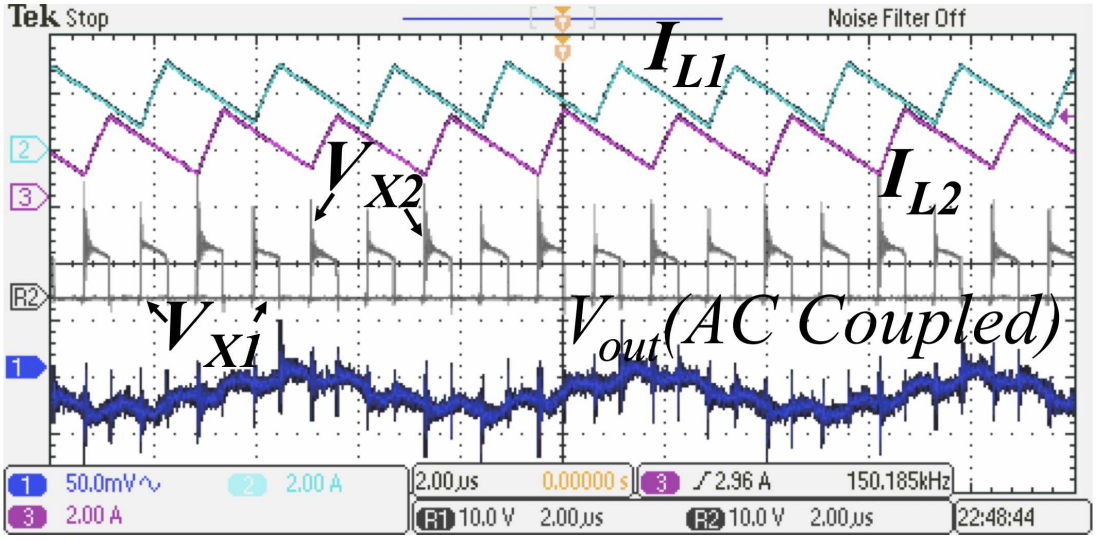


Figure 3.5. Operational waveforms of prototype at 48V-1.8V/4A.

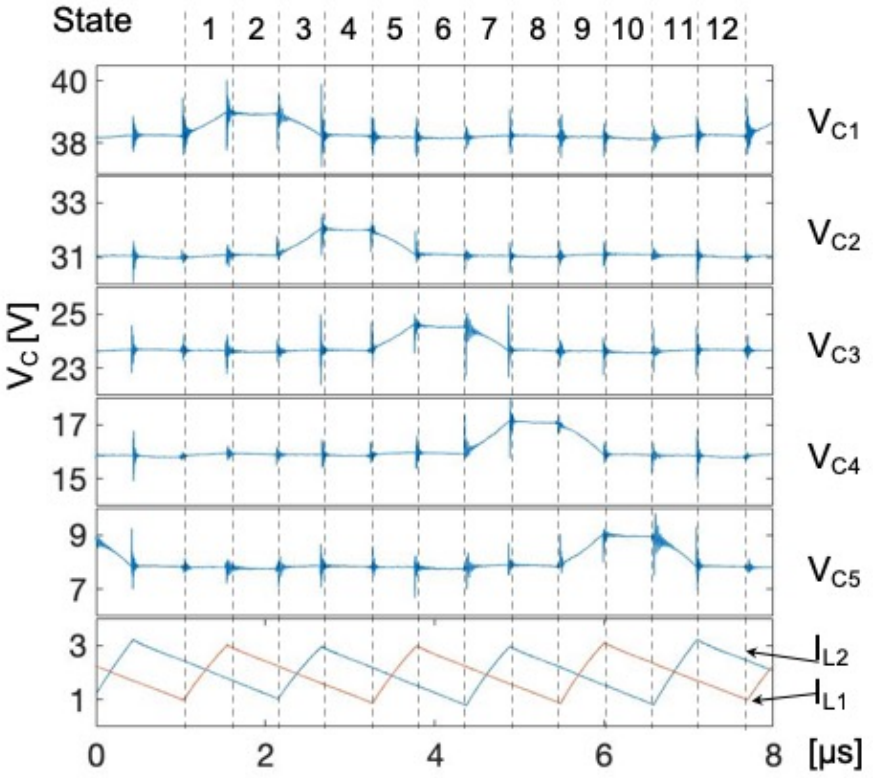


Figure 3.6. Flying capacitor voltage with no hard-charging.

ing loss, magnetic component loss, conduction loss and non-ideal parasitic loss of 40%, 37%, 20%, and 3%, respectively, as given in the Fig. 3.9. It can be concluded that to further increase the

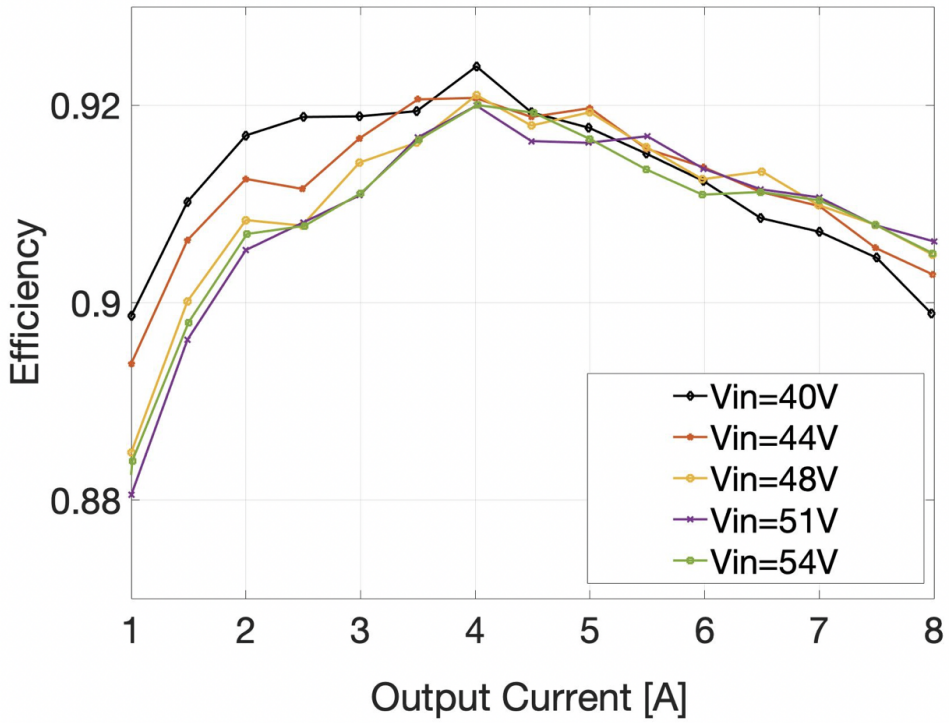


Figure 3.7. Measured efficiency for different input voltages at $V_{out} = \mathbf{1.8V}$ regulated

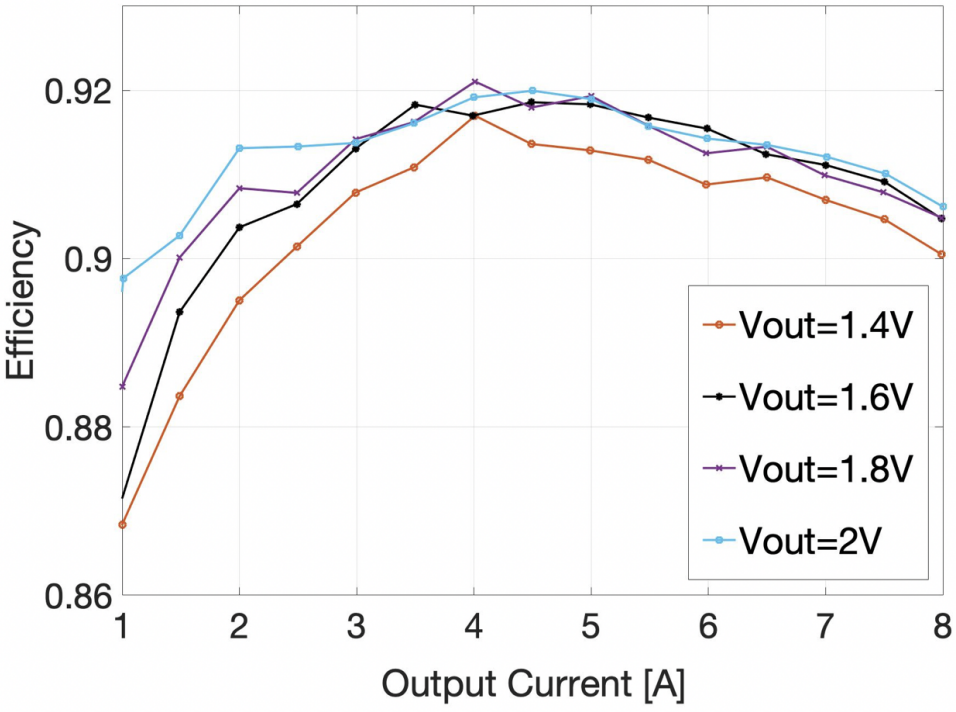


Figure 3.8. Measured efficiency for different output voltages at $V_{in} = \mathbf{48V}$regulated

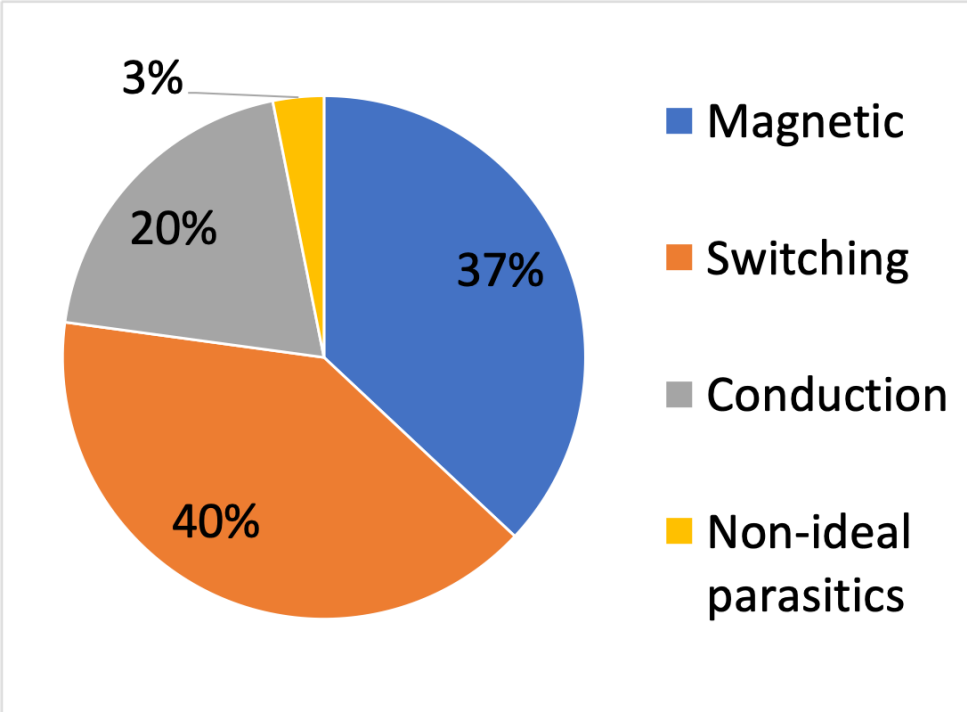


Figure 3.9. Loss breakdown at 1.8V/4A output

efficiency of this Multi-Phase Dual Inductor Hybrid (MP-DIH) converter, a customized and more optimized inductor design is required. Moreover, a soft-switching approach and discontinuous conduction mode (DCM) operation are necessary for better efficiency at light load operations.

3.3 Summary

In this chapter, a multi-phase hybrid converter, namely Multi-Phase Dual-Inductor Hybrid (MP-DIH) converter is proposed. With multi-phase operation, the effective frequency over the output inductors is 3 times higher leading to smaller inductors. While retaining the benefits of using a Dickson-Star hybrid converter, such as high conversion ratio, soft-charging of flying capacitors, the multi-phase operation has also been proved to gain the robustness on the flying capacitor mismatch. A demonstration PCB has been made to show the experimental results. The peak efficiency was captured at 40 V-1.8 V/4 A with a number of 92.4 %.

3.4 Acknowledgements

This chapter, in full, is a reprint of the material as it appears in 2019 IEEE Applied Power Electronics Conference and Exposition (APEC). Tianshi Xie; R. Das, G.-S. Seo, D. Maksimovic, and H.-P. Le, “Multiphase Control for Robust and Complete Soft-charging Operation of Dual Inductor Hybrid Converter,” APEC 2019. The dissertation author was the primary investigator and author of this paper.

Chapter 4

Soft-switching Assisted by Additional Circuitry

Introduced in Chapter. 2, the volume of inductors and hence the overall system size can be shrinked if operating the converter at a higher switching frequency. However, this comes with the penalty of higher switching loss. To alleviate it, several methods including variable frequency, BCM operation and auxiliary circuit assisted ZVS have been published. Among them, the last one is the most applicable approach as it requires no complexity circuit for tuning frequency and maintains the acceptable current ripple. But the current solutions don't have sophisticated timing control and therefore lots of charge have been wasted.

Alternatively, a new topology named Zero-Voltage-Switching 3-Level Buck (ZVS-3LB) converter, shown in Fig. 4.1, is proposed. A small auxiliary circuit is added to a 3LB converter to achieves full ZVS for both high-side and low-side switches. Because the significant reduction of switching loss, the converter can operate at Mega-Hertz switching frequency, while maintaining $> 92.2\%$ efficiency at light load. In Section. 4.1, the detailed operation principle is introduced. The design considerations are discussed in Section. 4.2. In Section. 4.4, the experimental results are given. And the paper is concluded in Section. 4.6.

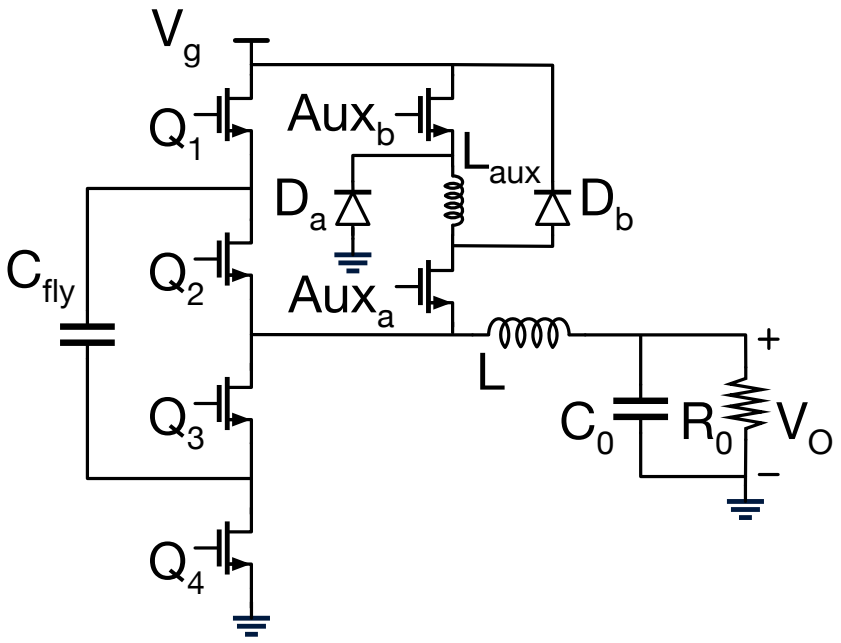


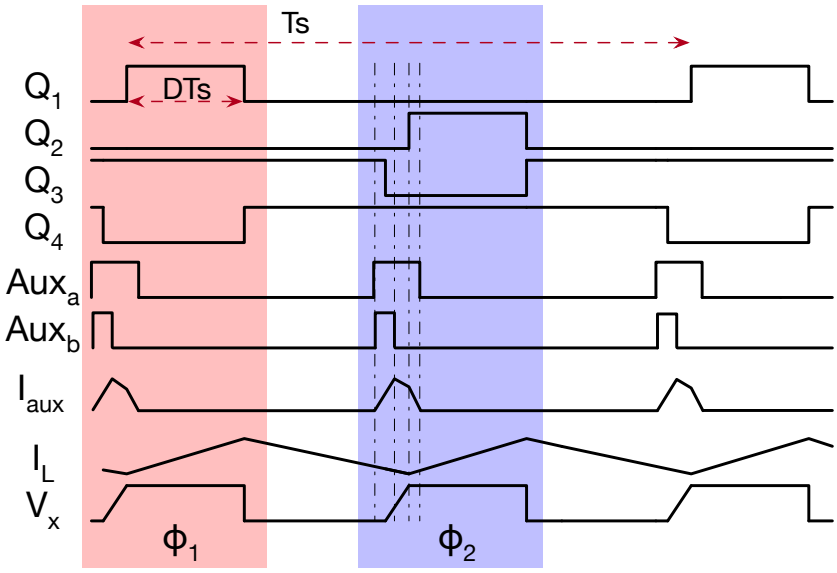
Figure 4.1. The proposed Zero-Voltage-Switching 3 Level Buck (ZVS-3LB) converter schematic

4.1 Topology and Operation of the ZVS-3LB Converter

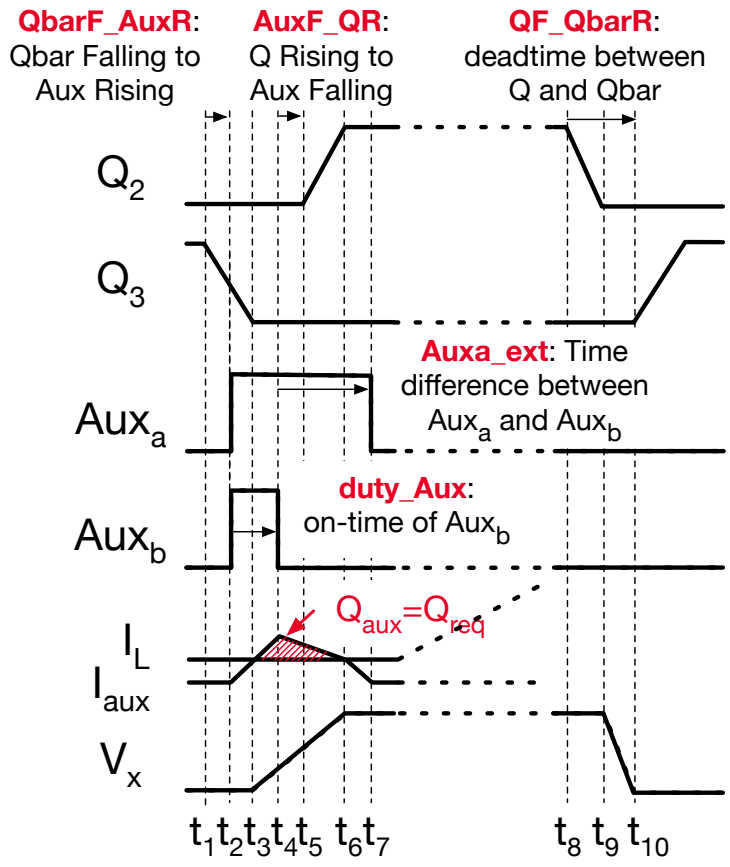
The proposed ZVS-3LB converter is constructed by adding an auxiliary circuit to the conventional 3LB converter. As shown in Fig. 4.1, the auxiliary circuit contains two N-type transistors Aux_a & Aux_b, two diodes D_a & D_b, and one small inductor L_{aux}. The presence of the auxiliary circuit is to provide additional charge for soft-switching when High Side (HS) switches, namely Q_1 and Q_2, turn on.

The complete operation of the proposed converter is depicted in Fig. 4.2(a) where the ZVS parts are highlighted for Φ_1 and Φ_2. Because the auxiliary circuit operates the same in Φ_1 and Φ_2 to softly turn-on Q_1 and Q_2. The operation details during Φ_2 with all time intervals of the ZVS operation are presented in Fig. 4.2(b) and explained below, while Fig. 4.3 shows the status of main power switches Q_1-Q_4 corresponding to the time intervals during both Φ_1 (in red) and Φ_2 (in blue).

- Before t_1: Only Low Side (LS) switches Q_3&Q_4 are on. The auxiliary circuit is inactive.



(a) Full operation



(b) Zoomed-in ZVS operation during Φ_2

Figure 4.2. Operation principle of the proposed ZVS-3LB converter.

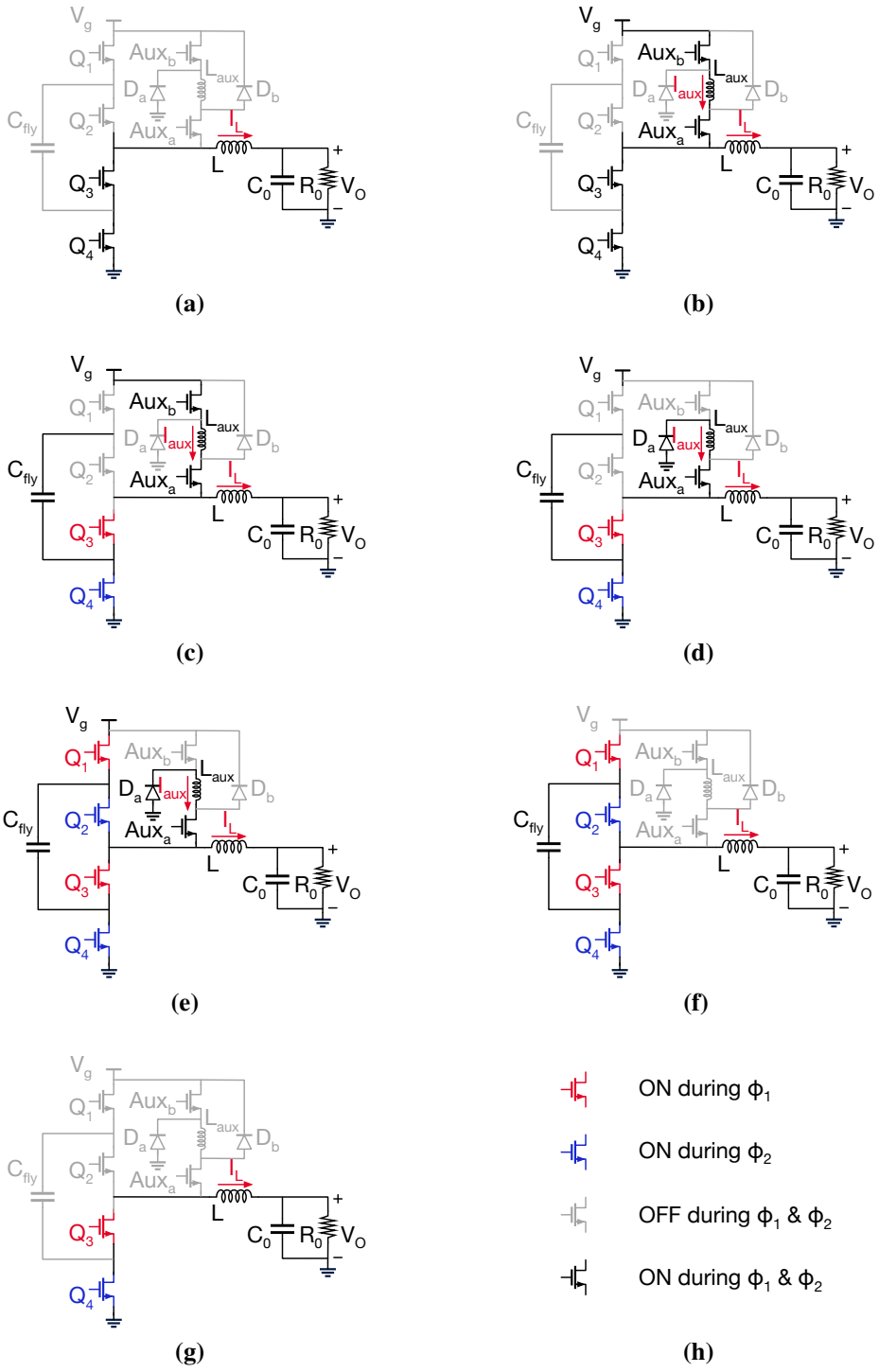


Figure 4.3. Key operation states of the proposed ZVS-3LB converter during the time interval: (a) before t_2, (b) $t_2 \sim t_3$, (c) $t_3 \sim t_4$, (d) $t_4 \sim t_6$, (e) $t_6 \sim t_7$, (f) $t_7 \sim t_9$, (g) $t_9 \sim t_{10}$

- $\underline{t_1 \sim t_2}$ (Fig. 4.3(a)): one of the LS switches (Q_3 or Q_4) is turning off. Since it has not been fully off yet, the auxiliary circuit remains hibernated to avoid flowing extra charge to the ground.

- $\underline{t_2 \sim t_3}$ (Fig. 4.3(b)): Despite the LS switch is not completely off yet, L_{aux} must be magnetized in advance so as to ramp its current I_{aux} to I_L at the rate of $\frac{V_g}{L_{aux}}$. When $I_{aux} > I_L$, the extra charge starts flowing into the switching node once the LS switch is off at t_3.

- $\underline{t_3 \sim t_4}$ (Fig. 4.3(c)): As the LS switches are off, the additional charge resulted from $(I_{aux} - I_L)$ is transferred to the switching node parasitic capacitor C_x. Aux_b is turned off at the end of this time interval since L_{aux} is sufficiently magnetized for completely soft-switching of the HS switches.

- $\underline{t_4 \sim t_6}$ (Fig. 4.3(d)): The free-wheeling diode D_a conducts, leading to ramping down of I_{aux}. Since $I_{aux} > I_L$, C_x is continuously soft-charged until the HS switch is completely on at t_6. The extra charge from the auxiliary circuit for soft-switching one HS switch is given by

$$Q_{aux} = \int_{t_3}^{t_6} (i_{aux} - i_L)\, dt \tag{4.1}$$

  And the total charge required for ZVS is

$$Q_{req} = Q_{oss,HS}(HS\,switch) + Q_{oss,LS}(LS\,switch). \tag{4.2}$$

  To exhaust Q_{aux} for ZVS HS switches and to minimize power loss, $Q_{aux} = Q_{req}$ is desired.

- $\underline{t_6 \sim t_7}$ (Fig. 4.3(e)): The I_{aux} continues ramping down to zero at the rate of $\frac{V_g}{2L_{aux}}$. Note that $V_{Cfly} = \frac{V_g}{2}$.

- $\underline{t_7 \sim t_9}$ (Fig. 4.3(f)): Aux_a turns off at zero current putting L_{aux} into inactive status again. The rest of the circuit operates the same as a conventional 3LB converter. The presence of D_b helps reduce current ringings during auxiliary circuit inactive states.

- $\underline{t_9 \sim t_{10}}$ (Fig. 4.3(g)): The HS switches are completely off letting I_L fully discharge switching node parasitic capacitor. As a result, the LS switch will be zero-voltage switched on.

4.2 Design Consideration of the ZVS-3LB Converter

A careful analysis and selection of auxiliary circuit devices are necessary to achieve the efficiency benefit from ZVS operation. The auxiliary circuit will reduce the main circuit switching loss by

$$P_{sw,redu} = 2\left(\frac{C_{oss}}{2}(\frac{V_g}{2})^2 + \frac{V_g}{2}I_L t_{on} + Q_{rr(LS)}\frac{V_g}{2}\right)f_s \tag{4.3}$$

where C_{oss}, t_{on} and $Q_{rr(LS)}$ are HS switches output capacitance, turn-on time, and LS switches body diode reverse recovery charge, respectively. Meanwhile, the auxiliary circuit incurs additional power loss, namely $P_{tot,aux}$, which can be divided into conduction loss $P_{con,aux}$, switching loss $P_{sw,aux}$ and inductor loss P_{Laux}.

4.2.1 Auxiliary Circuit Conduction Loss

When computing conduction losses, it can be assumed that I_{aux} rises from t_2 to t_4 and falls from t_4 to t_7 at constant rates of $k_r = \frac{V_g}{L_{aux}}$ and $k_f = \frac{V_g}{2L_{aux}}$, respectively, for simplicity. Thus, (4.1) becomes

$$Q_{aux} = 0.5\left((t_r - \frac{I_L}{k_r}) + (t_f - \frac{I_L}{k_f})\right)(k_r t_r - I_L) \tag{4.4}$$

where t_r is the time duration from t_2 to t_4 and t_f represents the time duration from t_4 to t_7. Apparently, $t_f = 2t_r$. On the other hand, $Q_{aux} = Q_{req}$ is required. Therefore, the relation between t_r and Q_{req} can be derived as

$$t_r = \sqrt{\frac{2Q_{req}}{3k_r}} + \frac{I_L}{k_r} \tag{4.5}$$

Then, the conduction loss of the auxiliary circuit can be computed by

$$\begin{aligned} P_{con,aux} &= \frac{I_{pk}^2}{3}(R_{on,a}+R_{on,b})t_r f_s + \frac{I_{pk}^2}{3}R_{on,a}t_f f_s \\ &= \frac{{k_r}^2 {t_r}^3}{3} f_s (3R_{on,a}+R_{on,b}) \end{aligned} \tag{4.6}$$

where I_{pk} is the peak value of I_{aux}, $R_{on,a}$ and $R_{on,b}$ are the on-resistance of the switches Aux_a and Aux_b, respectively. Interestingly, the conduction loss of the auxiliary circuit has strong relation with the switching frequency f_s which is not very common in PWM controlled switched-inductor converters. This is simply because Q_{req}, which is only determined by the devices, doesn't change along with f_s. And to achieve fully soft-switching in a faster switching converter, the auxiliary circuit has to be activated more frequently which resulting in higher average conduction loss. Moreover, plugging (4.5) into (4.6) would help better understand the relation between $P_{con,aux}$ and L_{aux}. To simplify, let's assume one converter, which means fixed on-resistance of the switches, operating at a constant f_s.

$$P_{con,aux} \propto \sqrt{k_r}\left(\sqrt{\frac{2}{3}Q_{req}} + \frac{I_L}{\sqrt{k_r}}\right)^3 \tag{4.7}$$

By analyzing (4.7), it can be observed that for each set of I_L and Q_{req}, a minimum conduction loss can be approached by varying L_{aux}, which is inversely proportional to k_r. From Fig. 4.4(a), it can be summarized that a higher I_L or output current would require a smaller L_{aux} to achieve the corresponding minimum auxiliary circuit conduction loss. Meanwhile, a greater Q_{req}, which means larger main switches of 3LB converter, requires a higher value of auxiliary inductor, as implied in Fig. 4.4(b).

4.2.2 Auxiliary Circuit Switching Loss

As the auxiliary switches are all small, the switching time is short. Besides, the auxiliary switches are switched at zero current. As a result, the auxiliary circuit switching loss is dominated

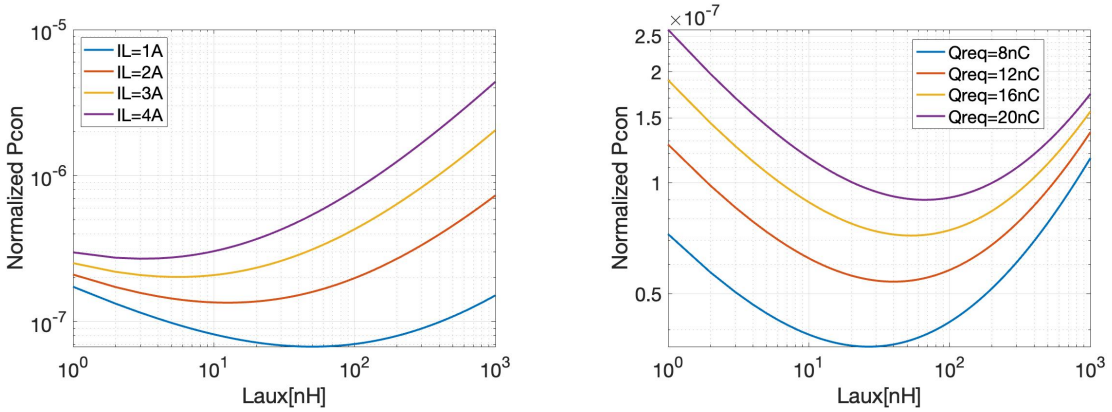


Figure 4.4. Normalized auxiliary circuit conduction loss vs. L_{aux} at different: (a) output inductor current I_L, (b) required charge Q_{req} for soft-switching.

by output capacitance and reverse recovery charge ($Q_{rr,aux}$) of D_a and D_b, given by

$$P_{sw,aux} \approx 2\left(C_{oss,aux}(\frac{V_g}{2})^2 + Q_{rr,aux}\frac{V_g}{2}\right)(2f_s) \tag{4.8}$$

The expression indicates trade-off between auxiliary circuit switching loss and conduction loss just like other switch mode power converters. To achieve the most optimized efficiency, the total loss of the auxiliary switches must be considered.

4.2.3 Auxiliary Inductor Loss

In general, inductor loss can be estimated by the summation of copper loss, which is determined mostly by the winding resistance, and core loss, which is related to switching frequency of the converter.

$$P_{Laux} = P_{cu}(Copper\,loss) + P_{core}(Core\,loss) \tag{4.9}$$

The copper loss is computed by

$$P_{cu} = I_{aux,rms}^2 (R_{ac} + R_{dc}) \tag{4.10}$$

Where the ac resistance R_{ac} and dc resistance R_{dc} can usually be found in the data sheet of a commercial inductor or be calculated by the winding parameters if it is customized designed.

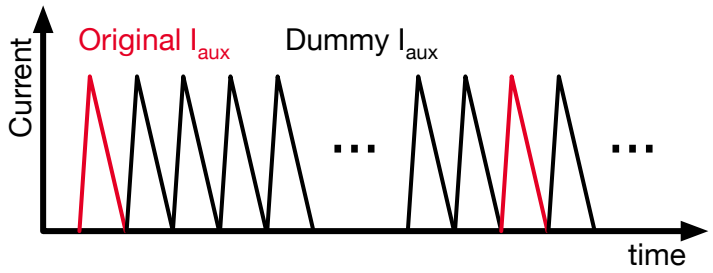


Figure 4.5. Convert pulsed current into continuous sawtooth current for convenient core loss estimation

The modeling of the core loss is however tricky as the current going through is not continuous. One easy approach to calculate its core loss is to convert it to a continuous triangle-shape current with switching frequency of $f_{aux} = \frac{1}{t_r + t_f}$ as sketched in Fig. 4.5. Its core loss can be modeled by using the provided data from the inductor vendor and the iGSE method described in [40] after determining the peak flux density ΔB which can be written as $Volt \cdot Sec$ expression $V_g t_r$. The rising time t_r is approximated as one third of the auxiliary current period $\frac{1}{3 f_{aux}}$. Then, the actual core loss is the calculation value from the continuous current divided by the number of repeating cycles $N = \frac{f_{aux}}{f_s}$. Thus, the actual core loss is given by

$$\begin{aligned} P_{core,aux} =& \frac{V_{core} C_M {f_{aux}}^{\alpha} \Delta B^{\beta}}{N} \\ =& V_{core} C_M {f_{aux}}^{\alpha - 1 - \beta} (\frac{V_g}{3})^{\beta} * f_s \end{aligned} \tag{4.11}$$

where V_{core} is the core volume and C_M, α and β is from fitting data. For a typical ferrite material, α is in a range of 1.4-2.0, while β is within 2.4-3.0 [13]. That being said, the term ${f_{aux}}^{\alpha - 1 - \beta}$

is always reversely proportional to f_{aux}. Therefore, when optimizing the auxiliary circuit for a given 3LB converter, a higher f_{aux} would result in less core loss if assuming the same core is used.

An optimization flow is created using the loss calculations above. To achieve the goal of improving efficiency, the total loss of auxiliary circuit $P_{tot,aux}$ must be smaller than the reduced switching loss $P_{sw,redu}$ of main circuit. As shown in the loss breakdown graph in Fig. 4.10(a), this can be achieved with load currents smaller than 1.7 A.

4.3 System Design

The system design of the proposed ZVS-3LB converter is critical as the auxiliary circuit is sensitive to tiny timing change which fails the fulfillment of (4.2) and thus leads to unexpected power loss.

To control the timing in a closed-loop manner, one example of the system configuration can be set as Fig. 4.6 shown. First of all, the switching node voltage must be sensed. The soft-switching sequence is initialized at t_2 when both Aux_a and Aux_b are turned on. Reset of Q_3 is upon sensing of the switching node voltage V_x and comparing it with zero voltage. Ideally, Q_3 is turned off at t_3 when I_L equals to I_{aux}, which means $V_x = 0$. Here, the turn-on/off time of the switches is ignored for simplification of the description. In reality, to guarantee Q_3 is off at the time t_3, the control signal of it has to be pulled down before t_3. The set of Q_3 is based on zero voltage sensing at t_{10} and the circuit design is not shown. The set of Q_2 happens when V_x reaches zero slope at t_6 as it means $I_L = I_{aux}$ and no charge current flows into the switching node. Once the zero-slope point is found, a comparision will be conducted between V_x and half V_g. When $V_x > \frac{V_g}{2}$, abundant Q_{aux} is generated and therefore a $Delay-$ signal is triggered. And vice versa. After going through an integrator and a voltage-controlled delay block, a reset signal R_b will determine the falling edge of Aux_b. While the set of both Aux_a and Aux_b is generated from zero-current detection (ZCD) of I_{aux}.

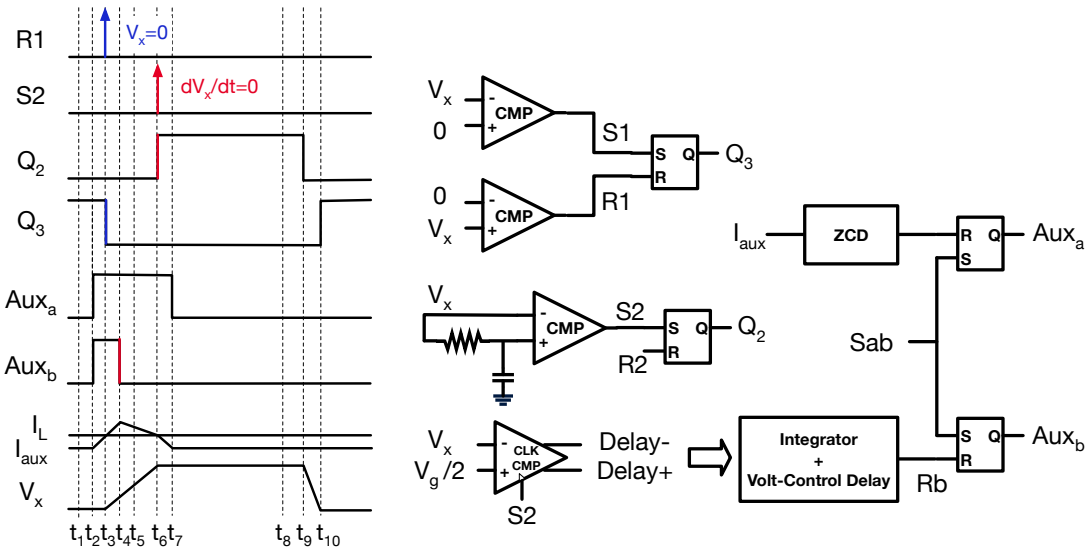


Figure 4.6. An example of closed-loop design

From the control loop diagram shown above, it's obviously that the success of the closed-loop control, and thus the efficiency of the converter, is a result of precise sensing. From (4.5), the rising time of L_{aux} can be derived as 3.25 ns if assuming 15 V input voltage, 1 A load current, 10 nH L_{aux} and 15 nC Q_{req}. However, sub-ns window of sensing on PCB is apparently very difficult. As a consequence, the soft-switching timing including the status of the auxiliary circuit is controlled in an open-loop manner.

In addition, as for a 3-level buck converter, there is always a balancing issue along with the flying capacitor [41]. Therefore, while the output voltage is modulated by varying duty cycles of Q_1 and Q_2, the flying capacitor voltage is balanced by changing their difference [41]. Due to the aforementioned voltage and current sensing difficulty, the timing for soft-switching function together with output voltage regulation as well as flying capacitor voltage balancing is determined by parameter sweeping. The timing for all the signals displayed in Fig. 4.2 can be broken down into the time delay parameters listed in Table. 4.1. To exhaustively sweep these parameters and to capture the optimized soft-switching operation, an FPGA board ADC-SOC from Terasic with designed embedded system based on NiosII is employed. This complete automation system, as sketched in Fig. 4.7, formed by the FPGA board, ZVS-3LB demonstration

board, testing equipments, remote desktop and a control program in Matlab, all connected to a PC, is designed to accomplish over 3000 groups of data searching within one hour. Each data group contains a set of control parameters and measured performance of the converter. Thus, the optimized points are found and the results are presented in Section. 4.4. The resulted parameter values are listed in Table. 4.2. The parameter sweeping is based on different load currents. Since it's open-loop, the output voltage must be kept consistently 4 V in order to have a fair comparison between ZVS-3LB converter and conventional 3LB converter. Because the minimal time duration of 1 bit is translated into 5 ns, at some load current, V_o is hard to well-regulated to desired voltage, e.g 4 V. But the same output voltage is achieved for performance comparison between topologies. Please also be noted, the duty ratios of Q_1 and Q_2 are different due to flying capacitor balancing requirement as discussed above. This duty ratio difference is also programmed. As a result of the 5 ns minimum time step set by the maximum counter clock frequency on FPGA, the minimum load current where the timing of auxiliary circuit is optimized is 0.7 A. It can be seen that the duty ratio of Aux_b is 1 bit which is 5 ns. As the load current increases, the number of bits accumulates but with 5 ns step. Consequently, the load current set for measurement has to follow this step. It's impossible to capture the optimized timing between the load currents shown in the table.

Table 4.1. Parameters to define time delay.

Parameters	**Delay from**	**To**
QbarF_AuxR	Falling edge of Qbar	Rising edge of $Aux_{a,b}$
duty_Aux	Rising edge of Aux_b	Falling edge of Aux_b
AuxF_QR	Falling edge of Aux_b	Rising edge of Q
Auxa_ext	Falling edge of Aux_b	Falling edge of Aux_a
QF_QbarR	Falling edge of Q	Rising edge of Qbar

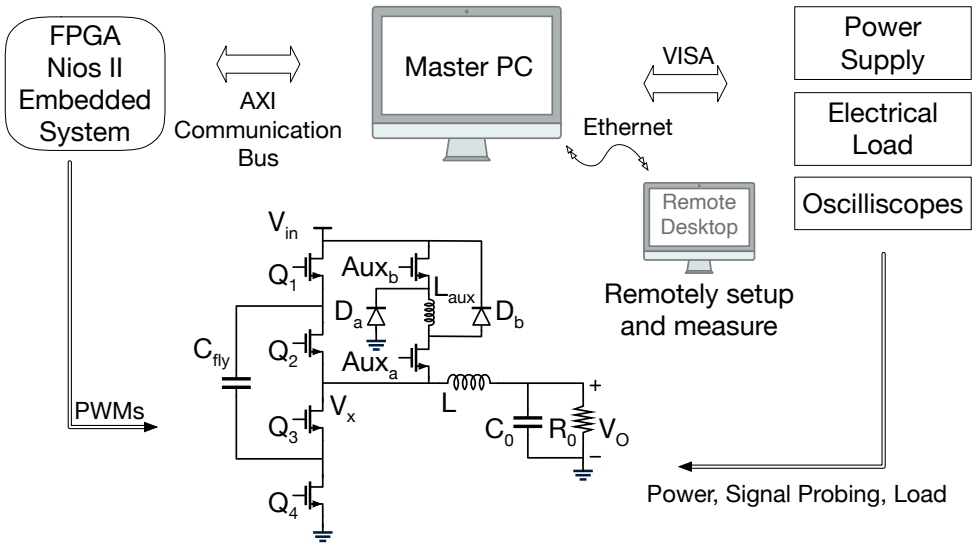
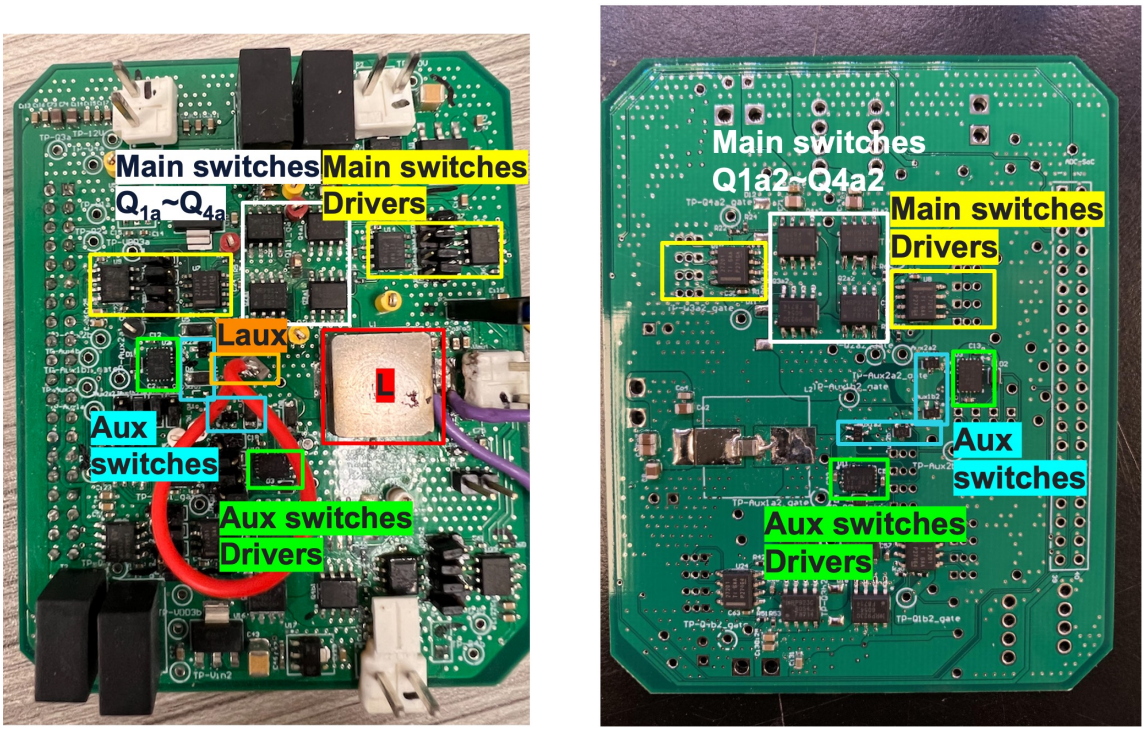


Figure 4.7. The testbench for ZVS-3LB converter demonstration



(a) **(b)**

Figure 4.8. Prototype of the proposed ZVS-3LB converter: (a) front side, (b) back side.

Table 4.2. Parameters setup at various load.

	Numbers					Comments
I_L	0.7A	1A	1.6A	2A	2.5A	Where integer number of Duty_Aux provides required Q
V_g	15V	15V	15V	15V	15V	
V_o	4.38V	3.99V	3.98	4.07	4.09	Output voltage points where Vc is balanced
Eff. of ZVS-3LB	92.33%	92.2%	92.33%	91.99%	90.84%	Efficiency of ZVS 3LB
Eff. of 3LB only	89.4%	91.66%	93.31%	93.84%	94.39%	Efficiency of normal 3LB with the same Vo
duty ratio	0.525	0.47	0.475	0.505	0.505	
∆d	0.035	0.02	0.015	0.005	0.005	Q1 duty = duty+∆d; Q2 duty = duty-∆d;
Duty_Aux3	1	2	3	4	5	For the edge ZVS Q2. t=n*5ns, 5ns is the resolution.
Duty_Aux1	1	2	3	4	6	For the edge ZVS Q1
QbarF_AuxR3	3	2	1	0	-1	Q3 falling edge to Aux rising edge. ZVS Q2
QbarF_AuxR1	3	2	1	0	-1	Q4 falling edge to Aux rising edge. ZVS Q1
AuxF_QR3	4	4	4	3	3	Aux falling to Q2 rising
AuxF_QR1	6	6	6	6	5	Aux falling to Q1 rising
Auxa_ext1	6	12	15	20	25	On-time of Auxa minus on-time of Auxb at ZVS Q1 edge
Auxa_ext3	6	12	15	20	25	On-time of Auxa minus on-time of Auxb at ZVS Q2 edge

Table 4.3. Key components

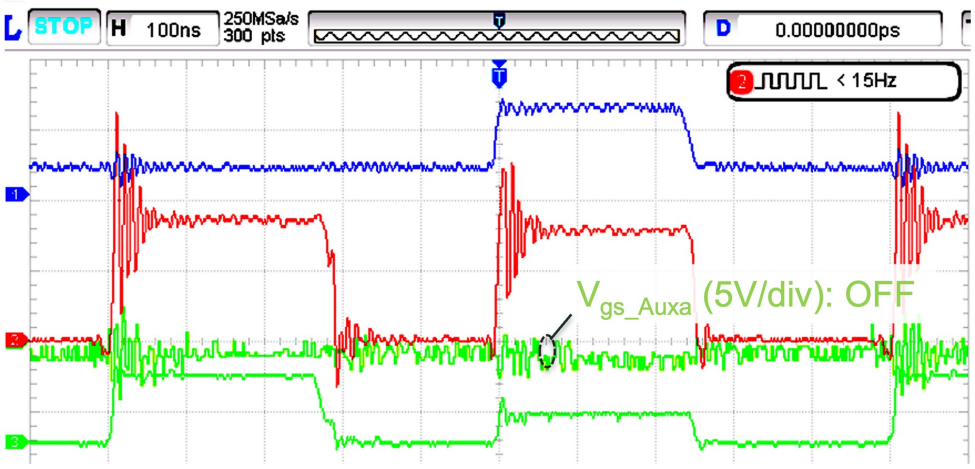
Components	Details
L	IHLP-5050 (1.5 μH)
L_{aux}	IHLP1616BZ (100 nH)
C_{fly}	4 μF
Q_1-Q_4	IRF8714 $\times$ 2 (4 mΩ)
Aux_a, Aux_b	PMF250XNE $\times$ 2 (127 mΩ)
D_a, D_b	CRS01
Main switches gate driver	UCC27201
Auxiliary switches gate driver	LMG1210
Controller	Terasic ADC-SOC FPGA

4.4 Hardware and Experimental Results

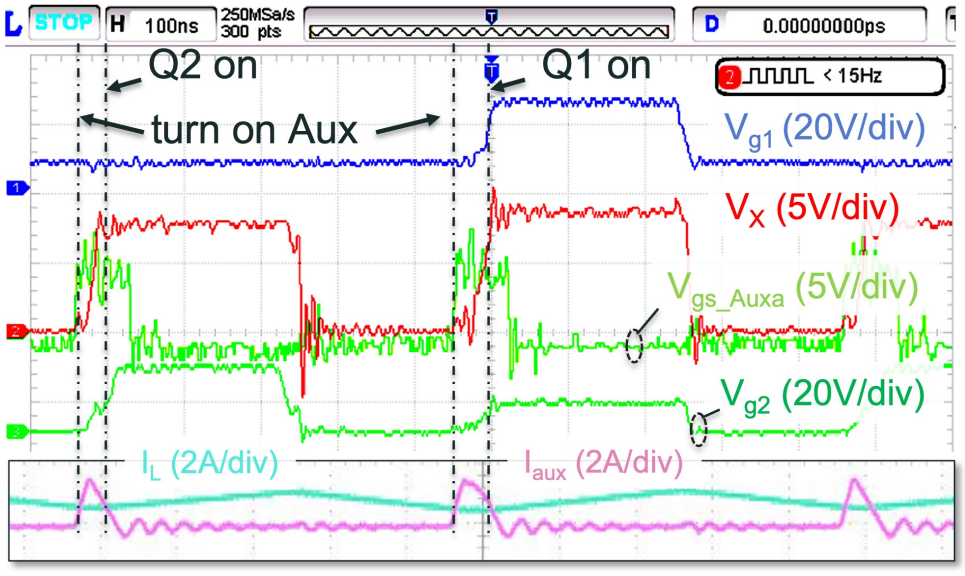
As a result of the optimization described in Section. 4.2, the selection of each device is listed in Table. 4.3. Particularly, auxiliary inductor L_{aux} is only 100 nH, which is ˜15X smaller than the main inductor L. Note that, to achieve the peak efficiency at heavy load, two paralleled devices are used for each power switch. To minimize the timing mismatch, two sets of devices are mirrored on each side of the demonstration PCB as shown in Fig. 4.8. The total footprint

area of the auxiliary circuit is around 20% of the conventional 3LB converter.

Using the test automation system, the maximum efficiency points for each operating condition were found and the feature of full ZVS was verified as shown in Fig. 4.9. The results clearly reflected that at 15 V/4 V conversion, and 1 MHz switching frequency, the switching node voltage V_x ringings due to hard switching are significantly alleviated by the auxiliary circuit.



(a)



(b)

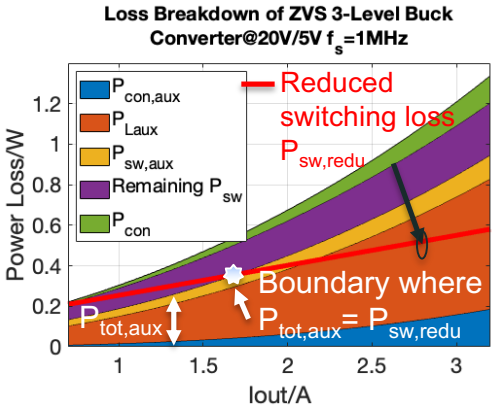
Figure 4.9. Measured waveforms @15 V/4 V, 1 A, 1 MHz condition (a) without ZVS, (b) with ZVS because of auxiliary circuit.

To compare the conventional 3LB converter and the proposed ZVS-3LB converter, their measured efficiencies (Exp.) are plotted in Fig. 4.10 together with analytical calculation results (Cal.) at 20 V/5 V and 15 V/4 V conversions and various loads. At light load conditions below 1.5 A, the ZVS-3LB converter significantly reduces power loss by up to 30% and improves efficiency by up to 3%. The improvement is proved to come from the auxiliary circuit for ZVS, which occupies only 20% additional area. The peak light load efficiencies are 92.4% and 92.2% for 20 V/5 V and 15 V/4 V conversion at 1 A and 0.7 A, respectively.

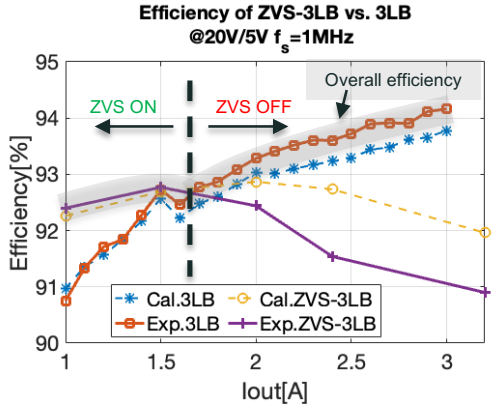
4.5 Limitation of the Prototype

As already introduced in Section. 4.3, the parasitics on a PCB would add difficulties on rapid and precise sensing. Consequently, an open-loop design with parameter sweeping is necessary. To facilitate this system design requirement, an FPGA with NiosII embedded system is employed. However, the minimum time step on FPGA becomes one bottleneck of achieving optimized inductor dimension while maintaining high efficiency.

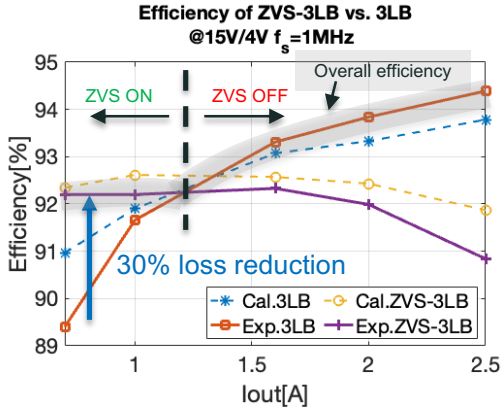
For a smaller L_{aux}, it requires shorter time period for ramping the auxiliary inductor current up to acquire adequate Q_{req} for complete soft-switching. Numerically, by using 10 nH auxiliary inductor, to achieve the desired soft-switching, the pulse width of Aux_b is 3.25 ns if assuming 15 V input voltage, 1 A load current, 10 nH L_{aux} and 15 nC Q_{req}, way lower than the 5 ns minimal time step on the FPGA. Therefore, a larger auxiliary inductor has to be selected, e.g. 100 nH. From the analysis in Section. 4.2, a longer Aux_b would cause higher conduction loss on the auxiliary circuit limiting the range where efficiency is benefited from ZVS. A comparison of the efficiency with different auxiliary inductor is conducted as shown in Fig. 4.11. The result suggests that when the pulse width boundary of PWM signals can decrease to a few nano-second or even sub-ns, the L_{aux} would drop to a lower value while the system efficiency as well as the power density would be greatly enhanced.



(a)



(b)



(c)

Figure 4.10. (a) loss breakdown at 20 V/5 V; and measured efficiencies of the proposed ZVS-3LB converter and their comparison with the conventional 3LB converter at (b) 20 V/5 V, (c) 15 V/4 V

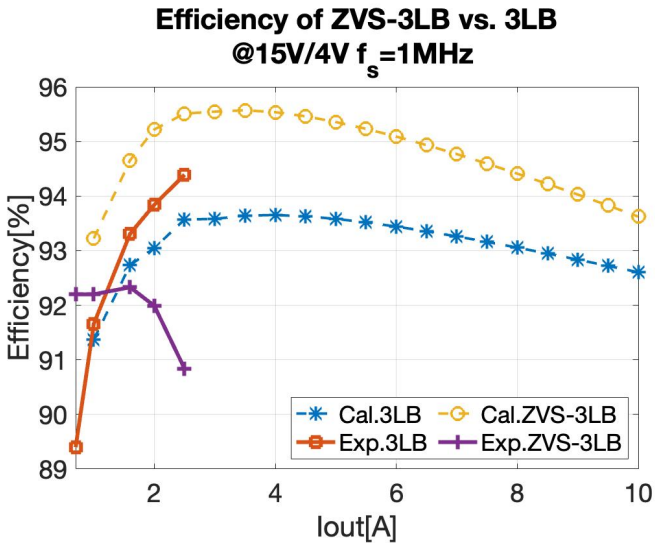


Figure 4.11. The efficiency comparison of ZVS-3LB converter with (solid lines) 1.5 μH main inductor and 100 nH auxiliary inductor,
and the one (dash lines) with 500 nH main inductor and 10 nH auxiliary inductor

4.6 Summary

The proposed ZVS-3LB converter has been proved a good candidate for reducing the switching loss related to high side switches. The same idea of adding auxiliary circuit to assist soft-switching is also applicable for other topologies when there is a need for alleviating switching loss. As a consequence, it results in a higher switching frequency and thus smaller inductors. Despite the limitation of the prototype testing, analysis shown in Fig. 4.11 has indicated the possible improvement of the results when the circuit is built on a more compact package, e.g. an integrated circuit, and controlled more precisely. The potential value of inductance would rest in 100s of nH, which is a great improvement compared with the conventional buck converter, but is still outside the acceptable range for fully integration.

4.7 Acknowledgements

This chapter, in full, is a reprint of the material as it appears in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC). Tianshi Xie; H. Le, ”A Zero-Voltage-Switching

3-Level Buck Converter Achieving 30% Loss Reduction at Light Load for USB-C Charger Applications," APEC 2023. The dissertation author was the primary investigator and author of this paper.

Chapter 5

ITSAB Converter

5.1 Operation Principle

Figure 5.1 shows the power stage of the proposed ITSAB converter. It consists of 2 P-type power switches Q7 and Q8, 6 N-type power switches Q1-Q6, 3 flying capacitors C1-C3, and two nH-scale inductors L1 and L3. The proposed converter can be viewed as adding inductors to the flying capacitors of a Dickson-star Switched Capacitor (SC) converter. The presence of these inductors helps with soft-charging the flying capacitors to achieve high efficiency. Although the circuit topology resembles the prior works that rely on resonant operation [8, 34, 42, 43], the ITSAB converter has completely different operation that enables the use of nH-scale inductors at moderate switching frequency. A detailed comparison between these topologies has been presented in [44].

Operation of the ITSAB converter can be divided into 4 different states as shown in Fig. 5.2. Two phases of gate control signals, ϕ-ϕ_b and ϕ_S-ϕ_{Sb}, are illustrated in Fig. 5.3 together with the waveforms of the inductor currents and flying capacitor voltages. Phase ϕ_S-ϕ_{Sb} is shifted by t_ϕ from ϕ-ϕ_b forming the two phase-shift states 2 and 4. The operation of capacitor charge transfer in the ITSAB converter resembles that of a Dickson-Star SC converter. The key difference is that the charge transfer between flying capacitors and to the output in the Dickson-star SC converter is hard-charging, while it is soft-charging in the ITSAB using the two inductors L1 and L3. As a result, the steady-state voltages across C1, C2 and C3 are $\frac{3Vin}{4}$,

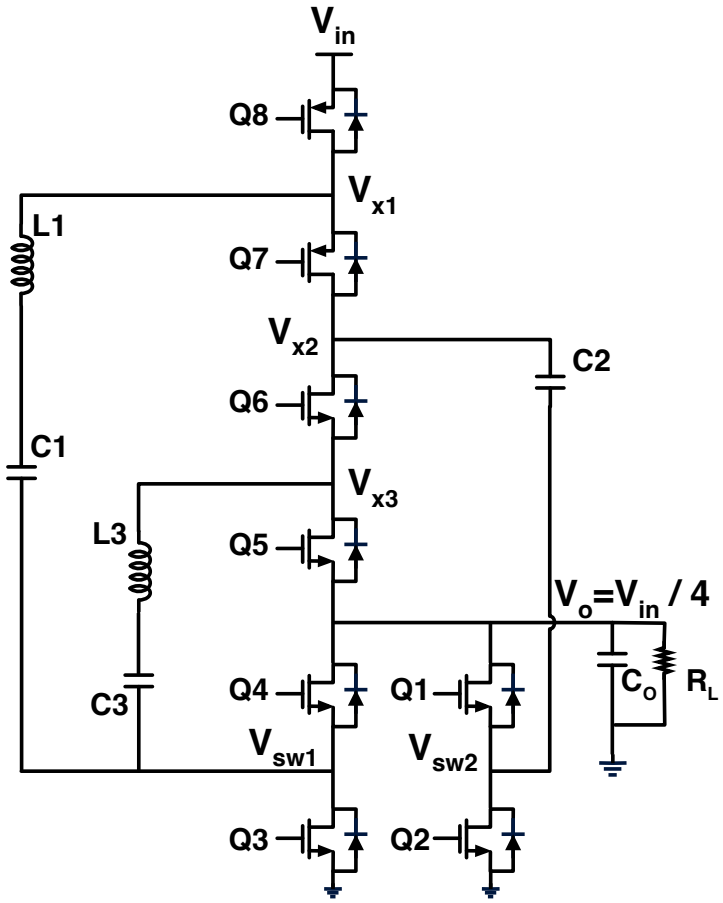
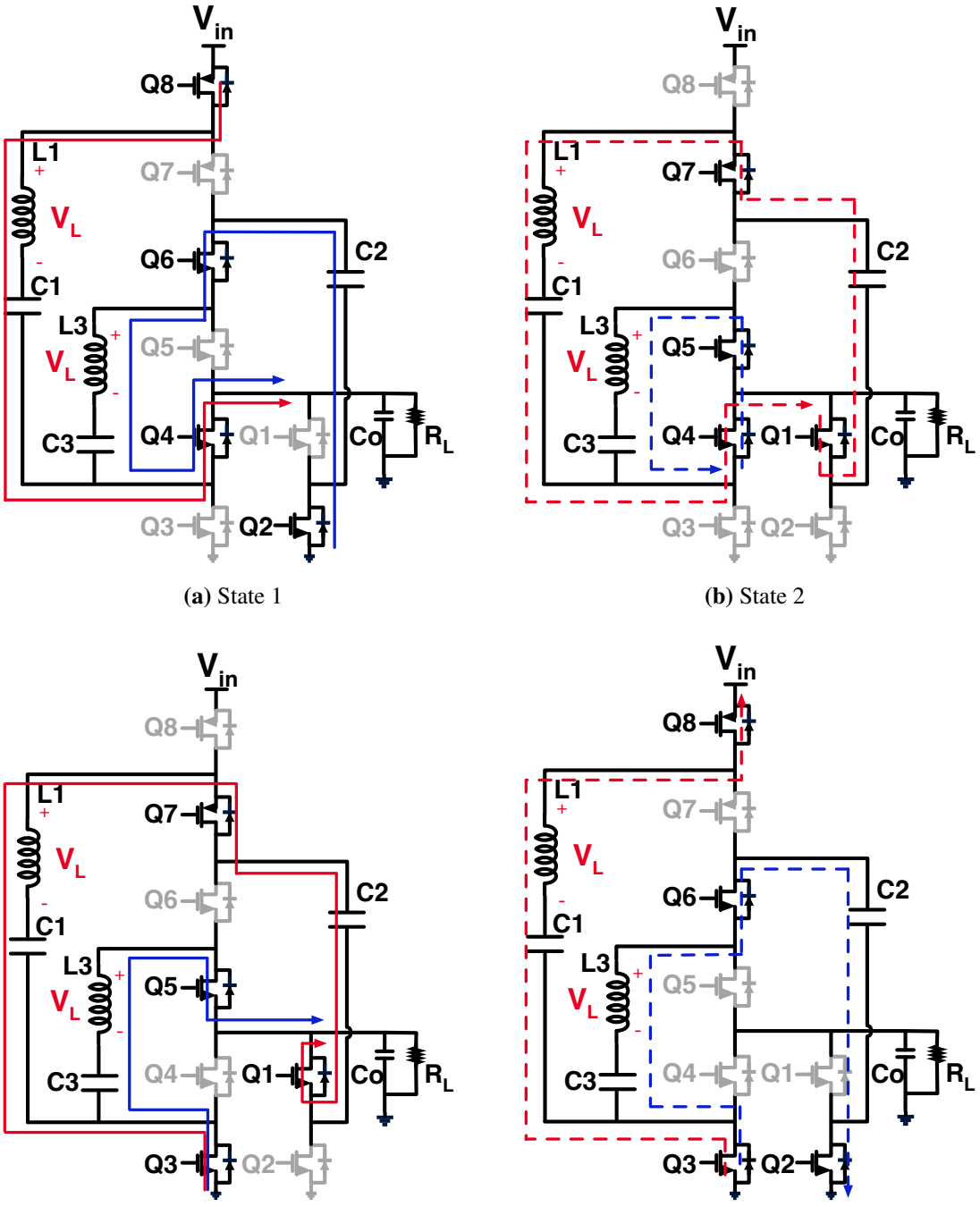


Figure 5.1. Schematic of the proposed integrated transformerless stacked active bridge (ITSAB) converter.

$\frac{V_{in}}{2}$ and $\frac{V_{in}}{4}$, respectively. Unlike the resonant switched-capacitor (ReSC) converters in [45][8], the passive components values are selected to ensure the $L1$ $(L3)$ and $C1\&C2$ $(C3\&C2)$ tank resonant frequency is well below the switching frequency f_s.

State 1: Unique in this converter, both inductors carry near-constant $I_o/2$ currents to the output as a result of near-zero voltage across each of the inductors during this time interval. Subsequently, both flying capacitor C1 and C3 are softly charged, while C2 is softly discharged, all by the same amount of current.

State 2: This phase-shift time interval starts when all the switches toggle except for Q3 and Q4. As a consequence, both inductors have $V_L = -V_{in}/4$ across them, which is the voltage of C3 for L3 and the voltage difference across C1 and C2 for L1. As the result, both inductor



(a) State 1

(b) State 2

(c) State 3

(d) State 4

Figure 5.2. Power stage operation of the ITSAB converter.

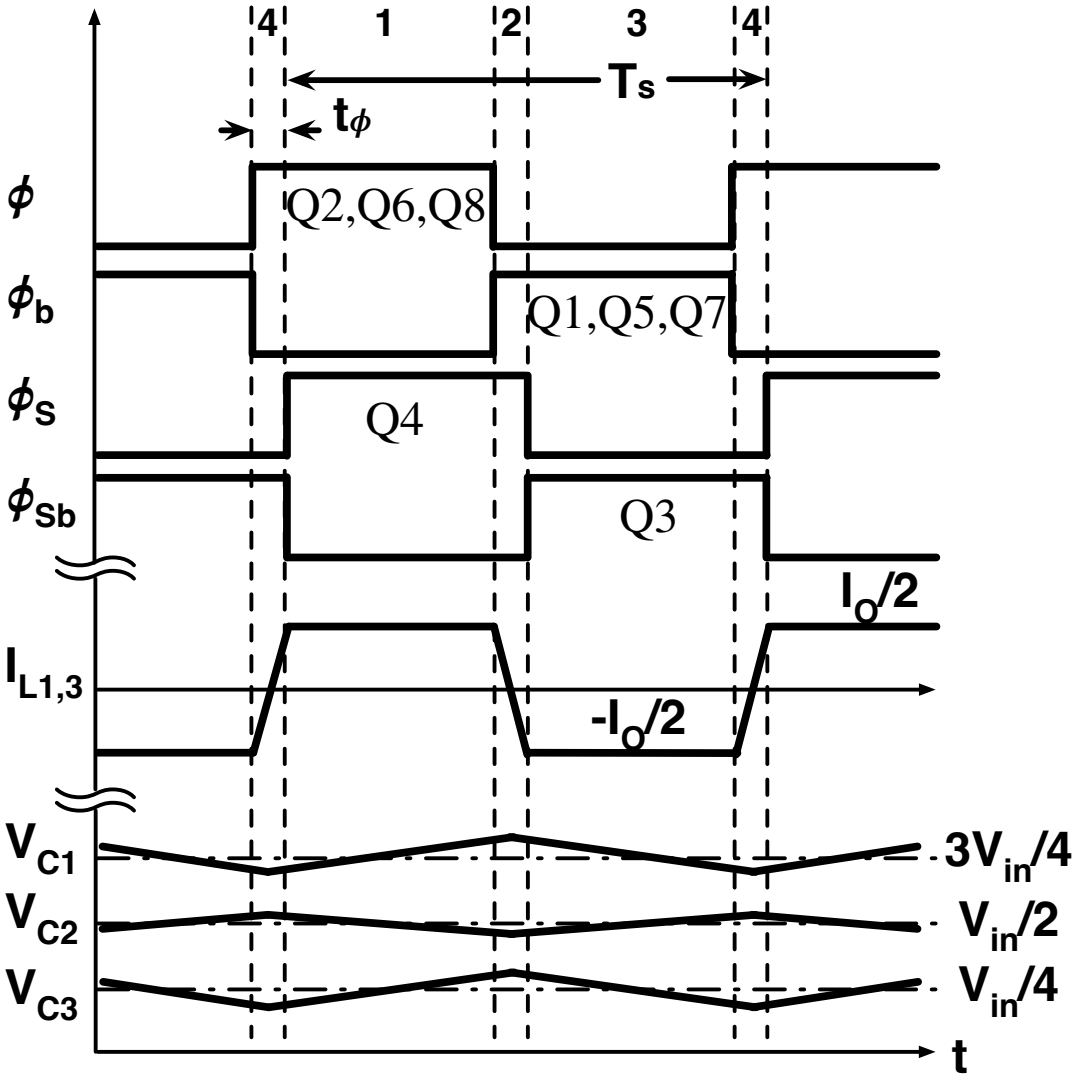


Figure 5.3. Operating waveforms in the ITSAB converter.

currents ramp down to zero then continue ramping up in the opposite direction. All flying capacitors shift their charging/discharging status during this time interval when the inductor currents are zero. This state ends when Q3, Q4 change their ON/OFF status as the inductor current reaches approximately $-I_o/2$.

State 3: This state is the same as State 1, except the inductor currents are flipped. The capacitors' charging status is also altered.

State 4: Inductor currents are flipped compared with State 2. The voltages across the inductors are $V_L = V_{in}/4$.

During the two phase-shift states 2 and 4, the inductor currents ramp up and down at a same rate of

$$\frac{di_L}{dt} = \frac{V_{in}}{4L} \tag{5.1}$$

From charge balance, the output current I_o can be found as [44]

$$I_o = \frac{V_{in}}{8Lf_s}\phi(1-\phi) \tag{5.2}$$

where $\phi = \frac{2t_\phi}{Ts}$ is the phase shift ratio. Therefore, by modulating t_ϕ, I_o and thus the output voltage V_o can be regulated.

The length of t_ϕ depends on the inductance, the load current, as well as the input voltage. Practically, it is in nano-second range when using nano-Henry inductors, considering 1 A output current and 12 V input voltage. The trapezoidal shape with ripple-free maximum values of currents I_{L1} and I_{L3} not only leads to small RMS value and thus small conduction loss but also results in small output voltage ripple. This eventually reduces the required output capacitance, which further contributes to high power density.

5.1.1 Soft-switching

As an additional benefit of flipping the inductor current flowing direction, at the end of states 2 and 4, the switching node V_{sw1} is fully soft-discharged and soft-charged by the inductor

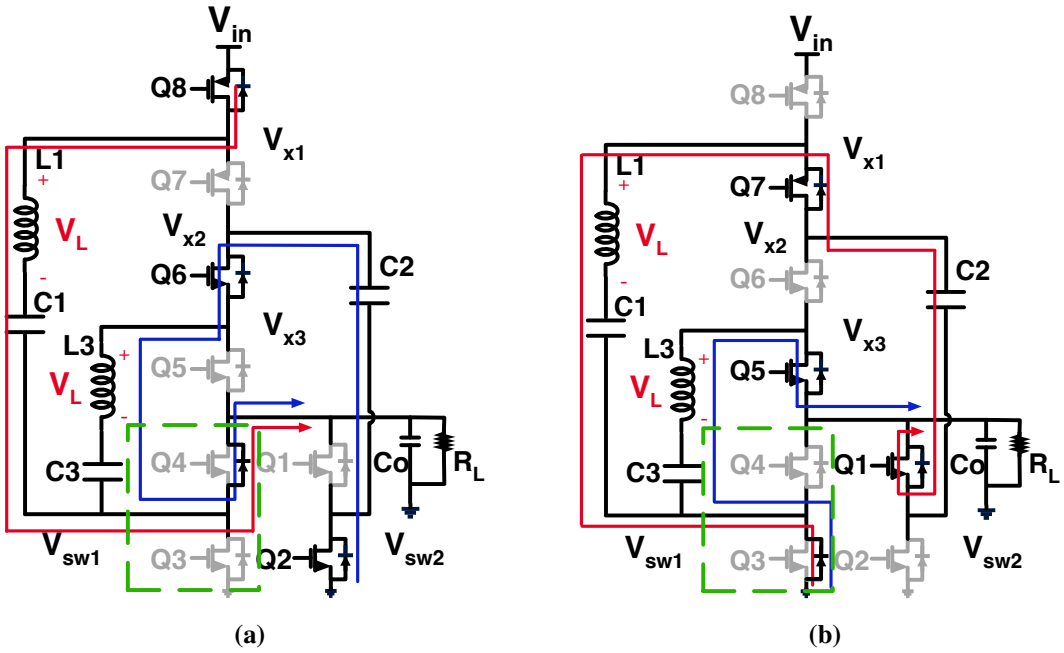


Figure 5.4. Zero-voltage-switching (ZVS) of Q3 and Q4 between (a) state 4 and 1, (b) state 2 and 3.

currents during the deadtime of ϕ_S and ϕ_{Sb}, as illustrated in Fig. 5.4. Consequently, Q3 and Q4 are fully soft-switched. On the contrary, I_{L3} and I_{L1} keep forward biasing the body diodes of Q2 and Q1 during the deadtime between state 1 and 2, and the one between state 3 and 4, respectively. In other words, Q1 and Q2 are hard-switched. Meanwhile, the switches Q5-8 are partially soft-switched, because the switching nodes V_{x1-3} are partially charged/discharged by I_{L1} and I_{L3} while being impacted by hard-switching node V_{sw2}. As an example, V_{x1}, also the Source of Q7, is soft-charged to V_{in} by I_{L1} once Q7 is turned off at the end of state 3. When Q1 and Q2 hard-switch in state 4, V_{x2} jumps from $3V_{in}/4$ to $V_{in}/2$ causing drain-to-source capacitor C_{ds} of Q7 being hard-charged. Even though Q1 and Q2 are hard-switched, they are half the size of the switches Q3 and Q4 because they carry half the current and thus cause lower additional switching loss. Because of the ZVS operation, the ITSAB power stage can operate efficiently at switching frequency in the Mega-Hertz range.

5.2 Loss Analysis of ITSAB Converter

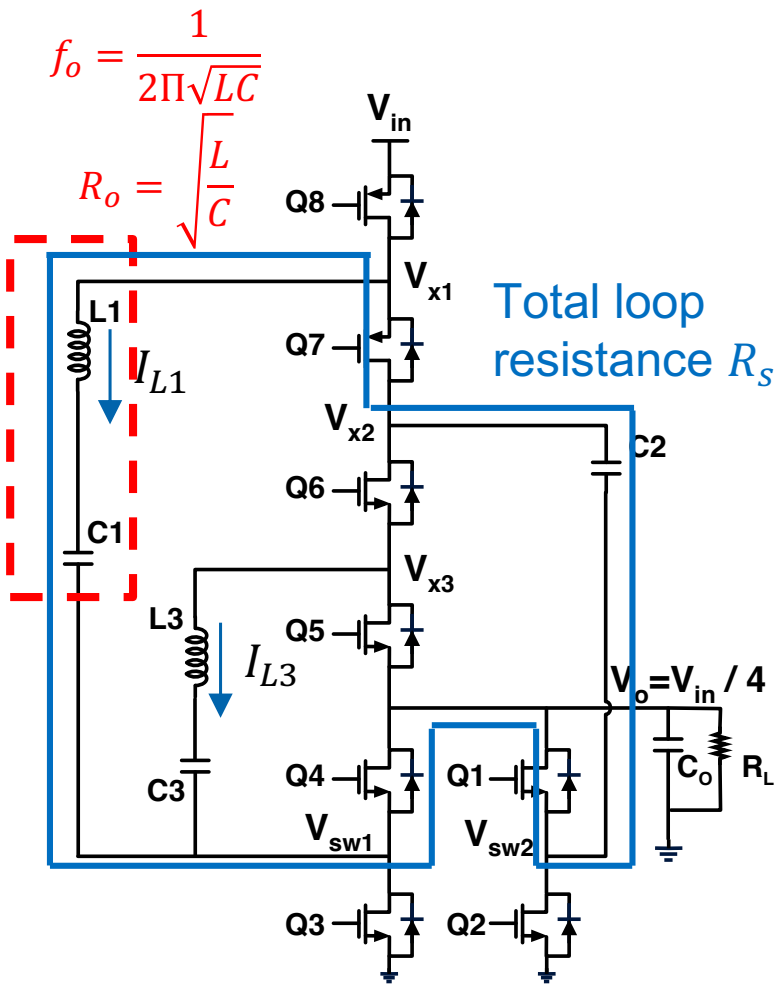


Figure 5.5. Definitions of parameters f_o, R_o and R_s.

The power loss of the ITSAB converter can be categorized into two major parts: conduction loss and switching loss. To accurately calculate the conduction loss, the RMS value of the inductor currents is needed. In this section, the detailed loss analysis with RMS current value calculation is given.

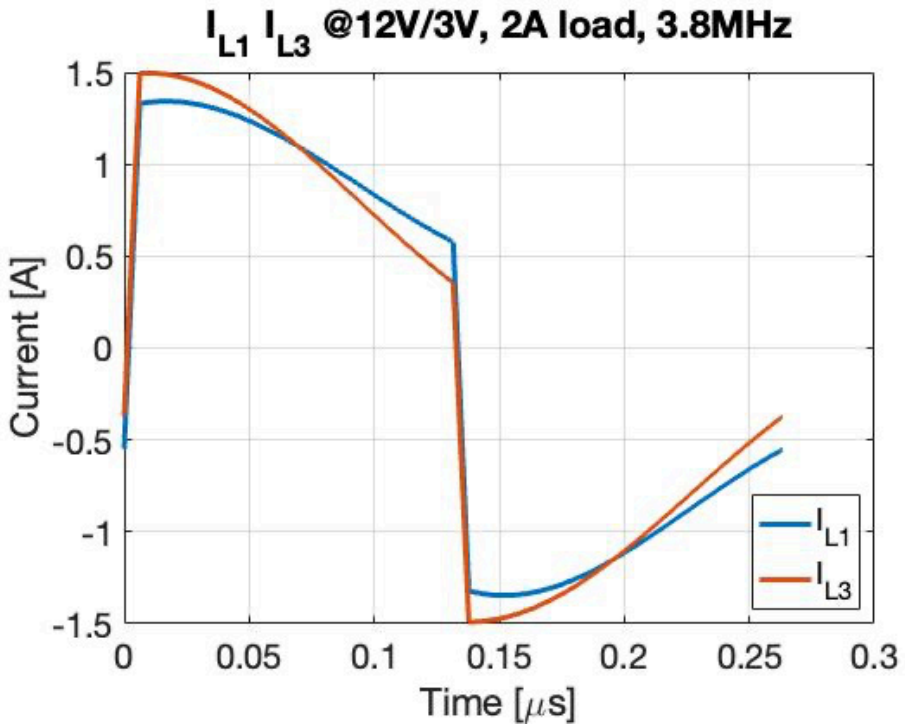


Figure 5.6. Calculated I_{L1}, I_{L3} waveforms for 12 V-to-3 V conversion, 2 A load, $f_s = 3.8\,\text{MHz}$, with $R_s = 55\,\text{m}\Omega$.

5.2.1 Conduction Loss

The conduction loss can be written as

$$\begin{aligned} P_{cond} = &\sum_{i=7}^{8} R_{on_i} I_{L1,RMS}^2 + \sum_{i=5}^{6} R_{on_i} I_{L3,RMS}^2 \\ &+ \sum_{i=3}^{4} R_{on_i} I_{L1+L3,RMS}^2 \\ &+ R_{on_2} I_{L3,RMS}^2 + R_{on_1} I_{L1,RMS}^2 \end{aligned} \tag{5.3}$$

where R_{on_i} is the on resistance of each power switch and $I_{L1,RMS}$, $I_{L3,RMS}$ are the RMS current of L1 and L3, respectively. While the inductor currents are displayed in Fig. 5.3 as having an ideally trapezoidal shape with $\frac{I_o}{2}$ value at the top, they slightly curve in practice owing to the response of the LC tank network with parasitic series resistances. To improve the conduction loss model accuracy, it is necessary to include these effects in calculation of the current RMS

values.

The approach described in [46] can be extended to the 4-to-1 ITSAB circuit. In each switch state shown in Fig. 5.2, the state-space equation can be written as

$$\dot{x} = A_i x + b_i V_{in}, i = 1,2,3,4 \tag{5.4}$$

where $x = [i_{L1}, i_{L3}, v_{C1}, v_{C3}, v_{C2}, v_O]^T$ and

$$
\begin{aligned}
A_1 &= \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & 0 & -\frac{1}{L1} \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & \frac{1}{L3} & -\frac{1}{L3} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C2} & 0 & 0 & 0 & 0 \\ \frac{1}{Co} & \frac{1}{Co} & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, b_1 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix} \\
A_2 &= \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & \frac{1}{L1} & 0 \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & 0 & 0 \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, b_2 = \begin{vmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix} \\
A_3 &= \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & \frac{1}{L1} & \frac{1}{L1} \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & 0 & \frac{1}{L3} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{Co} & -\frac{1}{Co} & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, b_3 = \begin{vmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix} \\
A_4 &= \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & 0 & 0 \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & \frac{1}{L3} & 0 \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, b_4 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix}
\end{aligned}
\tag{5.5}
$$

where R_s is the total loop resistance as drawn in Fig. 5.5.

To numerically compute the inductor currents at various time, the augmented state-space approach [47] is utilized in this work. It provides a viable way to accurately calculate the exact solution of the aforementioned state-space equations, especially when the system matrix A_i is singular. Examples of the computed I_{L1} and I_{L3} are plotted in Fig. 5.6, assuming $R_s = 55\,\mathrm{m}\Omega$

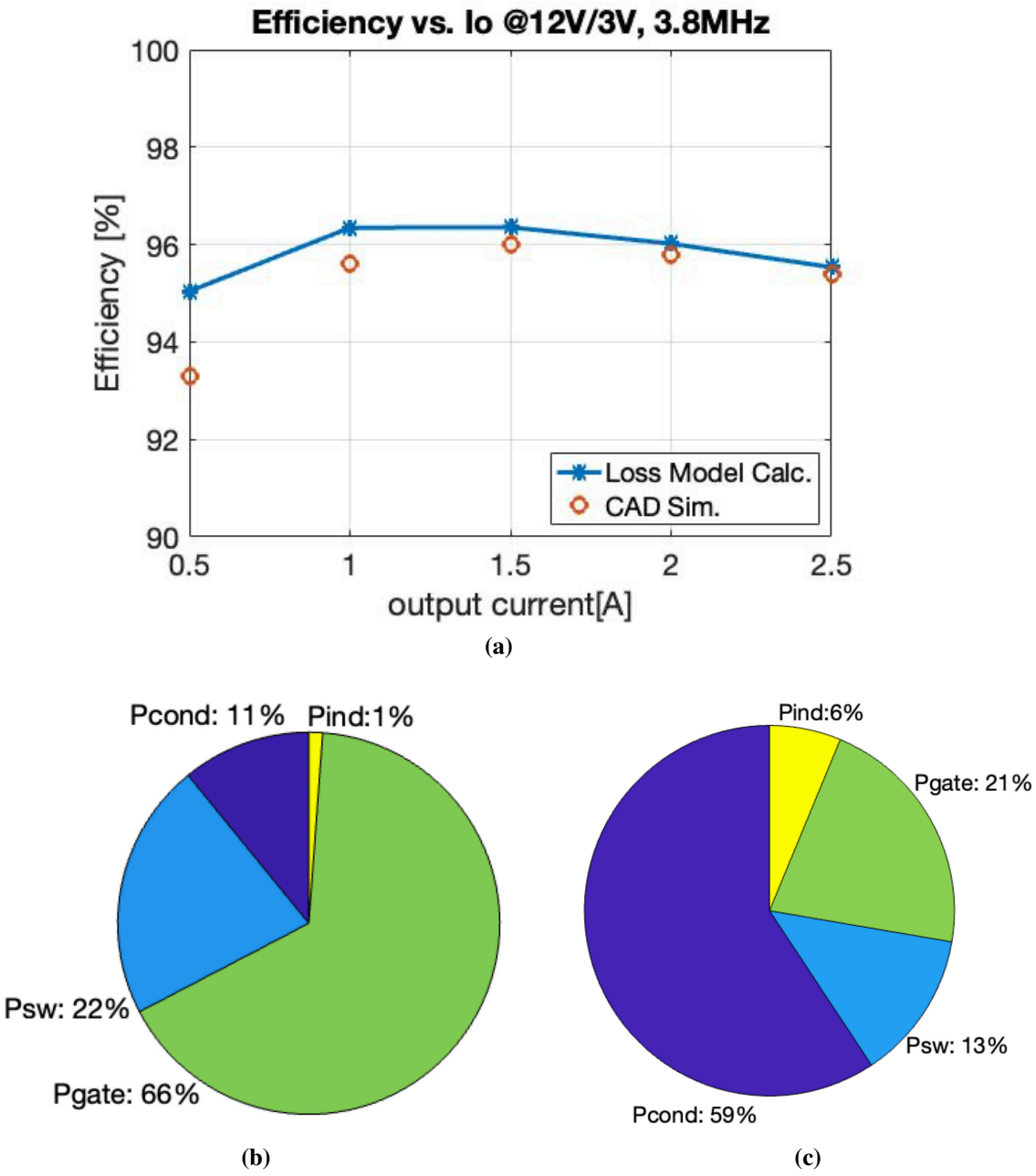


Figure 5.7. Loss model verification: (a) efficiency comparison; Loss breakdown at (b) 0.5 A load, (c) 2 A load

. When the load current is 2 A, and each inductor delivers 1 A on average, with $\sim$ 1 A ripple during states 1 and 3. One may note how the exact RMS values of these currents are higher than ideal $I_o/2$, which yields a more accurate conduction loss evaluated from (5.3).

5.2.2 Switching Loss

Switching loss is primarily related to power switches gate capacitances C_{gg} and the parasitic capacitors of the switching nodes, namely, C_{X1}, C_{X2}, C_{X3}, C_{SW1}, C_{SW2}. The gate capacitors switching loss can be written as

$$P_{gate} = \sum_{i=1}^{8} C_{ggi} V_{DD}^2 f_s \tag{5.6}$$

where V_{DD} is the V_{GS} driving voltage for the power switches. As mentioned in Section 5.1, Q5-Q8 are partially soft-switched, Q3 and Q4 are fully soft-switched, while Q1 and Q2 are completely hard-switched. Therefore, the total switching loss of the switching nodes parasitic capacitors can be approximated by

$$P_{coss} = \left(\sum_{i=1}^{3} \frac{1}{2} C_{Xi} + C_{SW2} \right) V_{ds}^2 f_s \tag{5.7}$$

where $V_{ds} = V_{in}/4$. The last part of switching loss is caused by V-I overlap [48] during the hard-switching transitions of Q1,2 and partial hard-switching transitions of Q5-8, which can be expressed by

$$P_{tr} = P_{tr,on} + P_{tr,off} = 8 \times \frac{1}{2} V_{ds} I_{L1,3} t_{tr} f_s \tag{5.8}$$

Where the transition time t_{tr} indicates V-I overlap time. Practically in this design, the P_{tr} is small compared to other losses and therefore can be ignored. This is because: 1) the nature of Dickson-Star SC that blocks most of V_{in} so that Q1,2 are only stressed by $\frac{V_{in}}{4}$; and 2) t_{tr} is short as for small power switches. However, this type of loss can't be ignored when the ITSAB converter is designed for heavier loads that the power switches are large enough to have significant reverse

recovery charge and long t_{tr} .

5.2.3 Inductor Loss

Considering an air-core inductor realization, no core loss needs to be accounted for. As a consequence, only DCR and ACR loss of the inductor are considered. The DCR loss is given by

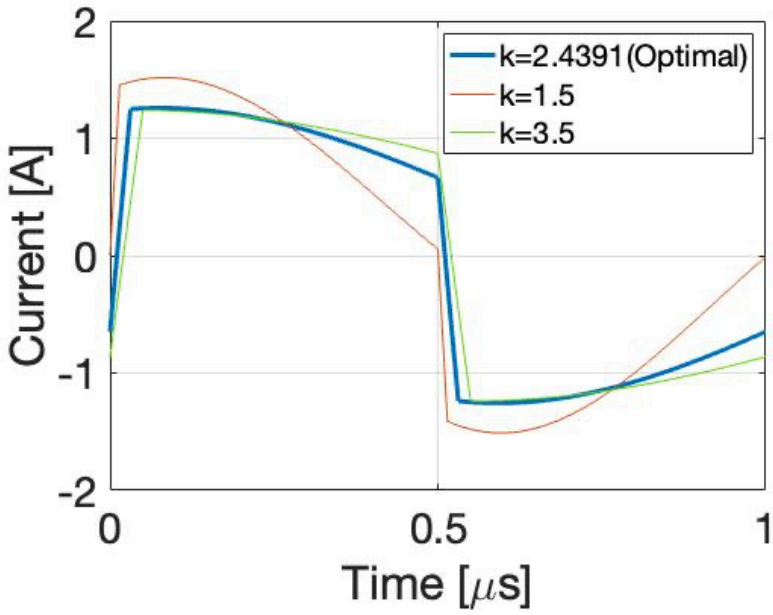
$$P_{ind,DCR} = (I_{L1,RMS}^2 + I_{L3,RMS}^2)R_{DC} \tag{5.9}$$

where the RMS value of the inductor currents can be computed by the same approach as described in Section 5.3. The AC loss of the specific inductor can be calculated using the model provided by the manufacturer. For simplicity, the inductor loss is approximated as the DCR loss, $P_{ind} \approx P_{ind,DCR}$.

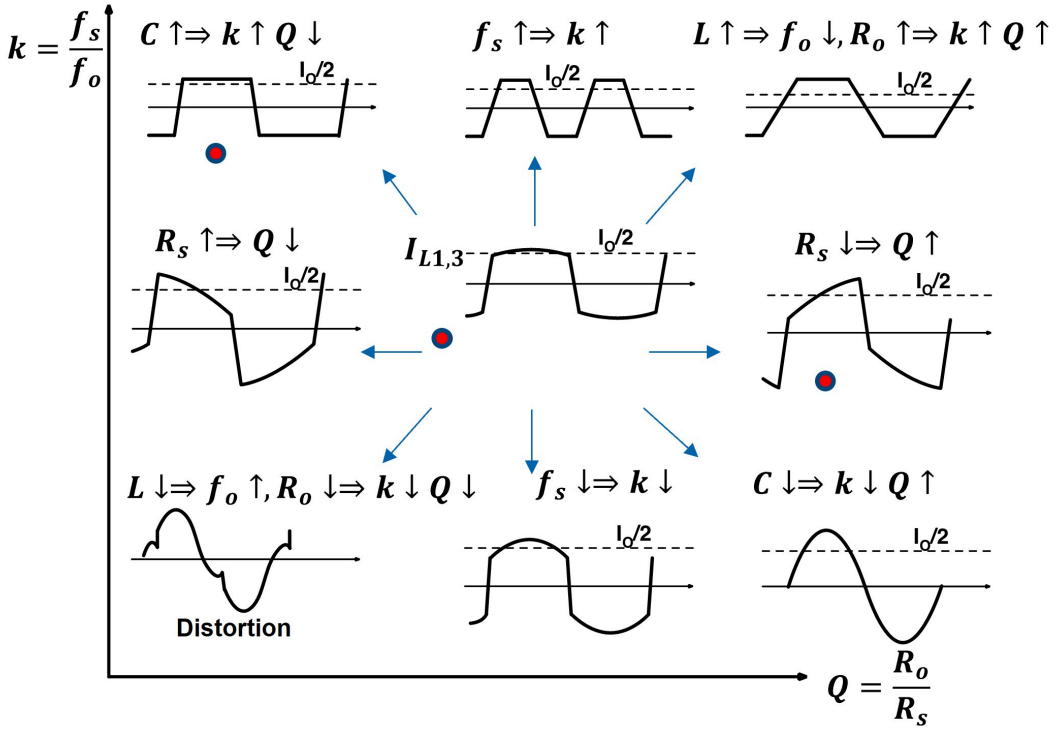
The loss model is verified by comparing the calculated efficiency to the CAD simulated results, as shown in Fig. 5.7, which shows a good match. Two pie charts of the loss breakdown computed at 12 V/3 V, $f_s = 3.8\,\text{MHz}$, 0.5 A and 2 A loads are given in Fig. 5.7(b) and Fig. 5.7(c), respectively. In the calculation, switching loss P_{sw} includes P_{coss} and P_{tr}. It can be seen that the frequency related losses, mostly P_{sw} and P_{gate}, dominate the total loss at light load as a result of less conduction loss and insufficient I_o for completely soft-switching Q3 and Q4 [44]. At heavy load, however, the conduction loss dominates and it is therefore crucial to properly design and operate the converter so that the minimum RMS value of the inductor currents is achieved. In the next section, the optimization methodology is discussed in more detail.

5.3 Optimization Methodology

As discussed in Section 5.2, two major loss mechanisms in the ITSAB converter are conduction loss P_{cond} and switching loss $P_{sw} + P_{gate}$. To minimize the power loss at a desired operating point, one can sweep the converter parameters, including power switch area, switching frequency, etc. However, as shown in Fig. 5.6 and the analysis in Section 5.2, the shape of the



(a) Inductor current waveshape for $Q = 2.6$ and three different values of $k = f_s/f_o$. The minimum $I_{L1,RMS}$ is obtained for $k = 2.4391$.



(b) Summary of inductor current waveshapes in the k versus Q plane. The minimum-RMS cases are highlighted (red dots).

Figure 5.8. Illustration of how inductor RMS current is minimized using $k = f_s/f_o$ and $Q = R_o/R_s$ as optimization parameters.

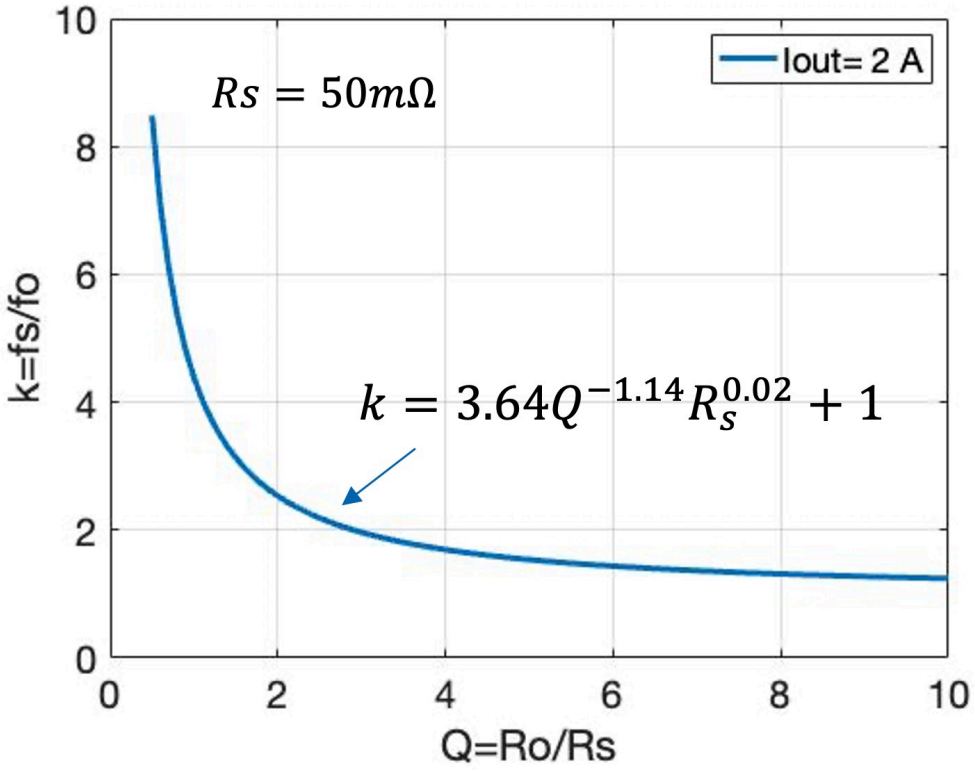


Figure 5.9. Optimum k as a function of Q for $R_s = 50\,\text{m}\Omega$ and $I_o = 2\,\text{A}$.

inductor currents is sensitive to the system parameters. In other words, even though a minimum power loss can be found by sweeping the parameters, the inductor currents could potentially be distorted and peaking above the saturation current of the inductors, potentially resulting in malfunction of the circuit. In this section, a novel optimization methodology is proposed so that the inductor current distortion can be prevented while the minimum power loss is found.

5.3.1 Minimum RMS Current

As marked in Fig. 5.5, the resonant frequency and the characteristic impedance of each resonant tank are

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \text{ and } R_o = \sqrt{\frac{L}{C}} \tag{5.10}$$

where L is the inductance of L1 and L3, and C is the capacitance of C1 and C3. Two variables are used in this optimization process, k defined as

$$k = \frac{f_s}{f_o} \tag{5.11}$$

and the quality factor Q,

$$Q = \frac{R_o}{R_s} \tag{5.12}$$

where R_s is the total loop resistance as indicated in Fig. 5.5, which comprise of power switches on-resistance and ESR of L and C. Given the above equations, the inductance and the capacitance of each resonant tank can be expressed in terms of k and Q

$$L = \frac{kQR_s}{2\pi f_s},\ C = \frac{k}{2QR_s\pi f_s} \tag{5.13}$$

where f_s is the switching frequency. In order to find the parameters that make the inductor current achieve minimum RMS value, a relation between k, Q and R_s must be carried out. The augmented state-space approach [47] is utilized to obtain the inductor current waveforms for various sets of parameters and operating conditions. For instance, when Q is picked as 2.6 and R_s equals 50 mΩ, current I_{L1} can be depicted in Fig. 5.8(a) for different k at 12 V-to-3 V, 2 A conversion at $f_s = 1$ MHz. The highlighted curve, which is for $k = 2.4391$, has minimum RMS value. When k is smaller, indicating a smaller L and the resonant frequency becomes closer to the switching frequency, the curve has higher ripple. On the other hand, an increased k means larger L and slower current ramping speed during states 2 and 4, leading to shorter times for states 1 and 3, and thus higher peak current to deliver the same load current. Neither of the above two cases can achieve smaller RMS value than the optimal point. A brief summary of how k and Q value change along with the circuit parameters L, C and R_s, and the resulted inductor current shapes is listed in Fig. 5.8(b). The dots on each column indicate the corresponding minimum RMS value point. Once a range of Q is evaluated in the same manner, the targeted parameters

relation can be depicted by using a curve fitting method as shown in Fig. 5.9. It sets the boundary of distortion region which is the area below the curve. This curve-fit relation is:

$$k = 3.64Q^{-1.14}R_s^{0.02} + 1 \tag{5.14}$$

From this equation, it can be seen that the optimum k approaches 1 when Q approaches infinity, which represents operation at resonance. For a practical, finite Q, the optimum is for above-resonance $k > 1$ operation.

5.3.2 Optimization Process

Semiconductor parameters are scaled with the device area A_s

$$R_{on} = \frac{R_{on,sp}}{A_s} \tag{5.15}$$

$$Q_{tot} = (Q_{gg,sp} + Q_{dd,sp} + Q_{ss,sp})A_s \tag{5.16}$$

where $R_{on,sp}$, $Q_{gg,sp}$, $Q_{dd,sp}$ and $Q_{ss,sp}$ are the density of on-resistance, gate charge, drain charge and source charge per unit area, respectively. After plugging these scaling equations (5.15) and (5.7), the loss modeling expressions (5.3), (5.6) and (5.7) can then be formulated as

$$P_{cond} = \frac{P_{cond,sp}}{A_s} \tag{5.17}$$

$$P_{gate} = P_{gate,sp}A_s \tag{5.18}$$

$$P_{sw} = P_{sw,sp}A_s \tag{5.19}$$

where $P_{cond,sp}$, $P_{gate,sp}$ and $P_{sw,sp}$ represent the specific power loss per unit area. As a result, the total power loss can be turned into the following form

$$P_{tot} = \sum_{i=1}^{8} \left(\frac{P_{cond,sp_i}}{A_{s_i}} + (P_{gate,sp_i} + P_{sw,sp_i}) A_{s_i} \right) + P_{ind} \tag{5.20}$$

The optimization process of the proposed circuit can be expressed in the following form

$$\begin{aligned} &minimize\ P_{tot}(X) \\ &subject\ to\ \sum_{i=1}^{8} A_{s_i} \leq A_{tot,max} \\ &A_c \leq A_{c,max} \\ &L \leq L_{max} \end{aligned} \tag{5.21}$$

where the vector $X = [f_s, A_s, R_o]^T$ denotes the variables in this converter design, and $A_{tot,max}$, $A_{c,max}$ and L_{max} set the limit of chip area, capacitor footprint area and inductor value, respectively. Mathematically, minimizing P_{tot} in (5.20) is a geometric programming (GP) problem [49], which can be efficiently solved using tools such as CVX[50]. The optimization results, including selected passive component, switching frequency and areas of the power switches, are summarized in Table 5.1.

Table 5.1. Optimization results.

Parameters	Details
L	$10\,\mathrm{nH}$
C1, C3	$1.05\,\mu\mathrm{F}$
C2	$4\,\mu\mathrm{F}$
f_s	$3.35\,\mathrm{MHz}$
Q1, Q2 area	$0.1139\,\mathrm{mm}^2$
Q3, Q4 area	$0.2007\,\mathrm{mm}^2$
Q5, Q6 area	$0.1194\,\mathrm{mm}^2$
Q7, Q8 area	$0.1373\,\mathrm{mm}^2$

5.4 Implementation Details

The system block diagram including all key blocks and the power stage is shown in Fig. 5.10. The blocks within the solid rectangle are implemented on-chip, while the passive components between the solid line and dash line are on the package substrate. The key on-chip blocks include Gate Drivers (GD1-GD8) and their voltage-supply Linear Regulators (LR); Ramp Generator (RG) for synchronization and generating ramp signal at the required frequency; Phase Shift Modulator (PSM) for closed-loop regulation; Non-overlapped Signal Generator for dead-time control; serial Programming Register for setting up frequency and dead time; Biasing circuit for creating bias currents for other sub-blocks throughout the chip; OTA-based Error Amplifier (EA) to form the closed-loop controller. In the following parts of this section, the control signal generation, gate drivers and LRs, control loop design and synchronization are addressed separately.

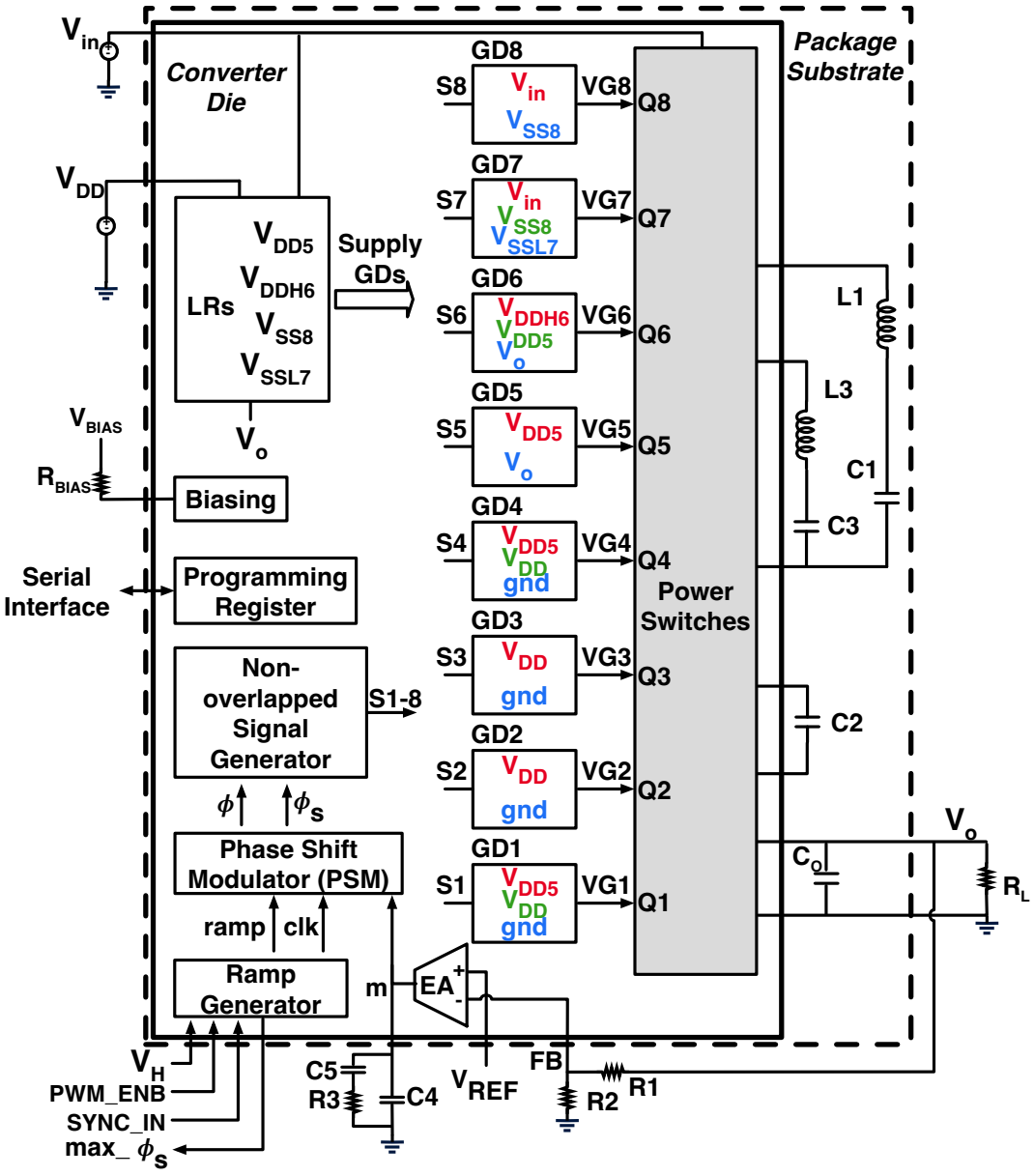
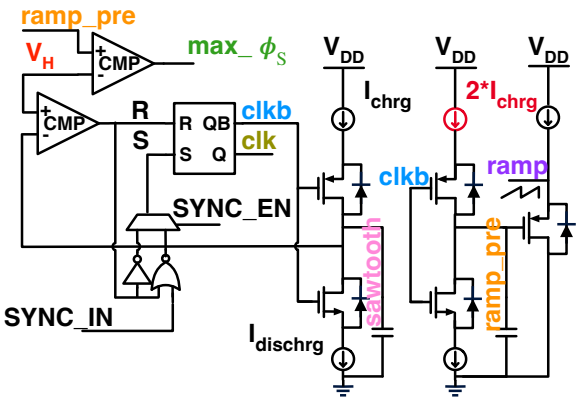
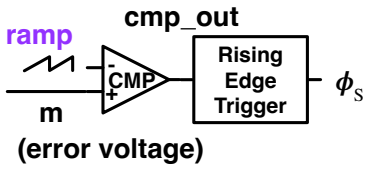
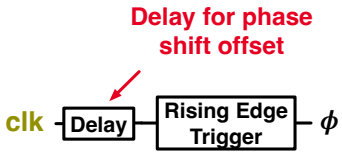


Figure 5.10. Block diagram of the prototype ITSAB converter realized on a 130 nm BCD die flip-chipped on a package substrate together with power capacitors and two 10 nH inductors.

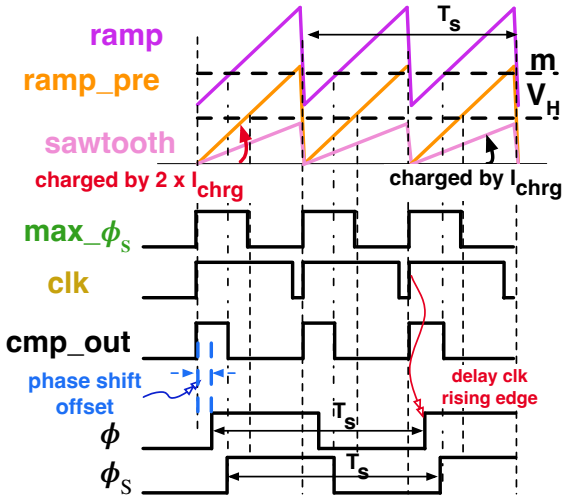


(a)





(b)



(c)

Figure 5.11. Phase-shifted control signal generation, including block diagrams of (a) Ramp Generator (RG), and (b) Phase Shift Modulator (PSM); (c) timing diagram: generation of ϕ, ϕ_S.

5.4.1 Control Signal Generation

As derived in (5.2), the output voltage of the implemented ITSAB converter is fully regulated by the phase shift between ϕ and ϕ_S. These control signals are generated from the Phase Shift Modulator (PSM) and the Ramp Generator (RG), illustrated in Fig. 5.11 along with the timing diagram of the corresponding signals. Particularly, ϕ_S is periodically toggled by the rising edge of *cmp_out* (Fig. 5.11(b)) which is the output of comparing the error voltage m with the ramp signal from RG (Fig. 5.11(a)). Meanwhile, ϕ is triggered by the rising edge of the *clk* signal after a short delay as indicated in Fig. 5.11(c). Practical delay mismatches on signal paths from this control circuit to the final power gates would potentially result in delay mismatch on ϕ and ϕ_S at the converter power stage, which could lead to a minimum phase shift that is larger than zero even if the control circuit sets the phase shift to zero. A non-zero minimum phase shift would limit the minimum load current that the converter can support, following (5.2). To ensure that the converter can support an output current at light load current down to open-circuited load, it is desirable to generate a negative phase shift value of t_ϕ at this control circuit to compensate for any possible timing mismatch in the signal paths. Therefore, a short delay of ~ 15 ns is added after *clk* to give ϕ the phase shift offset for this purpose, as shown in Fig. 5.11(c).

The sawtooth waveform is generated by charging a MiM capacitor with I_{chrg} between ground and V_H. In this design $V_H = 1.5 - 2.5V$ depending on the target frequency, while V_{DD} can vary from 3V to 5V to optimize switching loss and conduction loss of power switches. From (5.2), it can be seen that the maximum output current is achieved when the phase shift time $t_\phi = \frac{Ts}{4}$. $t_\phi > \frac{Ts}{4}$ will lead to smaller average output current, because there is not sufficient time left after the phase shift to allow inductor currents to flow to the output. Therefore, the comparison to generate ϕ_S for phase-shift control need only be in the lower half of the sawtooth waveform. Exploiting this characteristic to get better noise immunity in generating the phase-shift control signal, *ramp_pre* is generated by a second branch with two times larger charge current. Finally, *ramp_pre* is slightly shifted up using a source-follower stage to make the *ramp*

signal that fits in the input common-mode range of the comparator inside PSM and the output range of Error Amplifier, m. To prevent the regulation loop from falling into a positive feedback when $t_\phi > \frac{T_S}{4}$, the phase shift must be limited using the signal $\max\_\phi_S$, which is a byproduct of ramp generation, by comparing the intermediate signal *ramp_pre* with the peak voltage V_H of the sawtooth signal.

Another feature of this design is to allow multiple converter chips to be synchronized, possibly in an interleaved manner, to improve the output current capability. This synchronization mode, therefore, is added and enabled by turning *SYNC_EN* of the RG to 1. With this setting, the current chip frequency can be triggered and synchronized by an off-chip clock signal to *SYNC_IN*. The synchronization is proved to work well when two chips are synchronized to the same frequency with 180° out of phase operations, as shown in the experiments in Section 5.5.

5.4.2 Gate Drivers & Supply Voltage Generation

The gate driver design is more challenging for a multi-level converter, because of flying source voltages and a larger number of power switches. The source voltages and the required gate voltages during ON and OFF state of all the power switches are listed in Table 5.2. There are four additional voltage levels defined as follows:

$$\begin{aligned} V_{SS8} &= V_{in} - V_{DD} \\ V_{SSL7} &= V_{SS8} - V_o \\ V_{DD5} &= V_{DD} + V_o \\ V_{DDH6} &= V_{DD5} + V_o \end{aligned} \tag{5.22}$$

A bootstrap driver containing a large capacitor and a diode is the most common way of driving high-side switches. However, the large bootstrap capacitor and diode would require to be off-chip and take significant area and volume. Furthermore, the diode voltage drop may reduce the available gate-drive swing resulting in weak driving, especially in the context of a multi-level

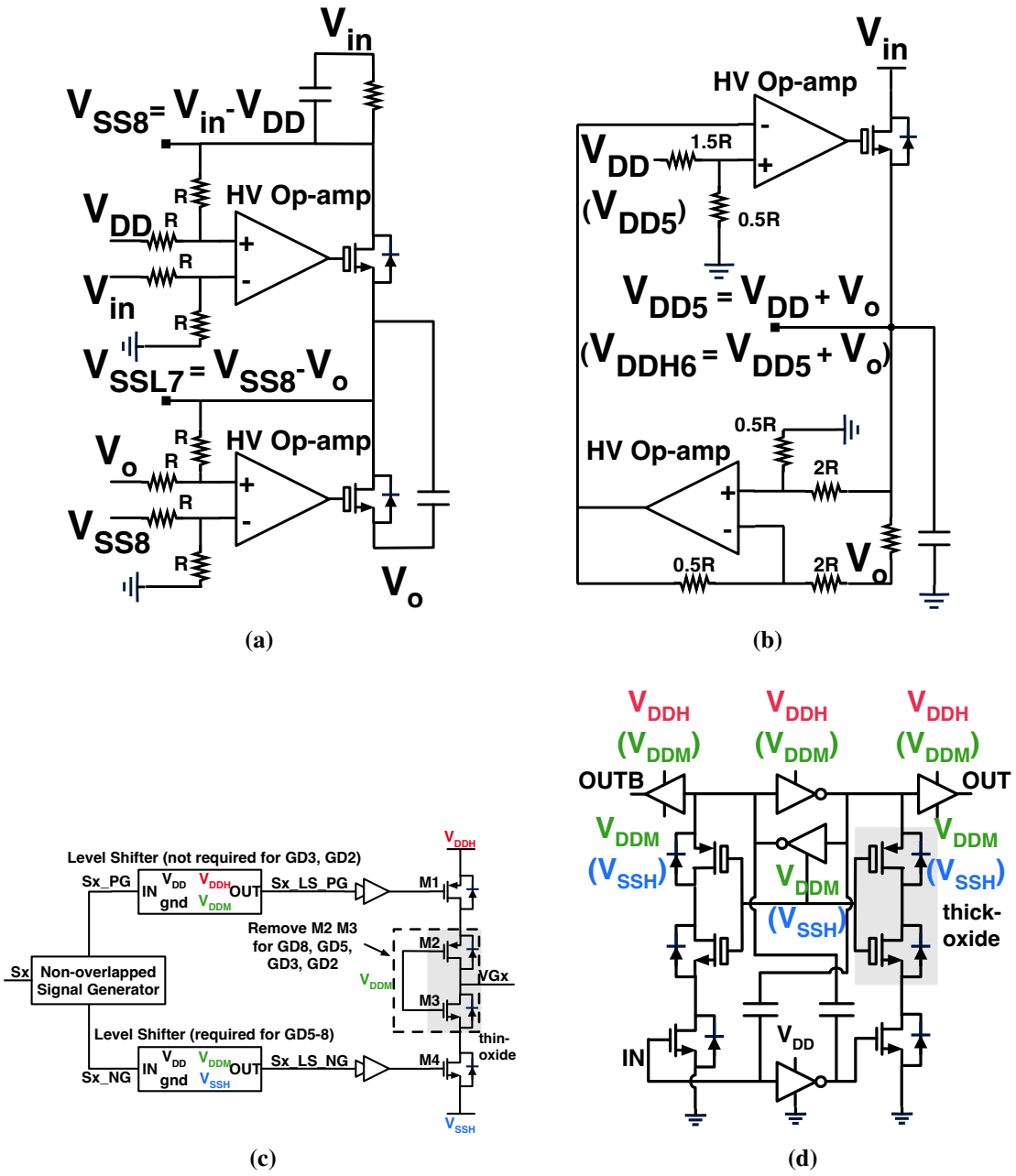


Figure 5.12. Block diagrams of (a) subtraction LR to generate V_{SS8} and V_{SSL7}, (b) summation LR to generate $V_{DD5}(V_{DDH6})$, (c) gate driver for Q6, and (d) level shifter.

Table 5.2. Source and gate voltages of each switch during ON and OFF intervals, when the ITSAB prototype is generating $V_o = 2.4\,\text{V}$ from $V_{in} = 9.6\,\text{V}$.

Switch	Source Voltage		Gate Voltage	
	ON	OFF	Low Swing	High Swing
Q8	V_{in} (9.6V)	V_{in} (9.6V)	V_{SS8} (6V)	V_{in} (9.6V)
Q7	$3V_{in}/4$ (7.2V)	V_{in} (9.6V)	V_{SSL7} (3.6V)	V_{in} (9.6V)
Q6	$V_{in}/2$ (4.8V)	$V_{in}/4$ (2.4V)	V_o (2.4V)	V_{DDH6} (8.4V)
Q5	$V_{in}/4$ (2.4V)	$V_{in}/4$ (2.4V)	V_o (2.4V)	V_{DD5} (6V)
Q1,4	$V_{in}/4$ (2.4V)	gnd (0V)	gnd (0V)	V_{DD5} (6V)
Q2,3	gnd (0V)	gnd (0V)	gnd (0V)	V_{DD} (3.6V)

power converter with multiple high-side switches. To overcome these obstacles, and to guarantee the same voltage (V_{DD}) over Vgs during ON time, regardless of the value of V_{in} and V_{DD}, fixed-level gate driver structures with the driver supply voltages generated by Linear Regulators (LR) are designed and presented in Fig. 5.12.

The subtraction LR, which is implemented using two high-voltage op-amps as shown in Fig. 5.12(a), is used to generate V_{SS8} and V_{SSL7}. The stacked structure is used to reduce power loss as the efficiency of a linear regulator depends on the voltage difference between its input and output voltage. Another type of LR is for summation function as shown in Fig. 5.12(b). Two circuits of this type are used for supplying V_{DD5} and V_{DDH6}, respectively. Two high voltage op-amps are connected so that the reference voltages are summed at the output. Both of the

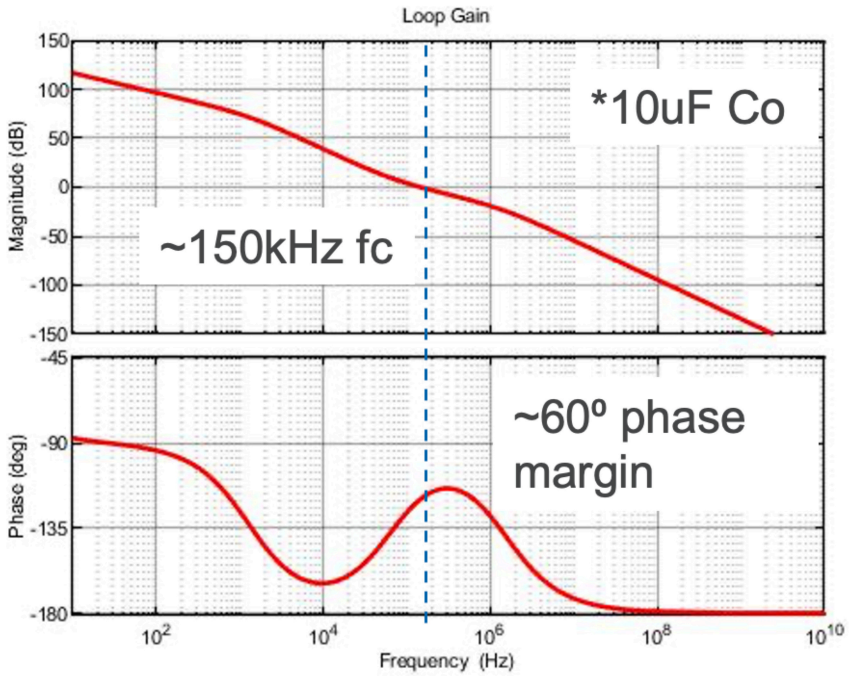


Figure 5.13. Magnitude and phase responses of the loop gain obtained under the following conditions: $V_{in} = 9.6\,\text{V}$, $V_o = 2.38\,\text{V}$, with $\sim 74\,\text{nH}$ parasitic inductors of the wire loops used to measure inductor currents, as shown in Fig. 5.15.

Subtraction LR and Summation LR recycle the residual charge to V_o to further save power.

As an example, the gate driver for Q6 is given in Fig. 5.12(c). To minimize the shoot-through current at the last stage of the gate driver, the PMOS M1 and NMOS M4 are driven separately with dead time created by the Non-overlapped Signal Generator at the front of this block. Stacking of M2 and M3 reduces the voltage stress on M1 and M4 so that when driving the switches with flying source voltages, such as Q1, Q4, Q6, Q7, it is still safe to use only thin-oxide devices. M2 and M3 are not present in the GD2, GD3, GD5 and GD8 gate drivers.

Level shifters are also required for non-gnd referenced signals. The level shifter circuit is shown in Fig. 5.12(d), with MiM capacitors used for coupling signals between different voltage domains with minimal latency while keeping small area. The cross-coupled inverters at the high voltage domain employ weak NMOS transistors to ensure rail-to-rail operation[9].

5.4.3 Control Loop Design

To achieve a large DC gain and adequate phase margin as well as fast closed-loop transient response, a proprtional-integral (PI, or Type-II) compensator is used in this implementation, as indicated in Fig. 5.10. An on-chip OTA together with PSM enables the design of a fast analog control loop. The control-to-output transfer function can be expressed as [46]:

$$\begin{aligned} \hat{I}_o &= \frac{V_{in}}{8Lf_s}\hat{\phi} = K_\phi \hat{\phi} \\ G(s) &= \frac{\hat{V}_o}{\hat{\phi}} = K_\phi \frac{1}{1+s/\omega_p} \end{aligned} \tag{5.23}$$

where $\omega_p = 1/R_L Co$. The transfer function of the compensator is

$$G_c(s) = G_0 \frac{1+\omega_z/s}{1+s/\omega_p} \tag{5.24}$$

where $G_0 = \frac{R2}{R1+R2}\frac{g_m R3C5}{C4+C5}$, $\omega_p = \frac{C4+C5}{R3C4C5}$ and $\omega_z = \frac{1}{R3C5}$. The position and connection of the passive components R1-R3, C4 and C5 are shown in Fig. 5.10. As part of the control loop, the ramp signal has the gain of $\frac{1}{2V_H}$, because its peak voltage is about $2V_H$. Consequently, the loop gain can be written as

$$T(s) = \frac{R_2}{R_1+R_2} G_c(s)G(s)\frac{1}{2V_H} \tag{5.25}$$

The system is designed to work at a switching frequency f_s of around 3 MHz. The crossover frequency f_c is selected to be around $f_s/10$. As (5.23) suggests, the system dynamic performance is highly related to the circuit parameters L, f_s, output capacitor Co and load current. Based on the values of passive components in the converter, the Type-II compensator is designed for 3 MHz switching frequency and 0.2 A load is listed in Table 5.3. The Bode plot of the computed loop gain is shown in Fig. 5.13. The designed 150 kHz crossover frequency and 60° phase margin ensure the fast response and stable operation.

Table 5.3. Components for the PI (Type-II) compensator.

Component	Details
C4	2.7 pF
C5	56 pF
R3	43.2 kΩ
R1,2	80 kΩ

5.5 Experimental Verification

Table 5.4. Components on the package substrate

Component	Details
C1	2 x 2.2 µF, 16 V 0402 (0.92 µF)
C2	2 x 10 µF, 10 V 0402 (4 µF)
C3	1 x 2.2 µF, 6.3 V 0201 (0.87 µF)
Cin(V_{in})	2 x 10 µF, 25 V 0603 (3.2 µF)
Cin(V_{DD})	1 x 10 µF, 10 V 0402 (2 µF)
Co	3 x 2.2 µF, 6.3 V 0201 (2.6 µF)
Decap(V_{DDH6})	2 x 1 µF, 16 V 0201 (304 nF)
Decap(V_{DD5})	1 x 1 µF, 16 V 0201 (244 nF)
Decap(V_{SS8})	2 x 1 µF, 16 V 0201 (408 nF)
Decap(V_{SSL7})	1 x 1 µF, 16 V 0201 (353 nF)
L1,3	10 nH, Ferric IPD or 0807SQ-Coilcraft

The demonstration chip was fabricated in TSMC 130 nm BCD technology with a dimension of 1.9 mm × 1.7 mm as indicated in Fig. 5.14(a). Aiming for a high power density performance, the chip die was flip-chipped on a $6.5 \times 6.5\,mm^2$ 6-layer organic package substrate

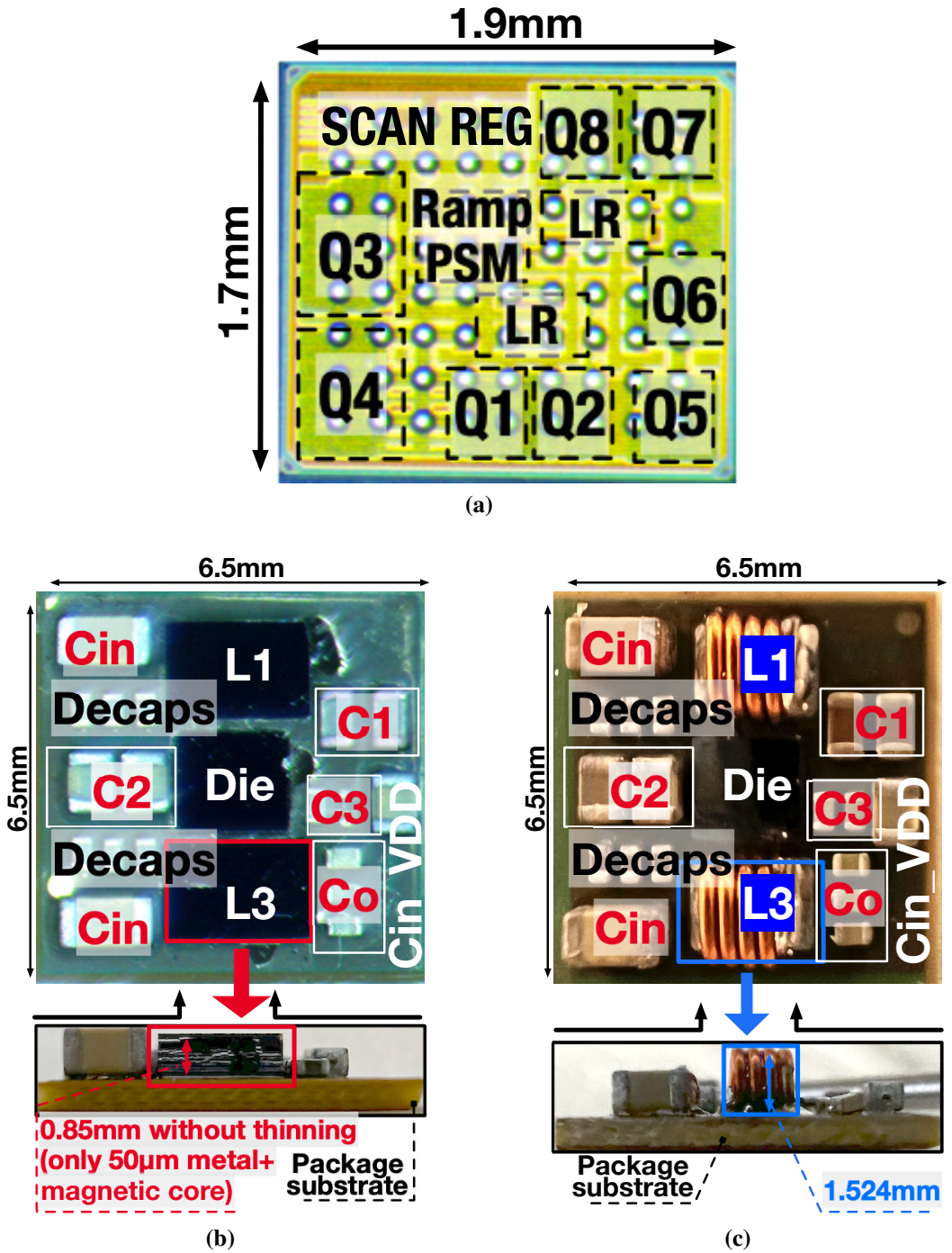


Figure 5.14. Top and side views of the ITSAB converter prototype, including (a) 1.7 mm × 1.9 mm die in a 130 nm BCD process, and 6.5 mm × 6.5 mm package substrate with flip-chipped die, power capacitors and 2 × 10 nH (b) IPD inductors or (c) discrete (Coilcraft 0807SQ-10N) inductors.

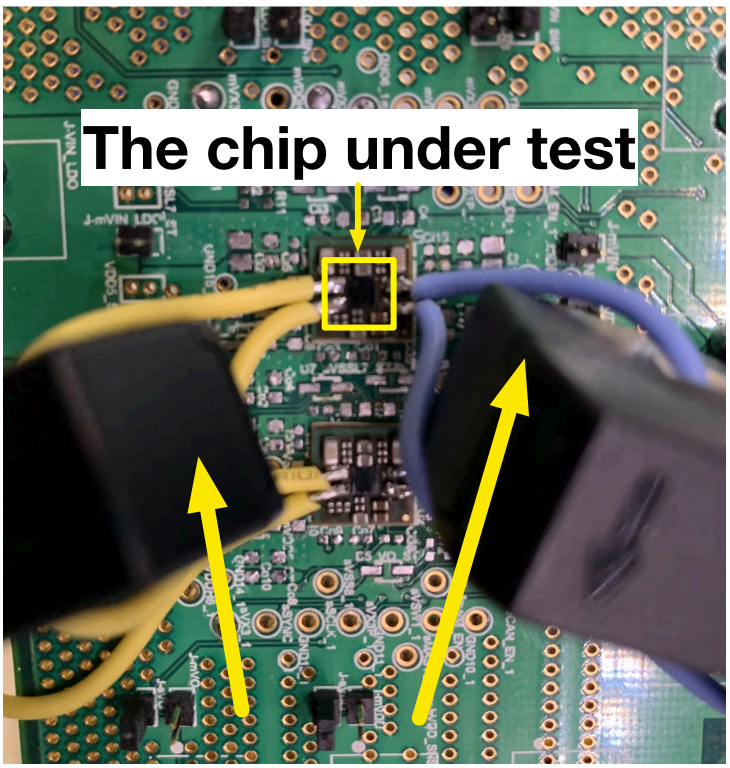


Figure 5.15. Current-measurement test setup with wire loops having ($\sim$ 74 nH parasitic inductances serving as the power-stage inductors.

together with flying capacitors, decoupling capacitors, input/output capacitors and two 10 nH IPD inductors supplied by Ferric Semiconductor. Note that the IPD inductors promise much higher power density because they achieve a thickness of 50 μm (plus 800 μm unused silicon carrier as shown in Fig. 5.14(b), which could be thinned substantially down to 10s μm), while discrete inductors are 1.524 mm thick. While the flip-chip die has 180 μm bump pitch, the organic substrate has a ball grid array (BGA) with 0.8 mm ball pitch to reduce the cost of the PCB. The details of each passive component are listed in the Table 5.4. The selection of the flying capacitors guarantees the actual capacitance of C1 and C3 are equal and much less than the one of C2 so that R_o and f_o are relatively the same for both LC tanks.

Since the design uses small inductors of 10 nH, any additional wires with reasonable length added in series with the inductors to allow measuring their currents with current probes would add significant inductance beyond the inductors themselves. Therefore, to measure

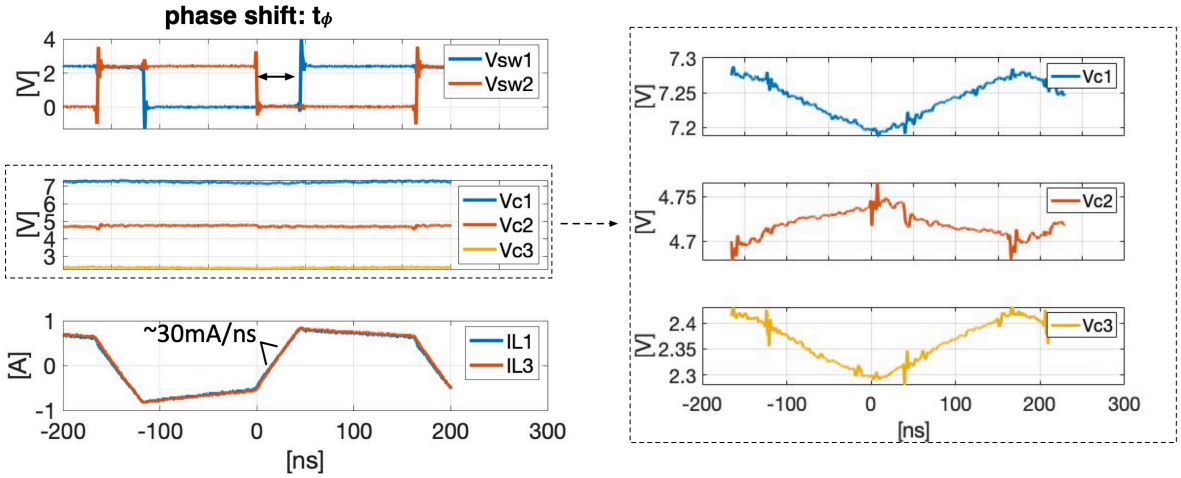


Figure 5.16. Measured steady-state converter waveforms, with 74 nH inductors due to the current measurement setup shown in Fig. 5.15. The converter operates at $V_{in} = 9.6\,\text{V}$, $V_o = 2.38\,\text{V}$, $I_o = 1\,\text{A}$.

operational waveforms, the inductors are removed and replaced by two short wire loops, as shown in Fig. 5.15. Note that even when the two wires are sized just long enough to clip the small current probes, their effective parasitic inductances are approximately 74 nH, which is about 7× more than the inductors used on the package. The significantly larger wire-loop inductances limit the maximum load current according to (5.2), but the measurement setup still provides verification of operating waveforms at light to medium loads.

Fig. 5.16 shows the measured steady-state waveforms of switching node voltages V_{sw1}

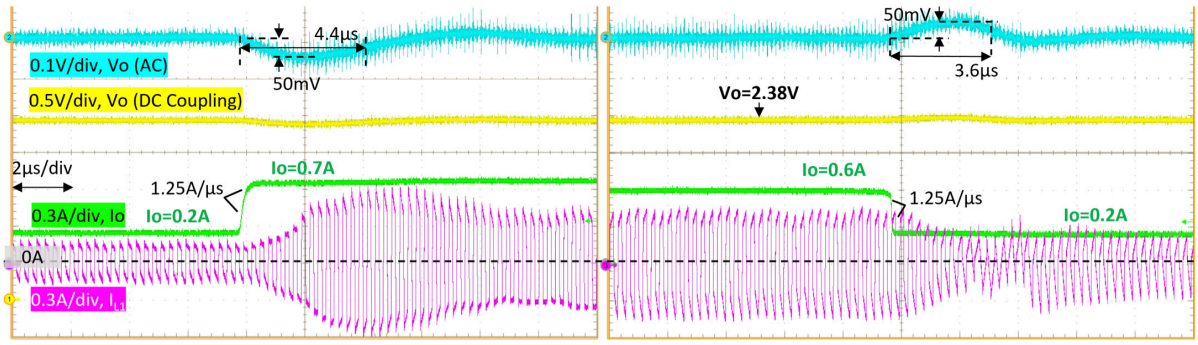


Figure 5.17. Step-load transient responses of the experimental prototype operating at $f_s = 3\,\text{MHz}$ with wire loops as inductors. The output voltage is closed-loop regulated at $V_o = 2.38\,\text{V}$ from $V_{in} = 9.6\,\text{V}$.

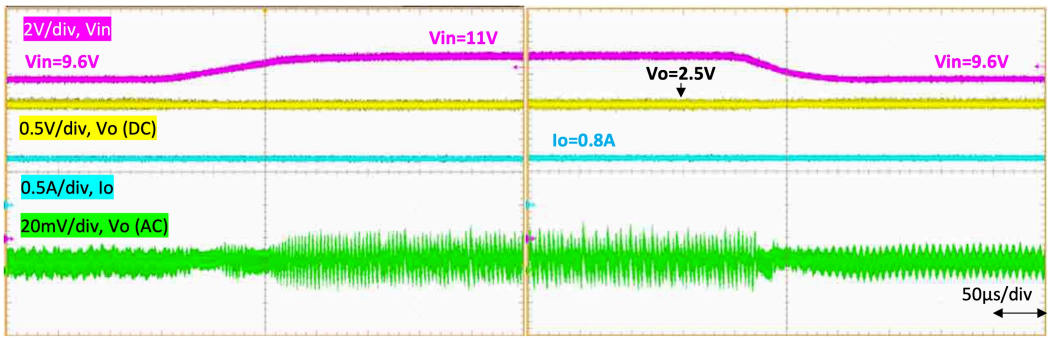


Figure 5.18. Line transient responses of the experimental prototype operating at $f_s = 3.8\,\text{MHz}$ with 10 nH discrete inductors. The output is closed-loop regulated at $V_o = 2.5\,\text{V}$.

and V_{sw2}, flying capacitor voltages, and inductor currents. The noticeable time difference between V_{sw1} and V_{sw2} is the phase shift time t_ϕ, during which the inductors are magnetized or demagnetized with a slope of $\sim 30\,\text{mA/ns}$, implying $\sim 74\,\text{nH}$ parasitic inductance of the wires. The top of I_{L1} and I_{L3} is not as flat as in the theoretical waveforms in Fig. 5.3 due to the additional path resistances. The flying capacitor voltages are measured by a differential probe, verifying the soft charging behavior as discussed in Section 5.1.

The synchronization feature is verified by running two ITSAB converters at the same time. The phases are set up by two 180^o-phase-shifted synchronization control signals generated by an FPGA, which also allows any other amount of phase shift if more converters are connected in parallel for a larger load. The measured switching node V_{sw2} voltages and the inductor current I_{L1} for both converters are shown in Fig. 5.20.

Fast closed-loop load-step transient performance is measured at a 9.6 V-to-2.38 V conversion and $f_s = 3\,\text{MHz}$, with 0.5 A and 0.4 A load steps. The waveforms of AC-coupled and DC-coupled output voltage V_o, output current I_o and inductor current I_{L1} are shown in Fig. 5.17. Corresponding to the two load steps, the output voltage takes $4.4\,\mu\text{s}$ and $3.6\,\mu\text{s}$ to settle within 1%, and the undershoot and overshoot during the step-load transients are within 2% of its DC value. In addition, the full-load step response is performed on the prototype with 10 nH discrete inductors as in Fig. 5.14(c). V_o settles in $14\,\mu\text{s}$ and $10\,\mu\text{s}$ with undershoot and overshoot of 30 mV when responding to 2.3 A step load as shown in Fig. 5.19.

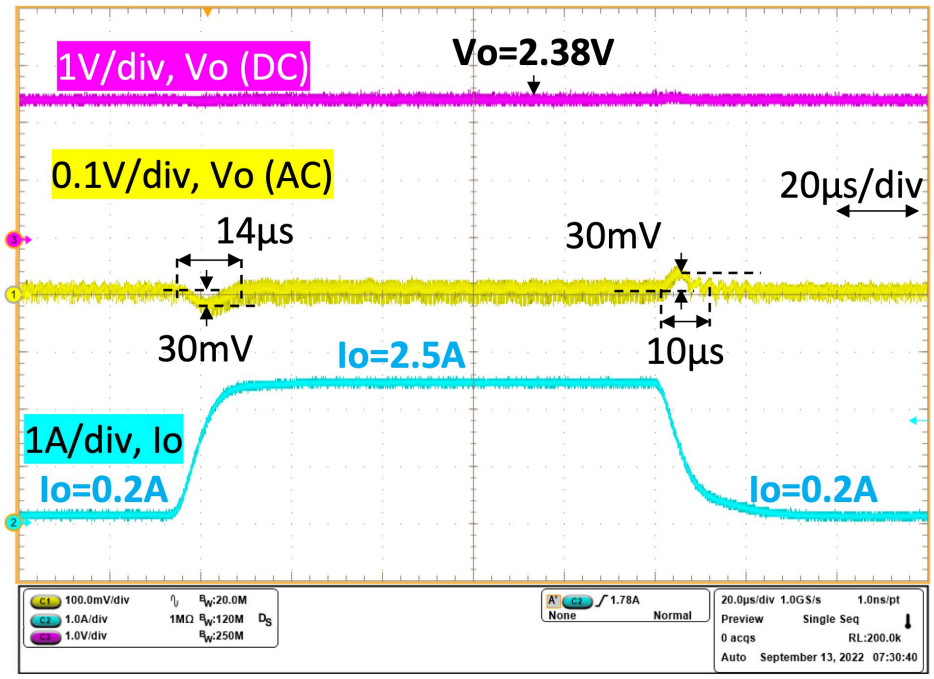


Figure 5.19. Step-load transient responses of the experimental prototype with 10 nH discrete inductors operating at $f_s = 3.8$ MHz. The output is closed-loop regulated at $V_o = 2.38$ V from $V_{in} = 9.6$ V.

A line transient of 1.4 V step at V_{in} is performed on the experimental prototype that has two 10 nH discrete inductors and operates at 1 A load. As shown in Fig. 5.18, V_o is well regulated to 2.5 V with no significant fluctuation.

On Fig. 5.21, the efficiency is measured with two types of inductors, discrete and IPD, at various input/output voltages and different switching frequencies. The peak efficiency measured at 9.6 V/2.33 V, 3.1 MHz, 1 A load is 92.4% with 0807SQ discrete inductors, compared to 91.2% with Ferric IPD inductors at 0.6 A. The efficiency difference between the prototypes with two types of inductors is largely caused by the large difference in the inductor series resistance, which is consistent with the differences in size. Fig. 5.21(a) also illustrates the matched efficiency between analytical calculation and simulation in addition to the drop in measurement results. This is largely due to the paths and connection resistances and capacitances in both the silicon layout and the PCB prototype. The additional resistances not only directly affect the conduction loss, but also result in larger inductor current ripple, which further increases the total conduction

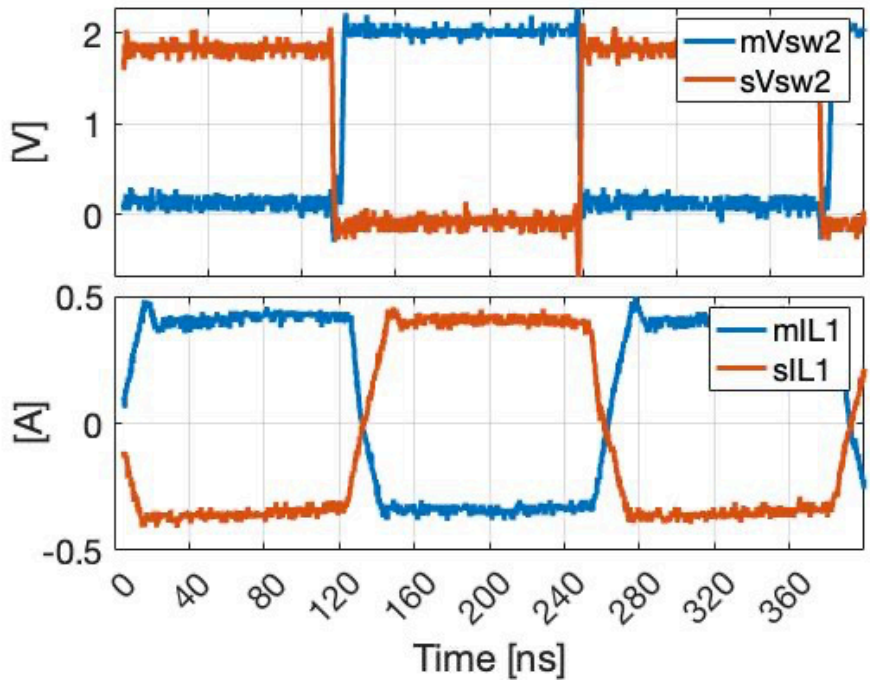
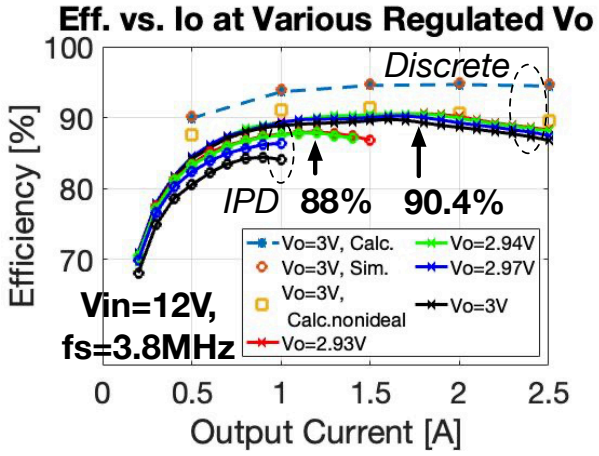


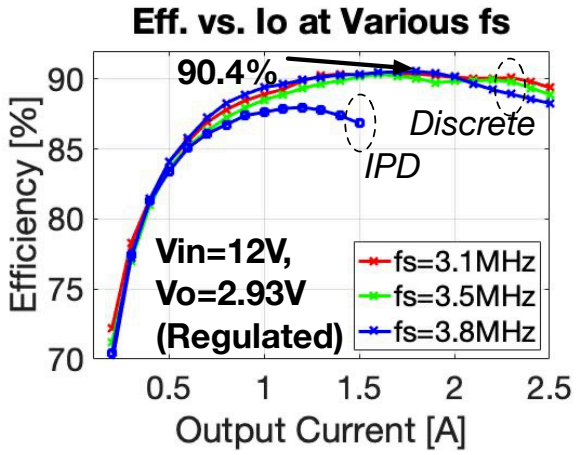
Figure 5.20. V_{sw2} and I_{L1} of two converters (m and s) with 180° phase shift @8.2 V/2 V, 3.8 MHz, 1 A (0.5 A each), open-loop.

loss across all the load conditions. An additional efficiency calculation considering 50% more on-resistance due to paths and vias on silicon layout, 30% more parasitic resistance from PCB routing and connection, and 40% more parasitic capacitance from dense layout routing is plotted in Fig. 5.21(a), which shows an excellent match with the measurement results.

The converter prototype is also tested for its output regulation range. As shown in Fig. 5.22, the output voltage ranges from 2.15 V to 2.65 V and 2.7 V to 3.3 V with an input voltage of 9.6 V and 12 V, respectively. The lower boundary of V_o is set once there is zero phase shift, meaning the inductors couple and resonate directly with $C1,3$ and deliver charge to the output during states 1 and 3, without the charging states 2 and 4. The peak values of I_{L1} and I_{L3} are determined by f_o and f_s as well as the desired load current. On the other hand, the upper boundary is limited by maximum phase shift ratio which is one quarter of T_s as calculated from (5.2) and Section 5.4.1. Hence, the upper boundary of V_o can be larger than the measured values. However, as the inductors are charged longer time during states 2 and 4, the peak current can be



(a)



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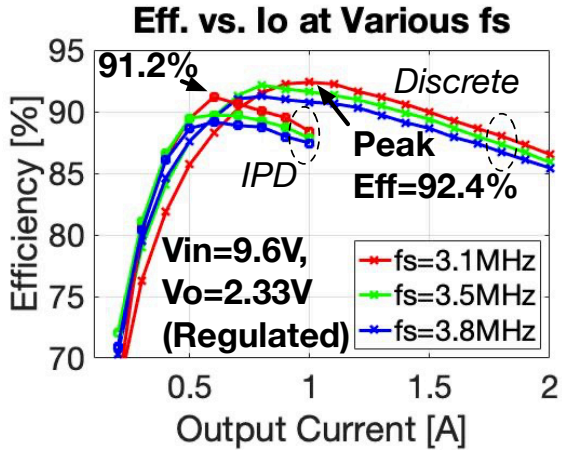


(c)

Figure 5.21. Efficiency vs. load current I_o measured at (a) $V_{in} = 12\,\text{V}$, $f_s = 3.8\,\text{MHz}$, various V_o, (b) $V_{in} = 12\,\text{V}$, $V_o = 2.93\,\text{V}$, various f_s, and (c) $V_{in} = 9.6\,\text{V}$, $V_o = 2.33\,\text{V}$, various f_s.

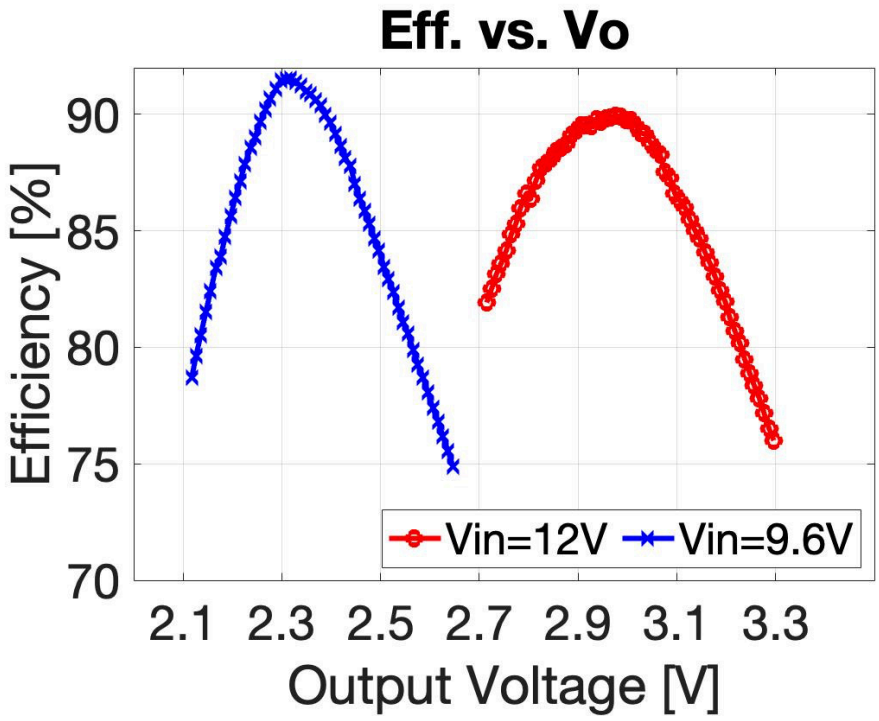


Figure 5.22. Efficiency vs. V_o at 1 A load, 3.8 MHz f_s.

significantly larger than the saturation current of small and integrated inductors. The large RMS currents in steady state can also be detrimental for other parts of the circuits, including the power switches and capacitors. To keep the prototype in a safe and reliable operating region, a range of $\pm 10\%$ of nominal V_o is chosen for the demonstration. In this output voltage range, the efficiency remains greater than 75%.

The power density of the prototype with IPD inductors is about two times larger compared to the power density of the prototype with the discrete inductors, counting the volume of the active die, the flying capacitors and the effective inductors volume. The comparison is summarized in Table 5.5. One may note that the package substrate is not fully optimized for power density. As indicated by the thermal image in Fig. 5.23, which is measured at 12 V/2.93 V, 3.8 MHz, 1.5 A load, the temperature rise is only $10^{\circ}C$ from the room temperature. This suggests that a finer pitch package design can be utilized to further increase the overall power density.

The connection of inductors and capacitors in ITSAB converter form resonant tanks similar to well-known resonant converters. In contrast, however, the ITSAB converter requires

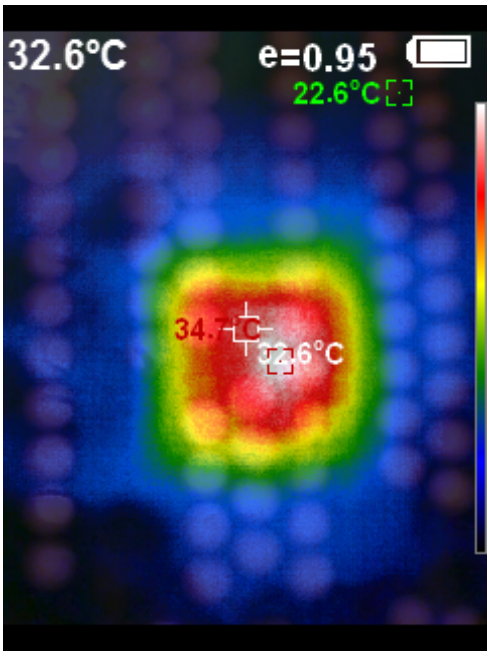


Figure 5.23. Thermal image of the prototype with IPD inductors taken at full load (1.5 A).

Table 5.5. Performance comparison: discrete vs. IPD inductors

Inductor		V_{in}/V_o	$I_{o,max}$ [A]	Peak Eff. @I_o	Pout,max [W]	Peak power density [W/mm^3]*
10 nH	Discrete	9.6 V/2.33 V	2.5	92.4% @1 A	7.5	0.62
	IPD	9.6 V/2.33 V	1.5	91.2% @0.6 A	4.4	1.36

*Space counts active die, flying capacitors and effective inductors volume only.

less inductance and much lower switching frequency because of phase shift modulation, although both these types of converters achieve best efficiency at nominal conversion ratio, i.e. 4. Moreover, as (5.23) suggests, ITSAB converter is a first-order system, which allows for faster closed-loop design and transient responses.

The proposed ITSAB converter employs only two 10 nH inductors, at least 1.8× smaller values compared to the state-of-the-art designs with otherwise similar specifications, as shown in the comparison Table 5.6. Because of the small inductors, the prototype converter has an outstanding power density of 1.36 W/mm^3. Furthermore, it is capable of operating over a wide input and output range with similar peak efficiency of 92.4%. As summarized in Table 5.7, the ITSAB converter in this paper exhibits an effort to overcome challenges in other types of converter that either require much larger inductors (conventional hybrid converter), have no

Table 5.6. Comparison with prior works

	This Work	[4]	[5]	[6]	[7]	[8]
Topology	**ITSAB**	Tri-State DSD	3:1 ReSC	Hybrid SC	Hybrid Dickson	Cascade Hybrid
Technology	**130 nm**	180 nm	180 nm	130 nm	65 nm	180 nm
Inductor	**2x10 nH**	2x560 nH	36 nH	1 μH	180 nH	240 nH
Inductor switching frequency	**2-5 MHz**	200 k-2 MHz	1.7 MHz	2.3 MHz	400 k-10 MHz	1.5 MHz*
Input voltage [V]	$V_{in} \geq 9V$				$V_{in}<9V$	
	9.6-12	12/24	12	9	3-4.5	4-6
Output voltage [V]	**2.15-3.3**	1	3.5-3.8	3-4.2	0.3-1	0.4-1.2
Peak output current [A]	**2.5**	3	1.24*	3.4	1.53	1
Peak power density [W/mm^3] ***	**1.36 @ 4.1****	0.06 @ 12*	1.12 @ 3.4*	0.41 @ 2.7*	0.14 @ 5.2*	0.18 @ 4.5*
Efficiency [%] @ CR	**92.4 @ 4.12**	91.2 @ 12	82 @ 3.4	94.3 @ 2.5	88.3 @ 5.2	96.9 @ 4.2
Regulation Method	**Phase shift modulation**	Duty cycle	Deadtime control	Duty cycle	Duty cycle	Ripple injection
Package	**Flip-chip**	Wire-bonding	Flip-chip	Flip-chip	Flip-chip	Wire-bonding

*Estimation from reported measurement results, **Assuming Ferric IPD inductor being used

***Area counts active die, flying capacitors and inductors only. Calculated at given conversion ratio (CR)=V_{in}/V_o

Table 5.7. Comparison between converter topologies

Converter	Inductor	Regulation	Efficiency
Resonant	tens to hundreds of nH	Limited in most cases	Good
Switched-capacitor (SC)	N/A	Limited	Poor trade-off with regulation
Conventional hybrid	hundreds of nH to μH	Yes	Good
ITSAB converter (this work)	**up to tens of nH**	**Yes**	**Good**

regulation or difficulty in achieving regulation together with high efficiency and compact size (resonant converter), or suffer from lower efficiency for fine regulation (SC converter).

5.6 Summary

In this chapter, a new hybrid converter, named integrated transformerless stacked active bridge (ITSAB) converter, is presented. It requires only 10 nH inductors, while operating at a modest switching frequency in the MHz range. A voltage regulation approach is provided as well as a detailed loss analysis for the ITSAB converter. Additionally, an augmented state space method is employed to accurately calculate the inductor current waveshapes and RMS values. A novel optimization methodology is described, which is used to determine passive components, switching frequency and areas of the power devices so as to minimize the total loss. Moreover, circuit design details are provided for the key sub-blocks, including an adaptive gate driver design and phase-shifted control signal generation. The article also includes an analysis of open-loop control-to-output frequency responses, based on which a voltage control loop with a PI (Type-II) compensator is designed.

To validate operation and design of the proposed ITSAB converter, the power stage and the controller are implemented and fabricated on a 1.7 mm $\times$ 1.9 mm die in a 130 nm BCD process. Two prototypes are constructed: one with Ferric IPD inductors and another one with discrete air-core inductors, both using an organic substrate and BGA package to house the flip-chip die, power capacitors and the inductors. Steady-state operation and load transients are verified by replacing the discrete inductors with two wire loops to facilitate capturing of inductor

currents. Peak efficiencies of 91.2% and 92.4%, which are comparable to prior works, are measured for the two prototypes operating from 9.6-12 V input to 2.15-3.3 V output, respectively. Thanks to the low inductance requirements, and the usage of IPD inductors, the ITSAB converter prototype reaches a superior maximum power density of $1.36\,\mathrm{W/mm^3}$.

5.7 Acknowledgements

This chapter, in full, is a reprint of the materials as they appear in 2022 IEEE Custom Integrated Circuits Conference (CICC) and IEEE Journal of Solid-State Circuits. Tianshi Xie; J. Zhu, T. Byrd, D. Maksimovic, and H. Le, "A 0.66 W/mm2 Power Density, 92.4% Peak Efficiency Hybrid Converter with nH-Scale Inductors for 12 V System," in 2022 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2022. Tianshi Xie; J. Zhu, D. Maksimovic and H. -P. Le, "A Highly Integrated Hybrid DC–DC Converter With nH-Scale IPD Inductors," in IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 705-719, March 2023, doi: 10.1109/JSSC.2022.3227163. The dissertation author was the primary investigator and author of these papers.

Chapter 6

ITSAB Converter for Heavy-Load Applications

As addressed in Chapter. 1, the demanding power for HPC continuously soars. Moreover, the miniaturization trend desires monolithic solutions. One chip or one package that supplies as much power as possible becomes a viable solution. As a consequence, co-design of chip die, which integrates power switches together with all the gate drivers and their supporting analog and digital blocks, with power inductors, which is proved to be the bottleneck of high power density design, is crucial. In this chapter, the design of a high-power version of ITSAB converter using the previously introduced methodology is presented together with an overview of a high power inductor.

6.1 System Design of High-Power ITSAB Converter

Targeting one compact package, the desired design would be sketched as Fig. 6.1, which shows top view, side view and bottom view of the package. The coppers with net names are labeled in different colors to show the preliminary floorplan. The chip die will be flipped on one side of the PCB, while two inductors are mounted on the other side of the PCB beneath the chip die so that the overall volume of the package is minimized. There are three sets of flying capacitors, C_1, C_2 and C_3. Because of de-rating effect due to voltage stress, each of them usually has nominal value two to three times of the actual capacitance needed. To maintain low ESR and

to constrain the overall volume, four 0402 package capacitors are paralleled to form C_1 and C_2, two 0201 package capacitors are paralleled to form C_3.

Different from the package design in ITSAB converter introduced in Chapter. 5, the high-power ITSAB converter distributes components on both sides of substrate. Specifically, the big components, such as the chip die and the inductors, are placed on each side of the substrate to save the overall volume. The inductors are about 3.5 mm x 2.5 mm. To cover this area, the desired chip die area should be around 3.5 mm x 5 mm, which is the sum of the area of two inductors. From the 3D floorplan given in Fig. 6.1, this area is roughly the maximum allowable number of the chip die area, and this die area is desired, as the area is proportional to the maximum output power delivered by the converter.

Giving a little bit of headroom, the chip is designed in 3 mm x 5 mm. Based on the current density of each power switch, the chip die area can be divided into the following ratio. Basically, $Q1,2$ are the same area as $Q5,6$ and half of $Q3,4$. Because $Q7,8$ are PMOS, their area is roughly assigned as 1.5 X of $Q1,2$.

Table 6.1. Optimization results.

Area	Ratio
Q1, Q2 area	1 X
Q3, Q4 area	2 X
Q5, Q6 area	1 X
Q7, Q8 area	1.5 X

After taking the area of gate drivers and peripheral circuits into consideration, using the optimization methodology given in Chapter. 5, the resulted components selection and the converter operating parameters as well as the size of power switches are listed in Table. 6.2.

The operating frequency is significantly lower than the low power ITSAB converter because the switch sizes for the high-power one are a lot larger and thus much higher parasitic capacitance. From the loss analysis presented in Section. 5.2, to reduce the switching loss, a

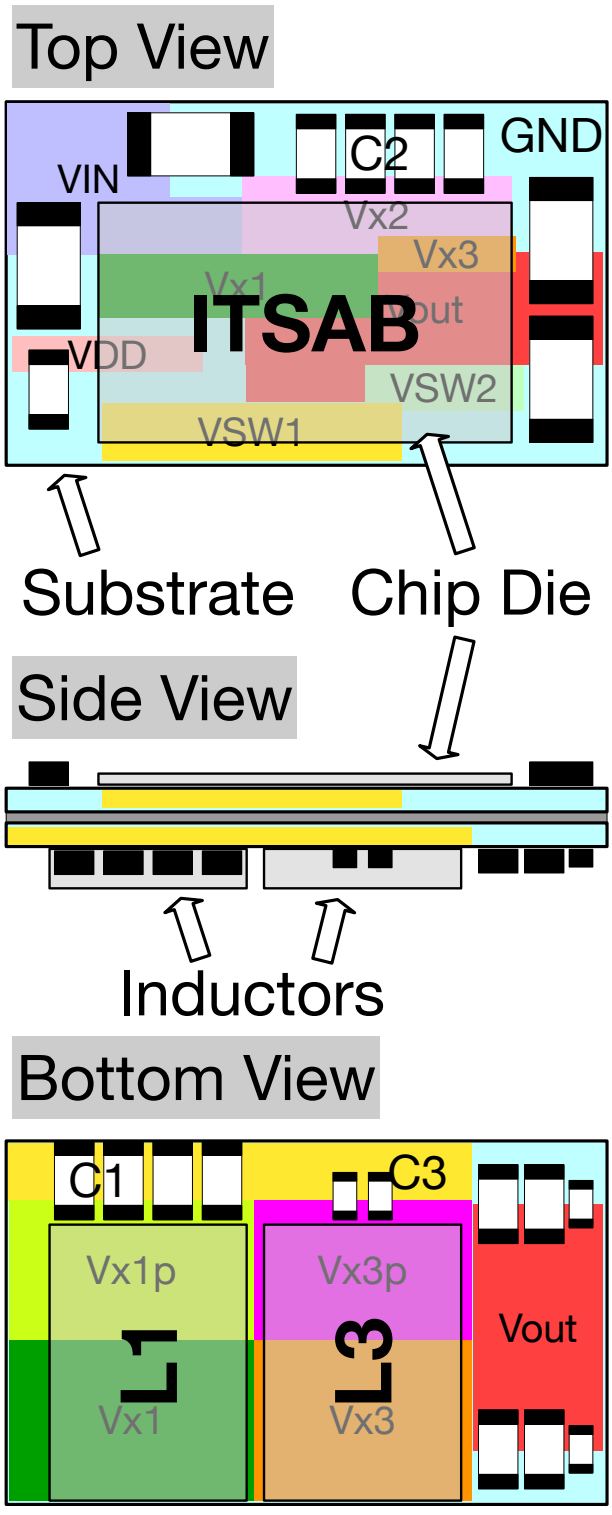


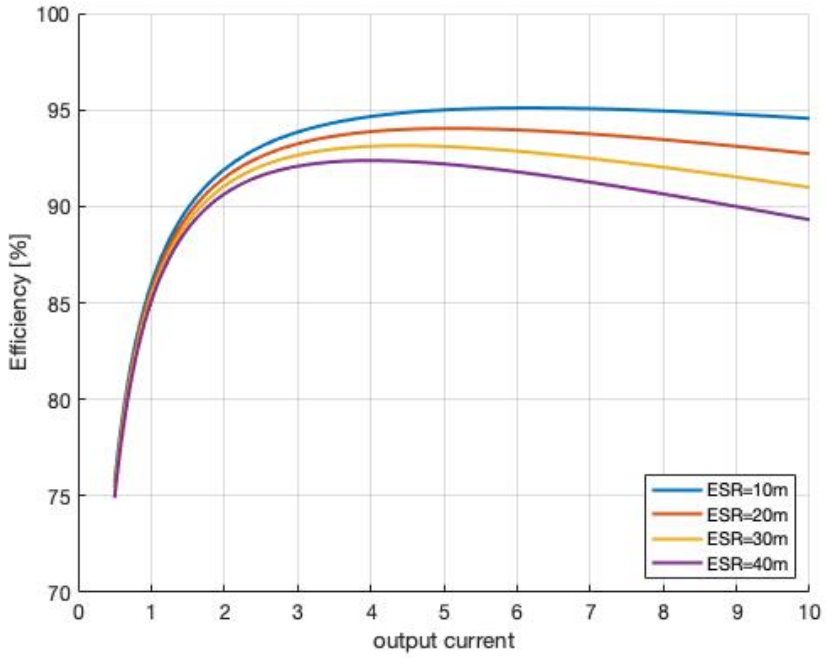
Figure 6.1. 3D floorplan of high power ITSAB converter package

Table 6.2. High-power ITSAB converter optimization results.

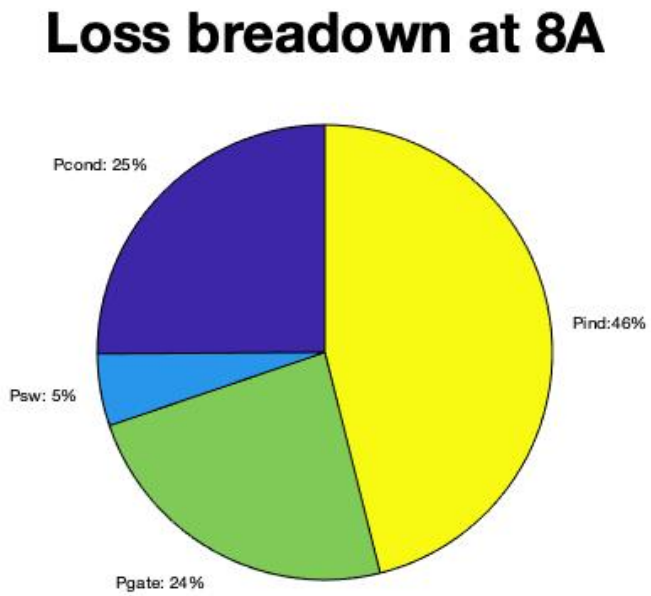
Parameters	**Details**
L	10 nH
C1, C3	1.75 μF
C2	4 μF
f_s	2.1 MHz
Q1, Q2 area	0.882 mm^2
Q3, Q4 area	1.812 mm^2
Q5, Q6 area	0.866 mm^2
Q7, Q8 area	1.343 mm^2

lower switching frequency is required. Meanwhile, to keep $k = \frac{f_s}{f_o}$ much greater than 1, larger capacitance is therefore desired. The area of each power switch is measured directly from the chip layout and therefore does not strictly follow the ratio given in Table. 6.1.

The theoretical efficiency and loss breakdown at 8 A load are shown in Fig. 6.2. Apparently, the ESR of inductors affects the efficiency at heavy load. But at light load, unless shrinking the size of switches or reducing the switching frequency, which are not applicable for high-power applications, the efficiency can hardly be improved. To enhance the light load efficiency, a special switch partitioning approach is applied. Fundamentally, only one quarter of each switch is turned on at light load so that a total gate capacitance of $\frac{C_{gg}}{4}$ instead of C_{gg} is switched and thus P_{gate} is decreased by three quarters. The resulted efficiency is plotted in Fig. 6.3 on top of the efficiency curve with $20 m\Omega$ inductor ESR and the entire power switch. It shows 15% loss reduction at light load. The detailed circuit design for this switch partitioning function will be introduced in Section. 6.2.1.



(a)



(b)

Figure 6.2. (a) efficiency with different inductor ESRs; (b) Loss breakdown at 8 A load

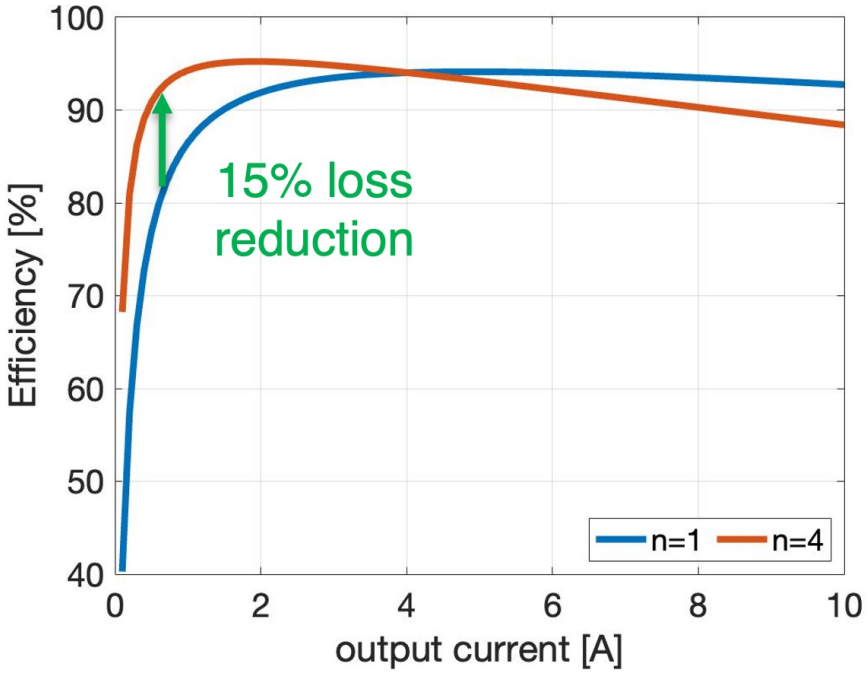


Figure 6.3. Efficiency improvement with switch partitioning

6.2 Circuit Design of High-Power ITSAB Converter

While the major analog blocks, such as Ramp Generator (RG), Phase Shift Modulator (PSM), OTA, gate drivers and Linear Regulator (LR), are inherited from the low-power ITSAB design and only scaled with switching frequency and switch size, two other blocks including switch partitioning logic cell and fine-tuned deadtime generator are newly added to support high-power circuit requirement.

6.2.1 Switch Partitioning

The power switch is divided into two pieces: one quarter (x1) and three quarters (x3) of the switch. The according gate driver must be also separated into one quarter and three quarters of the original size as designed in Fig. 5.12c. Specifically, the last stage of gate driver, which is an inverter or an inverter with stacked PMOS and NMOS, is divided into two cells to drive x1 and x3 power switches, respectively. For simplicity, the last stage inverter and its PMOS,

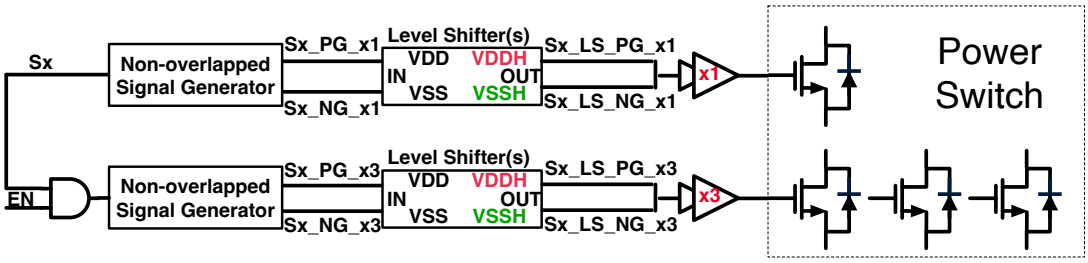


Figure 6.4. (redraw with signal names, 1x to x1) Block diagram of switch partitioning circuit

NMOS drivers are lumped in one gate driver symbol with ”x1” or ”x3” marked on it. The Non-overlapped Signal Generator (SG) is required for each VDD-domain driving signal S_x, as some deadtime is needed between the driving signals of the last stage inverter PMOS (S_x_PG) and NMOS (S_x_NG) to prevent shoot-through current. The following level shifter is required for every gate driver except GD2 and GD3. Again, the level shifter symbol in Fig. 6.4 represents one or two level shifters for S_x_PG and S_x_NG to generate $S_x\_LS\_PG$ and $S_x\_LS\_NG$, respectively, for PMOS and NMOS drivers. Every level shifter is the same as the design in Fig. 5.12d no matter x1 or x3 power switch is driven. There is an enable signal EN at front to control ON/OFF of the driving chain of x3 switch.

6.2.2 Fine-tuned Deadtime Generator

The deadtime generator is to produce proper deadtime to achieve soft-switching while avoiding shoot-through current. For ITSAB converter, since the inductors are only 10 nH, the inductor currents ramp up in a very steep slope, for example 3.3 ns of ramping time for 1 A load 12 V input. This creates a big challenge for deadtime tuning. Particularly at light load where the switching loss is dominant, it desires to achieve complete soft-switching for Q_3 and Q_4 while keeping body diode from conducting current. It’s even more critical for high-power converter which has larger switches and thus higher switching loss if soft-switching fails. Moreover, the body diode conduction loss, which is proportional to the flowing current, can be significant at heavy load and becomes one major obstacle for achieving desired high output power, yet to mention the potential latch-up issue caused by reverse conduction within an integrated power

switch. All in all, a fine-tuned deadtime generator is required for ITSAB converter, especially for a high-power design.

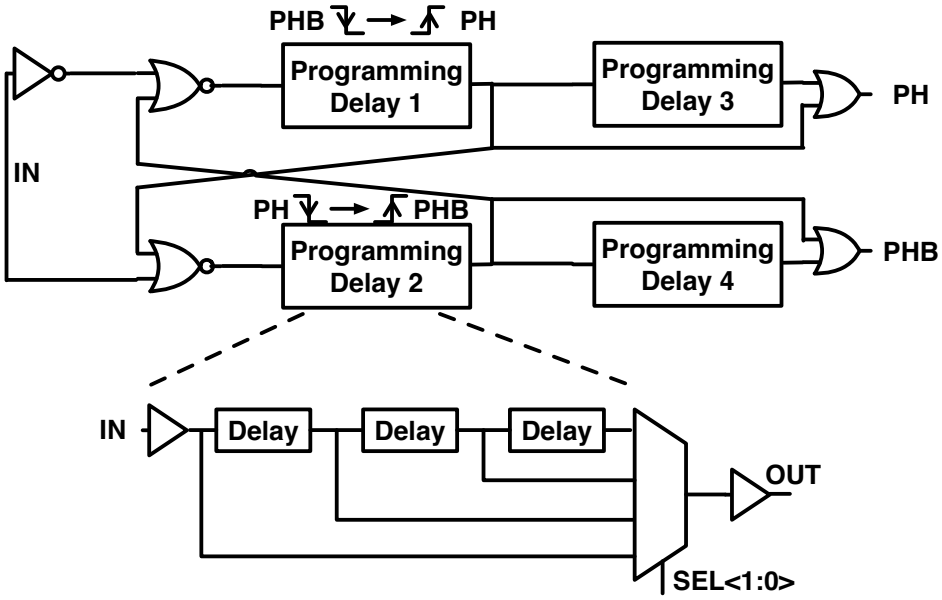


Figure 6.5. Block diagram of fine-tuned deadtime generator

The fine-tuned deadtime generator is sketched as Fig. 6.5, which is constructed from basic SR Latch. The rising edge of input signal *IN* sets the rising edge of *PH* and the trailing edge of *PHB*, while the trailing edge of *IN* resets *PH* and sets *PHB*. There are total 4 Programming Delay (PD) blocks. The PD#1 determines the deadtime from trailing edge of *PHB* to rising edge of *PH*, whereas PD#2 configures the deadtime between the trailing edge of *PH* and the rising edge of *PHB*. The presence of PD#3 pushes the trailing edge of *PH* to a later time. In other words, the total deadtime from the trailing edge of *PH* to the rising edge of *PHB* is the delay of PD#2 minus the one of PD#3. It's the same mechanism for generating the other deadtime by taking the difference between PD#1 and PD#4. The benefit of adding PD#3 and PD#4 is to compensate for any delay on the signal paths that causing none-zero deadtime even when PD#1 and PD#2 are set to zero. To gain the fine-tuned capability while maintaining wide range of tuning, each of PD#1 and PD#2 contains 18-bit Short Delay (SD) and 2-bit Long Delay (LD) blocks. Each of SD and LD block is made of several basic 2-bit programmable delay block as

indicated at the bottom of Fig. 6.5. The basic cell can be programmed from zero delay to 3 units of delay. For SD block, each of this unit delay is 80 ps/bit and this number is 1 ns/bit for each unit delay in LD block. That means the total deadtime ranges from 0 to 5.16 ns with 80 ps step. PD#3 and PD#4 are the same as 2-bit LD block.

6.3 Experiment Results

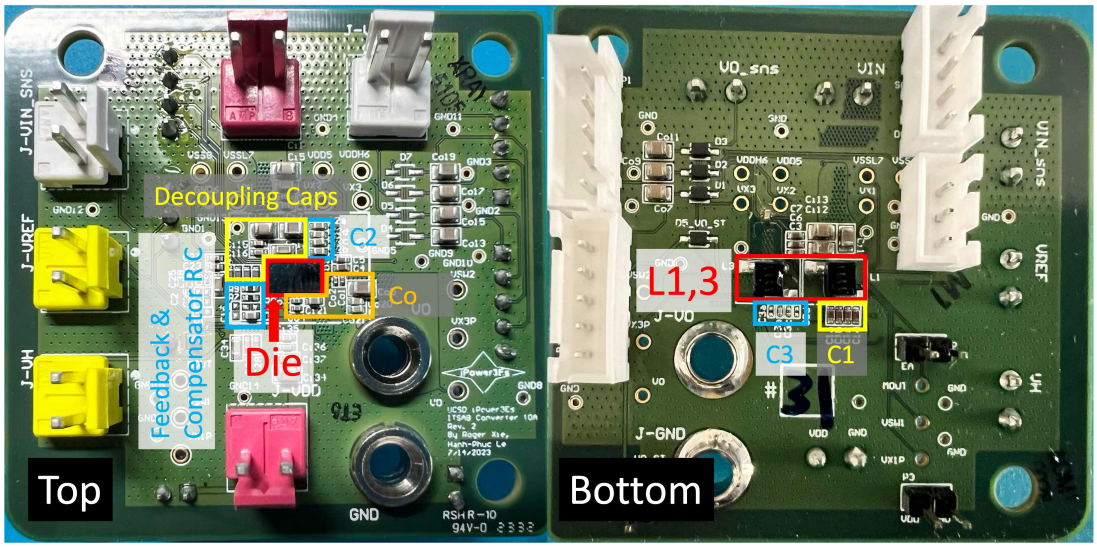


Figure 6.6. PCB prototype of high-power ITSAB converter

To evaluate the performance of this high-power ITSAB converter, a PCB prototype is designed and measured. Different from the demonstration PCB designed for low-power ITSAB converter in Chapter. 5, where all the power components are mounted on one fine-pitch substrate, the one for high-power ITSAB converter places components on both sides of PCB as enlightened by the 3D floorplan in Fig. 6.1. Specifically, the chip die, which is integrated with all the power switches and analog/mixed-signal blocks, is flipped-chip on the top side of the PCB together with the flying capacitor $C2$, input and output capacitors as well as resistors and capacitors for feedback loop. While on the bottom side of the PCB, inductors $L1$ and $L3$ are soldered beneath the position of the chip die surrounding by the other two flying capacitors $C1$ and $C3$. The part numbers and the details of each component are listed in Table. 6.3. Note that the flying capacitors

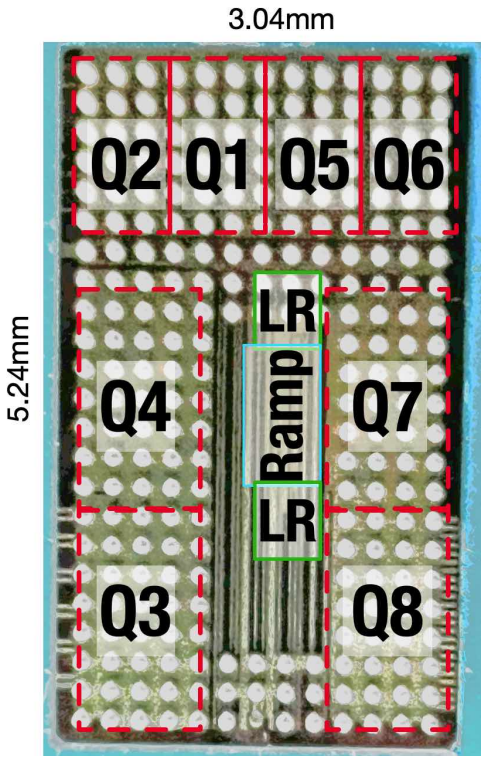


Figure 6.7. Die photo of high-power ITSAB converter

are selected based on their derated value after considering bias voltages so that $C1$ and $C3$ are matched in value, and $C2$ is much larger than the other two capacitors. The inductors are selected because of small ESR so that the conduction loss is minimized for heavy load capability.

The chip die is designed in TSMC 130 nm BCD technology with a dimension of 3.04 mm $\times$ 5.24 mm. The placement of power switches are labeled in the die photo (Fig. 6.7). Their positions are referred to the connections shown in the 3D floorplan in Fig. 6.1 for shortest path. The other function blocks are in the middle of the chip die, such as Linear Regulators (LR) and Ramp Generator (RG).

The major waveforms, such as the switching nodes V_{SW1}, V_{SW2}, V_{X2} and LR output V_{DD5}, are measured at $f_s = 1.8\,\text{MHz}$, $V_{in} = 9.6\,\text{V}$ and $V_o = 2.3\,\text{V}$ with Coilcraft 1512SP as inductors. They are displayed in Fig. 6.8. It can be summarized that V_{DD5} is well regulated at $V_{DD} + V_o = 6.2V$. What's more, from the rising edge of V_{SW1}, there's almost no overshoot or ringing can be noticed, meaning the deadtime is set precisely and thus complete soft-switching

Table 6.3. Components on the demonstration PCB

Component	Part No.	Details
C1	GRM155C81C225ME15D	4 x 2.2 µF, 16 V 0402 (1.83 µF)
C2	CL05A106MP8NUB8	4 x 10 µF, 10 V 0402 (8 µF)
C3	CL03A225MQ3CRNC	2 x 2.2 µF, 6.3 V 0201 (1.73 µF)
Cin(V_{in})	GRM21BR61E106MA73L	6 x 10 µF, 25 V 0805 (10.5 µF)
Cin(V_{DD})	CL05A106MP8NUB8	1 x 10 µF, 10 V 0402 (2 µF)
Co	CL03A475MQ5C65	4 x 4.7 µF, 6.3 V 0201 (4.1 µF)
Decap(V_{DDH6})	GRM155C81C225ME15D	3 x 2.2 µF, 16 V 0402 (1.24 µF)
Decap(V_{DD5})	GRM155C81C225ME15D	2 x 2.2 µF, 16 V 0201 (1.23 µF)
Decap(V_{SS8})	GRM155C81C225ME15D	2 x 2.2 µF, 16 V 0201 (1.04 µF)
Decap(V_{SSL7})	GRM155C81C225ME15D	1 x 1 µF, 16 V 0201 (0.9 µF)
L1,3	Coilcraft 1512SP	10 nH, 2.5 mΩ ESR

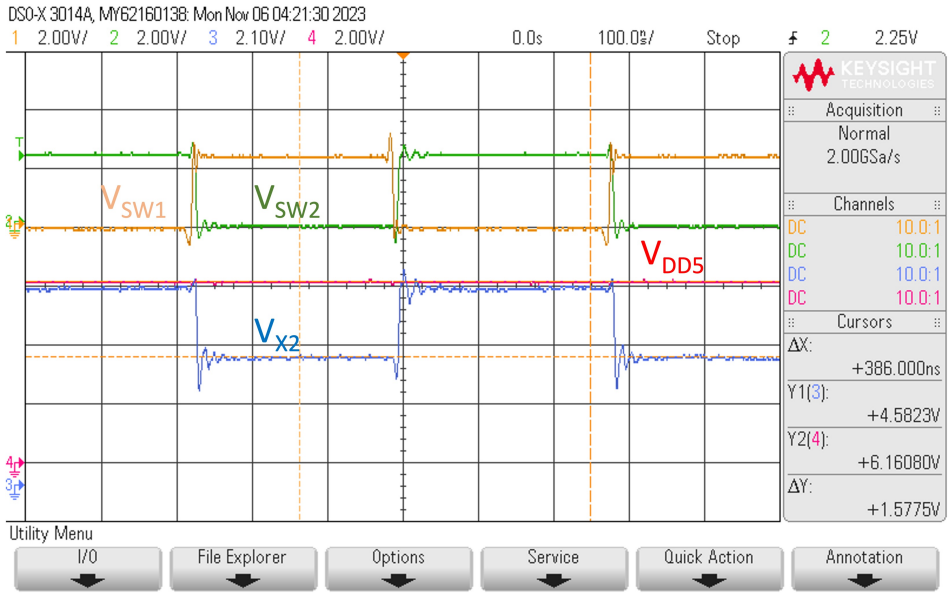
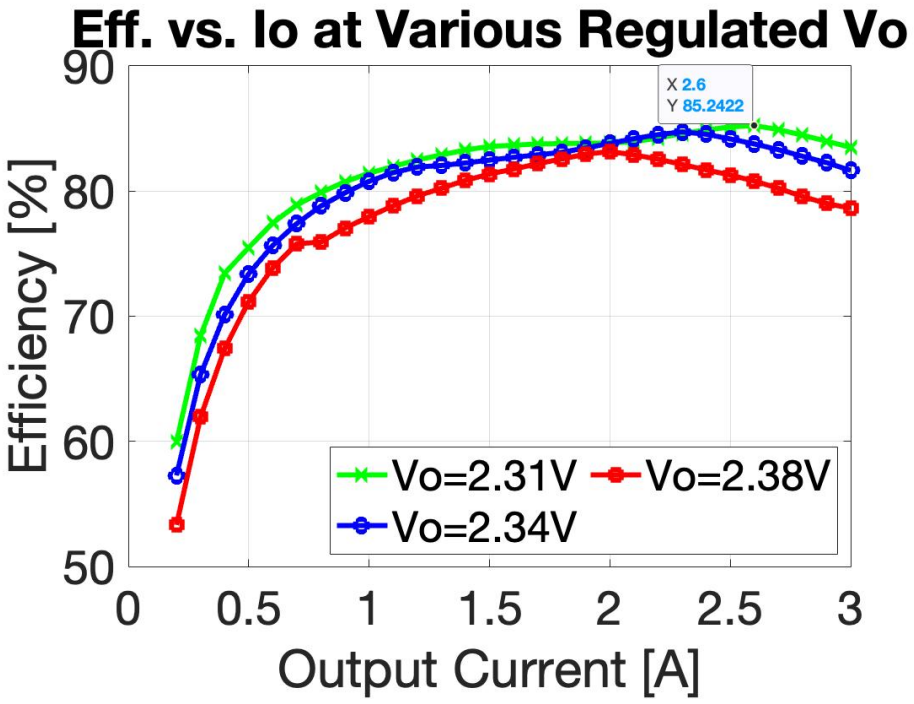


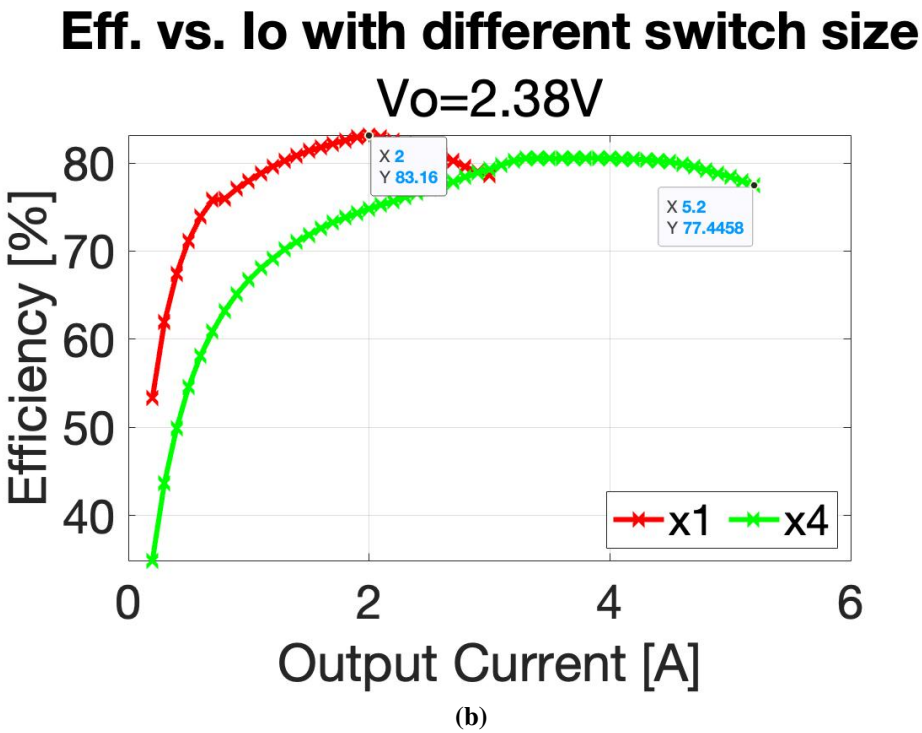
Figure 6.8. Measured switching nodes voltages

is achieved.

The efficiency curves are plotted in Fig. 6.9(a) at various regulated V_o. The peak efficiency



(a)



(b)

Figure 6.9. (a) Efficiency with different output voltages at 1.8 MHz; (b) efficiency with (x1) and without (x4) switch partitioning at 2.38 V output voltage

of 85.24 % is captured at 9.6 V/2.31 V, 1.8 MHz switching frequency, 2.6 A load condition. The switch partitioning benefit can be verified in Fig. 6.9(b) at the same input voltage and switching frequency with 2.38 V output voltage. By turning on switch partitioning, the efficiency at 2 A load is increased from 75 % to 83.16 %. The recorded peak output current is 5.2 A, twice of the value in the other ITSAB converter in Chapter. 5.

6.4 Summary

In this chapter, the application of ITSAB converter is extended to high output power. By co-design the chip die and the prototype PCB, the converter is now capable of 5.2 A load in a compact 3D package. To achieve high efficiency at both heavy and light load, a switch partitioning mechanism is implemented such that only one quarter of the entire power switches are turned on at light load condition. Another fine-tuned deadtime generator is also added for minimized body diode conduction and fine-tuned timing of complete soft-switching. The chip die is fabricated in TSMC 130 nm BCD technology with a dimension of 3.04 mm $\times$ 5.24 mm and is mounted with two 10 nH inductors supplied by Coilcraft on two sides of the demonstration PCB. The captured peak efficiency is 85.24 % when operating the converter at 9.6 V/2.31 V, 1.8 MHz switching frequency, 2.6 A load. The recorded peak output current is 5.2 A.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

In this dissertation, it has discussed the increasingly demanding of high power but compact power delivery system for high performance computing systems. From the case study of some commercial products, it can be summarized that the magnetic devices, namely inductors and transformers, are the major obstacle of this trend. By analyzing several existing solutions, the issue can hardly be solved as none of these solutions achieves 10s nH inductance, fine regulation and high efficiency at the same time.

While the existing solutions are not satisfying, three works have been proposed from the perspective of circuit operation innovation, special circuit technique and novel circuit topology. The first one is a dual-inductor hybrid converter operated in multi-phases. Different from the conventional dual-phase operation for this dickson-star switched-capacitor converter derived hybrid converter, the proposed one can potentially reduce the output inductor by 3x and thus the overall volume of the converter is shrunk.

The second introduced method is zero-voltage-switching assisted by an auxiliary circuit. Detailed operation and optimization are presented in Chapter. 4. The demonstrated ZVS-3LB converter has shown great advantage at light load operation where normally the switching loss dominates. With the help of ZVS operation, the switching frequency can be boosted so that the inductor size will be reduced.

Further more, in the last work, a novel ITSAB converter is proposed. There are two demonstration prototype of this type of converter. The first chip is optimized, designed and fabricated in 1.7 mm $\times$ 1.9 mm area of a 130 nm BCD process. The active die is flip-chipped on a 6.5 mm $\times$ 6.5 mm package substrate together with power capacitors and two 10 nH IPD inductors for demonstration. The other chip, which targets higher output power, is fabricated in the same process but has considered more of 3D packaging during PCB prototyping. All of these attempts have demonstrated 10 nH inductors can be used on power converters that operate below 5 MHz switching frequency, while achieving high power density and heavy load capability.

In addition to the works presented in this dissertation, some other works can be done to enrich the proposed solutions.

7.2 Future Work

7.2.1 Bi-directional Operation

The ITSAB converter is derived from a Dual Active Bridge (DAB) converter, who has a feature of bi-directional operation as illustrated in Fig. 7.1. Basically, by swapping the leading phase and trailing phase of A and B, the current flows in different directions. The same concept can be applied to ITSAB converter. By moving the control signals of $Q3$ and $Q4$ from trailing phase to leading phase, the current could flow from lower voltage to higher voltage. Of course, to enable this operation, the power switches must be able to block both directions of voltage and current and the related gate drive signals should also be re-designed. Despite of the implementation difficulty, the bi-directional converter could potentially be found useful in applications of robot, EV, where a battery is used and recycling energy to charge battery is promising.

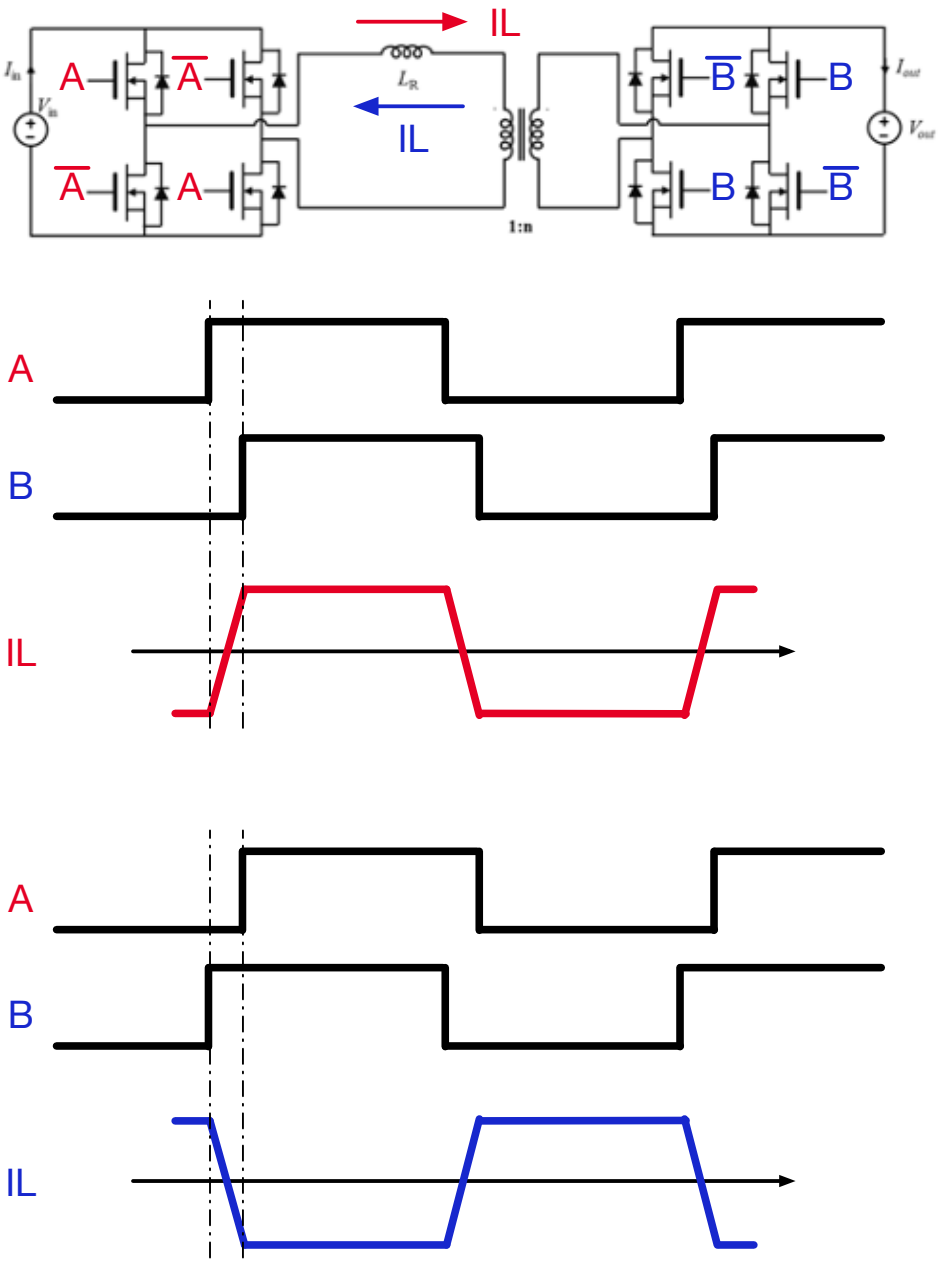


Figure 7.1. Bi-directional operation of DAB converter

7.2.2 Constant Current (CC) Mode for Battery charger

The regulation of ITSAB converter is different from the most step-down converter which is based on the modulation of the pulse width of control signals. As introduced in Chapter. 5, ITSAB converter regulates its output voltage by modulating the phase shift ϕ, as illustrated in Fig. 7.2. In fact, the converter doesn't directly modulate the output voltage but instead regulating its output current in response to different reference voltages.

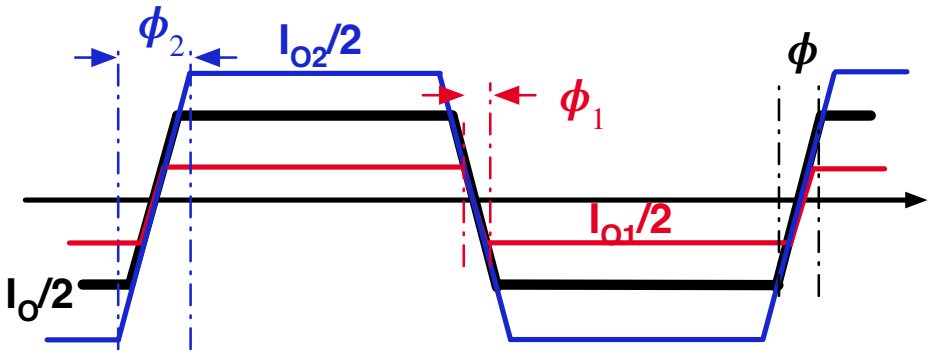


Figure 7.2. Modulation of inductor current in ITSAB converter

How about directly feeding back the output current and modulating the phase shift time in response to that current? This is absolutely applicable, but the range of resulted output voltage needs some more analysis. This CC mode can be used on a battery charger. As commonly known, the charging of a battery must go through CC mode when the energy level is low and enter constant-voltage (CV) mode when it's charged to a certain power level. ITSAB converter, because of its special control method, would be a potential candidate for this application.

Appendix A

FPGA Embedded System Design for ZVS-3LB Converter

In the ZVS-3LB converter design, the embedded system on FPGA as shown in Fig. 4.7 is designed based on NiosII system. The blocks added and the connection between them are captured in Fig. A.1. The system core is Nios II Processor, while its supporting system clock is generated from a PLL IP. On-chip memory is to stored the data received from the master PC. PWM generators are the blocks to output gate control signals for each power switch and its source code is attached in the following pages. Another important block is MATLAB AXI bus IP for communicating between the master PC, where a MATLAB software is used to sweep parameters, and the slave FPGA which is built on Nios II processor. By programming to the specific address of each PWM generator through the MATLAB AXI bus, each PWM signal would have its duty ratio and phase completely controlled by the master PC, so that the automation testing can be launched.

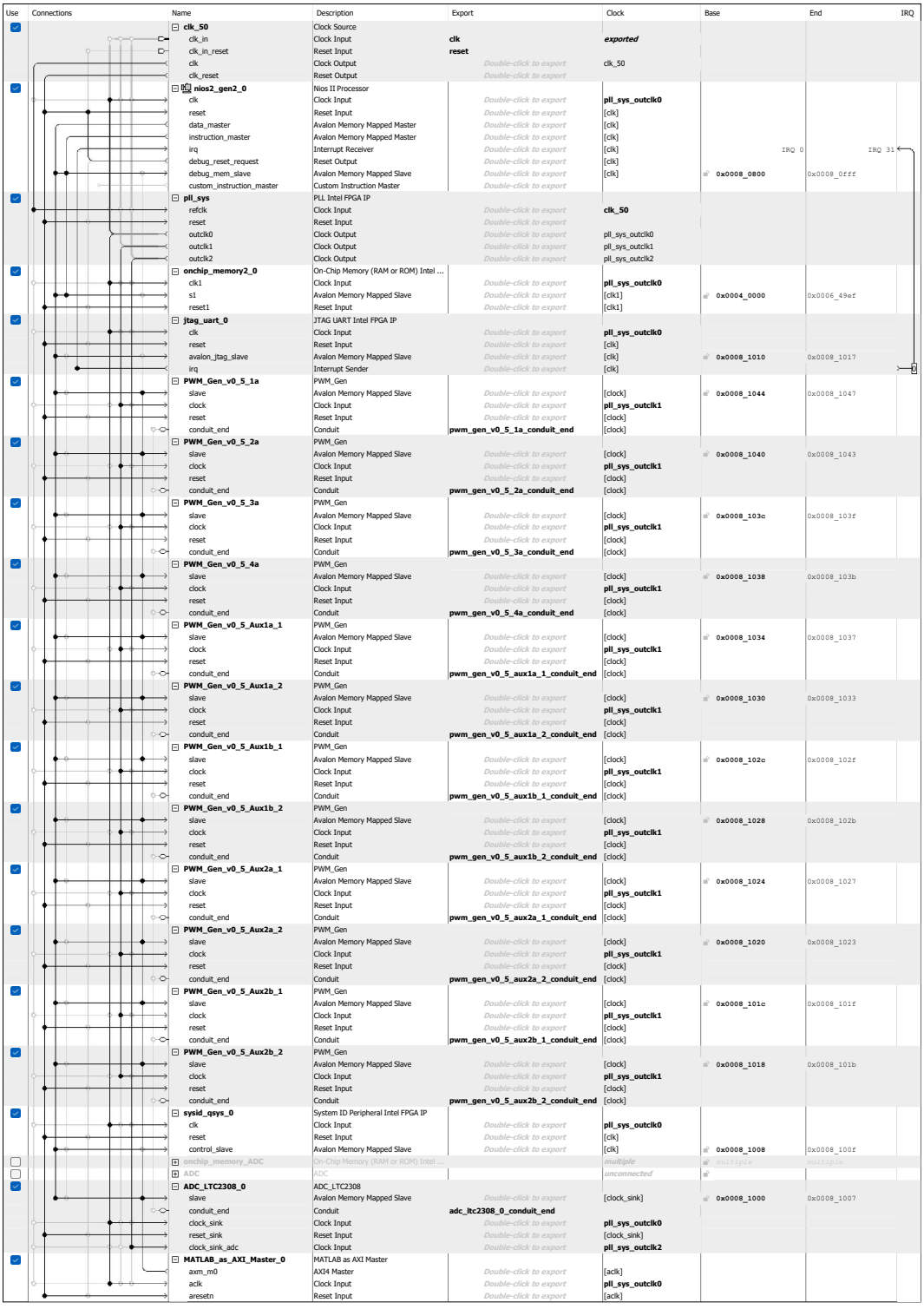


Figure A.1. Embedded system design of the ZVS-3LB controller based on NiosII system

One of the key blocks is the PWM signal generator as the verilog source code shown below. This block can read the data memory in the NiosII core. Therefore, by sending data from a PC to the FPGA, the PWM generator block can fetch the required duty ratio and phase information and thus generates the desired PWM control signals. The verilog source code for the up counter is also listed following the PWM generator block.

PWM Generator

```
module PWM_Gen_v0_5(
    input          clk,
    input          reset_n,
    input          slave_chip_select_n,
    input          slave_read,
    output  reg [31:0]  slave_readdata,
    input          slave_write,
    input   [31:0]  slave_writedata,
    input sync,
    input [15:0] period_minus2,
    output reg pwm_out,
    output reg S_reg
);
wire [15:0] counter_out;
////////////////
// avalon slave
reg R_reg;
reg [15:0] duty;
reg [15:0] phase;
reg writedone;
always @(posedge clk or negedge reset_n)
begin
  if (~reset_n)
  begin
    duty <= 16'b0;
```

```
26      phase <= 16'b0;
27      writedone <= 1'b0;
28    end
29    else if (~slave_chip_select_n & slave_read)
30      slave_readdata <= {16'hffff, 16'h0};
31    else if (~slave_chip_select_n & slave_write)
32    begin
33    //load in duty and phase setup of the PWM signal
34      duty <= slave_writedata[15:0];
35      phase <= slave_writedata[31:16];
36      writedone <= 1'b1;
37    end
38    else writedone <= 1'b0;
39  end
40
41  always @(posedge clk or negedge reset_n) begin
42  if (~reset_n) begin
43    R_reg <= 1'b0;
44    end
45    //when counter counts to duty number, trigger falling edge of PWM
46    else if(counter_out == duty) begin
47    R_reg <= 1'b1;
48    end
49    else begin
50    R_reg <= 1'b0;
51    end
52  end
53  always @(posedge clk or negedge reset_n) begin
54  if (~reset_n) begin
55    S_reg <= 1'b0;
56    end
57    //when counter counts to 0, initiate PWM rising edge
```

```
58    else if(counter_out == 16'b0) begin
59    S_reg <= 1'b1;
60    end
61    else begin
62    S_reg <= 1'b0;
63    end
64  end
65  Cnt_Up16_1 Cnt16_inst(
66    .clk(clk),        //Counter clock
67    .period_minus2(period_minus2),
68    .counter_out(counter_out),         // 8 bit output from the counter
69    .load(~sync),       //command of loading phase
70    //load in starting counter number, which is phase shift
71    .phase_loadin(phase)
72  );
73  SR_latch_gate SR_latch_inst(
74    .R(R_reg),
75    .S(S_reg),
76    .Q(pwm_out)
77  );
78  endmodule
```

Up Counter

```
`timescale 1ps / 1ps
module Cnt_Up16_1 (
  clk,        //Counter clock
  period_minus2,
  counter_out,         // 8 bit output from the counter
  phase_loadin,
  load        //command of loading phase
);

  input clk;      // clock declared as an input port
  input [15:0] period_minus2;
  input load;
  output reg [15:0] counter_out;  // counter_out declared as an 8 bit
   output register
  input [15:0] phase_loadin;

  always @(posedge clk)
    begin
    if (~load) begin
      counter_out <= (phase_loadin+1);
      end
    else begin
      if (counter_out > (period_minus2) ) begin//FFE=-2//period-2
      counter_out <= 0;
      end
      else begin
      counter_out <= counter_out + 1'b1;
      end
    end
    end
endmodule       // identifies the end of the module
```

Appendix B

Automatic Parameter Sweeping Source Code in Matlab for ZVS-3LB Converter

```
clc
clear all
close all
%% create a seperate folder to store mat, data and screenshot
datename=date;
mkdir(datename);
%% parameters to include in the file name
L=['IHLP-5050_'];
Cfly=['10_1_0p1uF_'];
Laux=['IHLP-1616BZ_'];
%% Instrument Connection
% Find a VISA-USB object.
rigol_load = instrfind('Type', 'visa-usb', 'RsrcName', 'USB0::0x1AB1::0
    x0E11::DL3A201300268::0::INSTR', 'Tag', '');
% Create the VISA-USB object if it does not exist
% otherwise use the object that was found.
if isempty(rigol_load)
     rigol_load = visa('NI', 'USB0::0x1AB1::0x0E11::DL3A201300268::0::
    INSTR');
else
```

```
    fclose(rigol_load);
    rigol_load = rigol_load(1);
end
%
% Find a VISA-USB object.
ks_ps = instrfind('Type', 'visa-usb', 'RsrcName', 'USB0::0x2A8D::0x0102
    ::MY56003339::0::INSTR', 'Tag', '');

% Create the VISA-USB object if it does not exist
% otherwise use the object that was found.
if isempty(ks_ps)
    ks_ps = visa('NI', 'USB0::0x2A8D::0x0102::MY56003339::0::INSTR');
else
    fclose(ks_ps);
    ks_ps = ks_ps(1);
end
% Find a VISA-USB object.
RIGOL_PS = instrfind('Type', 'visa-usb', 'RsrcName', 'USB0::0x1AB1::0
    x0E11::DP8B213700918::0::INSTR', 'Tag', '');
% Create the VISA-USB object if it does not exist
% otherwise use the object that was found.
if isempty(RIGOL_PS)
    RIGOL_PS = visa('NI', 'USB0::0x1AB1::0x0E11::DP8B213700918::0::INSTR
    ');
else
    fclose(RIGOL_PS);
    RIGOL_PS = RIGOL_PS(1);
end
%% input parameters
fsw=1e6;%switching frequency
fclk=200e6;%Embedded system clk
period=fclk/fsw;
```

```
vref=3.75;%target output voltage
vg=15;%input voltage
vdri=12;%gate driving voltage
idri=0.5;%gate driving supply current setup
duty0=round(vref*period/vg);
QF_QbarR=4;
ddmax=12;
ddmin=5;
dd0=round(mean([ddmax ddmin]));
cd0=-3;
duty=duty0+cd0;%duty ratio
duty10=duty+dd0;%duty ratio for phase 1
duty30=duty-dd0;%duty ratio for phase 2
duty_Aux10=1;%duty ratio of Auxa
duty_Aux30=1;%duty ratio of Auxb
QbarF_AuxR10=2;
QbarF_AuxR30=QbarF_AuxR10;
AuxF_QR10=3;
AuxF_QR30=3;
Auxa_ext10=5;
Auxa_ext30=5;
%% initialize pwm
fun_PWM_setting(period, duty10, duty30, QF_QbarR,duty_Aux10, duty_Aux30,
    QbarF_AuxR10, QbarF_AuxR30, AuxF_QR10, AuxF_QR30, Auxa_ext10,
   Auxa_ext30);
%% file name
file=['ZVS_3LB_', L, Laux, Cfly, datename];
%% instruments parameters
ival = [0.5 0.8 1 1.2 1.5 1.8 2 3 4];
pts=length(ival);
i=1; %init array pointer
k=1;
```

```
78 ramp_down = 0; %ramp down flag. If set, then ramp down. If cleared, ramp
       up.
79 delay = 1; %time delay between current steps while ramping
80 %pre-form various measurement/calc arrays
81 vbus_meas = zeros(1,pts);
82 ibus_meas = zeros(1,pts);
83 vo_meas = zeros(1,pts);
84 io_meas = zeros(1,pts);
85 pout_meas = zeros(1,pts);
86 pin_meas = zeros(1,pts);
87 eff_per = zeros(1,pts);
88 %% initialize test
89 %connect to instrument objects
90 fopen(rigol_load);
91 fopen(ks_ps);
92 fopen(RIGOL_PS);
93 %communicating with instrument objects
94 %driver supply
95 fprintf(RIGOL_PS, ':INST CH1');
96 fprintf(RIGOL_PS, ':CURR 0.5');
97 fprintf(RIGOL_PS, ':CURR:PROT 1');
98 fprintf(RIGOL_PS, ':CURR:PROT:STAT ON');
99 fprintf(RIGOL_PS, ':VOLT 12');
100 fprintf(RIGOL_PS, ':OUTP CH1,ON');
101 pause(delay);
102 %load
103 fwrite(rigol_load,'SOUR:SENS 1'); %enable voltage sense inputs
104 scpi_str = ['SOUR:CURR:LEV:IMM ' num2str(ival(1,i))];
105 fwrite(rigol_load,scpi_str); %set initial current value to imin
106 fwrite(rigol_load,'SOUR:INP:STAT 1');
107 pause(delay);
108 %turn on power supply
```

```
fwrite(ks_ps, ['VOLT ', num2str(vg),', (@2)']);
fwrite(ks_ps,'OUTP ON, (@2)');
%create spreadsheet for data
for Iout=ival
Row1=["Num" "duty1" "duty3" "duty_Aux1" "duty_Aux3" "QbarF_AuxR1" "
    QbarF_AuxR3" "AuxF_QR1" ...
            "AuxF_QR3" "Auxa_ext1" "Auxa_ext3" "QF_QbarR" "Vg" "Vout"
    ...
            "Iout" "Eff"];
writematrix(Row1, ['./', datename, '/', [file, '_', num2str(Iout), 'A'],
     '.xls'], 'Sheet',1,'Range', 'A1:P1');
end
disp('Ramping up current and measuring efficiency');
while ramp_down==0
%% set pwm
for duty1=[duty10 duty10+1 duty10+2 duty10+3]
    for duty3=[duty1-ddmax:1:duty1-ddmin]
        duty=duty0+cd;
        for duty_Aux3=[duty_Aux30]
            for duty_Aux1=[duty_Aux10 duty_Aux10+1]
                for QbarF_AuxR1=[QbarF_AuxR10 QbarF_AuxR10+1]
                    for QbarF_AuxR3=[QbarF_AuxR1]
                    for AuxF_QR3=[AuxF_QR30 AuxF_QR30+1 AuxF_QR30+2]
                        for AuxF_QR1=[AuxF_QR3+2 AuxF_QR3+3 AuxF_QR3+4]
                            for Auxa_ext3=[duty_Aux3*5 duty_Aux3*6]
                                Auxa_ext1=Auxa_ext3;
                                fun_PWM_setting(period, duty1, duty3,
    QF_QbarR, ...
                                    duty_Aux1, duty_Aux3, QbarF_AuxR1,
    QbarF_AuxR3, AuxF_QR1, AuxF_QR3, ...
                                    Auxa_ext1, Auxa_ext3);
        %display current parametes
```

```
136         disp(['duty1=',num2str(duty1),', duty3=',num2str(duty3),',
    duty_Aux1=',num2str(duty_Aux1), ...
137             ', duty_Aux3=',num2str(duty_Aux3),', QbarF_AuxR1=',num2str(
    QbarF_AuxR1),', QbarF_AuxR3=',num2str(QbarF_AuxR3), ...
138             ', AuxF_QR1=',num2str(AuxF_QR1),', AuxF_QR3=',num2str(
    AuxF_QR3),', Auxa_ext1=',num2str(Auxa_ext1), ...
139             ', Auxa_ext3=',num2str(Auxa_ext3)]);
140         %turn on load here
141         scpi_str = ['SOUR:CURR:LEV:IMM ' num2str(ival(1,i))];
142         fwrite(rigol_load,scpi_str); %increment current
143         fwrite(rigol_load,'SOUR:INP:STAT 1');
144         pause(delay);
145         vbus_meas(i) = str2num(query(ks_ps,'meas:volt:dc? (@2)')); %
    measure vbus voltage w/ tek_dmm
146         ibus_meas(i) = str2num(query(ks_ps, 'meas:curr:dc? (@2)')); %
    measure ibus current w/ ks_ps
147         vo_meas(i) = str2num(query(rigol_load, 'meas:volt:dc?'));
148         io_meas(i) = str2num(query(rigol_load, 'meas:curr:dc?'));
149         pout_meas(i) = vo_meas(i)*io_meas(i);
150         pin_meas(i) = vbus_meas(i)*ibus_meas(i);
151         eff_per_new = (pout_meas(i)/pin_meas(i))*100;
152         M=[k duty1 duty3 duty_Aux1 duty_Aux3 QbarF_AuxR1 QbarF_AuxR3
    AuxF_QR1 ...
153             AuxF_QR3 Auxa_ext1 Auxa_ext3 QF_QbarR vbus_meas(i) vo_meas(i
    ) ...
154             io_meas(i) eff_per_new];
155         writematrix(M, ['./', datename, '/', [file, '_', num2str(ival(1,
    i)), 'A'], '.xls'], 'Sheet',1,'Range', ['A',num2str(k+1),':P',num2str
    (k+1)]);
156         k=k+1;
157         disp(['Vout=',num2str(vo_meas(i)),', Iout=',num2str(io_meas(i)),
    ', Efficiency=',num2str(eff_per_new)]);
```

```
        if(abs(vo_meas(i)-vref)<0.1)%only keep the data with Vo=vref
            if(eff_per(i)<eff_per_new) %save the max eff data points
                opt.eff_per(i)=eff_per_new;
                opt.vo(i)=vo_meas(i);
                %
                opt.duty1(i)=duty1;
                opt.duty3(i)=duty3;
                opt.duty_Aux1(i)=duty_Aux1;
                opt.duty_Aux3(i)=duty_Aux3;
                opt.QbarF_AuxR1(i)=QbarF_AuxR1;
                opt.QbarF_AuxR3(i)=QbarF_AuxR3;
                opt.AuxF_QR1(i)=AuxF_QR1;
                opt.AuxF_QR3(i)=AuxF_QR3;
                opt.Auxa_ext1(i)=Auxa_ext1;
                opt.Auxa_ext3(i)=Auxa_ext3;
            end
        end


                                    end
                                end
                            end
                        end
                    end
                end
            end
        end
    end
end
%update starting point for next load current
        dd0=0.5*(opt.duty1(i)-opt.duty3(i));
        cd0=0.5*(opt.duty1(i)+opt.duty3(i))-duty0;
        duty_Aux10=opt.duty_Aux1(i);
```

```
190         duty_Aux30=opt.duty_Aux3(i);
191         QbarF_AuxR10=opt.QbarF_AuxR1(i);
192         QbarF_AuxR30=opt.QbarF_AuxR3(i);
193         AuxF_QR10=opt.AuxF_QR1(i);
194         AuxF_QR30=opt.AuxF_QR3(i);
195         Auxa_ext10=opt.Auxa_ext1(i);
196         Auxa_ext30=opt.Auxa_ext3(i);
197
198         i=i+1;%load current to next value
199         k=1;
200         if(i>pts)
201             ramp_down = 1;
202             i=pts;
203         end
204 end
205
206 disp('Ramping down current.');
207 while ramp_down==1 %check if in ramp down mode
208     if i<1 %if in ramp down mode and at the imin value, clear ramp down
    flag
209         ramp_down = 0;
210         i=1; %initialize i pointer to first position in ival array to
    prep for current ramp up
211         hold off; %turn off plot hold so plot is wiped on next current
    ramp up sweep
212     else %otherwise continue to decrement the current value
213         scpi_str = ['SOUR:CURR:LEV:IMM ' num2str(ival(1,i))];
214         fwrite(rigol_load,scpi_str); %decrement current
215         pause(delay);
216          i = i - 1; %decrement to next pointer value in ival array
217     end
218 end
```

```
fwrite(ks_ps, 'OUTP OFF, (@2)');
fclose(ks_ps);
delete(ks_ps);
clear ks_ps;

fwrite(rigol_load, 'SOUR:CURR:LEV:IMM 0');
fwrite(rigol_load,'SOUR:INP:STAT 0');
fwrite(rigol_load,'SOUR:SENS 1'); %keep sense input enabled voltage
    sense inputs
fclose(rigol_load);
delete(rigol_load);
clear rigol_load;

fprintf(RIGOL_PS, ':OUTP CH1,OFF');
fclose(RIGOL_PS);
delete(RIGOL_PS);
clear RIGOL_PS;
%% save workspace
mat_name=['./', datename,'/', file, '.mat'];
save(mat_name);
%
disp('Efficiency sweep complete');
```

Appendix C

ITSAB Converter Optimization Source Code in Matlab

```
%% topology independent constants
clear
L0=10e-9;
f0=100e6;
AL0=0.7;
Kc=1.4e-6;%F/mm2
Iout=1;
Vin=12;
Vout=Vin/4;

%% power switches parameters
%process related, critical numbers are hided for confidential reason
Ron=1e-3*1.5;%on resistance unit
Vg=3.6;%gate drive voltage
%NMOS, for Q1~6
AsN=x;%Ron density mohm*mm2
CggN_den=x;%Cgg of NMOS density per mm2
CddN_den=x;%Cdd of NMOS density per mm2
CssN_den=x;%Css of NMOS density per mm2
%Total parasitic caps used in loss analysis
```

```
CdsN_den=CddN_den+CssN_den;
CggN_AsN=CggN_den*AsN;
CdsN_AsN=CdsN_den*AsN;
%PMOS, for Q7,8
AsP=x;
CggP_den=x;%Cgg of PMOS density per mm2
CddP_den=x;%Cdd of PMOS density per mm2
CssP_den=x;%Css of PMOS density per mm2
%Total parasitic caps used in loss analysis
CdsP_den=CddP_den+CssP_den;
CggP_AsP=CggP_den*AsP;
CdsP_AsP=CdsP_den*AsP;
%x1:Q1-Q2: 5V NMOS
%x2:Q3,Q4: 5V NMOS
%x3:Q5,Q6:5V NMOS
%x4:Q7,Q8:5V PMOS
%% Total capacitor area as one constrain
ACmax=10/3;
%% Total switch area as one constrain
Asmax=10;
%% CVX tool starts optimizing
cvx_clear
cvx_solver mosek
for i1=1:length(Asmax)
        for i2=1:length(ACmax)
            cvx_begin gp quiet
            variables x1 x2 x3 x4 Ro fs
            alpha=1.1;
            %inductor RL model
            RL=(32+382*(fs/f0)^3.78);%mohm
            %loop resistance
            Rs=(Ron/x3+Ron/x1+Ron/x2)*1e3+RL;%mohm
```

```
            %k vs. Q, from minimum RMS current evaluation
            kopt=25.22*Ro^-1.14*(Rs)^(1.14-0.51)+1.44;
            L1=kopt*Ro*1e-3/2/pi/fs;
            C1=kopt/(Ro*1e-3*2*pi*fs);
            L2=L1;
            C2=C1;
            C3=2*C1;
            %conduction loss
            Pcond=(Ron/x1+Ron/x3+Ron/x4)*(alpha*0.5*Iout)^2+...
                Ron/x2*(alpha*Iout)^2;%W
            %gate switching loss
            Pgate=Vg^2*fs*2*(CggN_AsN*x1+CggN_AsN*x2+CggN_AsN*x3+
    CggP_AsP*x4)*2;%W
            %Cds charging/discharging loss
            Psw=0.5*(Vout)^2*fs*(CdsN_AsN*x1*2+CdsN_AsN*x3+CdsP_AsP*x4);
            %inductor loss
            PL=(alpha*Iout*0.5)^2*(RL)*1e-3*2;%W
            %capacitors and switch area constrain
            AC=(C1+C2+C3)/Kc;
            As=2*(x1*AsN+x2*AsN+x3*AsN+x4*AsP);
            Q=Ro/Rs;
            minimize(Pcond+Psw+PL+Pgate)
            subject to
                AC <= ACmax(i2);
                As <= Asmax(i1);
                L1 <= 5e-9*2;
                1/Q <=1;
            cvx_end
%% the rest is for printing results
            fprintf( 'loss = %3.2f\n', cvx_optval );
            fprintf( 'fs = %3.2f kHz\n', fs/1e3 );
            fprintf( 'Q= %3.2f\n', Ro/Rs);
```

```
            fprintf( 'kopt= %3.2f\n', kopt );
            fprintf( 'L= %3.2f nH\n', L1*1e9);
            fprintf( 'C= %3.2f uF\n', C1*1e6);
            fprintf( 'As= %3.2f\n', As );
            fprintf( 'Rs= %3.2f mohm\n', Rs );
            min_loss(i2)=cvx_optval;
            Pcond_opt(i2)=Pcond;
            Psw_opt(i2)=Psw;
            PL_opt(i2)=PL;
            As_opt(i2)=As;
            Q_opt(i2)=Ro/Rs;
            k_opt(i2)=kopt;
            C1_opt(i2)=C1;
            fs_opt(i2)=fs;
            Pgate_opt(i2)=Pgate;
            Rs_opt(i2)=Rs;
            As1_opt(i2)=AsN*x1;
            As2_opt(i2)=AsN*x2;
            As3_opt(i2)=AsN*x3;
            As4_opt(i2)=AsP*x4;
        end
end
figure
plot(C1_opt*1e6, min_loss,'LineWidth',2)
ax=gca;
set(ax,'FontSize',20)
xlabel('C_1 [\mu F]')
ylabel('Loss [W]')
grid on

figure
plot(C1_opt*1e6, fs_opt/1e6,'LineWidth',2)
```

```
ax=gca;
set(ax,'FontSize',20)
xlabel('C_1 [\mu F]')
ylabel('Switching Frequency [MHz]')
grid on

figure
plot(C1_opt*1e6, As_opt,'LineWidth',2)
ax=gca;
set(ax,'FontSize',20)
xlabel('C_1 [\mu F]')
ylabel('Switch size [mm^2]')
grid on

figure
plot(C1_opt*1e6, k_opt,'LineWidth',2)
ax=gca;
set(ax,'FontSize',20)
xlabel('C_1 [\mu F]')
ylabel('Optimal k=f_s/f_r')
grid on

figure
plot(C1_opt*1e6, Q_opt,'LineWidth',2)
ax=gca;
set(ax,'FontSize',20)
xlabel('C_1 [\mu F]')
ylabel('Optimal Q=R_o/R_s')
grid on

Io_vec=logspace(log10(0.5),log10(3),20);
Pcond=(Ron/x1+Ron/x3+Ron/x4)*(alpha*0.5*Io_vec).^2+...
```

```
Ron/x2*(alpha*Io_vec).^2;%W
Pgate=Vg^2*fs*2*(CggN_AsN*x1+CggN_AsN*x2+CggN_AsN*x3+CggP_AsP*x4)*2;%W
Psw=0.5*(Vout)^2*fs*(CdsN_AsN*x1*2+CdsN_AsN*x3+CdsP_AsP*x4);
PL=(alpha*Io_vec*0.5).^2*(RL)*1e-3*2;%W
figure
Ptot=Pcond+Pgate+Psw+PL;
hold on
plot(Io_vec,Vout*Io_vec./(Vout*Io_vec+Ptot)*100,...
    'LineWidth',2)
ylim([90 97])
max(Vout*Io_vec./(Vout*Io_vec+Ptot))*100
xlabel('output current')
ylabel('Efficiency [%]')
set(gca,'FontSize',12)
grid on

figure
p=pie([Pcond_opt Psw_opt Pgate_opt PL_opt]./min_loss)
pText = findobj(p,'Type','text');
percentValues = get(pText,'String');
txt = {'Pcond: ';'Psw: ';'Pgate: ';'Pind:'};
combinedtxt = strcat(txt,percentValues);
pText(1).String = combinedtxt(1);
pText(2).String = combinedtxt(2);
pText(3).String = combinedtxt(3);
pText(4).String = combinedtxt(4);
set(gca,'FontSize',30)
title('Loss breadown at 1.5A')
```

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