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Energy-Efficient Intra-Data Center Coherent Links with High Link Budget

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Doctor of Philosophy
in
Electrical and Computer Engineering

by

Aaron Maharry

Committee in charge:

Professor Clint Schow, Chair
Professor James Buckwalter
Professor Larry Coldren
Professor Adel Saleh

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The Dissertation of Aaron Maharry is approved.

Professor James Buckwalter

Professor Larry Coldren

Professor Adel Saleh

Professor Clint Schow, Committee Chair

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For my family

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Curriculum Vitæ

Aaron Maharry

Education

2023	Ph.D. in Electrical and Computer Engineering (Expected), University of California, Santa Barbara.
2019	M.S. in Electrical and Computer Engineering, University of California, Santa Barbara.
2017	B.S. in Electrical and Computer Engineering, Ohio State University.

Publications

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Abstract

Energy-Efficient Intra-Data Center Coherent Links with High Link Budget

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As demand for internet applications, cloud computation, and AI continue to grow, data center networks must scale to support increased traffic flow. While current intensity modulation links are an economical solution today, coherent links are an increasingly attractive option to improve performance. Conventional coherent link technologies that are used today in >40 km transmission are based on power-hungry and expensive digital signal processing, and cannot be easily scaled to the high volumes required for data centers. Coherent links must be optimized for low power consumption and cost for reaches <2 km to make them viable for intra-data center networks. The enlarged link loss budgets from such links will also enable optical switching networks, which can dynamically reconfigure the network for improved server utilization, leading to vast improvements in overall data center energy efficiency.

The focus of this work is to develop energy-efficient coherent links with large link budgets for intra-data center networks. Design methodologies and architectural trade-offs for short-reach coherent link optimization will be presented. Using these techniques, custom electronic and photonic integrated circuits for coherent transmitters and receivers were designed, fabricated, assembled, and characterized. The first-ever full coherent link operating in the O-band was demonstrated with 56 Gbaud QPSK transmission. An O-band coherent link with custom packaged integrated circuits for both the transmitter and receiver was also demonstrated with 224 Gbps DP-QPSK transmission below the HD-FEC threshold with <10 pJ/bit power consumption expected for circuits including

integrated optical gain. These results shows that optimized O-band coherent links can support high data rates and link budgets with attractive energy efficiency for future intra-data center networks.

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Chapter 1

Introduction

1.1 Background and Motivation

Perhaps the defining feature of the times we live in is the impact of the computing and communications revolutions of recent decades. The astoundingly rapid development of these technologies has profoundly changed how people live their lives, and will continue to do so in times to come. A large part of the global computing infrastructure is concentrated in data centers, which house compute servers and associated infrastructure at massive scale. These data centers support the internet cloud infrastructure, and increasingly host dedicated hardware for artificial intelligence and machine learning (AI/ML) computation. Data center electricity consumption accounts for 2% of total US consumption, and new installations are continually deployed and upgraded to meet rising computation and communications demands, so efficiently scaling data center hardware is of paramount importance.

The intra-data center communications network has evolved over the years from copper interconnects to fiber optic interconnects for any link longer than a few meters. This has been due to the excellent loss and signal integrity characteristics of optical fibers,

and also due to advances in design and manufacturing of integrated photonic transmitter and receiver components. Optical links that transmit 400 Gbps over 2 km on a single fiber are being deployed in data centers today, and fiber parallelism enables large aggregate network throughput. However, even as overall internet traffic demand is growing, demand for low-latency and high bandwidth machine-to-machine communication within data centers is growing faster. Next-generation data centers will need to support 800 Gbps links within the decade, and 1.6 Tbps, 3.2 Tbps, and 6.4 Tbps ones not long thereafter. The current paradigm of widely-deployed optical link technologies won't be able to scale to meet this demand in a cost-effective and energy-efficient way, or maybe not at all. Therefore, the optics industry will need to innovate on the fundamental link technology to deploy data center optical interconnects that can power the computing and communications revolutions for years to come.

The aim of this dissertation is to outline the foundation for such a technology. Coherent optical links, which are widely deployed for longer-reach are an attractive option because of their high data rates, but as we will see, face significant challenges in reducing power consumption and cost. This work will describe novel coherent link architectures that are redesigned from the perspective of optimized energy efficiency for short-reach intra-data center links. It will be shown that competitive power consumption is achievable for these links, and that a departures from the design regimes of both short- and long-reach conventional link technologies are required to optimize performance.

1.2 Optical Switching Networks

One of the most promising technologies for improving data centers is optical switching. Conventional data center networks are based on folded-Clos, or fat tree topologies, where servers connected to each other and to the outside world by optical links to multiple layers

of electronic packet switches. Switches with 51.2 Tbps of total data throughput are being deployed today, and subsequent generations supporting 102.4 Tbps and 204.8 Tbps are planned in the coming years. These switches can route vast quantities of data through the data center and facilitate server communication, but because they have to convert optical signals to electrical ones, process and route the packets, and convert the electrical signals back to optical ones, they add significant energy consumption, cost, and latency. In contrast, optical switches do no signal conversion, but simply route input optical signals to desired outputs. Various optical switching technologies are possible, with different benefits and different amounts of technical difficulty.

The most promising technologies are based on optical circuit switching (OCS), in which optical connections are reconfigured slowly and left in place for a period of time. The optical signals can either be routed by a wavelength-selective switch, or by a broadband switch. The former option enables more fine-grained adjustment of server connectivity, but is challenging to implement and has not been demonstrated with low losses for high port counts [1]. Broadband switches based on rotating MEMS mirrors, on the other hand, have already been widely deployed in data center networks by Google [2]. They were able to replace an entire layer of electronic packet switches in their network with optical circuit switches, which resulted in significant improvements of 41% power consumption and 30% cost in the network. In addition, these optical switches provided improvements in overall network throughput and the ability to incrementally deploy hardware during data center upgrades. This is because a dynamically reconfigurable optical switch-based network enables intelligent and low-latency resource interconnection that can improve computation run times and server utilization. Even though the optical circuit switches are not able to reroute every single packet of data, a simple reconfiguration to allocate network bandwidth to the resources that need it for a particular compute job can significantly improve the performance of that job. The OCSs can then recon-

figure to support the next job, where each network configuration can be maintained for timescales of a few seconds or minutes. There is still work to be done on full-system resource optimization with reconfigurable OCS-based networks, but a >2X energy efficiency improvement *for the entire system* (not just the network) has been projected [3].

A more comprehensive vision for optical switching, known as optical packet switching, involves reading and interpreting header information in the optical domain, and performing fast optical routing on each incoming packet. This technology is still nascent, however, and it is clear that most of the advantages of optical switching can be reaped with circuit switches, which already have mature and robust implementations.

Besides the development of the optical switches themselves, and their associated controls and algorithmic schemes, the intra-data center optical interconnects need to support the additional losses they introduce into the link. These losses can vary depending on the optical switch technology, from 2 dB for MEMs mirror switches to >10 dB for high port count or wavelength selective switches based on integrated optics. Additional impairments such as signal crosstalk and polarization dependent loss must also be accommodated. A key feature of coherent links inside data centers is that they have much larger link loss budgets and therefore allow the inclusion of optical switches in the network.

Although a large portion of this dissertation focuses on improving the energy efficiency of these intra-data center coherent links, it is important to note the power savings that could be achieved be making the link transmitters and receivers themselves infinitely efficient would be dwarfed by the potential power savings the could be achieved by replacing a layer of power hungry electrical switches with optical ones, or by increasing server utilization and computation efficiency across the whole data center. It will be shown below that short-reach coherent links can be made to operate at low power, but even if they couldn't, their enlarged link loss budgets that support optical switching would still improve overall data center energy-efficiency.

1.3 Preview of Dissertation

The remainder of this dissertation will cover the design, implementation, and future prospects of energy-efficient intra-data center coherent optical links. Design methodologies and architectures for conventional intra-data center links and longer-reach coherent links will be described in Chapter 2, as well as the newly proposed low-power coherent architecture. Chapter 3 will outline an analysis and optimization framework for short reach coherent performance and power consumption. A high-speed packaging platform implementation will be presented in Chapter 4, showing characterization capabilities above 100 Gbaud. Design and measurement of high-speed and low-power travelling wave modulators and drivers will be discussed in Chapter 5. The first O-band coherent full-link measurement results, including the first >200 Gbps/λ O-band link of any kind, will be reported in Chapter 6. Finally, Chapter 7 will conclude with a discussion of future work.

Chapter 2

Low-Power Optical Links

2.1 Intensity Modulation and Direct Detection

This chapter will give an overview of the current state-of-the-art optical link technologies, and describe their relative tradeoffs, advantages, and future development challenges. Short-reach intra-data center optical links deployed today are all based on intensity modulation and direct detection technology (IMDD). This is a simple and robust link architecture in which data is encoded by modulating the intensity of the transmitted light.

IMDD links can be implemented with multiple photonic and electronic technologies. At the receiver, either vertically incident or waveguide coupled photodiodes (PDs) absorb light and generate a photocurrent signal that is amplified and detected. More advanced devices like avalanche photodiodes (APDs) can be used to trade off gain and bandwidth for improved performance. For the transmitter, directly modulated lasers (DML), or externally modulated lasers (EML) are possible. In the former, the laser diode itself it directly modulated to change the intensity of the emitted light. This category includes both waveguide-coupled lasers as well as vertical-cavity surface-emitting lasers (VCSELs). EMLs, on the other hand, integrate a laser with a separate modulation de-

vice. While adding complexity, this approach allows more degrees of freedom in designing laser performance as well as modulation efficiency and bandwidth.

A typical architecture for a single-wavelength IMDD link based on an EML is shown in Fig. 2.1, and a similar schematic for a VCSEL-based link is shown in Fig. 2.2 Several material systems and modulation technologies can be used for these photonic integrated circuits (PICs). In InP, electro-absorption modulators (EAMs) can modulate the band edge of the device, and thus absorption of incoming light, through the quantum confined stark effect, or through the Franz–Keldysh effect. The electro-optic effect in InP, or other material systems like $LiNbO_3$, can modulate the phase of the incoming light. When such a phase shifter modulator is placed within a Mach-Zehnder interferometer biased at quadrature, this phase modulation can be converted to an intensity modulation. High-speed phase shifters and Mach-Zehnder modulators (MZMs) can also be implemented on a silicon photonic (SiPh) material platform, using the free carrier plasma dispersion effect. While SiPh platforms offer low-loss waveguides and components with immense potential for integration, the modulation efficiency of SiPh-based pn-junction phase shifters is inferior to that of the electro-optic modulators that can be fabricated in InP or $LiNbO_3$. Heterogeneous integration platforms that can cost-effectively combine the passive component performance and integration of SiPh with the optical gain and efficient high-speed modulation capabilities of InP, $LiNbO_3$, or other materials may provide the best-of-both-worlds PIC fabrication platform for optical communications.

For each of these cases, an electrical driver circuit must be integrated to drive the desired modulator, and a receiver amplifier chain based on a low-noise transimpedance amplifier (TIA) at the input are required. Driver and TIA implementations include complimentary metal-oxide semiconductor (CMOS) inverters and bipolar SiGe differential pairs, and can be designed to integrate with either lumped capacitive loads or distributed ones.

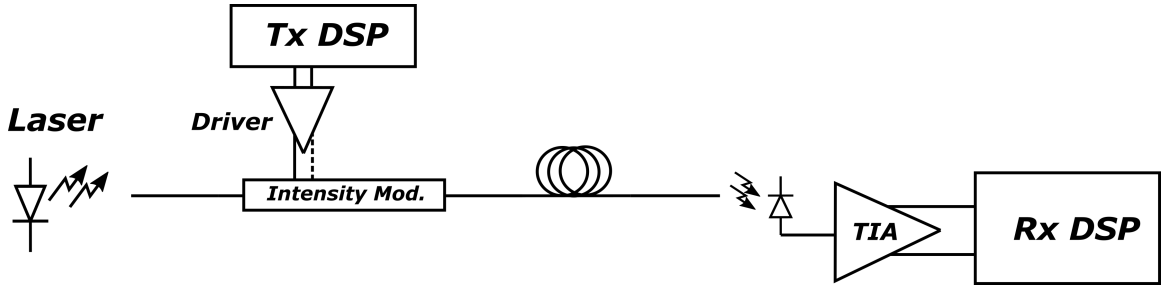


Figure 2.1: Schematic of a standard IMDD link with DSP and an externally modulated transmitter.

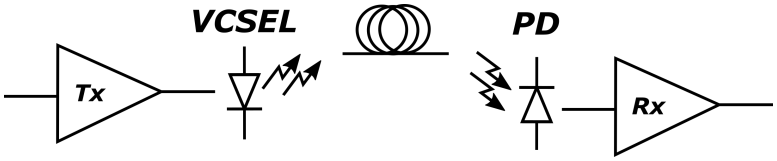


Figure 2.2: Schematic of a standard IMDD link with a VCSEL or DML transmitter.

Due to the high bandwidth of optical fibers, these interconnects can make excellent use of parallel transmission on multiple wavelength channels co-propagating on a single fiber. This enhances a link's cost effectiveness, as a single transceiver can multiply its data throughput given the same fiber plant infrastructure. Four or even eight wavelengths (λs) can be combined in a wavelength multiplexer (MUX) at the transmitter, and separated by a wavelength demultiplexer (DEMUX) at the receiver. These devices can be integrated with a PIC or purchased as a separate glass planar lightwave circuit (PLC) component, and can achieve low losses and crosstalk. In addition, devices such as ring resonators can perform wavelength-selective modulation combining or extracting optical signals from multiple laser wavelengths directly. Such highly parallel ring resonator circuits are promising, but have yet to be deployed widely.

Simple IMDD links can use two-level non-return-to-zero signalling (NRZ) to encode one bit of information per symbol, while in recent years, widespread deployment of links with higher order modulation has begun. Data center links operating over 25 Gbps/λ. IMDD links employing 4-level pulse amplitude modulation (4-PAM), which encodes 2

bits of data per symbol have begun to be deployed, and there are proposals for 6- or 8-level PAM to support higher data rates in future generations.

The transition to 4-PAM has marked a turning point in IMDD optical link development. NRZ links can be implemented with extremely low power consumption by utilizing limiting electronic circuits for the driver and receiver. 4-PAM links, on the other hand, require more complex and high-power linear electronics. The greater signal-to-noise ratio (SNR) requirements for 4-level signalling mean that laser output power and link loss specifications also become more constrained. New digital signal processing (DSP) application-specific integrated circuits (ASICs) need to be incorporated in the link to equalize linear inter-symbol interference (ISI) in the link, as well as to interface with host-side serializer/deserializer (SerDes). These DSP chips account to for large fractions of the cost and power consumption of modern 4-PAM links. Moreover, while NRZ links were able to achieve error-free operation, corresponding to a bit error rate (BER) $< 10^{-12}$, 4-PAM links must rely on forward error correction (FEC) in the DSP to make links effectively error free. FEC adds latency on the order of 100 ns for the 400G generation [4], and contributes significantly to DSP power and cost. Despite this, 4-PAM IMDD solutions are being widely deployed and further developed to scale data rates for intra-data center optical links [5].

2.2 Coherent Modulation and Detection

In contrast to IMDD links, which modulate and detect the intensity of the optical signal, coherent links modulate and detect both the amplitude and phase of the optical signal. The signal is often decomposed into orthogonal in-phase (I) and quadrature (Q) channels, effectively doubling the data rate relative to a link with a single intensity channel. Furthermore, coherent links can incorporate polarization-multiplexed signals,

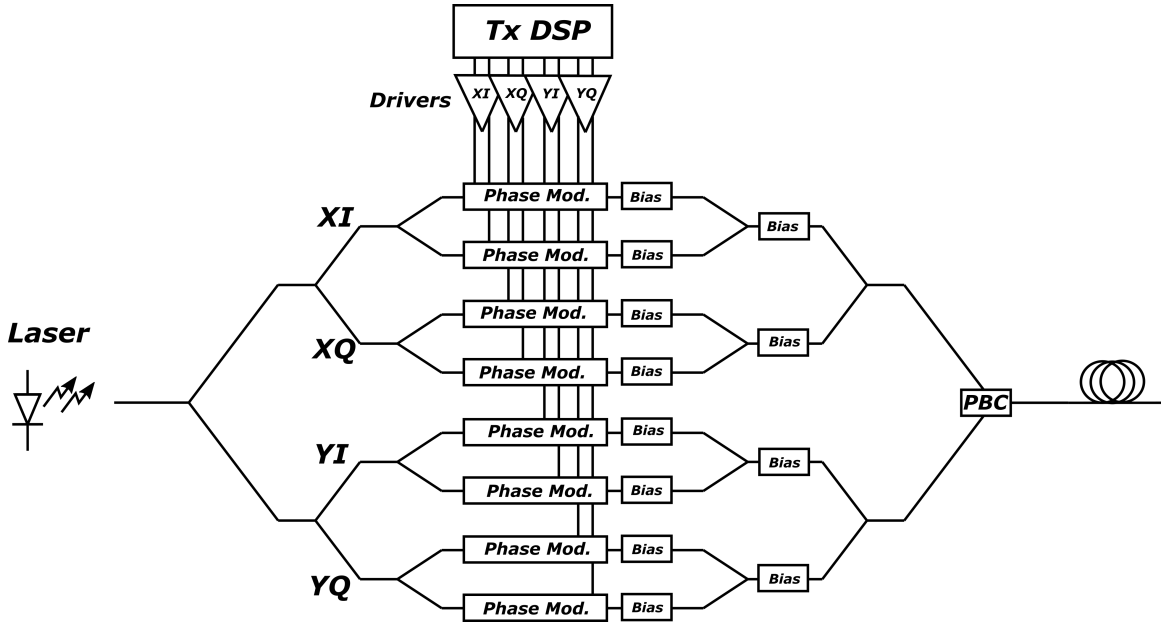


Figure 2.3: Schematic of a standard coherent transmitter. PBC: polarization beam combiner.

increasing the effective channel count to 4 per wavelength (two orthogonal polarizations, X and Y, each with I and Q channels).

In order to recover the phase information for coherent detection, the incoming signal is mixed with a local oscillator (LO) signal at the receiver. As the LO can come directly from a high-power continuous wave laser, this has the added benefit of introducing coherent gain and improving the sensitivity of the receiver. Whereas for IMDD the received photocurrent is directly proportional to the optical signal intensity, for coherent detection we have

$$I_{pd} \propto \sqrt{P_{sig} P_{LO}}. \tag{2.1}$$

The data rate and sensitivity benefits of coherent come at the cost of higher power consumption, cost, and complexity. Fig. 2.3 shows a schematic of a standard coher-

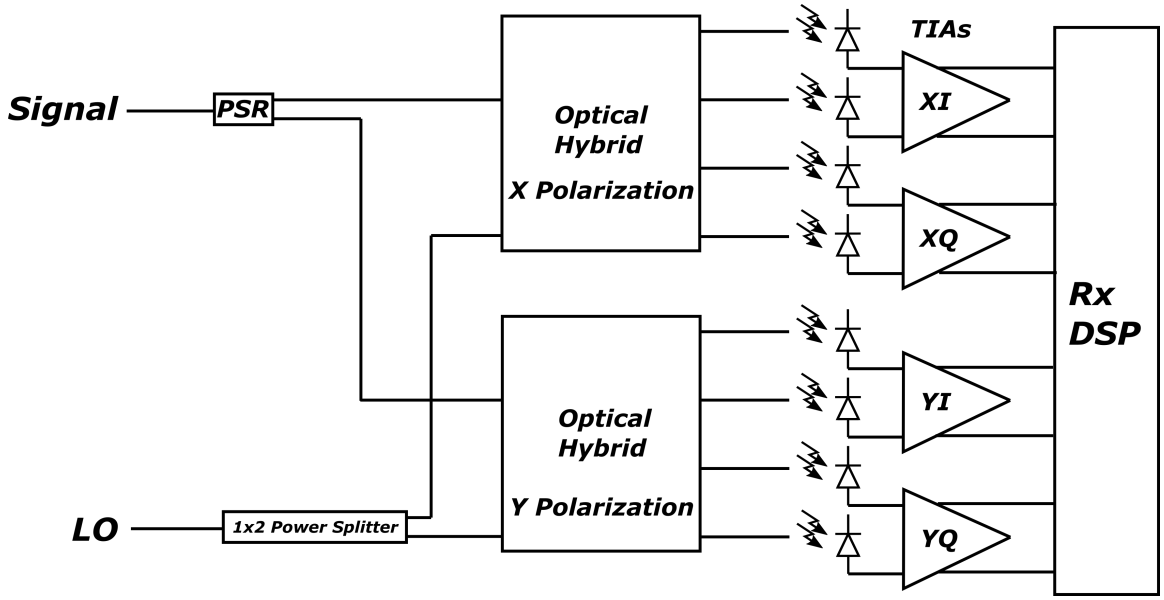


Figure 2.4: Schematic of a standard coherent receiver. PSR: polarization splitter rotator.

ent transmitter (Tx), and Fig. 2.4 shows a corresponding receiver schematic. At the transmitter, 4 MZMs are nested to form a dual-polarization (DP) IQ modulator, and at the receiver, the signal and LO must be mixed in an optical hybrid for each polarization channel. Furthermore, conventional coherent links require more complex DSP to perform carrier recovery and polarization recovery, since the signal polarization may have rotated randomly on the fiber and since the Tx and LO laser phases may drift apart. Current DSP-based coherent links consume ∼40 pJ/bit, of which roughly half comes from the DSP ASIC [6]. Increased FEC complexity, too, adds latency on the order of 10 μs [6].

As digital CMOS electronics technology scales to shorter nodes, coherent DSP and power consumption becomes more attractive for higher volume markets. Coherent links are widely used today for long-haul transmission, and are beginning to be deployed for shorter reaches >40 km [7]. The trend of coherent link penetration into shorter and shorter reach applications will continue, with 10 km links in development and 2 km intra-data center links soon to follow.

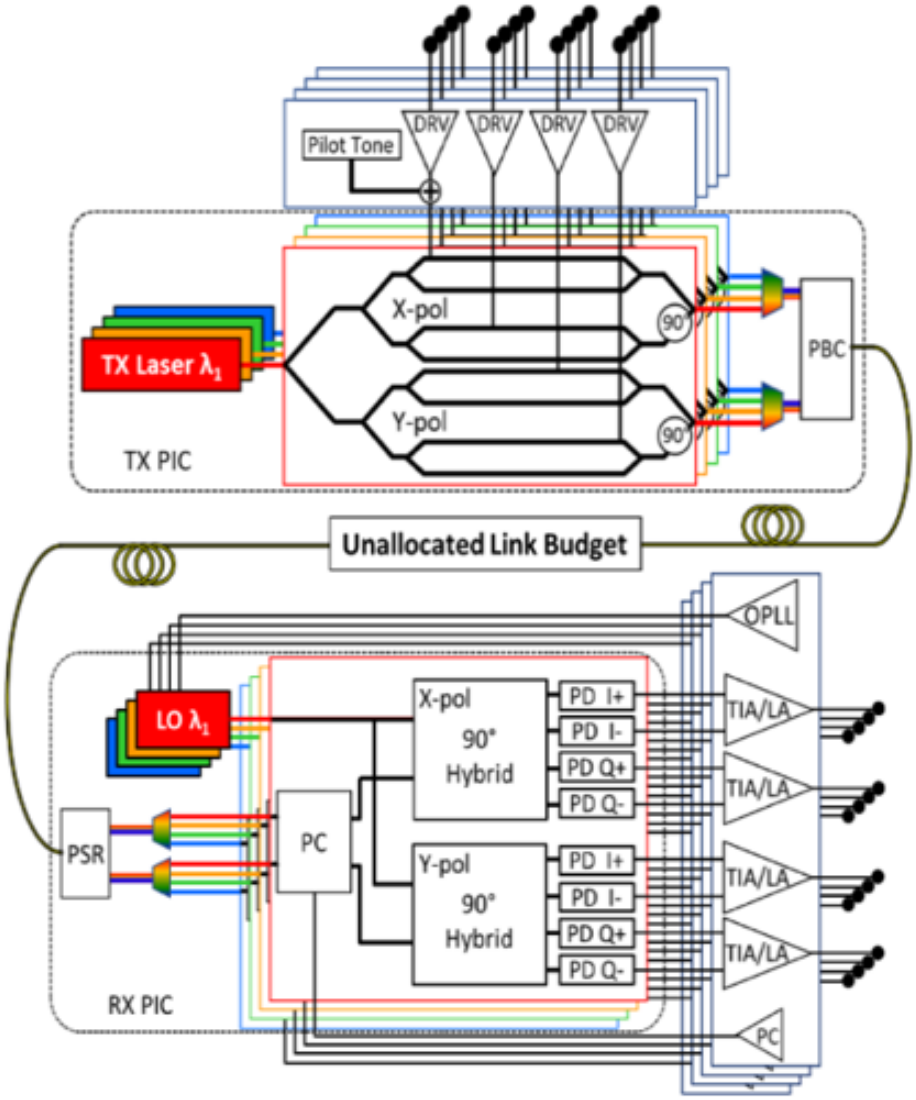


Figure 2.5: Schematic of a proposed analog coherent detection-based optical link. PC: polarization controller. OPLL: optical phase locked loop.

2.3 Analog Coherent Detection

An alternative approach to short-reach coherent optical links is analog coherent detection (ACD) [10]. The core principle of an ACD-based link is to offload functions from the DSP ASIC and perform them efficiently in the analog domain. This saves power and cost, and we have shown through link energy-efficiency analysis that power consumption

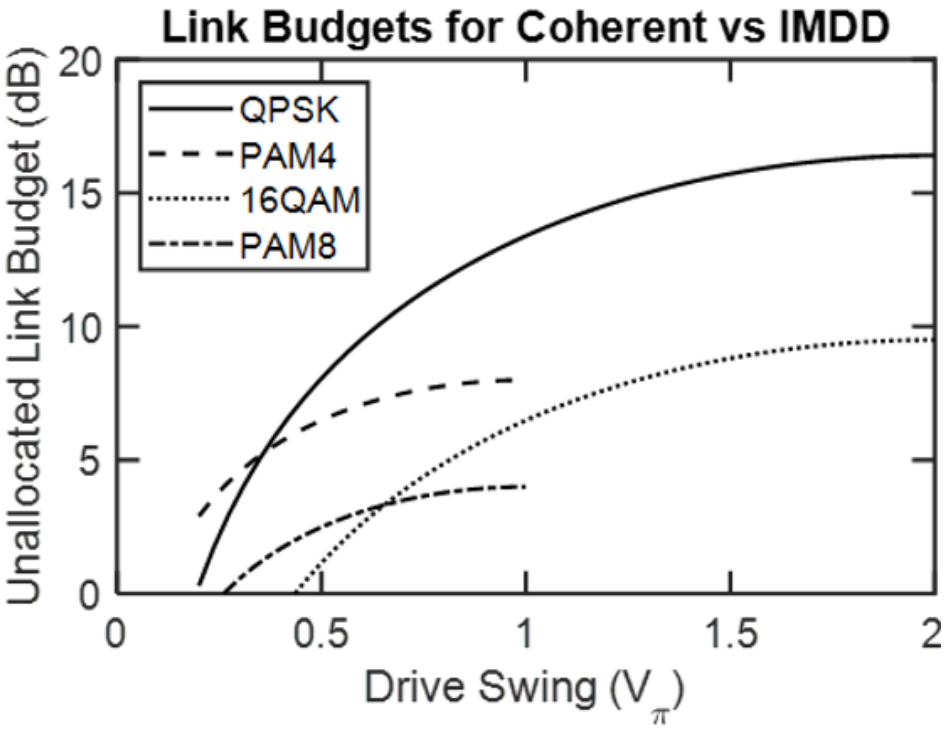


Figure 2.6: Link budgets vs driver voltage swing for various coherent and IMDD modulation formats.

on the order of 5-10 pJ/bit is possible with this architecture, which is shown in Fig. 2.5 [8].

The first such DSP function that can be transferred to the analog domain is carrier recovery. Conventional coherent links require the wavelengths of the Tx and LO lasers to be aligned within a few GHz, and then rely on a DSP-based carrier recovery algorithm to accommodate frequency and phase offsets between the lasers that arise from laser phase noise and thermal drift. Alternatively, an ACD-based link employs an optical phase locked loop (OPLL) to lock the frequency and phase of the LO to that of the incoming signal. This OPLL is formed from the coherent receiver components on the PIC, the receiver chain and phase frequency detector (PFD) circuit in the Rx EIC, and an off chip loop filter. Integrated OPLLs have been demonstrated, and shown to support error-free link operation for up to 35 Gbps binary phase shift keying (BPSK), in [9].

One critical requirement for such an OPLL is that the loop delay — the total time

it takes for the LO output light to mix with the incoming Tx signal, get absorbed in the PDs, get amplified in the Rx EIC, pass through the PFD and loop filter, and return to tune the LO frequency to correct for any offsets — must be short. The loop delay is critical for the stability of a loop that must track laser frequency and phase variations up to 100s of MHz or even GHz. Thus, a key technological requirement for the realization of an OPLL (and thus an ACD-based link) is that the LO must be integrated with the Rx PIC. This enables loop delays on the order of 100-200 ps, which would not be possible with a fiber-coupled LO.

The second DSP function that can be transferred to the analog domain is the polarization controller. This circuit serves to demultiplex the received polarization channels, even if the signal underwent an arbitrary polarization state rotation on the fiber. An optical polarization controller circuit can be realized by a set of cascaded phase shifters and 2x2 couplers, and reset-free operation has been demonstrated [11].

Finally, while conventional coherent links operate in the C-band, near the 1550 nm minimum-loss point in standard fibers, ACD links are designed to operate in the O-band, near the 1310 nm zero-dispersion point instead. This is a fundamental tradeoff for short-reach coherent links. The difference in transmission loss — 0.1 dB/km at 1550 nm, compared to 0.2 dB/km at 1310 nm — is critical for long-haul links, but becomes a minor inconvenience for links <2 km. And because of the short link length, if the link is operated at or near the zero dispersion wavelength, the chromatic dispersion penalty becomes negligible [10]. This enables the elimination of the dedicated chromatic dispersion (CD) compensation function in the coherent DSP, further improving energy efficiency.

The the ACD architecture discussed here is based on quadrature phase shift keying (QPSK), which uses simple NRZ signalling for each individual channel. When a polarization controller is combined with an OPLL for carrier recovery, these functions

ensure that the photocurrent signals at the Rx PDs simply contain the demultiplexed data for each individual channel (XI, XQ, YI, and YQ). Thus, ACD-based links can use low-power and robust limiting NRZ-based electronic circuits for the driver and Rx EICs. Furthermore, as linear operation is no longer required in the DSP either, power-hungry analog-to-digital converters (ADCs) can be omitted from the ASIC.

A further benefit of using QPSK modulation is that reduced SNR requirements at the receiver improve the link loss budget of the link. As shown in [12], while coherent links benefit from coherent gain from the local oscillator, increased optical losses in the transmitter can negate this benefit. For conventional coherent link architectures that use 16QAM, this can result in the same, or even worse available link budget than a comparable IMDD link. QPSK, however, can surpass the performance of all of these alternatives and tolerate additional losses in the link. Fig. 2.6 shows the available link budget for various modulation formats vs the driver output swing used at the transmitter [8]. The link parameters used to calculate the link budgets were based on those reported in [12], with the addition of a curve for QPSK, which shows significant improvements over PAM4 and 16QAM above 0.5 V_π of voltage swing.

While certain functions, such as FEC, differential decoding, and SerDes interfaces, may need to remain to successfully integrate an ACD-based link into a data center system, the techniques described above can significantly reduce the power consumption of a coherent link. This holistic optimization of the entire link architecture is required to adapt coherent links for short-reach applications inside the data center.

Chapter 3

Short-Reach Coherent Link Optimization

3.1 Introduction

Fiber optic intra-data center network bandwidth has grown rapidly in recent years, and is projected to continue to do so, driving the need for continued optical transceiver performance scaling. As transceiver datarates surpass 1 Tb/s, scaling current pulse amplitude modulation (PAM) intensity modulation direct detection (IMDD) links requires increasing some combination of the baudrate, the number of PAM modulation levels, or the number of parallel fibers/wavelengths. Each of these strategies have significant challenges, and while IMDD may be able to support transceiver datarates above 1 Tb/s, it will soon become preferable to use coherent modulation and detection for high-bandwidth intra-data center links [12].

Coherent links, which can provide 4X increased datarate per wavelength relative to a comparable IMDD system due to polarization multiplexing and in-phase and quadrature (IQ) modulation, have been widely used in long haul and metro network applications, and

more recently for inter-data center links below 120 km using the 400ZR standard [7]. Advances in photonic integrated circuit (PIC) technologies and continued scaling of coherent digital signal processing (DSP) application-specific integrated circuits (ASICs) implementation nodes are improving the form factor, cost, and power consumption of coherent links to rival IMDD links for short-reach intra-data center applications. In addition, our recent work has investigated the possibility of using an analog coherent detection (ACD) architecture to perform the DSP functions of carrier recovery and polarization recovery in the optical domain, removing the need for power-hungry analog-to-digital converters (ADCs) and further improve coherent link power efficiency [8].

Developing coherent links for short-reach applications requires new design tradeoffs to meet the stringent power efficiency, size, cost, and interoperability requirements for intra-data center links, as opposed to the fiber capacity maximization requirements typical of longer reach coherent link implementations. Already in the 400ZR architecture, module power consumption is reduced by driving the Mach-Zehnder modulator (MZM) with an input swing well below 1 V_π. There have been several proposals for modified DSP implementations targeted for power savings in short-reach coherent links [13, 14]. Most notably, chromatic dispersion (CD) is negligible for 50 Gbaud links under 2 km, and thus CD compensation can be bypassed or omitted in the DSP [10]. Higher baudrate links may become more sensitive to CD, limiting their application to shorter reaches, or requiring the re-introduction of CD compensation. Short-reach coherent architectures using analog signal processing [15] or self-homodyne [16, 17] techniques to reduce DSP power consumption have also been proposed. The trend of optimization for shorter reach applications will have to continue and be applied to other aspects of the link to enable viable intra-data center coherent links.

The power efficiency of an optical transceiver is not, however, a complete picture of its effect on overall data center power consumption. Advances in the field of optical

switching have brought forward the possibility of including passive arrayed waveguide grating routers (AWGRs) or actively controlled optical switches into data center network architectures. There are proposals to replace a layer of electrical switches in current data center architectures with a layer of AWGRs or optical switches, achieving great power savings [1,18]. Additionally, data center network requirements are rapidly morphing with the rise of diverse artificial intelligence and machine learning workloads. This makes real-time network reconfiguration though optical switching especially attractive, as it has the potential to not just save power by replacing electrical switches, but also by increasing server utilization across the data center [19–21]. The potential power savings from this approach is not limited to the portion of overall data center power that is consumed by the network, but by the possible overall improvements in server utilization across the data center. Overall data center efficiency improvement of > 2X was projected in [3]. Thus, a critical consideration for supporting future data center growth is not just the power efficiency of the optical links themselves, but also their ability to support the inclusion of optical switches or AWGRs in the network. The available link budget of future intra-data center links is therefore crucial, since optical switches and AWGRs introduce additional losses that need to be accommodated. Coherent receivers have improved sensitivity over IMDD, and coherent links that use QPSK modulation can support greater overall link budgets than comparable IMDD links, making them attractive for optical switching applications [8].

Optical amplification is commonly used in conventional coherent links in the form of erbium doped fiber amplifiers (EDFAs) to extend link reach, and integrated semiconductor optical amplifiers (SOAs) to boost the optical power output of the transmitter (Tx), or to preamplify the signal at the receiver (Rx) [22, 23]. In this paper, we present an analysis of optical amplification, namely SOAs integrated with the coherent PICs, as applied to short-reach coherent links. Design tradeoffs between Rx sensitivity, total link

budget, compatibility with optical switching, inter-symbol interference (ISI), and link power consumption will be examined, with the goal of outlining short-reach coherent link architectures with optimized power efficiency and viability for implementation in data centers. Optimization for link power consumption gives rise to new design spaces for short-reach coherent links in which shot, thermal, and amplified spontaneous emission (ASE) noise can all contribute substantially to overall noise at the receiver. This hybrid regime contrasts sharply with both conventional coherent links dominated by ASE noise and IMDD links dominated by thermal noise, and thus careful design is required to optimize coherent links for short-reach applications.

Section 3.2 will describe the various link architectures that will be examined. Section 3.3 will examine the link performance penalties associated with the addition of optical amplification under various architectures. Section 3.4 will present an analysis of link power efficiency incorporating optical amplification. These results will be compared to other coherent link architectures in Section 3.5. Concluding remarks will be made in Section 3.6.

3.2 Link Architecture

The generalized coherent link architecture that will be considered in this paper is shown in Fig. 3.1, where 5 possible locations for SOAs have been highlighted. The optical components in this diagram can be integrated into a Tx, Rx, or combined PIC using a photonic integration platform such as [24] or [25]. The SOA in position #1 serves to directly boost the Tx laser output power with minimal impairment to the link, since a constant input power will not induce an SOA pattern effect. The principle drawback of using an SOA in this position is that the high input optical power will saturate the SOA gain. In positions #2 and #3, which come after the MZM, the attenuated input

signal allows higher SOA gain, but the SOA pattern effect will introduce ISI. In these positions, the SOAs each amplify one of the two polarization channels, since SOAs are typically implemented as single-polarization devices. If wavelength division multiplexing (WDM) is used, as in the ACD-based architecture described in [8], a single pair of SOAs in position #3 can amplify all the wavelengths simultaneously after the multiplexer (MUX). Compared to position #2, this has the potential to greatly reduce power consumption in the SOAs, but will suffer from additional gain saturation, ISI, and crosstalk impairments. Similarly, SOAs in positions #4 and #5, before and after the demultiplexer (DEMUX), respectively, would act as Rx pre-amplifiers. SOAs in either of these positions would benefit from reduced nonlinear effects due to a further attenuated input signal, but would also contribute higher ASE noise at the Rx.

In-line fiber amplifiers are commonly included in longer reach coherent links, but are not considered in this analysis, as power and size requirements for intra-data center applications would be prohibitive compared with SOAs that can be readily integrated with transceiver PICs or packages. Moreover, as will be shown, additional in-line amplifiers are not needed to close short reach coherent links that have < 1 dB of fiber losses, even for demanding link budgets that include optical switches.

3.3 SOA Noise and Gain Saturation

In the architectures proposed here, the ASE noise in the SOAs introduces a current noise at the photodiodes (PDs) dominated by the beating of the LO signal with the SOA ASE noise. The ASE-induced current noise variance when detected at a PD can be expressed as

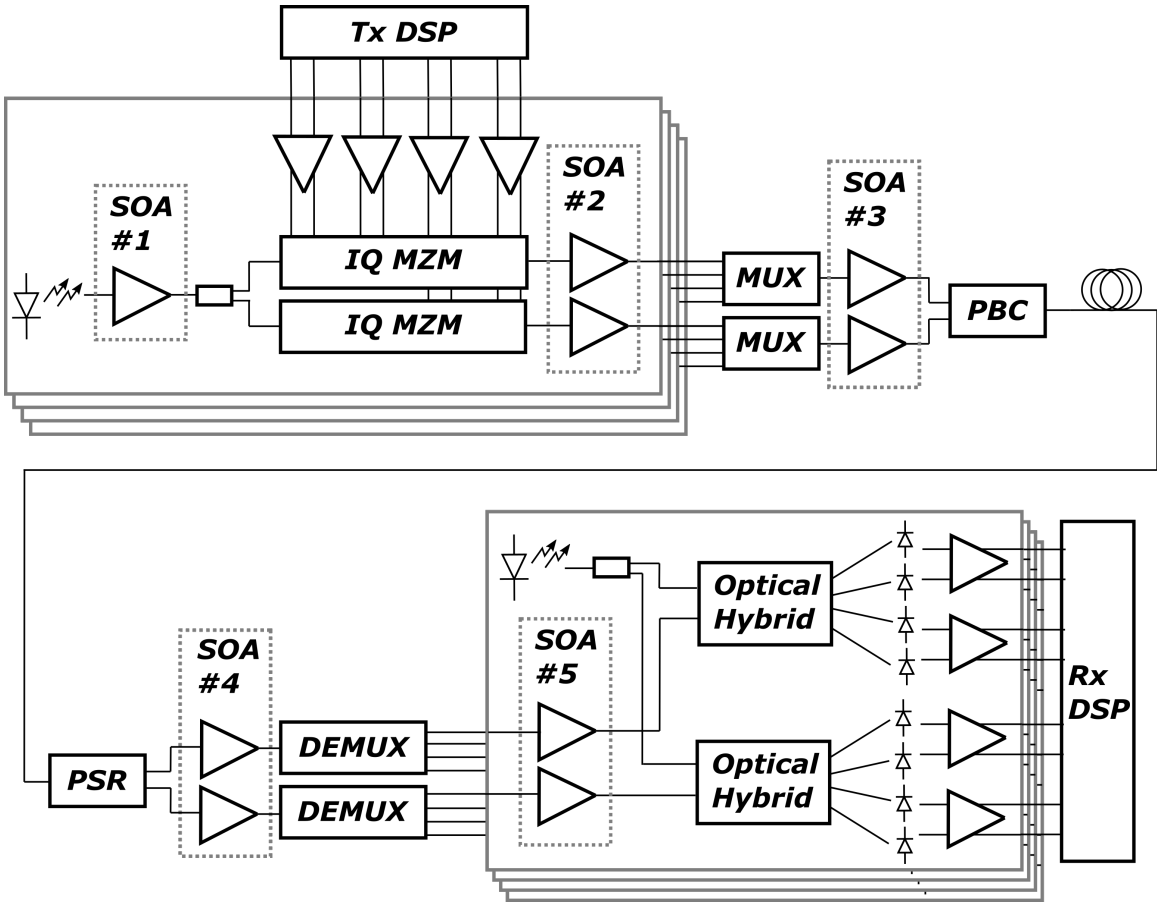


Figure 3.1: General coherent link architecture. Boxes labeled SOA #1-5 indicate potential SOA insertion points throughout the link.

$$\sigma^2_{ASE} = 4\mathbb{R}^2|E_{LO}|^2 S_{ASE}\Delta f \tag{3.1}$$

where $\mathbb{R}$ is the PD responsivity, E_{LO} is the normalized field from the LO, S_{ASE} is the optical power spectral density of the SOA ASE noise, and Δf is the receiver bandwidth. The ASE noise spectral density at the SOA output is calculated from

$$S_{ASE} = n_{sp}\frac{hc}{\lambda}(G-1) \tag{3.2}$$

where n_{sp} is the population inversion factor of the SOA, hc/λ is the photon energy, and G is the SOA gain [26]. Due to the mixing in the optical hybrid, the ASE-induced noise currents at each differential PD pair are correlated, and the total ASE-induced RMS current noise is $\sigma_{ASE,I} = \sigma_{ASE,Q} = \sqrt{2}\sigma_{ASE}$.

In addition, SOA gain saturates with increasing input optical power, and can be written as

$$G = G_0 e^{-(G-1)P_{in}/P_{sat}} \tag{3.3}$$

where G is the saturated gain of the SOA, G_0 is the unsaturated or low input power gain of the SOA, P_{in} is the input optical power, and P_{sat} is the saturation power parameter [27]. P_{sat} is an internal parameter that does not correspond directly to either the input or output 3 dB gain saturation points. Static gain saturation would have the largest effect on SOA #1 in Fig. 3.1, since the optical input power will be the highest directly after the Tx laser.

For SOAs in positions #2-5, instantaneous changes in the power of the modulated signal at the SOA input will cause the saturated gain to fluctuate, inducing nonlinear signal distortions known as the pattern effect and nonlinear phase noise (NLPN). The pattern effect and NLPN have been well studied for IMDD applications [28, 29], as well as coherent 16QAM [30, 31] and RZ-QPSK [32, 33]. There has not however been an experimental investigation of SOA nonlinear effects on QPSK. A QPSK-modulated signal, which is used in the ACD architecture, has a quasi-constant power envelope where the only SOA input power fluctuations occur during bit transitions. Thus, it is inherently more robust to SOA nonlinearities than IMDD or higher order QAM modulation formats. To investigate the performance of SOA-amplified QPSK, a time-domain simulation was

used. The optical field at the SOA output is described by

$$E_{out}(t) = E_{in}(t)e^{h(t)(1+j\alpha)/2} \tag{3.4}$$

where $E_{in}(t)$ is the modulated field at the SOA input, $h(t)$ is the instantaneous SOA gain parameter, and α is the SOA linewidth enhancement factor, which describes the relationship between gain fluctuation and the induced NLPN. The instantaneous SOA gain is described by

$$\frac{d}{dt}h(t) = \frac{h_0}{\tau_c} - \frac{h(t)}{\tau_c} - (e^{h(t)} - 1)\frac{|E_{in}(t)|^2}{\tau_c P_{sat}} \tag{3.5}$$

where h_0 is the unsaturated SOA gain parameter and τ_c is the SOA carrier lifetime [27]. The SOA gain parameter $h(t)$ is related to the total SOA gain by $G = e^{h(t)}$.

In order to confirm this model for QPSK modulation, a coherent link was tested with an SOA (Thorlabs S9FC1132P) biased at 300 mA. The measured G_0 was 23 dB and the P_{sat} was 5 dBm. Measured output constellations for a reference link operating at 10 Gbaud QPSK are shown in Fig. 3.2 for SOA input power levels between -10 dBm and -22 dBm. For higher SOA input power levels, the SOA NLPN contributes substantial additional phase noise. The measured link results in Fig. 3.2 were replicated in a simulation that modelled the SOA using the above measured parameters as well as link component bandwidths and shot, thermal, and ASE noise contributions. The SOA carrier lifetime of $\tau_c = 200$ ps and linewidth enhancement factor of $\alpha = 5$ were estimated from the literature [27]. The measured and simulated root-mean-square (RMS) phase noise characteristics are compared in Fig. 3.2(e), showing good agreement across SOA

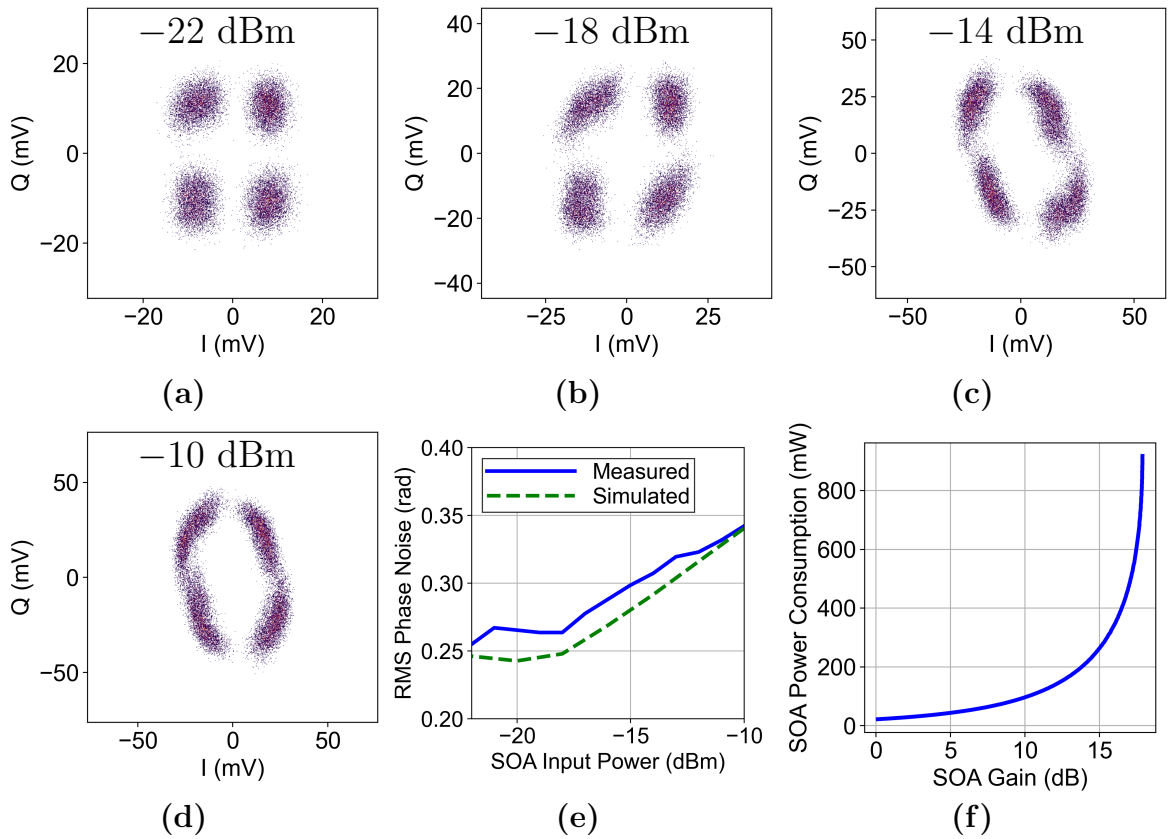


Figure 3.2: Measured sampled QPSK constellations depicting the SOA pattern effect and NLPN for SOA input power levels of −22 dBm (a), −18 dBm (b), −14 dBm (c), and −10 dBm (d). (e) Measured vs modeled RMS phase error for various SOA input power levels. (f) Simulated SOA power consumption P_{soa} vs saturated gain G.

input power levels and validating the above SOA analytical model for application to NLPN effects on quasi-constant power envelope QPSK modulation.

3.4 Power Efficiency Optimization

3.4.1 Simulation Model

The performance and power efficiency of the links considered here will now be modelled and compared in simulation. The simulation model incorporates static optical losses of various components, modulation efficiency of the Tx MZM, SOA gain, time-domain

simulation of BW effects and SOA nonlinearities, and various noise sources to compute the bit error rate (BER) at the receiver. All the simulations used a full PRBS15 sequence. One of the conclusions of our previous work analyzing short reach coherent links [8] was that for typical ACD links, optimal power consumption was achieved when the Tx and LO lasers were operating at high power, which is limited by laser reliability considerations. Therefore, a constant, realizable integrated laser power of 13 dBm is assumed in this work for both the Tx and LO lasers in ACD-based coherent links. For DSP-based coherent links, a 16 dBm ITLA is assumed, with equal Tx/LO splitting. All BW impairments are assumed to be single-pole low-pass filters. CD and polarization mode dispersion (PMD) are neglected. Nonlinear WDM crosstalk in each SOA is simulated in time-domain with uncorrelated aggressor signals. All of the parameters used in the simulations are shown in Table 3.1, for both ACD- and DSP-based coherent link configurations.

The power consumption of the link is optimized by trading off driver output voltage swing and SOA gain in simulation. All other link components are assumed to have a static contribution to the overall link power consumption, which will be considered in Section 3.5. The driver power consumption is calculated from

$$P_{driver} = c_0 + c_1 \frac{V_{driver}}{Z_0} + c_2 \frac{V_{driver}^2}{Z_0} \tag{3.6}$$

where V_{driver} is the desired output swing, Z_0 is the MZM impedance, and $c_{1,2,3}$ are coefficients that depend on the driver design and process. In this work, we define the output swing of the drivers in an ACD-based link by the rail-to-rail differential voltage, since limiting electronics may be used in concert with driver output stage peaking circuits. We define the output swing of the linear drivers required for DSP-based links by the peak-to-peak differential voltage, including any peaking from linear equalization. The SOA

Simulation Parameter	Value for ACD	Value for DSP	Notes
Modulation Format	QPSK	16QAM	
Baudrate	56 Gbaud	60 GBaud	
Target BER	$3.8 \cdot 10^{-3}$	$1.25 \cdot 10^{-2}$	HD-FEC and CFEC thresholds
Rx Adaptive Equalizer Taps	1	31	No DSP equalization in ACD link
Laser Power on PIC	13 dBm	16 dBm	Integrated for ACD, ITLA for DSP
Laser Splitting	N/A	50:50	
Driver Power Coefficient c_0	0.075 W	0.1 W	Linear driver power fit to commercial driver performance. Limiting driver power fit to performance in [34].
Driver Power Coefficient c_1	0.175 V	-0.375 V	
Driver Power Coefficient c_2	1.225	1.25	
Driver CTLE Peaking	6 dB		
Driver CTLE Frequency	50 GHz		
Driver Bandwidth	40 GHz		
MZM Bandwidth	30 GHz		
TIA Bandwidth	40 GHz		
MZM Phase Efficiency V_π	6.7 V		
MZM Z_0	30 Ω		
SOA Carrier Lifetime τ_c	200 ps		
SOA P_{sat}	15 dBm		Fit to performance in [35]
SOA α	5		
SOA n_{sp}	3.5		
SOA V_d	0.88		
SOA R_s	10 Ω		
Operating Wavelength	1310 nm		
Photodiode Responsivity $\mathbb{R}$	1 A/W		
TIA RMS Input Noise	7.2 μA		
Tx Excess Losses	9 dB		
Mux+Demux Excess Losses	2 dB		
Rx Excess Losses	5.5 dB		
LO Excess Losses	2 dB		
Fiber Loss	1 dB		

Table 3.1: Link simulation parameters.

power consumption is calculated from

$$P_{SOA} = V_d I_{SOA} + R_s I_{SOA}^2 \tag{3.7}$$

where V_d is the diode voltage drop and R_s is the SOA series resistance. The modeled SOA power consumption vs. saturated gain is shown in Fig. 3.2(f) for -11 dBm of input

power.

3.4.2 Simulation Results

The link simulation was carried out for each of the coherent architectures outlined in Section 3.2. For each configuration of driver output voltage and SOA gain, the link was simulated multiple times to determine the acheivable unallocated link budget (ULB), modelled as additional insertion loss on the fiber, while meeting the target BER. The simulation results for various architectures are shown in Fig. 3.3, where Fig. 3.3(a-d) show the combined driver and SOA power consumption vs. the saturated SOA gain G. ACD-based and DSP-based link power consumption are normalized to 200 and 400 Gbps/λ, respectively, ignoring forward error correction (FEC) overhead bits.

Across the simulations, power consumption is generally improved by operating at lower driver swings and higher SOA gains. Fig. 3.3(a) shows the link design space for an ACD-based link with an SOA in position #2, where compensating for reducing driver output voltage by increasing SOA gain results in lower overall power consumption for all ULBs plotted. Further modest improvements in power consumption are achieved by moving from SOAs in position #2 to WDM amplification with SOAs in position #3, as shown in Fig. 3.3(b) and (d), despite increased input power and crosstalk at the SOA from three other simulated WDM channels. WDM amplification improved power efficiency by a larger amount for the ACD-based architecture than for the DSP-based architecture due to QPSK's increased tolerance to SOA NLPN.

The expected drawback of an architecture with an SOA in position #1 was that the high input power from the laser would saturate the SOA. Indeed, Fig. 3.3(c), shows that large SOA gains were not attainable, as they were in Fig. 3.3(a), (b) and (d). This limits the power efficiency of this architecture compared to one with SOAs in position #2 or

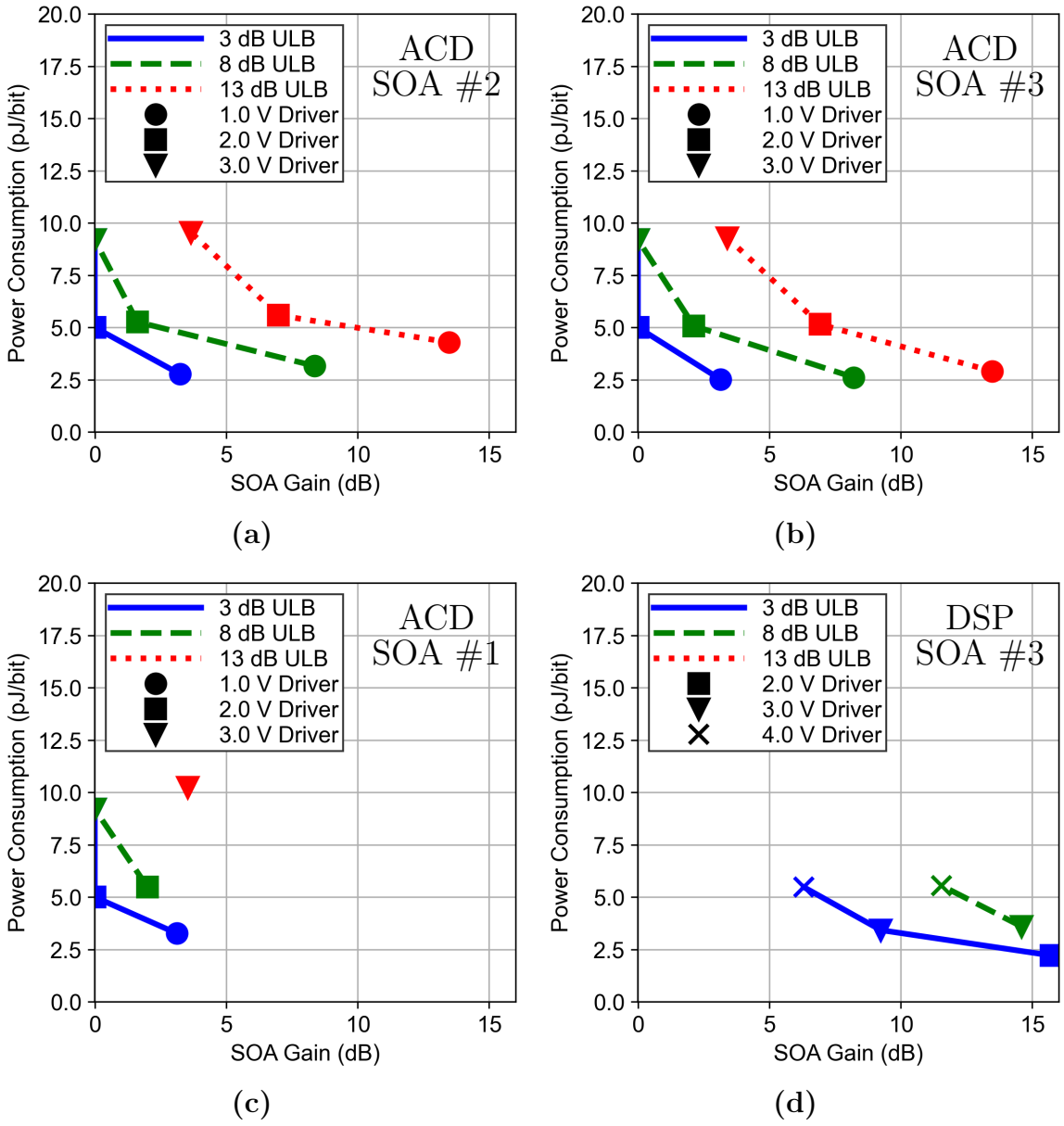


Figure 3.3: Driver and SOA Power consumption vs. SOA gain for an ACD-based link with SOA in position #2 (a), #3 (b), and #1 (c), and for a DSP-based link with SOA in position #3 (d), where each curve corresponds to a particular supported ULB, and the differential peak-to-peak driver output voltages are marked.

#3, where the minimally saturated SOA gain enables 6 pJ/bit better power efficiency for link operation at 13 dB ULB. Links with SOAs in positions #4 or #5 were dominated by ASE noise at the receiver that was unattenuated by link losses, and did not see improved

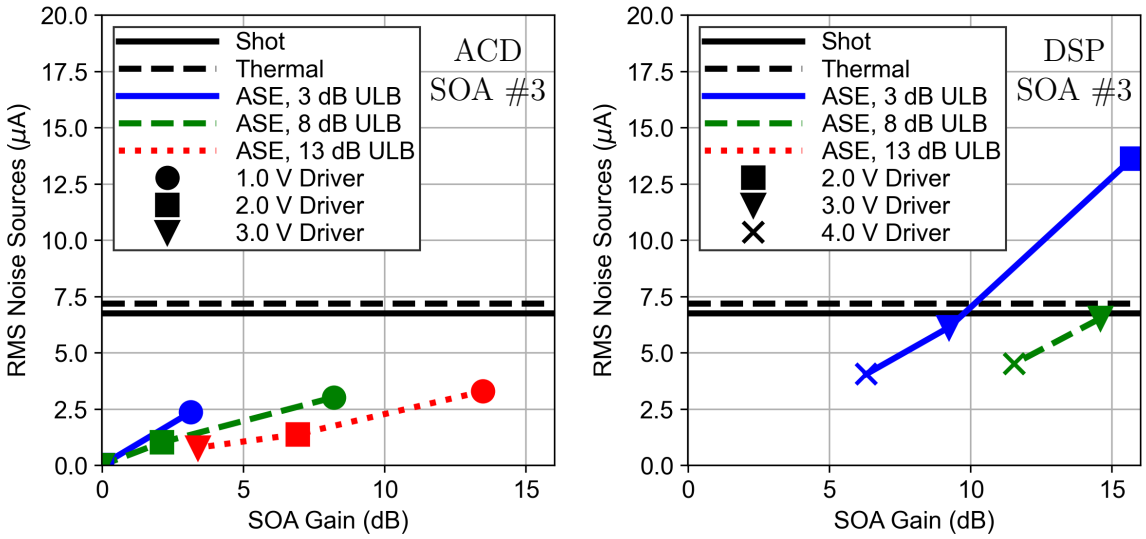


Figure 3.4: RMS noise currents at the receiver vs position #3 SOA Gain for an ACD-based link (e) and a DSP-based link (f).

performance for the link parameters assumed here.

The shot, thermal, and ASE noise components, referred to the input of the receiver and corresponding to the plotted results in Fig. 3.3(b) and (d), are shown in Fig. 3.4(a) and (b), respectively. While the shot and thermal noise levels remain constant, the ASE noise varies strongly with SOA gain. The ASE noise in the DSP-based link simulations was comparable to the receiver shot and thermal noise levels, and the ACD-based link simulations had lower, although non-negligible ASE noise contributions. The power consumption vs SOA gain curves in Fig. 3.3(c-f) do not reach an optimized minimum, however, because they were limited by the 16 dB maximum gain determined by the SOA model parameters that were chosen for this analysis. A higher-gain SOA design could enable power efficiency improvement with increased ASE noise contribution at the optimal operating point. These results suggest that short-reach coherent links optimized for power efficiency will operate in a hybrid regime in which the shot, thermal, and ASE noise contributions are all appreciable. This is a notable departure from current

conventional links, where long-reach coherent links are dominated by ASE noise and short-reach IMDD links are dominated by receiver thermal noise. In describing the links that operate in this hybrid noise regime, receiver BER sensitivity can no longer be characterized solely with respect to either received optical power or OSNR, but now requires a combination of both optical power and ASE noise information.

3.4.3 Optimization Theory

The simulation results in Fig. 3.3 were carried out for discrete and somewhat arbitrary driver swing and SOA gain values. Those results showed that driver voltage and SOA gain can be traded off for improved power efficiencies and supported link budgets. Here, we will develop a theoretical model for continuous optimization by examining figures of merit (FOMs) for the driver and SOA link budget improvement per additional pJ/bit of power consumption. Optimal link operation will then be characterized by a set of driver swing and SOA gain operating points where the respective driver and SOA FOMs are equal.

For coherent modulation with an IQ-MZM, the driver swing determines the effective optical loss of the modulator, which is given by the modfactor

$$F_M = sin(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})^2 \tag{3.8}$$

where V_{driver} is the differential peak-to-peak driver output voltage swing, L_{mod} is the phase shifter length of one MZM arm, and $V_\pi L$ is the modulator phase efficiency. The modfactor describes the effective loss due to not driving a full $2V_\pi$ in the MZM transfer function. For 16QAM, due to the presence of lower power inner constellation points, the MZM effective loss is degraded by an additional static 2.55 dB. In this analysis,

the modfactor loss directly corresponds to reduced available link budget. By defining $P_{driver}(V_{driver})$ as the driver power consumption in pJ/bit for a given driver voltage swing, converting the modfactor to dB, and differentiating, the driver figure of merit can be written as

$$\left.\frac{dF_M}{dP_{driver}}\right|_{dB} = \frac{5\pi}{ln(10)F_M}\frac{L_{mod}}{V_\pi L}sin(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})cos(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})\frac{dV_{driver}}{dP_{driver}} \tag{3.9}$$

where the driver power consumption is modelled as shown in Eqn. 3.6 and the differential is

$$\frac{dV_{driver}}{dP_{driver}} = \frac{1}{\sqrt{\frac{c_1^2}{Z_0^2} - \frac{4c_2(c_0-P_d)}{Z_0}}}. \tag{3.10}$$

A similar calculation can be carried out for an $FOM_{SOA} = dG/dP_{SOA}$, following well-known SOA gain and bias relationships [36]. The resulting power consumption and gain relationships are described by Eqn. 3.7 and Fig. 3.2(f). These FOMs, with units of dB/(pJ/bit), quantify the marginal link budget improvement associated with a marginal increase in power expenditure in either the driver or SOA, enabling a comparison of the efficiency of each component. The final FOMs for the driver and SOA, plotted against the driver voltage swing and the SOA gain, for the parameters assumed in this paper for an ACD-based link, are shown in Fig. 3.5(a). In agreement with the simulation results in Fig. 3.3, it is clear that at low SOA gains, the ULB can be increased more efficiently by increasing SOA gain than by increasing driver swing. In fact, the FOM curves show that it is most efficient to raise the SOA gain to 11 dB before raising the driver swing above 1 Vppd, and again up to 15 dB before raising the driver swing past 2 Vppd.

This reasoning can be extended to form a continuous set of operating points where $FOM_{driver} = FOM_{SOA}$, yielding optimal link performance per watt. This equal-FOM curve is plotted in Fig. 3.5(b), along with a shaded contour map showing total driver and SOA power consumption and contour lines showing supported ULBs for each operating point. The equal-FOM operating points indeed achieve the minimum power consumption for each desired ULB. This theoretical analysis agrees well with time-domain simulation results for each of the link architectures reported above. The equal-FOM curve for an ACD-based link with and SOA in position #1 was normalized to the link receiver sensitivity and is shown in Fig. 3.5(c) alongside corresponding simulation results for power consumption vs. supported ULB for different driver voltages. This Equal-FOM analysis accurately describes optimally power efficient driver and SOA operating points, including SOA saturation effects.

3.5 Architectural Comparisons

The results reported above show that integrated optical amplification in various configurations can improve short-reach coherent link power consumption, but the analysis has been confined to the power consumption changes in the drivers and SOAs alone. We will now consider the power consumption of the full link in order to compare the performance across various ACD- and DSP-based short-reach coherent links.

The estimated power consumption of all of the components of a short-reach coherent link, namely the lasers, thermo-electric coolers (TECs), transimpedance amplifiers (TIAs), biasing components, and DSP/CDR (clock data recovery) chips are shown in Table 3.2 for ACD-based and DSP-based links for two ULB cases. The numbers reported here do not consider any power supply overhead, which can be on the order of 10%. Driver and SOA power consumption was taken from Fig. 3.3, assuming SOAs in

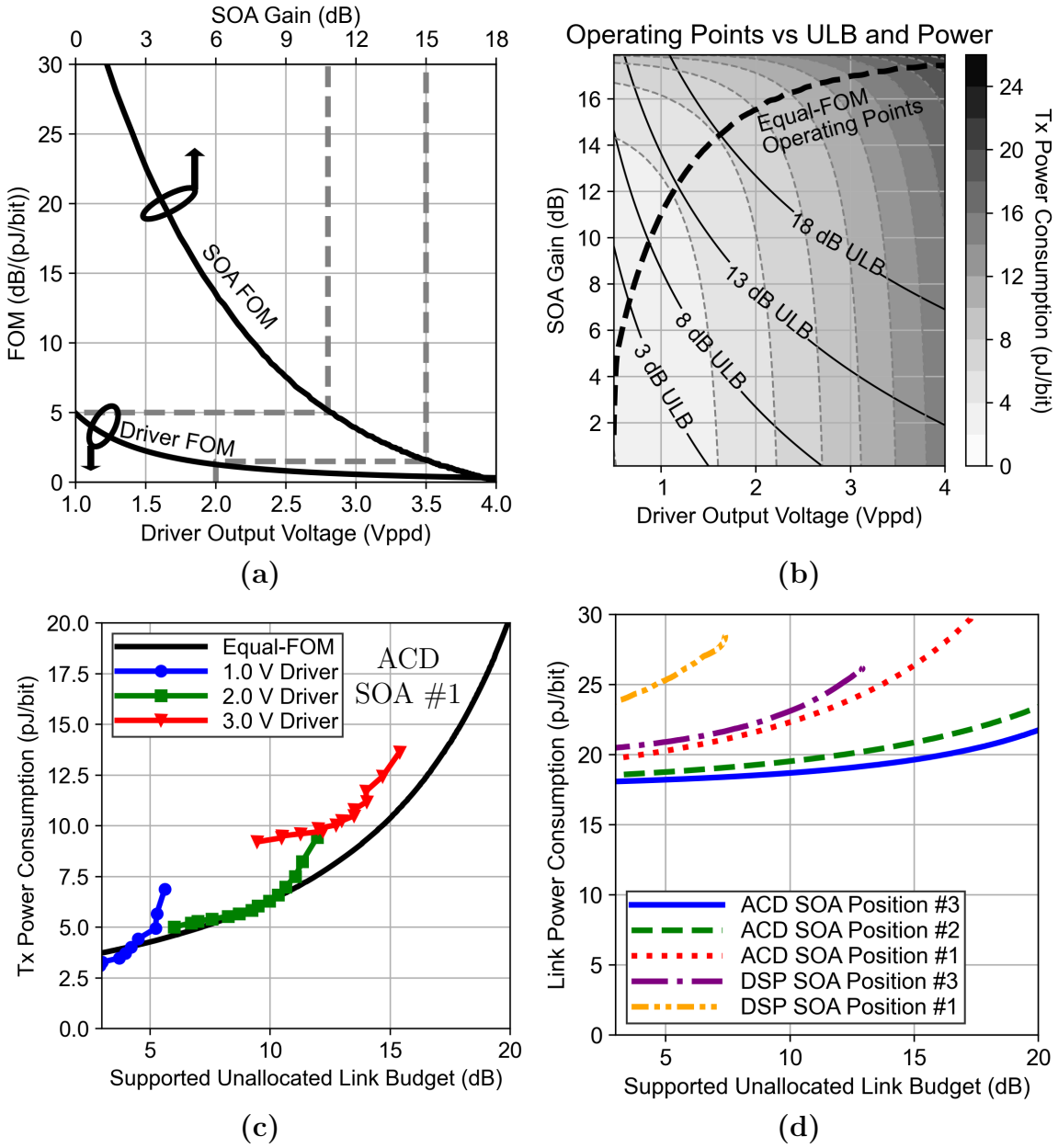


Figure 3.5: Driver and SOA FOMs vs output voltage and gain operating points (a). Optimal equal-FOM operating points plotted with Tx power consumption and ULB contours for an ACD-based link with SOA in position #2 (b). Equal-FOM curve for an ACD-based link with SOA in position #1 vs. time-domain simulation results (c). Calculated full-link power consumption vs. ULB for multiple architectures (d).

position #3. The DSP ASIC power consumption for the DSP-based coherent link is estimated from 400ZR DSP performance [6] scaled from 7 nm CMOS to 3 nm. DSP ASICs

Component	ACD-Based Link		DSP-Based Link	
ULB	3 dB	13 dB	3 dB	13 dB
Drivers + SOAs	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	8.5 pJ/bit
Lasers (with cooling)	6.5 pJ/bit		6 pJ/bit	
TIAs	1 pJ/bit		1.5 pJ/bit	
OPLL	1.5 pJ/bit		0 pJ/bit	
Biasing	2 pJ/bit		1 pJ/bit	
DSP/CDR	5 pJ/bit		10 pJ/bit	
Total	18.5 pJ/bit	19 pJ/bit	21 pJ/bit	27 pJ/bit

Table 3.2: Full-link power consumption tabulation for short-reach coherent links.

specifically tailored for short-reach applications could further improve power consumption substantially by removing CD and PMD compensation and optimizing equalizer implementations [14]. Since the ACD architecture employs limiting drivers and receivers and does not require polarization recovery or carrier recovery in DSP, power-hungry ADCs and digital-to-analog converters (DACs) can be eliminated and a greatly simplified CDR circuit can be used. Since such an ASIC tailored to ACD-based links does not yet exist, we estimate that it will consume half the power of a conventional coherent DSP chip. As coherent DSPs scale to future CMOS nodes, DSP-based links will have more attractive power consumption, albeit with higher ASIC development costs. DSP-based 16QAM links also require half the quantity of lasers, modulators, and receivers as an ACD-based QPSK link with the same overall data rate, leading to cost and size advantages. Full-link power consumption for several link architectures, calculated from optimal equal-FOM operating points derived in Section 3.4, and including the static contributions in Table 3.2, are shown in Fig. 3.5(d). An ACD-based coherent link can improve power consumption by 2.5 and 8 pJ/bit over a DSP-based coherent link for 3 and 13 dB ULB, respectively.

Considering the power consumption of the transceivers themselves, however, does not capture their full impact on data center energy efficiency. The introduction of AWGRs or optical switches has the potential to reduce data center latency, and enable network

topologies that can increase server utilization in high performance computing (HPC) and artificial intelligence (AI) clusters, and in the data center overall. These changes, which are only enabled by optical links that support higher link budgets, will directly impact overall data center efficiency. Networks with optical switching save power by reducing the total number of electrical switches and optical transceivers needed in the data center, directly improving effective transceiver energy efficiency by $> 2X$ [1]. In addition, the network reconfiguration potential of optical switching is still being explored, but efficiency improvements of $> 2X$ for the *overall* data center have been projected [3]. It is clear that modest increases in server utilization can lead to data center power savings greater than the total power consumption of all of the optical transceivers. Thus, optical transceivers that consume more power, but support ULBs that enable optical switching, could still bring about a more efficient overall data center.

As we have seen in Section 3.4, SOAs are a key enabler of efficient link operation with large ULBs. Links with SOAs in positions #2 and #3 supported higher ULBs than those with an SOA in position #1, despite any ISI penalties due to the SOA pattern effect and NLPN. Furthermore, ACD-based QPSK links are able to support higher ULBs than their DSP-based 16QAM counterparts, in part due to receiver sensitivity and SNR requirements [8], but also in part due to decreased susceptibility of QPSK signals to SOA NLPN. DSP-based SOA NLPN compensation algorithms exist, but come at the expense of additional DSP power consumption and complexity [31].

3.6 Conclusion

As per-wavelength data rate requirements for short-reach optical interconnects rise, coherent links will become an attractive option for intra-data center applications. The stringent power consumption and cost constraints placed on intra-data center links will

require an evolution of conventional coherent link architectures and designs. SOAs integrated with coherent PICs enable link operation with reduced driver output voltages, supporting larger link budgets with reduced power consumption. Positioning SOAs after the Tx modulator results in the most improved link performance, with simulated power savings of 6 pJ/bit shown for a 13 dB ULB. Figures of merit for driver and SOA link budget improvement per additional unit of power consumption were proposed and used to derive optimal driver and SOA operating points. For typical operating points, SOAs are more energy-efficient than drivers at increasing the link budget.

While DSP-based coherent architectures using 16QAM modulation benefit from SOA gain, their performance is hampered by SOA NLPN. Due to its quasi-constant power envelope, QPSK-based modulation is more tolerant to SOA saturation effects, making ACD-based coherent links that use power-efficient limiting drivers and TIAs especially attractive for short-reach coherent links with large ULBs. Since optical amplification can efficiently increase the supported link budget, it enables the inclusion of AWGRs or optical switches, which can revolutionize data center networks and improve overall server utilization and energy efficiency. Integrated optical amplification is the key to meeting link performance and energy efficiency targets for intra-data center coherent optical interconnects.

Chapter 4

High-Speed PCB Packaging Platform

This chapter describes work originally published in [52].

4.1 Introduction

The demand for additional network bandwidth in data centers is ever-increasing. In order to meet transceiver datarate targets, designers of future generations of intra-datacenter optical interconnects will need to add additional optical lanes, use more spectrally efficient modulation formats, and increase optical baudrates. Increasing baudrates from 50 Gbaud to 100 Gbaud will require increased component bandwidths for both optical and electrical transceiver components, and careful transceiver packaging design to maintain radio frequency (RF) signal integrity, while at the same time maintaining good power efficiency and low cost.

A low-cost printed circuit board (PCB) packaging platform for testing optoelectronic devices beyond 100 Gbaud will be presented here. The platform is flexible, and can be

used to test standalone transmitter and receiver electronic integrated circuits, as well as copackaged assemblies that include photonic integrated circuits or components. The platform is based on an FR-4 PCB with wirebonded connections for high speed signals on-chip, which lowers cost and assembly effort compared to more specialized PCB materials and flip-chip bonding alternatives. A similar PCB packaging platform has previously been used to demonstrate high baudrate [37] and high density [38] optical links. The platform presented here platform was used to perform the high speed measurements reported in [39–41]. The high baudrate testing enabled by this platform will be crucial for developing the high speed photonic and electronic integrated circuits (ICs) that will make possible future generations of optical interconnects, and it can also inform the design of the module packaging for 100+ Gbaud intra-datacenter transceivers.

Section 4.2 will present an overview of the various aspects of the PCB packaging platform. Section 4.3 will detail the design, optimization, and performance of the high speed signal path. High speed time-domain measurement results achieved using this packaging platform will be shown in Section 4.4. Finally, concluding remarks will be made in Section 4.5.

4.2 Platform Overview

This flexible platform can support packaging and testing of multiple different types and configurations of electronic ICs (EICs) and photonic ICs (PICs), and some representative example configurations will be shown. One example of a fully assembled PCB supporting a single channel high speed photoreceiver is shown in Fig. 4.1, with the locations of the IC, photonic components, and connectors highlighted.

4.2.1 High Speed Signals

In this platform, wirebonds are used to deliver high speed signals to and from the chips. Assemblies are carefully designed to limit RF wirebond length and thus maintain an acceptable amount of parasitic inductance. Fig. 4.2 shows closeup views of two wirebonded assemblies with electronic ICs copackaged with photonic components, in

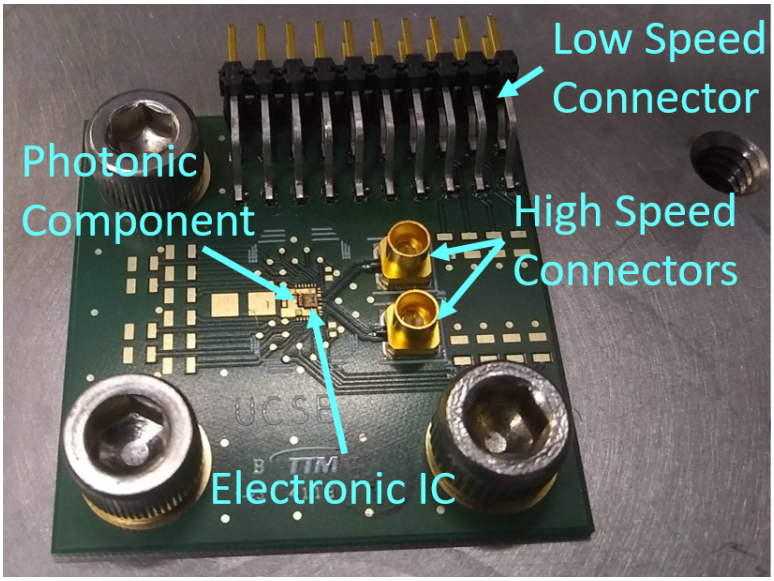
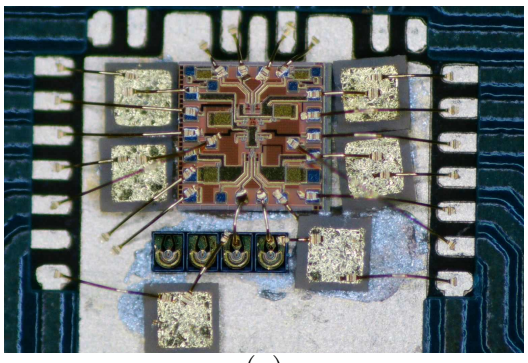
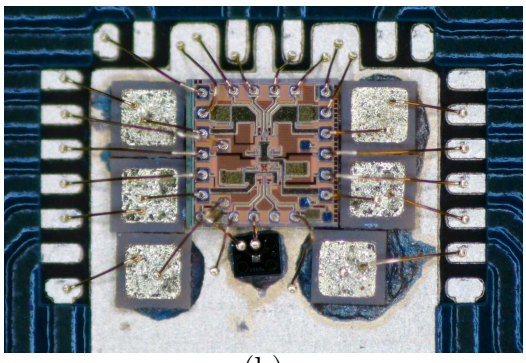


Figure 4.1: An example optoelectronic assembly on an FR-4 PCB.



(a)



(b)

Figure 4.2: Example optoelectronic assemblies, zoomed to show wirebonding detail. (a) Transmitter assembly including copackaged electronic driver IC, VCSEL array, and surface mount decoupling capacitors. (b) Receiver assembly including copackaged electronic TIA, vertically incident photodiode, and surface mount decoupling capacitors.

which the RF wirebonds at the tops and bottoms of the ICs are as made as short as possible given the assembly spacing constraints. For reference, the electronic ICs (EICs) in Fig. 4.2 are 1 mm $\times$ 1 mm.

Microstrip lines route the high speed signals across the PCB. Since FR-4 PCB material is used, the RF losses of the microstrip lines are dominated by the dielectric losses, and can be quite high. However, by minimizing the on-board microstrip trace length, these losses can be reduced so much that they no longer dominate the RF losses of the full packaging platform. In order to prevent crosstalk, the microstrip ground plane separates and isolates the RF microstrip traces, which are located in the top metal layer, from the other DC traces, which are routed in lower metal layers. Vias also provide ground plane stitching around the RF traces to further reduce crosstalk and maintain signal integrity.

The high speed signals are brought on and off the PCB through Mini-SMP connectors (Rosenberger 18S102-40ML5). The design, optimization, and measurement showing a 60 GHz bandwidth of the connector and optimized on-board launch structure will be presented in detail in Section 4.3. Once brought off the PCB, coaxial cables deliver the high speed signals to and from the test equipment. For high speed time domain testing, the coaxial cables introduce losses that cannot be calibrated out, making it crucial to minimize their lengths as well, ideally to $\leq$ 4in per cable. Carefully managing RF signal integrity in all of these parts of the PCB packaging platform is critical for enabling high baudrate testing.

4.2.2 Low Speed Signals

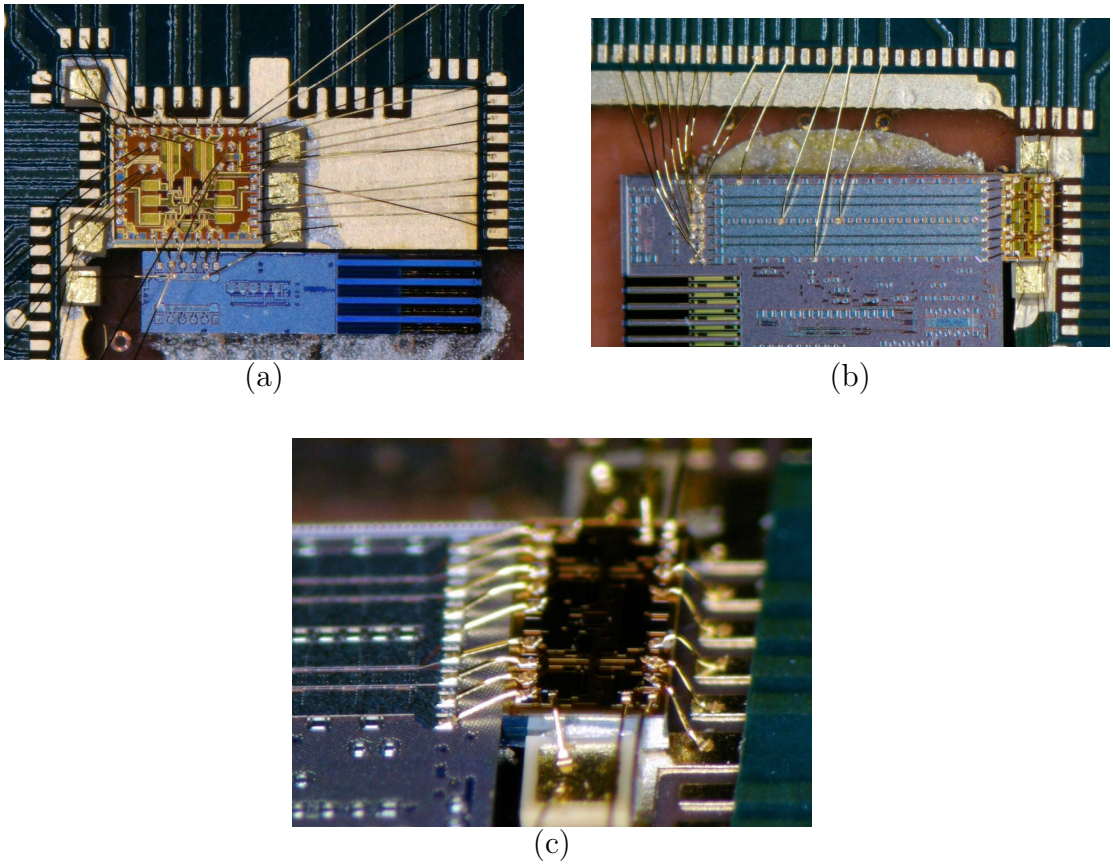
The power distribution and low-speed signalling capabilities of the package are also critical for high speed testing of electronic and photonic integrated circuits. In this platform, low speed signals, once bonded out of the EICs and PICs, are brought to a standard

header for interfacing with a variety of test equipment. To the extent possible, supplies and DC signals are decoupled directly on electrical ICs with integrated capacitors. However, since on-chip decoupling is space limited and can be inadequate for critical supplies, surface mounted wirebondable capacitors are mounted directly adjacent to the device under test, as shown in Fig. 4.2. The close location of the decoupling capacitor to the IC is crucial to minimize parasitic wirebond inductance that would degrade noise performance. If required, larger surface mount capacitors can also be placed further away on the PCB to provide additional decoupling.

4.2.3 Optical Assembly

This packaging platform is compatible with a wide variety of optical devices for co-packaging. Vertically incident optical devices, such as discrete photodiodes, vertical cavity surface emitting lasers (VCSELs), or vertically coupled PICs, can easily be packaged and fiber-coupled by aligning a fiber vertically above the chip. Edge coupled PICs are also supported, provided there is clearance for the fiber above the PCB. If this is not the case, special care needs to be taken to design for vertical shimming or milling of the PCB to provide clearance.

Fig. 4.3(a) shows an example receiver assembly including a coherent receiver PIC and a receiver IC. Another assembly with a driver IC and a coherent transmitter PIC containing a Mach-Zehnder modulator (MZM) is shown in Fig. 4.3(b). The PICs were fabricated in the GlobalFoundries 9WG silicon photonic process, and the EICs were fabricated in the GlobalFoundries 8XP process. In both of these assemblies, a section of the PCB under the PIC was milled away in order to match the chip height of the 250 μm thick EICs with the 750 μm thick PICs to within $\pm$50 μm. This is critical for minimizing the length of the EIC-to-PIC RF wirebonds, which are shown in detail in Fig. 4.3(c).



(a) (b)

(c)

Figure 4.3: Example optoelectronic assemblies, consisting of a silicon photonic receiver PIC with edge coupling copackaged with a receiver IC (a), and a driver IC copackaged with a silicon photonic transmitter PIC with edge coupling (b). The PCBs have been milled to accommodate different chip thicknesses. (c) A zoomed view of the transmitter assembly showing critical wirebonds between the EIC and PIC.

A critical consideration for maintaining the performance of many photonic devices, and especially integrated semiconductor diode lasers, is effective thermal management and heat sinking. In this platform, copper vias directly underneath the photonic and electronic ICs provide a low thermal impedance path for heat sinking. The PCB can also be mounted on a thermoelectric cooler (TEC) for further thermal management. In the case of the assemblies shown in Fig. 4.3, the thermally conductive epoxy and the copper thru-vias ensure that the PIC is well heat-sunk, even when the top metal layer has been milled away.

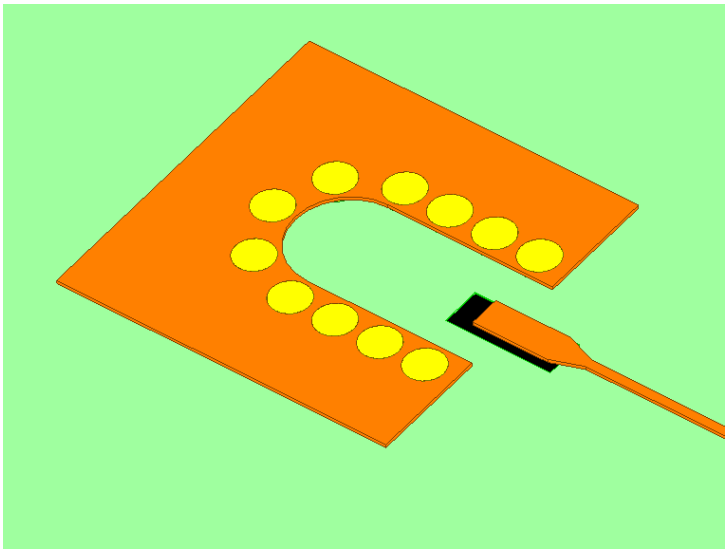


Figure 4.4: The simulation model of the high speed connector launch structure, with the ground plane cutout shown in black.

4.3 High Speed Design

The transition from the PCB microstrip line, to surface mounted Mini-SMP connector, to RF cable, is a critical point in the high speed signal path, and requires proper design to ensure minimal RF reflections and high bandwidth. Specifically, as noted in [38], the surface mounted RF connector creates additional capacitance at the PCB interface, causing the signal to no longer be in a 50 Ω environment. To counteract this effect, a portion of the ground plane directly below the RF connector was removed. Fig. 4.4 shows the simulation model of the connector launch structure geometry, with the ground plane cutout shown in black. The particular geometry of the launch structure with the removed ground plane was optimized in simulation using Ansys HFSS, and then further optimized by measuring the performance of various connector launch structures with skewed parameters.

The time domain reflectometry (TDR) impedance of the optimized second generation connector launch structure, measured with a 50 GHz TDR sampling module (Tektronix

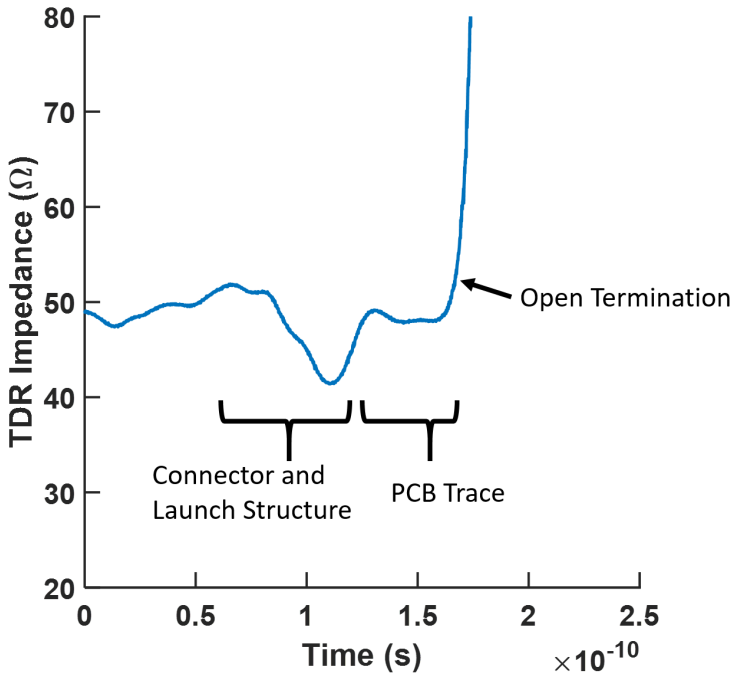


Figure 4.5: Measured TDR Impedance for the high speed connector launch structure. Sections of the TDR trace are labelled with their corresponding physical structures.

80E10B), is shown in Fig. 4.5. The TDR measurement time can be mapped to physical distance in the device under test using the microwave index in each region, and thus the approximate locations of the PCB features have been labelled. The TDR impedance remains between 41 and 52 Ω throughout the entire connector launch structure. In addition to TDR characterization, simple microstrip structures with identical RF connector launch structures at both the input and output were also measured on a vector network analyzer (VNA). The extracted insertion loss and measured return loss of the optimized connector launch structure are shown in Fig. 4.6. The optimized structure has a 3 dB bandwidth of 60 GHz, as well as < 10 dB of return loss below 55 GHz.

The frequency dependent insertion loss of the PCB microstrip line and the RF coaxial cables were also extracted from the VNA measurements, and are shown, along with the connector launch structure loss and the calculated cascaded loss of a complete high speed

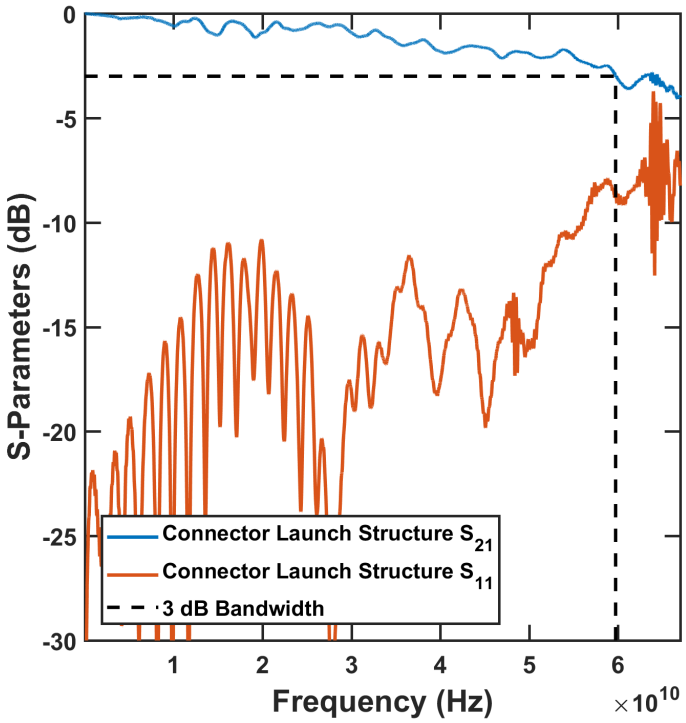


Figure 4.6: Return loss and extracted insertion loss from S-parameter measurement of the fabricated high speed connector launch structure.

path, in Fig. 4.7. Since low-cost FR-4 material was used for the PCB, the microstrip line can account for the highest RF losses in the entire packaging system if the traces are long. Thus, it is critical to minimize the length of the high speed traces on the PCB. For single differential input or differential output assemblies, such as the assembly in Fig. 4.1, we have reduced the microstrip length to just 5 mm, so that it no longer dominates the RF losses. Packaging chips that require large numbers of high speed traces requires careful design to keep trace lengths low and losses acceptable, and may eventually warrant a lower loss, albeit more expensive, PCB material choice.

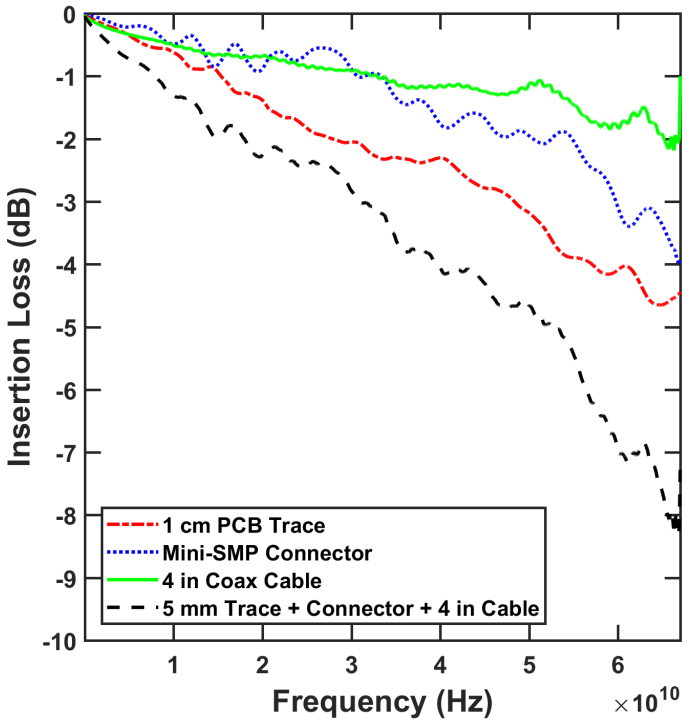


Figure 4.7: Insertion losses extracted from S-parameter measurements for the PCB microstrip line, high speed connector launch structure, RF cables, and a cascaded high speed path. The curves have been smoothed to remove some measurement noise.

4.4 Experimental Demonstration

In this section, two demonstrations of high speed device and system measurement using this packaging platform will be shown. The first is a full optical link based on a vertical cavity surface emitting laser (VCSEL), which uses separate single channel transmitter and receiver PCB assemblies, and the second is an all-electrical measurement of a packaged transimpedance amplifier (TIA).

4.4.1 Optical Link Characterization

The packaged transmitter and receiver assemblies shown in Fig. 4.2(a) and Fig. 4.2(b), respectively, were used to operate a full VCSEL-based optical link. The TIA

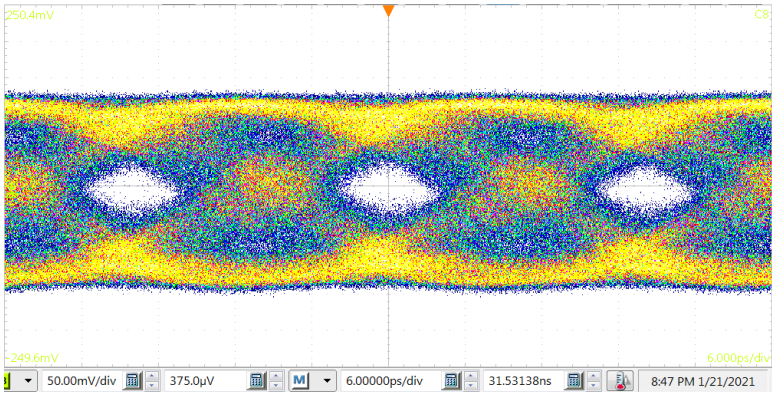


Figure 4.8: Measured 50 Gbps electrical eye diagram at the receiver output for full VCSEL-based optical link operation using this packaging platform.

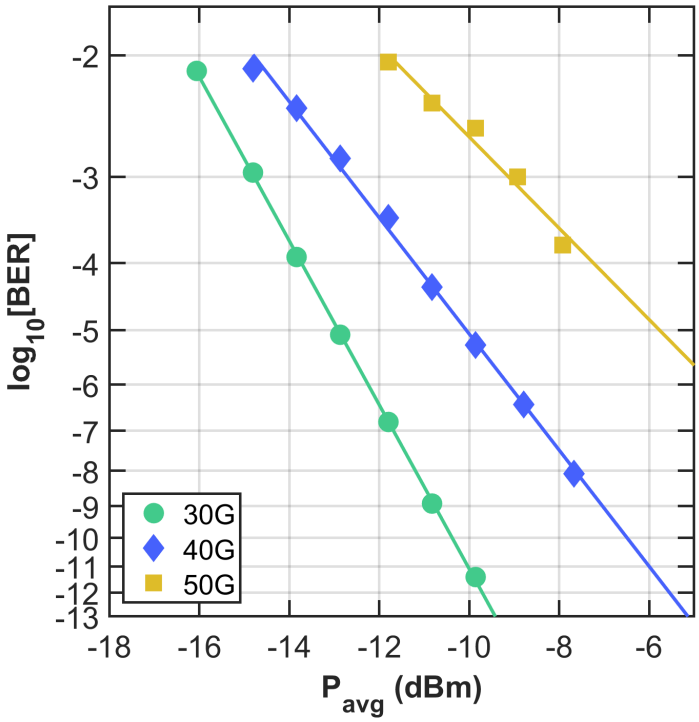


Figure 4.9: Measured bit error rate vs average optical received power (assuming infinite extinction ratio) for the full VCSEL-based optical link operating at 30, 40, and 50 Gbps

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circuit that was used is described in [41]. The link was characterized with a bit pattern generator (SHF 12104A) at the Tx input, and a digital sampling oscilloscope (Tektronix DSA8300) with a 70 GHz sampling module (Tektronix 80E11) at the Rx output. Fig.

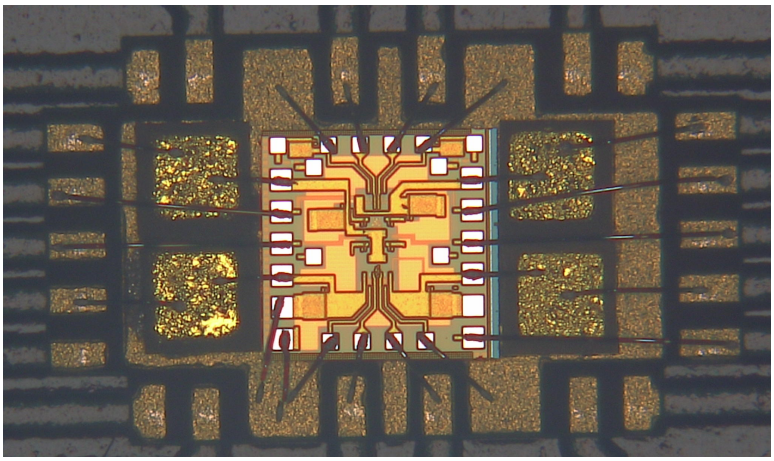


Figure 4.10: Fully electrical TIA assembly.

4.8 shows the measured 50 Gbps non-return-to-zero (NRZ) eye at the Rx output for full link operation. Bit error rate (BER) sensitivity curves were measured with a bit error rate tester (BERT) (SHF 11104A) at the Rx output, and are shown in Fig. 4.9.

This result includes all of the bandwidth limitations from a cascade of the two separate Tx and Rx PCBs, including the wirebonds, microstrip lines, connectors, cables, driver and receiver circuits, and the VCSEL and photodiode. Notably, the VCSEL bandwidth on its own is 26 GHz. Despite these limitations, an open eye was measured at 50 Gbps. Additionally, there is no indication of a BER floor at 50 Gbps, meaning that the amount of received optical power, not just the available bandwidth was limiting the link performance.

4.4.2 Electrical TIA Characterization

The same TIA chip used in the above optical link was also characterized in an electrical input and electrical output environment using this packaging platform. The packaged device is shown in Fig. 4.10. The time domain characterization was carried out with the same bit pattern generator and sampling oscilloscope module as above, but with the

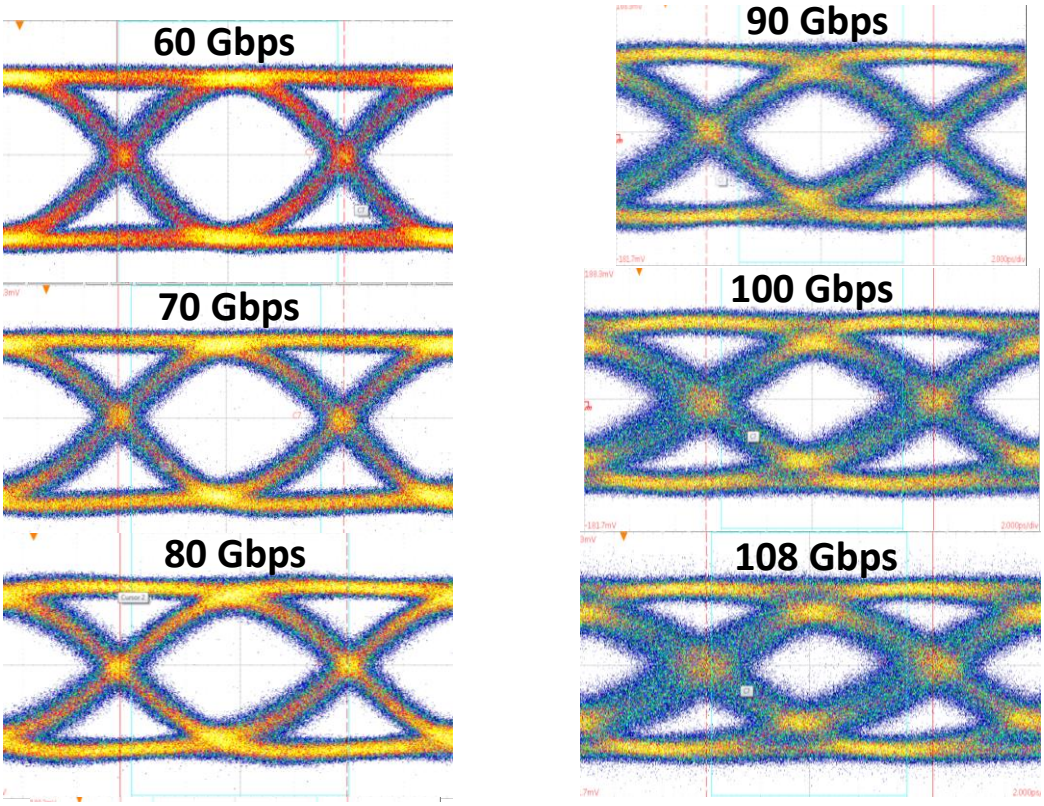


Figure 4.11: Measured single-ended eye diagrams from 60 to 108 Gbps for the fully electrical TIA assembly.

addition of a multiplexer (SHF 603A) at the Tx input to allow for NRZ signal generation above 64 Gbps. For BER measurements, a demultiplexer (SHF 623A) was inserted at the Rx output before the BERT. Electrical eye diagrams showing open eyes from 60 to 108 Gbps measured through the packaged device are shown in Fig. 4.11. Measurements showing BER $< 10^{-11}$ though this assembly were collected up to 96 Gbps. Higher datarate BER measurements were limited by the test setup clock distribution. More details of this measurement are presented in [41].

This measurement demonstrates that this FR-4 PCB packaging platform is capable of supporting device testing at speeds $>$ 100 Gbaud. Since this chip is targeted for links with either either NRZ or quadrature phase shift keying (QPSK) modulation with an optical phase-locked loop (OPLL), as described in [8], the receiver chain has variable

gain amplifier stages that limit the signal at high gain setting and effectively make a bit decision directly on chip. In cases like this, the EIC output stage can incorporate equalization that is designed to compensate for RF losses in the packaging and testing environment. For this TIA, a continuous-time linear equalizer (CTLE) circuit was included in the output stage. The equalized TIA output has 4 dB of peaking at 40 GHz, which helps to compensate for the expected packaging losses that were shown in Fig. 4.7. The CTLE has a relatively small impact on the overall device efficiency. The full TIA power efficiency was 1.5 pJ/bit, of which 0.3 pJ/bit is used in the output stage.

4.5 Conclusion

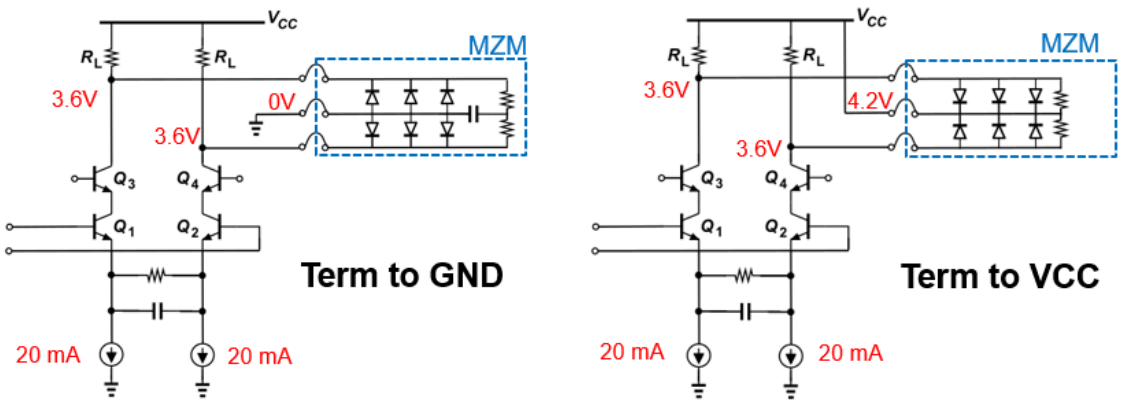
An FR-4 PCB packaging platform for testing of copackaged optoelectronic devices at speeds up to and beyond 100 Gbaud has been presented. Design and optimization of the RF performance of the various parts of the packaging system, and crucially the RF traces and high speed connector launch structure, was also described. This PCB packaging platform enables high baudrate testing that will be crucial for designing future generations of optical interconnects, and could also inform the packaging design for high baudrate, low cost intra-datacenter optical transceivers.

Chapter 5

Low-Power Travelling Wave Modulators and Drivers

5.1 Introduction

As demand for higher datarate intra-data center optical links grows, improved performance constraints will be placed on optoelectronic transmitters. A tradeoff inherent to travelling-wave Mach-Zehnder modulators (TW-MZMs) is that reducing their length increases bandwidth, but decreases modulation efficiency, making it difficult to improve overall system throughput of future optical links. Furthermore, as discussed in Chapter 2 and Chapter 3, the driver power consumption is a driving factor in overall link energy efficiency. Thus, this chapter will describe design methodologies and present measurement results for low-power travelling wave modulators and their associated drivers.



(a) (b)

Figure 5.1: Schematic of output stage of (a) Term-to-GND and (b) Term-to-VCC driver and MZM architectures. Nominal bias currents and voltages are shown.

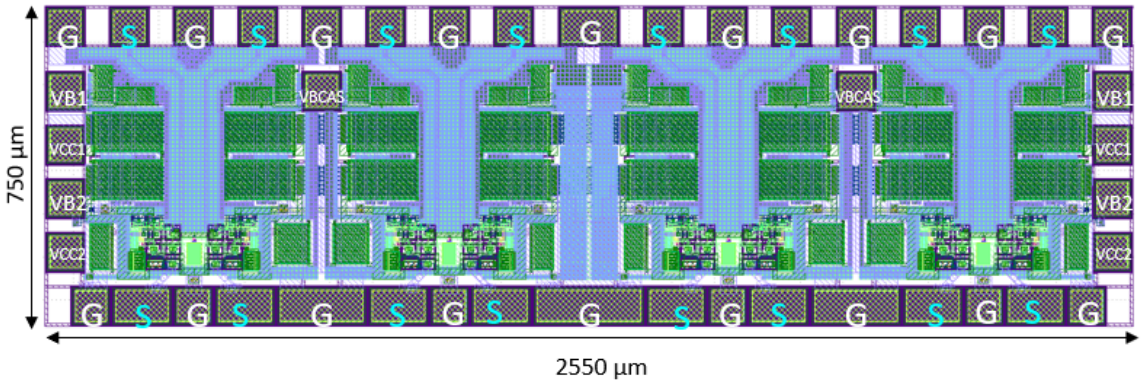


Figure 5.2: 4-channel driver chip layout, with pad functions enumerated.

5.2 Low-Power Modulator Drivers

Based on the full-link analysis and optimization carried out in Chapter 3, it is clear that an optimized ACD-based link's driver swing will be much lower than that of a conventional coherent link. A series of drivers were designed in the GlobalFoundries 9HP and 9HP+ 90 nm SiGe BiCMOS process, with a target of 2.0 Vppd output swing into a TW-MZM with 30Ω characteristic impedance. Simple NRZ modulation at this reduced swing, relative to highly linear modulation at swings closer to 4 Vppd for more conventional coherent drivers allows these designs to consume only 250 mW and 270 mW

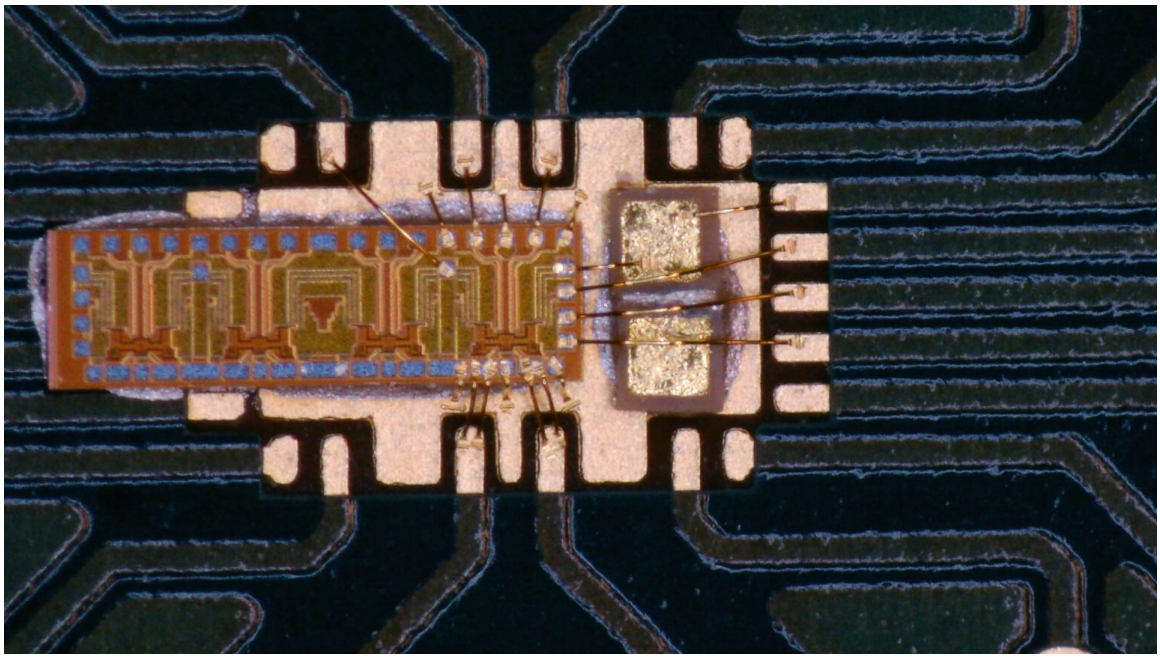
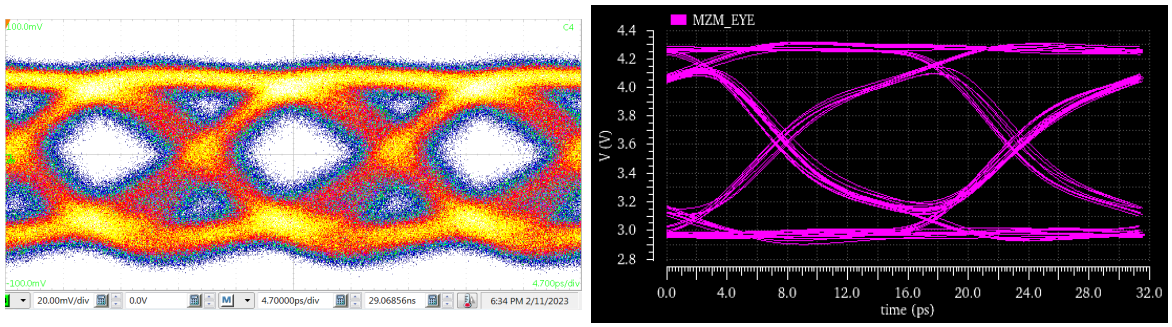


Figure 5.3: Chip micrograph of a 4-channel driver configured for single-channel electrical testing.

per channel for the 9HP and 9HP+ designs, respectively. The driver circuits consisted of an emiter-follower input stage followed by a cascode differential pair amplifier output stage with CTLE for peaking, and were designed to integrate with the TW-MZM through wirebonds.

Schematics of the two different driver and MZM configurations are shown in Fig. 5.1. The two termination configurations are intended to interface with different MZMs. the Term-to-GND driver design modulates the MZM phase shifter cathodes, and provides a high ($\approx$ 4 V) junction reverse bias, since the MZM phase shifter anode is tied to GND. This design includes a DC differential termination, which is decoupled to ground with a capacitor to avoid unnecessary current draw. Alternatively, the Term-to-VCC driver modulates the MZM phase shifter anodes, and provides a lower ($\approx$ 0.6 V) junction reverse bias, since the MZM phase shifter cathode is tied to V_{CC}. The Term-to-VCC design is purely DC terminated. Both of these architectures can have comparable power



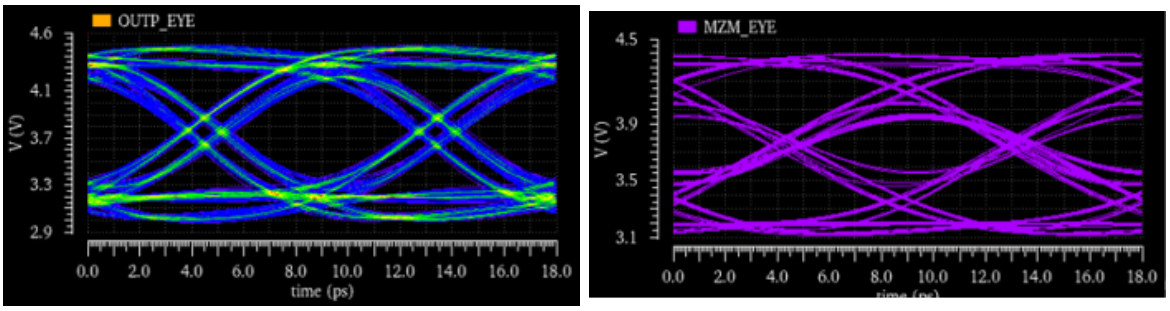
(a) (b)

Figure 5.4: (a) Measured 64 Gbaud NRZ eye diagram of a packaged driver in all–electrical testing. (b) Corresponding simulated eye diagram of driver in all-electrical test-bed, for reference.

consumption, but performance depends on the TW-MZM phase efficiency and BW, which both depend on the phase shifter design and junction bias. Thus, different MZMs are suited to one or the other driver configuration.

In both cases, power consumption is traded off for ISI tolerance by designing the driver output stage load resistor. Conventional drivers typically use an open-collector ($R_L = \infty$) design, sourcing all of the bias current for the driver output stage through the MZM termination for optimal power efficiency. This, however, results in increased susceptibility to second order reflections as the electrical signal propagates along the TW-MZM, which need to be compensated for with DSP-based equalization. For these low-power drivers designed for ACD, a quasi-open collector design was employed, where R_L is chosen to be large, but not infinite. This causes some of the bias current to be sourced through R_L, and reduces energy efficiency. But, ISI improves significantly, and external equalization is not necessary for link operation. Through transistor-level co-simulation of reflections and link performance with frequency-dependent input impedance models of candidate modulators, a value of $R_L = 200\ \Omega$ was selected. This quasi-open collector design is described further in [34].

An image of the 4-channel driver layout, capable of driving a full DP-IQ-MZM, is



(a) (b)

Figure 5.5: (a) Simulated 112 Gbaud NRZ eye diagram of the driver voltage signal when integrated with a 40 Ω TW-MZM. (b) Corresponding simulated 112 Gbaud eye diagram of the optical output signal, assuming 45 GHz TW-MZM EO BW.

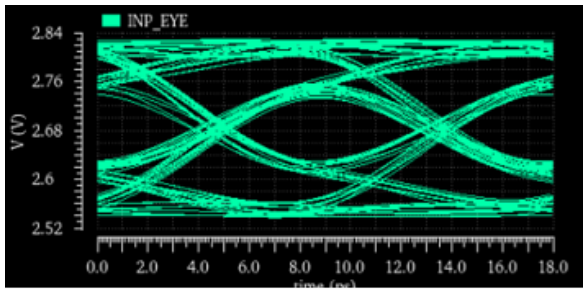


Figure 5.6: Simulated 112 Gbaud NRZ eye diagram of input signal to the driver. Pattern generation and packaging BW limitations contribute significant ISI even before the driver IC itself.

shown in Fig. 5.2, and an image of a driver packaged on a PCB for an all electrical test is shown in Fig. 5.3. A measured all-electrical 64 Gbaud NRZ transmission eye diagram is shown in Fig. 5.4(a). The output swing, measured single-ended and through a 20 dB attenuator, was 2.0 Vppd in a 50 Ω environment. The input to the driver was 400mV from a bit pattern generator (SHF 12105 A), and the output was measured with a 70 GHz electrical sampling module (Tektronix 80E11). As this driver was designed to target 100 Gbaud operation, the per-channel power consumption was an elevated 450 mW.

The full 100 Gbaud performance of the driver must be characterized by integrating it with a high-speed TW-MZM in the future. For the present all-electrical characterization, comparison to simulation results can indicate potential performance. For comparison,

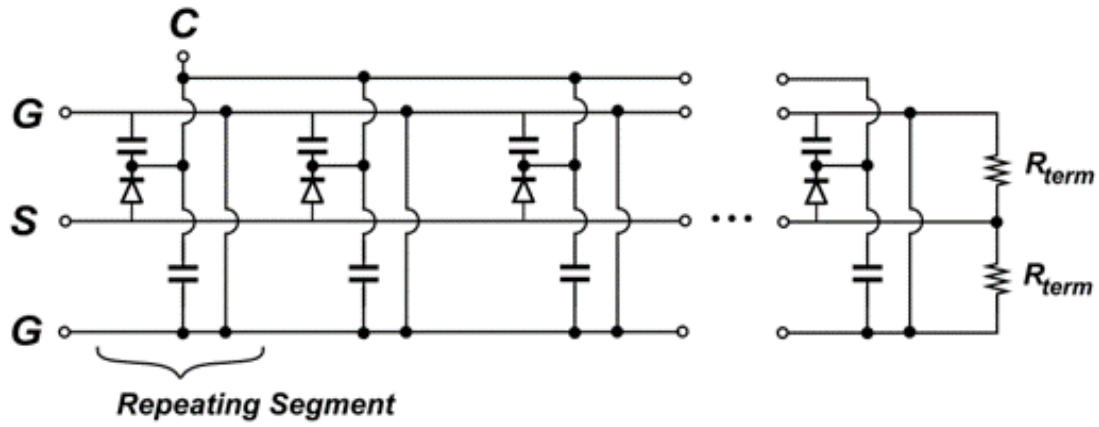


Figure 5.7: Circuit model of one single-ended arm of the 90WG TW-MZM. The cathode bias has distributed decoupling along the travelling wave electrode, and a 50 Ω DC termination is integrated.

the simulated 64 Gbaud output eye is shown is displayed in Fig. 5.4(b), showing good agreement. The simulated performance of the driver+TW-MZM system at 112 Gbaud is shown in Fig. 5.5. Fig. 5.5(a) shows the simulated voltage signal at the driver output, and Fig. 5.5(b) shows the simulated optical signal after accounting for a 45 GHz EO 3 dB BW in the TW-MZM. For completeness, the simulated voltage signal at the input of the driver is shown in Fig.5.6. At such high symbol rates, pattern generation and packaging BW limitations degrade the input signal substantially before arriving at the driver. As indicated by these validated simulations, this driver has potential for use in 100 Gbaud links.

5.3 Silicon Photonic Travelling Wave Modulators

Multiple generations of silicon photonic TW-MZMs were designed and fabricated in the GlobalFoundries 90WG and 45CLO silicon photonics processes, as well as Intel's silicon photonics process. These devices were designed to take advantage of the unique capabilities of these silicon photonic processes and include integrated termination and

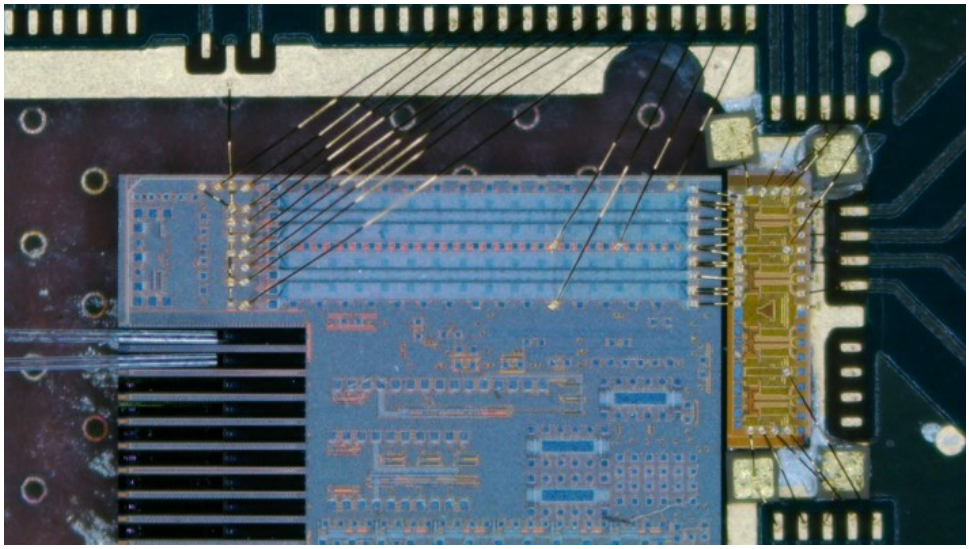


Figure 5.8: The assembled and wirebonded 90WG TW-MZM and 9HP driver. Edge–coupled input and output fibers are shown on the left.

capacitive decoupling structures to improve performance. Further details regarding modulator simulation and design optimization are included in Appendix A.

Fig 5.7 shows a schematic of one single-ended arm of a TW-MZM designed and fabricated in GlobalFoundries 90WG. The diodes represent 100 μm long phase shifter segments, of which there are a total of 30 in the modulator with loading factor of 75%, for a total phase shifter length of 3 mm per arm. The cathode of each segment is decoupled to ground, and controlled with an external supply to set the junction bias. Without this decoupling, the junction bias would be inextricably linked to the DC supply and biasing configuration of the combined driver and TW-MZM system. This distributed decoupling, however, enables independent control of the junction bias, enabling flexibility in optimizing both driver and TW-MZM performance. The decoupling capacitance is designed to be much larger than the capacitance of each of the corresponding phase shifter segments, so that it minimally interferes with the TW-MZM transmission line performance. Integrated resistors for a 50 Ω termination are also included on the chip, which is designed to be compatible with a Term-to-VCC driver, as in Fig. 5.1(b).

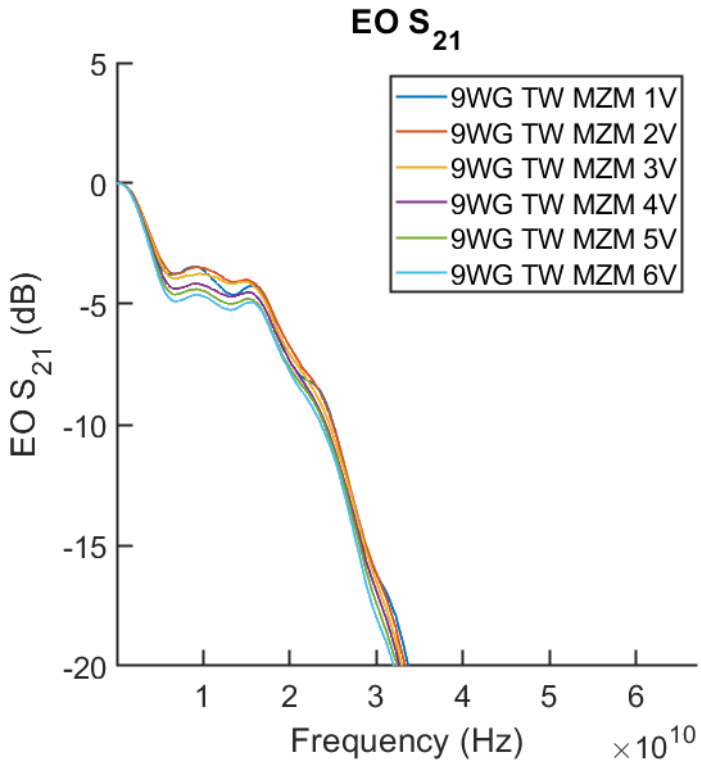


Figure 5.9: EO S_{21} of the 90WG TW-MZM assembled with driver for various junction bias voltages.

Fig. 5.8 shows an assembled IQ TW-MZM co-packaged with a Term-to-VCC driver fabricated in GlobalFoundries 9HP. The design and performance of this driver will be discussed in more detail in Chapter 6. The EO frequency response of the assembled transmitter is shown for different amounts of junction reverse bias in Fig. 5.9. Although, the measured frequency responses of the PCB packaging and coaxial cables have been calibrated out of this plot, a significant low-frequency drop remains present. This is due to a mismatch between the TW-MZM characteristic impedance and the fixed termination resistance, which causes electrical reflections on the modulator. This mismatch could be corrected in future generations, and the EO 3 dB BW of the transmitter is ≈20 GHz, ignoring the low-frequency tail.

A next-generation TW-MZM design was fabricated in GlobalFoundries 45CLO sili-

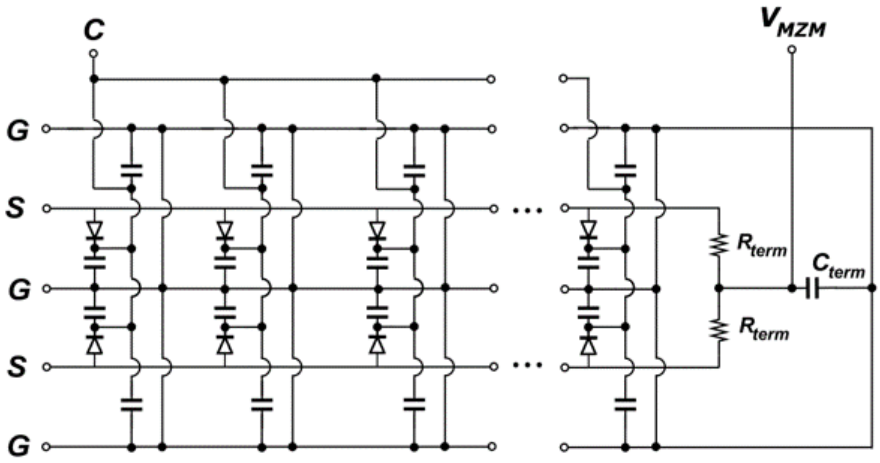


Figure 5.10: Circuit model of the full differential 45CLO TW-MZM. The cathode bias has distributed decoupling along the travelling wave electrode, and variable termination resistances are integrated, with a decoupled bias voltage V_{MZM}.

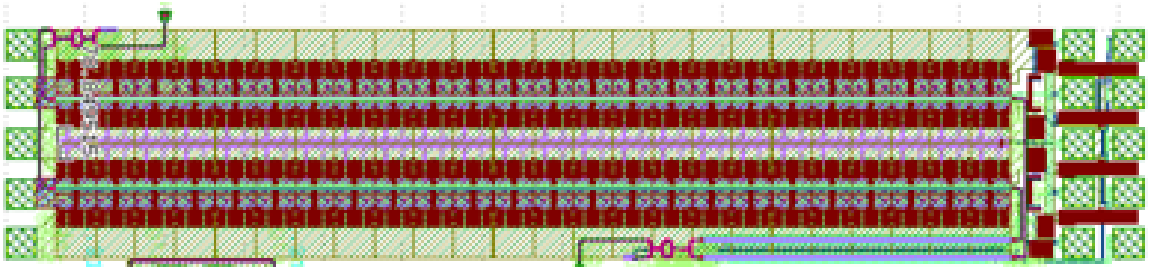


Figure 5.11: Layout view of the 45CLO TW-MZM.

con photonics process. The TW-MZM schematic is shown in Fig. 5.10, and the resulting layout design is shown in Fig. 5.11. The design of this TW-MZM is similar to the previous 90WG design, but except that there is a decoupling capacitor C_{term} that enables an independent supply V_{MZM} at the modulator termination, making this design compatible with a range of potential drivers, including either Term-to-GND or Term-to-VCC designs. Additionally, a series of wirebondable pads allow wirebond connections to alter the termination resistance of the device, giving additional flexibility in performance optimization. This design included fully loaded phase shifters with a total length of 2.4 mm per arm.

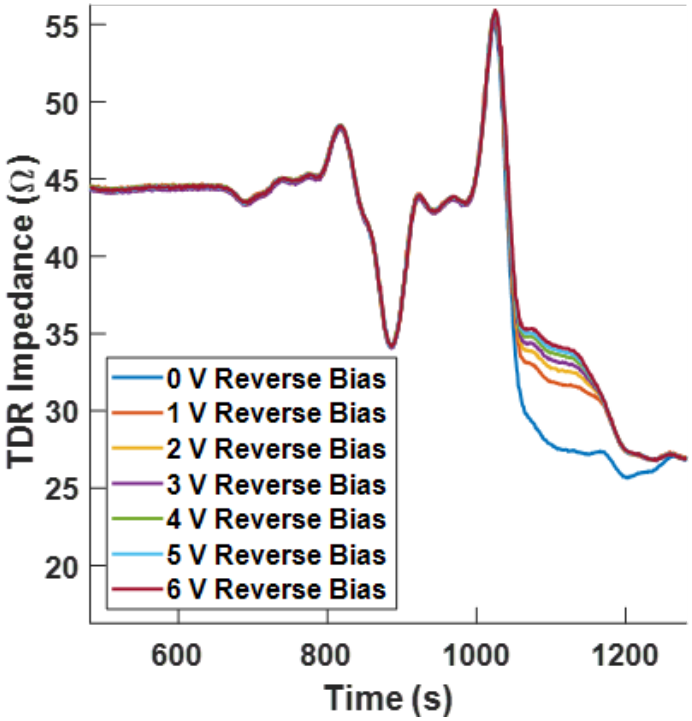


Figure 5.12: Time domain reflectometry (TDR) measurement of the 45CLO TW-MZM with 25 Ω termination setting for various junction bias voltages.

The effect of the variable reverse bias on the TW-MZM transmission line impedance was characterized with time domain reflectometry (TDR), and the results are plotted in Fig. 5.12. The first part of the TDR trace corresponds to packaging components, which are unchanged by reverse bias. The last part of the trace, however, shows the measured impedance of the TW-MZM transmission line itself, which varies from 27-35 Ω as the junction reverse bias varies from 0-6 V. Due to packaging losses and reflections in the TDR measurement, the absolute values of the MZM impedance measured in this way have significant uncertainty, but the general trend they illustrate remains valid.

The measured EO S_{21} of the 45CLO MZM, with packaging parasitics extracted, is shown in Fig. 5.13. Due to inaccurate simulation assumptions for this device, the resulting MZM impedance was lower than expected. This contributed to the sharp roll-off visible in

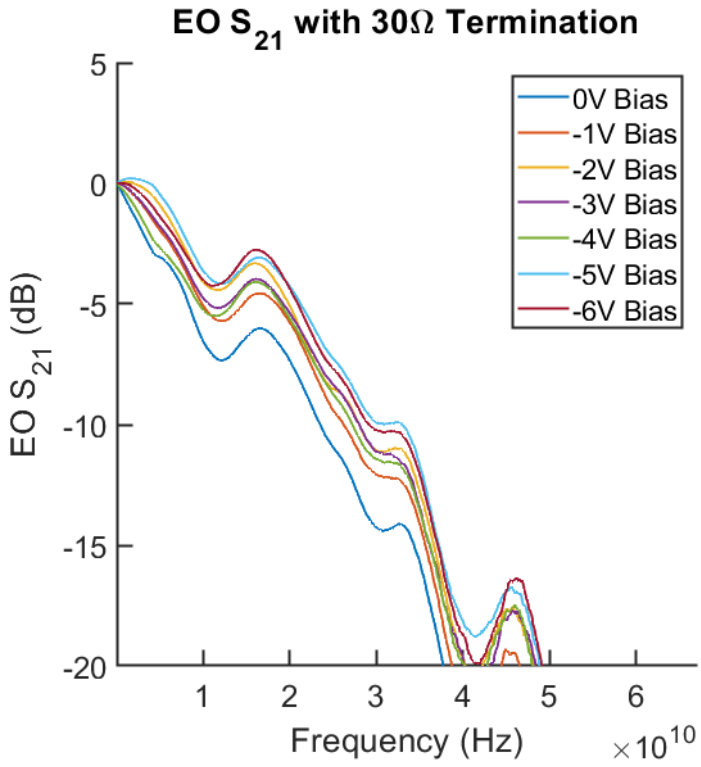
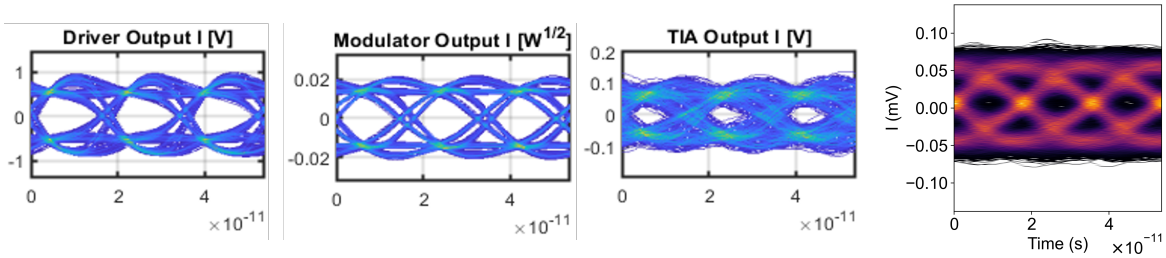


Figure 5.13: EO S_{21} of the 45CLO TW-MZM with 25 Ω termination setting for various junction bias voltages.

the frequency response below 10 GHz. A new design with optimized decoupling structure parasitics is being fabricated to correct this error and support improved performance.

Finally, TW-MZMs were also designed in Intel's silicon photonic process, and will be described in further detail in Chapter 6. As is clear from the above TW-MZM design efforts, great care must be taken to manage impedance mismatches and reflections in the combined driver+MZM system, especially if the driver is an open-collector or quasi-open collector design. To this end, the design process for the Intel TW-MZMs included rigorous co-simulation of the driver and MZM, and the transmitter designs were actually based on optimization of the full link BER sensitivity performance. In order to do this, and crucially to properly simulate the electro-optic effects of reflections between the driver and TW-MZM, an electrical and optical co-simulation was devised. An input impedance



(a) (b) (c) (d)

Figure 5.14: Driver and TW-MZM cosimulation results. 56 Gbaud QPSK operation is plotted as an NRZ waveform for the I channel for the driver output voltage signal (a), the modulator output optical field signal (b), and the received electrical signal at the output of the TIA (c). A measured I-channel eye diagram for 56 Gbaud QPSK transmission with the fabricated driver, TW-MZM, and receiver components is also plotted, and has good agreement with simulation (d).

model of the TW-MZM, which was based on CAD modelling and measured performance data, was incorporated into a transistor-level simulation of the driver circuit. This enables the simulation to capture reflection effects at both the input and the termination of the TW-MZM. Next, this simulated driver output signal was used in a full-link optical simulation that captured electro-optic interaction in the TW-MZM structure, as well as optical losses, noise sources, and frequency responses for the rest of the link. This simulation model was similar to the one described in Chapter 3, and used link parameters based on the best available measured data for the designed components.

The results of this co-simulation for the driver and TW-MZM that will be discussed in Chapter 6 are shown in Fig. 5.14. The simulated driver output voltage signal, modulator output optical field, and receiver TIA output are shown in Fig. 5.14 (a), (b), and (c), respectively, for the I channel for 56 Gbaud QPSK transmission. These simulations were used to predict the performance of the overall link, and tune driver and TW-MZM design to improve overall link budget and BER. This kind of whole-link optimization is key for adapting coherent links to low-power short-reach applications. For comparison, a measured eye diagram of the I channel for 56 Gbaud QPSK transmission in the actual

fabricated link that resulted from these designs. There is reasonably good agreement with the simulated TIA output waveform, validating the usefulness of this co-simulation and holistic link optimization approach.

5.4 Design of a Optoelectronic Transmitter based on Artificial Transmission Lines

One of the promises of silicon photonics (SiPh) has been its compatibility with mature CMOS fabrication processes. For SiPh TW-MZM designs, a fabrication process with integrated inductors provides an opportunity to redesign the MZM transmission line with a higher characteristic impedance. A SiPh TW-MZM that used integrated inductors in a double-pass phase shifter design has been demonstrated, with 18 GHz electro-optic (EO) BW and MZM characteristic impedance close to 50 Ω [42]. This demonstrates the feasibility of improving modulation efficiency independent of the length tradeoff by taking advantage of mature photonic integrated circuit (PIC) fabrication processes with back-end metal stacks for integrated inductors, which could enabling scaling of SiPh TW-MZMs into future generations of optical links.

Here we present an optoelectronic transmitter that comprises an MZM driver, SiPh TW-MZM, and MZM termination chip operating at 50 Gbaud NRZ. The TW-MZM design is a novel hybrid loaded artificial transmission line based on integrated inductors that incorporates a low-power biasing and termination architecture.

The driver in this transmitter is a distributed amplifier designed in the GlobalFoundries 45RFSOI process that is based on an artificial transmission line formed by integrated inductors. The driver includes a 2-tap feedforward equalizer (FFE), and has a 3 dB BW of $>$ 60 GHz and 2 Vppd output swing into a 50 Ω load with the FFE on.

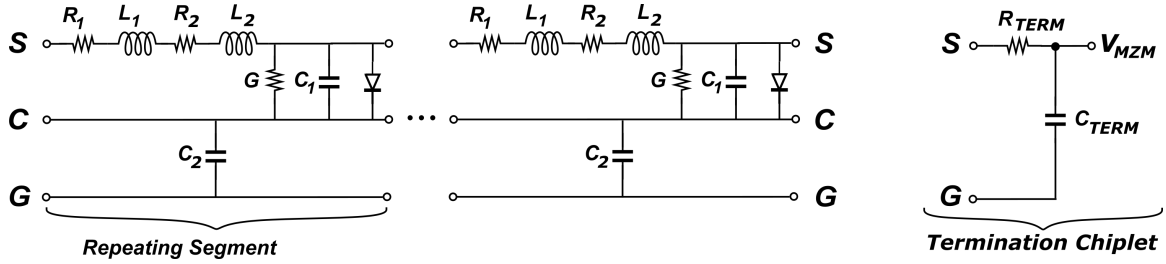


Figure 5.15: Schematic of the TW-MZM and termination designs.

Additional details regarding the driver design and performance are reported in [43].

The designs of one of the two differential arms of the TW-MZM and accompanying termination chip are shown in Fig. 5.15. Each of the eight 300 μm segments fabricated in the GlobalFoundries 90WG process contains a 200 μm pn-junction phase shifter section and a 190 pH spiral inductor denoted by L_2 and R_2. The inductor has a self-resonance frequency of 50 GHz. R_1, L_1, G, and C_1 represent the RLGC transmission line model of the unloaded metal electrodes. Each phase shifter is measured to have a junction capacitance C_j of 40 fF and a $V_\pi L$ of 2.2 V-cm at 2 V reverse bias. The design attempts to minimize the losses in the metal electrodes and spiral inductors, R_1, R_2, and G, in order to improve the TW-MZM BW. Each segment has a large capacitor C_2 that decouples the cathode electrode C to the ground electrode G, enabling independent phase shifter bias control without contributing to DC power dissipation or affecting driver biasing. A TW-MZM with independent cathode bias control that relied on capacitively coupled electrodes was previously reported in [44]. The design presented here makes use of large integrated C_2 capacitors for decoupling to ensure a good AC ground. Within each segment, $C_2 >> (C_1||C_j)$, so the cathode bias decoupling has a negligible effect on the high-speed transmission line characteristics. The loaded characteristic impedance and microwave index of the TW-MZM can be approximated by $Z_0 = \sqrt{(L_1 + L_2)/(C_1 + C_j)}$ and $n_\mu = c_0\sqrt{(L_1 + L_2)(C_1 + C_j)}$ respectively, where c_0 is the speed of light. The integrated inductors contribute to a higher characteristic impedance, which enables a larger

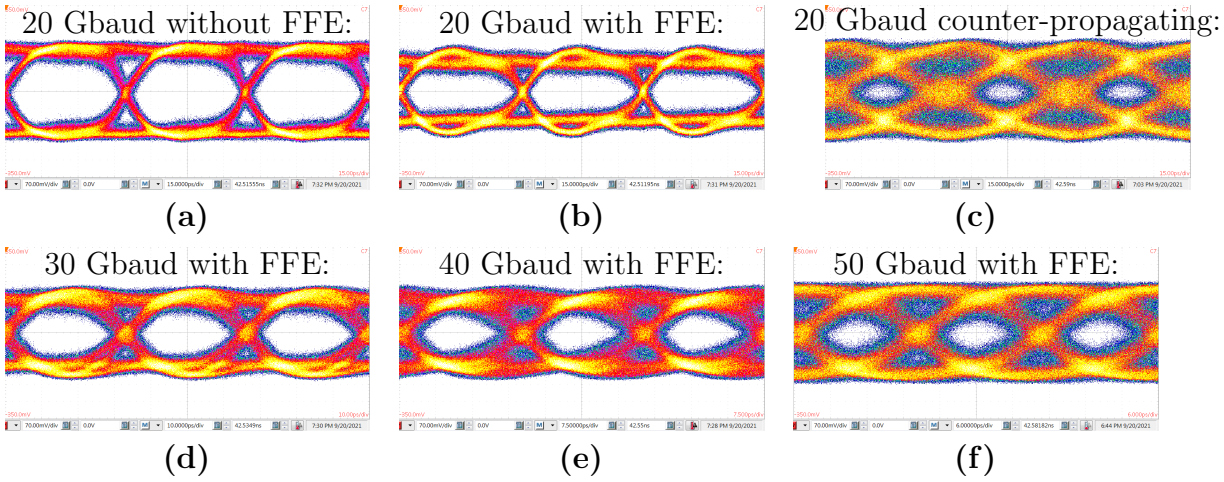


Figure 5.16: Measured optical eyes at 20 Gbaud without (a) and with (b) driver FFE, with a counter-propagating optical signal (c), and at 30, 40, and 50 Gbaud (d-f) with driver FFE.

voltage swing from the MZM driver. An optical delay loop is included in each segment to match the optical and RF wave velocities.

The termination chip is designed to have a differential termination for the two MZM arms, with a designed value of $R_{TERM} = 46\ \Omega$ for each arm. The TW-MZM was designed to have a characteristic impedance of 50 Ω, but the fabricated device had a smaller C_j than expected, resulting in a higher realized impedance, and introducing impedance mismatches. The termination chip allows DC current to be sourced through the V_{MZM} pad to facilitate driver biasing, and additionally decouples this supply to ground with a large capacitor C_{TERM}.

5.5 Experimental Results for a Optoelectronic Transmitter based on Artificial Transmission Lines

The optoelectronic transmitter time domain performance was measured by driving it with bit pattern generator (SHF 12105 A) with 1300 mVppd. Due to the relatively

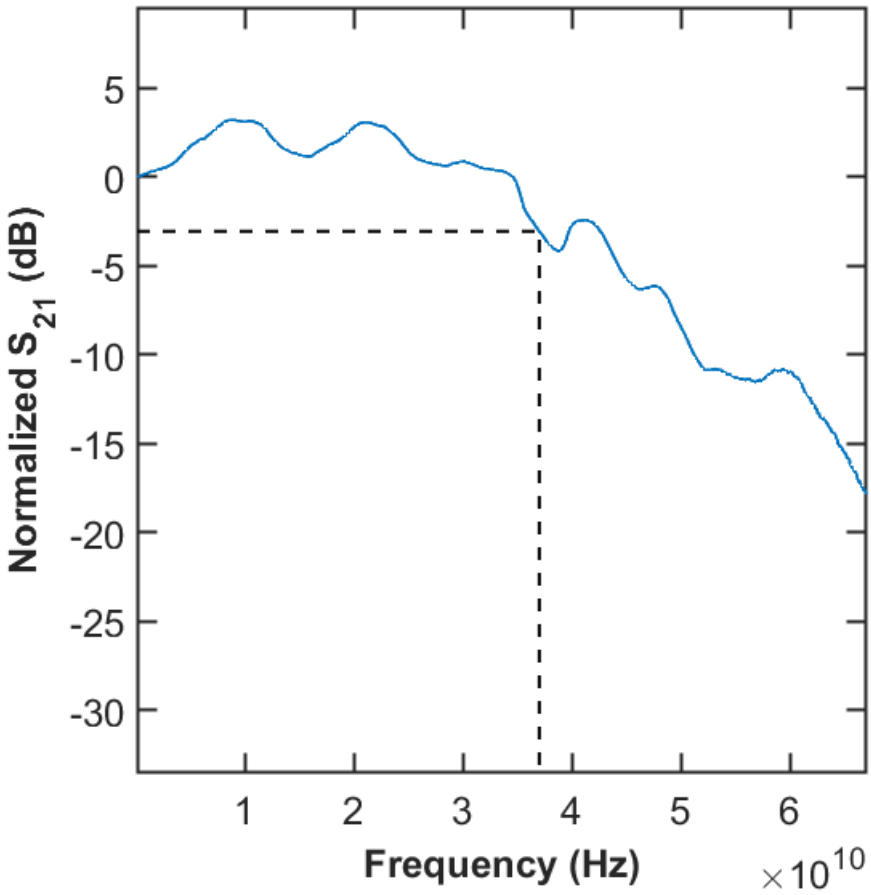


Figure 5.17: Measured EO S_{21} of the TW-MZM.

high insertion loss of the grating couplers on the TW-MZM PIC, a 43 Gbps reference receiver (Finisar XPRV2322A) and electrical sampling module (Tektronix 80E11) with 60 GHz BW were used to measure the eye diagrams shown in Fig. 5.16. Optical amplifiers were also used to amplify the 1310 nm signal before and after the PIC. 20 Gbaud measurements with 2 V phase shifter reverse bias are shown in Fig. 5.16 (a-c), for operation without driver FFE, with driver FFE, and counter-propagating optical signal with driver FFE respectively. The signal degradation in the counter-propagating measurement demonstrates that the MZM is indeed acting as a travelling-wave structure. Additional eye diagrams for operation at 2 V phase shifter reverse bias with driver FFE at 30, 40, and 50 Gbaud are shown in Fig. 5.16 (d-f), respectively.

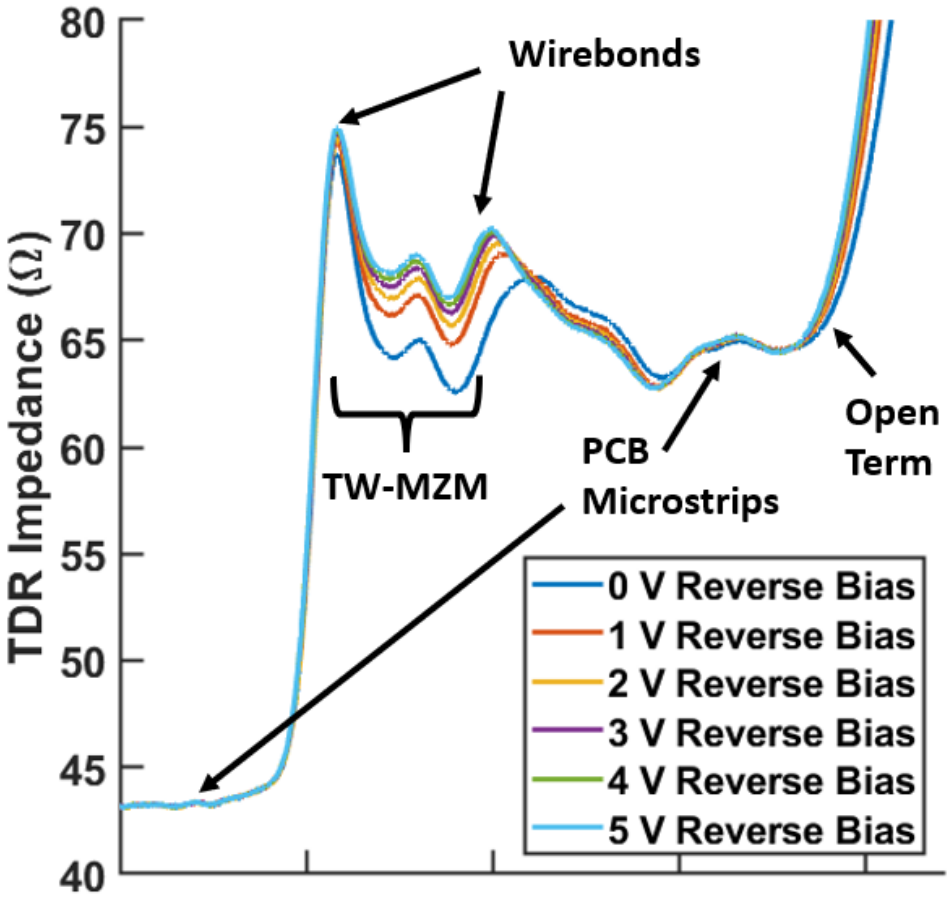


Figure 5.18: Measured TDR impedance for the TW-MZM.

The EO S_{21} of the TW-MZM, measured in a 50 Ω environment, is plotted in Fig. 5.17 for the case of 2 V phase shifter reverse bias, showing a 3 dB BW of 37 GHz. The time-domain reflectometry (TDR) impedance of the TW-MZM is also plotted in Fig. 5.18, where certain features have been labelled. The precise characteristic impedance of the TW-MZM structure could not be accurately extracted due to reflections and losses in the device packaging, although it is estimated to be between $60 - 80$ Ω. The transmitter assembly, including the driver, TW-MZM, and MZM termination chips is pictured in Fig. 5.19. Bathtub curves characterizing the full transmitter operation with the reference receiver and a bit error rate tester (SHF 11104A) are shown in Fig. 5.20. Due to the BW limitations of the reference receiver, higher baudrate bathtubs are not

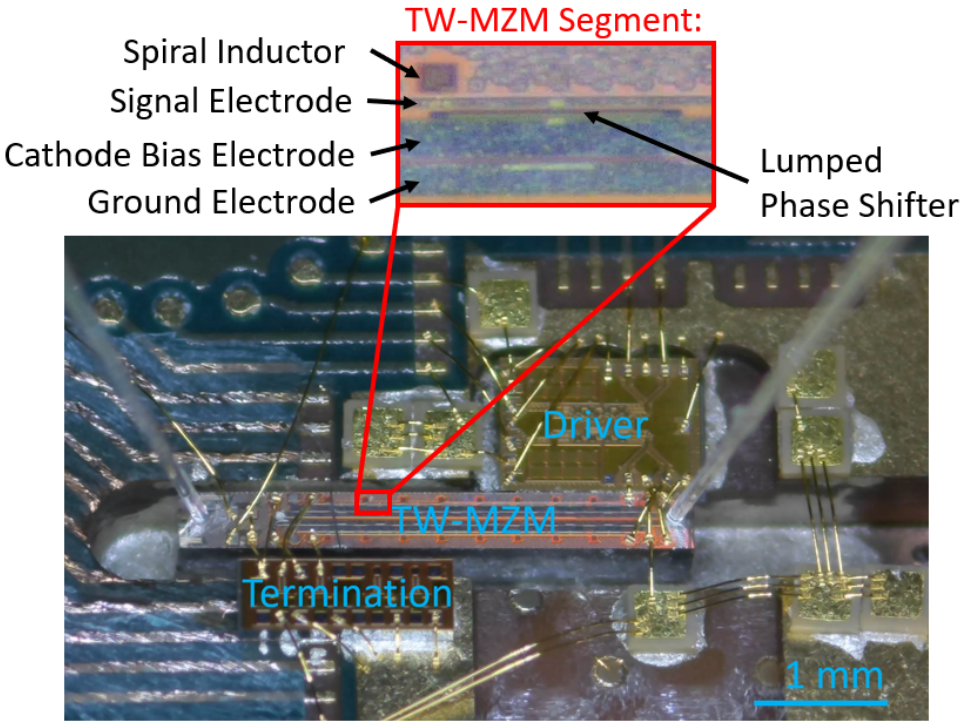


Figure 5.19: The copackaged driver, TW-MZM, and MZM termination chips.

reported and high-baudrate eye diagrams in Fig. 5.16 have significant eye closure. The overall transmitter consumes 233 mW with driver FFE off, and 282 mW with driver FFE on, corresponding to 4.7 and 5.6 pJ/bit at 50 Gbps, respectively.

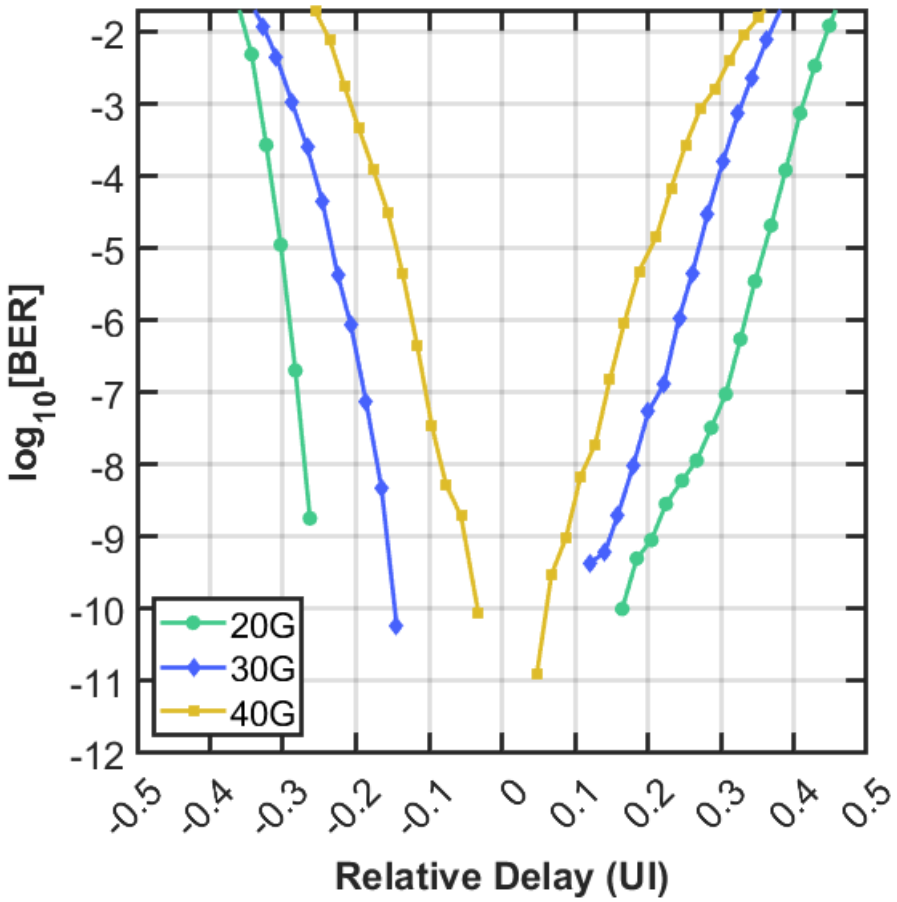


Figure 5.20: Measured bathtub curves for 20, 30, and 40 Gbps NRZ transmission using a PRBS31 pattern.

Chapter 6

O-Band Coherent Links

The O-band coherent link measurements described in this chapter were originally published in [45] and [46].

6.1 Introduction

As data center network traffic continues to increase, future intra-data center optical interconnects must scale to higher data rates while improving overall cost and power efficiency. Through in-phase and quadrature (IQ) modulation with polarization multiplexing, coherent optical link technologies provide a path to increased data rates over intensity modulation direct detection (IMDD) technologies. Short-reach O-band applications with low chromatic dispersion make power-efficient coherent links an attractive replacement for IMDD technologies for the 1.6 Tbps generation and beyond [12]. In an analog coherent detection (ACD)-based link architecture, power consumption is further reduced by performing carrier and polarization recovery in the analog domain without high-speed analog-to-digital conversion and digital signal processing (DSP). We previously reported an ACD link architecture analysis that showed 5-10 pJ/bit energy efficiencies are possible

with 13 dB of unallocated link budget [8].

The design tradeoffs for coherent links change significantly when moving from conventional longer reach long-haul, metro, and inter-data center links to shorter intra-data center ones. Power consumption and cost improvements are crucial for this high-volume application, so link performance must be sacrificed in key areas for coherent link technology to be viable. The ACD link architecture does this by eliminating the carrier and polarization recovery functions traditionally performed by the coherent DSP application specific integrated circuit (ASIC) and replacing them with an optical phase locked loop (OPLL) and analog polarization controller. DSP-based chromatic dispersion compensation is obviated by operating in the O-band, near the zero-dispersion point of single mode fiber. Long-reach coherent links have thus far operated in the C-band because it offers the lowest attenuation and chromatic dispersion can be straightforwardly compensated in DSP, but an additional 0.2 dB/km of loss is tolerable for intra-data center reaches and and O-band coherent link can omit DSP-based chromatic dispersion compensation with negligible penalties [10]. Further power savings come from using QPSK transmission, which enables power-efficient limiting electronics and removes the need for power-hungry analog-to-digital converters. Analog techniques for carrier recovery have been previously demonstrated with an OPLL in [9], and with a carrier phase synchronization chip in a polarization-multiplexed-carrier self-homodyne link, in [47].

The design requirements for intra-data center coherent links goes beyond the transceivers themselves, however. ACD links with large unallocated link budgets enable data center networks with passive arrayed waveguide grating routers (AWGRs) or active optical switches, improving overall network latency, cost, and power consumption [1]. Dynamic network reconfigurability from optical switching can optimize server and resource utilization for specific workloads, with projections of >2X energy efficiency improvement for the entire system [3]. In fact, optical switching is already deployed at scale in data

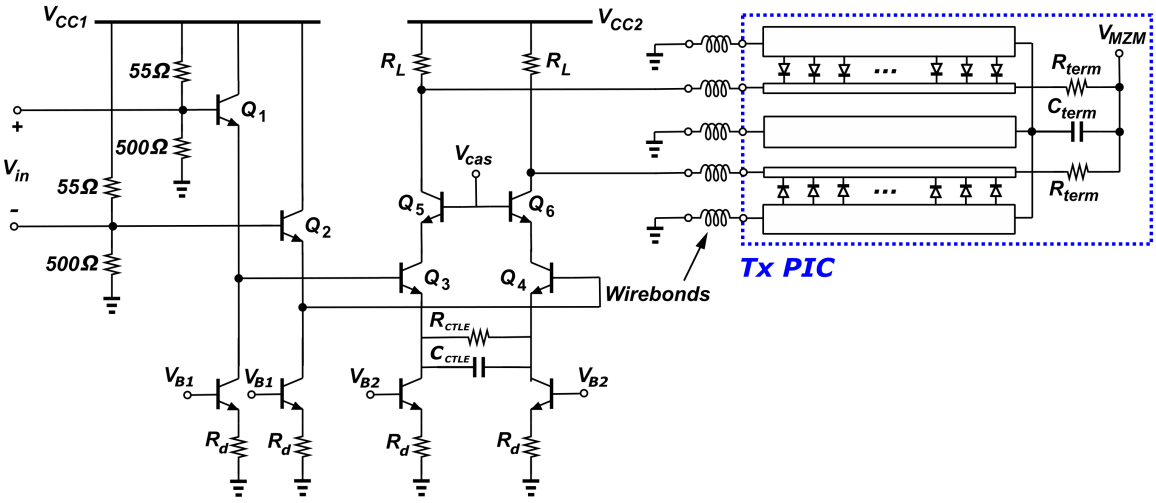


Figure 6.1: Schematic of one differential driver and MZM channel. The full Tx includes 4 channels for the DP-IQ-MZM.

centers. In [2], Google report 41% reduced power consumption and 30% reduced cost for their overall data center networks, including switches and interconnects. Furthermore, dynamically reconfigurable optical circuit switches have yielded advantages in network throughput and incremental installment. These optical switches have been widely and reliably deployed in production traffic, and are enabled by optical link technologies that support additional loss in their link budgets. As data rates scale, low-power analog coherent links are the ideal link technology to support widespread adoption of optical circuit switching across the industry.

We present here the first full-link demonstration of an O-band coherent link designed for intra-data center applications, with 56 Gbaud quadrature phase shift keying (QPSK) operation for 112 Gbps per polarization with a bit error rate (BER) of $2.1 \cdot 10^{-4}$. The achieved BER is below the threshold for KP4 forward error correction (FEC). We have designed and fabricated custom transmitter (Tx) and receiver (Rx) electronic and photonic integrated circuits (EICs and PICs) for an ACD-based link. Previously reported O-band coherent results for either high-speed Tx PICs [48] or Rx PICs and EICs [49]

have relied on test equipment in the absence of integrated photonics or electronics for the full link. Our custom Tx was also measured stand-alone, resulting in record-high 64 Gbaud operation with a BER $< 10^{-4}$ for a combined O-band coherent driver and modulator. A full-link demonstration of an O-band coherent link that includes custom Tx and Rx EICs and PICs operating at 224 Gbps will then be presented. This result is the first demonstration of any >200 Gbps full link operating in the O-band, either coherent or IMDD. Section 6.2 will describe the design of the first O-band coherent Tx and Rx demonstration, while Section 6.3 will present results of component and link characterization experiments. The 224 Gbps link design and experimental results will be reported in Section 6.4 and Section 6.5, respectively, and concluding remarks will be made in Section 6.6.

6.2 Design of first O-band Coherent Link for Data Center Applications

The Tx and Rx PICs were fabricated in Intel's silicon photonics process. The Tx and Rx EICs were fabricated in the GlobalFoundries 9HP 90 nm and 8XP 130 nm SiGe BiCMOS processes, respectively. The driver has 2 Vppd output swing and 45 GHz bandwidth across four differential channels that drive a dual-polarization (DP)-IQ travelling wave Mach-Zehnder Modulator (MZM) on the Tx PIC. The output stage load resistor R_L is 200 Ω. This quasi-open collector design maintains low power consumption while suppressing back-reflection effects from the travelling wave MZM, thereby averting the need for DSP-based equalization to recover Tx signal integrity [34]. The driver also included a continuous time linear equalizer (CTLE) circuit in the output stage to peak the output and compensate for bandwidth degradation in the Tx PIC and receiver. The

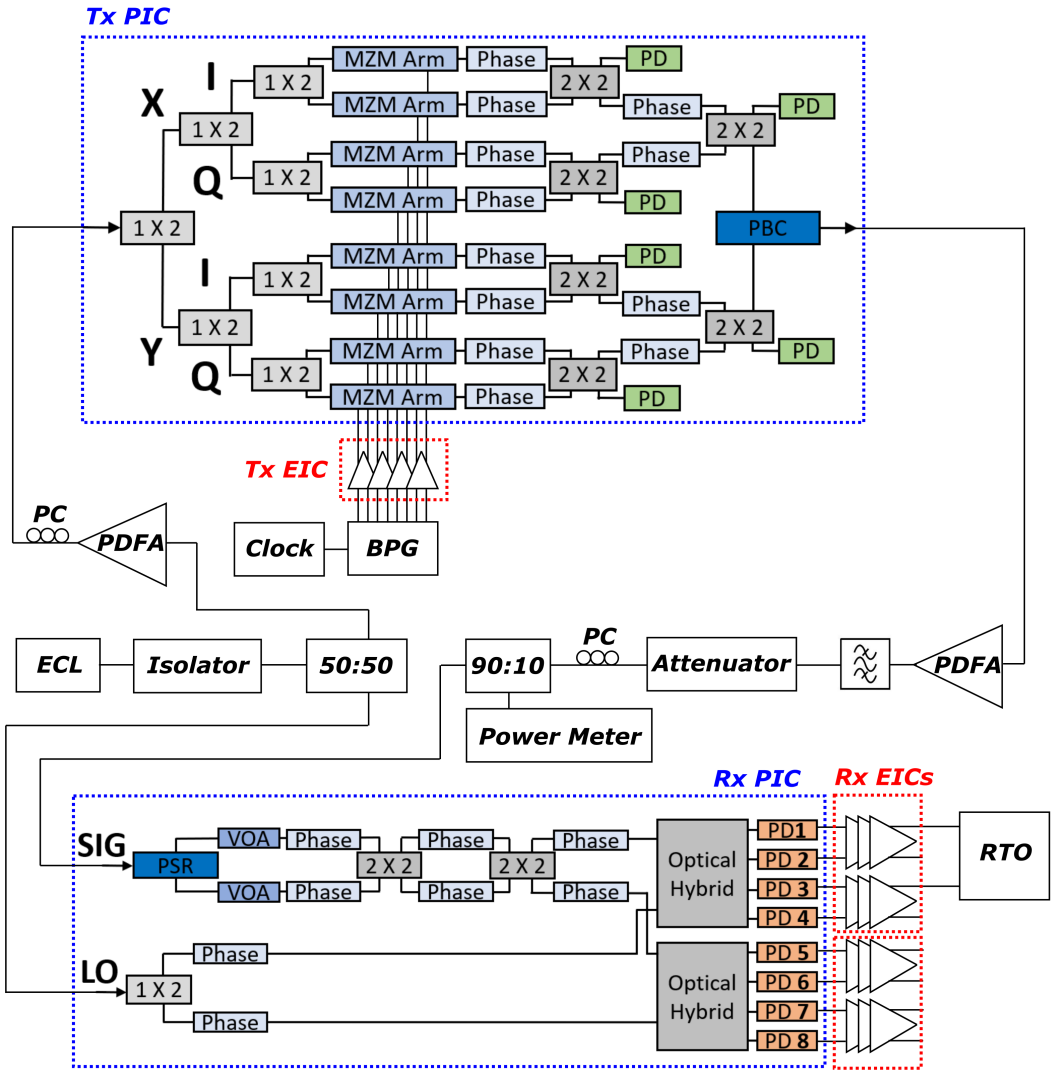


Figure 6.2: Schematic of the full link measurement setup, including optical component block diagrams of Tx and Rx PICs.

nominal design had 9.5 dB of peaking at 30 GHz, and a schematic of one channel of the driver circuit integrated with a MZM on the Tx PIC is shown in Fig. 6.1.

The Rx EIC design was reported previously [50], and included the data path Rx chain with transimpedance amplifiers (TIAs) and variable gain amplifiers (VGAs) as well as the phase-frequency detector (PFD) circuit required for closed-loop OPLL operation. Since the target modulation format is QPSK, the Tx and Rx both took advantage

of power-efficient limiting amplifier circuits. The Rx PIC is similar to a conventional dual-polarization coherent receiver with differential photodiodes (PDs), except that it includes an analog polarization controller, formed from a series of phase shifters and 2x2 multi-mode interferometers (MMIs) after the polarization splitter rotator (PSR) in the signal path. Endless reset-free polarization control has been previously demonstrated [51], including recent demonstrations with integrated phase shifters [11]. This polarization controller is based on integrated thermal phase shifters and can perform arbitrary polarization rotation, but not in a reset-free manner. In this work, the polarization controller was controlled manually to provide a static polarization rotation at the receiver. Appropriate feedback and closed loop control will be incorporated in a future ACD-based receiver PIC.

The Tx and Rx EICs and PICs were packaged with wirebonds on FR4 PCBs, with mini-SMP connectors and coaxial cables forming a high-speed interface to test equipment. Additional details of the PCB packaging platform used in this work are described in [52]. The assemblies are compatible with a permanent fiber attachment process, forming complete dual-polarization designs capable of capable of 224 Gbps/λ. During the design process, electronic and photonic circuit and component performance was optimized using full-link time-domain simulations. The link model included component losses, bandwidths, packaging parasitics, and noise contributions, and incorporated co-simulation of high-speed optoelectronic device performance with transistor-level electronic circuit simulations. In this manner, the designs were optimized with the direct goal of full-link integration. This allowed for co-optimization of driver output stage CTLE, driver load resistor, and travelling wave MZM phase efficiency and bandwidth to minimize ISI and noise across both the Tx and Rx, and to improve the overall available link loss budget.

6.3 Results of first O-band Coherent Link for Data Center Applications

6.3.1 Experimental Setup

As the integrated lasers required for an OPLL were not included in these first-gen PICs, a 1310 nm external cavity laser (ECL) was split into local oscillator (LO) and signal paths in a self-homodyne link configuration. The link measurement setup is shown in Fig. 6.2 along with block diagrams of components of the Tx and Rx EICs. 500 mV PRBS15 differential signals from a bit pattern generator (BPG) (SHF 12105A) drove the Tx EIC, and Rx EICs outputs were detected by a real-time oscilloscope (RTO) (Keysight UXR0702A) with a 0.875 μs acquisition time at 256 GSa/s. A post-processing script corrected static constellation rotation, then sampled and counted bit errors. No external equalization or additional post-processing was performed, so the results reported in this work represent native link performance, including all ISI and packaging effects. These results are for the first Tx and Rx subsystems we have built, and due to assembly yield we are reporting dual-polarization QPSK transmission with only single-polarization 112 Gbps receiver operation. Future assemblies will be capable of full dual-polarization 224 Gbps/λ operation.

6.3.2 Transmitter Characterization

The driver EIC all-electrical time-domain performance was measured by driving a single channel with 650 mVppd from the BPG and measuring the output with a 70 GHz electrical sampling module (Tektronix 80E11). The resulting 56 Gbaud eye is shown in Fig. 6.3 for a driver EIC variant that included output stage CTLE. This eye diagram includes bandwidth effects from the PCB packaging and coaxial cables at both the input

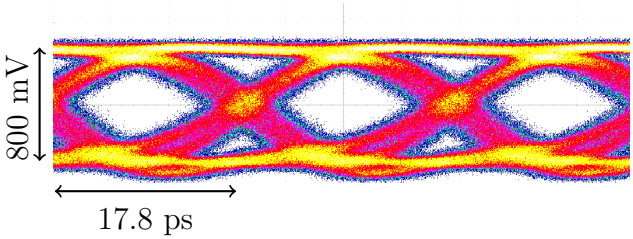


Figure 6.3: Measured all-electrical eye diagram of 56 Gbaud NRZ driver operation for one single-ended output.

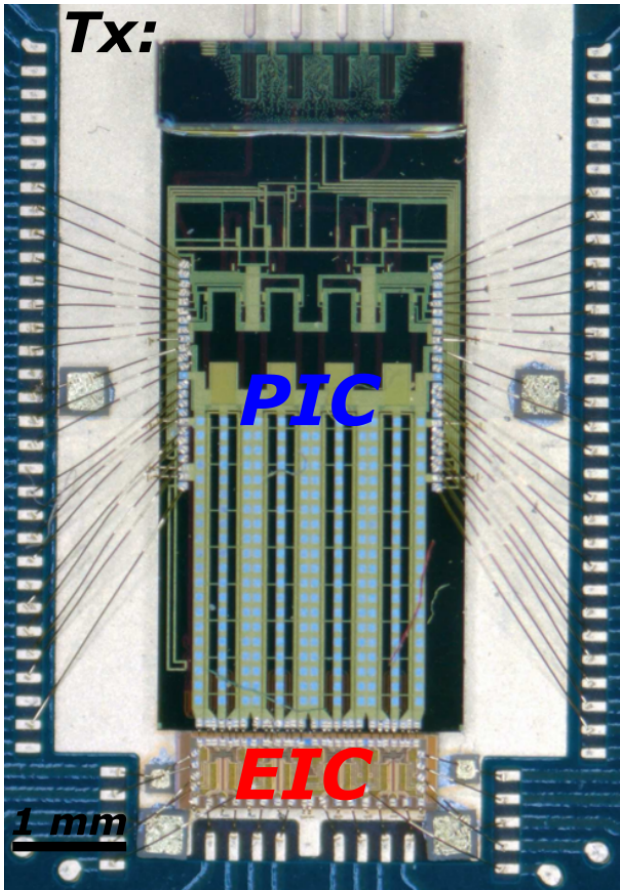


Figure 6.4: Transmitter EIC and PIC, packaged on a PCB with wirebonded connections.

and output.

A Tx subassembly consisting of a DP-IQ-MZM PIC and a driver EIC variant without output stage CTLE was then characterized in a standalone configuration with a reference receiver. The packaged transmitter is shown in Fig. 6.4. The Rx PIC and EICs in Fig. 6.2

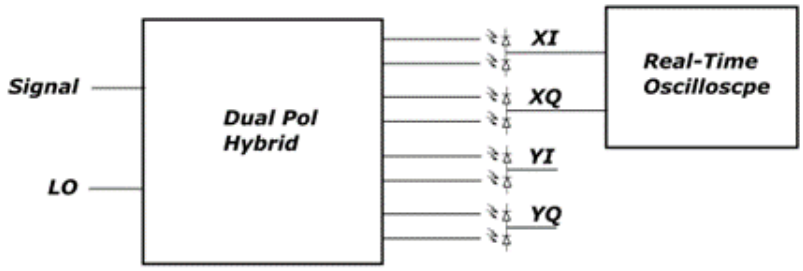


Figure 6.5: Schematic of the reference receiver setup used for standalone transmitter characterization.

were replaced by a reference optical hybrid (Kylia COH28X-FCAPC-1300nm) and balanced 70 GHz PDs (Finisar BPDV3320R), shown in Fig. 6.5. Resulting 56 and 64 Gbaud sampled constellations with BER $< 10^{-4}$ are shown in Fig. 6.6. Raw unsampled constellations are shown in 6.6(a) and (b), I-channel eye diagrams are shown in 6.6(c) and (d), and sampled constellations are shown in 6.6(e) and (f). BER sensitivity curves for this standalone Tx and reference Rx are shown in Fig. 6.7. As the unamplified output signals from the PDs were measured directly by the real-time oscilloscope, the absolute Rx input power sensitivity of this measurement does not correspond to the sensitivity of a full-link with an integrated TIA-based receiver EIC. Due to the lack of a receiver EIC and the 70 GHz PD bandwidths, however, the link inter-symbol interference (ISI) is dominated by bandwidth limitations in the Tx. The 28 Gbaud curve in Fig. 6.7 is noise-limited with negligible ISI penalty, and since no external or post-processing equalization was performed, the power-penalties shown in the 56 and 64 Gbaud curves can be attributed to the increased Tx ISI at higher symbol rates.

6.3.3 Full-Link Demonstration

Finally, the full-link performance with custom Tx and Rx EICs and PICs was characterized. The assembled transmitter is shown in Fig. 6.4, and the assembled receiver is

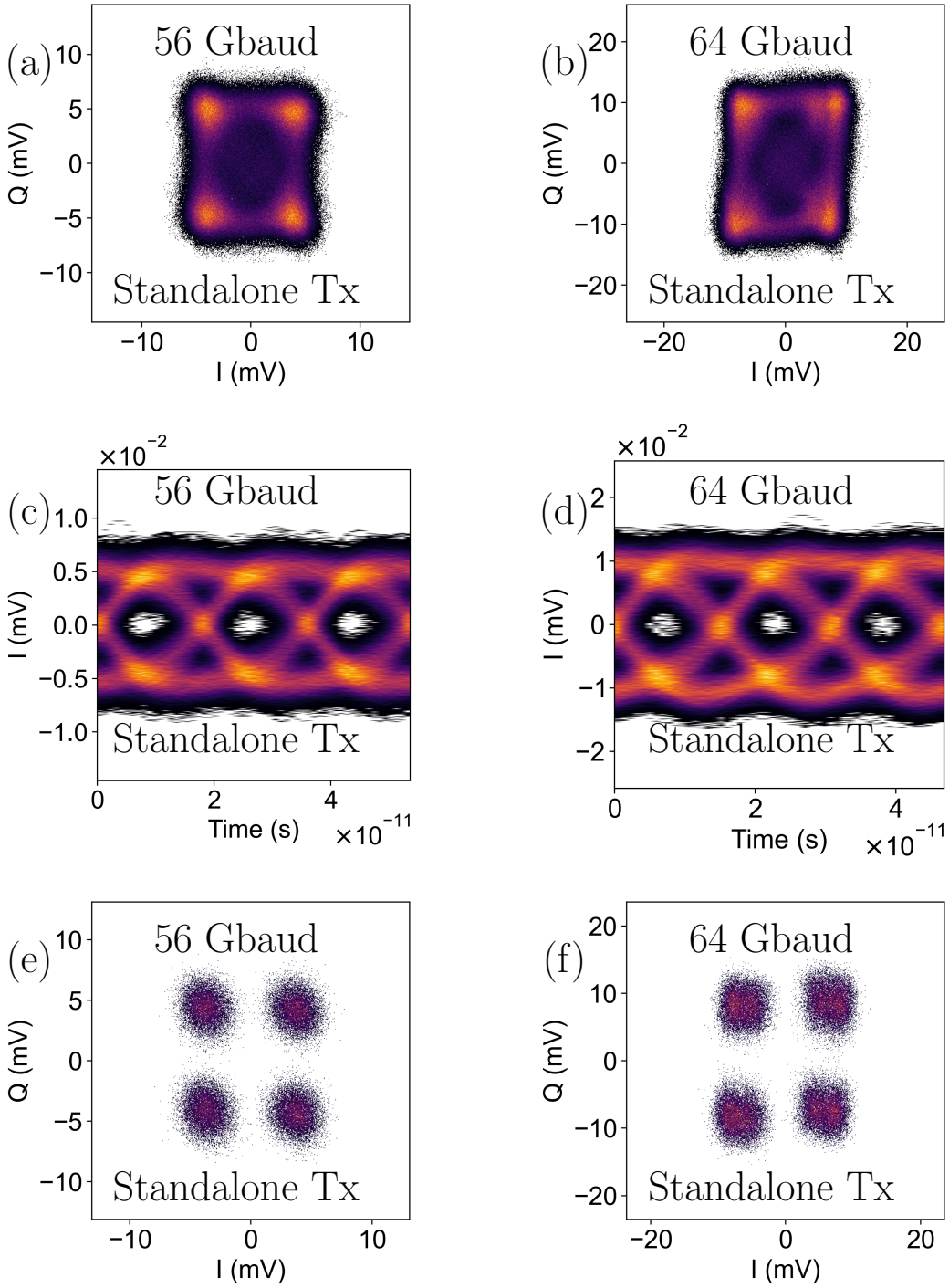


Figure 6.6: Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for standalone transmitter 56 and 64 Gbaud QPSK operation with reference receiver.

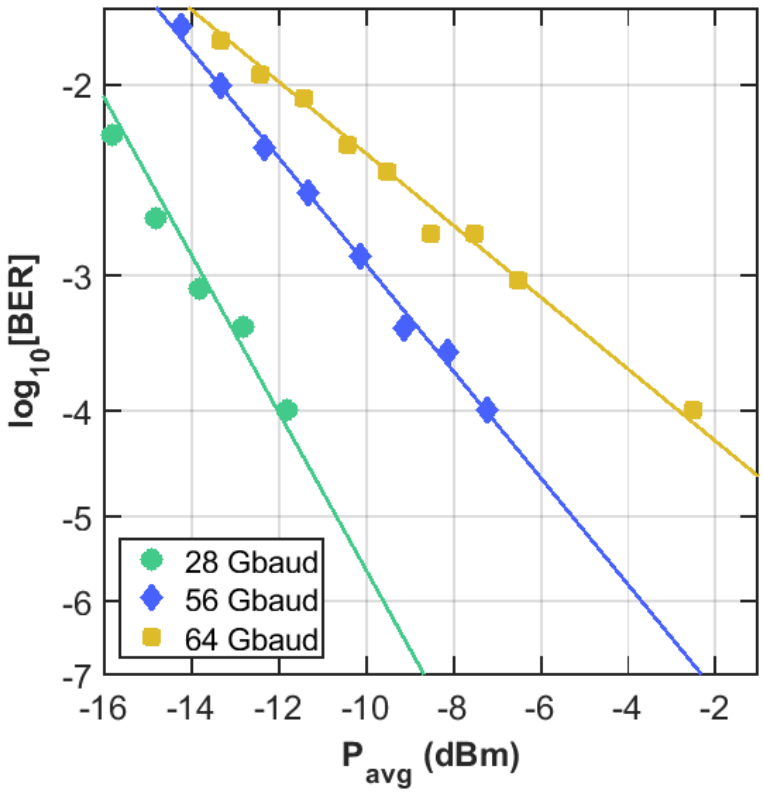


Figure 6.7: Measured BER vs Rx input power for the standalone Tx with a reference receiver with −2 dBm LO power per PD.

shown in Fig. 6.8. Single-polarization 56 Gbaud QPSK full-link operation is shown in Fig. 6.9(a), (c), and (e). Dual-polarization transmission, with one polarization channel operating at the receiver, is shown in 6.9(b), (d), and (f). The raw unsampled constellations are shown in 6.9(a) and (b), the projections of each constellation onto the in-phase (I) received channel are plotted as eye diagrams in 6.9(c) and (d), and sampled constellations are shown in 6.9(e) and (f). Sampled constellations for single- and dual-polarization QPSK transmission at 28 Gbaud are shown in Fig. 6.10. All of these constellations correspond to measured BER $< 10^{-3}$. Because no external equalization is being performed, cumulative link ISI from bandwidth limitations in the EICs, PICs, and packaging manifests in the sampled constellations shown here. Constellation points resulting from lower baudrate transmission are noise-limited and appear as circular additive white Gaussian

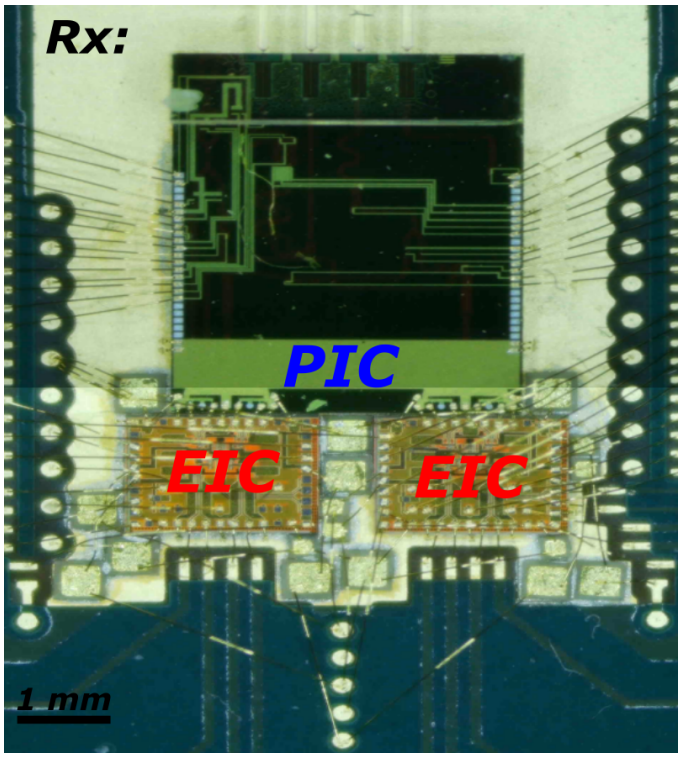


Figure 6.8: Receiver EIC and PIC, packaged on a PCB with wirebonded connections.

noise (AWGN) distributions, as in Fig. 6.10. Meanwhile, constellation points from higher baudrate operation appear more square, as in Fig. 6.6(f) and Fig. 6.9(e) and (f).

The impact of polarization crosstalk can be seen by comparing corresponding measured constellations. BER vs average signal power at the Rx input for the full link is plotted in Fig. 6.11 for 28 and 56 Gbaud. The achieved BER is $2.1 \cdot 10^{-4}$ at 56 Gbaud. Rx input power is reported for a single polarization to normalize the results, and the measured power penalty from polarization crosstalk is 1 dB. The 9 dB power penalty between the 28 and 56 Gbaud sensitivity curves is a measure of the ISI from cumulative link bandwidth impairments, including PICs, EICs, and packaging.

Total power consumption with both polarization channels on was 2.1 W (9.5 pJ/bit). This includes 1.0 W (4.5 pJ/bit) from the driver, 0.2 W (1 pJ/bit) from the Tx PIC, and 0.9 W (4 pJ/bit) from the Rx EIC. Although external optical amplifiers were employed

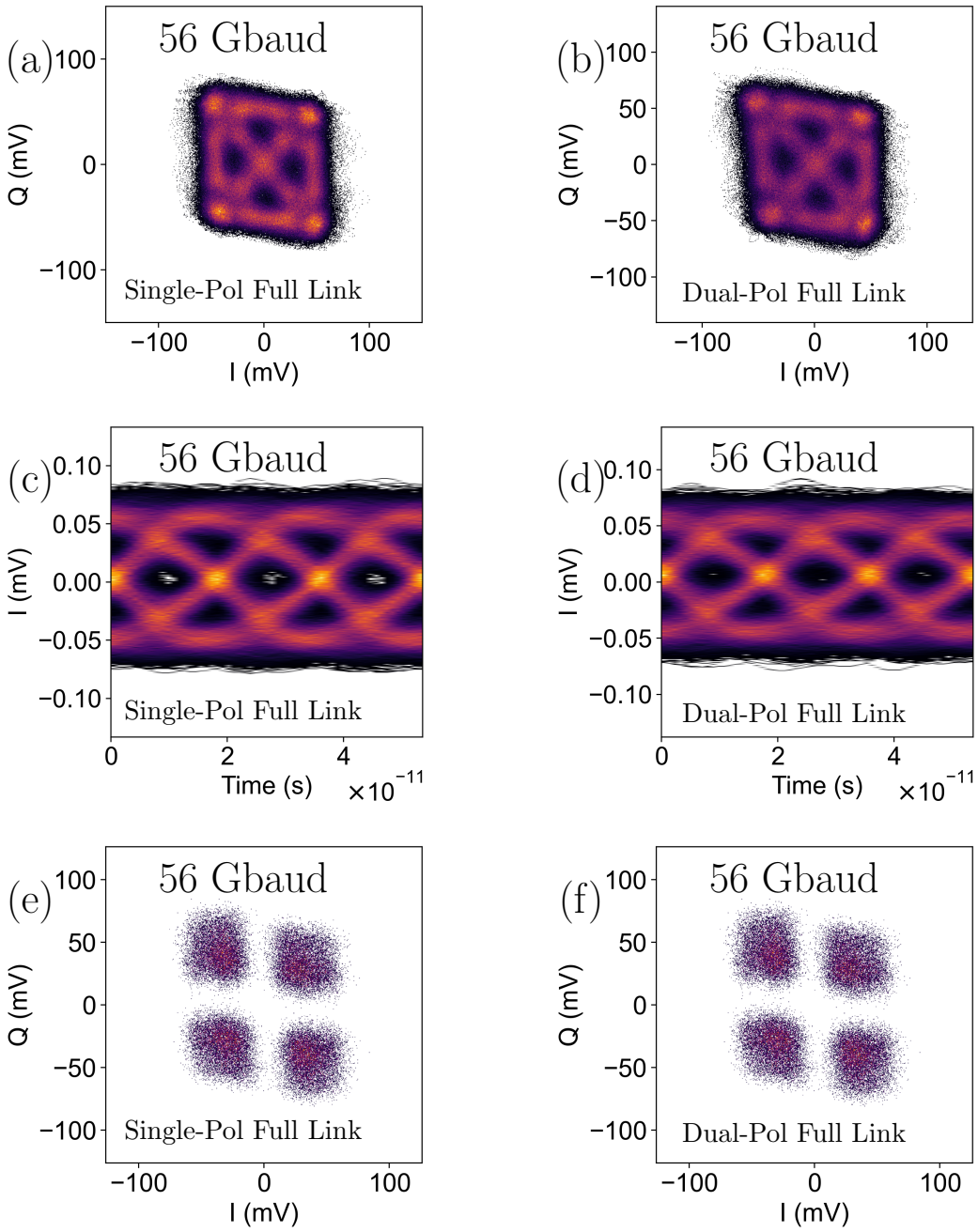


Figure 6.9: Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for single- and dual-polarization 56 Gbaud QPSK full-link transmission.

in this first demonstration, received photocurrents were kept below levels expected from next-gen PICs designed with integrated lasers and SOAs. The average LO power incident

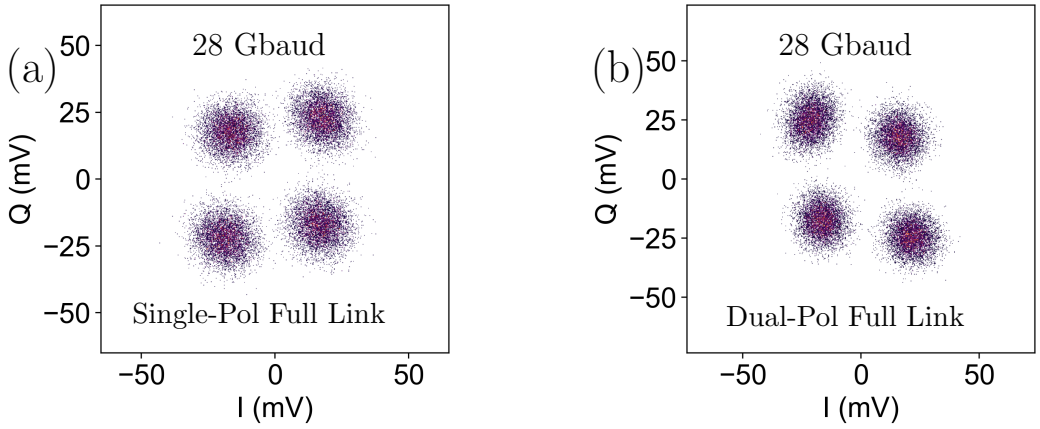


Figure 6.10: Measured sampled constellations for single- and dual-polarization 28 Gbaud QPSK full-link transmission.

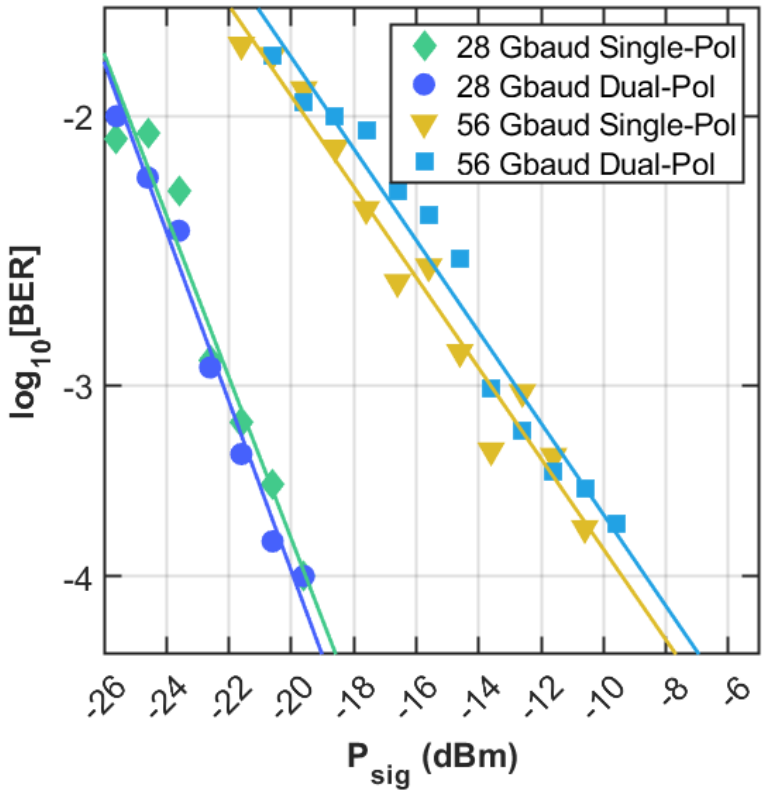


Figure 6.11: Measured BER vs Rx input power (per polarization) for the full Tx + Rx link with and without polarization crosstalk.

on each PD was -3.3 dBm, and the received signal power sensitivity values plotted here are expected to improve with higher LO power. Thus, the absolute receiver sensitivity values shown in Fig. 6.11 don't correspond directly to the sensitivity of a realistic link implementation. For reference, an ACD-based receiver with an integrated 13 dBm output power LO laser and 2 dB of on-chip excess losses would have 2 dBm LO power incident on each PD. Measurement results with next-generation Tx and Rx PICs that include integrated lasers and SOAs are forthcoming. These PICs will improve on the relatively constrained link budget demonstrated in this work by removing unneeded Tx and Rx fiber coupling as well as signal/LO splitting losses. We expect the full ACD-based link based on these PICs to operate below the KP4 FEC threshold with 13 dB of available link loss budget on the fiber, without any external amplification.

6.4 Design of 224 Gbps/λ O-band Coherent Link

The Tx and Rx PICs in this work were fabricated in Intel's silicon photonics process. Dual-polarization in-phase and quadrature Mach-Zehnder modulator (DP-IQ MZM) PIC operation with the DP-IQ MZM driver EIC, which was fabricated in GlobalFoundries 9HP 90 nm BiCMOS process, was previously reported in Section 6.2. The DP coherent receiver PIC was packaged with a transimpedance amplifier (TIA) EIC fabricated in GlobalFoundries 45RFSOI 45 nm CMOS process. The PIC includes an integrated analog polarization controller circuit that allows for optical domain manipulation and demultiplexing of the received polarization channels. The Rx EIC is based on a record low-power inverter shunt-feedback TIA, and was previously reported in [55]. The total power consumptions of the Tx and Rx ICs were 1.3 W and 0.2 W, or 5.9 pJ/bit and 0.9 pJ/bit at 224 Gbps, respectively. PICs and EICs for both Tx and Rx were packaged on FR4 PCBs with wirebonded high-speed connections. In future designs, wavelength

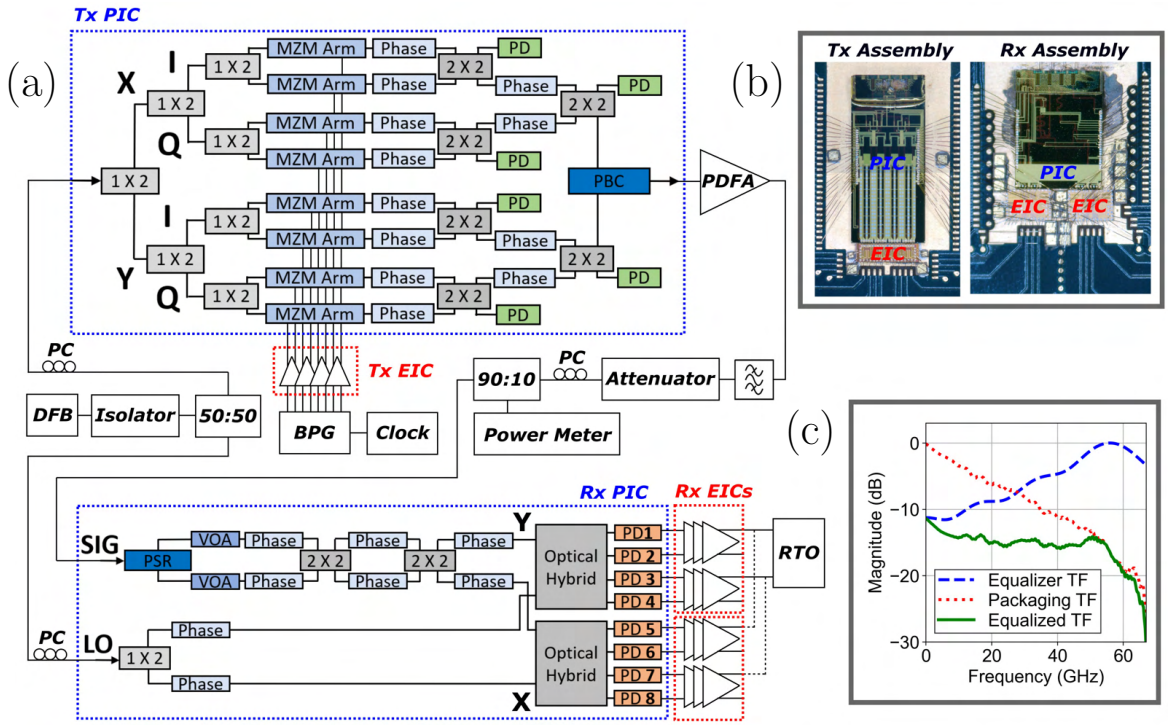


Figure 6.12: (a) Block diagram of measurement setup and Tx and Rx PIC components. (b) The packaged Tx and Rx with custom EICs and PICs. (c) Measured packaging frequency response compared to post-processing equalizer and resulting equalized frequency responses.

division multiplexing (WDM) can scale the transceiver data rate with 4 λs for 800G or 8 λs for 1.6T.

6.5 Results of 224 Gbps/λ O-band Coherent Link

A diagram of the link measurement setup and images of the packaged Tx and Rx are shown in Fig. 6.12(a) and (b), respectively. Since first-generation PICs that do not include integrated optical gain were used, a distributed feedback laser (DFB) (AeroDIODE 1310LD-4-1-1) was split into signal and local oscillator (LO) paths in a self-homodyne configuration. A bit-pattern generator (BPG) (SHF 12105A) drove the driver EIC with 500 mV PRBS15 signals, and a real-time oscilloscope (RTO) (Keysight UXR0702A) mea-

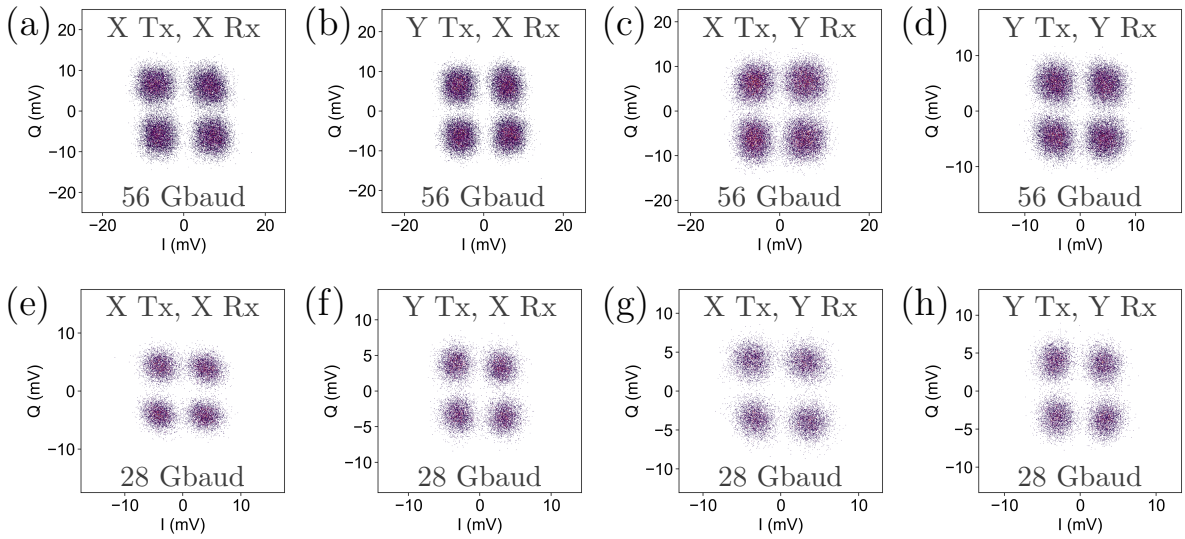


Figure 6.13: Measured DP-QPSK constellations for (a-d) 56 Gbaud and (e-h) 28 Gbaud full-link operation. Individual constellations are shown for the X and Y polarization channels in the Tx and Rx.

sured the recevier EIC output at 256 GSa/s with a 0.586 μs acquisition time. Due to limited RTO channels, only one Rx polarization channel was measured at a time, and the coaxial cable connections were swapped to characterize the other polarization channel. The measured constellations were post-processed to apply static constellation rotation, equalization, and sampling, and then to count bit errors. A 7-tap feed-forward equalizer (FFE) was used in post-processing to de-embed the insertion loss due to Tx and Rx packaging. The packaging losses from the PCB microstrip transmission line, mini-SMP connector, and coaxial cables are unfortunately unavoidable for link characterization with a BPG and RTO, but they would not be present in an integrated transceiver module. As shown in Fig. 6.12(c), this equalizer does not compensate bandwidth impairments beyond measured off-chip packaging losses.

Constellations for full-link DP-QPSK transmission are shown in Fig. 6.13(a-d) for 56 Gbaud and Fig. 6.13(e-h) for 28 Gbaud. The on-chip polarization controller was used to switch between Rx polarization channels. A constellation is shown for each configu-

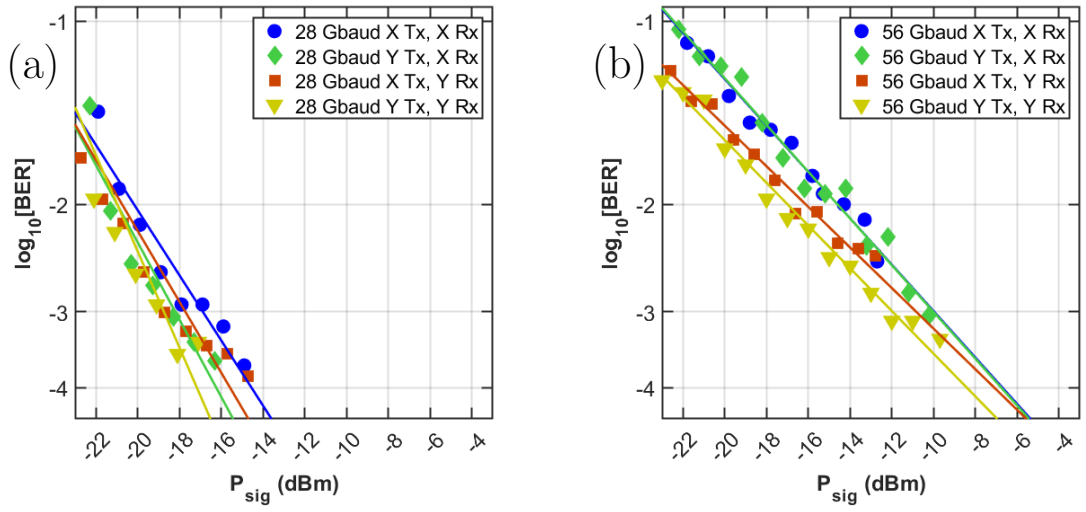


Figure 6.14: Measured BER vs Rx input power for (a) 28 Gbaud and (b) 56 Gbaud DP-QPSK operation. Plotted trend lines are fit from the data.

ration of Tx and Rx X and Y polarization channels with operation below the $3.8 \cdot 10^{-3}$ HD-FEC threshold in each case. Corresponding BER sensitivity curves for each polarization configuration for 28 Gbaud and 56 Gbaud DP-QPSK are shown in Fig. 6.14(a) and (b), respectively. All of these measurements are for dual-polarization transmission in the presence of polarization crosstalk effects, with Rx input power reported as the power on the fiber of the polarization channel being measured and 3.8 dBm average LO power incident on each photodiode (PD).

6.6 Conclusion

We have demonstrated the first full O-band coherent link, including custom driver and receiver EICs integrated with Tx and Rx PICs. Stand-alone O-band coherent Tx operation was shown at a record 64 Gbaud. Full-link 56 Gbaud dual-polarization QPSK transmission was shown with a BER of $2.1 \cdot 10^{-4}$ with 2.1 W (9.5 pJ/bit) power consumption. We expect 2.8 W (12.5 pJ/bit) power consumption for the full 224 Gbps/λ link,

including the OPLL, based on next-generation PICs with integrated optical gain. Tunable O-band lasers integrated in this silicon photonics platform were previously reported in [53].

We have also demonstrated a 224 Gbps/λ O-band coherent link with full dual-polarization Tx and Rx operation below the $3.8 \cdot 10^{-3}$ HD-FEC threshold in [46]. This is the first demonstration of a >200 Gbps/λ O-band optical link, either coherent or IMDD, that uses custom integrated electronics and photonics for the Tx and Rx. The link power consumption in this work was 1.5 W (6.8 pJ/bit), and <10 pJ/bit power consumption is expected for a next-generation link using PICs that include integrated optical gain.

Coherent interconnects for intra-data center applications remain an attractive solution to the meet the demands of rising data rates, but require significant redesign to achieve competitive power consumption and cost. The analog coherent approach outlined in this work aims to obviate and offload functions from the coherent DSP ASIC, which represents the dominant contribution to transceiver power consumption and cost in conventional coherent architectures. Performing polarization recovery, carrier recovery, and bandwidth equalization in the analog domain removes the need for power-hungry analog to digital converters (ADCs), and O-band operation removes the need for chromatic dispersion compensation. Perhaps the most significant benefit of intra-data center coherent link adoption would be the optical switching networks enabled by larger link budgets. Optical switching deployment has already demonstrated significant and quantifiable improvements to data center networks, and short-reach O-band coherent links will empower them by efficiently scaling links with higher data rates and expanded link budgets. While integration challenges remain, the full-link optimization, analog techniques, and new design spaces described in this work are building blocks for future low-power short-reach O-band coherent link deployment. These results show the potential of a low-power ACD architecture and pave the way for bringing coherent links inside data centers.

Chapter 7

Conclusion

7.1 Summary of Findings

Various aspects of the development of energy-efficient intra-data center coherent links with high link budget have been presented. Coherent link technology is an attractive option for next-generation data center networks, because of the higher realizable per-wavelength data rates, and especially because of the potential for improved link budget and tolerance to optical losses in the network. However, the coherent links that will widely deployed inside future data centers will look quite different from the more conventional longer-reach coherent technologies used today. One option for rearchitecting coherent links for short-reach applications is to incorporate the analog coherent techniques used in the hardware designs throughout this work. Transitioning to O-band operation for the coherent link removes the need for DSP-based chromatic dispersion compensation, and analog polarization and carrier recovery can efficiently offload those functions from the DSP as well. Further, QPSK-based modulation, while supporting lower data rates than higher-order modulation formats, is attractive for its improved link budgets and its potential to leverage power-efficient limiting electronics and remove power-hungry DACs

and ADCs from the DSP ASIC. Additionally, integrated SOAs and the analysis carried out in Chapter 3 will play a crucial role in optimizing the energy-efficiency of intra-data center coherent links, whether or not all of the specific ACD techniques mentioned above are eventually adopted.

Experimental demonstrations of electronic and photonic circuits that embody these design philosophies were also presented in this work. A 100 Gbaud PCB packaging platform was developed to support the integration and testing of various electronic and photonic components and subsystems involved. Silicon photonic coherent transmitter and receiver PICs were designed and fabricated in multiple processes. Whole-link optimization techniques were used to design each component for optimum energy-efficiency and performance for the overall link. An integrated O-band coherent transmitter based on co-designed driver and TW-MZM chips was demonstrated with 64 Gbaud QPSK operation, and measured next-generation driver performance shows potential for >100 Gbaud modulation. The world's first demonstrations of full O-band coherent links designed for intra-data center applications have also been presented. These demonstrations culminated in a 224 Gbps/λ 56 Gbaud DP-QPSK link which supports <10 pJ/bit power consumption including the PICs and EICs for the Tx and Rx. This was in fact the first such >200Gbps/λ full-link demonstration of any type to-date, either coherent or IMDD.

7.2 Future Work

The first O-band link demonstrations reported here are based on first-generation PICs that did not include integrated lasers and SOAs. Future work that characterizes the performance and stability of full ACD-based links that include these integrated lasers and SOAs is underway, and initial results for an integrated transmitter have already been reported [56]. OPLL operation for 50 Gbaud QPSK, and endless reset-free polarization

control remain to be demonstrated for ACD link operation. Future work could also involve scaling coherent link components and subsystems to wavelength multiplexed operation in the O-band, which is necessary for high per-fiber data rates. Looking further ahead, low-power coherent link scaling for future generations would need to use higher order modulation, more parallel wavelengths or fibers, or higher symbol rates. OPLL operation can be extended to accommodate 16QAM by using 2-bit quantizers in the loop, but this complicates the design linearity requirements and constrains the tolerable input signal swing range. In principle, the QPSK OPLL could support 16QAM carrier recovery without modification, due to alignment of diagonal constellation points, but the resulting phase detector performance penalty remains to be characterized. Characterization and subsequent iteration of next-generation driver and TW-MZM designs that are being fabricated could demonstrate higher-speed operation and approach the next generation's required 100 Gbaud performance.

7.3 Conclusion

Coherent links that are optimized for the energy-efficiency and cost requirements of the high-volume data center market have a promising future. Optical switching network deployment is already underway, and has demonstrated concrete, significant power and cost savings from replacing power-hungry electronic switches in the network. But the low-latency and dynamic reconfigurability offered by these networks can lead to increased compute resource utilization and substantial overall data center efficiency improvements. This must be supported by optical links with expanded link budgets that tolerate the additional losses from the optical switches themselves. Redesigning coherent links for short-reach applications inside data centers will be crucial to scaling these high link budget interconnects as data rate requirements continue to rise. The results presented here

validate the potential of these low-power coherent link technologies for making energy-efficient intra-data center coherent links with high link budget.

Appendix A

Simulation Methods

A.1 HFSS Simulation for TW-MZMs

Accurately predicting the performance of a novel travelling wave Mach-Zehnder Modulator (TW-MZM) design is a non-trivial task, and great care must be taken in simulating and modelling such devices. As described in Chapter 5, the first design iterations of TW-MZMs in new processes tended to miss their impedance or bandwidth targets. This was caused by some combination of unknown phase shifter junction capacitance values, and poor modelling of the RF performance of the electrodes and junctions. The aim of this appendix is to articulate and outline improved TW-MZM simulation methods for RF performance modelling.

High Frequency Structure Simulator (HFSS) was used to measure coplanar waveguide (CPW) TW-MZM structures. Driven Terminal wave ports were used, and the HFSS S-parameter simulation results (the common mode, for the case of CPW structures used here) can then be converted to transmission line per length RLGC model, propagation constant, and characteristic impedance using the relationships defined in equations 12-18 in [57].

Especially for the novel TW-MZM structures described in Chapter 5 that leveraged the full metal stack routing capabilities of integrated CMOS and silicon photonic processes, it is important to include the full metal structure in the HFSS model. While it may be possible to simulate the standalone CPW electrodes in HFSS, and use theoretical analysis such as is outlined in [58] to account for the loading effect of the phase shifter segments, in practice it is important to fully model the RF effects of the phase sections and accompanying metal traces. The metal and doped-semiconductor regions used to connect the pn-junction phase shifter to the travelling wave electrodes necessarily contribute parasitic capacitance, and the geometry, pitch, and spacing of ground straps connecting different electrodes or VNCAP structures providing decoupling capacitance all affect the overall performance of the device. Thus, for periodically loaded TW-MZMs, it is important to simulate multiple segments, if not the entire length of the modulator, to capture the full characteristic impedance of the line any effects of segment-to-segment coupling. Finally, if all of these metal and semiconductor structures are included in the model, the junction itself must be physically modelled and present an appropriate capacitance and series resistance.

These requirements present challenges with calibrating the simulation model to match the characteristics of the actual device. In our work, we measured the capacitance of different lengths of test structures to extract hardware junction capacitance values under different junction bias conditions. These measured junction capacitance values inherently include static pad and metal routing capacitance, which can be extracted with a capacitance per unit length regression, but the resulting capacitance will still include parasitic capacitance of any metal or doped regions that continue to scale with the junction as its length changes. In order to calibrate the HFSS model, then, 4 separate terms need to be accounted for, with the total written as:

$$C_{total} = C_{electrodes} + C_{connections} + C_{junction} + C_{parasitics} \quad [pF/m]. \tag{A.1}$$

The CPW electrode contribution, $C_{electrodes}$, can be simulated in the unloaded case without any phase shifter loading, and $C_{parasitics}$ can be excluded for initial calibration, but the combination of metal and doped semiconductor routing between the electrodes and the pn-junctions ($C_{connections}$) and the junction itself ($C_{junction}$) need to be calibrated to the junction depletion region geometry used in the HFSS simulation. In the absence of accurate junction doping process and depletion region simulations, a simple parallel plate model based on the known ridge geometry can be used, where $C_{junction} \approx A/w_{depl}$ and A is some constant. By sweeping the modelled depletion width geometry, w_{depl}, the capacitance contributions of the junction and accompanying metal and doped connections can be calibrated to measured performance for various junction bias points. Finally, once the junction capacitance contribution is calibrated, effects of additional parasitic elements and metal routing can be confidently introduced and modelled.

Once an HFSS model of a TW-MZM has been calibrated to measured hardware performance, it can be used to predict high speed performance under various potential design optimizations. An important consideration is the chosen parameter or set of parameters used to guide the optimization process. For TW-MZMs, there are any number of candidate specification targets, such as the, capacitance per length, inductance per length, bandwidth, frequency response, impedance, group index, length, and size, and many of these can vary strongly with the choice of junction bias voltage. The optimization problem can be significantly constrained if one can select a specific target bandwidth, typically related to the target modulation symbol rate (eg. roughly 30 GHz for 50 Gbaud modulation). The simulated propagation constant can be used to determine the maximum

modulator length to meet the target bandwidth. As discussed in [59], the -6.34 dB point in the electrical TW electrode frequency response will correspond to the -3 dB BW for the EO frequency response, due to the interaction of the increasingly-bandwidth-limited voltage signal with the optical phase shifters along the TW-MZM structure. Further BW degradation due to velocity mismatch can be calculated from the simulated propagation constant, following the relationships established in [60] and [59].

The characteristic impedance of the modulator can be used to calculate the expected driver output voltage swing, and, combined with the phase shifter efficiency and modulator length, used to calculate the expected effective optical loss through the modulator, as described in Chapter 3. The static waveguide and phase shifter optical losses for the simulated target MZM length can also be incorporated and added to this number. In this manner, all of the relevant performance parameters for the TW-MZM can be combined into a single quantitative number for the optical loss through the IQ-TW-MZM, which can then be minimized during optimization. This framework is useful for optimizing the TW-MZM component within an HFSS simulation. Resulting candidate device performance can then be incorporated into holistic time-domain link simulations for further analysis and optimization, as described in Chapter 5.

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