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J. Ding
(M.S. Thesis)

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TABLE OF CONTENTS

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ABSTRACT

Ohmic contacts to n-GaAs formed by the heat treatment of In films have been studied previously. However, many of the fundamental relationships between processing and microstructure remain essentially unknown. In order to improve the electronic properties of the In/GaAs contact, it is necessary to understand the effect of the surface condition of the substrate, and the heat treatment on the interface structure and reactions.

In this study, the interface morphologies of the In/GaAs heterojunction with and without a thin (1 ~ 2 nm) intervening native oxide layer have been studied before and after annealing at 350°C by scanning electron microscopy, transmission electron microscopy and diffraction, energy dispersive spectrometry of x-rays and cross-sectional high resolution transmission electron microscopy. The results from these techniques were combined to provide a detailed description of the structural evolution of the In/GaAs heterojunction and the effect of the intervening oxide on the In/GaAs reaction.

The SEM and TEM images revealed the surface morphologies of the as-deposited indium on the GaAs substrate with and without the intervening oxide. Epitaxial indium islands were formed on the

oxide-free substrate with the orientation relationship $[0\bar{1}1]_{GaAs} \| [1\bar{1}\bar{1}]_{In}$, $(200)_{GaAs} \| (110)_{In}$. This morphology was explained by considering the surface energy of indium and the reduction in interfacial energy due to epitaxy. Instead of a graded heterojunction, an abrupt interface was found between the epitaxial phase $In_{1-x}Ga_xAs$ formed after annealing and the GaAs substrate. The results also showed that the native oxide on the substrate disrupts the orientation relationship at the In/GaAs interface, and greatly inhibits the In/GaAs reaction at 350°C.

1. INTRODUCTION

1.1 Objective

The recent development of GaAs devices has shown them to have a promising future in both high speed and optoelectronic applications. As GaAs device technology reaches toward maturity, the need for low resistance, reproducible, stable and reliable ohmic contact becomes increasingly important. During the past decade, a number of detailed studies of ohmic contacts to III-V compound semiconductors, especially to n-GaAs, have been undertaken.

A recent report by Lakhani[1,2] shows that ohmic contacts to n-GaAs can be formed by the heat treatment of indium films evaporated onto GaAs substrates. Lakhani observed a low density of isolated rectangular islands which consisted of graded $In_{1-x}Ga_xAs$ heterojunctions. He attributed the ohmic characteristics of this contact to conduction through these isolated islands. Most of the surface, however, remained unreacted, due presumably to an intervening oxide layer originally formed on the GaAs substrate surface prior to In deposition. Unfortunately, the detailed microstructures of the heterojunctions, the surface morphology and the effect of the oxide at the interface have not been investigated. In this investigation, scanning, transmission and analytical electron microscopes have been employed in an effort to obtain a better understanding of the interface structure and contact morphology at the near atomic scale.

1.2 Ohmic Contacts

Semiconductor devices and specimens used for the measurements of semiconductor parameters require ohmic contacts through which the connection to the outside world can be made. "Ohmic" contacts between a metal and a semiconductor are defined as those which exhibit linear current-voltage characteristics. The most important feature for such contacts is that the voltage drop across them is negligible compared with the voltage drop across the device, so that the contacts do not affect the I-V characteristic. In principle, such a contact can be formed by using a metal with a work function less than the work function of the n-type semiconductor or greater than that of the p-type semiconductor. However, there are very few metal-semiconductor combinations which satisfy these conditions due to the presence of surface states and defects in the semiconductor near the interface. These surface states pin the Fermi-level near the middle of the energy band gap. Therefore, the vast majority of ohmic contacts involve a thin layer of very heavily doped semiconductor immediately adjacent to the metal, so that the depletion region is thin enough so that the carriers can easily tunnel through it. This heavily doped layer may be formed separately prior to the deposition of the metal contact or it may result from the deposition and subsequent heat treatment of an alloy containing an element which acts as a donor or acceptor. Recently, graded heterojunctions of the type $In_{1-x}Ga_xAs$ $(0 \leq x \leq 1)$ have been grown by Molecular Beam Epitaxy (MBE).[3] As discussed in Sec.

1.3.2, these graded structures overcome the problems related to Fermi-level pinning at the GaAs surface.

1.2.1 Band Structure

According to the Schottky-Mott model, when a metal is brought into intimate contact with a semiconductor, the ohmic or rectifying nature of the contact depends on the work functions ϕ_m and ϕ_s of the metal and the semiconductor, respectively. The barrier height ϕ_B is equal to the difference between the metallic work function ϕ_m and the electron affinity X_s of the semiconductor.

$$\phi_B = \phi_M - X_s \tag{1}$$

This point is illustrated in Fig. 1 which shows the metal/n-type semiconductor energy band diagrams both before [Fig. 1(a,c)] and after [Fig. 1(b,d)], the establishment of thermal equilibrium. In most practical metal-semiconductor contacts, the ideal situation shown in Fig. 1(b,d) is never reached because there is usually a thin insulating layer of oxide about 1 ~ 2 nm thick on the surface of the semiconductor. Such an insulating film is often referred to as an interfacial layer. Under the assumptions that there are no surface states and that the surface dipole contributions to ϕ_m and X_s do not change when the metal and the semiconductor are brought into contact (or, at least, their difference does not change), the practical contact is therefore more likely to be that shown in Fig. 2(a). However, the barrier presented to electrons due to the oxide layer is so narrow that electrons can tunnel through it quite easily, and the case

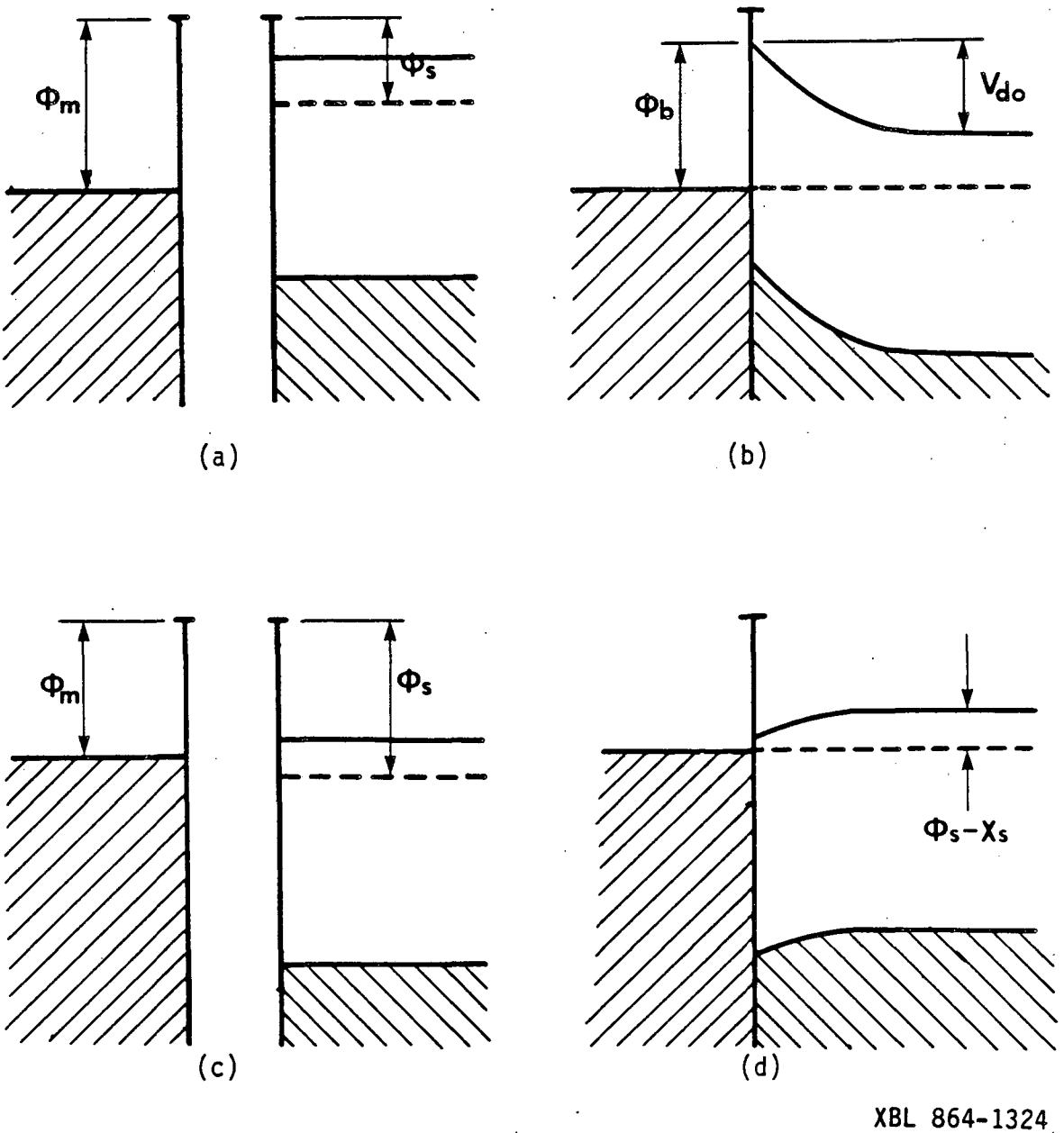
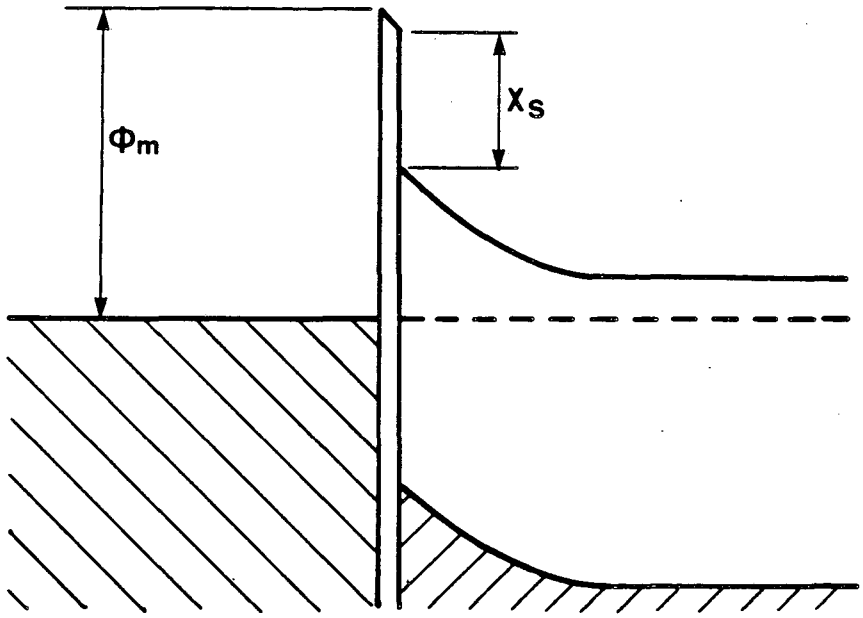
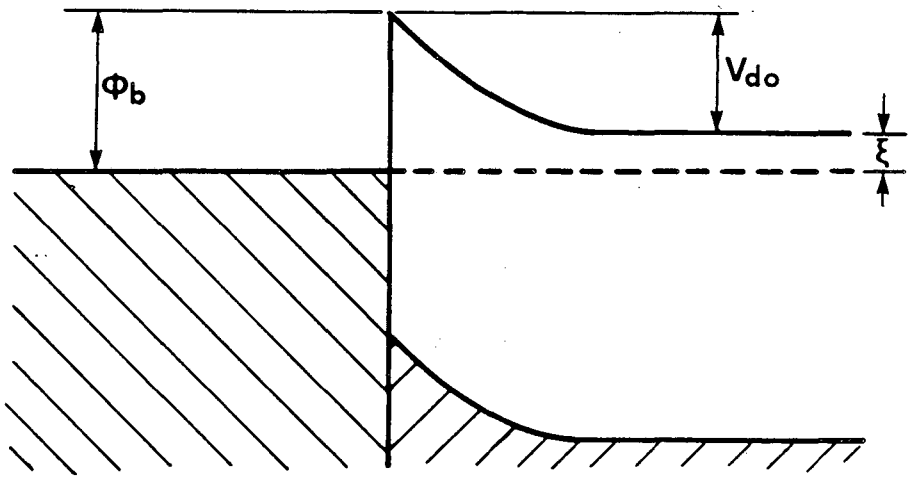


Fig. 1. The ideal metal n-type semiconductor band diagram for $\phi_m > \phi_s$ (a) before contact, (b) after contact, and for $\phi_s > \phi_m$ (c) before contact, (d) after contact, where ϕ_m and ϕ_s are the work functions of metal and semiconductors, respectively. X_s is the electron affinity of semiconductor. ϕ_B and V_{do} are the barrier height and diffusion potential of electrons (carriers), respectively.



(a)



(b)

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Fig. 2. Band diagrams for a metal and an n-type semiconductor (a) a thin insulating layer of oxide about 1 ~ 2 nm thick at the interface. (b) ideal Schottky contact, where ξ is the energy difference between the Fermi-level and the bottom of the conduction band.

shown in Fig. 2(a) is almost indistinguishable from the ideal case [Fig. 2(b)] as far as the conduction electrons are concerned. Moreover, the potential drop V_i in the oxide film is so small that the equation (1) is still a good approximation.[4-6]

Experimental evidence has not, however, borne out the relationship of Eq. (1). Metal-semiconductor barriers have been found to exhibit weak or no dependence at all on the metallic work function. An explanation of this weak dependence on ϕ_m was put forward by Bardeen,[7] who suggested that the discrepancy may be due to the effect of surface states; that in thermal equilibrium there exists a barrier even at the free surface of a semiconductor. If the surface state density is high, this barrier can be pinned to its free surface value after subsequent contact to a metal. Energy band diagrams relating to the formation of the Bardeen barrier are shown in Fig. 3. Equation (2) represents the limiting form of the Bardeen theory for a high density of surface states such that ϕ_B is independent of the metallic work function ϕ_m

$$\phi_B = E_g - \phi_o \qquad (2)$$

where E_g is the energy gap of the semiconductor, and ϕ_o is the neutral level which characterizes the continuous distribution of surface states present at the semiconductor surface. More recent models ascribe the formation of Schottky barriers to "metal-induced gap states",[8] or to defects like anion clusters[9] or point defects[10] near the interface.

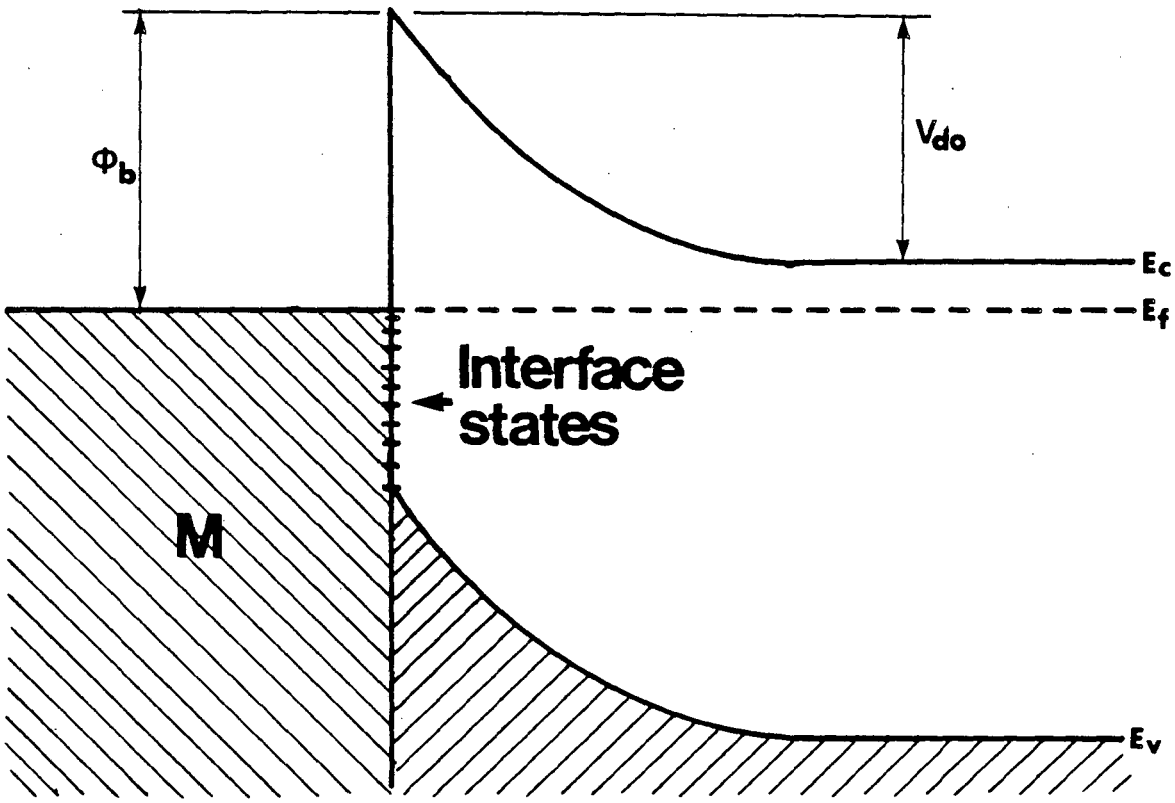

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Fig. 3. The equilibrium band structure at the metal-semiconductor interface containing a high density of interface states.

1.2.2 Carrier Transport Mechanisms

Experimental studies of metal-semiconductor contacts have shown that most of the metal-semiconductor combinations form depletion layer contacts (usually rectifying or blocking). The conduction properties of such contacts are determined by the actual transport mechanism. Electrons can be transported across a metal-semiconductor junction in various ways. Figure 4 shows schematically electron transport mechanisms under forward bias for an n-type semiconductor. The inverse processes occur under reverse bias. The mechanisms are:

(a) emission of electrons from the semiconductor over the top of the barrier into the metal;

(b) quantum-mechanical tunneling through the barrier;

(c) recombination in the space-charge region;

(d) recombination in the neutral region (hole injection).

The dominant mechanism of current flow depends primarily on temperature, barrier height, dopant concentration profile, the effective masses of the charged carrier and the dielectric constant. Besides, several other factors such as the presence of interfacial layers or the stoichiometry of the semiconductor surface influence the transport mechanism. At room temperature, and for a relatively light to moderate doping level ($N_{D,A} < 10^{18}$ cm^{-3}), the dominant mechanism for current transport across a metal-semiconductor interface is thermionic emission[11] of carriers over the top of a barrier. In the case of a very heavily doped (degenerate) semiconductor, it is possible for electrons with energies lower than the top of the barrier to penetrate the bar-

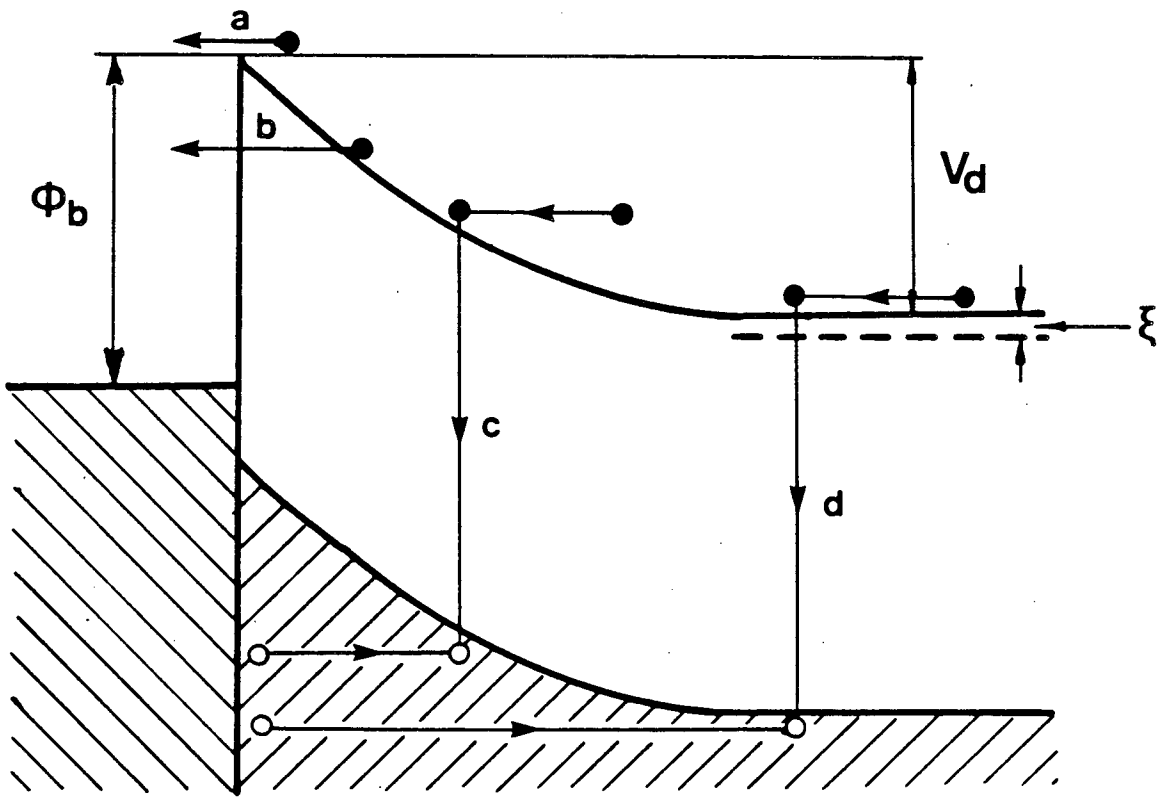

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Fig. 4. Transport processes in a forward-biased Schottky barrier on an n-type semiconductor. (a) emission of electrons from the semiconductor over the top of the barrier into metal; (b) quantum mechanical tunneling through the barrier, and recombination in (c) the space charge region and (d) the neutral region. (From Ref. 4)

rier by quantum-mechanical tunneling. This may modify the thermionic process in one of the two ways shown in Fig. 5. At low temperature, electrons with energies close to the Fermi-energy in the semiconductor tunnel through the barrier. This is known as "field" emission.[12,13] By increasing the temperature, electrons are excited to higher energies at which they "see" a thinner and lower barrier. Therefore, the tunneling probability is increased very rapidly. This process is known as "thermionic-field" emission.[14] If the temperature is raised still further, all of the electrons can obtain enough energy eventually to go over the top of the barrier. In other words, the thermionic emission mechanism becomes dominant.

For example, if an abrupt metallurgical transition between a metal and a nondegenerate semiconductor forms a rectifying Schottky barrier junction with thermionic emission as the dominant conduction mechanism, then by increasing the doping concentration, even though the barrier height ϕ_B remains essentially the same, the barrier width decreases with the square root of the doping concentration and thermionic-field emission starts to dominate. Finally, at very high doping levels, the barrier width becomes so narrow that field-emission tunneling is dominant. The contact starts to behave like an ohmic contact when the contact resistance reaches a sufficiently small value. Consequently, the study of ohmic contact formation according to Schottky's theory is reduced to the study of conditions under which the "impedance" of the Schottky barrier is low. Two current transport mechanisms, i.e., thermionic emission and field emission (tunneling), correspond respectively

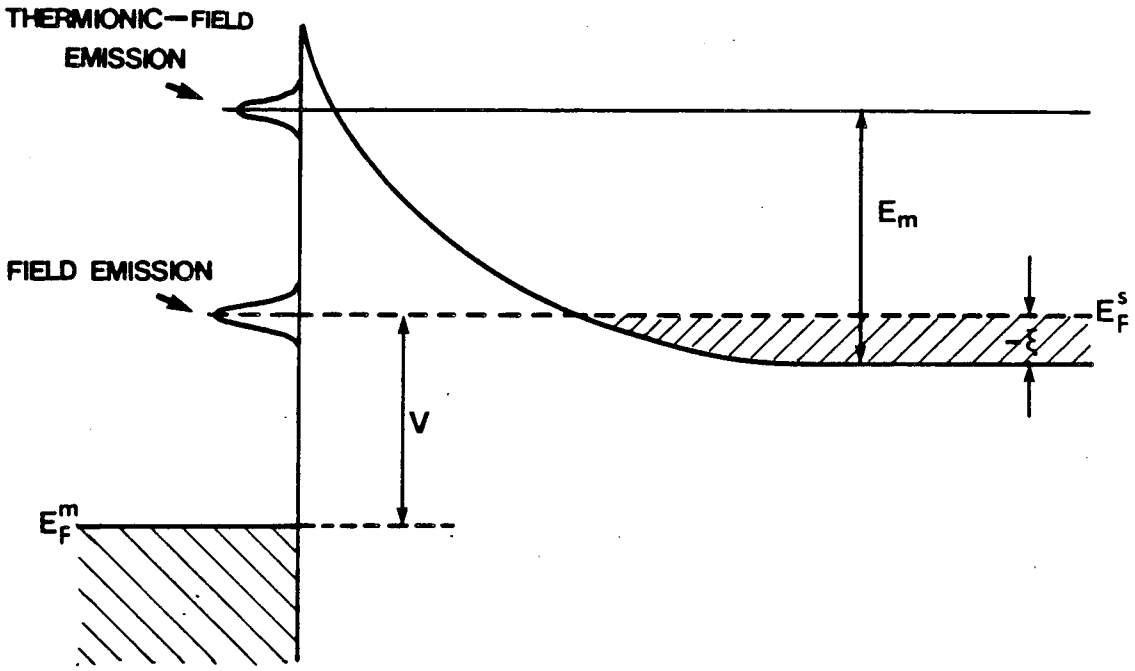

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Fig. 5. Field and thermionic-field emission under forward bias. The diagram refers to a degenerately doped semiconductor for which ξ is negative. (From Ref. 47)

to the two major empirical ways of fabricating ohmic contacts: (1) choose a metal which makes a low Schottky barrier with semiconductor or (2) dope the semiconductor heavily near the contact so that the barrier will be thin enough to be easily penetrated by tunneling.

1.3 Ohmic Contacts to GaAs

Low resistance ohmic contacts are essential in the formation of GaAs devices, particularly for the demands of high frequency operation and/or small device geometry required in microwave diodes and transistors. It is well known that low resistance ohmic contacts to n-GaAs are difficult to fabricate since the large density of surface states present under ordinary processing conditions pins the Fermi-level near mid-gap so that deposition of most metals onto a cleaned n-GaAs surface results in Schottky barriers with barrier heights of about 0.8 eV. Spicer et al.[15] have suggested that these surface states are induced by the interaction of either metal or oxygen with the GaAs surface, and by the surface native defects, e.g., arsenic and gallium vacancies or antisite defects. Due to this pinned Fermi-level, the fabrication of an ohmic contact to n-GaAs requires the formation of a thin n^{++} layer or an intentionally grown heterojunction between the metal contact and the bulk semiconductors. A highly doped layer is expected to permit electrons tunneling between the metal and the semiconductors resulting in lower I-V characteristics. It is also possible to fabricate a graded heterojunction to decrease the barrier height to a negligible value, creating what might be called an "ohmic heterojunction contact" (discussed in Sec. 1.3.2).

1.3.1 Alloyed Ohmic Contacts

The earliest contacts to GaAs were made with Sn, alloyed at ~450°C.[16,17] However, this contact tended to be laterally nonuniform, and the tin proved to be a fast diffuser under applied field, tending to form conducting channels. Braslau et al.[18] introduced an evaporated AuGe eutectic (88 wt% Au - 12 wt% Ge) with a Ni overlayer, alloyed at a temperature greater than the eutectic temperature, which overcame these problems and has become a very widely used technique for contacting n-GaAs. A specific contact resistance as low as $r_c = 1.5 \times 10^{-6} \Omega cm^2$ has been achieved for a doping concentration $N_D = 5 \times 10^{16}$ cm^{-3}.[19] Since all components of the AuGeNi system play an active role in ohmic contact formation and performance, the relative thicknesses of the metallic layers are of primary importance. Germanium, a group IV element, is used as an n^+ dopant and acts as a donor in GaAs when it occupies Ga sites. Au-Ge was originally chosen for its low eutectic melting temperature (360°C), and for the low resistivity ρ, high corrosion and oxidation resistance and ductility of Au. Since Au acts as a selective getterer for the Ga,[20-22] the amount of gold is very important for providing sites for Ge. When too much Au is present, however, the non-stoichiometric conditions below the interface form a region of high resistivity and degrade the ohmic contact properties. Moreover, during contact formation, the amount of Au influences the amount of GaAs consumed. Ni is used to improve wetting and enhance a driving force for Ge diffusion.[23,24] The amount of Ni influences both the morphology and electrical properties as well

as the contact reliability. The optimum Ni thickness has been defined in each laboratory depending on the technology employed. As a matter of fact, the alloyed technology of contacts is still only poorly controllable.

Through a large number of studies over the past several years, a fairly complete picture of the alloyed region has been obtained by using Auger electron spectroscopy, x-ray diffraction, transmission electron microscopy and other techniques. Germanium and nickel penetrate deeply but non-uniformly into GaAs, leaving grains of germanium-rich material together with Au-Ga regions at the interface with GaAs.[25] The assumption has been made that the interface consists of ohmic regions where germanium accumulates, and other areas of the interface still are barriers of some kind. Current will flow through the matrix of these low-resistance regions in the interface. Therefore, the contact resistance will be determined by the combination of the true contact resistance in these sub-micron regions, in series with the spreading resistance in the doped semiconductor.[26] This is shown schematically in Fig. 6. A correlation between the interface structure and the contact resistance was found by Kuan et al.[27] In this study, the interface structures resulting from the alloying reactions between a Au/Ni/Au-Ge composite film and a (100) GaAs substrate were studied by transmission and scanning electron microscopies.

Having gained wide acceptance over the past years, the art of forming alloyed AuGeNi ohmic contact to GaAs has reached the stage where it is reasonably reproducible and compatible with device

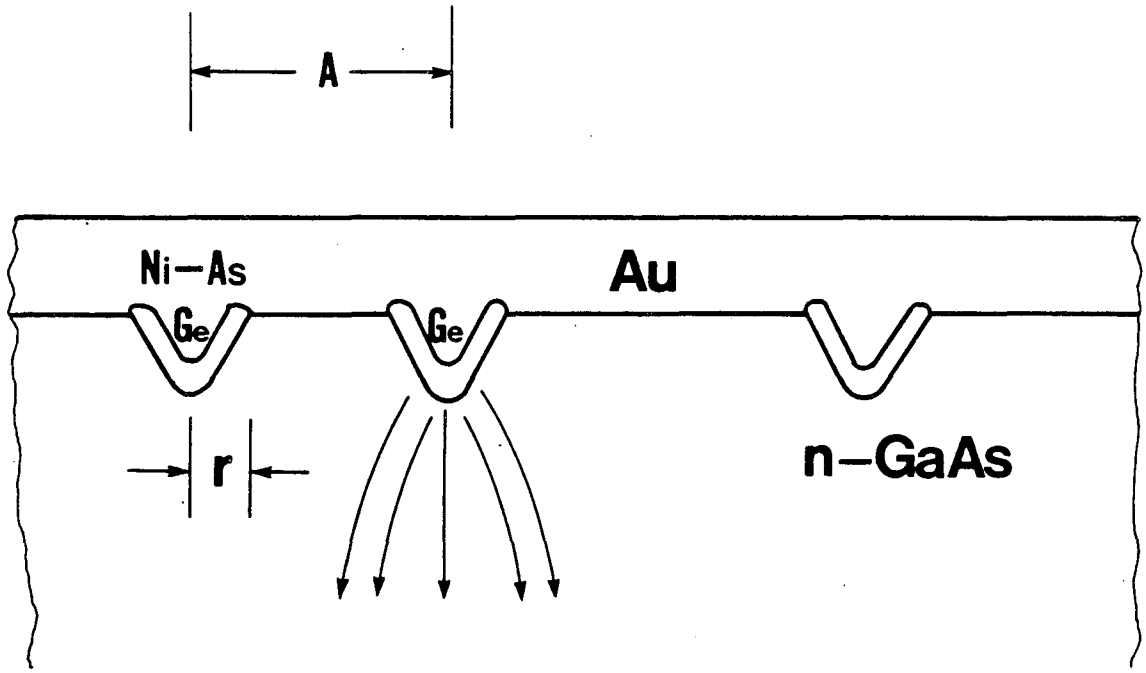

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Fig. 6. Suggested model of an alloyed ohmic contact to GaAs. Conduction is through a parallel array of germanium-rich protrusions of negligible contact resistance ($(r_c)_{meas} \approx \langle A \rangle^2(\rho_n/\pi\langle r \rangle + r_c/2\pi f\langle r \rangle^2)$ for $f \gg 1$, where f is a field enhancement factor for field emission for protruding electrodes and ρ_n is the resistivity of the n-GaAs) compared with the spreading resistance in series with them. (From Ref. 23)

processing and yields an acceptable contact resistance for most purposes. But its long-term reliability is a weak point and the spatial inhomogeneity of the interface will become a serious drawback as device dimensions shrink with the development of large-scale integration in GaAs. Due to the unsuitability of this irregular morphology for modern devices and its insufficient reproducibility, many other techniques have been proposed and explored, e.g., non-alloyed or sintered contacts, ion-mixed contacts and "graded" heterojunction ohmic contacts. In the next section, this latter approach, the graded heterojunction ohmic contact, will be described in detail.

1.3.2 Graded Heterojunction Contacts

The phenomenon of Fermi-level pinning at the midgap for GaAs surfaces is currently dealt with by using heavily doped alloyed ohmic contacts for discrete and monolithic devices. New contacting techniques including the use of lattice-matched heterojunctions, non-alloyed n^{++} and p^{++} surfaces, graded band gap structures and special surface treatment prior to metallization promise to provide both greater flexibility and greater control for future applications.

An approach to improving the "contactability" in some special cases is the formation of a graded crystalline layer of a mixed semiconductor between the contact-metal system and the semiconductor. In fact, model calculations for graded heterojunctions have shown that for thick graded layers the barrier height decreases to a negligible value and ohmic heterojunctions are formed.[28-30]

The technique for forming graded heterojunction ohmic contacts to GaAs utilizes the fact that for InAs surfaces, Fermi-level pinning occurs at or in the conduction band.[31,32] InAs, with its small band gap (0.36 eV) and Fermi-level pinning at or in the conduction band, can easily form an ohmic contact with most deposited metal films. Figure 7(a) shows the "conventional" metal-GaAs contact with ϕ_B = 0.8 eV. In order to make an "ohmic" contact, it is necessary to form an n^+ layer between metal and n-doped semiconductor. Figure 7(b) shows the analogous situation for the metal/n-InAs contact. In this case, the Fermi-level is pinned in the conduction band. Thus, there is no barrier ϕ_B to electron flow and the contact is ohmic. This indicates that tunneling is not required, and low-resistance contacts can be formed for a wide region of n-type doping levels without the need for n^{++} layer formation. From this result, one might conclude that an ohmic contact for GaAs can be formed by using the structure M/n-InAs/n-GaAs. This is shown in Fig. 7(c). Note that the Fermi-level E_F is pinned at the same position as for the metal/GaAs case, which results in a positive barrier ϕ_B between n-InAs and n-GaAs. This band structure will form a rectifying or tunneling ohmic contact, depending on the doping level. This may be due in part to the large lattice mismatch(7%) between GaAs (lattice parameter a_o = 5.65 Å) and InAs (a_o = 6.06 Å). This large lattice constant discontinuity can result in a large density of misfit dislocations at the interface which, in turn, pin the Fermi-level in both GaAs and InAs.[33] Other reasons for rectifying behavior may be a large con-

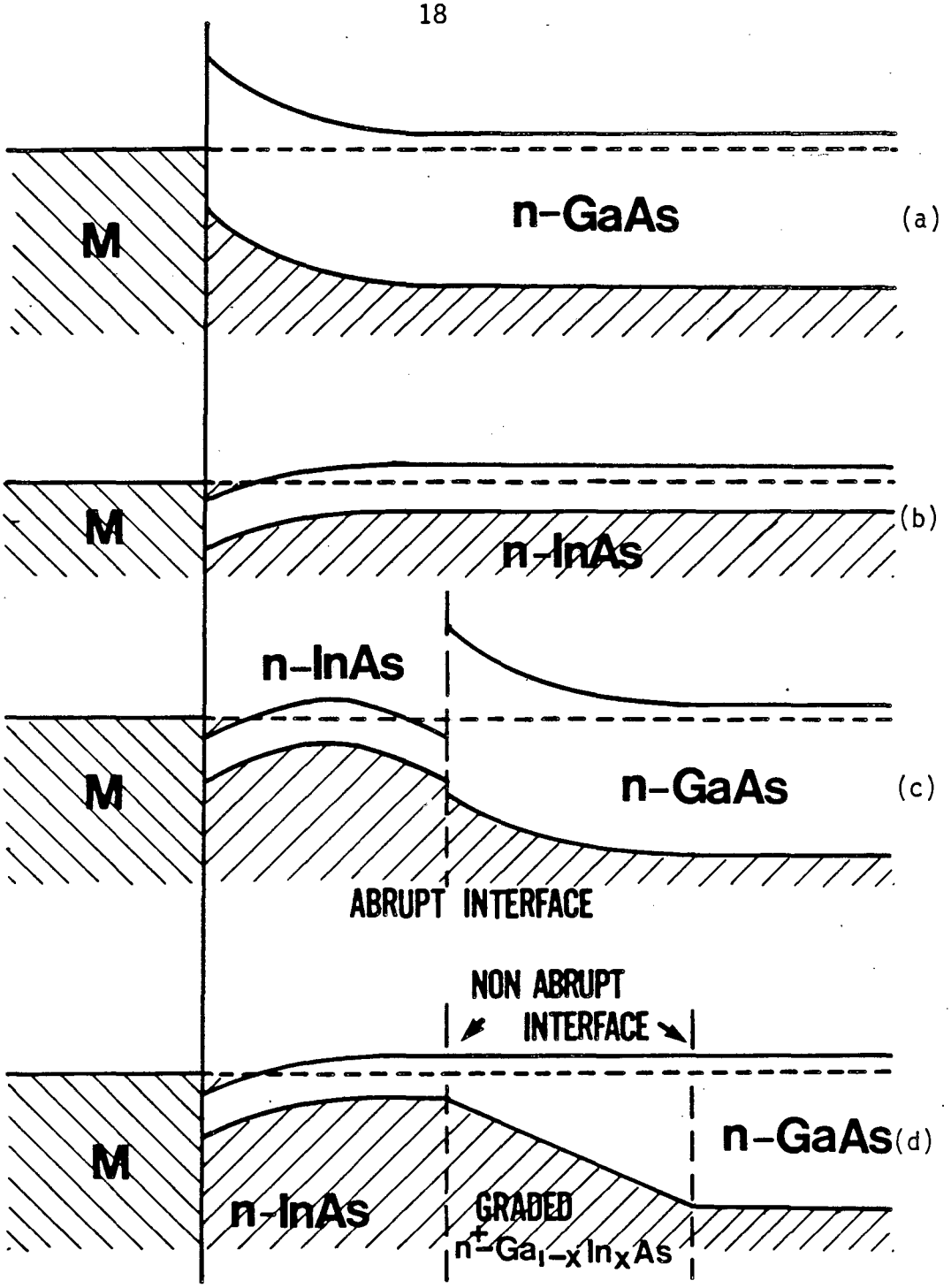

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Fig. 7. Band bending diagram for various semiconductor interfaces: (a) metal on n-GaAs; (b) metal on n-InAs; (c) metal on n-InAs/n-GaAs; (d) metal on n^+-InAs/graded n^+-$In_{1-x}Ga_xAs$/n-GaAs. (From Ref. 3)

duction band discontinuity across the interface, and a "dirty" GaAs surface condition prior to epitaxial growth. To overcome these problems, a non-abrupt interface is formed by grading the interface region $In_{1-x}Ga_xAs$ in composition from x = 0 at InAs interface to x = 1 at the GaAs interface. The solution to this problem is shown in Fig. 7(d). Due to the fact that there are no abrupt discontinuities in the conduction band, and that ϕ_B is ≤ 0 for the M/n-InAs contact, this structure is expected to form non-alloyed low resistance contacts. Misfit dislocations, if present, are distributed and result in a reduced barrier action. J.M. Woodall et al.[3] have fabricated this structure by using Molecular Beam Epitaxy (MBE) to grow a graded band gap layer of $In_{1-x}Ga_xAs$. A low contact resistance, $< 10^{-6}\,\Omega\,cm^2$, has been obtained for a Ag/n-$In_{1-x}Ga_xAs$/n-GaAs MESFET structure. Unfortunately, the ultra high vacuum requirement for MBE may not be practical for large-scale device fabrication.

Recently, Lakhani[1,2] reported the formation of indium-based ohmic contacts to n-GaAs using only conventional vacuum levels ($> 10^{-7}$ torr). The result shows that a graded heterojunction ohmic contact results from annealing an indium film on a GaAs substrate at 350°C. The interface reaction, however, is highly localized. During the heat treatment, a low density of isolated rectangular islands are formed. It is believed that the ternary semiconductor $In_{1-x}Ga_xAs$ ($0 \leq x \leq 1$) is formed in the reacted rectangular regions. These islands are typically 5 μm wide and 10 μm long, and are aligned along the <110> family of directions on the (100) surface of the GaAs

substrate. The unreacted regions are thought to be caused by oxide on the GaAs surface. In principle, a graded heterojunction layer of $In_{1-x}Ga_xAs$ on GaAs should result in extremely low specific contact resistivity. However, the measured value ($1.2 \times 10^{-5}\ \Omega cm^2$) is much higher than that expected ($< 10^{-6}\ \Omega cm^2$). This may be due to the fact that the isolated islands, i.e., "graded heterojunction regions," cover only a small fraction of the total area of the "contact" surface. The non-uniformity, with the graded heterojunction forming only in the isolated regions on the contact surface, was believed to be responsible for the measured contact resistivity being larger than has been reported[3] for MBE grown InGaAs heterojunctions ($R_c \leq 10^{-6}\ \Omega cm^2$).

2. EXPERIMENTAL METHODS

2.1 Heterojunction Fabrication

2.1.1 Thin Film Deposition

In order to obtain suitable TEM specimens for the studies of surface and interface morphologies and orientation relationships between the GaAs substrate and the thin films, a very thin indium film is necessary. Molecular Beam Epitaxy has been used to satisfy this requirement because of the possibility of accurate thickness control.

In this investigation, LEC semi-insulating GaAs wafers were used as substrates. The polished wafers had an orientation of (100). In the case of MBE deposition, the samples were divided into two groups, one with the native oxide, another with an oxide-free surface. The samples were prepared by the following processes. After the substrates were degreased by boiling in chloroform, acetone and methanol twice for five minutes each time, respectively, they were etched with concentrated HCl for two minutes. Before swabbing the surface with H_2SO_4, the substrates were cleaned again in methanol by boiling twice for five minutes each time. Finally, the substrates were rinsed in deionized water and blown dry with nitrogen gas. These wafers were divided into two groups: one ready for deposition, another group was to have the native oxide desorbed prior to deposition of In. The wafers from the second group were loaded into the MBE vacuum chamber. The temperature was increased up to 600°C in approximately 10 minutes under ultra high vacuum conditions. The native oxide on the surface

of the substrate was desorbed at 600°C without an arsenic flux impinging on its surface. The RHEED pattern showed an arsenic stabilized surface after the oxide desorption. Following the oxide removal, the substrate was allowed to cool to 25°C (approximately 30 min.). Indium was then deposited onto the rotating substrate (8 RPM) for 10 minutes with a deposition rate of 5.7 nm/min. under a vacuum of 3.2×10^{-9} torr. The identical conditions were used for the deposition of In onto the chemically cleaned samples. As will be shown below, the native oxide layer on the substrate which was not subjected to a desorption heat treatment was ~1.3 nm thick.

2.1.2 Annealing

In order to investigate the effect of the native oxide on the interface reaction and the reacted interface structures, furnace annealing was carried out at 350°C for 10 minutes. All specimens were annealed in an atmosphere of flowing forming gas (95% Argon, 5% Hydrogen) under the same conditions.

2.2 TEM Specimen Preparation

2.2.1 Plan-View Specimens

Specimens were prepared by cleaving several pieces (~2 x 2 mm) from each wafer. Wax was used to mount each of these specimens on a 30 mm diameter glass disk with the indium-deposited surface facing down. In order to avoid melting the indium film when the specimen was put into the molten wax on the glass disk, the glass disk was taken off the hot plate, then cooled until the wax was viscous (~80°C) before the specimen was placed on the disk. Larger pieces of silicon were

mounted around the specimen so that the edges could be preserved during mechanical thinning. The specimen then was mechanically polished from the unprocessed side on a rotating wheel with 1200 mesh emery paper until its thickness approached 60 μm. The final polishing was done by using 0.05 μm gamma alumina on a micropolish cloth until the protecting silicon pieces were transparent (brown color). The specimen was separated from the glass disk by dissolving the wax in a beaker of acetone. The solvent was poured into a second beaker and a stream of acetone was used to gently wash the specimen onto filter paper.

Each mechanically thinned specimen was mounted on a 3 mm circular-hole copper grid by epoxy (Devcon "two ton" epoxy works well) with the processed surface facing the grid. The specimen then was glued on a teflon holder by using a protective lacquer with the copper grid facing down. The edges of the specimen were also protected by painting with the same lacquer. After drying the lacquer (25-30 minutes in air or 10 minutes in an oven at 50°C), the holder was set into the chemical jet polishing assembly. The specimen was jet polished from the unprocessed side using a freshly prepared solution with ~3% chlorine in methanol (prepared by bubbling Cl_2 gas through CH_3OH just prior to the etching). The flow rate, the strength of the solution, and the distance between the jet and the specimen influence the etching (thinning) rate. The specimen had to be observed frequently under an optical microscope at low magnification in order to monitor the thinning. Etching was terminated as soon as a hole appeared in the thinned area.

The specimen then was removed from the teflon holder by dissolving the lacquer in acetone.

2.2.2 Cross-Sectional Specimens

Pieces of the processed specimens (2 x 5 mm) were cleaved from the samples along the <110> cleavage directions. After cleaning with acetone, two pieces were glued face to face with epoxy. This was done to attain better mechanical strength and facilitate handling, and also for the protection of the processed surfaces. This GaAs specimen assembly was allowed to stand for 24 hours for a complete drying of the adhesive. It was then mounted onto a 30 mm diameter glass disk with wax which allows the specimen to be thinned in the <110> GaAs directions. The same attention was paid to the process of mounting the specimen on the glass disk as for the plan-view sample. Two pieces of silicon were mounted on both sides of the assembly to protect the edges of the specimen. Note that an increasing viscosity of the wax was again the condition used for the specimen assembly.

The assembly was polished flat using 1200 mesh emery paper down to 1.5 mm. The final polishing was accomplished with 0.05 μm gamma alumina powder on a micropolish cloth with a rotating wheel. This polishing procedure was repeated on the other side of the specimen until a final thickness of between 20 and 80 μm was achieved. In order to facilitate uniform thinning, care was taken to ensure that the specimen was in good contact with the glass disk along its entire length. The same processes were repeated to remove these specimens.

Finally, the specimens were glued to a copper grid (3 mm diameter) for support and ease of handling. Subsequent thinning was performed in an ion milling machine with a liquid nitrogen cold stage. The thinning conditions were set at 14° specimen tilt, 4 KeV accelerating voltage and 0.5 mA argon ion (Ar^+) beam current for two guns. In order to limit the effects of ion beam heating, the specimen stage was cooled in liquid nitrogen for 30 minutes prior to milling.

2.3 Electron Microscopy Investigations

The electron microscopy studies of the surface morphology, heterojunction interface structures and the orientation relationships between the thin films and the substrate were carried out using plan-view and cross-sectional specimens. The ISI DS 130 scanning electron microscope was used to study the surface morphology of the specimens. Conventional TEM studies of the interface structures and orientation relationships were performed in a Philips EM 301. Energy dispersive x-ray spectra (EDS) were acquired with a Kevex model 7000 spectrometer on a Philips EM 400 electron microscope. A JEOL 200CX transmission electron microscope equipped with an ultra-high resolution pole piece was employed for the cross-sectional work to obtain more detailed images of the interfaces.

Several specimens from each sample were studied in both plan-view and cross-sectional geometries in order to make an unambiguous determination of the film morphology. A GaAs standard was used for partial quantification of the EDS spectra.

2.4 Quantitative Microanalysis

The compositions of the reaction products after annealing at 350°C were estimated by application of the EDS technique to cross-sectional samples. Proportionality factors were determined for quantitative microanalysis. The proportionality factor Kx/y relates the height ratio Hx/Hy of the x-ray peaks (proportional to the total counts or intensities for Gaussian distribution peaks) to the concentration ratio [X]/[Y] of the elements X, Y. This relationship between the concentration ratio and the peak height ratio is expressed as:

$$[X]/[Y] = Kx/y \cdot Hx/Hy$$

Employing spectra from the GaAs substrate as standards, $K_{Ga/As}$ (relating the heights of the Kα peaks) was obtained to be 0.95 ± 0./013. The proportionality factors $K_{In/Ga}$, $K_{In/As}$ (relating the height of the L-series peak of In to the heights of the Kα peaks of Ga and As) were also determined from spectra of InAs which was identified by TEM diffraction analysis. They are: $K_{In/Ga} = 0.489$, $K_{In/As} = 0.465$. These three proportionality factors (only two are independent) were used for estimation of x in $In_{1-x}\ Ga_xAs$ epitaxial patches.

3. RESULTS

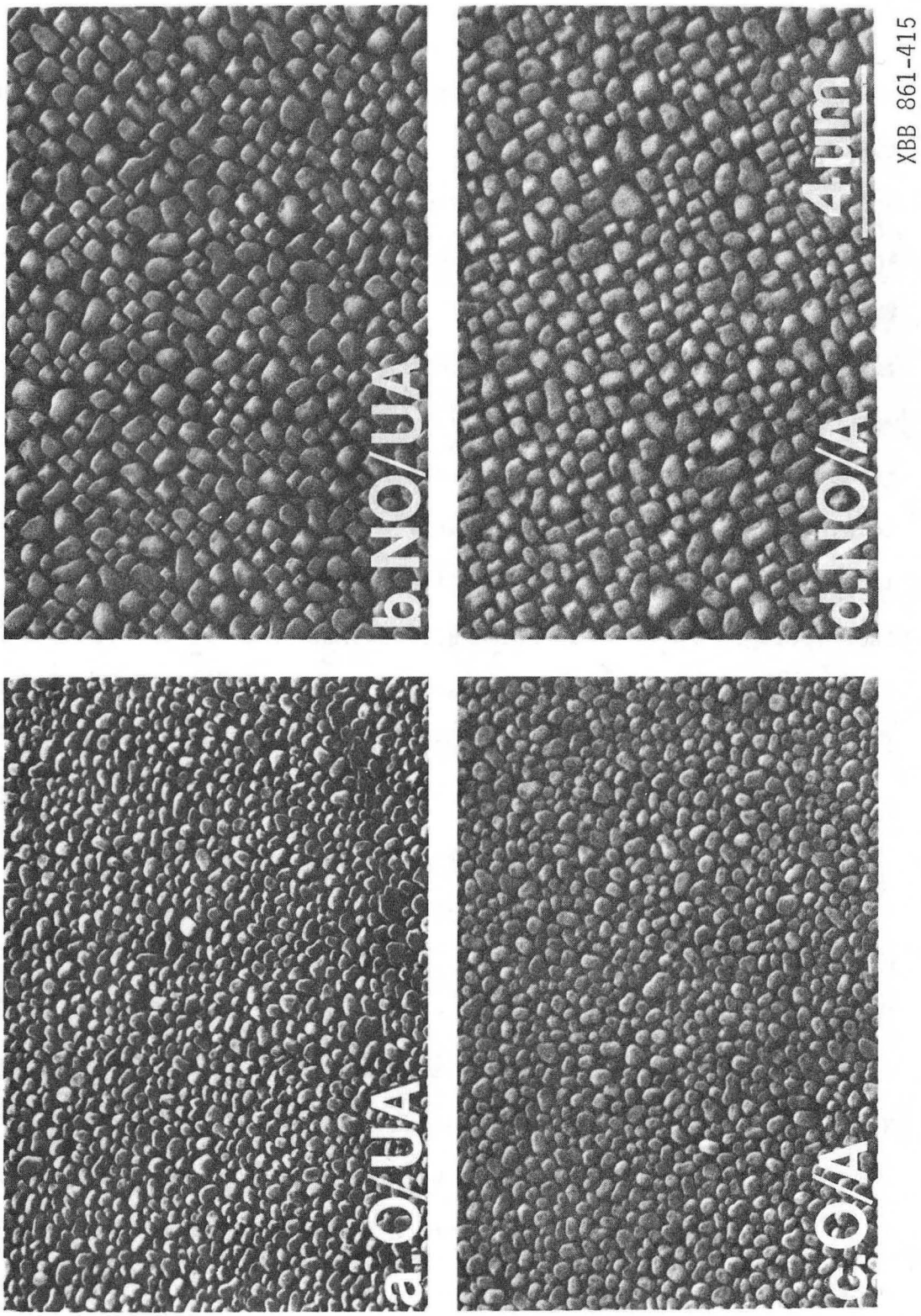
The surface morphologies of the as-deposited and annealed In/GaAs samples were revealed with scanning electron microscopy and conventional transmission electron microscopy of plan-view specimens. Orientation relationships between the various phases were determined by transmission electron diffraction of plan-view and cross-sectional specimens. Images of the cross-sectional specimens showed clearly the effect of the thin native oxide layer on the reaction. Energy-dispersive x-ray spectroscopy and high-resolution lattice imaging of these specimens provided a detailed description of the composition and structure as a function of depth. In this section, these electron microscopy results are presented for each of the four samples:

1) As-deposited In/native oxide/GaAs
2) Annealed In/native oxide/GaAs
3) As-deposited In/GaAs
4) Annealed In/GaAs

3.1 As-Deposited In/native oxide/GaAs

For this chemically cleaned sample, a 1 ~ 2 nm thick native oxide layer is expected on the surface of the GaAs substrate before the MBE deposition. The surface morphology of the as-deposited sample is shown in the SEM micrograph (Fig. 8a). As can be seen in this image, the thin indium film does not cover the GaAs surface completely. Instead, a large number of isolated indium islands with irregular shapes were formed on the substrate surface. Most of the islands have a diameter

Fig. 8. SEM images of the surface morphology of the as-deposited samples (a) with and (b) without the intervening oxide and of the annealed samples (c) with and (d) without the interface oxide layer.



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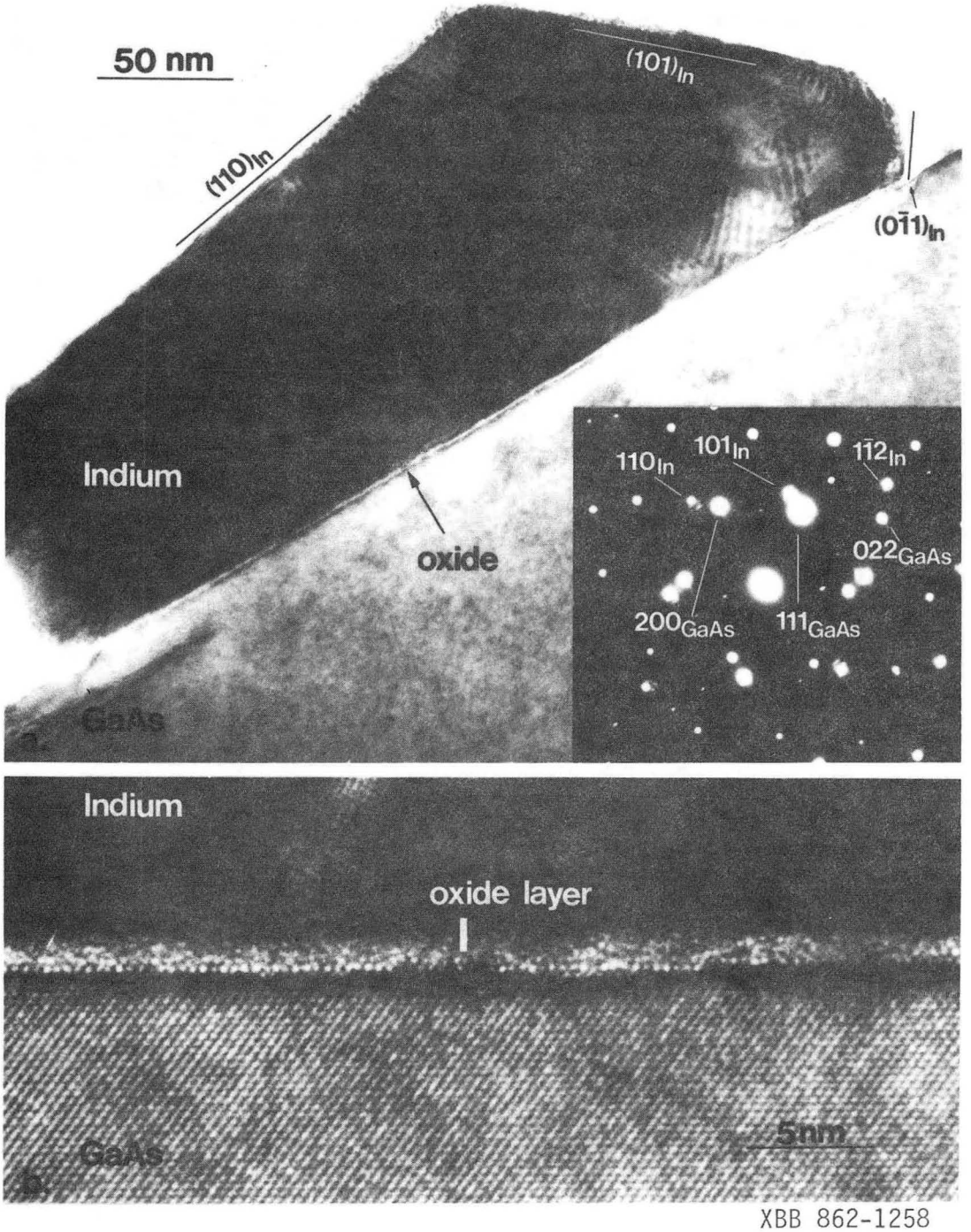
of approximately 0.2-0.3 μm, and many small islands (20 nm dia.) are situated between the large islands.

A cross-sectional study of this chemically cleaned sample is shown in Fig 9. From the TEM micrographs in this figure, it is clear that there is no large-scale reaction. The intervening native oxide layer is visible as a thin white line in Fig. 9a. The diffraction pattern was taken from the interface region, and shows the superimposed diffraction patterns from the GaAs substrate and the indium single crystal island. The surface of the indium island is faceted along crystallographic planes. With the addition of electron diffraction analysis, the facets of the indium island are determined to be the {011} and {110} families of planes of tetragonal indium. A lattice image taken from the interface region is shown in Fig. 9b. A thickness of 1.3 ± 0.3 nm for the native oxide layer was estimated from the image. The indium islands observed in this sample exhibited no orientation relationship with GaAs; however the island observed in Fig. 9 is (fortuitously) oriented with $[1\bar{1}\bar{1}]_{In}$ parallel to $[0\bar{1}1]_{GaAs}$. This particular island was chosen for detailed study since it illustrates most clearly the faceting of the indium crystallites.

3.2 Annealed In/native oxide/GaAs

Investigation of the samples with the intervening native oxide layer by SEM shows that no difference is observed in the surface morphology between the annealed sample (Fig. 8c) and the unannealed sample (Fig. 8a). The detailed surface morphology of this annealed sample is shown in the higher magnification SEM micrograph (Fig. 10a).

Fig. 9. (a) TEM micrograph of the as-deposited cross-sectional sample with the intervening oxide. The as-deposited indium island has been faceted at the low energy planes. Note that the native oxide appears as a white line at the interface. Inset diffraction pattern from the interface region shows the diffraction spots from $(0\bar{1}1)$ GaAs and $(1\bar{1}\bar{1})$ indium zone axis orientations. (b) Lattice image of the In/GaAs interface with the 1.3 nm thick native oxide layer.


50 nm
$(101)_{In}$
$(110)_{In}$
$(0\bar{1}1)_{In}$
Indium
oxide
GaAs
a.
110_{In}
101_{In}
$1\bar{1}2_{In}$
022_{GaAs}
200_{GaAs}
111_{GaAs}
Indium
oxide layer
5nm
GaAs
b.

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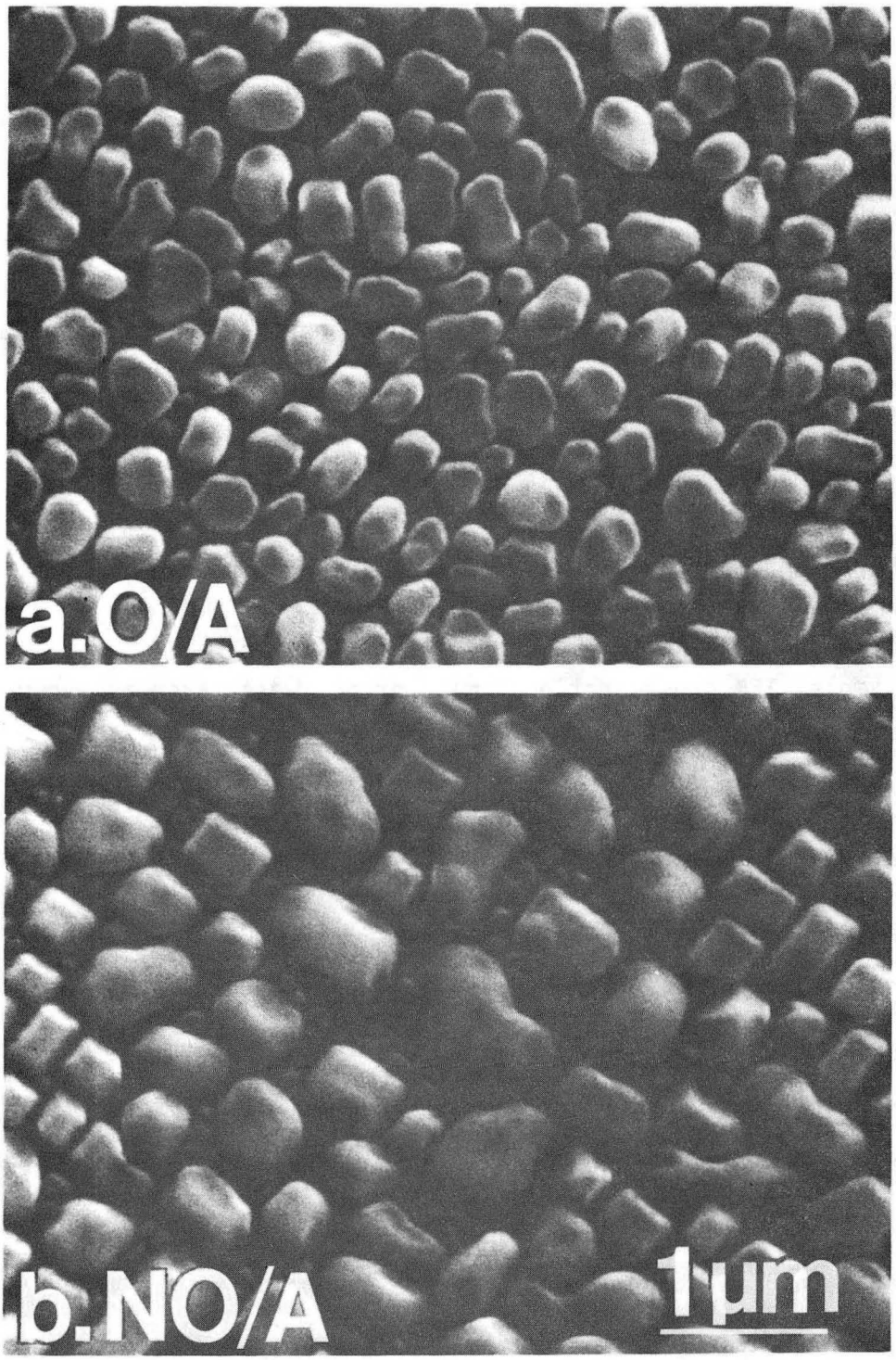

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Fig. 10. High magnification SEM images of the annealed samples (a) with and (b) without the intervenig native oxide, which show the detailed surface morphology.

Figure 11 is a plan-view TEM bright-field image from this sample. In this figure, one can see the randomly oriented indium islands with many small islands between them. It is also seen that a dark periphery appears around each island, and there exists a dark region within each indium island. This dark periphery of the indium island has been determined from the diffraction analysis to be indium oxide In_2O_3 on the surface of the island. The dark regions in the islands are thought to be the reacted phase $In_{1-x}Ga_xAs$ grown through broken or very thin regions of native oxide.

In order to understand the interface morphology of the annealed sample, TEM cross-sectional micrographs were taken as shown in Fig. 12. From these images, it is clear that the native oxide layer, visible as a thin white line, exists at most of the interface between the In island and the substrate. It is not surprising that the reacted regions in the indium island exist at the interface since the native oxide may not cover the surface of the substrate completely and uniformly. As shown in this figure, several reacted regions appear at the interface. The diffraction analysis from this specimen shows that there exist two indium grains with different orientations, and the epitaxial ternary phase $In_{1-x}Ga_xAs$. The indexed diffraction pattern gives the 112 and 002-type reflections with the zone axes $[1\bar{1}\bar{1}]$ and $[\bar{1}10]$, respectively from the body-centered tetragonal indium. Using Vegard's law,[34] the ternary phase was identified from this diffraction pattern to be $In_{0.8}Ga_{0.2}As$.

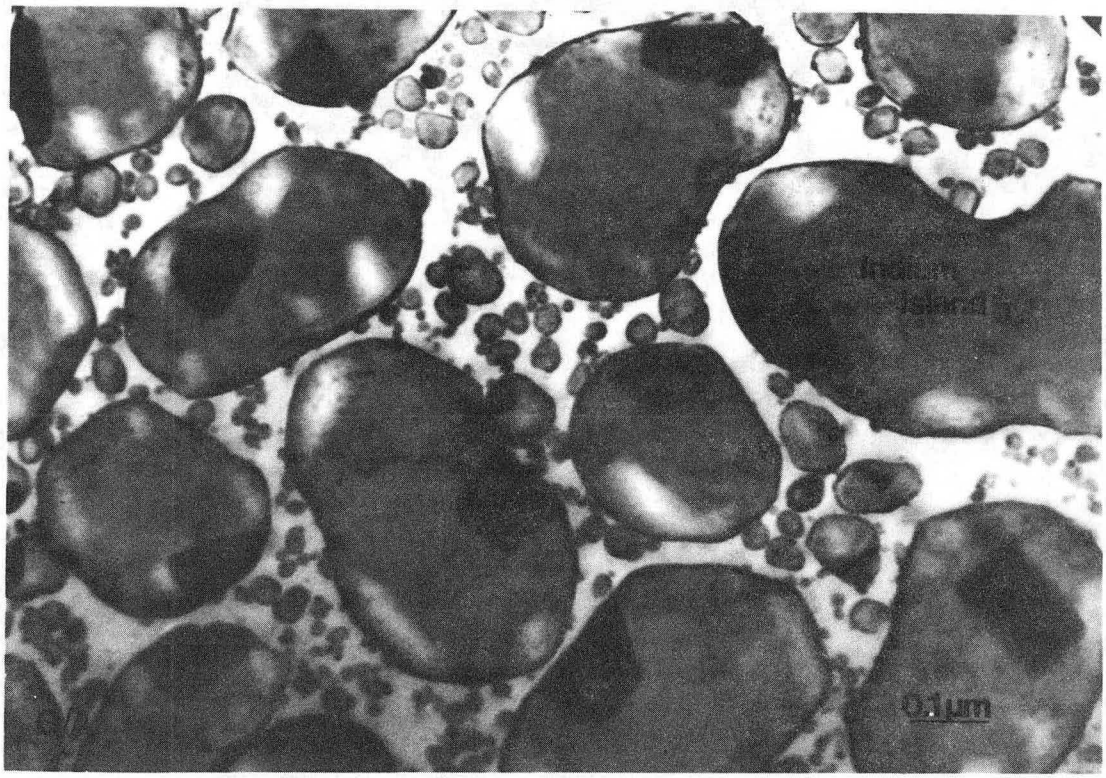

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Fig. 11. TEM image of the annealed plan-view sample with the native oxide. The indium oxide (In_2O_3) shells on the surface of islands show as the dark peripheries of the indium islands. The small reacted region is within the island.

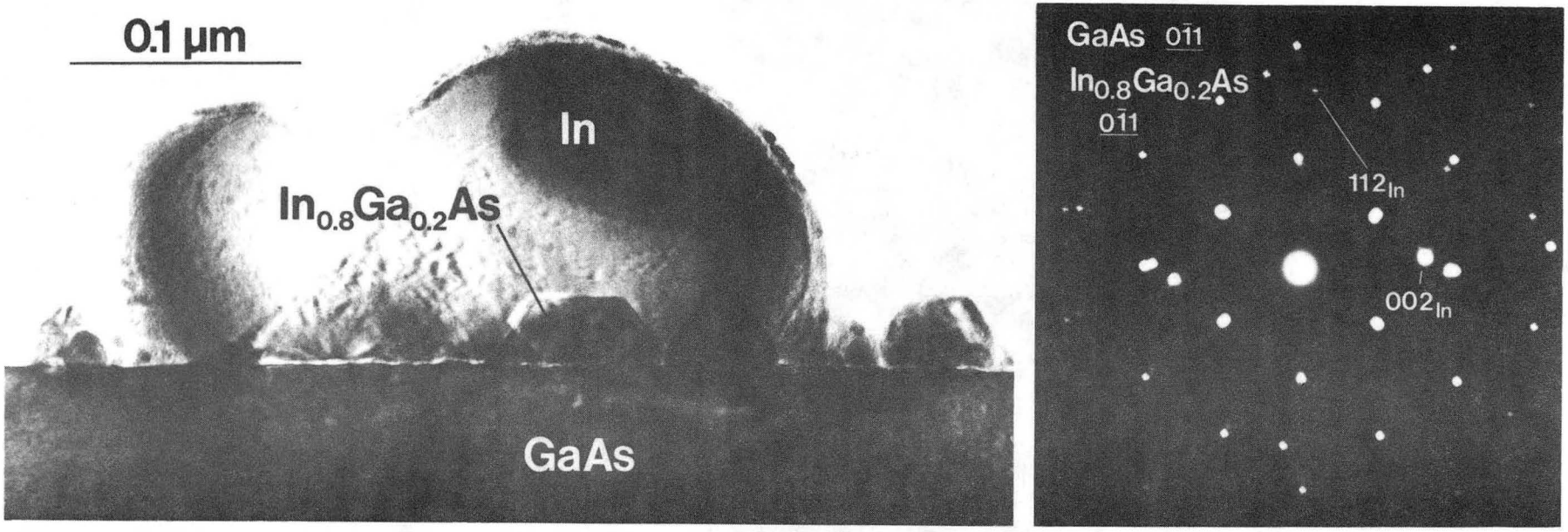

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Fig. 12. TEM micrograph of the annealed ($0\bar{1}1$) cross-sectional sample with the intervening native oxide. The native oxide appears as a white line at the interface. The two reacted patches with the faceted surface are shown in the indium island above the interface. One patch was estimated to be $In_{0.8}Ga_{0.2}As$ phase by the diffraction analysis. Diffraction pattern gives the reflections from the GaAs substrate, the $In_{0.8}Ga_{0.2}As$ and two indium grains.

The lattice image shown in Fig. 13 reveals the structure of the $In_{0.8}Ga_{0.2}As$ patch. As expected, measurement of the $\{111\}_{In_{1-x}Ga_xAs}$ spacing also suggests the composition $In_{0.8}Ga_{0.2}As$ in agreement with the diffraction analysis. Also, microtwins and stacking faults appear in these epitaxial patches. The origin of these faults will be discussed in a latter section. Note also that the epitaxial patches are faceted on $\{111\}$ and $\{100\}$ $In_{1-x}Ga_xAs$ planes as would be expected from growth kinetics and surface energy considerations.

3.3 As-Deposited In/GaAs

Figure 8b shows a scanning electron micrograph of the UHV cleaned sample that is considered to be free of interfacial oxide. As can be seen in the micrograph, the as-deposited indium on the oxide-free substrate forms isolated rectangular islands. Most of the substrate surface was covered by the islands with an average side of $0.4 \times 0.4\ \mu m^2$. Small rectangular islands ($0.1 \times 0.1\ \mu m^2$) are located between these large islands. Their geometrical shape and well-defined orientations strongly suggest an epitaxial relationship between the isolated rectangular islands and the substrate.

Further study of these rectangular islands was performed by a combination of TEM plan-view and cross-sectional techniques. Figure 14 is a plan-view micrograph which shows the indium islands with the rectangular shape as seen in the SEM micrograph. From the analysis of the diffraction pattern together with the bright field image, the edges of the rectangular islands have been determined to be aligned

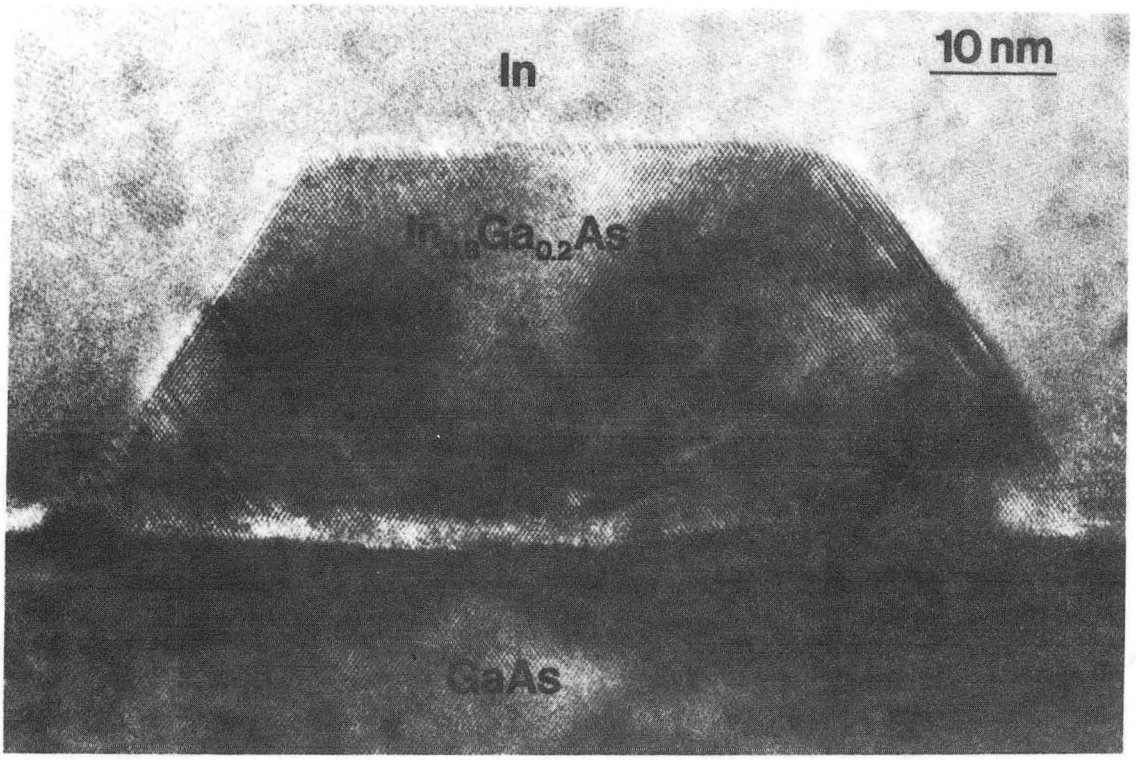

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Fig. 13. Lattice image of the $In_{0.8}Ga_{0.2}As$ patch shown in Fig. 12. The patch is faceted on the {111} and {100} close-packed planes. The microtwins and stacking faults formed to accommodate the oxide particles on the interface during the $In_{0.8}Ga_{0.2}As$ growth.

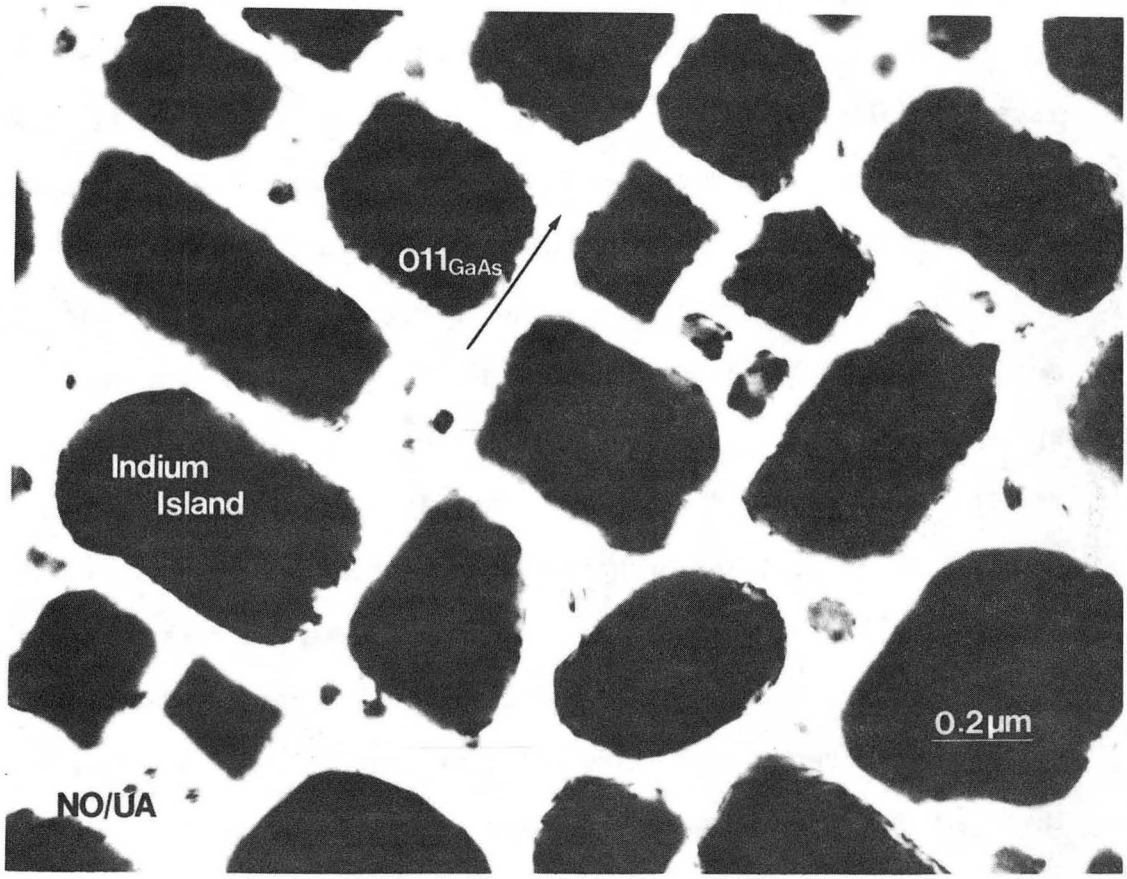

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Fig. 14. TEM image of the as-deposited oxide-free sample. The edges of the rectangular indium islands are aligned along the <011> directions of the (100) GaAs substrate.

along the <110> family of directions on the (100) surface of the GaAs substrate.

The cross-sectional technique was used to investigate the interface morphology for the as-deposited oxide-free sample. The orientation relationship between the In crystallites and the GaAs substrate (described below) have also been determined by this technique. A TEM cross-sectional micrograph is shown in Fig. 15. Comparing with specimens containing the intervening oxide, it is obvious that there is no appreciable oxide layer appearing at the interface. Instead, a small reacted patch with a faceted shape is visible at the interface. From the diffraction pattern, four different phases have been found in this specimen. The four phases were identified by the diffraction analysis to be GaAs, In, InAs and In_2O_3 as shown in the indexed diffraction pattern. The very interesting point is that all four phases are epitaxial with the orientation relationships:

$$[0\bar{1}1]_{GaAs} \| [1\bar{1}\bar{1}]_{In} \| [0\bar{1}1]_{InAs} \| [01\bar{1}]_{In_2O_3}$$

and

$$(100)_{GaAs} \| (110)_{In} \| (100)_{InAs} \| (100)_{In_2O_3} \quad .$$

The orientation relationship between the GaAs substrate and the indium is further demonstrated with the aid of a stereographic projection which will be shown in the discussion section. The reacted patch with a geometrical shape above the interface in Fig. 15 was identified to be epitaxial InAs formed during the thin film deposition or sample preparation. The facets of the InAs patch are on the $\{111\}_{InAs}$ and $\{100\}_{InAs}$ surfaces. The indium oxide In_2O_3 was formed on the surface

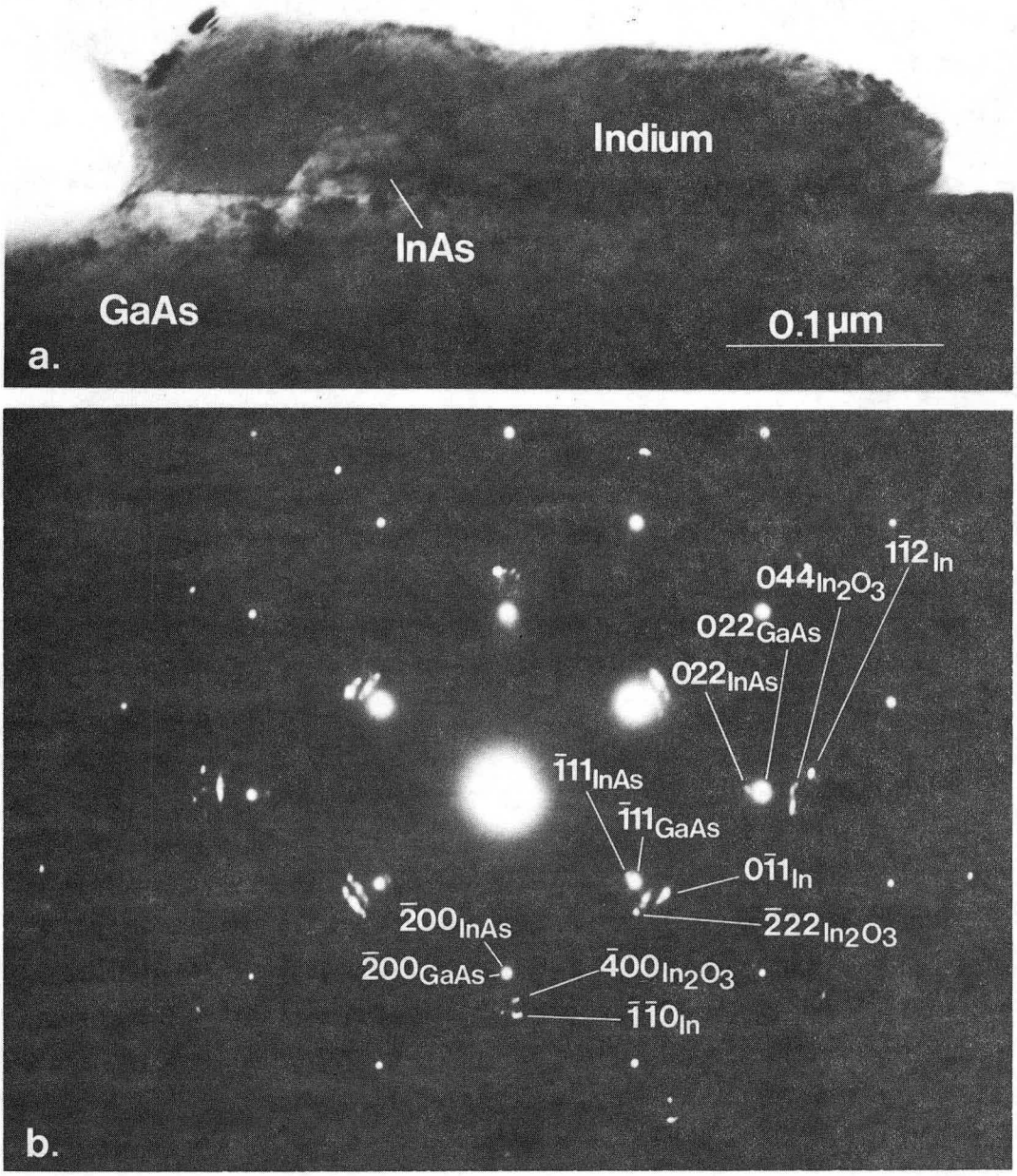

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Fig. 15. (a) TEM image of the as-deposited cross-sectional oxide-free sample. An InAs patch estimated by the diffraction analysis is shown on the oxide-free interface.
(b) The diffraction pattern illustrating the orientation relationships between the four epitaxial phases, GaAs, InAs, In and In_2O_3.

of the indium island after MBE deposition. The structure of the indium oxide In_2O_3 is cubic with a lattice parameter of a = 1.012 nm.[35]

3.4 Annealed In/GaAs

The SEM micrograph (Fig. 8d) of the annealed oxide-free specimen shows that the surface morphology of the sample remains unchanged by annealing. The SEM image with higher magnification is shown in Fig. 10b to give a clearer picture on the surface morphology.

The interface morphology of the oxide-free sample after annealing has been studied by conventional, high resolution and analytical microscopies of the cross-sectional samples. As can be seen in Fig. 16, the high resolution image reveals the reacted interface morphology. It is clear that the interface has moved ~5-8 nm down into the substrate. The misfit dislocations and moiré fringes at the interface result from the two distinct lattice parameters of the epitaxial island and the GaAs substrate. This information reveals that there is no graded layer existing at the interface, i.e., the interface is abrupt. The reacted phase formed after annealing can be identified structurally by the diffraction analysis and compositionally by the energy dispersive spectrometry. Based on Vegard's law, the epitaxial island was determined from the diffraction pattern to be the ternary phase $In_{0.9}Ga_{0.1}As$ with the zincblende structure. Analytical electron microscopy was also used to identify this phase. The EDS spectra from A and B give the compositional information from the epitaxial island and the GaAs substrate, respectively. Quantitative microanalysis of spectrum A suggests that the composition is

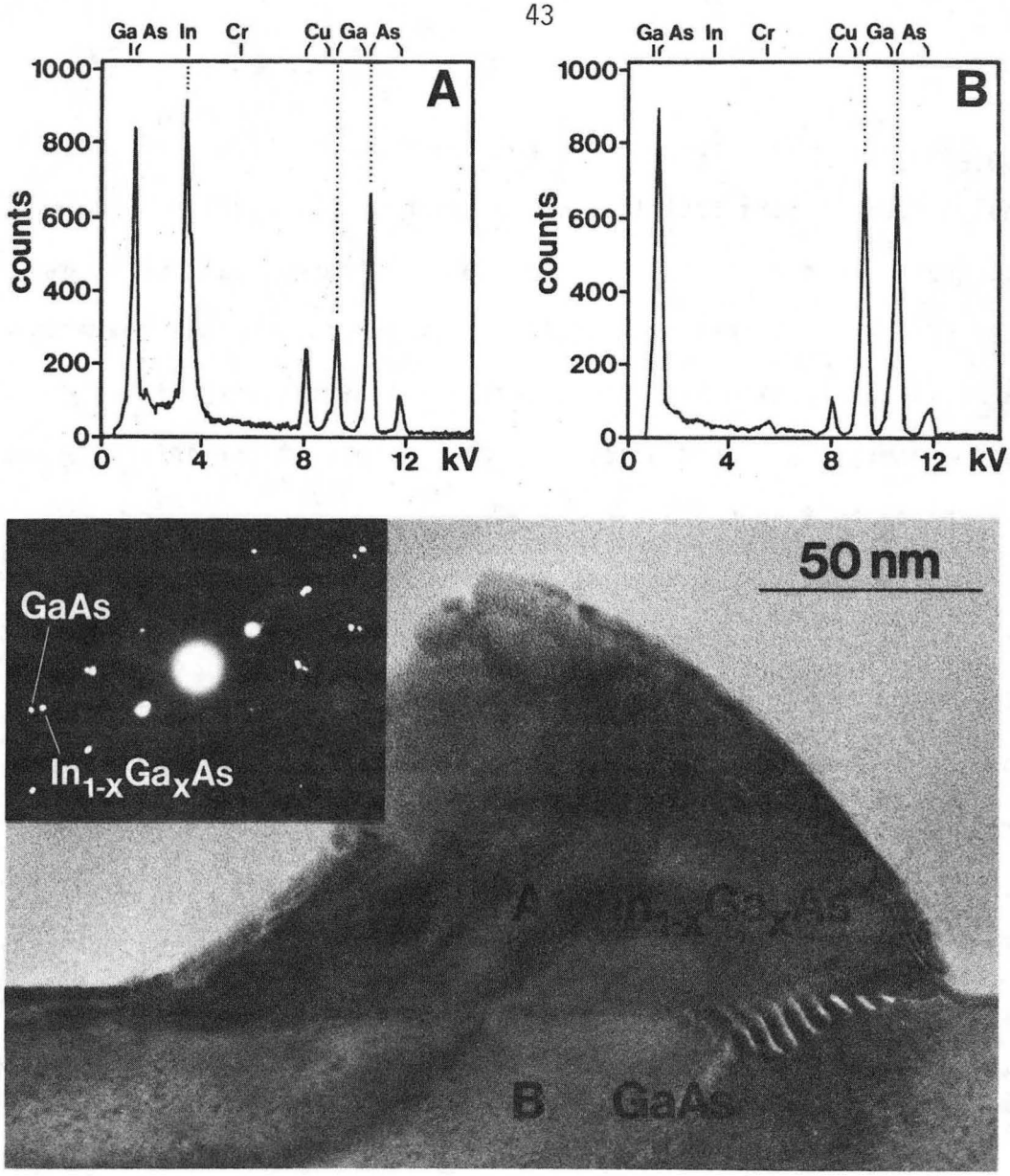

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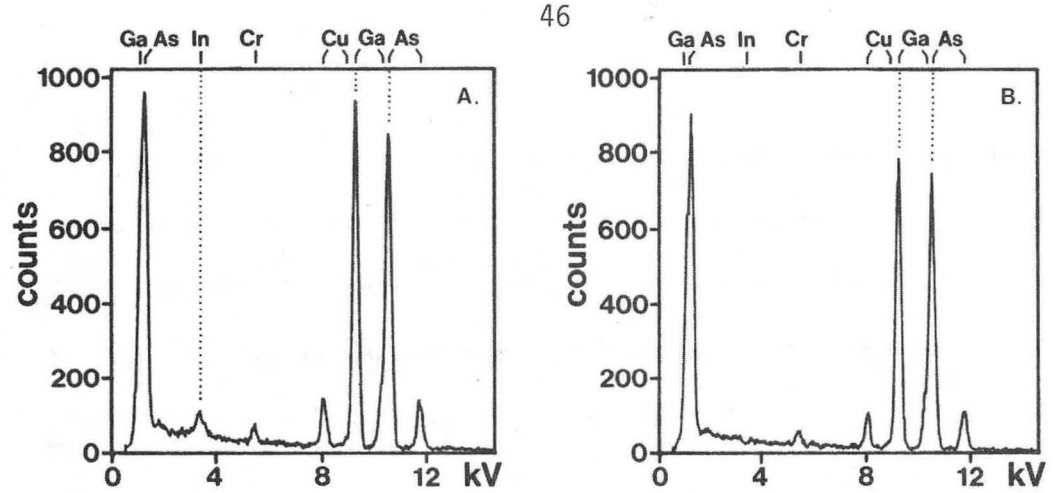
Fig. 16. High resolution image of the annealed cross-sectional oxide-free sample. The misfit dislocations and the moiré fringes indicate an abrupt interface. Inset diffraction pattern was taken from the region including the reacted patch A and the substrate B. The patch A was estimated to be $In_{0.9}Ga_{0.1}As$ by diffraction analysis. The energy dispersive x-ray spectra obtained from the patch A and the substrate B are also shown to identify the patch as $In_{1-x}Ga_xAs$.

$In_{0.6}Ga_{0.4}As$. This result does not coincide with the diffraction analysis due to the fact that the electron probe overlaps some of the substrate. Since the $In_{0.9}Ga_{0.1}As$ has a different lattice parameter (a = 6.02 Å) than GaAs (5.65 Å), it is obvious that there should be misfit dislocations at the interface to decrease the interfacial strain energy. These dislocations are visible at the interface and are spaced by 3-4 nm.

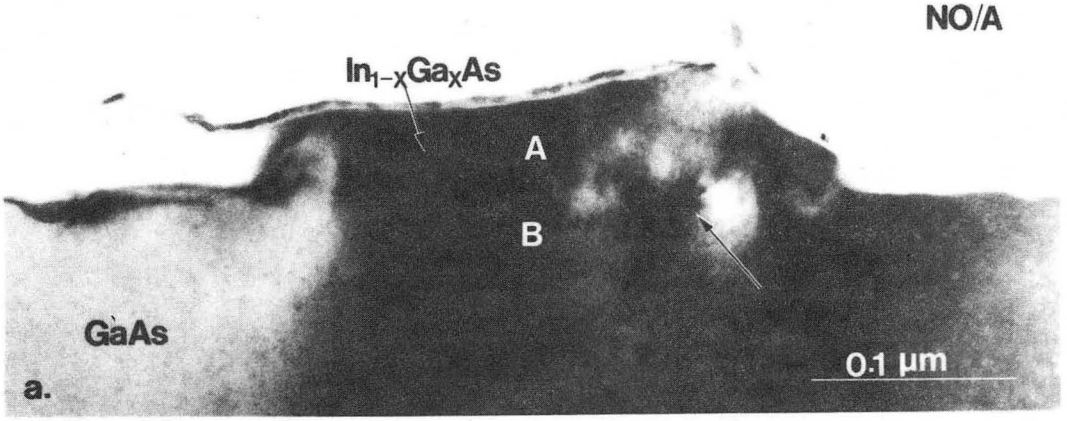
Figure 17 gives another example of the oxide-free In/GaAs interface reaction after annealing. The two beam bright field image is shown in Fig. 17a. Indium oxide can be seen to cover the reacted island. The spectra from the island A and the substrate B are shown above the image. From the quantitative analysis of spectrum A, this epitaxial island is determined to be $\sim In_{0.02}Ga_{0.98}As$. The diffraction pattern shown in Fig. 17b from the interface region indicates that it is difficult to distinguish the diffraction spots of this phase from those of GaAs because of the small amount of indium in this ternary phase. The high resolution lattice image in Fig. 17c reveals the detailed interface morphology. A misfit dislocation can be seen at the interface due to the mismatch (0.16%) between these two phases. This small mismatch leads to a low density of misfit dislocations at the interface. This result indicates that a large amount of GaAs has been dissolved into the molten indium during annealing.

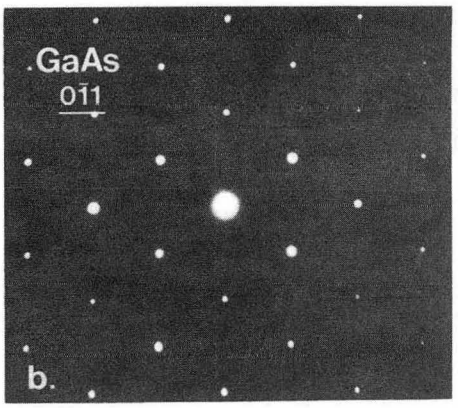
A third example is shown in the cross-sectional micrograph in Fig. 18. The reacted island shows three regions with different contrast. These phases were identified quantitatively by the EDS

Fig. 17. (a) HRTEM image of the annealed oxide-free sample. The misfit dislocations can be seen at the interface. The indium oxide shell appears on the surface of the $In_{1-x}Ga_xAs$ phase.
(b) Diffraction pattern taken from the island A and the substrate B shows only the reflections from the GaAs [011] zone axis orientation.
(c) Lattice image of a misfit dislocation (arrowed in (a)) at the interface.
Quantitative microanalysis of the energy dispersive x-ray spectrum A indicates the patch A to have the composition of $In_{0.02}Ga_{0.98}As$.



NO/A





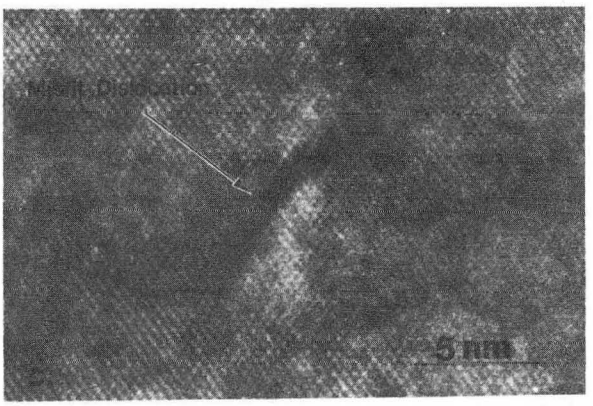


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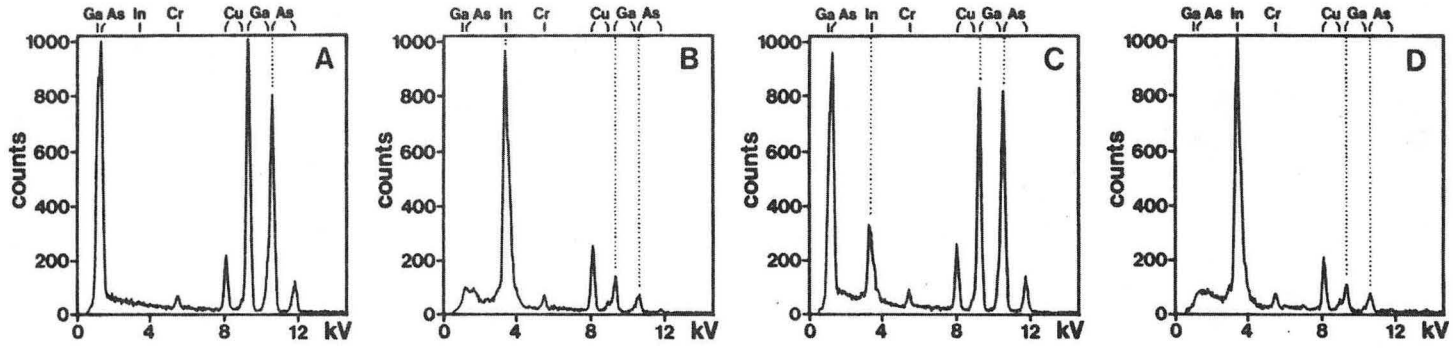
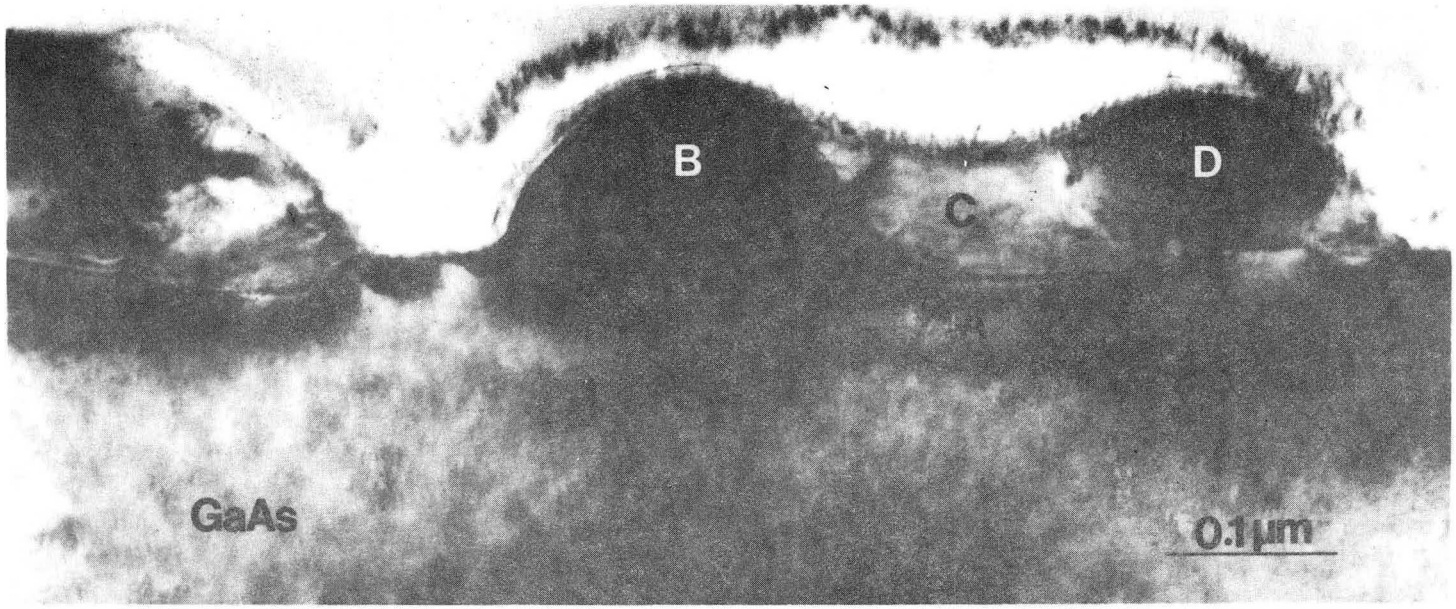
Fig. 18. TEM image of the annealed oxide-free sample. The three grains B, C, and D formed after annealing at 350°C for 10 minutes show different contrast. The indium oxide shell is visible over the whole surface of the reacted island. The energy dispersive x-ray spectra were taken from the substrate A and the grains B, C and D, respectively. The grain C was identified to be $In_{0.1}Ga_{0.9}As$. B and D were found to have the compositions 70.6% In, 18.8% Ga, 10.6% As and 76.4% In, 13.2% Ga and 10.4% As, respectively.


Ga As In Cr Cu Ga As
A
B
C
D
counts
1000
800
600
400
200
0
0 4 8 12 kV


B
C
D
GaAs
0.1 µm

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technique. Four spectra have been obtained from the substrate A and the three grains B, C and D. The grain C has been determined to be $In_{0.1}Ga_{0.9}As$. As shown in the spectra, the grains B and D are indium with small amounts of Ga and As. Grain B consists of 70.6% indium, 18.8% gallium and 10.6% arsenic, and grain D has a composition of 76.4% indium, 13.2% gallium and 10.4% arsenic.

4. DISCUSSION

4.1 Mechanism of the In/GaAs Reaction

Materials-related limits to the performance and the stability of contacts to GaAs have motivated recent investigations of Metal/GaAs interface reactions. Following Sands et al.,[36] reactions between compound semiconductors, AB, and reacting metal species, M, can be classified into four categories based on the types and depth distributions of the product phases. These four categories are:

1) Reactions that produce layered binary compounds. The layer sequence is determined by the dominant moving species and interfacial effects. An example of this type of product phase morphology is the PtGa/$PtAs_2$/GaAs layer sequence that results from the Pt/GaAs reaction;

2) Reactions that result in the formation of ternary phases of the type M_xGaAs where the reaction is analogous to the formation of a silicide on silicon. For example, Ni and Pd react with GaAs to form the ternary compounds Ni_xGaAs, and Pd_xGaAs (phases I and II), respectively;

3) Reactions that involve the exchange of cations in which the reacting species M (usually from the same column of the periodic table as A) exchanges with the cation A, leaving the B sublattice essentially invariant. The topotaxial product phase has a similar or, in many cases, identical structure and orientation as the semiconductor substrate. For example, In on GaAs reacts to form $In_{1-x}Ga_xAs$ + In_xGa_{1-x};

4) Reactions that result in the accumulation of the anion B at or near the M-A/AB interface. This product phase morphology results from a preferential reaction between M and A under conditions which do not allow the escape of B by diffusion or sublimation. The thermal oxidation of GaAs at 500°C[37] and the Au/GaAs reaction[38] are examples of anion accumulation reactions. These four categories are sufficient to describe the initial reactions between most metals and compound semiconductors. During further annealing and during annealing at high temperature, additional reactions may occur.

Previous studies[1,2] suggest that the In/GaAs reaction is a cation exchange reaction during which $In_{1-x}Ga_xAs + In_xGa_{1-x}$ should be formed. Lakhani[2] interpreted his AES results as demonstrating the existence of a graded $In_{1-x}Ga_xAs$/GaAs heterojunction ($0 \leq x \leq 1$) produced by heat treating thermally-evaporated indium films on GaAs substrates. As described in the introduction, the presence of a graded layer is thought to be a criterion for producing ohmic contacts with low specific resistance.[3] Lakhani found that annealing above 250°C produced ohmic contacts (the lowest resistance resulted from annealing at 350°C). Based upon the theory described in Ref. 3, this electrical behavior is consistent with the formation of a graded heterojunction. The results of this investigation, however, clearly demonstrate that annealing an In film, albeit a thinner film than studied by Lakhani (50 nm compared with 200 nm), on GaAs at 350°C results in an abrupt heterojunction.

The mechanism of the In/GaAs interface reaction during annealing has been revealed by the analyses of two-beam bright-field images, diffraction patterns and energy dispersive spectrometry from cross-sectional and plan-view TEM specimens. During annealing at 350°C, the as-deposited indium thin film is molten (indium melts at 156°C). Gallium and arsenic dissolve into the molten In to their solubility limits at 350°C (probably a few atomic percent). Evidently the system can lower its free energy further by entering a metastable supersaturated state. In other words, Ga and As are dissolved into the molten In until $In_{1-x}Ga_xAs$ is nucleated. Diffraction patterns and images (Figs. 16, 17, 18) show that the $In_{1-x}Ga_xAs$ epitaxial patches are rather uniform in composition. The atom function x in $In_{1-x}Ga_xAs$ is determined by the degree of Ga and As supersaturation at the time of nucleation. As discussed below, most epitaxial $In_{1-x}Ga_xAs$ patches have $x < 0.2$. In the sample free of the intervening native oxide, $In_{1-x}Ga_xAs$ islands with $x > 0.9$ are also observed. No islands with intermediate values of x have been observed suggesting that there may be a miscibility gap in the InAs-GaAs pseudo binary phase diagram at 350°C. If a miscibility gap is present, it may be impossible to grow a graded layer at 350°C. This would appear to be in direct conflict with Lakhani's model of heterojunction formation. Furthermore, it is apparent from images such as Fig. 16 that the In/GaAs reaction does not involve the solid-state exchange of cations. Such a reaction could very well lead to the formation of a graded heterojunction over at least part of the composition range. Instead the In/GaAs reaction involves dissolution

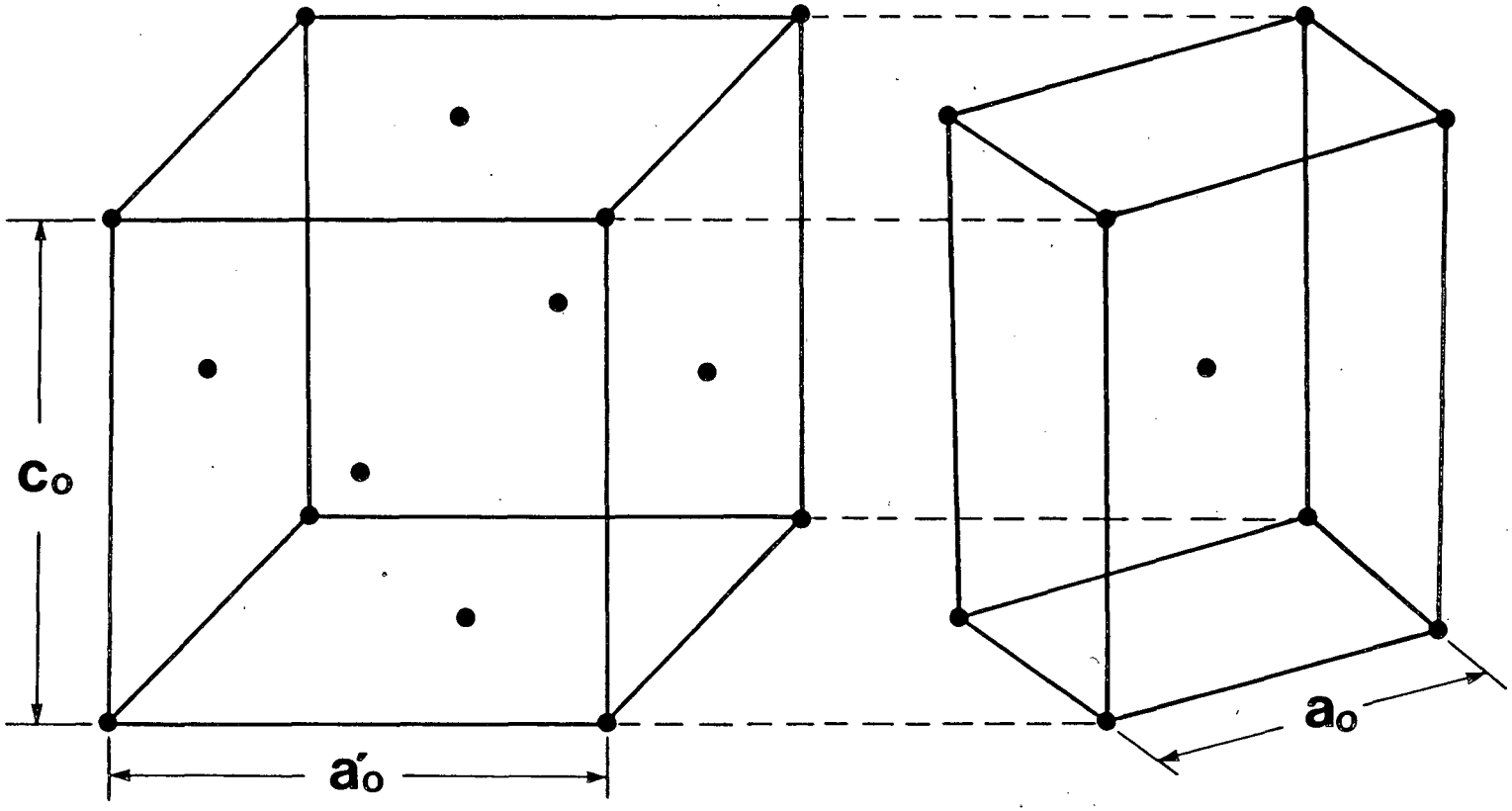
of the substrate, supersaturation of Ga and As in In, and finally, precipitation of $In_{1-x}Ga_xAs$ in the form of islands on top of the new substrate surface.

4.2 Morphological Features of the In/GaAs Reaction

4.2.1 The In-GaAs Orientation Relationship

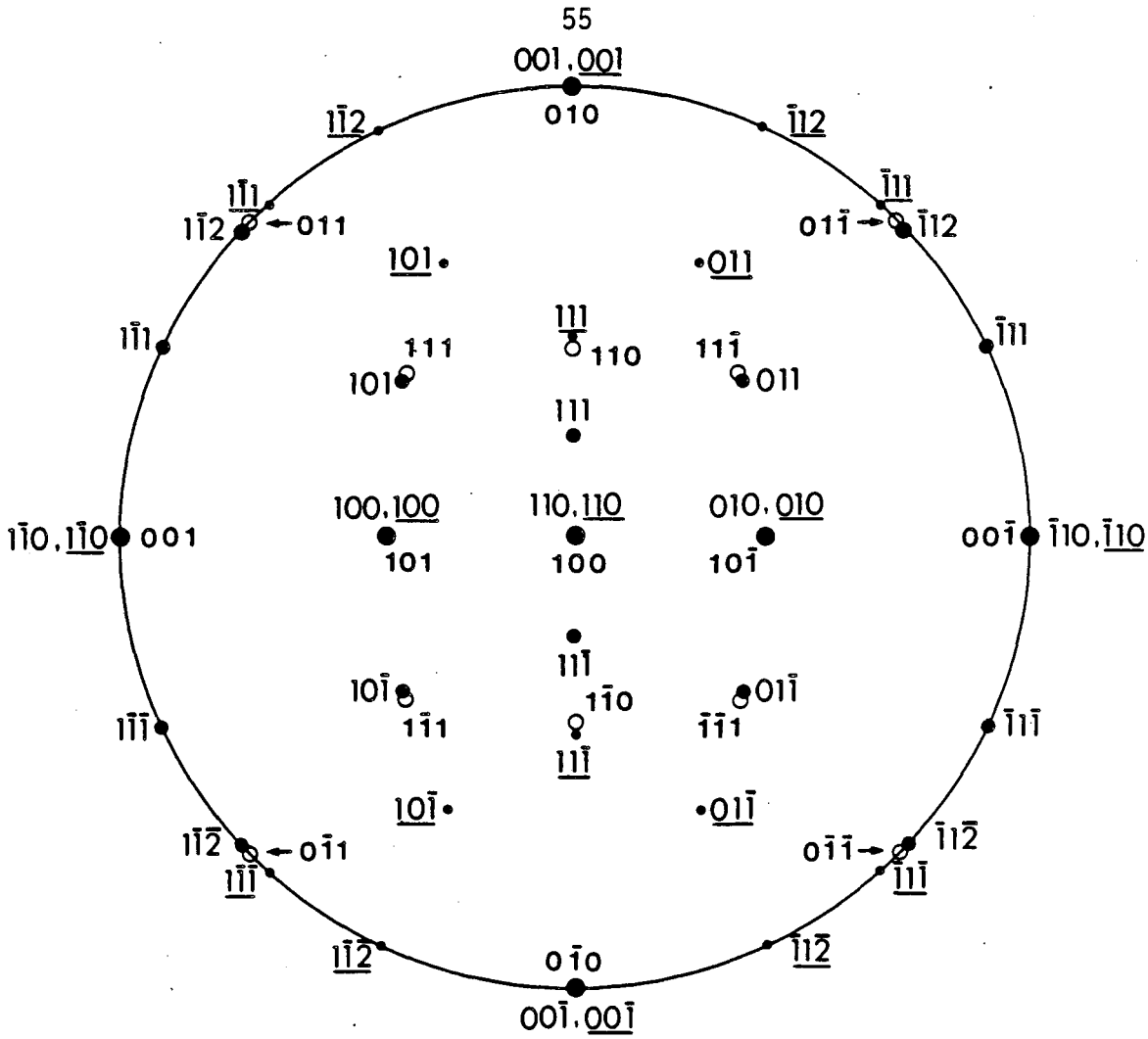
Indium is a pseudo-metal which is placed in the periodic table as a IIIB element. The crystal structure of the IIIB elements are not those of typical metals (fcc, hcp, bcc). Indium has a body-centered tetragonal unit cell with a_o = 0.3244 nm and c_o = 0.4938 nm. This structure can be obtained by the elongation of a face-centered cubic unit cell by a factor of 1.07 along a <100> f.c.c. direction [Fig. 19]. Thus the structure of indium can be described alternatively in terms of a distorted f.c.c. pseudo-unit cell having a_o' = 0.4588 nm and $c_o' = c_o$ = 0.4938 nm. As in f.c.c. metals, the coordination number of In is 12. However, four of the nearest neighbor atoms are at a distance of 0.324 nm with the remaining eight atoms at a distance of 0.337 nm.[39]

As shown in the results section, the In/GaAs orientation relationship is $[0\bar{1}1]_{GaAs} \| [1\bar{1}\bar{1}]_{In}$, $(100)_{GaAs} \| (110)_{In}$. This orientation relationship is illustrated in Fig. 20 with the aid of a stereographic projection. In terms of the pseudo-cubic unit cell described above, the orientation relationship is pseudo-cubic (In) on cubic (GaAs). In other words, close-packed planes in indium ($\{011\}_{tet,In}$) and GaAs($\{111\}_{GaAs}$) are approximately parallel.



XBL 864-1326

Fig. 19. The structure of indium shown as body-centered tetragonal on the right and the pseudo face-centered cubic on the left.



110 **In plane normal**

<u>110</u> **In direction**

100 **GaAs plane normal and direction**

XBL 864-1320

Fig. 20. Stereographic projection representing the orientation relationship between the indium body-centered tetragonal and the GaAs zinc blende structures.

$(110)_{In} \parallel (100)_{GaAs}$
$(100)_{In} \parallel (101)_{GaAs}$
$(101)_{In} \parallel (111)_{GaAs}$

From the orientation relationship given above and the known indium structure, we now are able to discuss the microstructure at the In/GaAs interface. For the as-deposited In/GaAs specimen, the mismatches of the two perpendicular arrays of In and GaAs lattice planes ($(010)_{GaAs}\|(001)_{In}$ and $(001)_{GaAs}\|(1\bar{1}0)_{In}$) can be calculated according to Eq. (3)

$$f = \frac{d_f - d_o}{d_{avg}} \quad , \tag{3}$$

where d_f is the unstrained plane spacing in the overlayer, d_o is the corresponding plane spacing of the substrate and d_{avg} is the average of d_o and d_f. The misfits (mismatches) at the In/GaAs interface are found to be 13.4% and 20.6% for the arrays of $(010)_{GaAs}\|(001)_{In}$ and $(001)_{GaAs}\|(1\bar{1}0)_{In}$, which are the low values relative to other possible combinations of low index lattice spacings except $\{110\}_{GaAs}\|\{110\}_{In}$ lattice spacing with a misfit of 14%. This is the key point for the orientation relationship because the interfacial energy increases with the degree of misfit at the interface between two crystals.[40] Therefore, the arrangement of the low mismatched lattices at the interface will be formed to make the system reach a low energy and stable condition.

4.2.2 Faceting of In Particles

As shown in the results section, In particles on both the samples with and without the intervening oxide exhibit crystallographic faceting on {110} and {011} Indium planes. Since the $\{011\}_{In}$ planes

are the most closely packed planes, this faceting behavior is consistent with the minimization of surface energy.[40]

By combining the observation of faceting of In particles on low energy planes with the determination of the In/GaAs orientation relationship, one can explain the shape and orientation of the In particles observed in Fig. 9. As will be discussed below, the native oxide disrupts the In/GaAs orientation relationship. The In islands, however, are still faceted.

4.2.3 The $In_{1-x}Ga_xAs$/GaAs Interface

As described in Sec. 4.1, the In/GaAs reaction involves the dissolution of the substrate, supersaturation of Ga and As in the molten In and precipitation of $In_{1-x}Ga_xAs$ in form of islands on top of the substrate surface. The epitaxial $In_{1-x}Ga_xAs$ islands that grow during annealing have the zinc blende structure with a different lattice parameter from the substrate. The mismatch between the two phases can be accommodated by straining elastically one or both of the two lattices at the interface, or by forming misfit dislocations to allow the lattice constant of the film to relax towards the unstrained value. As shown in Fig. 16, there is a high density of misfit dislocations at the interface between the epitaxial $In_{0.9}Ga_{0.1}As$ phase and the substrate due to the large mismatch (6.3%). The existence of the misfit dislocations further indicates the abrupt nature of the interface between the $In_{1-x}Ga_xAs$ island and the substrate.

$In_{1-x}Ga_xAs$ patches can also be found in the sample with the intervening oxide, where the patch can grow into the In island through a broken oxide region during annealing. From the results section, such an $In_{1-x}Ga_xAs$ patch has been shown to have a composition with $x \simeq 0.2$ [Fig. 12]. The lattice image in Fig. 13 gives more detailed information. It is not surprising that this $In_{0.8}Ga_{0.2}As$ patch is faceted on {111} and {100} planes which are the first and second most closely packed planes, suggesting that they have the lowest surface energies. We would expect the same results from kinetic arguments. The stacking faults formed in this patch are due to the rough oxide layer on the substrate. When the patch grows on the rough oxide surface, stacking faults are formed to accommodate the oxide particles.

4.3 Effect of the Native Oxide

4.3.1 Effect of the Native Oxide on Morphology of As-Deposited Films

As discussed in Section 2.2, the as-deposited indium forms isolated rectangular islands on the oxide-free GaAs substrate. These rectangular indium islands have a well-defined orientation relationship with the GaAs substrate due to the energetic factors described above. In order to determine the effect of the native oxide at the interface, indium was deposited onto the chemically cleaned substrate which had not experienced an oxide-desorbing treatment under UHV conditions. Based on previous experience,[41] a native oxide layer of 1 ~ 2 nm in thickness was expected on the chemically cleaned GaAs surface. Figure 8 shows the SEM images from both UHV cleaned and chemically cleaned

samples. Comparing these two images, it is clear that the surface morphologies of these two samples are different. For the chemically cleaned sample, the isolated indium islands do not exhibit any preferential orientation in contrast to the In islands on the oxide-free GaAs substrate. This thin (1.3 ± 0.3 nm) oxide layer is sufficient to completely disrupt the In/GaAs orientation relationship as observed in the oxide-free sample.

4.3.2 Effect of the Native Oxide on the In/GaAs Reaction

The In/GaAs reaction is largely inhibited by the presence of the thin native oxide/hydrocarbon layer. The In/GaAs reaction does initiate locally, probably through pores, cracks and thin patches in the intervening oxide. Locally, the reaction mechanism is the same with or without the native oxide layer. However, the extent of the reaction is greatly limited by the presence of the oxide. The native oxide layer is also detrimental to the structural perfection of the $In_{1-x}Ga_xAs$ epitaxial islands. As can be seen in Fig. 13, stacking faults and microtwins in $In_{1-x}Ga_xAs$/GaAs emanate from particles of oxide at the $In_{1-x}Ga_xAs$/GaAs interface. This morphology strongly suggests that Shockley partial dislocations form due to stresses or growth mistakes which result from accommodation of the oxide particles during growth. Indeed, stacking faults were not observed in $In_{1-x}Ga_xAs$ patches grown on the oxide-free wafer.

To explain the inhibitation of the reaction by the native oxide, it is necessary to understand the mechanism of the oxide formation from a thermodynamic point of view. As discussed by Zilko et al.,[42]

Bertrand[43] and by Oda et al. experimentally,[44] the native oxide formed at room temperature consists of Ga_2O_3, As_2O_3 and elemental As depending on the details of the chemical cleaning method. The Gibbs free energies of formation of In_2O_3, Ga_2O_3 and As_2O_3 at 298.15°K are found to be -198.6, -238.6 and -138 Kcal/mol, respectively.[41] Since the Gibbs free energy for In_2O_3 formation is higher than that of Ga_2O_3, the indium oxide In_2O_3 is thermodynamically unstable relative to Ga_2O_3 so that no reaction is expected between the as-deposited indium and Ga_2O_3 during annealing. Thus, it is not surprising that the native oxide inhibits the In/GaAs reaction.

4.3.3 Comparison with Other M/GaAs Reactions

Chemical reactions between deposited metals and the native oxide on GaAs have been examined by Kowalczyk et al.[45] using x-ray photoemission spectroscopy. It was demonstrated that the (100) GaAs surface covered with a 1 ~ 2 nm thick native oxide layer can be altered by chemical reaction with the electropositive metals Al, Mg, Ti and Cr at the room temperature. Whereas, the more electronegative metals Au, Ag and Cu are inert with respect to the native oxide. As described in Ref. 45, the Gibbs free energy ΔG calculated for M/oxide reaction together with the experimental results indicates that the electropositive metals should reduce the initial native oxide layer on the GaAs surface to produce an interface region which consists of a non-insulating mixture of metal and metal oxide. The predicted chemical reactivities of deposited metals with the native oxide on GaAs are

summarized in Table 1. Of course, this crude analysis ignores the possibility of ternary oxide phases.

From a practical standpoint the effect of metal-native oxide interactions on metal-GaAs reactions is of primary importance. For example, Keramidas[46] showed that addition of a small amount of Al between Au-Be and AlGaAs enhanced the Au-Be/AlGaAs reaction. Evidently the Al reduced the native oxide on AlGaAs, causing the oxide to ball up thereby allowing direct contact between Au-Be and AlGaAs. In a study of the Ni/GaAs, Pd/GaAs and Pt/GaAs reactions, Sands et al.[36] found that the Pd-GaAs reaction mechanically disperses the native oxide during deposition of Pd whereas the Ni/GaAs reaction is completely prevented locally by the thin native oxide layer (1 ~ 2 nm) at temperatures up to 220°C. In regions where the Ni penetrates the native oxide through pores, cracks or thin spots, the residual native oxide is pushed toward the surface, eventually ending up on the surface when the reaction is complete. On the other hand, since both Pt and Ga are moving species during the Pt/GaAs reaction, the residual native oxide resides between the PtGa and $PtAs_2$ layers when the reaction is complete.

Of the three reactions, Ni/GaAs, Pd/GaAs and Pt/GaAs, only the Ni/GaAs reaction is noticeably inhibited by the native oxide layer. In examining Table 1, we see that Ni is situated between Ga and As in its affinity for oxygen. Thus Ni may have some limited interaction with the native oxide layer. From Table 1, one would expect In/GaAs,

Table 1. Summary of interfacial chemistry for several metals deposited on native oxide surfaces of GaAs.

Metal	Reaction with the native oxide (Ga_2O_3 + As_2O_3) predicted[a]	Oxide Products	ΔG (Kcal/mol)[b] Reacted with Ga_2O_3	ΔG (Kcal/mol)[b] Reacted with As_2O_3	ΔH (kcal/mol)[b] Heat of Formation of M_xO_y per oxygen	X (element)[c] Electronegativity (Pauling Scale)
Au	No	Au_2O_3	278.0	177.0	-0.72	2.4
Ag	No	AgO	249.0	148.0	-2.7	1.9
Pt	No	Pt_3O_4	--	--	-9.8	2.2
Pd	No	PdO	--	--	-20.0	2.2
Cu	No	CaO	149.0	-8.0	-37.6	2.0
As	--	As_2O_3	--	--	-50.3	2.0
Ni	No	NiO	83.5	-17.2	-51.7	1.8
In	No	In_2O_3	40.1	-60.0	-73.8	1.7
Ga	--	Ga_2O_3	--	--	-86.2	1.6
Cr	Yes	Cr_2O_3	-11.0	-112.0	-90.0	1.7
Ti	Yes	Ti_2O_3	-107.0	-208.0	-122.0	1.5
Al	Yes	Al_2O_3	-138.0	-239.0	-133.3	1.5
Mg	Yes	MgO	-169.0	-270.0	-143.8	1.2

[a] Prediction based on thermodynamic data presented in this table.

[b] The free energies used to calculate the ΔG's were obtained from Handbook of Chemistry and Physics, 64th ed., edited by R.C. Weast (CRC Press, Florida, 1983) and Lange's Handbook of Chemistry, edited by J.A. Dean (McGraw-Hill, New York, 1979).

[c] H. Hotop and W. C. Lineberger, J. Phys. Chem. Reference Data, 4, 539 (1975).

the subject of the current study, to behave in a similar manner to Ni/GaAs with respect to the native oxide layer. Indeed, the In/GaAs reaction has been shown above to be greatly impeded by the presence of an intervening oxide layer. The exact mechanisms behind this behavior, however, remain unclear. Certainly, the metal's affinity for oxygen, the morphology of any reaction products and the magnitude of the chemical driving force for the M/GaAs reaction must all be considered as important factors in determining the role of the native oxide in M/AB reactions.

5. SUMMARY

The principal conclusions of this investigation are summarized below:

1. The mechanism of the In/GaAs reaction is revealed by TEM study to be: the dissolution of Ga and As from the substrate into the molten In at 350°C, and the precipitation of epitaxial islands of $In_{1-x}Ga_xAs$ ($x < 0.2$, $x > 0.8$) on the new GaAs surface during annealing and cooling. The observed interface morphology shows that the interface is abrupt, and misfit dislocations appear at the interface between the epitaxial $In_{1-x}Ga_xAs$ and the GaAs substrate.

2. The SEM and TEM images show the surface morphology of as-deposited indium on the (100) oxide-free GaAs substrate. The results indicate that the as-deposited In islands have a rectangular shape with a size of about 0.4 x 0.4 $(\mu m)^2$. The edges of the islands are aligned along the <110> directions of the substrate. The rectangular shape of the indium islands is due to the effects of the interfacial lattice mismatch and the surface energy of indium.

3. The orientation relationships between the as-deposited indium and the oxide-free GaAs substrate, together with the InAs patch formed near the interface and the indium oxide In_2O_3 on the surface of the In island, have been revealed by the electron diffraction analysis to be:

$$[0\bar{1}1]_{GaAs} \| [1\bar{1}\bar{1}]_{In} \| [0\bar{1}1]_{InAs} \| [01\bar{1}]_{In_2O_3}$$

$$(100)_{GaAs} \| (110)_{In} \| (100)_{InAs} \| (100)_{In_2O_3}$$

4. The phenomenon of faceting of the indium patches on the GaAs substrate and the $In_{1-x}Ga_xAs$ phases formed after annealing have been observed by TEM. The orientations of the facets on the indium island and $In_{1-x}Ga_xAs$ phase are determined to be $\{011\}_{In}$, $\{110\}_{In}$ and $\{111\}_{In_{1-x}Ga_xAs}$, $\{100\}_{In_{1-x}Ga_xAs}$ which have low surface energy and stable surface structure.

5. The effects of the thin native oxide layer on the as-deposited and annealed samples have been studied by SEM and TEM techniques. The observations of the arbitrarily shaped indium islands and the interface morphology indicate that the native oxide layer disrupts the orientation relationship between the as-deposited indium and the GaAs substrate, and also greatly inhibits the In/GaAs interface reaction during annealing at 350°C for 10 minutes.

6. CONCLUSION AND FUTURE WORK

The mechanism of the In/GaAs reaction at 350°C and the In/GaAs interface morphologies with and without the intervening native oxide both before and after annealing at 350°C have been determined. The results show that it may be impossible to obtain a graded heterojunction layer of $In_{1-x}Ga_xAs$ at the interface by annealing at 350°C due to a miscibility gap in the InAs-GaAs system. Thus, a graded band gap, which should result in extremely low specific contact resistivity, cannot be obtained by annealing at 350°C. This is puzzling since Lakhani observed the lowest contact resistance after annealing at 350°C. On the other hand, the inhibition of the In/GaAs reaction by the intervening native oxide makes the ohmic contact fabrication impractical since an oxide-free interface can only be obtained under UHV conditions.

These results raise new questions regarding our basic understanding of the In/GaAs system from the structural, electronic and thermodynamic points-of-view. Further work is clearly necessary.

A systematic study of the effects of annealing temperature on the interface morphology and electronic properties of the In/GaAs heterojunction would be of both fundamental and practical interest. It would also be interesting to study the structure of $In_{1-x}Ga_xAs$ layers grown at higher temperatures and then annealed at 350°C in order to establish the existence of a miscibility gap in the InAs-GaAs pseudobinary system. A study of the In/Pd/GaAs system would also be of practical interest since the Pd/GaAs reaction can disperse the native oxide

layer mechanically during deposition of Pd so that indium may be free to react with the GaAs substrate in a manner similar to the reaction between In and UHV cleaned GaAs.

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