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Thermal Analysis of Five-Level Flying Capacitor Active Neutral Point Clamped
Converter and Dual Flying Capacitor Active Neutral Point Clamped Converter

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical Engineering

by

Yiming Ma

2015

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ABSTRACT OF THE THESIS

Thermal Analysis of Five-Level Flying Capacitor Active Neutral Point Clamped Converter and Dual Flying Capacitor Active Neutral Point Clamped Converter

By

Yiming Ma

Master of Science in Electrical Engineering

University of California, Irvine, 2015

Professor Keyue Ma Smedley, Chair

Derived from classic DC-AC multilevel converters, hybrid multilevel converters can combine distinct advantages, thus receiving increasing attention for their widespread industrial applications recently. The Active Neutral Point Clamped (ANPC) converter offers redundant switching states to achieve a better control and more even loss distribution compared to Neutral Point Clamped (NPC) converter. However, in terms of five-level converters, currently the only topology applied in industrial application is the Flying-Capacitor based Neutral Point Clamped converter (FCANPC), which gives a relatively good performance with a simple structure. Despite its advantages, the uneven loss distribution cannot be disregarded as a substantial drawback to affect the power processing capability. The Dual Flying Capacitor Neutral Point Clamped (DFCANPC) converter has been newly proposed to provide better loss balancing and "soft commutation" to have a higher power capability and efficiency.

In this thesis, traditional multilevel topologies such as Cascaded H-Bridge converter, Diode Clamped converter, and Flying Capacitor converter are summarized, followed by popular modulation schemes including carrier-based modulation, Space Vector Modulation and Selective Harmonic Elimination modulation. Thermal models and cooling strategies are then briefly discussed. As the main focus, thermal analysis and comparison regarding the five-level FCANPC converter and the newly proposed DFCANPC converter is reported in this thesis. A PSIM model has been built for verification of loss balancing performance of the DFCANPC converter.

CHAPTER 1

INTRODUCTION

DC-AC power inverters have been widely used in applications including uninterruptible power supplies, photovoltaic systems, power grid, high-voltage direct-current (HVDC) power transmission and electric motor speed control. The increasing demand for power energy calls for improvement in energy efficiency and power quality.

Medium-voltage (MV) inverter has been gradually introduced into the power electronics community with the development of semiconductor devices such as GTOs, IGBTs and GCTs which quickly became dominant for high power situations due to their outstanding switching characteristics. Compared with traditional two level converters, multilevel converters offer various benefits, including higher voltage capability, better power quality, and less switching loss [1][2]. Recently, MV power conversion has received increasing attention due to its potential for widespread applications across the energy sector. Examples are practical multilevel topologies in combination with active filters [3], renewable energy generation to the utility grid [4], multilevel converter with separate DC sources for large electric drives [5], the universal power conditioner for electrical distribution systems [6], and other applications [7][8].

The primary objective of multilevel converters is to acquire high voltage capability with lower voltage semiconductor devices. This can eliminate the need for a bulky transformer for stepping up the voltage to serve the medium voltage

applications and therefore lower the cost and improve energy efficiency. Technical challenges include device switching frequency, device voltage stress, dv/dt, and so on. As an example, it has been discussed in [9] the challenges regarding efficiency, EMI and short circuit protection for multilevel converters to be used for HVDC transmission.

To meet such requirements, various hybrid multilevel converter topologies have been derived from combination of conventional multilevel converters such as Cascaded H-Bridge converter, Diode Clamped converter and Flying Capacitor converter. Three-level Neutral Point Clamped (NPC) converter [10], five-level H-bridge NPC converter [11], and modular multilevel converter for power transmission [12] are among the useful topologies. Thermal and efficiency analysis is also conducted to provide a criteria to compare between topologies for various cases [13]–[17].

For applications in need of higher-level converters for the purpose of higher voltage capability as well as better power quality and efficiency, currently the only five-level converter seen in industrial application is the five-level Flying Capacitor based Active Neutral Point Clamped (FCANPC) converter [18]. The FCANPC converter avoided the large number of capacitors which exist in the same level FC converter and offers a comparatively good performance with a feasible structure. Also, different modulation techniques have been applied to control the FCANPC converter successfully, carrier based modulation, Space Vector Modulation (SVM) and Selective Harmonic Elimination (SHE) modulation included.

Even though the five-level FCANPC converter is in use in industrial applications, drawbacks such as uneven loss distribution and the requirement of transient voltage balancing snubber for series-connected devices exist. The loss balancing problem is worth great attention, as the devices with maximum loss would limit the switching frequency and output power rating. In the effort to improve the power processing capability, a new hybrid multilevel converter, the dual Flying Capacitor Active Neutral Point Clamped (DFCANPC) converter, has been proposed recently [19][20]. Its advantageous features include more even loss distribution and transient voltage balancing snubber elimination.

The main target of this thesis is to analyze and compare loss distribution of the five-level FCANPC converter and DFCANPC converter. Classic multilevel converter and modulation techniques are reviewed in chapter 2, followed by converter thermal analysis basics in Chapter 3. Chapter 4 compares the circuit topologies and features of FCANPC and DFCANPC, and Chapter 5 provides the simulation and analysis of loss distribution of both converters.

CHAPTER 2

CLASSIC MULTILEVEL CONVERTER AND MODULATION

The MV power converters are widely used in industry, for example, for pumps in water treatment stations, fans in the cement industry, and traction applications in transportation [21]. The power ratings typically range from 0.4 MW to 40 MW, with voltage levels varying from 2.3 kV to 13.8 kV [21]. The attraction of MV power converters lies in the better harmonic spectrum and higher voltage that they achieve.

The Insulated Gate Bipolar Transistor (IGBT), compared with all kinds of semiconductor devices, functions as the main switching device for various MV power converters with advantages such as higher speed, lower switching loss and better performance on protection and control. As the power applications promote the development of semiconductor industry, a variety of multilevel converter structures are also sprouting and growing.

Traditional multilevel converters, such as the Cascaded H-Bridge converter, the Diode Clamped converter and the Flying Capacitor converter, have distinct features and are also of substantial value themselves. In addition, they can also be rearranged and combined for the later hybrid topologies. Features of the three traditional converters mentioned above are summarized below.

2.1 Conventional Multilevel Converters

Cascaded H-Bridge Multilevel Converter

The name Cascaded H-Bridge Multilevel Converter came from the fact that the identical H-Bridge cells are connected in a series chain at the ac side for the purpose of achieving high AC voltage and low harmonic distortion in medium voltage applications [21]. The number of such cells should meet the requirements of working condition, harmonic requirements and manufacturing cost, and higher-level converters can help achieve lower line-current distortion and higher input power factor. As is indicated in [21], the voltage level of a Cascaded H-Bridge converter is defined by

$$m = 2H + 1 \tag{1}$$

where H is the number of H-Bridge cells in each of the three phases. For any multilevel converter, an m-level converter means that its output phase voltage is m level and line voltage is (2m-1) level. The circuit topology of a five-level Cascaded H-Bridge converter is presented in Fig. 2.1. Due to its cascaded connection, the equal voltage sharing problem is removed for series-connected devices so that the "resistor capacitor diode" snubber and its loss are avoided. The modular structure of the multilevel converter itself is already beneficial from the cost point of view, and the number of components is smaller than other topologies. However, each of the H-Bridge cells is fed by an isolated dc supply, which may shift up the cost and limit its application. For a three-phase system, two connection options as either Y or $\triangle$ are also available for the output voltages of three phases [1].

Applications of Cascaded H-Bridge converter include active filters, power factor compensators, dc power source utilization, electric vehicle drives, interfacing with renewable energy resources, and so on.

In addition, Cascaded H-Bridge converter can also operate with unequal dc voltages. The advantage is that the voltage levels can be increased without increasing the Cascaded H-Bridge cells [21]. However, in this way the converter would lose its modular configuration advantage and the modulation would need to be more sophisticated due to the lack of redundant switching states. These drawbacks make it infeasible for industrial application.
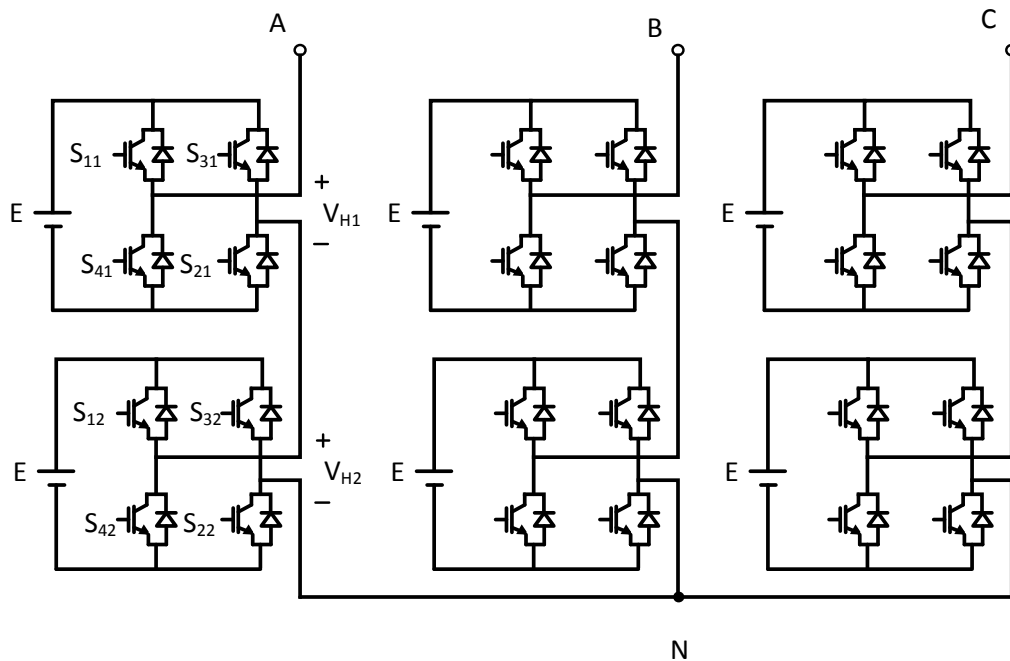
Fig. 2.1 Five-level Cascaded H-Bridge converter

Diode Clamped Multilevel Converter

The Diode Clamped multilevel converter, also known as Neutral Point Clamped converter, has been used in high power industry. The clamping diodes and cascaded dc capacitors, together with the IGBT switch units, are significant parts to produce ac voltages at different levels [22]. The topology of a Neutral Point Clamped converter is shown in Fig. 2.2, and single-phase diagram structure of the five-level

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Diode Clamped converter is shown in Fig. 2.3. Features of Diode Clamped converter are listed below.
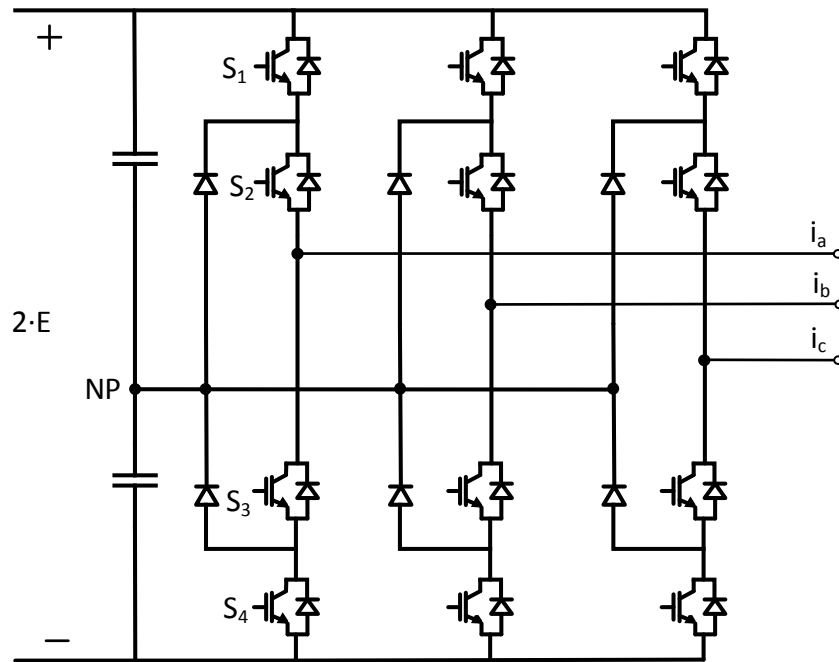
Fig. 2.2 Three-level Neutral Point Clamped converter

Advantages:

(a) The voltage stress of each swtich is a certain amout (e.g. $1/2$ V_{dc}, $1/4V_{dc}$) of the dc-link voltage so there is no dynamic voltage sharing problem. For example, the switch in NPC converter withstands half of the dc-link voltage.

(b) It can achieve static voltage equalization by choosing the leakage current of the outer switches to be higher than that of the inner switches.

(c) Low dv/dt and low THD can be reached thus filters can be avoided when the voltage level is high.

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(d) High effeciency is realized due to the fundamental operating switching frequency for all switches.

Disadvantages:

(a) It requires excessive number of clamping diodes for higher level converters, which makes it less attractive for implementation.

(b) Unbalanced voltage of dc-link capacitors at levels greater than three limits the application of this topology.

The Diode Clamped converter can be applied for static var compensation, variable speed motor drives, high voltage system interconnections and medium voltage dc and ac distribution lines.
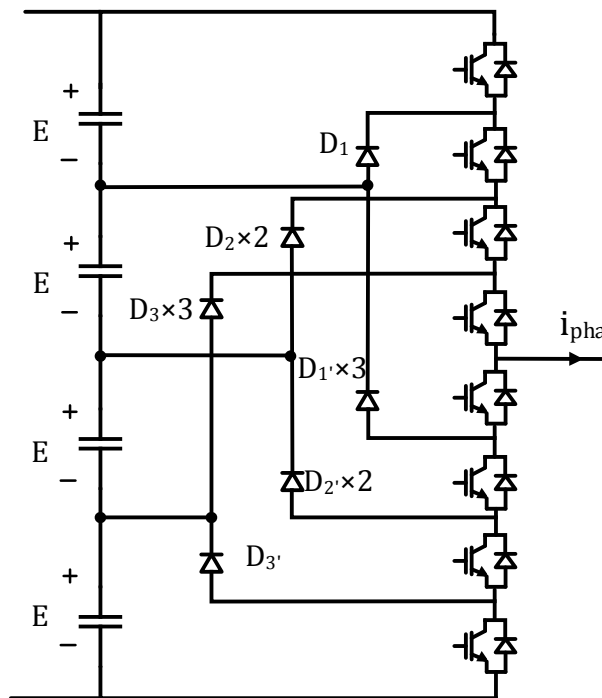
Fig. 2.3 Single-phase diagram of five-level Diode Clamped converter

As shown in Fig. 2.3, the five-level Diode Clamped converter needs twelve clamping diodes per phase. The result is that the number of clamping diodes reaches

thirty six for the three-phase converter, far more than only six such diodes of the three-level NPC converter. Thus, the strikingly increased number of clamping diodes becomes the main reason why the higher-level Diode Clamped converter is not as widely used as three-level NPC converter.

Flying Capacitor Converter

The single-phase circuit diagram of the five-level Flying Capacitor converter is shown in Fig. 2.4. The Flying Capacitor converter requires a large number of dc storage capacitors. An m-level converter will require as many as $(m - 1) \times (m - 2)/2$ auxiliary capacitors each phase and $(m - 1)$ DC bus capacitors [1]. Based on its structure, the benefits and drawbacks are presented below.
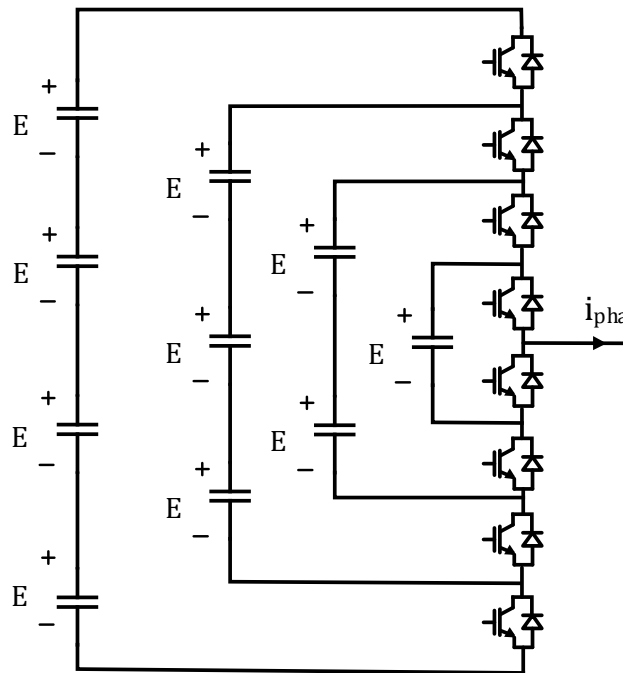
Fig. 2.4 Single-phase diagram of five-level Flying Capacitor converter

Advantages:

(a) The control scheme is flexible because of the switching state redundancy. By selecting different switching combinations, the flying capacitor voltages can be regulated.

(b) Low THD can be reached thus ac filters can be shrunk in size or even avoided.

(c) The switching and conduction losses are evenly distributed among the switches.

Disadvantages:

(a) Excessive number of flying capacitors at higher levels increases the initial cost and maintenance surcharges and decreases the reliability of the converter.

(b) The trade-off between switching frequency, output current, and capacitor size limits the nominal power of the converter.

(c) Control scheme becomes more complicated due to the capacitor voltage deviation.

(d) The flying capacitors need to be pre-charged for the converter to start normal operation.

There are lots of applications which can be realized with Flying Capacitor converter, such as induction motor drive, static var generation, ac-dc and dc-ac conversion, active rectifiers and so on.

Although Flying Capacitor converter has an outstanding performance in even loss distribution, because of the large number of capacitors it requires especially for

high-level converters, the use of the Flying Capacitor converter is limited in real applications.

2.2 Modulation Techniques

While the two level H-Bridge inverter can use the simple modulation methods such as unipolar or bipolar PWM, multilevel converters has more options in the choice of modulation techniques, including carrier-based PWM and non carrier-based PWM such as Space Vector Modulation (SVM) and Selective Harmonic Elimination (SHE), which are briefly introduced below. Due to more switches involved in the multilevel converters, the modulation techniques are more complicated compared to two-level ones.

Carrier-Based PWM Schemes

The Sinusoidal Pulse Width Modulation (SPWM) is a well-known modulation technique for power electronics converters, multilevel converters included. The switching signals are generated for the IGBTs by comparing between a sinusoidal wave and triangular waves in SPWM, where the sinusoidal wave is also named the modulation signal and the triangular signal is called the carrier signal. Therefore, SPWM is also referred to as the carrier-based PWM, which falls into two large categories: phase-shifted modulation and level-shifted modulation.

In phase-shifted modulation where an m level converter needs (m-1) triangular carrier waves with the same amplitude and frequency, the phase shift between the adjacent carriers is given as

$$\varphi_{cr} = \frac{360^{\circ}}{m-1} \tag{2}$$

The modulation waves and triangular waves for the five-level Cascaded H-Bridge converter are shown in Fig. 2.5.
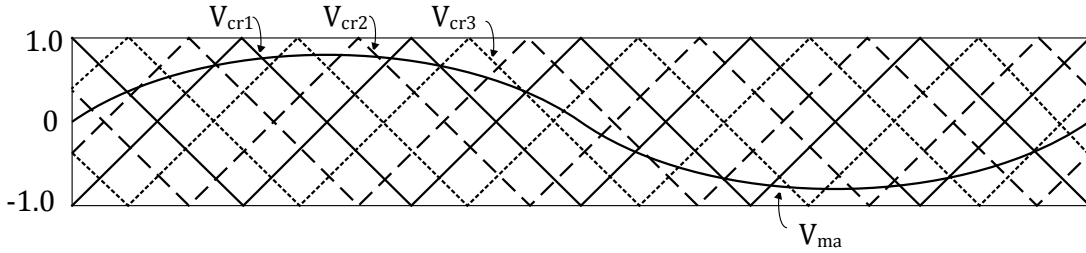
Fig. 2.5 Phase-shifted modulation for five-level CHB converter

(a) In-phase disposition (IPD)

(b) Alternative phase opposite disposition (APOD)

(c) Phase opposite disposition (POD)
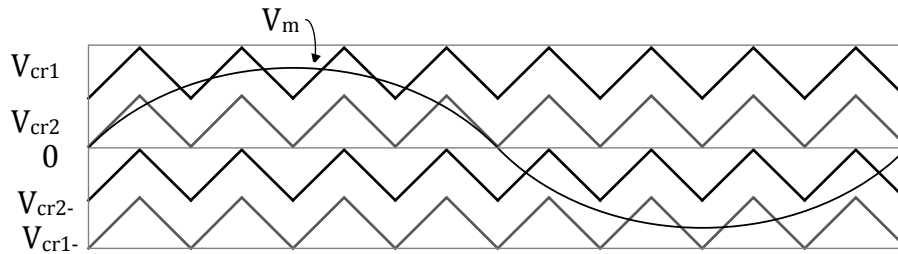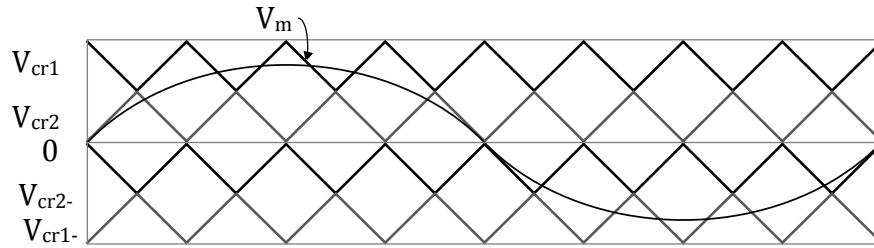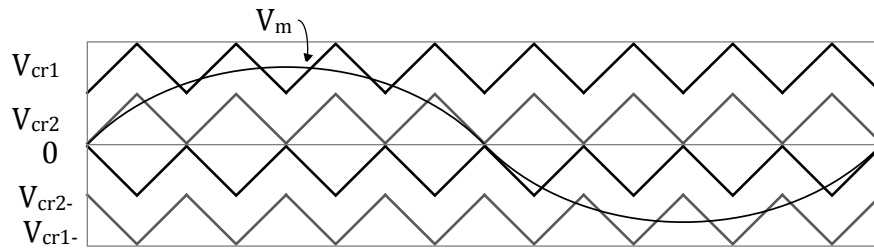
Fig. 2.6 Level-shifted modulation for five-level inverters for five-level converters

Also, the same as phase-shifted modulation, an m level converter with level-shifted modulation needs (m-1) triangular carrier waves with the same amplitude

and frequency, but the carriers are vertically shifted and may be different in terms of phase. Based on the difference in phase of the shifted carriers, the level-shifted scheme can be classified into three categories, which are shown in Fig. 2.6.

The first one is called in-phase disposition (IPD) with all carrier waves in phase. The second one is named alternative phase opposite disposition (APOD) with carriers alternatively in opposite phase disposition. The third one is referred to as phase opposite disposition (POD) with all carriers above zero reference in phase and all carriers below zero reference in the opposite phase with that of the above-zero carriers [21]. Comparatively, the APOD has more spread power in the first group of sideband harmonics, which makes it a better candidate for single-phase converters. The IPD has a better capability to concentrate the power on the switching frequency such that it is widely used in three-phase configurations.

By comparing the carrier-based modulation, the conclusion can be reached that the device switching frequency and conduction period is the same for all devices in phase-shifted modulation while they are different in level-shifted schemes.

Space Vector Modulation

Take the Neutral Point Clamped converter for example. Switching states can be used to denote different operation status. The states "P", "O", "N" represent the converter phase voltage to be $+V_{dc}/2$, 0, $-V_{dc}/2$ respectively. As there are three phases, the total of 27 switching states can be used for the modulation. The space vector diagram for NPC converter is shown in Fig. 2.7. In this way enough switching state redundancy is provided to make good use of the zero, small, medium and large

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vectors for the purpose of different requirements for switching sequence design such as minimum switching transitions and low neutral point deviation. From the states, the status of the switches can be determined to be on or off.
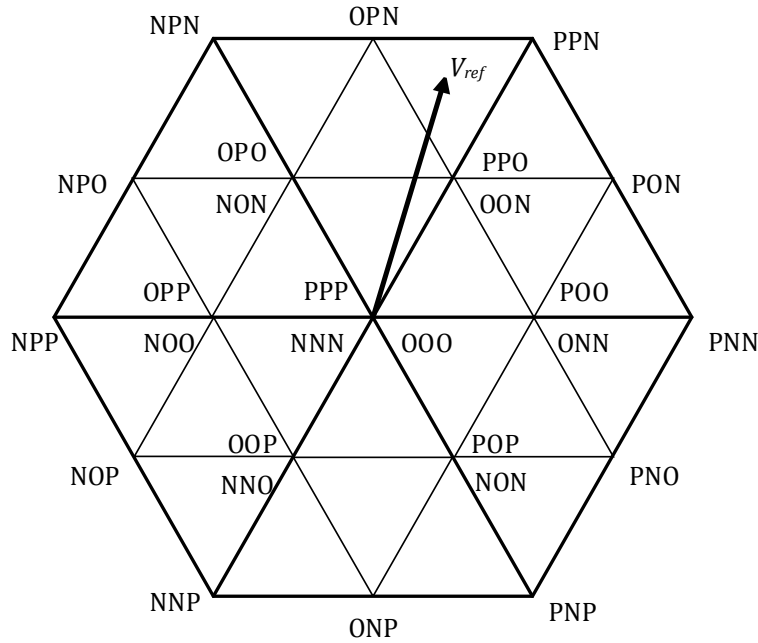
Fig. 2.7 Space vector diagram for NPC converter

Selective Harmonic Elimination PWM

Among different modulation schemes which are in use for conventional multilevel converters to get better quality control signals, SHE-PWM has been found to be a very efficient modulation scheme regarding to lowering total harmonic distortion (THD). The SHE-PWM control for full-bridge three-level inverters was proposed in [23]. The controlling criterion is set to be the harmonics elimination of either a specified order or a band of specified frequencies.
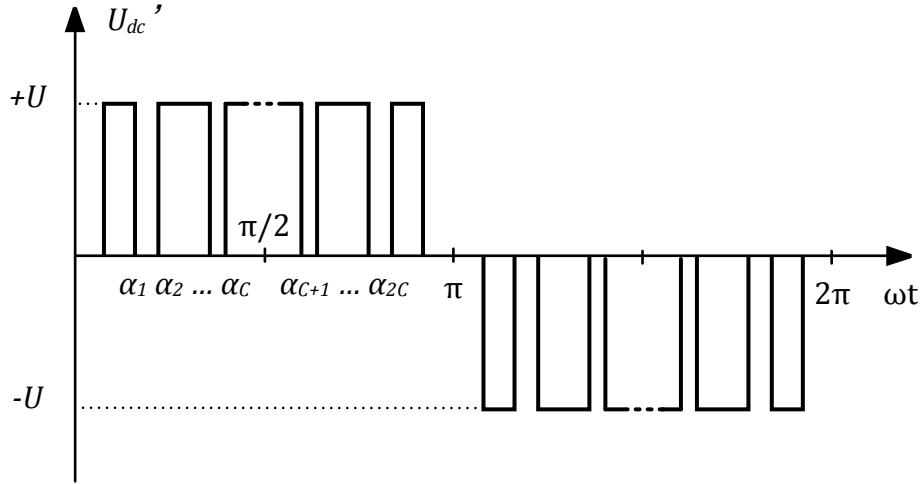
Fig. 2.8 Generalized three-level SHE-PWM waveform

In the recent publications, it is shown desirable that the low-order harmonics are eliminated, including harmonic orders of 3, 5, 7, 9, 11,... for single-phase system and the orders of 5, 7, 11, 13, 17,... for the three-phase system. It is shown in Fig. 2.8 an example of the generalized SHE-PWM waveforms for three-level inverters.

Because the Fourier transform will only show the existence of odd harmonic components and there is quarter symmetry property of the waveforms of these harmonic components, the following equations are given [23]:

$$U'_{dc}(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \tag{3}$$

$$a_n = \frac{4}{\pi} \int_0^{\pi/2} U'_{dc}(\omega t)\sin(n\omega t)d\omega t \tag{4}$$

After some calculation, the non-linear equations below are acquired for describing the system.

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cdots \pm \cos(\alpha_C) = \frac{\pi}{4} M \\ \cos(n\alpha_1) - \cos(n\alpha_2) + \cdots \pm \cos(n\alpha_C) = 0 \end{cases} \tag{5}$$

$$\alpha_1 < \alpha_2 < \cdots < \alpha_c < \frac{\pi}{2} \tag{6}$$

Where α is the switching angels, C is the switching angle index, n is the odd harmonic order and M is the modulation index with $M = \frac{h_1}{U_{dc}}$ (h_1 is the fundamental component of the output voltage and U_{dc} is the dc-link voltage).

To solve the non-linear system, some approximation algorithm such as Newton-Raphson method must be applied, which is a drawback of this modulation scheme. In this way, switching angles α can be calculated for each modulation index. After the fundamental harmonic amplitude is set, a number of C-1 harmonics following the first can be eliminated.

As the solutions for SHE-PWM in three-phase case are not unique, standards have been discussed recently on selection among results. One of the common criteria is to adopt a solution with low THD, which becomes the reason why SHE-PWM has been found as a desirable strategy to improve output voltage quality.

However, as SHE-PWM is an off-line modulation scheme, it is difficult to have it implemented in the closed-loop system due to the difficulty and complexity in the detection and obtaining the modulation phase. Therefore, the carrier based Selective Harmonic Elimination method has been introduced in [24] for three-level NPC converter.

The carrier based SHE is to approximate the SHE scheme to a carrier based modulation. The idea is to achieve a modified carrier wave to change the switching moments with a similar effect to what is achieved from SHE.

It has been shown the comparison on the modulation effect of SPWM, SHE and carrier-based SHE schemes with regard to THD and weighted THD related to harmonic position. The effect of the proposed carrier-based SHE is better than that of PWM but a little worse than SHE. However, it is still a good compromise to decrease THD for a closed-loop system.

It is reviewed in this chapter the conventional multilevel converters and popular modulation techniques. The Cascaded H-Bridge converter, Neutral Point Clamped converter and Flying Capacitor converter display distinct features and thus provide ideas for the later hybrid topologies to reach higher needs and give better performance. Carrier based (phase-shifted modulation and level-shifted modulation) and non-carrier based modulation schemes (SVM and SHE-PWM) are both capable of producing functional control signals. Some new modulation techniques have also been invented to appropriate SHE-PWM to bring its advantages to carrier based schemes for closed loop system. Trade-off between pros and cons should be taken into consideration on selection among topologies and modulation methods.

CHAPTER 3

THERMAL BASICS OF POWER CONVERTER

As mentioned earlier, the most essential target of using multilevel converters is to realize high voltage with low voltage semiconductor devices. Given the condition where a multilevel converter can perform the function for power conversion, one of the issues which should be taken into consideration is how well they can handle such conversion, that is, if they are reliable and efficient. It is also clear that the loss affects the device's temperature which will further influence the life expectancy and reliability of the converter. In terms of thermal analysis, temperature has been the main target, as high temperature may damage devices, require higher-performance cooling system, and raise the size and cost of power converters. Therefore, to keep the devices as cool as possible, to maintain highly efficient conversion, and to minimize the loss are mostly concerned. Basic thermal parameters and circuit modeling approaches are given below.

3.1 Definition of Junction Temperature Standards

Specific standards have been defined by the International Standard IEC for the parameters of insulated-gate bipolar transistors (IGBTs), among which the following are the most basic and widely used ones when it comes to thermal behavior. The definitions below are provided in [25].

"The junction temperature T_{vj} is the temperature in the junction region of a semiconductor chip. The junction temperature is to determine the thermal resistance junction to case R_{thJC} used for further calculations."

"The rated maximum operation junction temperature T_{vjmax} is used to determine the maximum allowable power dissipation of a continuously turned on IGBT (i.e. static operation). For switching operation, it has to be ensured that the device safely operates under high dynamic stress, short dynamic temperature transients and operational chip-and-module inhomogeneities."

Compared with T_{vj} and T_{vjmax}, the most practical value for real applications design is the operating temperature T_{vjop}, which determines the maximum and minimum limits of the junction temperature in which the semiconductor is operated safely [25].

3.2 Thermal Equivalent Circuit Models

The common way of calculating IGBT thermal impedance is related to the constant power consumed in the power stage and the difference of the measured temperatures of the heating and cooling phase[26]:

$$Z_{thjc}(t) = \frac{T_j(t) - T_c(t)}{P} \tag{7}$$

Due to the difference in thermal resistance and the aging phenomena, disagreement exists for the position of the thermal interface resistance. Two thermal interface modeling circuits are shown in Fig. 3.1. The transformation equation between the two models is presented below [26]. In some cases it is necessary to use the case to heat sink thermal resistance for the module as a whole, while such resistance is more likely to be given separately for IGBT and diode in recent datasheets as it represents more realistic cases.

$$R_{thc-h,module} = \frac{R_{thc-h,IGBT} \cdot R_{thc-h,Diode}}{R_{thc-h,IGBT} + R_{thc-h,Diode}} \tag{8}$$

Two thermal circuit models are introduced here among different models for analysis, which are shown in Fig. 3.2 and Fig. 3.3 respectively.
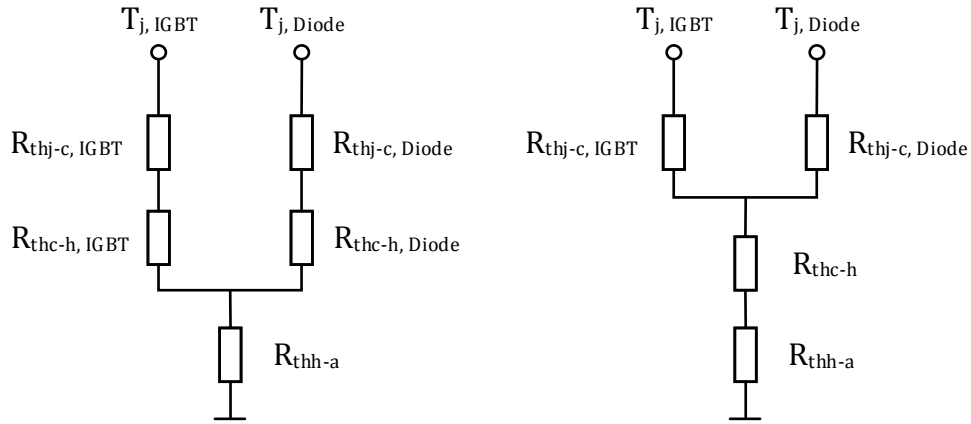

Fig. 3.1 Thermal interface model
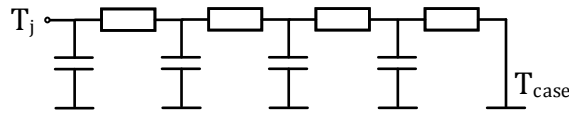
Fig. 3.2 Continued fraction model
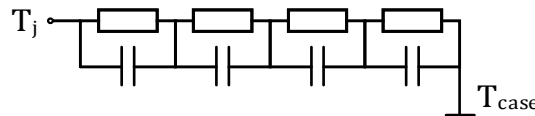
Fig. 3.3 Partial fraction model

Continued fraction circuit represents the physical setup of the semiconductor devices with thermal capacities and intermediary thermal resistances. Internal temperatures of each layer sequence that is represented with the RC pair are accessible by the network nodes. The RC pairs in partial fraction model, in contrast, do not have physical significance. The coefficients which are regularly provided in datasheets as r and τ can be easily calculated from the measured cooling curve. In application, continued fraction model is used where the characteristics of each

physical layer are given, while partial fraction model is widely applied for mathematical calculation and analysis using datasheets [27].

Equations are provided to calculate the device junction temperature by using the partial fraction model coefficients in [27]:

$$Z_{thj-c}(t) = \sum_{i=1}^{n} r_i \times (1 - e^{-\frac{t}{\tau_i}})$$
(9)

where r_i and τ_i are thermal coefficients and can be found in datasheets.

$$T_j(t) = P(t) * Z_{thj-c}(t) + T_{case}(t)$$
(10)

To analyze thermal performance in real applications, it is required to combine thermal circuit models of the IGBT and of the heat sink. In theory, both the continued fraction model and the partial fraction model can be applied for the merge. However, the continued fraction model has the limit that only one material of a specific heat sink can be considered each time, thus it will not work when the real case deviates from the simulation. Comparatively, the partial fraction model is measurement-based so that it can be easily set up by following datasheets for either a specific device or several devices as a whole. Two different approaches can be used to attain the partial fraction model for a system. One is to series-connect the partial fraction model of each device from the junction of IGBT, thermal grease, heat sink to ambient. It has some discrepancy due to the reverse effect of the heat sink on the thermal spreading of IGBT, and thus can affect the time response and the value of IGBT thermal resistance. In contrast, the other approach eliminates the fault by way of measuring simultaneously the thermal resistance and the entire thermal path.

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It is advantageous to investigate the thermal performance from the point of view of the whole chain of system thermal resistance. However, under the condition where it is impossible for the measurement of the system thermal resistance, the merge of the partial fraction model can be applied to get the system performance.

3.3 Cooling Strategies

Silicon has long been the dominant material for power electronics semiconductor devices. In addition, materials like SiC and GaN are capable to operate at even higher temperature. Nevertheless, what limit the real operating temperature to up to 175°C are not only the peripheral components and soldering materials from substantiality point of view, but also the consideration for the cost and the safe and reliable operating condition margins. A low temperature discrepancy is required between the semiconductor and the coolant for automotive applications, industrial drives, HVDC power transmission etc [28]. In order to deal with such issue, a variety of cooling approaches have been raised and in use by industrial power electronics companies, which can be classified into air cooling and liquid cooling as two basic kinds of realization.

Air cooling is the most wide spread and conventional way to cool down the IGBT module because of its low cost and good reliability. Systems that use air cooling transmit the heat directly from the heat sinks to the air either by natural or forced convection. This cooling method is the most effective for the lower power system but the use may be limited for high power density situations.

However, liquid cooling, say water cooling, would transfer heat from the system to the liquid which further transmits the heat into the air through a particular device. It is more beneficial in increasing semiconductor life and decreasing the package size. Advantages as smaller cooling package, better heat removal effect and lower noise make it suitable for all kinds of IGBT modules, particularly high power components. For demanding applications as in power generation, transportation and military equipment, liquid cooling plays a big role.

In this chapter, some important standards are reviewed to describe the thermal performance of power converters, among which the most practical is the device operating temperature T_{vjop}. The continued fraction model and partial fraction model are briefly discussed to extract thermal circuits for calculation. In addition, cooling methods also play a big role in the converter operating condition.

CHAPTER 4

COMPARISON OF FCANPC AND DFCANPC

The application of traditional multilevel converters in medium-voltage high power applications is widely recognized over recent decades. However, in order to utilize higher-level converters and take advantages of their better performance, problems must be overcome such as the increasing number of the isolated power supplies for the Cascaded H-Bridge Converter and the large numbers of capacitors in the Flying Capacitor topology. Given the problems above, hybrid multilevel converters, which rearrange and combine different properties of classic topologies, are discussed during the very recent years. The case of Diode Clamped converters, Neutral Point Clamped converter in particular, is discussed below.

The Neutral Point Clamped converter has gained success due to its advantages such as low THD, good reliability and comparatively low cost, particularly in the low and moderate frequency from 200 Hz to 1 kHz [10]. However, its drawbacks have also caught the industry's attention to seek for better solutions.

The neutral point voltage deviation problem has long been recognized, and various techniques have been discussed to effectively balance the neutral point voltage. In [29], the neutral point voltage control is presented using Space Vector Modulation. This method divides the neutral point current to the uncontrollable part generated by the medium switching vector and the controllable part produced by the small switching vector. The balancing function is attained by taking advantage of DQ coordination and adjusting modulation indexes of the neutral point

current. With such strategies, the following three control approaches are provided. The "passive control" can be for the perfectly balanced load and PWM scheme, or for establishing a scale to evaluate other control schemes. The effective hysteresis type control will allow the small switching vectors to move the neutral point voltage in the opposite direction from the direction of unbalanced phase current. The active control scheme which is to control the current modulation indexes by measuring the neutral point voltage unbalance and phase current amplitudes. Each way has its own downsides such as to generate current ripple or to increase the switching loss, but the neutral point unbalance can be solved satisfactorily through weighing the pros and cons and smartly selecting the approach based on the system operating characteristics.

Another significant disadvantage of the neutral point clamped converter is the unequal loss distribution among main semiconductor devices, which will limit the switching frequency and the maximum phase current of the converter [10]. In a quest for equal loss sharing among devices in order to get a higher utilization, the Active Neutral Point Clamped Voltage Source Converter (ANPC VSC) with additional active NPC switches has been proposed [10].

4.1 Active NPC Converter

Comparison of the single-phase diagram of the three-level NPC VSC and ANPC VSC is shown in Fig. 4.1. The active NPC switches in anti-parallel to the NPC diodes make it possible for new commutations and utilization of the NPC paths, thus it can help the ANPC converter to distribute loss more evenly. Furthermore, it is

convenient for industrial implementation for the IGBT modular structure, and the active NPC switches can be turned off by a gate-emitter short if none of them is used [16].
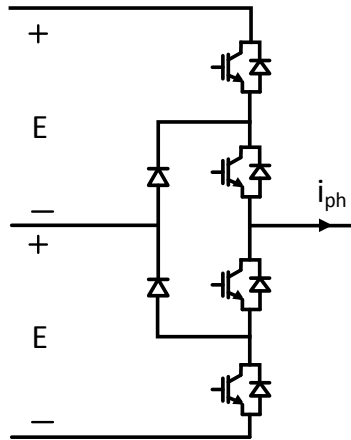
(a) Single-phase diagram of three-level NPC VSC
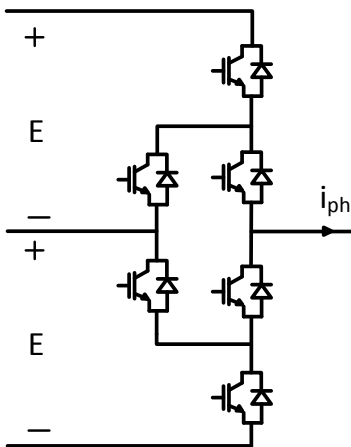
(b) Single-phase diagram of three-level ANPC VSC
Fig. 4.1 Comparison of single-phase diagram of NPC VSC and ANPC VSC

Compared to NPC VSC, the ANPC VSC has more switching states regarding the connection of the phase to the neutral point, which are known as the "0" states. By turning on T_2 and T_5, the phase current can conduct in both directions through the upper path of the neutral tap. Similarly, by turning on T_3 and T_6, the phase current can achieve bidirectional conduction through the lower path of the neutral tap. In

this way, four "0" states are created as "0U1", "0U2", "0L1", and "0L2". The switching

states of the NPC converter and the ANPC converter are shown in Table 4.1 and

Table 4.2, respectively [16]. The equal voltage sharing between T_1 and T_2 during "P"

state is attained by turning on T_6, and in the same manner T_3 and T_4 also achieve

equal voltage balancing during "N" state by turning on T_5. By making use of the

different zero states and commutations, the switching loss can be shifted from one

device to another, thus the ANPC converter can distribute loss more evenly. The

outer devices suffer the most losses at high modulation index while the inner

switches are the most vulnerable at low modulation index. Through always keeping

the most critical devices as cool as possible, higher power rating and longer device

life expectancy can be achieved.

Table 4.1 Switching states of three-level NPC converter

State	S_1	S_2	S_3	S_4
+E	1	1	0	0
0	0	1	1	0
-E	0	0	1	1

Table 4.2 Switching states of three-level ANPC converter

State	S_1	S_2	S_3	S_4	S_5	S_6
+E	1	1	0	0	0	1
0U2	0	1	0	0	1	0
0U1	0	1	0	1	1	0
0L1	1	0	1	0	0	1
0L2	0	0	1	0	0	1
-E	0	0	1	1	1	0

4.2 Flying Capacitor Based Active NPC Converter

In order to meet requirements such as higher voltage capacity and better

waveform quality in high power medium voltage cases, higher-level converters,

such as the five-level converter, are desired. Among a variety of five-level topologies,

currently the only topology seen in industrial applications is the five-level Flying

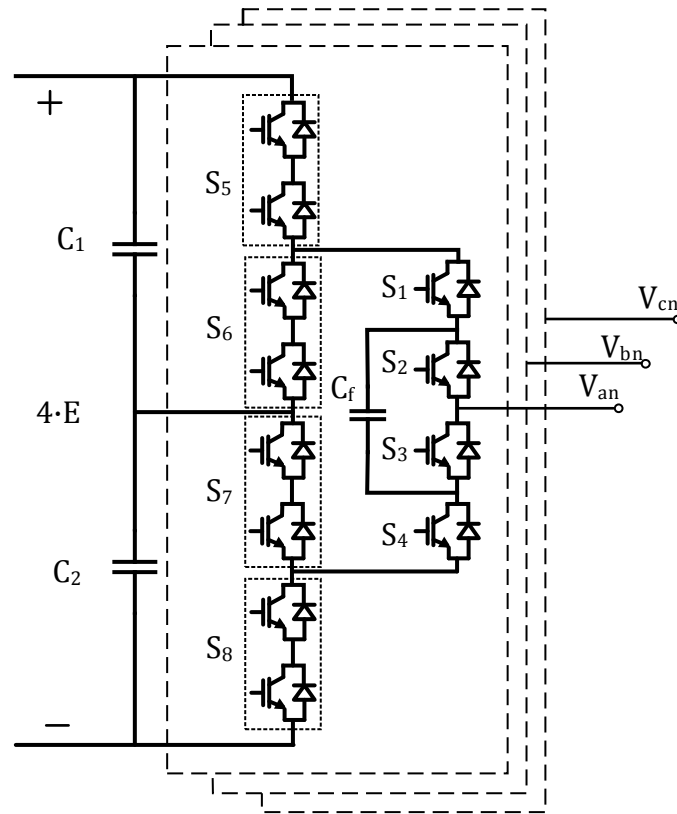Capacitor based ANPC (FCANPC) converter, which is shown in Fig. 4.2.

Fig. 4.2 Three-phase five-level FCANPC converter

As is shown, the DC-link voltage is set to 4E, thus the voltage of each of the DC-

link capacitors C_1 and C_2 would be 2E, and the voltage on the flying capacitor C_f

would be E. Also, because two outer switches connect in series, all switches can

withstand the same voltage stress which is equal to E. As for operation it is required

that the outer switches of the FC-based ANPC converter work under fundamental

frequency. Therefore, the FC circuit connects to the upper DC-link Capacitor C_1 and

the lower DC-link capacitor C_2 respectively during the first half and the second half

operation cycle, and the operation can be seen as similar to the three-level NPC

converter [18].

In a quest for lower switching frequency of the outer switches S_5 and S_8, only four out of six switching states are selected for the modulation of the five-level converter. There are eight switching states in total for each phase from the combination of these four switching states of three-level NPC converter and the two states of the two-level cell [18]. It is discussed in [18] about the complimentary switch pairs which are (S_1, S_4), (S_2, S_3), (S_5, S_6) and (S_7, S_8), and the same switching signal would go for S_5 and S_7. The switching redundancy is used to keep the flying capacitor voltage around a certain value i.e. E.

In order to achieve a good modulation strategy, different approaches have been discussed including SHE-PWM technique [30]. A variety of modulation techniques are able to work effectively with the FCANPC converter. However, the most essential concern is to keep the neutral point voltage and the flying capacitor voltage at a desirably constant level.

4.3 Dual Flying Capacitor Based Active NPC Converter

Though the five-level FCANPC converter gives a good performance and successfully found applications in the industry, there are still some drawbacks such as unequal loss distribution among switches and extra loss on the transient voltage balancing snubbers for the series connected devices during switching. To deal with such issues, a new hybrid multilevel converter, the Dual Flying Capacitor Active Neutral Point Clamped converter (DFCANPC), has been proposed in [19][20]. Circuit diagram of the five-level DFCANPC is shown in Fig. 4.3.
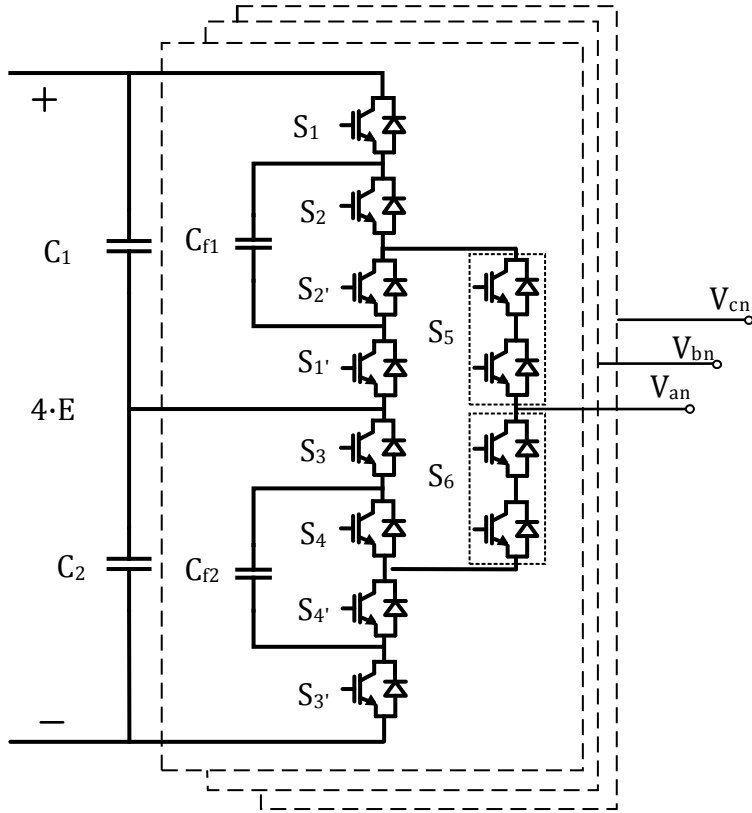
29

Fig. 4.3 Three-phase five-level DFCANPC converter

In this topology, S_1 - S_4, S_1' - S_4' operate on high frequency for PWM waveforms, and (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4') are complementary switching pairs. S_5 and S_6 are switched only with line frequency. The upper flying capacitor unit, which includes S_1, S_1', S_2, S_2' and C_{f1}, is connected to the output through the two series connected switches S_5 during the positive half-cycle. In a similar manner, the lower flying capacitor unit, S_3, S_3', S_4, S_4' and C_{f2}, is clamped to the output through S_6 during the negative half-cycle. The same as five-level FCANPC converter, the voltage stress for each device is also E.

In terms of switching states, there is also redundancy which can be used to maintain the voltage of the flying capacitors at a certain level. The switching states for DFCANPC are listed in Table 4.3.

Table 4.3 Switching states of DFCANPC converter

Level	State	S_1	S_2	S_3	S_4	S_5	S_6
+2E	+2E	1	1	1	1	1	0
+E	+EP	1	0	1	1	1	0
	+E0	0	1	1	1	1	0
0	0P	0	0	1	1	1	0
	00	0	0	1	1	1	1
	0N	0	0	1	1	0	1
-E	-E0	0	0	1	0	0	1
	-EN	0	0	0	1	0	1
-2E	-2E	0	0	0	0	0	1

One substantial feature of the DFCANPC converter is the "soft cycle commutation". To be specific, take the transition between 0P and 00 for instance. During the transition from 0P to 00, S_6 is turned on with zero voltage across it, while during the transition from 00 to 0P, S_6 can also be switched off softly. In this way, S_5 and S_6 can achieve soft commutation all the time, which means that the upper and lower FC units are capable to be connected softly to the output. In order to attain such commutation, it should be noted that the control signals for S_5 and S_6 should have a short period of overlap when the polarity change of the phase voltage happens. As a result, the switching loss on S_5 and S_6 is shifted down and the transient voltage balancing snubber is no longer needed compared with the five-level FCANPC converter, thus the efficiency is further boosted.

Similar to five-level FCANPC converter, a good modulation strategy is to well control the voltages of the neutral point and the flying capacitors, and a number of modulation techniques can be applied including carrier based and non-carrier based methods.

It is mainly demonstrated in Chapter 4 the features of FCANPC and DFCANPC converters. The three-level ANPC converter is reviewed first in terms of its advantages and operation states as an introduction to the feasible industrial five-level converters. The operation principle of FCANPC is discussed concisely. The more even loss distribution capability and soft commutation are introduced as improvements of DFCANPC over FCANPC.

CHAPTER 5

SIMULATION AND THERMAL ANALYSIS

As discussed before in Chapter 2 and Chapter 4, thermal performance of power converters directly influences the efficiency, converter complexity and cost. Consequently, the system's thermal management ability should be regarded as a significant criterion to evaluate and compare different circuit topologies.

For the FCANPC converter and the new proposed DFCANPC converter, simulation on loss distribution has been conducted using PSIM software and comparison is illustrated below, which can be used to verify the analysis.

Table 5.1 Operating points of multilevel converter
with maximum unequal loss distribution

	Power Factor	Modulation Depth (M)
Case 1	1 (motoring)	1.15 (Maximum)
Case 2	1 (motoring)	0 (very small)
Case 3	-1 (generating)	1.15 (Maximum)
Case 4	-1 (generating)	0 (very small)

It has been analyzed that the power converter thermal design is mostly determined by the four operating points that are listed in Table 5.1 [16], which is used for simulation setup. In each case, the most critical devices are the ones with the maximum loss, which would limit the phase current and output power ratings. The superior converter should have lower loss or more equal loss distribution if the total loss remains the same.

The IGBT from ABB, 5SNA-0750G650300, is selected for the main switch of both converters. The simulation conditions are set for both topologies with DC-link voltage V_{dc} = 16kV, switching frequency f = 1500Hz. Both air cooling and water cooling cases are simulated with $R_{thj\text{-}h, Q}$ =9.4°C/kW and $R_{thj\text{-}h, D}$ =16°C/kW, and thermal parameters are set for two cooling methods respectively with $R_{thh\text{-}a, air}$ = 40°C/kW and $R_{thh\text{-}a, water}$ =10°C/kW, $i_{rms, air}$ = 80A and $i_{rms, water}$ = 200A. For each converter, there are two cooling methods, two modulation indexes (M=0.1 and M=1.15) and two power factors (PF=1 and PF=-1), resulting in eight cases in total. Comparison between FCANPC and DFCANPC in each case is given below.

In order to simplify the data and clarify the outcome, the average value for both temperature and loss is used among devices that perform the same function. These six groups are (Q_1, Q_2, Q_7, Q_8), (D_1, D_2, D_7, D_8), (Q_3, Q_4, Q_5, Q_6), (D_3, D_4, D_5, D_6), (Q_9, Q_{10}, Q_{11}, Q_{12}), and (D_9, D_{10}, D_{11}, D_{12}).

5.1 Temperature Management

It is shown in Fig. 5.1 - 5.8 the temperature of devices under different conditions. Bar charts regarding temperature are put next to the groups of devices and the value is indicated by different colors.
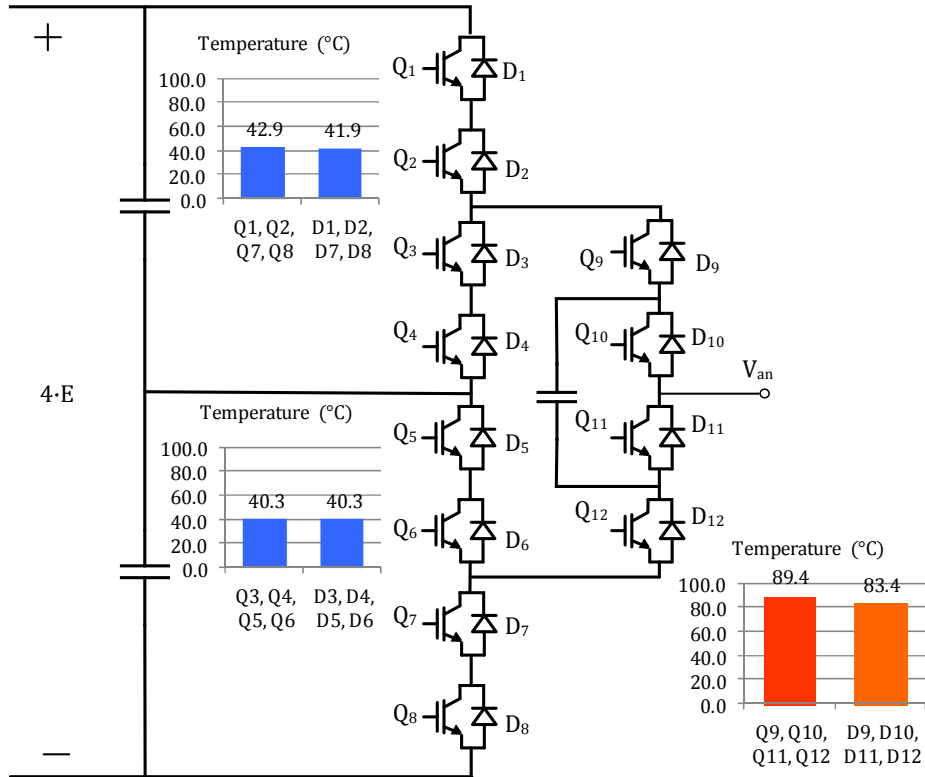
(a) FCANPC
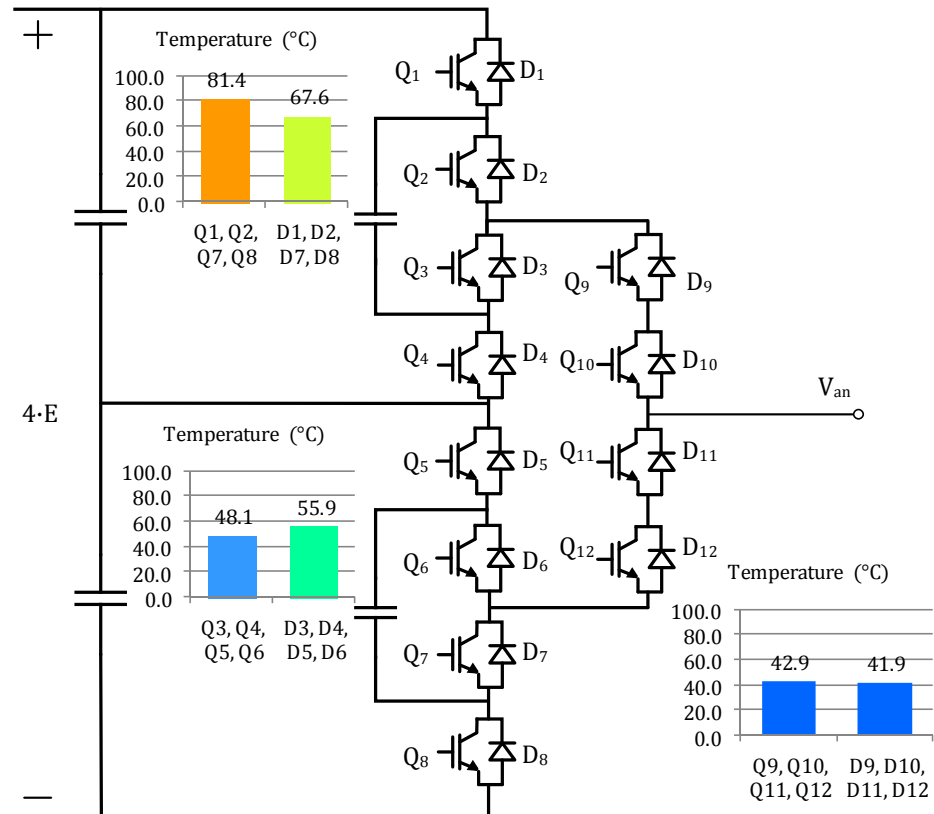
(b) DFCANPC

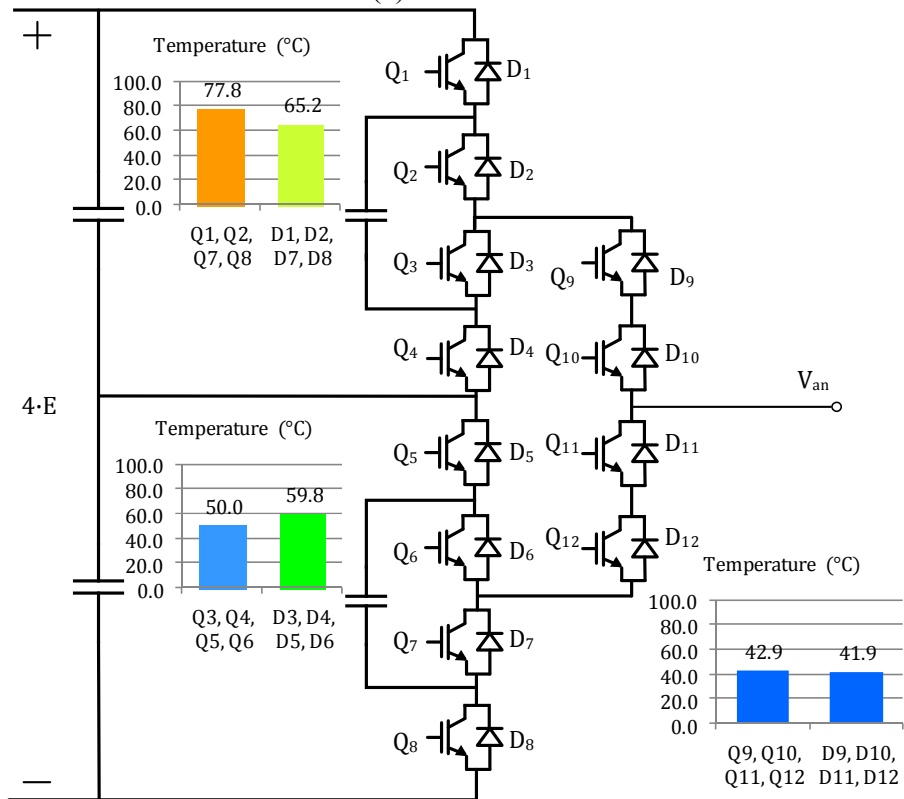Fig. 5.1 Temperature of devices with air cooling, M = 1.15, PF = 1
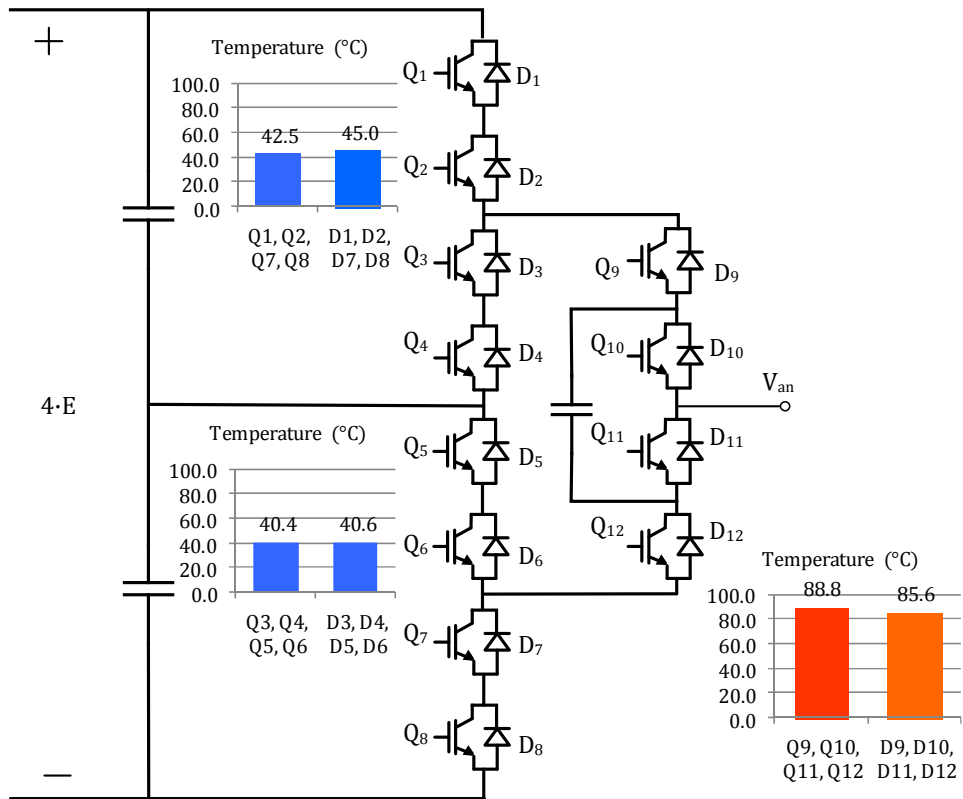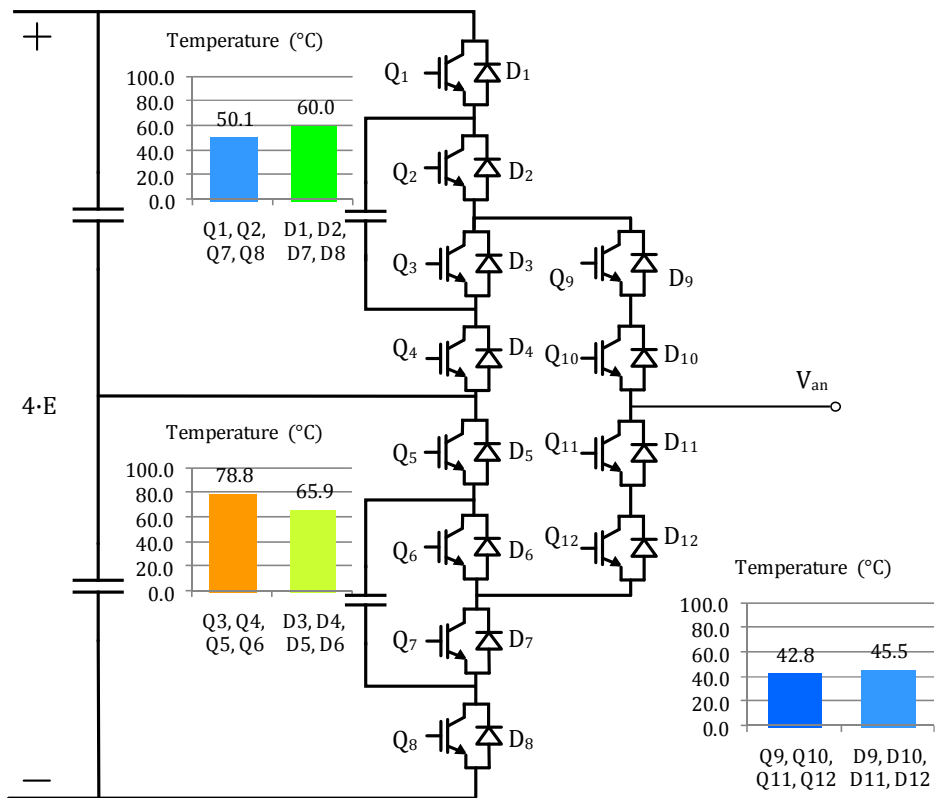
(a) FCANPC

(b) DFCANPC

Fig. 5.2 Temperature of devices under air cooling, M = 1.15, PF = -1
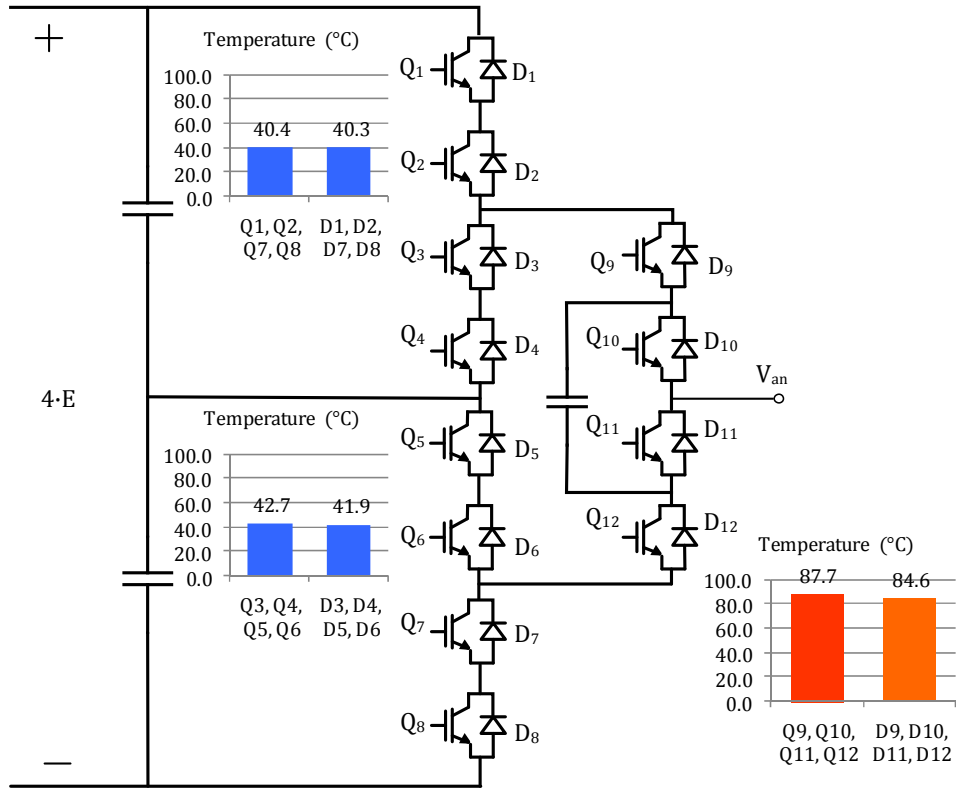
(a) FCANPC

(b) DFCANPC

Fig. 5.3 Temperature of devices under air cooling, *M* = 0.1, *PF* = 1
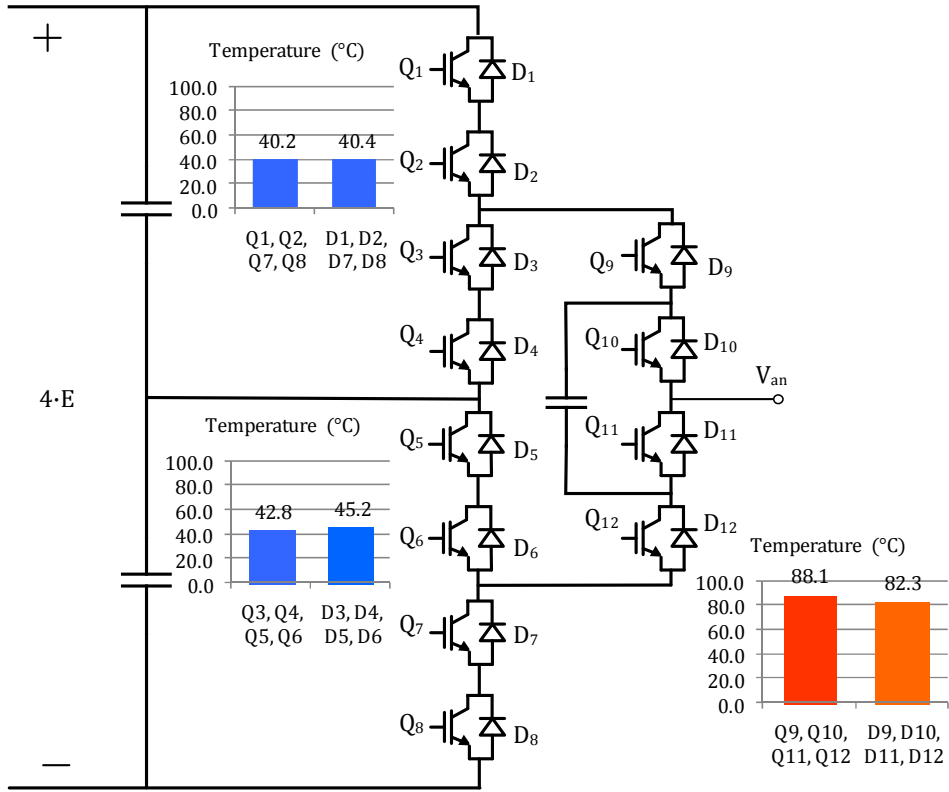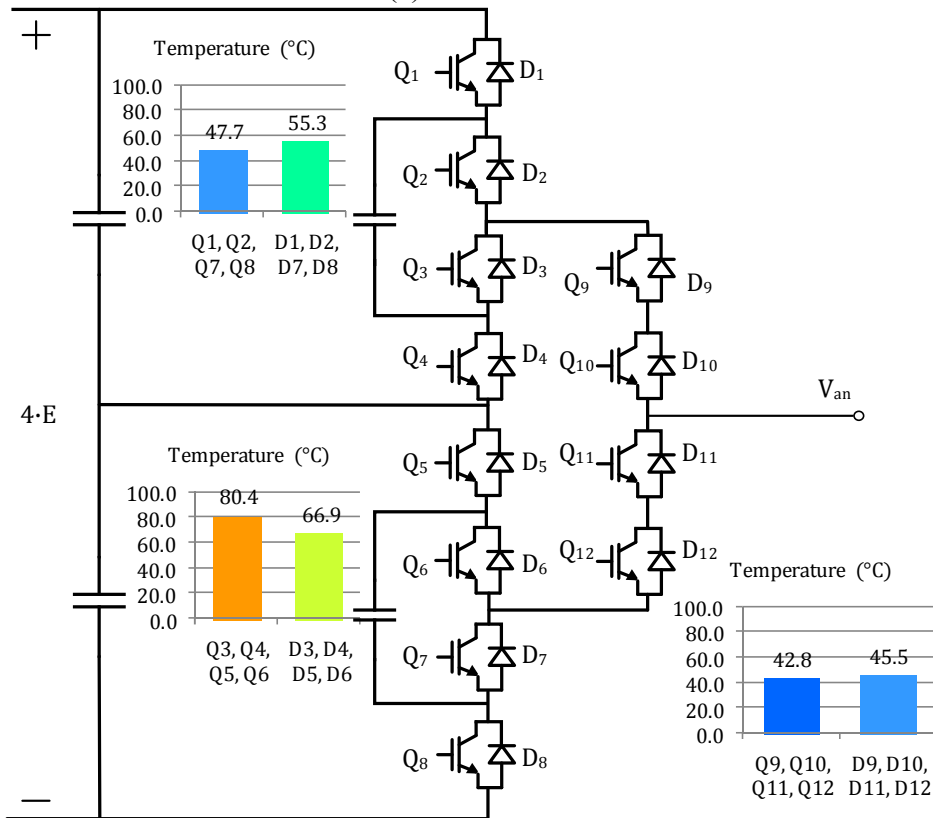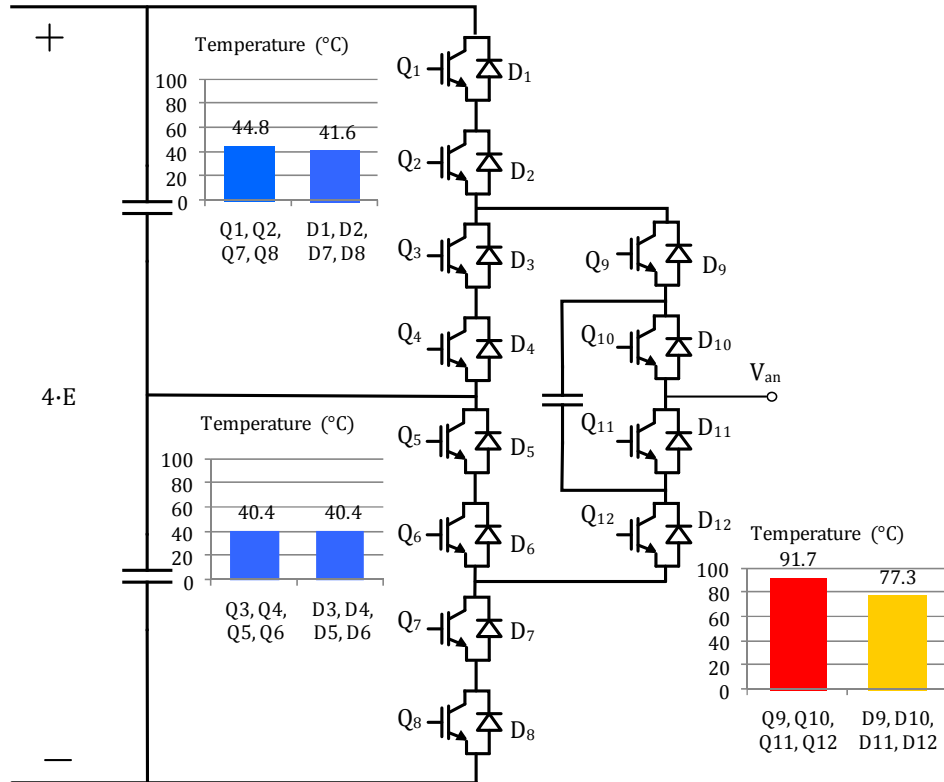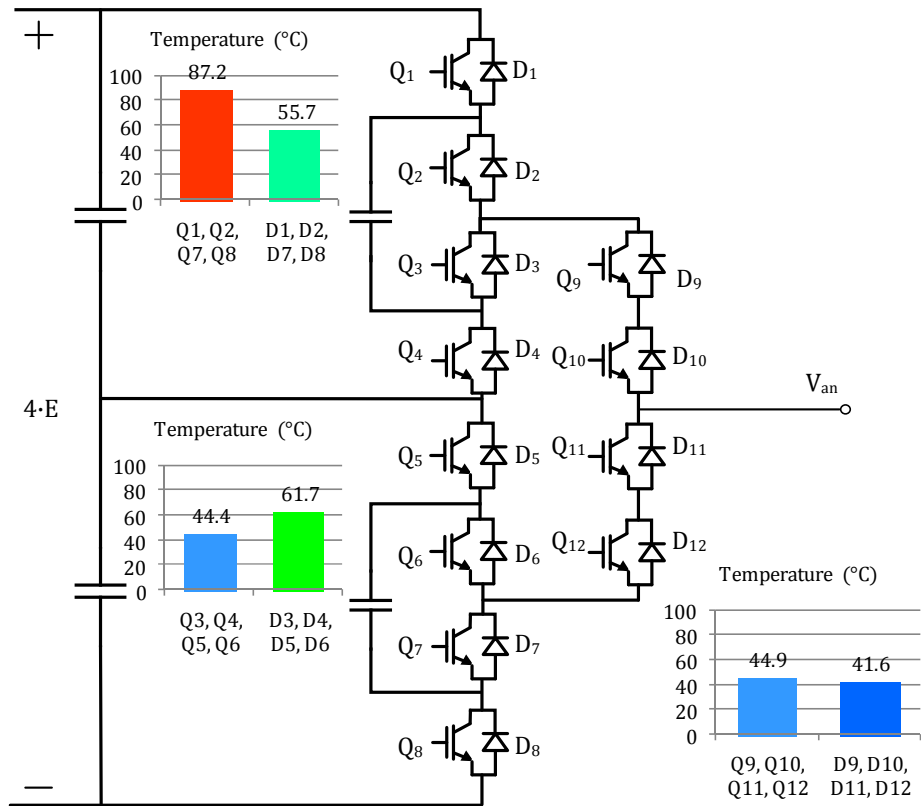
(a) FCANPC

(b) DFCANPC

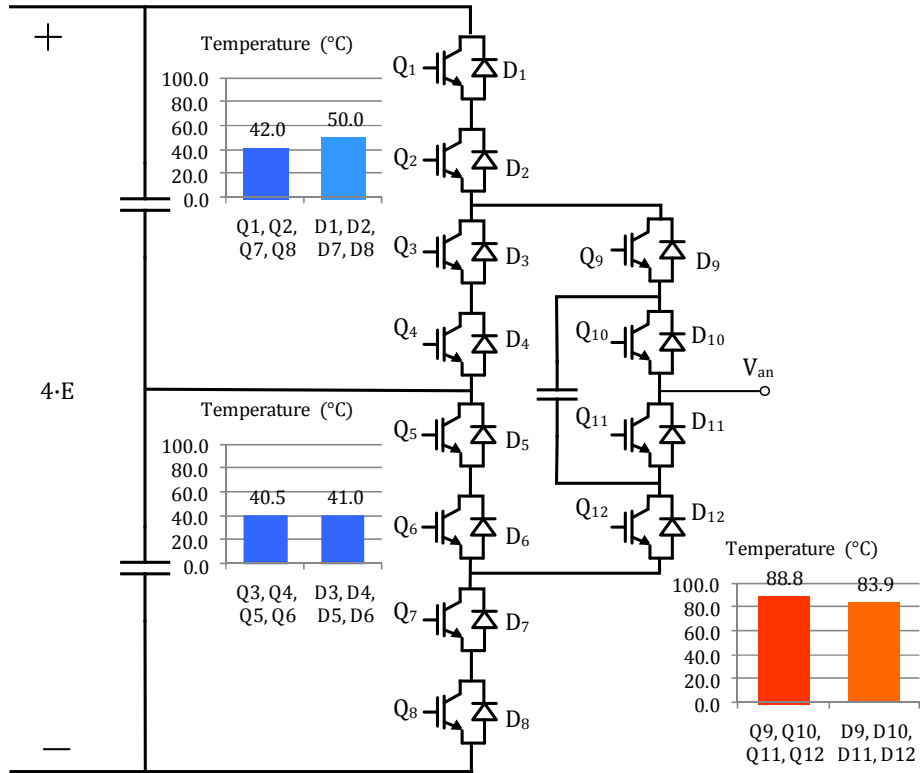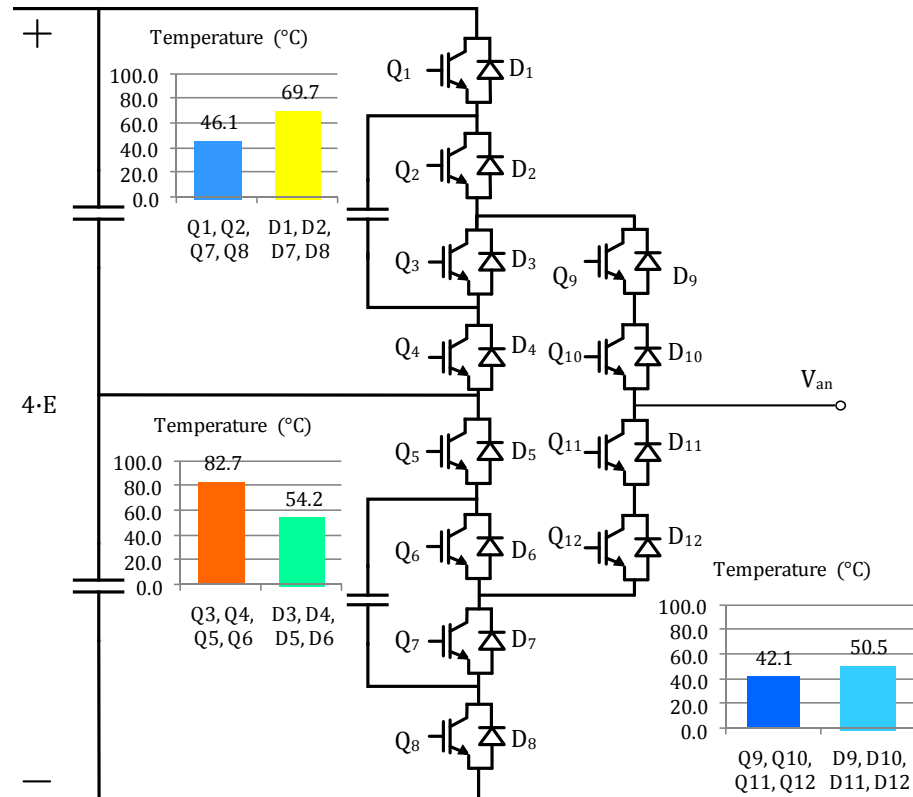Fig. 5.4 Temperature of devices under air cooling, $M = 0.1$, $PF = -1$

(a) FCANPC

(b) DFCANPC

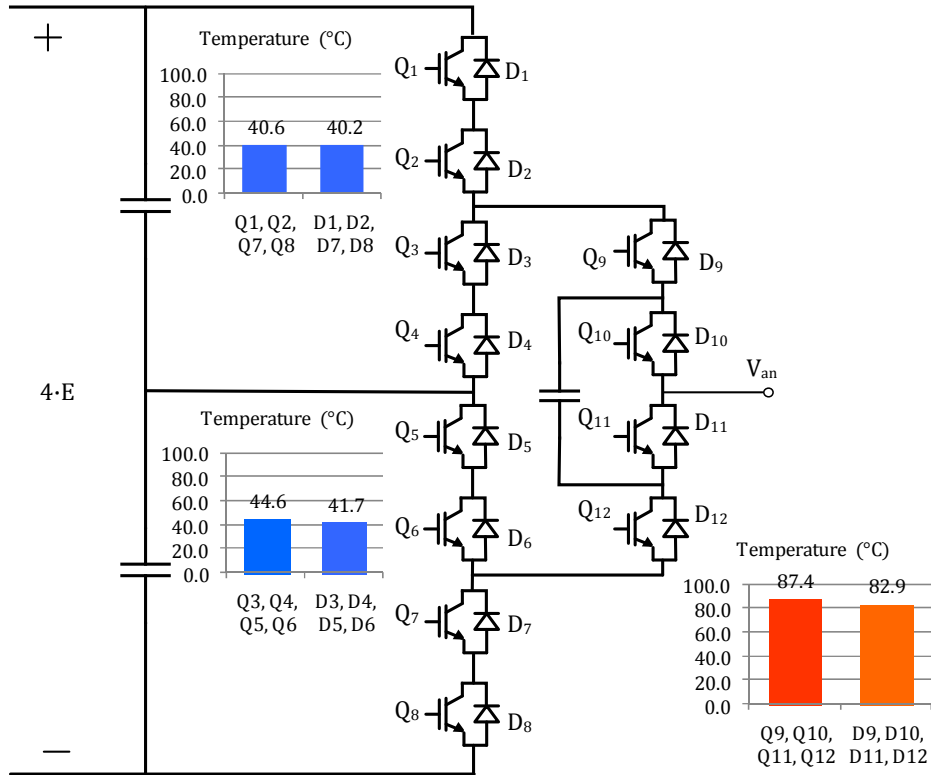Fig. 5.5 Temperature of devices under water cooling, M = 1.15, PF = 1
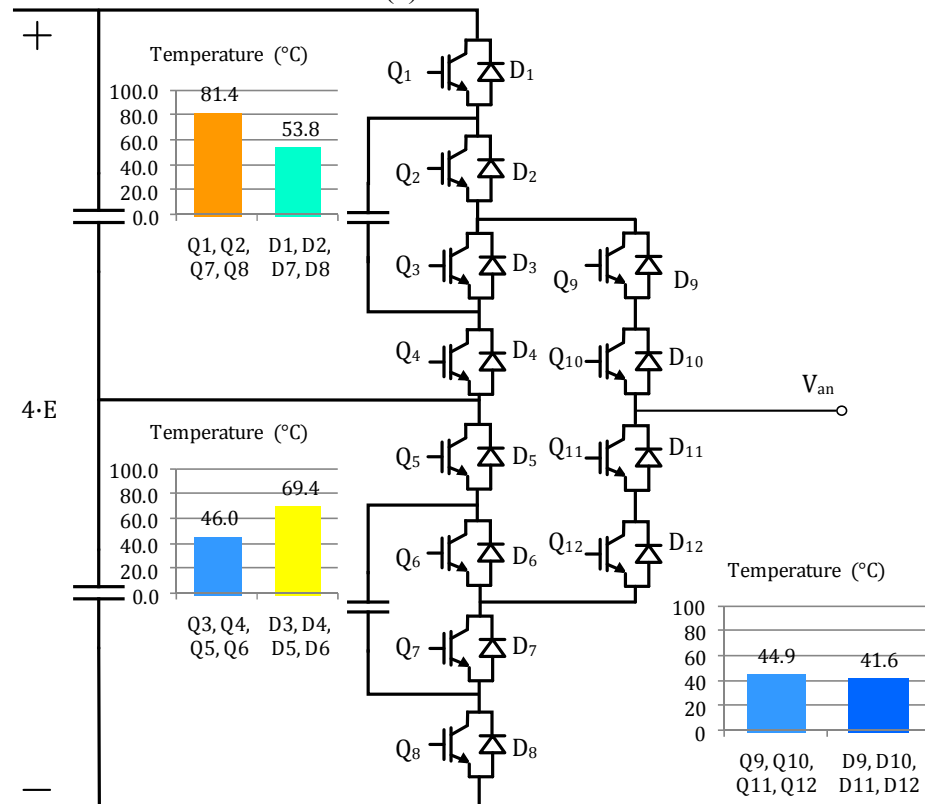
(a) FCANPC

(b) DFCANPC

Fig. 5.6 Temperature of devices under water cooling, $M = 1.15$, $PF = -1$
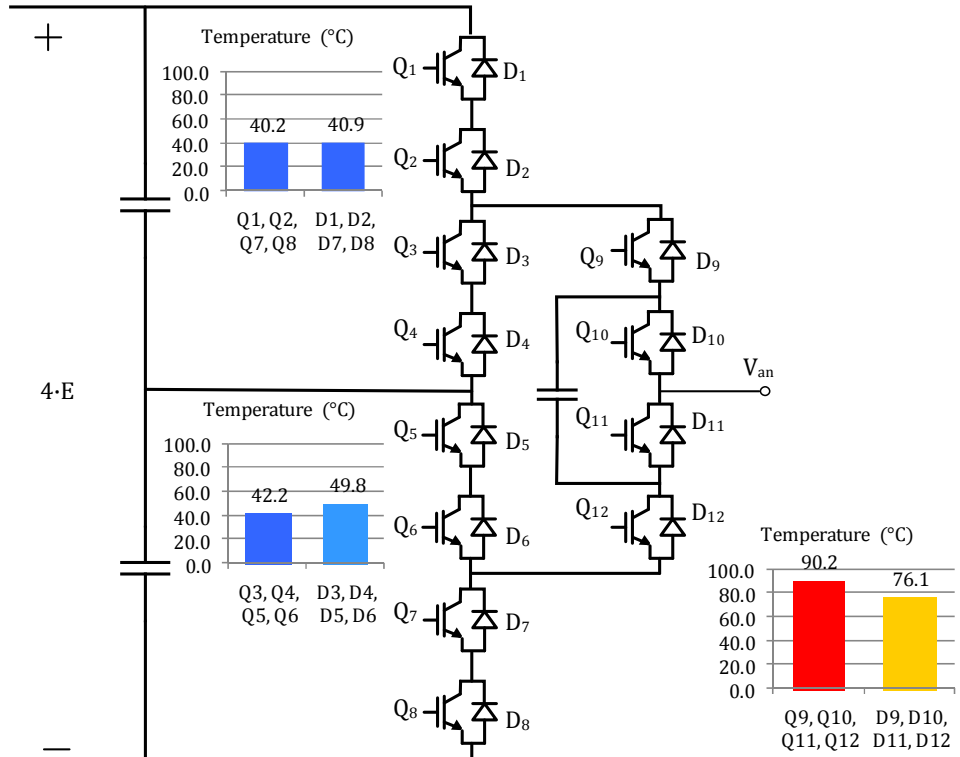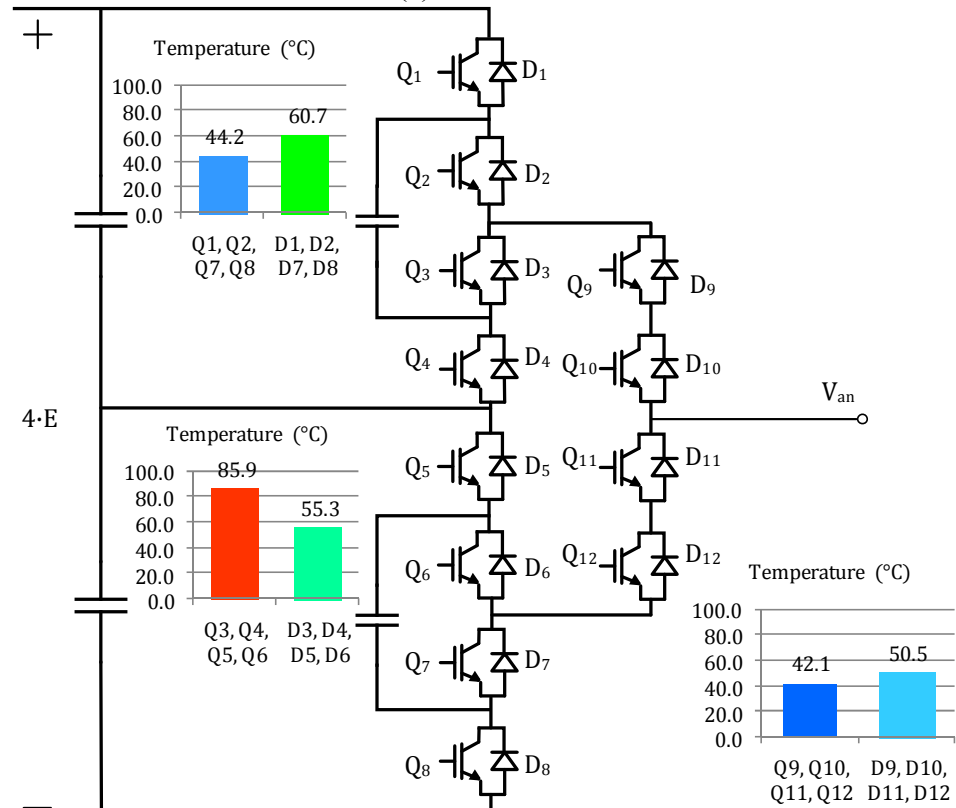
(a) FCANPC

(b) DFCANPC

Fig. 5.7 Temperature of devices under water cooling, M = 0.1, PF = 1
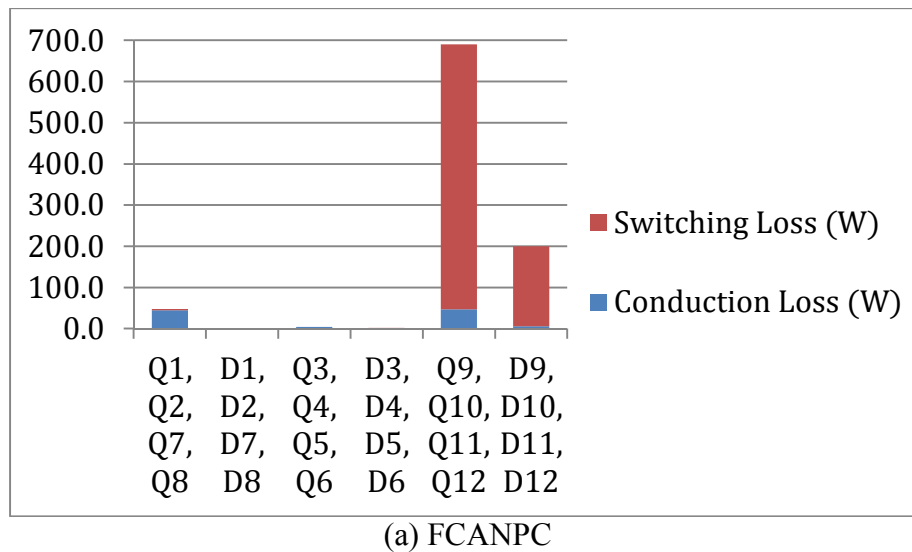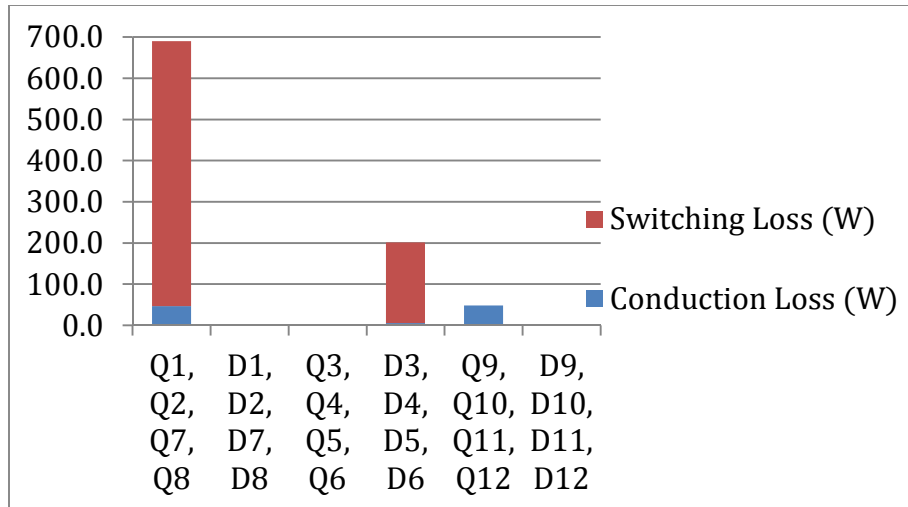
(a) FCANPC

(b) DFCANPC

Fig. 5.8 Temperature of devices under water cooling, *M* = 0.1, *PF* = -1

A few conclusions can be drawn from figures above. Firstly and basically, water cooling has a better effect than air cooling, for the devices reach similar temperatures under the same condition with the current of water cooling over twice higher than that of air cooling. Secondly, in each of the cases, regardless of the modulation index and power factor, Q_9 - Q_{12} and D_9 -D_{12} of FCANPC withstand the highest temperatures, while the other devices remain much cooler. In contrast, in DFCANPC converter, the temperature distribution of different groups of devices is more balanced and it changes with power factor, which means the converter is capable to make full use of its devices more evenly. Due to this, the highest temperature that appeared in DFCANPC is also lower than that of FCANPC converter.
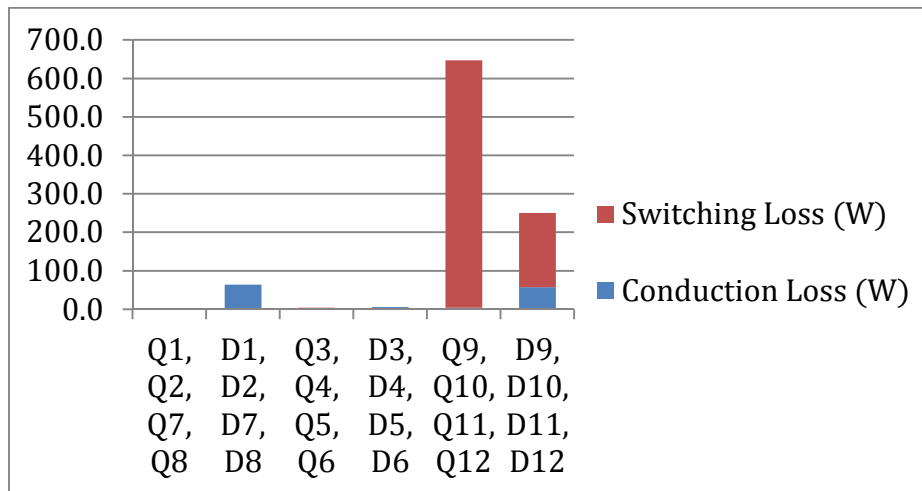
5.2 Loss Distribution Analysis

Fig 5.9 - 5.16 display the loss distribution of FCANPC converter and DFCANPC converter respectively in the eight cases.

(a) FCANPC

(b) DFCANPC

Fig. 5.9 Loss distribution under air cooling, $M = 1.15$, $PF = 1$

(a) FCANPC

(b) DFCANPC

Fig. 5.10 Loss distribution under air cooling, $M = 1.15$, $PF = -1$
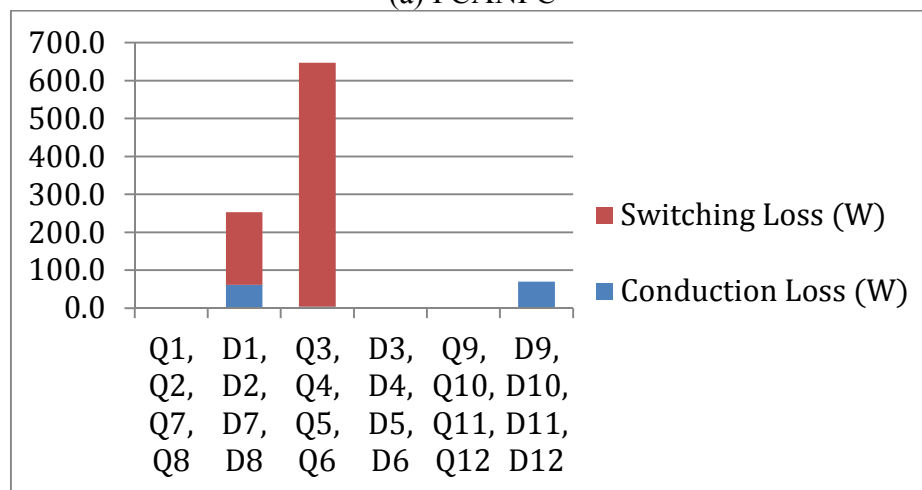
(a) FCANPC

(b) DFCANPC

Fig. 5.11 Loss distribution under air cooling, $M = 0.1$, $PF = 1$

(a) FCANPC

(b) DFCANPC

Fig. 5.12 Loss distribution under air cooling, *M* = 0.1, *PF* = -1

(a) FCANPC

(b) DFCANPC

Fig. 5.13 Loss distribution under water cooling, *M* = 1.15, *PF* = 1

(a) FCANPC

(b) DFCANPC

Fig. 5.14 Loss distribution under water cooling, M = 1.15, PF = -1
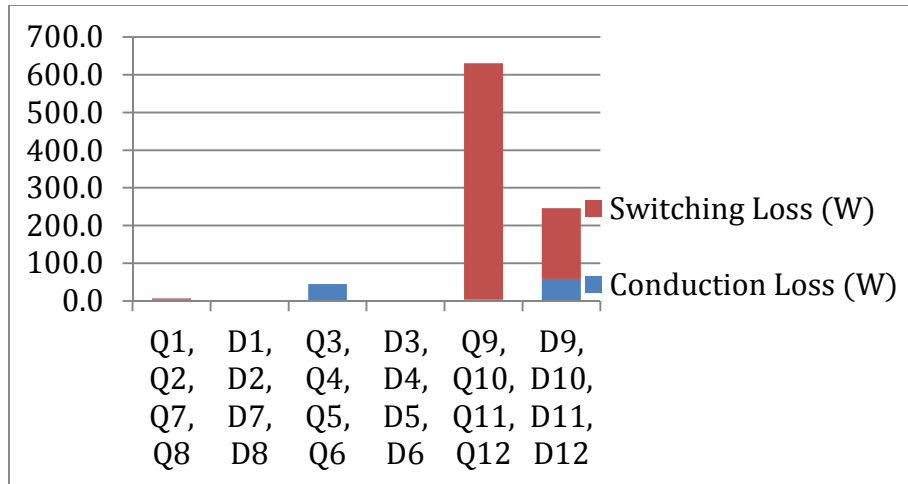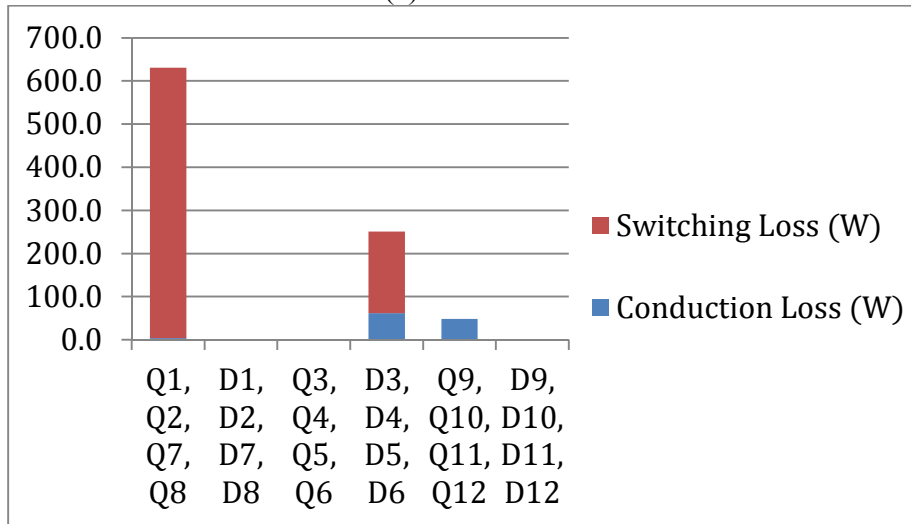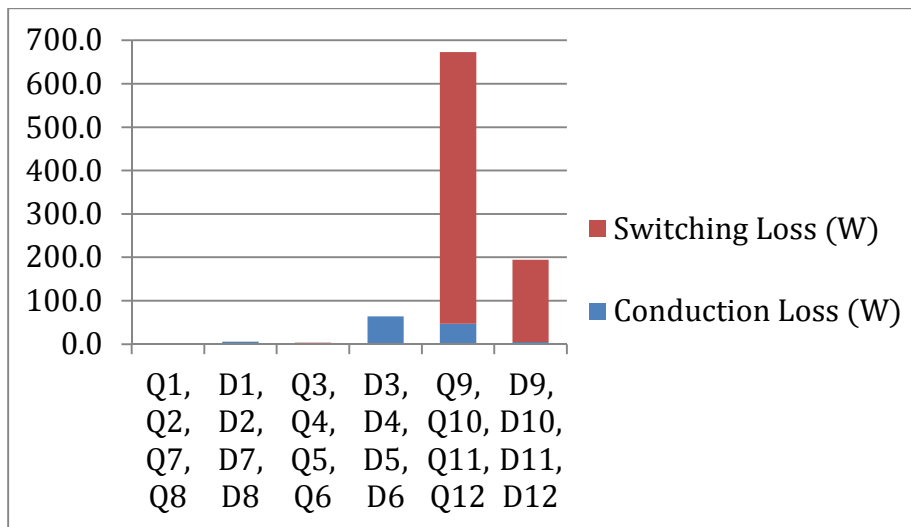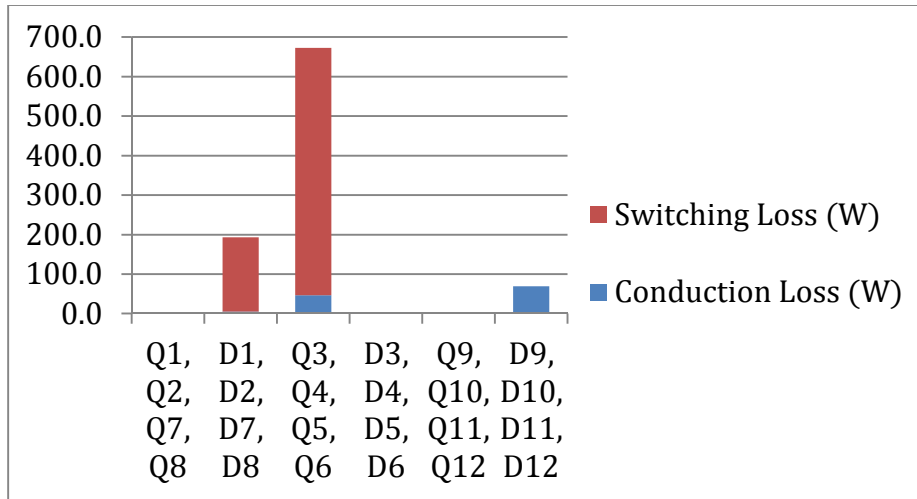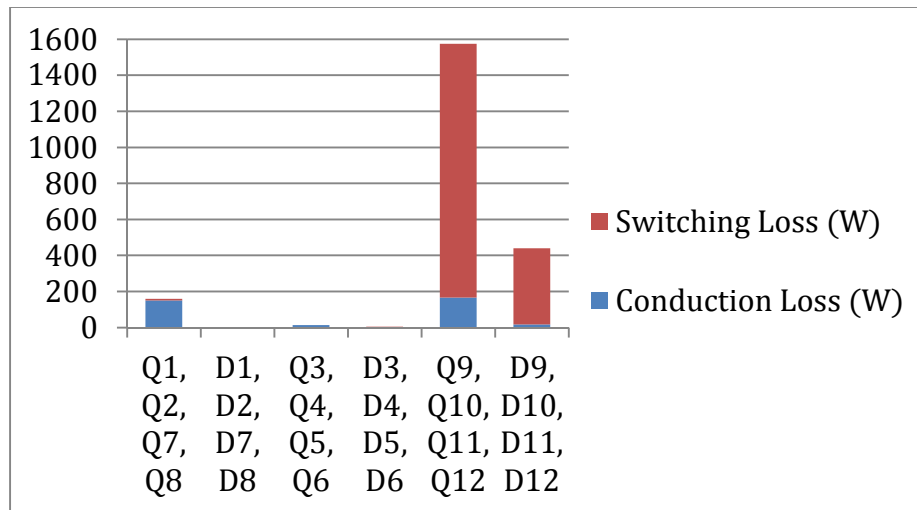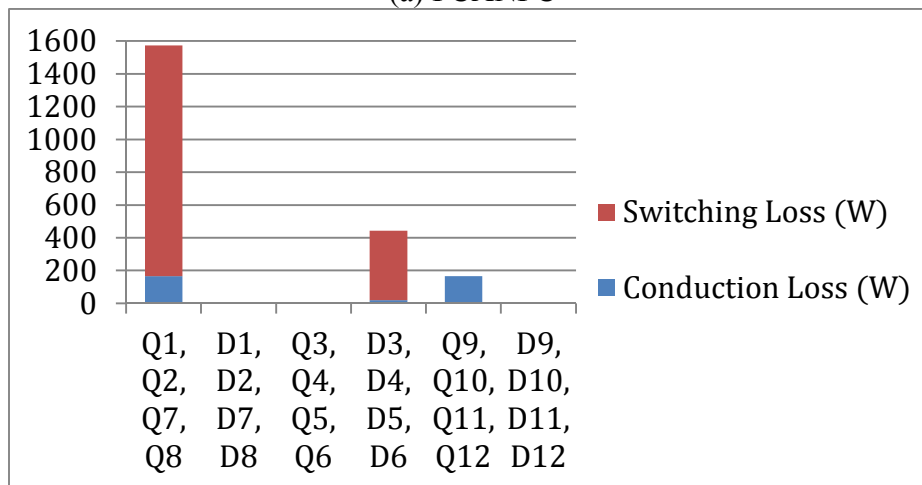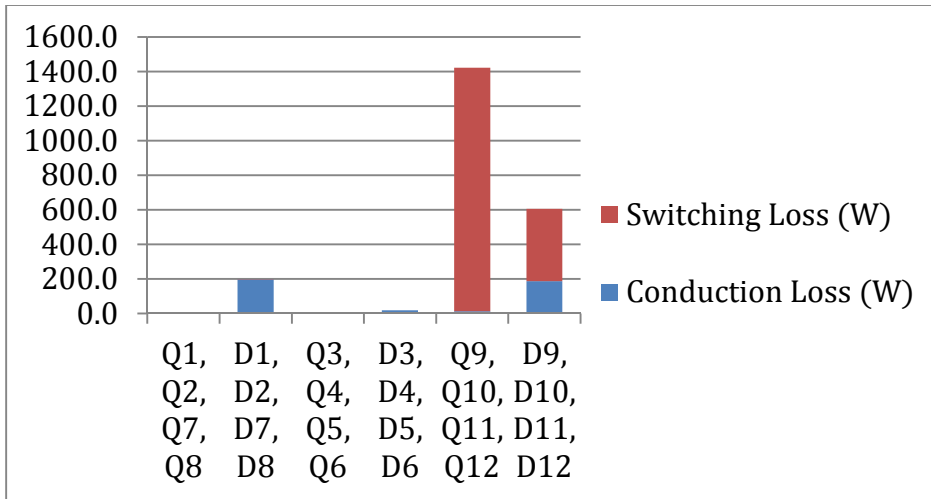

(a) FCANPC
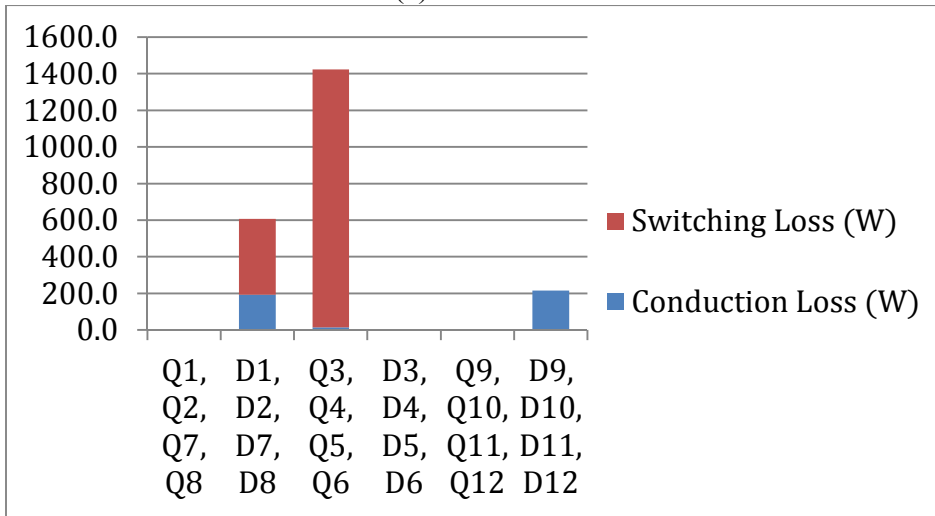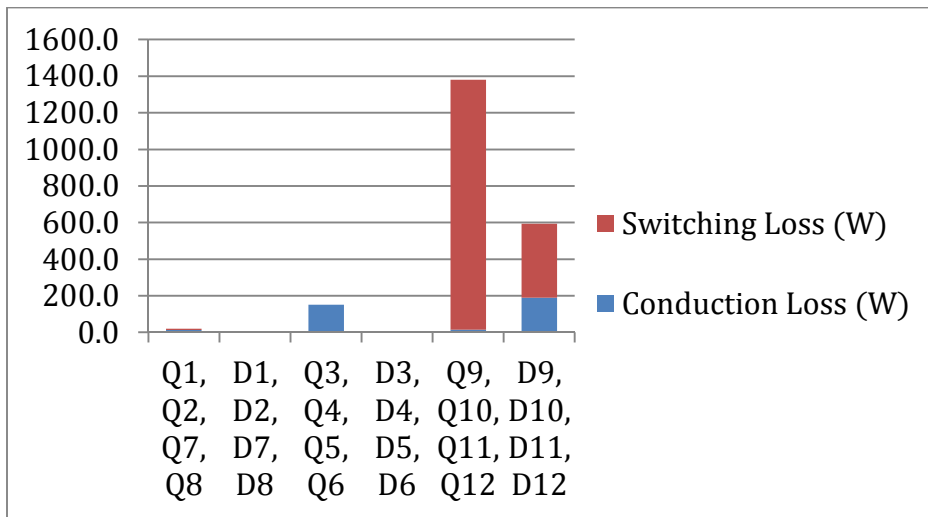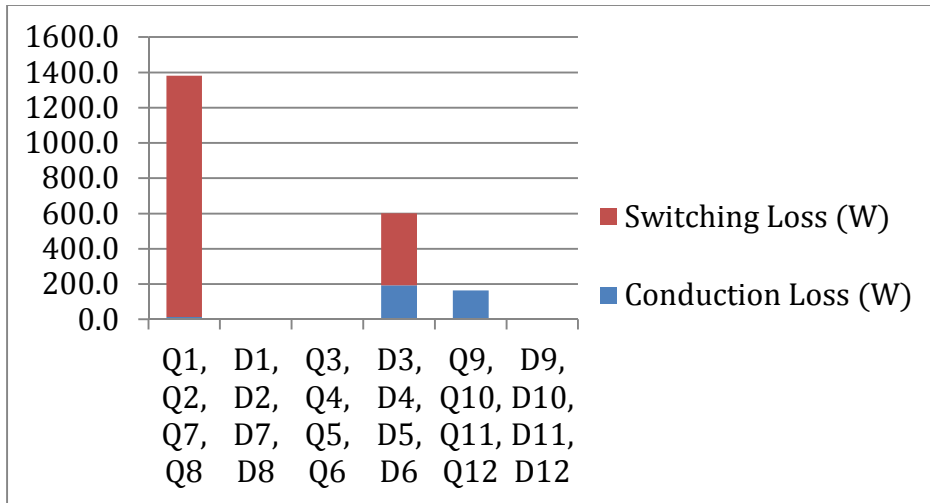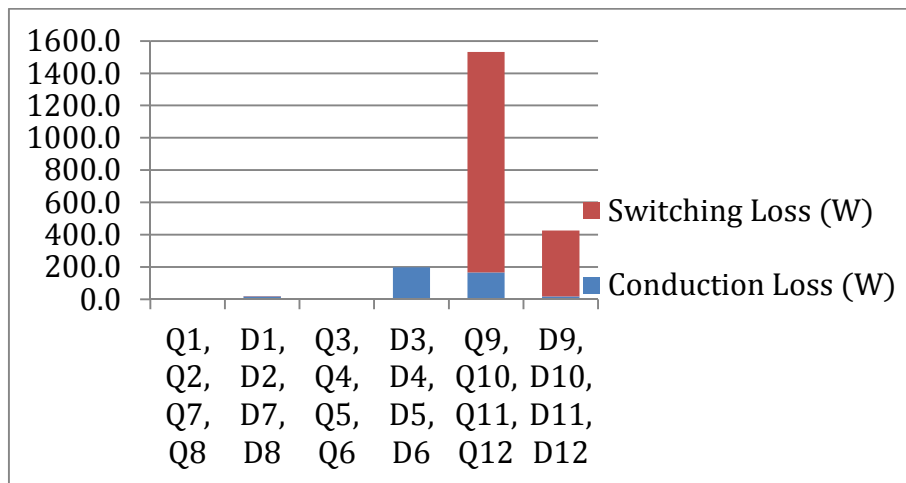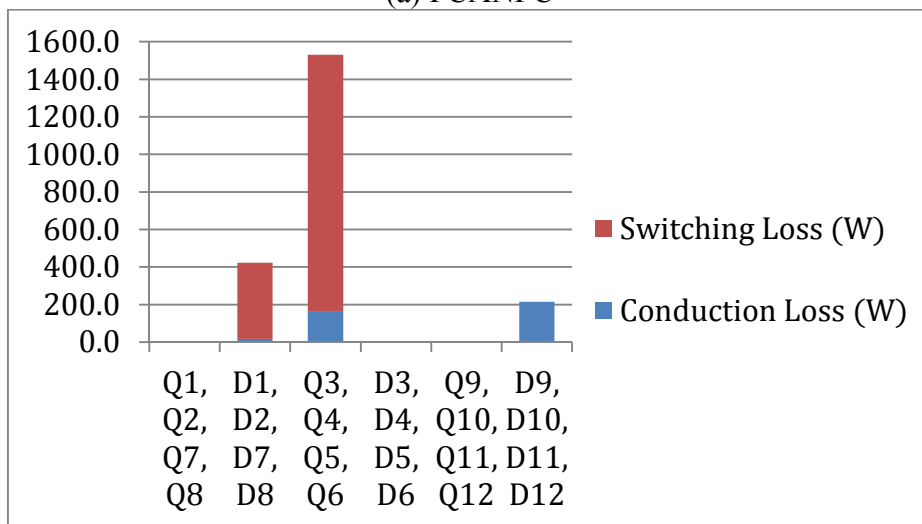
(b) DFCANPC

Fig. 5.15 Loss distribution under water cooling, $M = 0.1$, $PF = 1$

(a) FCANPC

(b) DFCANPC

Fig. 5.16 Loss distribution under water cooling, $M = 0.1$, $PF = -1$

Assuming a switch module (S_x) is composed of an IGBT (Q_x) and a diode (D_x), for FCANPC a large portion of loss is distributed among four switches (S_9, S_{10}, S_{11}, S_{12}), while for DFCANPC, this loss is distributed among eight switches (S_1, S_2, S_7, S_8) and (S_3, S_4, S_5, S_6). For example, consider the case $M = 1.15$ and $PF = 1$ in Fig. 5.9. For FCANPC the loss on each of (Q_9, Q_{10}, Q_{11}, Q_{12}) is roughly 700W while the diodes in the same modules are each dissipating 200W. Therefore, each of the switch modules in (S_9, S_{10}, S_{11}, S_{12}) is dissipating 900W. For DFCANPC case, however, the 700W is dissipated on each of (Q_1, Q, Q_7, Q_8) while the corresponding diodes have no loss. Also, the 200W is dissipated on (D_3, D_4, D_5, D_6) while there is no loss on the corresponding IGBTs in the same module. Therefore, each of (S_1, S_2, S_7, S_8) dissipates 700W and each of (S_3, S_4, S_5, S_6) dissipates 200W. This is evidently a more uniform distribution of loss among switch modules. Similar loss distribution trends can be observed for the other cases at different modulation index and power factors.

It is clearly illustrated that switching loss takes the majority part in the total loss, which becomes the reason why modulation schemes and topology configuration count. Similar to what is indicated from temperature, the two groups of switches in FCANPC, (Q_9, Q_{10}, Q_{11}, Q_{12}) and (D_9, D_{10}, D_{11}, D_{12}), withstand the highest loss in each situation, while Q_1 - Q_8 and D_1 - D_8 in DFCANPC have more balanced loss distribution with the different depth of use according to power factor. The soft commutation in DFCANPC is also proved by Q_9 - Q_{12} and D_9 - D_{12} with the total loss caused only by conduction. As a consequence, the transient voltage balancing snubber is no longer needed for DFCANPC.

The total loss of FCANPC and DFCANPC converter in the eight simulated cases is listed in Table 5.2. As demonstrated, the conduction loss and switching loss regarding semiconductor devices for both topologies remain almost the same, which is in accordance to the target of distributing loss more evenly rather than decreasing the loss. However, in FCANPC converter, the loss of eight snubbers with 45W each adds to the total loss, leaving it a disadvantage compared to the newly proposed DFCANPC topology.

Table 5.2 Total loss distribution of FCANPC and DFCANPC

	Conduction loss (W)	Switching loss(W)	Snubber loss(W)	Total loss(W)	Cooling	M	PF
FCANPC	402.4	3373.2	360.0	4135.6	Air (i_{rms}=80A)	1.15	1
DFCANPC	402.8	3356.4	--	3759.2			
FCANPC	525.2	3355.2	360.0	4240.4	Air (i_{rms}=80A)	1.15	-1
DFCANPC	539.6	3336.0	--	3875.6			
FCANPC	441.6	3276.8	360.0	4078.4	Air (i_{rms}=80A)	0.1	1
DFCANPC	456.8	3260.8	--	3717.6			
FCANPC	486.0	3274.0	360.0	4120.0	Air (i_{rms}=80A)	0.1	-1
DFCANPC	486.0	3256.8	--	3742.8			
FCANPC	1396.0	7374.0	360.0	9130.0	Water (i_{rms}=200A)	1.15	1
DFCANPC	1392.8	7329.6	--	8722.4			
FCANPC	1674.4	7340.8	360.0	9375.2	Water (i_{rms}=200A)	1.15	-1
DFCANPC	1685.2	7294.0	--	8979.2			
FCANPC	1474.4	7133.6	360.0	8968.0	Water (i_{rms}=200A)	0.1	1
DFCANPC	1488.0	7093.6	--	8581.6			
FCANPC	1594.0	7132.4	360.0	9086.4	Water (i_{rms}=200A)	0.1	-1
DFCANPC	1588.0	7089.2	--	8677.2			

In chapter 5, simulation results in PSIM are provided for comparison on thermal management of five-level FCANPC converter and DFCANPC converter. A few cases are built, including air cooling and water cooling, the maximum modulation index and a very small modulation index, and power factor to be 1 and -1. It is clearly illustrated from the results that DFCANPC converter has better capability in

equal loss balancing. Its soft commutation and the "snubberless" feature have also been verified.

CHAPTER 6

SUMMARY AND CONCLUSION

In this thesis, thermal and loss balancing analysis is investigated for five-level FCANPC VSC and the newly proposed DFCANPC VSC. Classic multilevel converter topologies and modulation schemes are discussed first as an introduction to hybrid topologies. Thermal models are provided for loss balancing analysis. The advantageous features of DFCANPC topology over FCANPC topology are demonstrated such as even loss distribution and "soft commutation". A model in PSIM platform has been established for both air and water cooling strategies, different power factors, and high and low modulation indexes. It is verified that the DFCANPC VSC has more balanced loss distribution to boost the output current capability, and its "soft commutation" feature makes it possible to further improve the converter efficiency by avoiding the transient voltage balancing snubber for series connected switches.

As modern power electronics has brought revolutionary changes in high power processing, higher-level multilevel converter topologies make MV power conversion possible. The five-level FCANPC has received popularity in the industry and relative products have sprouted, for example the ABB ACS 2000 drive. Its applications cover mills, fans, pumps and conveyors in cement and metal industry, oil and gas companies and renewable energy generation. With better thermal management over FCANPC, DFCANPC is expected to be another hit in medium voltage power world.

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