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Authors

Blackwell, Margaret E
Stillwell, Andrew
Pilawa-Podgurski, Robert CN

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M. E. Blackwell
A. Stillwell
R. C. N. Pilawa-Podgurski

Dynamic Level Selection for Full Range ZVS in Flying Capacitor Multi-Level Converters

Margaret E. Blackwell†, Andrew Stillwell‡, Robert C.N. Pilawa-Podgurski†
†University of California, Berkeley, Berkeley, CA, USA
‡University of Illinois at Urbana-Champaign, Urbana, IL, USA

***Abstract*— This paper presents a control technique for flying capacitor multi-level (FCML) converters to achieve zero-voltage switching (ZVS) across the full range of duty cycles, with application in high power density and high efficiency power converters. Previous works have used variable frequency control to enable ZVS at specific duty cycles in FCML converters, but have not been able to use these methods to allow ZVS across the full range. This work uses dynamic level selection and variable frequency control to increase inductor current ripple at duty cycle ranges for which ZVS was previously unattainable. An experimental 5-level FCML prototype has been built using GaN devices on a single-sided PCB to demonstrate this control technique. We demonstrate 4-level and 5-level operation with ZVS at duty cycles that are not possible with 5-level operation alone, as well as a dynamic level transition with active capacitor voltage balancing.**

I. Introduction

Flying capacitor multi-level (FCML) converters utilize one or more flying capacitors as energy storage elements to reduce the switch voltage stress of each transistor and to reduce the volt-second on the inductor [1]–[6]. These benefits allow the use of lower voltage rated switches, which permits higher switching frequencies as a result of lower switching losses. The increase in switching frequency, in conjunction with the reduction in inductor volt-second, due to inherent qualities of the FCML topology, leads to a reduction in the volume of the inductor and the total volume of the converter. However, with this decrease in volume comes a necessity to increase efficiency because the surface area for heat transfer is reduced. Further reduction in volume can be achieved through higher frequency switching at the cost of higher switching losses. To mitigate these switching losses, zero-voltage switching (ZVS) can be employed at selected duty cycles as shown in [7], [8] through variable frequency control. However, both works noted the challenges of obtaining ZVS at specific duty cycles inherent to FCML operation. For DC/AC or AC/DC converter applications, or for applications with wide input voltage ranges, the duty cycle of the switches must vary across a wide range. However, due to the nature of FCML operation detailed in this paper, maintaining ZVS across the full range is a challenge. In [9], the current ripple is *minimized* by dynamically varying the number of levels of the FCML, which is suitable for hard-switched operation. Here, we propose to dynamically vary the number of levels to *increase* the inductor current ripple and, in conjunction with variable frequency control, maintain the necessary conditions for ZVS across the full duty cycle range.

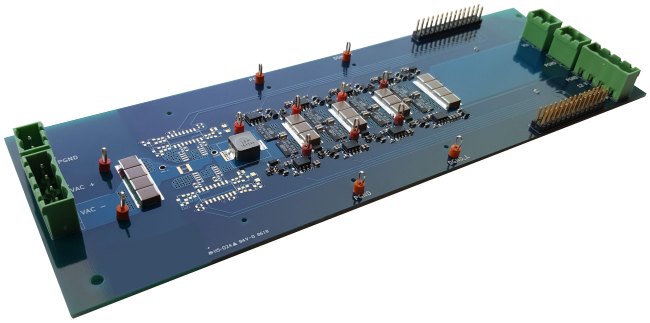

Fig. 1: Hardware Prototype.

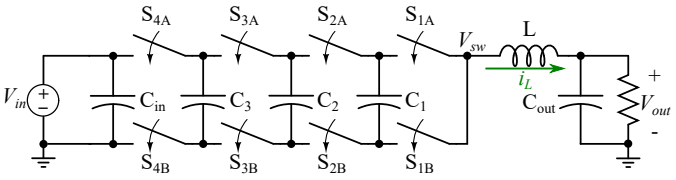

Fig. 2: 5-Level FCML Converter Schematic.

We derive the underlying mechanisms in FCML converters which make ZVS a challenge at specific duty cycle ranges, and show how dynamic level selection overcomes this challenge. Additionally, we detail the considerations of capacitor voltages necessary to decide the number of converter levels and switch implementation. Our control strategy is validated in hardware through a 5-level experimental prototype, which demonstrates ZVS at duty cycles previously unattainable. Level transitioning is demonstrated with active balancing through the use of duty cycle adjustment. This paper presents a method of ensuring ZVS operation across a full range of conversion ratios for an FCML converter and demonstrates this method in a compact and flat hardware prototype, shown in Figure 1.

II. Flying Capacitor Multi-level Converter

Figure 2 shows a schematic drawing of the 5-level FCML converter used in this work with flying capacitors labeled C_1, C_2, and C_3. Phase-shifted PWM (PS-PWM) [1], [10] is typically used for FCML converters of N levels with

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each switch pair (labeled S_{iA} and S_{iB}) operated complementary to each other at duty cycle, D, and phase shifted by $360°/(N-1)$. The voltage conversion ratio of the buck FCML is equivalent to that of the traditional two-level buck converter, given by Equation 1. One advantage of the FCML converter with PS-PWM control is the reduced switch voltage stress, $V_{in}/(N-1)$, because the flying capacitors, C_k, are held at a steady-state voltage, Equation 2.

$$V_{out} = D \cdot V_{in} \tag{1}$$

$$V_{C_k} = \frac{k \cdot V_{in}}{(N-1)}, k = 1, 2...(N-2) \tag{2}$$

Additionally, the FCML topology has an inherent frequency multiplication at the switch node, V_{sw} in Figure 2, that allows for a reduction in inductance. For a given switching frequency, f_{sw}, the effective switching frequency, f_{eff}, seen at the inductor is $(N-1) \cdot f_{sw}$ and the voltage across the inductor swings by $V_{in}/(N-1)$. Both the frequency multiplication and voltage reduction lead to a required inductance decrease by $(N-1)^2$.

III. Zero-Voltage Switching

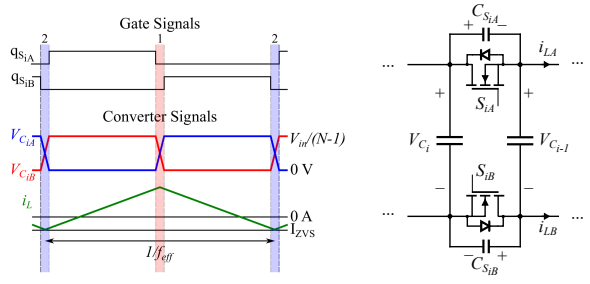
In addition to the frequency multiplication property and inductance reduction inherent to the FCML topology, the switching frequency should be increased to further increase power density. However, the switching losses also increase with frequency. One method to reduce these switching losses is to operate such that the inductor current goes negative and allows ZVS [11]. Only the basics of ZVS for FCMLs are described here and a more detailed explanation is available in [7]. In buck-mode operation, because the inductor current is naturally positive during the deadtime of Region 1 in Figure 3a, ZVS is easily attainable for the low-side switches. The small parasitic capacitance of the low-side transistor, $C_{S_{iB}}$ in Figure 3b, can discharge quickly from $V_{C_{SiB}} = V_{in}/(N-1)$ to 0 V with this positive current, i_L, thus enabling a zero-voltage at the time of switching. Conversely, ZVS for the high-side switches is more difficult because a negative current during the deadtime of Region 2 is required to discharge the parasitic capacitance, $C_{S_{iA}}$ to 0 V before switching.

Previous works, [11] and [12], have shown that a sufficiently large inductor current ripple is required to provide a negative current, i_L, during a specified deadtime which discharges the transistor parasitic capacitance and allows ZVS operation. However, due to the multi-level operation of the FCML, certain duty cycles inherently exhibit low or no current ripple, inhibiting the ability to achieve ZVS without going to extremely low switching frequencies. In this work, a constant negative inductor current peak, I_{ZVS}, is chosen along with a constant deadtime.

Inherent to the FCML operation are both the converter duty cycle, D, and an effective duty cycle, D_{eff}, (given by Equation 3) at the switching node, V_{sw}, which affects the inductor current ripple, Δi_{pp}, (given by Equation 4). It is apparent that D_{eff} is zero for certain values of D and therefore, the inductor current ripple approaches zero as well. Figure 4 shows the inductor current ripple at a fixed switching frequency, f_{sw}, for a 4- and 5-level FCML normalized to the conventional two-level buck converter, with current ripple valleys at duty cycles of 0.33 and 0.66 for the 4-level FCML, and 0.25, 0.5, and 0.75 for the 5-level FCML. Previous works [7], [8] have shown that by varying the switching frequency along the duty cycle range, the inductor current ripple can be changed to keep ZVS operation. However, the switching frequency can only be decreased to limits imposed by the flying capacitor ripple, inductor saturation, or practical limitations [8]. Moreover, the valleys of the inductor current ripple plot in Figure 4, cannot be avoided by decreasing the switching frequency and consequently, ZVS cannot be maintained at these operating points.

$$D_{eff} = D \cdot (N-1) - floor(D \cdot (N-1)) \tag{3}$$

$$\Delta i_{pp} = \frac{V_{in} \cdot (D_{eff} \cdot (1 - D_{eff}))}{L \cdot f_{sw} \cdot (N-1)^2} \tag{4}$$



(a) Converter waveforms for ZVS conditions.

(b) Arbitrary switch pair with parasitic capacitances.

Fig. 3: Inductor current must have enough ripple to reach a peak negative value, I_{ZVS} which can discharge the parasitic capacitance $C_{S_{iA}}$ of an arbitrary switch pair and allow for ZVS.

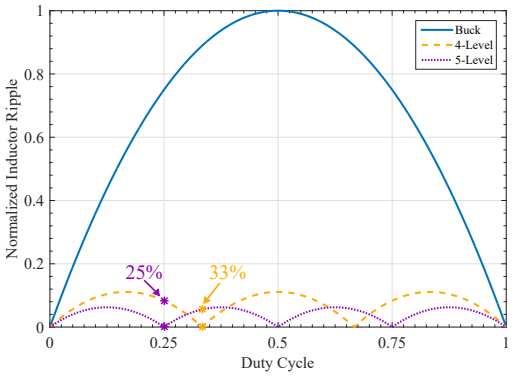


Fig. 4: Higher-level FCML converters inherently exhibit lower inductor current than two-level buck converters, but introduce inductor ripple valleys at certain duty cycles.

TABLE I: 4/5 Level Switch Pair Configurations and Flying Capacitor Impact

Level	Pair	S_4	S_3	S_2	S_1	V_{C3}	V_{C2}	V_{C1}	ΔV_C		
									C_3	C_2	C_1
5		$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{3}{4}V_{in}$	$\frac{1}{2}V_{in}$	$\frac{1}{4}V_{in}$	0	0	0
4a	S_4, S_3	$\frac{1}{4}V_{in}$	$\frac{1}{12}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{3}{4}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	0	$+\frac{1}{6}V_{in}$	$+\frac{1}{12}V_{in}$
4b	S_3, S_2	$\frac{1}{3}V_{in}$	$\frac{1}{6}V_{in}$	$\frac{1}{6}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{2}V_{in}$	$\frac{1}{3}V_{in}$	$-\frac{1}{12}V_{in}$	0	$+\frac{1}{12}V_{in}$
4c	S_2, S_1	$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{12}V_{in}$	$\frac{1}{4}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{4}V_{in}$	$-\frac{1}{12}V_{in}$	$-\frac{1}{6}V_{in}$	0

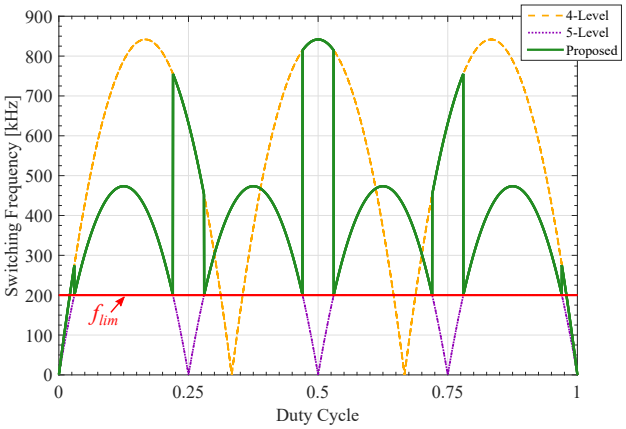


Fig. 5: The proposed method implements dynamic level changing to avoid operation at the inductor current ripple valleys and to maintain ZVS across the entire duty cycle range.

A. Dynamic Level Selection

Here, we propose to use dynamic level selection to maintain a minimally sufficient inductor current ripple required for ZVS operation. Figure 5 illustrates the proposed method for selecting the number of levels to operate across all duty cycles. Over the full range of duty cycles, we plot the switching frequency required to achieve ZVS for 4- and 5-level operation and a minimum switching frequency, f_{lim}, for which the converter is not designed to operate below. This plot is for a constant peak negative inductor current which can be controlled to maintain ZVS [13]. At each duty cycle, we prioritize 5-level operation because the switch voltage stress and therefore, the switching losses, is reduced in the case of a higher number of levels. Moreover, as shown in [14], lower device operating voltage also reduces dynamic $R_{ds,on}$ effects in GaN transistors, another important design consideration. The voltage swing of the inductor is also reduced for the case of a higher number of levels, consequently reducing inductor core losses. If the 5-level switching frequency must be below f_{lim} to maintain ZVS, the converter transitions to 4-level operation at a new switching frequency to maintain ZVS.

B. Level Evaluation

An analysis of the steady-state capacitor voltages for different number of FCML levels is used as reasoning for choosing a 5/4 level converter as well as for selecting which switch pair to operate in phase when in the 4-level mode [9]. The steady-state capacitor voltages for 5-level operation, as well as for 4-level operation with different switches operated as a pair are shown in Table I. Configurable level operation requires switches to be controlled similarly in phase so that the effective number of switches coincides with the desired level operation. When the two middle switch pairs, S_3 and S_2, are operated as one switch pair, configuration $4b$, the blocking voltage of the transistors is more evenly distributed, therefore distributing the voltage stress on each of the transistors. The amount of capacitor voltage change required to transition from 5-level to 4-level operation is also shown in Table I. The configuration with the middle pairs acting as one yields the smallest ΔV, $\frac{1}{12}V_{in}$, required for re-balancing on a new number of levels. This analysis was performed for 5/4, 6/5, and 7/6 level converters. Transitioning from a higher odd number of levels down to an even number of levels reduces the capacitor voltage change required. For the 5/4 converter and the 7/6 converter, the minimum voltage change required is $\frac{1}{12}V_{in}$ and $\frac{1}{15}V_{in}$, respectively compared to the 6/5 level converter which requires $\frac{1}{10}V_{in}$. For the 7/6 level converter, two flying capacitors would need to change by $\frac{1}{30}V_{in}$ and two by $\frac{1}{15}V_{in}$, with one remaining unchanged. However, for the 5/4 level converter, the capacitors which need re-balancing all require the same change in voltage, therefore simplifying the active balancing technique used to re-balance the flying capacitors.

In 4-level operation, the two middle pairs of switches (labeled S_2 and S_3 in Figure 6) are controlled in phase as shown by control signals q_{2A} and q_{3A} in Figure 7a. This switch pair is chosen so that the amount the flying capacitor voltages need to adjust by is minimized. The remaining switch pairs are operated as a 4-level FCML with a phase shift of 120°, shown in Figure 7a. Consequently, the voltage on the middle flying capacitor (labeled C_2 in Figure 6) remains constant at

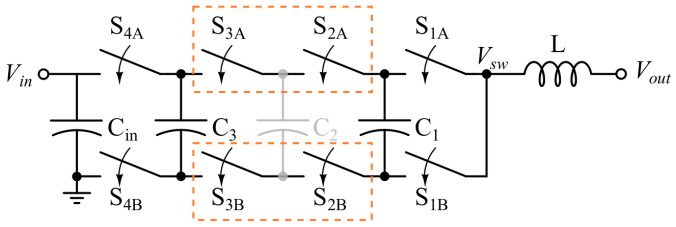
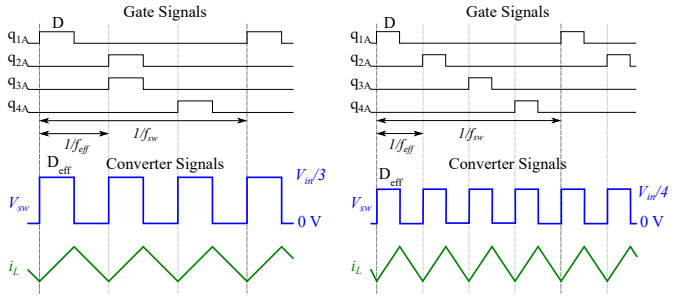


Fig. 6: The 5-level FCML operated as a 4-level with C_2 voltage maintained at the 5-level value while C_1 and C_3 re-balance to 4-level operation.



(a) Four-level operation. (b) Five-level operation.

Fig. 7: Simulated converter waveforms for the proposed method.

$V_{in}/2$ from the 5-level operation, while the remaining flying capacitors, C_1 and C_3 are actively re-balanced to $V_{in}/3$ and $2 \cdot V_{in}/3$, respectively, in accordance with 4-level FCML operation, as shown in Table I.

Similarly, when the converter needs to transition from 4-level to 5-level operation, the capacitors are re-balanced to 5-level voltages by active balancing techniques. The middle switch pairs are no longer controlled by similar PWM signals and the control scheme returns to that of the 5-level FCML, shown in Figure 7b. When sizing the switches and capacitors, the voltage ratings of the 4-level operation should be used since they are of greater magnitude, as shown in Table I.

IV. Active Balancing

Level transitioning requires flying capacitor re-balancing because the steady-state voltages on flying capacitors, C_1 and C_3, are at different values based on the number of levels, as shown in Table I. The FCML topology has natural balancing qualities [15]–[19], which will re-align the capacitor voltages with steady-state operation after some time. However, more switching cycles spent in an unbalanced condition, leads to more uneven voltage stress on the transistors. To reduce the amount of re-balancing time necessary, active balancing techniques can be used. Previous work [9] on level transitioning in FCML converters has used repeated switch states within each cycle in order to increase/decrease the charge on the capacitors. However, this work utilizes a technique of duty cycle adjustment [6], [20], [21] to increase or decrease the charge/discharge time of the flying capacitors that require re-balancing. Active balancing of the converter is done in 4-level operation because FCML converters have more balanced performance on even-numbered levels [19]. When transitioning from 4- to 5-level operation, the flying capacitors are re-balanced to 5-level voltages before the control signals are changed to the 5-level configuration. Table II shows the charge/discharge behavior of the flying capacitors for sub-periods in the lowest duty cycle range of 4-level operation (0 - 33%). For the transition from 5- to 4-level operation, the voltage on capacitor C_1 needs to increase and the voltage on capacitor C_3 needs to decrease, while capacitor C_2 is maintained. To achieve this voltage differential, the sub-period

TABLE II: Flying Capacitor Charge and Discharge Sub-periods

Sub-period	S_{4A}	S_{3A}/S_{2A}	S_{1A}	V_{C3}	V_{C2}	V_{C1}
d1	0	0	1			−
d2	0	1	0	−		+
d4	1	0	0	+		

where C_1 charges (indicated by a '+'), $d2$, when the middle switch pairs (S_2/S_3) are on (indictated by '1' in Table II), should be increased, while the sub-period where C_1 discharges (indicated by a '−'), $d1$, when switch S_1 is on, should be decreased. Similarly, to decrease the voltage on C_3, sub-periods $d2$ and $d4$ should be increased and decreased, respectively. On the contrary, active re-balancing for the transition from 4- to 5-level operation is accomplished by decreasing $d2$ while increasing $d1$ and $d4$. The sub-periods $d1$ and $d4$ are adjusted equivalently and are changed with respect to $d2$ so that the effective duty cycle at the switch node remains equivalent to that of normal 4-level operation [13]. Equation 5 shows the relationship between the switching sub-periods in 4-level operation for duty cycles less than 33%. Applying this duty cycle adjustment technique across multiple switching cycles can re-balance the voltages to the new steady-state operation values as shown in Figure 8. The amount to adjust the sub-periods by is chosen along with the number of active re-balancing cycles.

$$D_{eff} = d2 + d1 + d4 = d2 + 2 * d1 \tag{5}$$

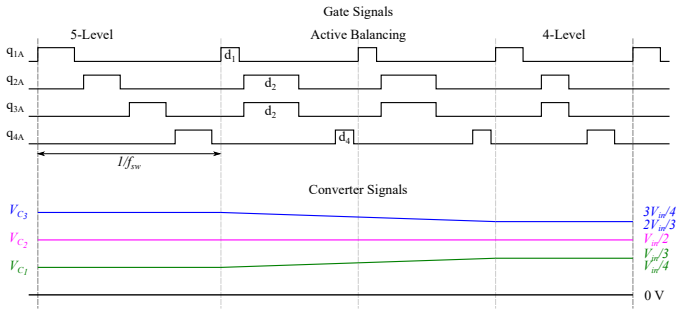


Fig. 8: Active balancing through duty cycle adjustment is implemented at transitions between different numbers of levels.

V. Experimental Prototype

A 5-level FCML converter, Figure 9, was built to demonstrate this control technique that maintains ZVS across the full duty cycle range. The prototype was built using 100 V GaN devices from GaN Systems due to their low conduction and switching losses. Because these GaN devices are bottom-side cooled, the FCML was constructed on a single-sided PCB to facilitate a heat sink across the whole bottom side. Assembling the FCML on a single side increases the commutation loop and introduces more parasitic inductance into the conduction

TABLE III: Component Listing of the Hardware Prototype

Function Block	Component	Mfr. & Part Number	Parameters
FCML	GaN FETs	GaN Systems GS61008P	100 V, 7mΩ
	Capacitors (C_1, C_2, C_3)	TDK C5750X6S2W225K250KA × 3	450 V, 2.2μF
	Capacitors (C_{in})	TDK C5750X6S2W225K250KA × 4	450 V, 2.2μF
	Capacitors (C_{out})	TDK C5750X6S2W225K250KA × 4	450 V, 2.2μF
	Inductor (L)	Vishay IHLP4040DZ-01	12 A, 2.2μH
Cascaded Bootstrap	Isolated gate drivers	Silicon Labs SI8271GB-IS	
	Bootstrap Diodes	Vishay VS-2EFH02HM3	400 V
	LDO	Texas Instruments LP2985IM5-6.1/NOPB	
Controller Board	Logic level shifters	Texas Instruments SN74LV4T125PWR	
	Microcontroller	Texas Instruments TMX320F28377D	

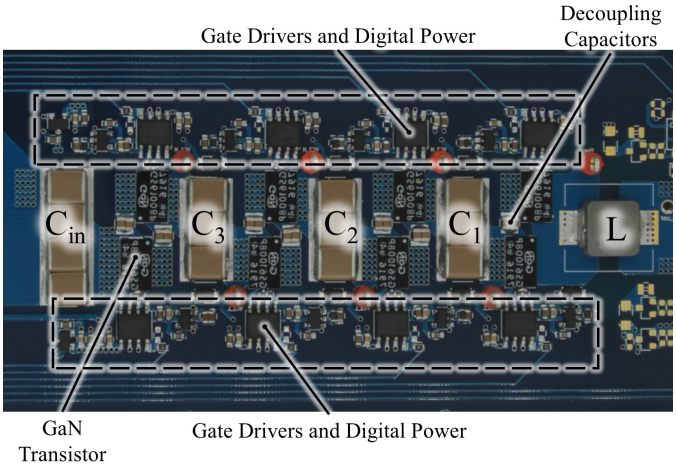


Fig. 9: Annotated photograph of the experimental prototype.

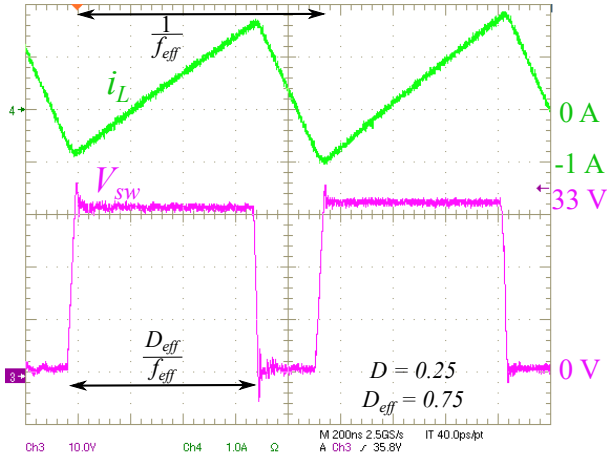


Fig. 10: ZVS is achieved for 4-level operation at a duty cycle for which 5-level operation cannot achieve ZVS.

path. To decrease the commutation loop area and absorb the excess parasitic energy, local decoupling capacitors are used for each switch pair [8]. Additionally, previous work [22] has proven the merit of using a cascaded bootstrap technique to power the isolated gate drivers for each switch of the FCML. The cascaded bootstrap technique has a reduced area and better efficiency when compared to the conventional single IC isolated gate driver [22]. Table III shows the full component listing of the hardware prototype.

VI. Experimental Results

To demonstrate the proposed method, the experimental prototype was tested in multiple operating conditions. Figure 10 shows the converter operating as a 4-level FCML at an input voltage of 100 V, 10 W, a switching frequency of 350 kHz, and a duty ratio of 25%, which, as shown in Figure 4, is an operation point where the 5-level FCML has no current ripple and cannot maintain ZVS. The inductor current ripple is shown to go negative which discharges the parasitic capacitances of the high-side transistors and allows ZVS, which is evident by the minimal overshoot on the rising edge of the switch-node voltage, V_{sw}. Likewise, Figure 11 shows the converter operating in ZVS as a 5-level FCML at the same voltage and loading condition, a 255 kHz switching frequency and

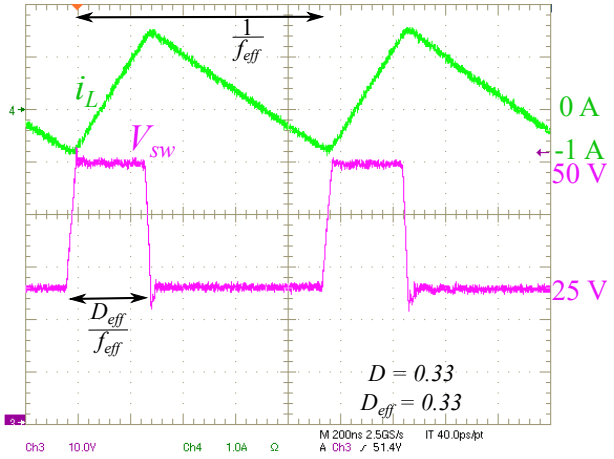
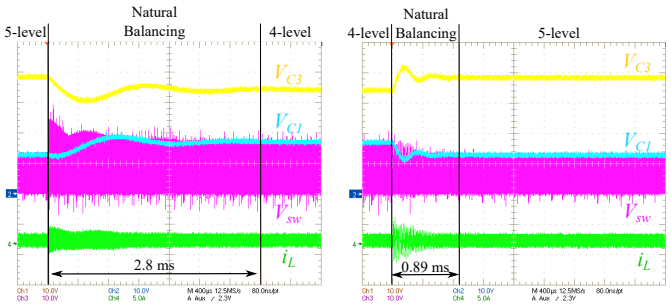


Fig. 11: ZVS is achieved for 5-level operation at a duty cycle for which 4-level operation cannot achieve ZVS.

a 33% duty ratio, which is a current ripple valley of the 4-level converter. These results show that ZVS is possible at two different duty cycles for which ZVS is not possible with a fixed number of levels.



(a) Five to four level transition. (b) Four to five level transition.

Fig. 12: Level transitioning with natural balancing.

A dynamic transition between levels is demonstrated in Figure 12. In this case, the converter transitions from 5-level to 4-level operation (Figure 12a) and vice-versa (Figure 12b) with only natural balancing. The measured settling time of the capacitor voltages, V_{C1} and V_{C3} for the 5- to 4-level transition is about 2.8 ms and from 4- to 5-levels is about 0.89 ms. Figure 13 shows the transition from 5- to 4-level operation with a region of active balancing by duty cycle adjustment to charge C_1 and discharge C_3 from 5-level steady-state voltages to 4-level voltages. The capacitor voltages balance to steady-state in 88 μs, which is over 30 times faster than the settling time using natural balancing. Figure 14 shows the transition from 4- to 5-level operation with active balancing, which takes 0.66 ms, which is about 1.3 times faster than natural balancing alone.

When performing active balancing, two parameters can be tuned for different balancing characteristics — the magnitude of duty cycle adjustment, and the number of active balancing cycles. If rapid balancing is desired, the percent change of duty cycles is set high, with a corresponding low number of active balancing cycles. Alternatively, slower, but with less inductor current ripple induced, balancing operation can be achieved with low percent change of duty cycles, and a higher number of active balancing cycles. In the case of the 5- to 4-level transition, shown in Figure 13, seven cycles of active balancing were used and the sub-periods were adjusted: $d2$ was 40%, or twice the width of the baseline duty cycle of 20%, and $d1$ and $d4$ where each 10%, maintaining a constant effective duty cycle at the switch node of 60%. This approach demonstrates a more aggressive duty cycle adjustment with a smaller number of active balancing cycles, which leads to a shorter settling time, with the trade-off of a brief time period with increased current ripple. However, if a more moderate adjustment to duty cycle and more cycles of active balancing can be permitted,

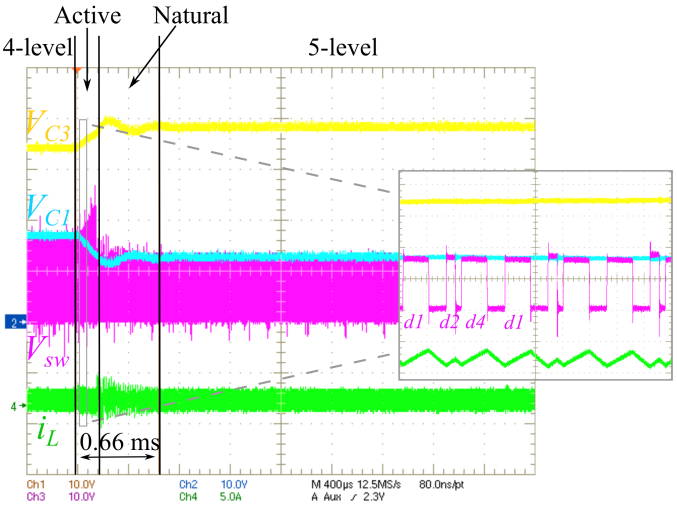


Fig. 14: Active balancing decreases the settling time of capacitors C_1 and C_3 during a transition from 4- to 5-level operation.

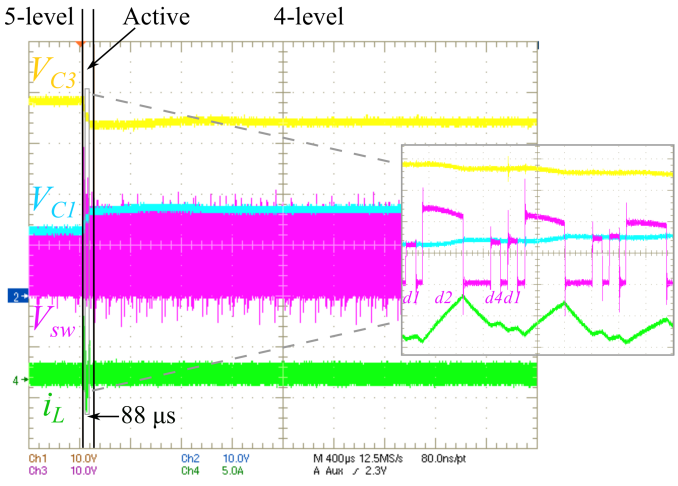


Fig. 13: Active balancing decreases the settling time of capacitors C_1 and C_3 during a transition from 5- to 4-level operation.

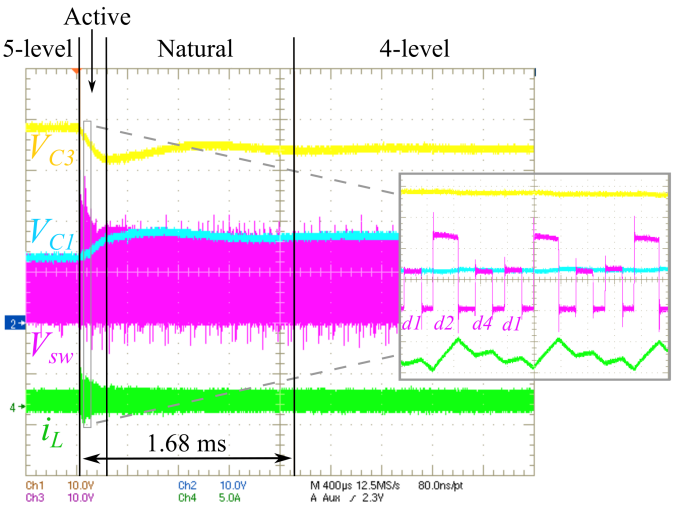
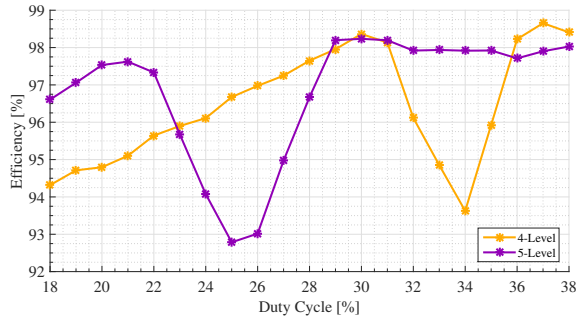


Fig. 15: Level transitioning with less aggressive active balancing has a longer settling time, but a lower magnitude of increased inductor current ripple.

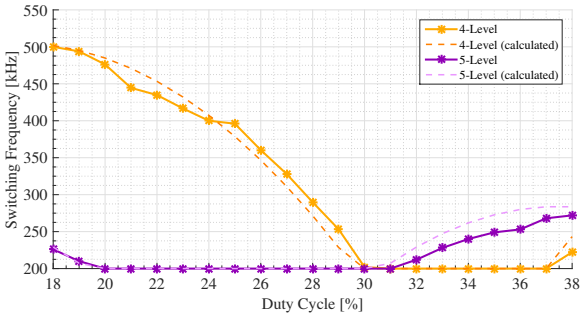
then the magnitude of the increased current ripple can be lower as shown in Figure 15 ($d2$ at 25% for 25 cycles) as compared to aggressive re-balancing in Figure 13. Both moderate and aggressive implementations of active balancing still reduce the settling time when compared to natural balancing.

To demonstrate the efficiency benefits of the proposed control method, we tested 4- and 5-level operation over a wide range of duty cycles. The efficiency at each duty cycle was measured in 4- and 5-level operation at 100 V_{in} and 0.5 A load with constant negative inductor current peak, I_{ZVS}, with a high precision power analyzer (Keysight PA2201A). The frequency was adjusted to achieve ZVS conditions, if possible, without violating the converter frequency limitation of 200 kHz. The switching frequency required for each 4- and 5-level operation is different, which is necessary as discussed above. Figure 16a shows the efficiency of 5- and 4-level operation at each duty cycle, which aligns with the proposed level transitioning technique in Figure 5. Operation as a 4-level converter is more efficient for the duty cycle ranges 23-28%, whereas operation as a 5-level converter is more efficient for 18-23% and 29-35%. The 4-level converter is more efficient than the 5-level converter when the 5-level converter exhibits a current ripple minimum and cannot maintain ZVS, but where the 4-level can. In this case, the switching losses and core losses in non-ZVS 5-level operation are greater than the core losses on the 4-level converter. For the duty cycle range of 29%-32%, the 5-level performance in ZVS conditions is similar to 4-level performance. Here, both 4-level operation and 5-level operation are at similar switching frequencies (as shown in Figure 16b) and inductor current ripple, so the losses are expected to be mostly equivalent.

In the duty cycle region 36-38%, the 4-level converter unexpectedly has a higher efficiency. In this region, both 4- and 5-level converters can maintain ZVS with similar inductor current ripple, but in our proposed method, we prioritize 5-level operation assuming the losses would be less than 4-level operation due to lower voltage stresses on the switches. Figure 16b shows that in this duty cycle range, the switching frequency of the 5-level converter needed to maintain ZVS is larger than for 4-level operation, which contributes to higher switching losses and lower efficiency. Further research can investigate more flexible transition patterns to take advantage of higher efficiencies in regions like this across the full duty cycle range. For both the 4- and 5-level converters, when ZVS can be maintained, the switching frequencies display a nearly sinusoidal characteristic similar to that of the proposed method and equations of [8]. Despite the 4-level converter operating at a much higher switching frequency, the switching losses can be reduced by maintaining ZVS, therefore demonstrating the benefit of dynamic level transitioning in order to maintain ZVS across duty cycles.



(a) Efficiency measurements of 4- and 5-level operation, maintaining ZVS where possible without violating converter switching frequency limitations.



(b) Corresponding switching frequencies for 4- and 5-level operation.

Fig. 16: Higher efficiencies closely correspond with the proposed method in Figure 5. The corresponding switching frequencies match the calculated switching frequencies for the proposed method.

VII. Conclusion

This paper presented a method for maintaining ZVS across the full range of duty cycles for an FCML converter by both controlling the switching frequency and dynamically changing the number of levels. An analysis of flying capacitor voltages and switch configurations was used to determine the number of levels and the switching scheme to achieve dynamic level transitioning. Additionally, a method of dynamic level transitioning with active capacitor balancing through duty cycle adjustment was detailed. A hardware prototype was constructed using bottom-side cooled GaN Systems devices, a single-sided PCB for improved cooling methods, and a cascaded bootstrap to supply the isolated gate drivers. The prototype achieved ZVS operation under 4-level and 5-level conditions at duty cycles not possible for a fixed number of levels. Dynamic level transitioning with active re-balancing of the flying capacitors was demonstrated in hardware. Transitioning between numbers of levels to avoid inductor current ripple valleys and maintain ZVS improves converter efficiency by reducing switching losses, which allows for more power dense designs.

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