# Lawrence Berkeley National Laboratory

**Title**
An overview of the DPAD detector for protein crystallography

**Permalink**
https://escholarship.org/uc/item/7r73f21b

**Author**
Datte, Philip

**Publication Date**
1999-07-01

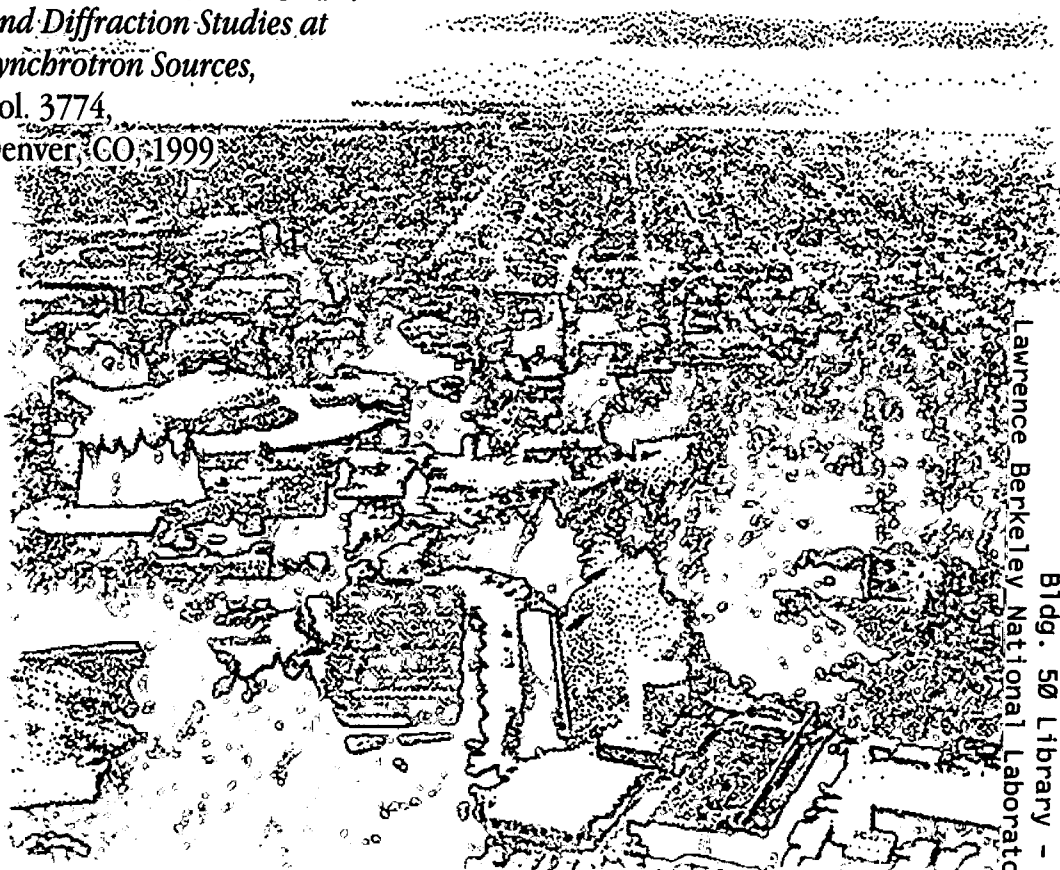# ERNEST ORLANDO LAWRENCE BERKELEY NATIONAL LABORATORY

# An Overview of the DPAD Detector for Protein Crystallography

P. Datte, J-F. Beche, F. Druillole, P.F. Manfredi, J. Millaud, and N-h. Xuong

**Engineering Division**

## DISCLAIMER

# An Overview of the DPAD Detector
# for Protein Crystallography

P. Datte,[1] J-F. Beche,[1] F. Druillole,[1] P.F. Manfredi,[1]
J. Millaud,[1] and N-h. Xuong[2]


[1]Engineering Division
Ernest Orlando Lawrence Berkeley National Laboratory
University of California, Berkeley, California 94720

[2]Department of Chemistry and Bio-Chemistry
University of California at San Diego
La Jolla, California 92093

July 1999

# AN OVERVIEW OF THE DPAD DETECTOR FOR PROTEIN CRYSTALLOGRAPHY

P.Datte[1*], J-F. Beche[1], F.Druillole[1], P.F. Manfredi[1], J. Millaud[1], N-h. Xuong[2]

[1]Engineering Division, Lawrence Berkeley National Laboratory, University of California, Berkeley, CA 94720, USA

[2]Department of Chemistry and Bio-Chemistry, University of California at San Diego, La Jolla CA, 92093, USA

## ABSTRACT

A 2D photon counting digital pixel array detector (DPAD) is being designed for static and time resolved protein crystallography. This room temperature detector will significantly enhance monochromatic and polychromatic protein crystallographic throughput data rates by more than two to three orders of magnitude when compared to present data collection systems. The detector has an unbounded photon counting dynamic range and exhibits superior spatial resolution when compared to present crystallographic phosphor imaging plates or phosphor coupled CCD detectors. The detector is a high resistivity N-type Si with a pixel pitch of (150x150) microns, and a thickness of 300 microns that is bump bonded to an application specific integrated circuit (ASIC). The event driven readout of the detector is based on the column architecture and allows an independent pixel hit rate above 1 million photons/sec. The device provides energy discrimination and sparse data readout that yields minimal dead time. This type of architecture allows an almost continuous (frame-less) data acquisition, a feature not found in any current detector being used for protein crystallographic applications. For the targeted detector size of (1000x1000) pixels, average hit rates greater than $10^{11}$ photons/sec for the complete detector appears achievable. This paper will present an overview of the hybridized detector performance which includes the analog amplifier response and the photon counting capabilities of the (16x16) array operating with both digital and analog circuitry. Also the operation of the serial interface will be described.

Keywords: Crystallography; Pixel Detector; Area Detector; Image Sensor; Si Detector

*Corresponding Author. Tel.: +1 510-495-2906; Fax: +1 510-486-7557
EMAIL:PSDatte@lbl.gov

## I. INTRODUCTION

X-ray crystallography has become a major tool for the study of molecular structures in biology. The very intense X-ray flux now available at synchrotron light sources provides for a rapid acceleration of these studies as well as for finer resolution of the structures[1]. The protein crystallography X-ray facilities urgently need advanced X-ray detectors that can accommodate the high luminosity and broad bandpass X-rays beams that are produced by these machines. The principal methods of data collection are monochromatic and polychromatic (Laue diffraction) radiation. Present detector technologies used at light sources are typically based on an analog integrating measurement of the X-ray intensity. These detectors include imaging plates, and phosphor screens coupled to CCDs. The integrating detectors have the advantage of being able to accommodate the very high intensity beams, which are common at these facilities. However they display a large point spread function and suffer from inadequate dynamic range and readout speed. These devices do not provide energy discrimination, and for time resolved crystallography, these devices can not meet the demands of millisecond multi-frame time resolution.

The Digital Pixel Array Detector (DPAD) presently being designed will offer a substantial (two to three orders of magnitude) improvement in dynamic range over present technology and, for the first time, offer truly frameless readout for high speed time resolved crystallography. The complete assembly consists of modules of (50x50) arrays assembled in a tiled arrangement. The detector for each module is a reverse biased Si diode array bump bonded to an Application Specific Integrated Circuit (ASIC). The detector pixel pitch is 150μm and the charge collection electrode is $(100x100)\mu m^2$. The ASIC contains both analog and digital circuitry which process a photon event and generates the associated pixel address in less than 80ns in the parallel output configuration. Each pixel processor has a preamplifier, shaper, differential discriminator and a 3-bit prescaler that divides the pixel event rate by 8, hence reducing the external data flow bandwidth requirements. At the end of the acquisition cycle the prescaler contents can be read out and combined with the histogram data. An overflow bit or pseudo 4th bit starts the readout logic sequence to generate the pixel address. The event-driven address is generated by the column architecture[2]. The pixel address is then sent off chip for processing to a VME pixel module which assigns additional column and page address-encoding bits. The combined bits are pipelined to the VME histogram memory processing module. The histogram data is stored in VME memory where the contents can be read by the CPU for off line

processing. It should be noted that the DPAD is a true digital photon counting device and is fundamentally different from other approaches that are presently being developed for X-ray imaging and crystallographic applications[3]. Figure 1.0 shows a single (50x50) module that will be assembled into a larger array.
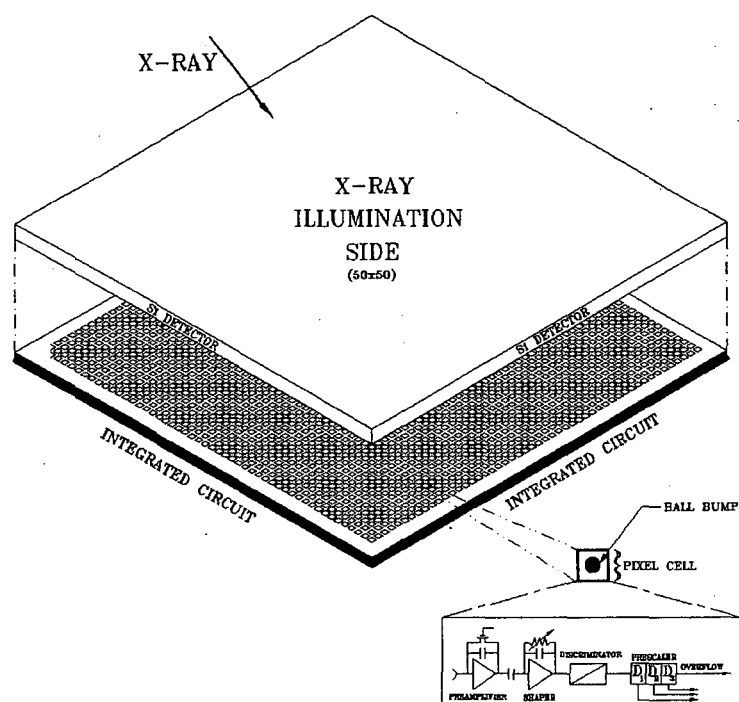


Figure [1.0] A single (50x50) module assembly that contains the hybridized detector and ASIC.

## II. SYSTEM DESIGN WITH SERIAL OUTPUT

The detector system consists of the application specific integrated circuit, bump bonded to a Si detector. The ASIC contains the pixel processor, column logic and end-of-column logic[4]. Data is transferred out of, and into the ASIC through a bi-directional serial interface. A FIFO interface receives data from the ASIC and provides data flow buffering to the histogram memory. The histogram memory performs a plus one operation on the pixel addresses data register contents and the VME computer interface provides programming capability and access to permanent memory storage. Two small local SRAM's are integrated into the system. One SRAM provides local storage for the read remainder contents that are retrieved from the prescaler of each pixel and the other provides storage for the mask and calibration data for programming the pixel processor. The latter SRAM, which stores the mask and calibration information for each pixel is written to before the reset of the ASIC. The SRAM is read during the read remainder mode.

Operation of the ASIC begins after power up by clearing the pixel prescalers and setting each pixel to the appropriate state (mask and calibration). The prescalers are reset through the read remainder operation. The prescaler is reset after the contents have been read and is the first operation after power up. Each pixel has a local two bit memory which stores the mask and calibration information for that pixel. The writing to this memory sets each pixel state. The two bit information is transferred from the local SRAM to the ASIC at the end of each read remainder cycle for that pixel. This method combines two operations on the same transfer cycle for each pixel. The pixel can have three programming states; mask, calibration or both. The mask function can be used for disabling the digital portion of the pixel, preventing any digital activity on the column logic. Noisy pixels or strong crystallographic reflections that occur during operation can be eliminated using this function. The calibration function typically is used to test the operation of each pixel for proper functionality. A programmable test capacitor is located at the input to each pixel and proper pulsing of this capacitor can mimic a photon event. The propagation of this test pulse through the logic will verify that the circuitry is functional up to and including the histogram memory.

Data leaving the ASIC can be of two forms, pixel address information and read remainder information. The two types of data share the same data lines (in serial operation) and proper handling of the data must be accommodated. Data is transferred

from the ASIC to the FIFO memory by a bi-directional serial shift register. Two dual columns share one "column FIFO". For a (16x16) ASIC four, "column FIFOs" are used to handle all the data flow out of the ASIC. A modified ring counter transfers data from the four "column FIFOs" to a single "master FIFO" that is connected to a histogram memory. The ring counter services only the "column FIFOs" that contain data and the logic guarantees that no one particular FIFO is favored over another. This allows equal processing of all columns. The histogram memory performs a plus one operation on the data and has a depth of 16 bits. In read remainder mode the data passes through the four "column FIFOs" and is redirected after the ring counter to local SRAM storage. The read remainder data and the histogram memory data are scaled and combined externally to form a complete data set.

This type of readout architecture provides the ability for almost non-stop photon counting with and unbounded dynamic range. The histogram memory paging capability allows each image frame to be stored in different memory areas (see section V). In this ways the dead time of the system is the time required to read the prescaler contents (8 counts). With other photon integration techniques, the crystal sample is normally rotated at constant angular velocity during each integration time interval and then stopped while the integration data is read out. For short exposures, this requires careful synchronization of fast photon shutters and precision sample goniometers. The DPAD's continuous readout architecture permits non-stop rotation of the sample over the entire range required for data collection.
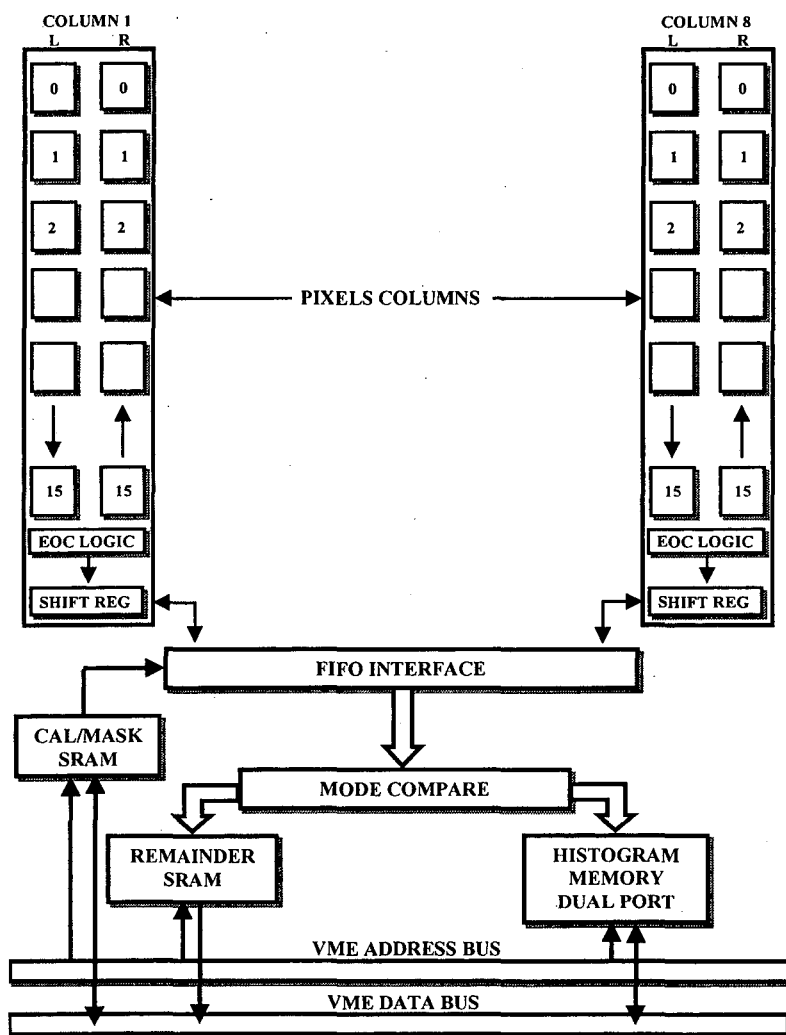


Figure 2.0. The system level interface of the DPAD detector containing the ASIC (8 dual columns), FIFO interface and histogram memory with VME interface.

# III. FRONT END ELECTRONICS AND PIXEL PERFORMANCE

The front end analog electronics has been designed in the HP 0.5 μm 3 metal process and consists of a preamplifier with a DC reset and a shaping amplifier which forms a RC-($C^2R$) shaping network. The combined gain of the circuit is 690mV/fC or 110mV/1000e⁻. The measured noise level is 60e⁻ (rms) @ 5.9keV ([55]Fe) using a Si detector with a total input capacitance 0.3pF. The overall analog power consumption is 50 μWatts/channel. A complete description of the circuit can be found in references [5,6,7]. Table 1.0 lists some of the more important circuit characteristics.

| Amplifier Parameters | Measured Values |
|---|---|
| Total Gain | 110mV/1000e⁻ |
| Reset Time (adjustable) | 1 μs |
| Peaking Time (50ns to 150ns adjustable) | 100 ns |
| Power (analog only) | 50 μW/Channel |
| Noise @5.9keV (Si pixel capacitance 0.3pF) | 60e⁻ - rms (480eV) |

Table 1.0 DPAD analog front-end electronics measured values.

Figure 3.0 shows the analog performance of the pixel amplifier. The plot is the pulse height analysis of a typical pixel in the detector. The Fe[55] 5.89 keV FWHM is 480 eV (60e- rms) and the 6.49 keV peak is visible as a bump to the right of the 5.89 keV peak. The small plateau at the lower energies is a result of charge trapping due to an oxide layer on the surface of the detector between the pixel electrodes. This represents a reduction in the amplifier amplitude of a photon event and with the proper setting of the discriminator the event will not be lost.

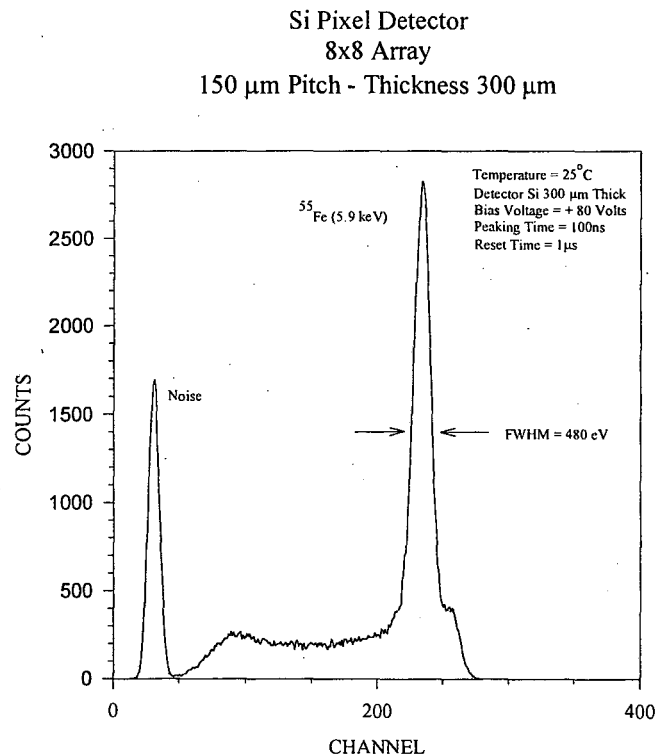Si Pixel Detector
8x8 Array
150 μm Pitch - Thickness 300 μm



Figure 3.0. Energy plot of a single Si pixel at room temperature. The Fe[55] 5.89 keV FWHM is 480 eV (60e⁻ rms), the 6.49 keV line is visible as a small bump to the right of the 5.89 keV line.

Figure 4.0 shows a linear plot of the amplifier. From this plot it can been seen that below 16 keV the amplifier operates quite well. Above 16 keV the preamplifier becomes nonlinear and is off by 8% at 20 keV. This would result in a nonlinear discriminator setting where energy discrimination is required and should be taken into account when X-ray energies above 16 keV are used.

Si Pixel Detector
Linear Energy Plot
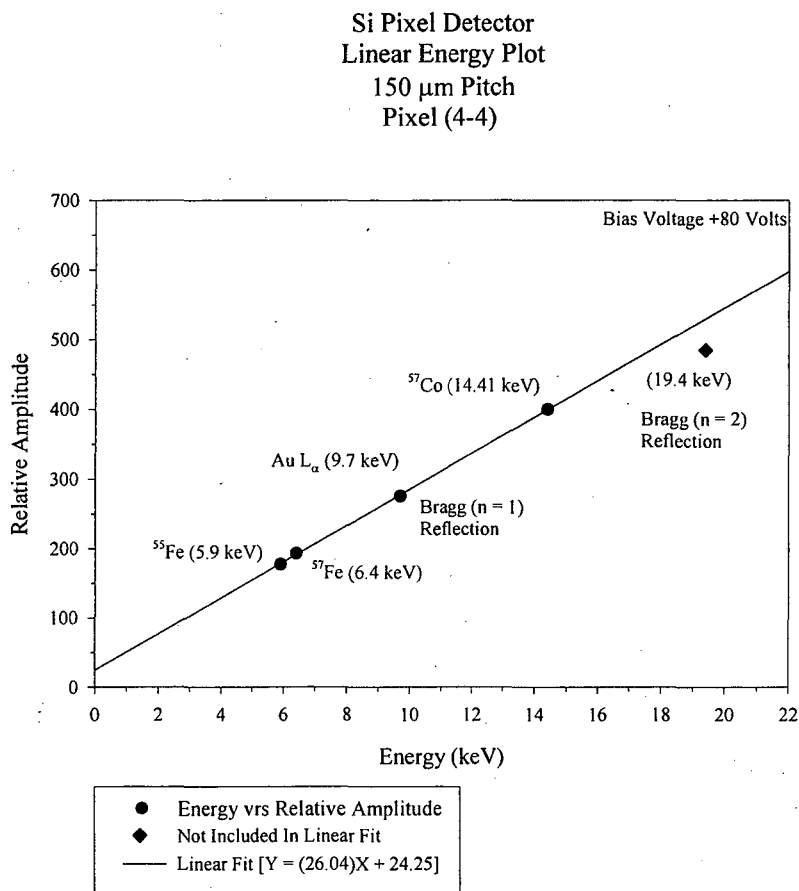150 µm Pitch
Pixel (4-4)



Figure 4.0. Linear plot of a Si pixel. The linearity falls by 8% at 20 keV.

The excellent digital characteristics of the detector are shown below in figure 5. The pixel dimensions (150 µm) are clearly visible and representative of the entire array. The measurement was taken with a highly collimated 10 keV X-ray beam scanned at 10 µm steps. The discriminator was set to 80 mV or 800 electrons. With this discriminator setting the cross talk between pixels is zero as seen by displaying the counting totals for each pixel on the same graph.
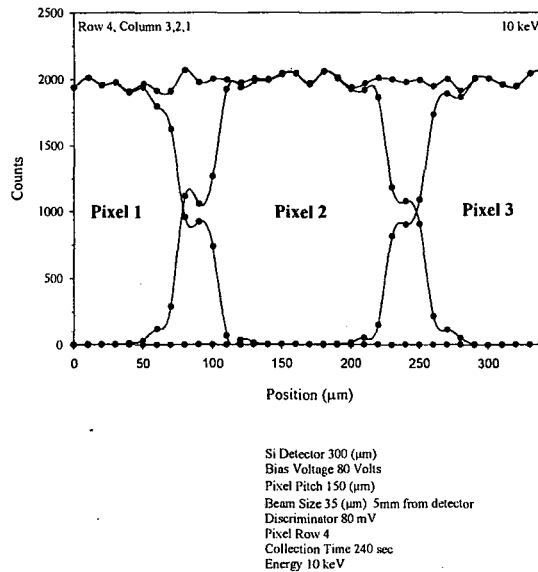
Figure 5.0. Plot of the digital "electrical" pixel dimensions of the Si pixel detector. The 150 μm pixels are clearly seen when scanned with a 10 keV X-ray beam. Viewing the total counts for each pixel demonstrates that there is no cross talk between pixels with a discriminator setting of 80 mV (800 electrons) or higher.

## IV. ASIC SIGNAL PROCESSING

The present ASIC is a (16x16) device and is a smaller version of the final (50x50) design. The (50x50) ASIC consists of a pixel processor that converts a single photon event into a digital pulse. The pixel processor consists of an analog charge integrating preamplifier and an adjustable shaping amplifier, a discriminator, 4-bit prescaler. The pixel processors are organized in columns. The maximum number of pixels in a single column is 50. Each column of 50 is grouped in pairs to form a dual column containing 100 pixels. A photon event is electronically recorded when a pulse from the output of the amplifier drives a differential discriminator circuit that converts an analog signal into a logic level. The logic level is used as the input to a 3-bit counter and divides the number of photon events by eight. The $4^{th}$ bit of the counter is used as an overflow bit and signals the column processor that a pixel address is available for processing. This process is event driven and is asynchronous to the system clock. Beginning with pixel 0, the column processor using ripple logic, performs a sparse scan on the dual column in response to an overflow from a prescaler in the dual column. The column logic services the overflow event and resets the overflow bit. Each time the column processor encounters a pixel with the overflow bit on, the address of that pixel is loaded in an 8-bit shit register at the end of the column. The pixel address is then shifted out at the system clock rate to an external FIFO memory for that column. While a pixel overflow bit is on, the pixel prescaler is not disabled and can continue to process photon events while the column logic is processing that pixel address. In addition, simultaneous overflow events that occur in the dual column are serviced in a sequential manner beginning with pixel 0. Reference [4] describes in detail the internal logic and control circuitry of the column architecture and the parallel data output capability.

The final version of the ASIC converts the parallel data lines to a single data line through an 8-bit, bi-directional, serial shift register (one line per dual column). Also the 2-bit programming of each pixel, (mask and calibration) is now incorporated in the same shift register allowing a single data line to transmit and receive data for each dual column. To facilitate the input and output shifting of data, a system clock is used to synchronize the event driven

column logic with the shift register. The clock frequency is scalable over a broad range from a few Hertz to more than 50 MHz (the original specification). All data cycles are synchronous to the falling edge of the clock. The clock is distributed at the bottom of the column logic. The pixel uses individual master clock related signals but only on an event driven basis to initiate the column logic. In this manner the analog portion of the ASIC is completely immune to digital logic transitions generated by the system clock. Figure 6.0 shows the data structure of this interface. The start of each event driven data transfer always begins with a "start" bit going high (bit 1). When the ASIC is in data acquisition mode the remaining bits is the pixel address starting with the LSB of the 7-bit pixel address represented by ($D_0 - D_5$). The MSB ($D_6$) of the pixel address is the Left/Right bit for the column logic and proper decoding of the address is required. Seven bits of data plus a start bit yield the maximum number of clock cycles per data transfer. The figure shows the bit representation of a series of addresses on the right and left sides of one dual column, beginning with the valid pixel address 0-right column. 0-left column is also shown and proper decoding would assign this value to pixel 16 in a dual column system. Additional pixel addresses are shown for various addresses.
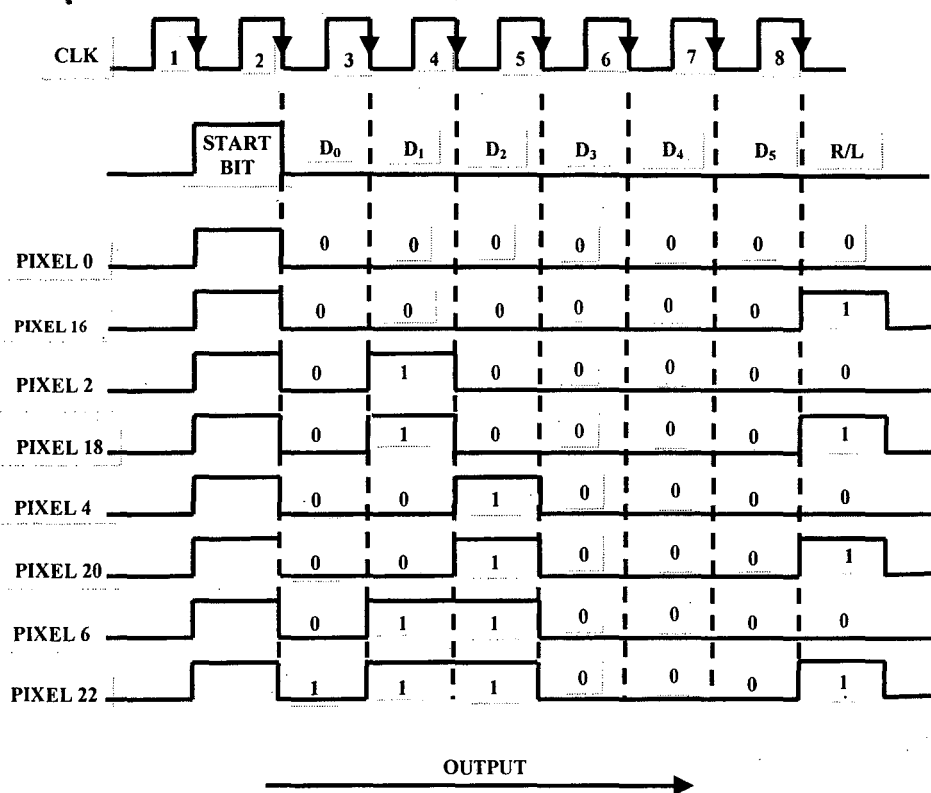


| CLK | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| | START BIT | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | R/L |
| PIXEL 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PIXEL 16 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| PIXEL 2 | | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| PIXEL 18 | | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| PIXEL 4 | | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| PIXEL 20 | | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| PIXEL 6 | | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| PIXEL 22 | | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

OUTPUT →

Figure 6.0 The pulse structure of the data transfer for the serial interface. The MSB of the data transfer ($D_6$-R/L) defines which column of the dual the pixel address belongs to. Proper decoding should be adhered to when handling this data bit.

Figure 7.0 shows the first 5 pixel addresses (0-4) for the operational (16x16) ASIC. This data was acquired using a logic analyzer with a nominal clock speed of 500 kHz.
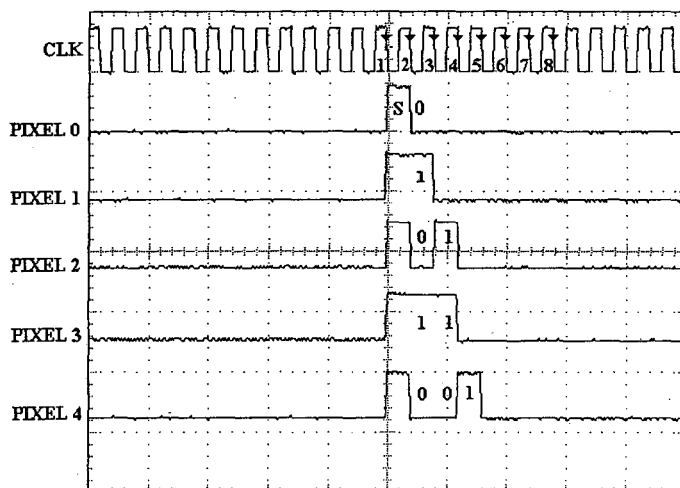


Figure 7.0. Serial data output of the (16x16) ASIC showing addresses 0 through 4. Nominal clock frequency is 500 kHz.

Figure 8.0 shows the independent operation of each dual column. The top trace is the system clock and is synchronous to all shift registers. However because the column logic is asynchronous and event driven, data only appears at the output of the shift register when an overflow bit is active in that column. The second trace is the output of dual column 1 and has a pixel address of 22. The third trace is dual column two operating in a completely independent manner with respect to column 1 and has the pixel address of 21 displayed. It can be seen that the addresses are completely independent and do not interfere with neighboring columns.
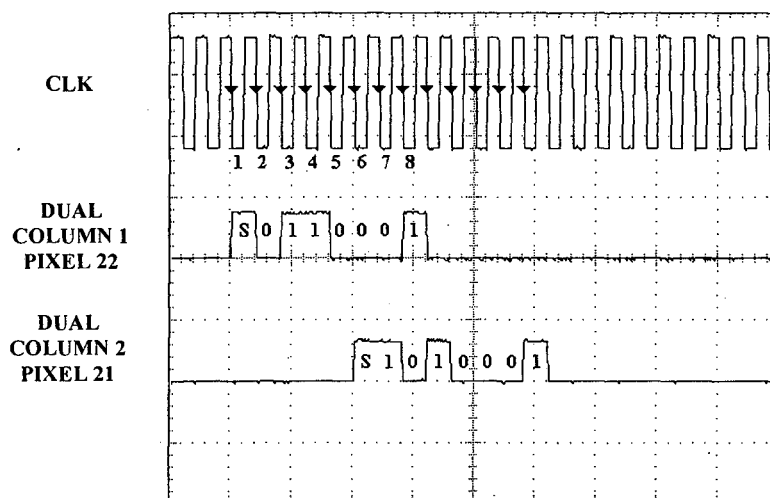


Figure 8.0. Plot of two independent dual columns operating with the same system clock. Second trace is dual column 1 with address 22 and the third trace is dual column 2 with address 21.

The read remainder mode is a synchronous operation and allows access to the contents of the prescalers in the dual column. During this data cycle the mask and calibration bits can be set for each pixel. The cycle begins when the read remainder control line is set high. In a dual column, each pixels prescalers contents starting with pixel 0 are sequentially readout through the column logic. The contents of each prescaler are displayed on the serial shift register output. As described above the transfer always begins with a start bit. Following the "start" bit the next three bits are the prescaler contents beginning with the LSB ($D_0$) through ($D_2$). The fifth and sixth bit of the transfer are not used, however on the fifth clock cycle the data line changes direction to allow data flow to the ASIC. The programming of the mask and calibration bits for each pixel is completed on the seventh and eighth clock cycle. This programming occurs when the column logic sequentially scans each pixel in the dual column to retrieve the prescaler contents. After the transfer of the prescaler contents has occurred, the two-bit memory for that pixel which stores the mask and calibration information is loaded. After the 8 clock cycles when the pixel prescaler has been read and the two-bit memory has been loaded, the column logic moves to the next pixel. The read remainder sequence ends when the last pixel in the column has been accessed. Although each dual column in the ASIC operates asynchronously and independently in the data acquisition mode, the read remainder cycle is common to all dual columns in the ASIC. The total time to acquire the prescaler contents equals the number of pixels in a dual column, times the system clock, times 8 (the number of clock cycles in the shift register). For the (16x16) ASIC this would be: 32 pixels in a dual column (16 pixels times 2), times a twenty nanosecond system clock (50 MHz), times 8 or approximately 5 microseconds. For the targeted (50x50) ASIC, the sequence will be 16 microseconds. Figure 9.0 show the waveforms for the read remainder data transfer cycle and various combinations of data and programming values.
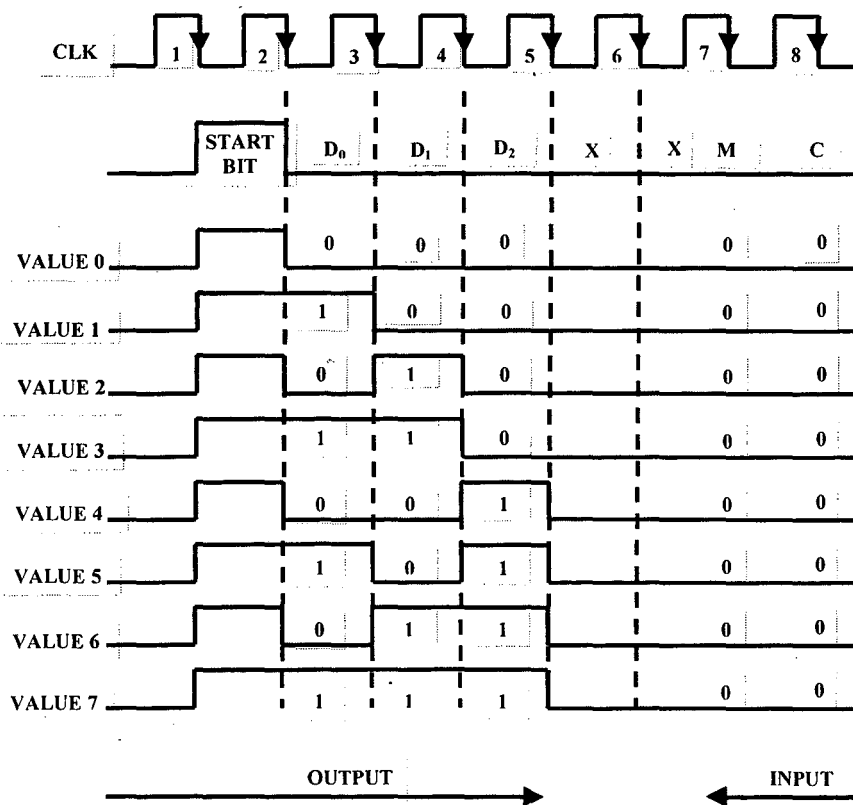


Figure 9.0. Timing diagram of the read remainder mode. A single bi-directional line is used for data transfer out of and into the ASIC.

Figure 10 A and B show the read remainder cycle for the (16x16) ASIC with a nominal system clock of 500 kHz. Figure A shows the prescaler contents 0 though 4 and figure B shows the contents 4 through 7. In all data transfers, the calibration bit has been programmed and the mask bit is turned off.
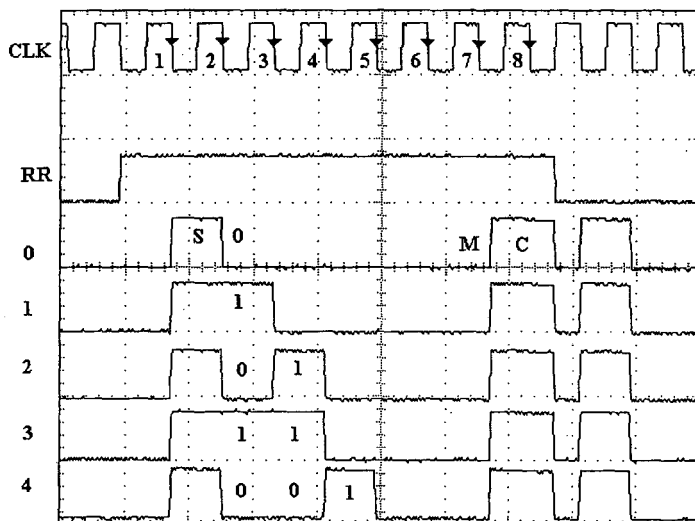


Figure 10.0 A. The ASIC operating in the read remainder mode and the first 5 values of the prescaler are displayed, values (0-4).
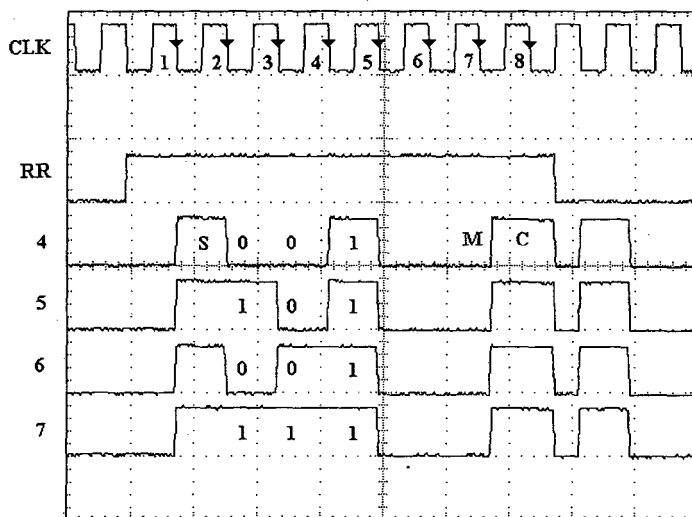


Figure 10.0 B. The ASIC operating in the read remainder mode and the last 4 values of the prescaler are displayed, values (4-7).
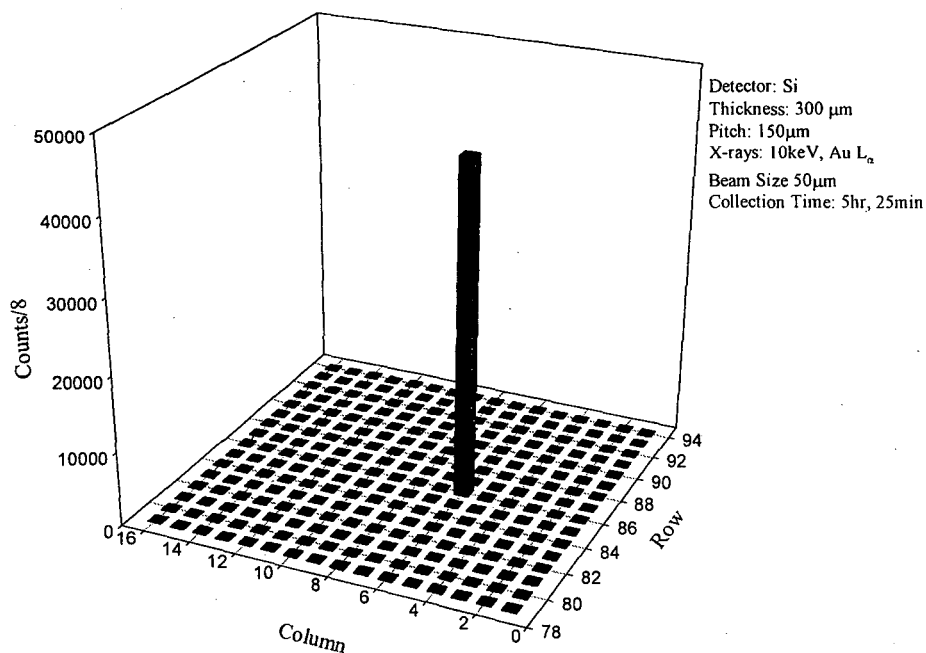
# V. HISTOGRAMMING MEMORY

The histogram memory that is presently in operation is a single port (32kx16) bit memory that performs a plus one operation on the data register contents of the incoming pixel address. The pixel address is directly memory mapped to the histogram memory. 15 bits represent each pixel address ($D_0$-$D_{14}$). The first seven bits is the pixel address in the dual column ($D_0$-$D_6$). The next bit defines one of two dual columns in the "column FIFO" ($D_7$). Two additional bits define one of the four possible column FIFOs that is being serviced by the ring counter ($D_8$-$D_9$). There is an additional 5 bits that define one of 32 available frames or pages ($D_{10}$-$D_{14}$). As the system expands in the size of pixels the paging area will be reduced. Framing allows for continues operation of the histogram memory by offsetting the active memory area. The data collection area can be change virtually instantly by programming a new page value. A counter that is pulsed by an external source can also control the page value. This capability provides the ability to perform time resolved crystallographic experiments on a frame by frame basis in the microsecond time scale. The clock frequency of the histogram operation is 50 MHz. This frequency is limited by the propagation delay of the plus one adder carry bit that operates on the histogram memory 16-bit register contents. One complete operation takes 100 ns (read-modify-write) and is reduced to 80ns if the data is back to back (i.e. pipelined).

Modifications to this technique that effectively double the plus one operation are underway. The first implementation is to change the memory from a single port to a dual port. This allows pixel addresses that are stored in the master FIFO to be serviced twice as fast. Bus conflicts between ports will not occur because there can never be two consecutive pixel addresses with the same value. Dual port operation can also provide access to a bank of memory via the VME bus with out interrupting the pixel processing operation on the other port. Switching one port from the pixel processing operation and connecting it to the VME bus allows CPU access to the histogram memory on the fly. In this way data can continue to be acquired on one port while external access is provided on the other port. Additional speed can be gained by breaking up the 16-bit data register into groups of 4 bits. This will allow a much faster propagation of the adder carry bit. In this way the carry bit will only propagate 1/4 of the time to the next group of 4 bits in the 16-bit word, allowing an increased clock speed on average. When the carry bit does occur an additional cycle will be provided to accommodate the carry bit delay.

# VI. DATA COLLECTION RESULTS

The results from a completed (16x16) pixel detector that is operating with parallel data outputs is shown below in figure 11.0. The X-ray source was a 10 keV L$\alpha$ X-rays from a gold rotating anode. The beam was collimated to a 50 µm size and a distance at 1 mm from the detector. The collection time was 5 hours and 25 minutes. The displayed numbers of interest centered at the peak clearly show the full width at 1/100 maximum ($\Gamma 0.001$) is less than 1 pixel width. The overall scale is reduced by a factor of 8 due to the prescalers.

16x16 Si Digital Pixel Array Detector



Detector: Si
Thickness: 300 μm
Pitch: 150μm
X-rays: 10keV, Au L$_\alpha$
Beam Size 50μm
Collection Time: 5hr, 25min

| 7 | 2 | 0 | 2 | 4 |
|----|-----|-------|-----|---|
| 11 | 8 | 6 | 0 | 6 |
| 4 | 27 | 51 | 10 | 4 |
| 13 | 127 | 44529 | 27 | 6 |
| 11 | 20 | 37 | 15 | 4 |
| 6 | 4 | 4 | 3 | 3 |
| 4 | 1 | 6 | 1 | 4 |

Figure 11.0. A single pixel image of the (16x16) array when illuminated by 10 keV Au L$_\alpha$ X-rays. The X-ray beam was collimated through a 50 μm hole at a distance of less than 1 mm. The data collection time is 5 hours and 25 minutes. The data has not been scaled to reflect the 3 bit prescaler for each pixel; to get the total count you must multiply by 8.

## VII. DETECTOR MODULE

The DPAD is a (15x15) cm$^2$ detector which is composed of a (1000x1000) array of (150x150) μm$^2$ pixels. The detector will be built using a (50x50) hybrid chip as the basic building block. An implementation of a (15x15) cm$^2$ detector containing 10$^6$ pixels is shown in figure12.0 Twenty rows containing twenty (50x50) detector/ASIC modules are staggered in a dual staircase like configuration. In order to allow the routing of cables, the spacing between each row is about 1mm from detector surface to detector surface. These flex cables will be made of metal on kapton or polyamide. The dual staircase configuration reduces by half the detector module thickness to approximately 10mm. The row overlap will be at most 150 μm (one pixel width). Each half of the detector module (10 rows) can be rotated about the symmetric center plane to accommodate various angles of the detector surface with respect to the crystal.
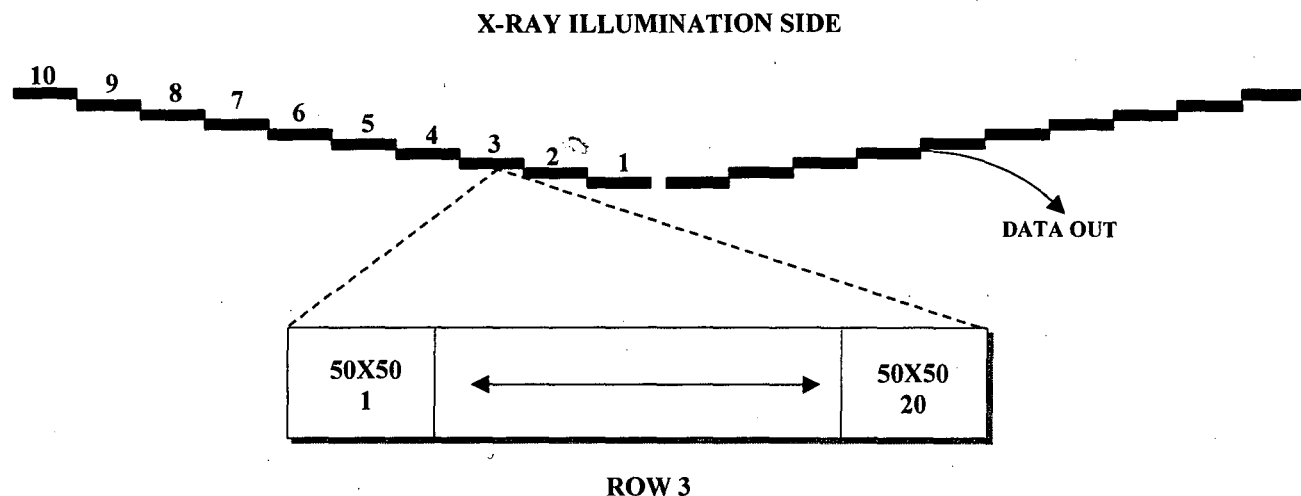
**X-RAY ILLUMINATION SIDE**



Figure 12.0. (15x15) cm$^2$ detector module consisting of two 10 rows of 20, (50x50) detector modules. Signal connections are made through the back side of the detector housing.

## VIII. CONCLUSION

The ASIC now includes the pixel processor, the column logic and the serial end-of-column logic. Initial test show that the logic operates in an independent manner without interfering with neighboring columns in the ASIC. With the complete system operational, detectors of 300 µm and 500 µm thickness shall be hybridized and a full characterization will occur. The ASIC layout is such that multiple modules can now be made to form a planer mosaic of four (16x16) arrays or 1024 pixels. The histogram memory is presently being up graded to a dual port version. Once the systems modifications have been completed, the multi-module will be characterized at the Advanced Light Source (ALS). Results from these measurements will be utilized in the final 50x50 ASIC design.

## IIX. REFERENCES

[1] Proceedings of the 17th International Union of Crystallography Congress, Seattle Washington, August 1996, Abstract MS01.04.04, pp. C20.

[2] "The Column Architecture - a Novel Architecture for Event Driven 2D Pixel Imagers", J.Millaud and D. Nygren, IEEE Transactions on Nuclear Science, June 1996, Vol. 43, No. 3, pp. 1243.

[3] S.L. Barna, *et. al.*, "Characterization of a Prototype Pixel Array Detector (PAD) for Use in Microsecond Framing Time-Resolved X-Ray Diffraction Studies", IEEE Transactions on Nuclear Science, Vol. 44, No. 3, June 1997.

[4] "Status of the Digital Pixel Array Detector for Protein Crystallography", P.Datte, et al., Nuclear Instrumentation and Methods in Physics Research, A 421 (1999) pp.576-590.

[5] "A 2D Smart Pixel Detector for Time Resolved Crystallography", E. Beuville, et al., IEEE Transactions on Nuclear Science, June 1996, Vol. 43, No. 3, pp. 1243.

[6] "Two-dimensional Pixel Array Image Sensor for Protein Crystallography", Eric Beuville, et al. Proceeding of SPIE (Denver, CO) August 7-8 1996, Volume 2859, pp. 85-92.

[7] "A 2D Pixel Array Image Sensor for Protein Crystallography", E. Beuville, et al. Proceedings of the Nuclear Science Symposium and Medical Imaging Conference, October 21-28 1995 San Francisco.

ERNEST ORLANDO LAWRENCE BERKELEY NATIONAL LABORATORY
ONE CYCLOTRON ROAD | BERKELEY, CALIFORNIA 94720