Title

A SOLID-STATE CHRONOTRON FOR DIGITIZING TIME DELAYS

Authors

Bjerke, Arthur E.
Kerns, Quentin A.
Nunamaker, Thomas A.

Publication Date

1960-12-12

UCRL-9270

UNIVERSITY OF CALIFORNIA

Ernest O. Lawrence Radiation Laboratory

BERKELEY, CALIFORNIA

DISCLAIMER

UCRL-9270
Limited Distribution

UNIVERSITY OF CALIFORNIA

Lawrence Radiation Laboratory
Berkeley, California

Contract No. W-7405-eng-48

A SOLID-STATE CHRONOTRON FOR DIGITIZING TIME DELAYS

Arthur E. Bjerke, Quentin A. Kerns, and Thomas A. Nunamaker

December 12, 1960

A SOLID-STATE CHRONOTRON FOR DIGITIZING TIME DELAYS

Arthur E. Bjerke, Quentin A. Kerns, and Thomas A. Nunamaker

Lawrence Radiation Laboratory
University of California
Berkeley, California

December 12, 1960

ABSTRACT

This solid-state chronotron measures the relative time delay between two shaped photomultiplier pulses, and quantizes this time delay into seven time intervals with widths of 3 to 7 nsec. These intervals represent the difference in time of flight of two particles in a large scattering experiment, and may be varied at will by changing front panel cables. The quantized time delay is then stored in a buffer storage until readout, at which time the system is recycled. Because the chronotron was used with a system having a 40-μsec cycle time, a maximum repetition rate of 100 kc was selected. However, this rate could be increased considerably if necessary.

The time intervals are formed by splitting the two shaped photomultiplier signals into parallel diode coincidence circuits, with the time delay of each coincidence circuit set for the center of its respective time interval. Since the coincidence circuits are identical, both the position and width of each time interval determined only by the delay cables. Thus the coincidence circuit with the greatest output voltage indicates the correct time interval. To detect this voltage the stretched output of each coincidence circuit has a common ramp voltage added to it, and together these signals begin driving a bank of blocking oscillators. As soon as one blocking oscillator triggers, all others are disabled and the blocking oscillator that triggered sets up its binary

coded number in the buffer storage. As the ramp generator always insures that one blocking oscillator triggers there is never a hole between time intervals, even if the edges of the intervals drift, because when one interval expands its neighbors will contract.

Long-term stability of the time interval centers is a few tenths of a nanosecond, and the 24-hr stability of the edges of the intervals is ±0.5 nsec. With the aid of a TV monitor used in checking the system, the chronotron can be held within the above limits indefinitely by simple daily adjustments.

A SOLID-STATE CHRONOTRON FOR DIGITIZING TIME DELAYS*

Arthur E. Bjerke, Quentin A. Kerns, and Thomas A. Nunamaker

Lawrence Radiation Laboratory
University of California
Berkeley, California

December 12, 1960

I. INTRODUCTION

The solid-state chronotron described here is designed to measure the time interval between two photomultiplier signals.[1] This interval represents the difference in time of flight of pions and neutrons in a large scattering experiment.[2]

The chronotron quantizes time into seven time intervals which vary in duration from 2.9 to 7.3 nsec, as shown in Fig. 1. It also stores the binary-coded numbers of the time intervals in a flip-flop buffer storage. For the time measurement described here, all phototube signals could have been superimposed onto two signal lines. However, because of the noise contribution of the large number of photomultipliers used in the experiment, it was felt safer to employ four separate chronotron channels.

Since all the chrontrons are identical, this discussion will be limited to only one unit. Figure 2 is a block diagram of the chronotron; Fig. 3 shows the sampling and detection circuits. Figure 4 shows all four chronotrons mounted together, along with their monitoring and power-supply panels. An individual chronotron is also shown in Figs. 5 and 6. A provision for monitoring has been used with the chronotron, and has proven very

*This work was done under the auspices of the U.S. Atomic Energy Commission.

necessary.[3] With the amount of equipment used, monitoring is needed in setting up the equipment initially as well as in checking each channel once the equipment is operating.

The time intervals are formed by splitting the two photomultiplier signals (called π for pion, and N for neutron) into parallel diode coincidence circuits, with the time delay of each circuit set for the center of its respective time interval. Since the coincidence circuits are identical, both the position and width of each time interval are determined only by the delay cables associated with that channel. Thus the coincidence circuit with the greatest output voltage indicates the correct time interval. In order to detect this, the stretched output of each coincidence circuit has a common ramp voltage added to it, and together these signals drive a bank of blocking oscillators. As soon as one blocking oscillator triggers, all others are disabled, and the blocking oscillator that triggered sets up its channel number in the flip-flop buffer storage. Because the ramp generator always insures that one blocking oscillator triggers, there is never a hole between time intervals even if the edges of the intervals drift; when one interval expands, its neighbors contract. If the ramp generator is not started, none of the blocking oscillators triggers, since the outputs of the coincidence circuits alone are less than the blocking-oscillator bias. If the ramp generator is fired in the absence of N and π signals, the most sensitive blocking oscillator will fire. For this reason, the end blocking oscillator--numbers 1 and 9--are made slightly more sensitive than the others. Thus if the ramp is started in the absence of any signal, a zero is read out.

Long-term stability of the time-interval centers is a few tenths nanosecond, and the 24-hr stability of the edges of the intervals is ± 0.5 nsec.

With the aid of a raster-type cathode-ray-tube display used in checking the system,[3] the chronotron can be held within the above limits indefinitely by simple daily adjustments.

II. CIRCUIT OPERATION

The N and π phototube signals are amplified and shaped by Hewlett-Packard 460A and B distributed amplifiers. The shaped pulses have symmeterical wave shapes with a half width of about 6 nsec and very little amplitude fluctuation. The output of the π amplifying and shaping circuits is fed into a splitting transformer where it is split into nine identical outputs. These outputs are then delayed relative to one another by the center-to-center time separation of each chronotron interval. The delay cables are made accessible from the front panel to facilitate changing the width of the time intervals. Nine channels are necessary to form seven time boxes, the extra two channels being necessary to give good time definition to the beginning of the first time box and the end of the seventh time box. After being delayed, the π signal passes through an adding transformer (T2 of Fig. 3), where the N signal is added. The sum of these two signals is then applied to a Qutronics Q6-100 diode that samples the pulse through a sampling capacitance C1 of Fig. 3), thus leaving a charge on the sampling capacitor that is proportional to the sum of the two signals. The channel with the largest sampled charge corresponds to the best coincidence, and thus represents the correct time interval. To detect this channel, a bank of identically biased blocking oscillators is driven toward firing by a ramp voltage applied to the low side of the sampling capacitor(C1). The channel with the largest signal triggers its blocking oscillator first and disables all other blocking oscillators before they can trigger. This disabling is accomplished mainly by coupling all the

the blocking-oscillator emitters through a common-emitter transformer (T3 of Fig. 3). Therefore the firing of any one increases the reverse cut-off bias on the other blocking oscillators, thus preventing them from triggering.

The ramp is turned off by a stop signal taken from the common-emitter transformer (T3) of the blocking oscillator. This signal also starts an erase circuit that discharges each sampling capacitor, with a 10-μamp discharge current lasting for 10 μsec.

The decimal outputs of the blocking oscillators are fed through a diode matrix to a flip-flop buffer storage. Here the channel number is stored in binary form and is eventually read into the core storage. Alternatively, the blocking-oscillator outputs may be connected to the throw-away amplifier, which immediately resets the whole system.

III. SPLITTING AND ADDING TRANSFORMERS

The splitting transformer (T1) for the π signal has a 50-ohm input impedance and a 5.6-ohm output impedance (i.e., nine parallel 50-ohm Sub-Minax coaxial outputs). The transformer has a bifilar winding on a Ferroxcube type-102 core. There are four parallel primary windings and eight parallel secondary windings. Parallel windings are used in order to reduce the leakage inductance of the transformer. The measured rise time of this transformer is 1.2 nsec.

The π and N signals are added by means of the adding transformer (T2) placed as close as physically possible to the sampling diodes. The N signal is brought in on a 50-ohm coaxial cable and connected to a 6-turn winding on the type-102 core. The nine 50-ohm coaxial cables which contain the delayed π signals are bundled together and wound with two turns on the core. Each cable is terminated in a 51-ohm resistor, and its center conductor fastened to the Q6-100 sampling diode (D1 in Fig. 3). The shields of these nine cables are tied together on the sampling-diode side of the core and grounded through a 5.6-ohm resistor. This resistor terminates the incoming N signal, which then appears across the outer conductor of the * cables and ground. The signal at the input of the sampling diodes (D1) to ground is the sum of the π and N signals.

IV. SAMPLING CIRCUIT AND BUFFER AMPLIFIER

The sampling diodes are selected to insure that all nine circuits have similar sampling characteristics. First the diodes are selected for a reverse impedance of at least 1 meg, which gives leakage currents (Id) of 1 μamp or less. Next the junction capacitance (Cd) and the forward conductance are measured. From this data, nine similar diodes are selected for each chronotron. The C/I decay time constant of the sampling circuits must be kept large with respect to the time necessary to trigger a blocking oscillator. (Here C, the total sampling capacitance, is equal to C1 plus Cd and the input capacitance of the emitter follower. The total leakage current, I, is due to the reverse leakage of the sampling diode, Id, plus the base current of the emitter follower, Ib.) With the circuit used, the decay-time constant was of the order of 16 μsec. To keep this time-constant high the base current (Ib) of the 2N501 emitter followers is kept to less than 2 μamp by using high-beta transistors with low collector leakage current. The nine emitter-follower transistors for each chronotron are selected to have similar base currents, thus keeping all delay time constants similar. The final adjustment of the delay time constant is made by trimming the sampling capacitance (C1). The process of selection described here may seem overly restrictive, but we have found that the number of rejected components has been very small, because components that cannot be used in one part of the circuit usually can be used in another part of the circuit.

V. BLOCKING OSCILLATORS

The blocking oscillators (see Fig. 3) are biased in a cut-off condition, and their emitters are all coupled together through the emitter-coupling transformer (T3). When the ramp is applied, all blocking oscillators are driven toward conduction; the channel with the largest signal will trigger its blocking oscillator first. As soon as the first blocking oscillator triggers all others are prevented from triggering by the action of emitter-coupling transformer (T3), which increases the cut-off bias of all the other blocking oscillators as soon as any one has triggered . A stop signal is taken from the emitter-coupling transformer, which immediately reverses the ramp (this further insures that no other blocking oscillators will fire). In addition, the blocking oscillators have a common power supply to the collector (i.e., the simple RC network shown in Fig. 3) which stores only enough charge to support the firing of one blocking oscillator. By using these various precautions we have obviated trouble from double firing.

The blocking-oscillator transformer (T4) is wound bifilar on a type-102 Ferroxcube core, with a three-turn base winding, a 12-turn collector winding, and a six-turn output winding. The emitter-coupling transformer (T3) is also on a type-102 core. The blocking oscillator works into an impedance of about 50 ohms through this transformer. Type-2N501 transistors are used for the blocking oscillator and are selected for a minimum beta of 30. We have found that the majority of the transistors that can not be used in the emitter follower can be used as blocking-oscillator transistors. The firing voltage of the blocking oscillators was made adjustable by means of a varying dc potential at the ground side of the emitter coupling transformer (T3). Rise time of the blocking oscillator was 12 nsec, and the equivalent noise referred to the base of the transistors was 1.5 mv.

VI. READOUT AND CONTROL CIRCUITS

The outputs of the blocking oscillators are fed directly to a diode matrix with a binary 1, 2, 4 readout. The diode matrix drives a bank of three flip-flops that serve as the buffer storage between the chronotron and the core storage of the system.[4] Once the core storage has accepted the output of the chronotron, a reset signal is generated which resets the chronotron flip-flops. At this point the chronotron is ready to accept a new input.

The chronotron ramp signal is normally initiated by an external search command. When this command is not available, the chronotron may be started directly from the N signal by taking this signal from the adding transformer T2.

VII. OPERATING HISTORY

Four chronotrons were built and installed to measure time of flight in a large scattering experiment.[2] The time intervals for this experiment ranged from 3 to 7 nsec and are shown in detail in Fig. 1. A raster-type cathode-ray-tube display was used to monitor the chronotron intervals during the experimental dead time;[3] in operation with the Bevatron, monitoring was almost continuous.

During the experiment, the 24-hr stability of the edges of the time intervals was within ±0.5 nsec. To correct for this shift, the chronotron was adjusted daily, thereby operating within these limits during the entire experiment. Short-term stability of the time intervals was within a few tenths of a nanosecond.

ACKNOWLEDGMENTS

Many thanks are due the people who helped make this chronotron possible. In particular Mr. Robert F. Reynolds handled the mechanical design and construction. Messrs. Lee J. Wagner, William S. Flood, and E. Thomas Clark, contributed their time and ideas.

REFERENCES

1. I. A. D. Lewis and F. H. Wells, "The Chronotron Timing Unit," in Millimicrosecond Pulse Techniques (McGraw-Hill Publishing Co., New York, N. Y., 1954), pp. 269-271.

2. S. C. Baker, F. A. Kirsten, D. A. Mack, and C. Wiegand, Lawrence Radiation Laboratory Report UCRL-9271, December 1960.

3. S. C. Baker, Q. A. Kerns, F. A. Kirsten, D. A. Mack, and T. A. Nunamaker, Lawrence Radiation Laboratory Report UCRL-9273, December 1960.

4. Frank Evans and Frederick A. Kirsten, Lawrence Radiation Laboratory Report UCRL-9274, December 1960.

FIGURE LEGENDS

Fig. 1. Chronotron time-interval distribution.

Fig. 2. Chronotron block diagram.

Fig. 3. Chronotron sampling and blocking-oscillator circuits.

Fig. 4. Chronotron rack showing four chronotrons.

Fig. 5. Front view of two chronotrons showing one unit with delay cables and another without.

Fig. 6. Top view of chronotron.

Interval								
1	2	3	4	5	6	7	8	9
Zero output	2.9 nsec	3.3 nsec	3.9 nsec	4.6 nsec	4.8 nsec	6.8 nsec	7.3 nsec	Zero output

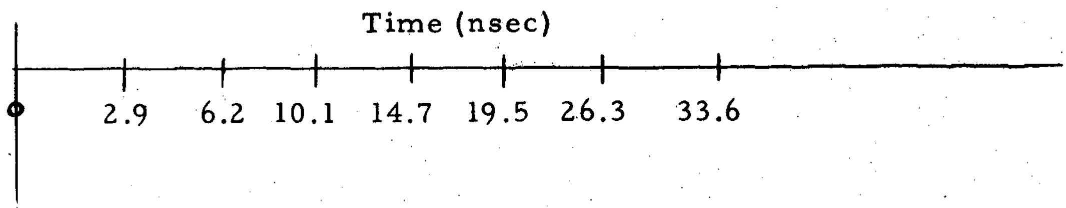


Fig. 1. Chronotron time-interval distribution.

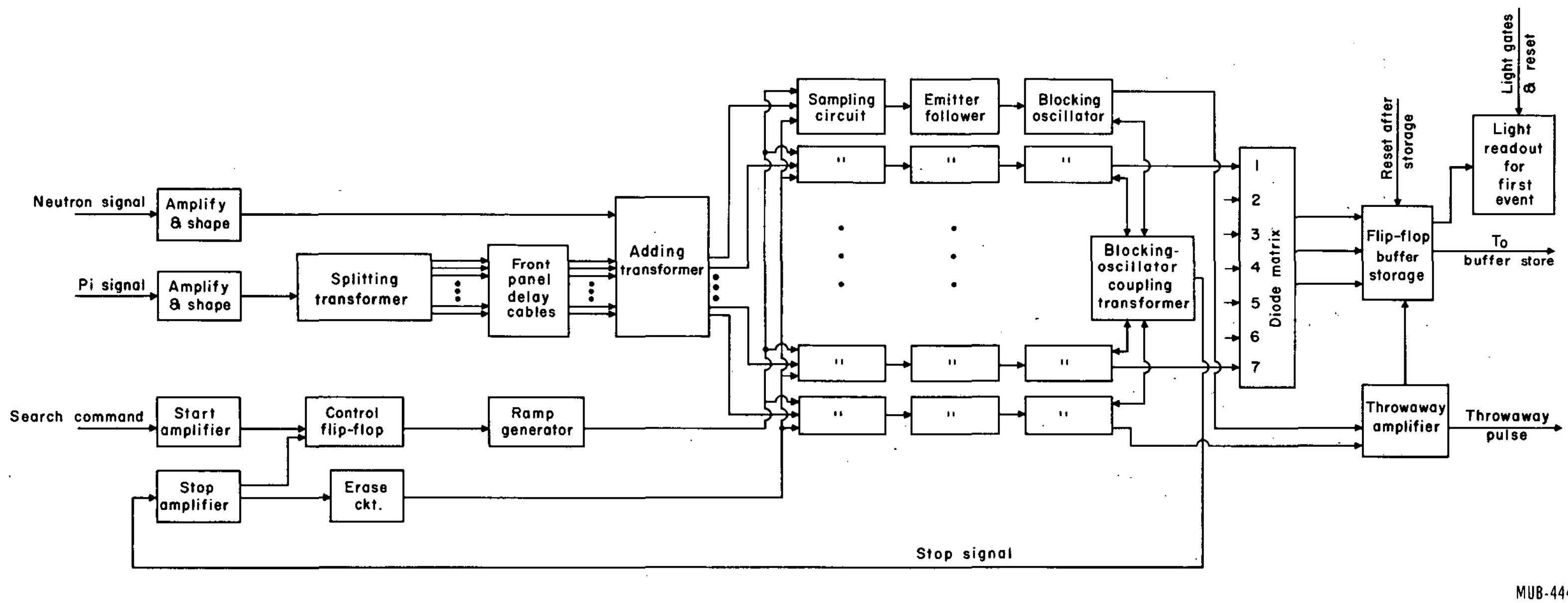

Neutron signal
Amplify & shape
Pi signal
Amplify & shape
Splitting transformer
Front panel delay cables
Adding transformer
Sampling circuit
Emitter follower
Blocking oscillator
Blocking-oscillator coupling transformer
Diode matrix
1
2
3
4
5
6
7
Reset after storage
Flip-flop buffer storage
Light gates & reset
Light readout for first event
To buffer store
Search command
Start amplifier
Control flip-flop
Ramp generator
Stop amplifier
Erase ckt.
Throwaway amplifier
Throwaway pulse
Stop signal
MUB-444

Fig. 2.

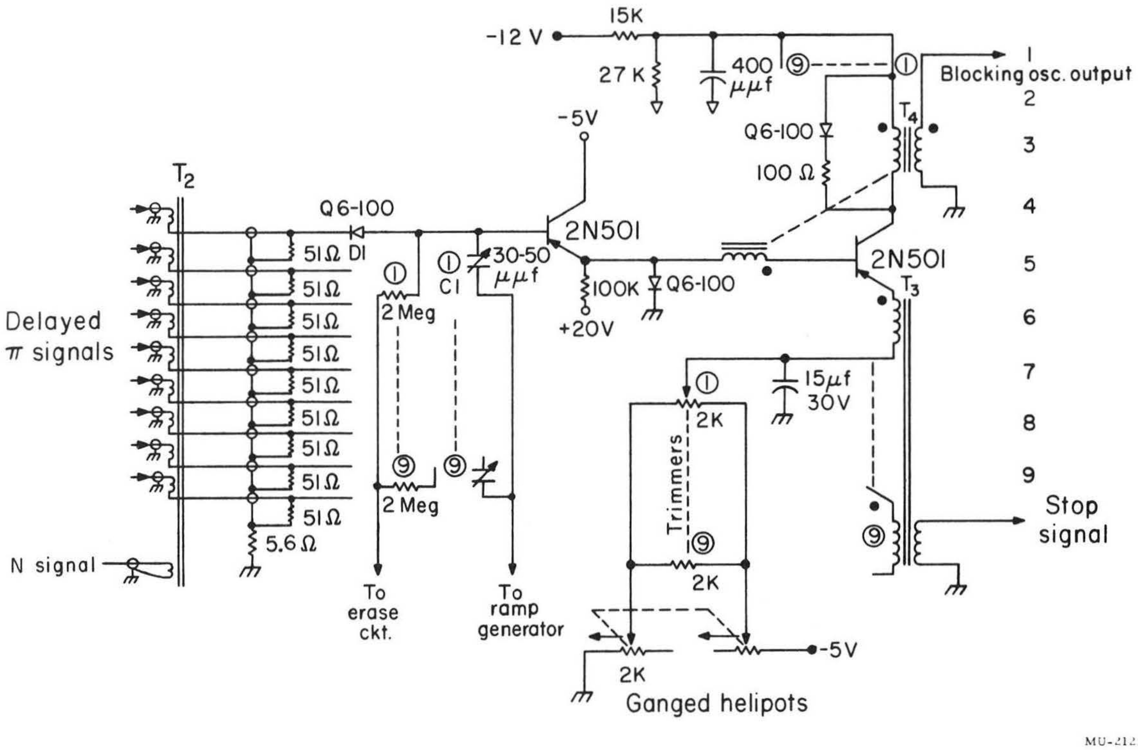
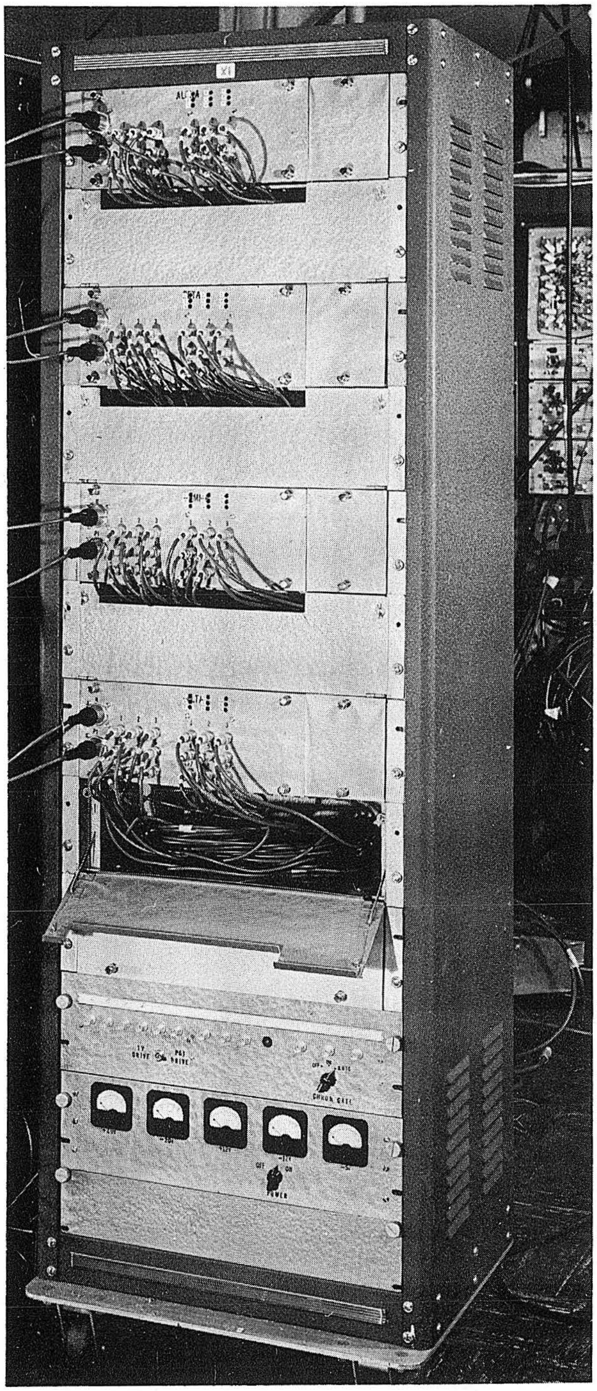
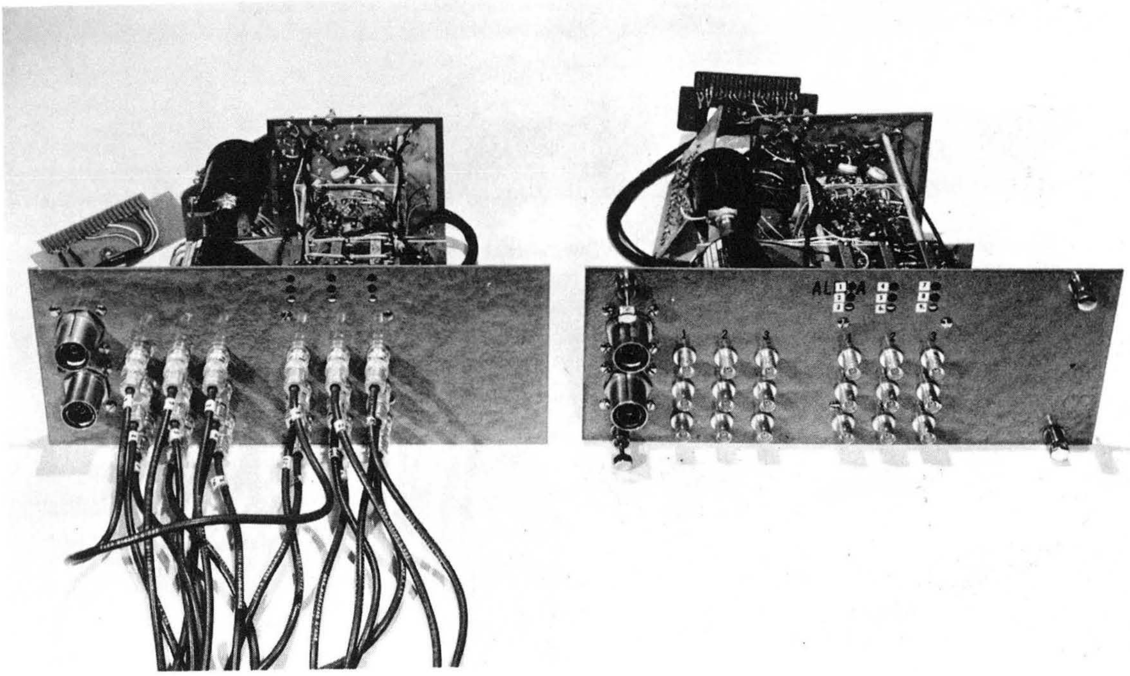

-12 V
15K
27 K
400 μμf
-5V
Q6-100
100 Ω
Blocking osc. output
T4
1
2
3
4
5
6
7
8
9
T2
Q6-100
D1
2N501
51 Ω
C1
30-50 μμf
2 Meg
100K
Q6-100
+20V
2N501
T3
Delayed π signals
15μf 30V
2K
Trimmers
2 Meg
5.6 Ω
N signal
Stop signal
2K
To erase ckt.
To ramp generator
2K
-5V
Ganged helipots
MU-21212

Fig. 3.



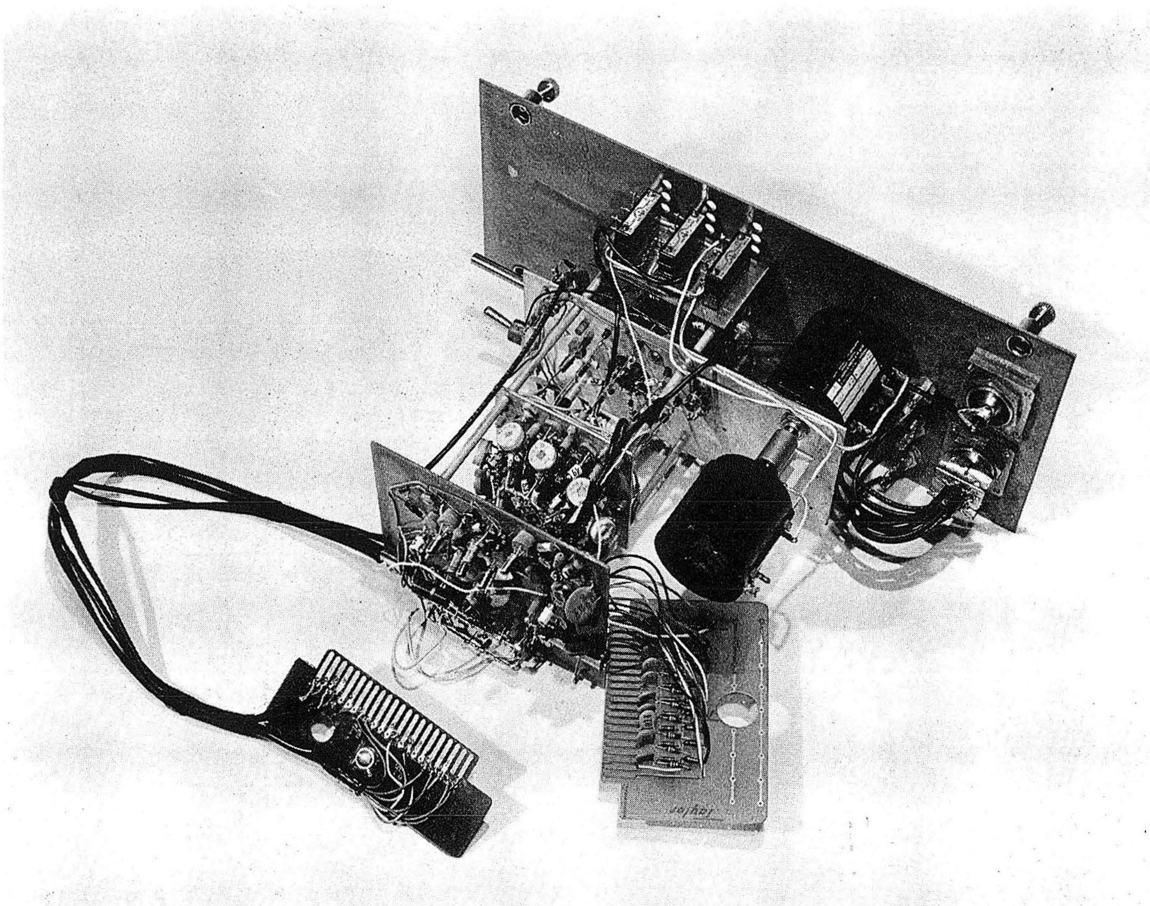
ZN-2631

Fig. 4.



ZN-2632

Fig. 5.



ZN-2633

Fig. 6.