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Split-Phase and Multi-Resonant Operation of Hybrid Switched-Capacitor Converters

By

Rose Antoinette Abramson

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Professor Robert C.N. Pilawa-Podgurski, Chair
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Abstract

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Professor Robert C.N. Pilawa-Podgurski, Chair

Hybrid switched-capacitor (SC) converters have seen increased use in applications that demand both high efficiency and high power density. These converters exhibit the traditional benefits of pure SC converters, such as efficient utilization of switches and the use of energy-dense capacitors, along with lossless capacitor charge transfer due to the use of one or more augmenting inductors. Increased performance can also be obtained by using more complex control schemes than the traditional two-phase control common with pure switched-capacitor converters.

Split-phase control, one such modified control scheme, is used to ensure full soft-charging of all flying capacitors in several hybrid switched-capacitor topologies belonging to the Dickson-derived class of converters. Here, capacitors are inserted into the switch-capacitor network in a staggered manner to ensure that they do not over- or under-charge in each phase, which would result in lossy hard-charging transitions. However, the time at which to insert these capacitors can change based on operating condition, component tolerance, and phase-ordering. This work will present an analysis of these effects, as well as describe specific control schemes and active-tuning methods that can ensure full soft-charging operation.

In addition, other control schemes such as multi-resonant operation, can be utilized to achieve high-performance designs. Multi-resonant hybrid switched-capacitor converters operate with multiple operating phases per switching period, and can achieve the same conversion ratio as standard two-phase hybrid switched-capacitor converters with a fewer number of switches and capacitors, allowing for higher efficiency and power density design. One such topology, the cascaded series-parallel (CaSP) converter, will be analyzed, and several high-performance hardware prototypes designed for 48 V data center dc-dc power delivery will be presented.

To Kai
for all the loving years gone by and all those yet to come

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Chapter 1

Introduction

1.1 Introduction

Hybrid switched-capacitor (SC) converters have seen increased use in applications that demand both high efficiency and high power density. These converters exhibit the traditional benefits of pure SC converters, such as efficient utilization of switches [1] and the use of energy-dense capacitors [2], along with lossless capacitor charge transfer due to the use of one or more augmenting inductors [3–6]. Hybrid SC topologies have become more popular in application spaces such as automotive drive-trains [7–11] and 48 V-bus data center power delivery [12, 13], including both single-stage and two-stage architectures.

For this latter application area, hybrid SC converters are especially well-suited for use as first-stage intermediate bus converters (IBCs). These IBCs step the 48 V bus down to some intermediate voltage, which is then stepped down to the low-voltages and high-currents seen at the point-of-load (PoL). By using a two-stage architecture, the first stage often does not need to satisfy stringent transient requirements or provide regulation, allowing for the use of dc transformer (DCX) topologies. In addition, as hybrid SC converters can achieve high step-down conversion without significant degradation to efficiency or power density, there is an opportunity to decrease the input voltage of the second-stage PoL converters from the more conventional 12 V bus to a lower (i.e. 4 to 8 V) voltage, to allow for increased PoL-stage efficiency [14–16]. There has been an increased interest in these higher step-down options for the first-stage IBCs, as can be seen by the following surveys analyzing performance trends across industry and academic intermediate bus converters.

Fig. 1.1 shows the power density in W/in^3 plotted against year-of-release for a variety of industry and academic offerings. As expected, there is a large amount of 4-to-1 IBC options overall (both regulated and unregulated), as these are used to provide the 12 V bus commonly used in two-stage data center power delivery designs. However, in the past five or so years, several higher step-down options have been released, initially primarily from academia. The 8-to-1 multi-resonant doubler (MRD) converter [17], and the 6-to-1 and 8-to-1 variants of the cascaded series-parallel converter (CaSP) [18, 19] were some of the earlier

offerings in these higher conversion-ratios, and achieved state-of-the-art performance at the time of publishing. The CaSP hardware prototypes shown here will also be explored in more detail in Chapter 7. Another trend that can be seen from this survey is the increase in power density over time. This has been primarily driven by an increase in output current capability for many of these IBC implementations.

Fig. 1.2 shows the power density (W/in^3) and peak efficiency (%) for the same grouping of industry and academic IBCs. As expected, unregulated 4-to-1 step-down converters have some of the best combined power densities and efficiencies, due to their lower conversion-ratios and the fact that they do not need to size their inductors for regulation. However, many 6-to-1 and 8-to-1 implementations (including the CaSP prototypes discussed in this thesis) can still obtain high performance.

In addition, it is important to note that while data center power delivery is a very well-suited use-case of hybrid SC converters in general, the analysis and design techniques detailed in this work have direct application to any high-performance, high-conversion ratio application.

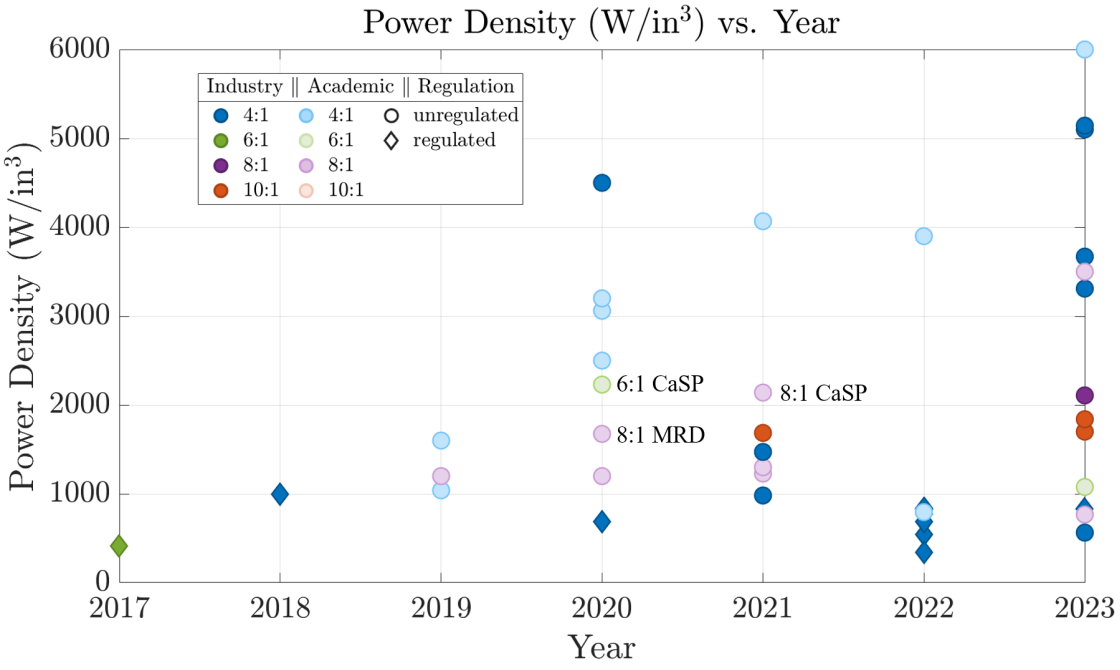


Figure 1.1: Power density versus year-of-release, for a survey of 48 V / 54 V intermediate bus converters for data center applications. Converters are categorized by conversion ratio, regulation capability, and whether the work is academic or commercial.

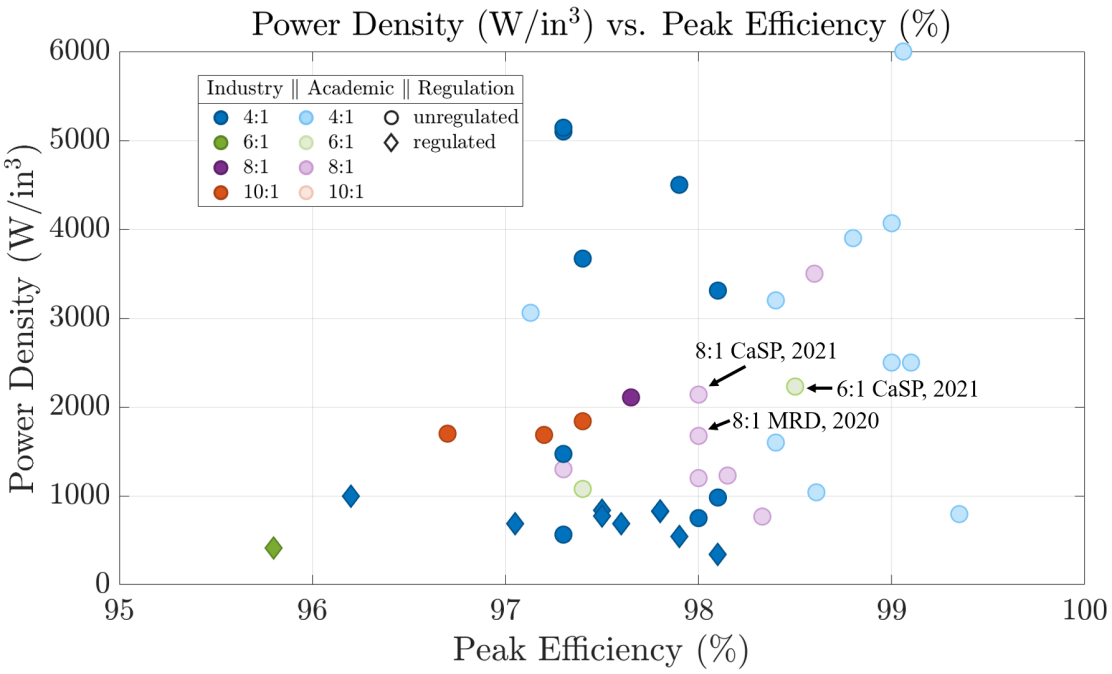


Figure 1.2: Power density versus peak efficiency, for a survey of 48 V / 54 V intermediate bus converters for data center applications. Converters are categorized by conversion ratio, regulation capability, and whether the work is academic or commercial.

1.2 Organization of Thesis

Throughout this work, we will we explore general hybrid SC design and analysis methods, as well as operating techniques (such as split-phase switching and multi-resonant operation) that can be used to achieve higher performance than would be obtained using conventional two-phase operation. This thesis is organized as follows.

Chapter 2: Soft-Charging of Hybrid Switched-Capacitor Converters

This chapter presents an overview of the concept of soft-charging, in which the capacitor charge and discharge losses inherently present in pure switched-capacitor converters can be mitigated by the use of an inductive or controlled-current load. Fundamental analysis techniques to determine the soft-charging capability of different switched-capacitor topologies are also presented, including new extensions to topologies with multiple inductors and multiple operating phases.

Chapter 3: Split-Phase Switching Overview

The Dickson converter is a popular hybrid SC topology that can achieve very good switch stress performance. However, many variants cannot achieve soft-charging without modifications to the standard two-phase operation. Split-phase switching is a technique used to softly charge the flying capacitors, wherein additional operating phases are introduced which charge and discharge the flying capacitors in a staggered manner. Here, we illustrate the inherent reason for the hard-charging present in these types of converters, as well as the mechanism by which split-phase switching mitigates these capacitor charge and discharge losses.

Chapter 4: Effects of Split-Phase Sub-Phase Ordering

The exact implementation of split-phase control can be nuanced, depending on the specific ordering of these introduced sub-phases. This chapter details the effects of different split-phase ordering patterns on split-phase switch blocking voltage, overall switch stress, and sub-phase timings. General trends and rules of thumb are also provided for both step-up and step-down Dickson-variant converter topologies.

Chapter 5: Active Splitphase Control Using Capacitor Voltage Discontinuity Detection

Due to the complex interaction of converter dynamics, parasitics, and component tolerances in a real hardware implementation, calculating precise split-phase timings can be nontrivial. This chapter therefore presents an active tuning method to automatically detect the presence of hard-charging events, which indicate incorrect split-phase timings for the given operating condition. The control then increases or decreases these split-phase timings in such a way as to restore the converter back to a soft-charging state. The technique as presented is general in nature, and can be applied to a variety of Dickson-derived topologies, switching both at and above the natural resonant frequency of the converter. In addition, the technique can be used to detect component tolerance mismatch in non-Dickson converter topologies, as will be explored more in Chapter 7.

Chapter 6: Passive Volume Analysis Using Peak Energy Storage Requirements

The volume of the passives in a hybrid SC converter can represent a large fraction of the overall converter volume. Therefore, in order to increase power density and minimize footprint, it can be desirable to shrink the passive volume as much as possible. This chapter details an analytical framework for comparing multiple hybrid SC topologies on the basis of peak energy storage for each passive component. This peak energy storage requirement is then converted into a passive volume, using empirical trends for capacitor and inductor energy densities. This chapter also presents a new extension to the analysis technique, which allows

for the inclusion of multi-resonant hybrid SC topologies such as the multi-resonant-doubler (MRD) and cascaded series-parallel (CaSP) converters.

Chapter 7: The Cascaded Series-Parallel (CaSP) Converter

The cascaded series-parallel (CaSP) converter is a multi-resonant hybrid SC topology that can achieve the same conversion ratio as conventional two-phase hybrid SC converters with a significantly reduced component count. This can lead to greatly improved power density and efficiency. This chapter presents the general theory of operation for the CaSP converter, as well as an example application of the soft-charging analysis presented in Chapter 2 and the passive volume analysis presented in Chapter 6. Two high-performance hardware prototypes designed for data center applications are also presented, which are capable of 6-to-1 and 8-to-1 step-down conversion, respectively. Finally, a "split-phase" control scheme for handling capacitance mismatch in the CaSP converter is introduced and validated in hardware.

Chapter 8: Conclusion

This chapter concludes the thesis, and presents possible extensions to split-phase and multi-resonant operation of hybrid SC capacitor converters. This chapter also summarizes the overall contributions of this work.

Chapter 2

Soft-Charging of Hybrid Switched-Capacitor Converters

2.1 Introduction

While pure switched-capacitor (SC) converters can achieve high power density due to their use of energy dense capacitors [2, 20], their performance has been limited in higher power applications due to the inherent capacitor charge sharing losses. Pure SC converters can experience large transient currents spikes when they switch from one circuit state to another during the switching cycle, termed "hard-charging". These current spikes result from pulsed charge redistribution as the capacitors are disconnected from one network and reconnected into another, and can lead to increased losses, increased device stress, and worsened electromagnetic interference (EMI) performance. Reducing these effects in pure switched-capacitor converters requires either increasing the switching frequency or increasing the capacitance – both of which reduce the voltage ripple on the capacitors. However, the first modification can result in increased switching losses, while the later can result in reduced power density. Fig. 2.1 shows an example 2-to-1 SC converter, which would see large transient inrush current in the capacitor, C_1.

The undesirable effects of hard-charging can be mitigated by adding an inductor or controlled current load in the charge and discharge path of the capacitors (illustrated in Fig. 2.2a and Fig. 2.2b, respectively), as first demonstrated in [3]. In doing so, the capacitors will experience resonant or constant currents, rather than the large transient spikes that lead to hard-charging losses. The converter can therefore "soft-charge" its flying capacitors. The addition of this inductor or current load is referred to as "hybridizing" a SC converter, and the resulting topology is termed a hybrid switched-capacitor (SC) converter.

However, the placement of these inductive elements can require significant analysis to ensure that their addition results in the full soft-charging of all flying capacitors. Furthermore, many topologies require specific ratios of capacitances to ensure that there are no capacitor voltage mismatches when the converter transitions from one operating phase configuration

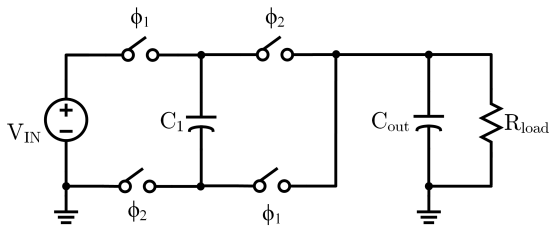


Figure 2.1: Example pure SC converter, showing a 2-to-1 conversion ratio.

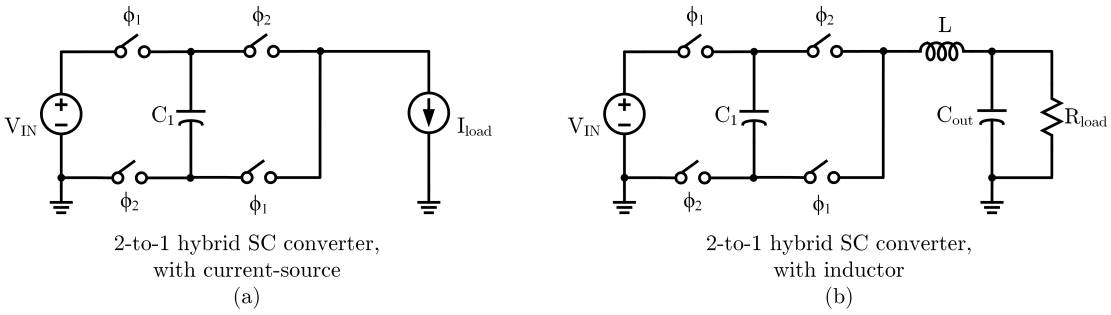


Figure 2.2: Example hybridized SC converter, showing a 2-to-1 conversion ratio. (a) shows hybridization with a controlled-current source load, and (b) shows hybridization with an inductor.

to another. Both of these considerations must be taken into account when analyzing how a pure SC converter can be successfully hybridized. The following sections will detail prior analysis techniques that can be used for this purpose, as well as present new extensions to this method designed to handle a broader range of hybrid SC topologies.

2.1.1 Output Impedance

Throughout this and other chapters, we will refer to the output impedance of a hybrid SC converter as a proxy for loss or efficiency performance. Here, we briefly introduce how this impedance is characterized. Both pure SC and hybrid SC converters can be modeled using the circuit shown in Fig. 2.3. The N:1 transformer models the fixed-ratio N:1 conversion of a general SC converter, while the output impedance, R_{out}, models the loss in the converter. The output impedance curves for both a pure SC converter and a hybrid SC converter are shown in Fig. 2.4. General equations for these curves can be found in [6]. The slow-switching limit (SSL)—where losses are dominated by capacitor charing sharing losses—and the fast-switching limit (FSL)—where losses are dominated by parasitics in the circuit such as switch

ON-state resistance, capacitor ESR, or inductor DCR—are also labeled, as described by [1]. The hybrid SC converter is able to achieve the FSL output impedance at a much lower frequency than the pure SC converter, near the hybrid SC converter's resonant frequency.

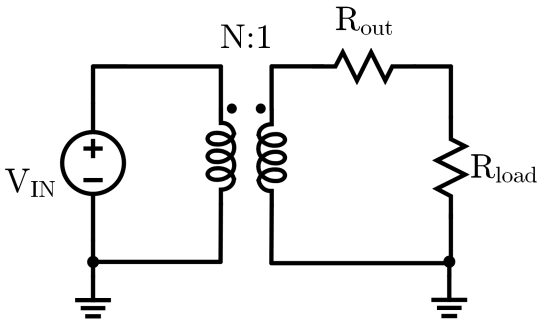


Figure 2.3: Switch-capacitor converter model, using an N:1 transformer to model the N:1 fixed-ratio conversion, and some output impedance, R_{out}, to model loss.

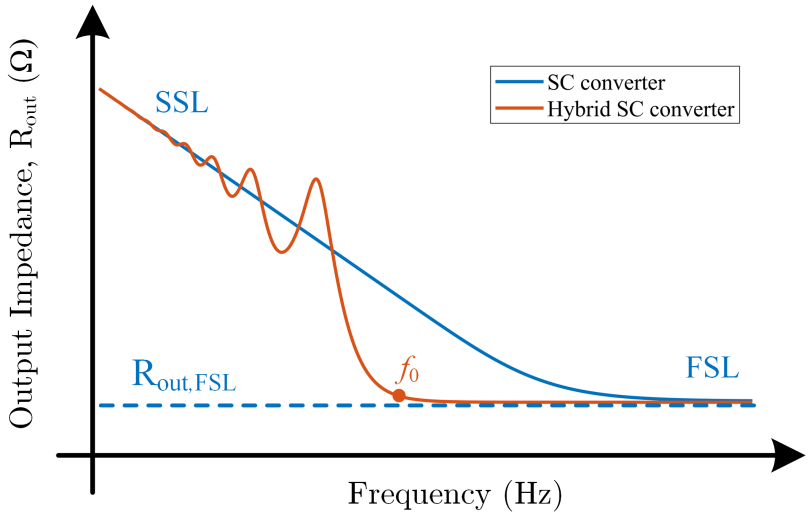


Figure 2.4: Output impedance, R_{out}, versus frequency for a pure SC converter and a hybrid SC converter.

2.2 Analyzing Arbitrary Switched-Capacitor Topologies for Soft-Charging Capability

In order to determine which conventional SC converters could be converted to soft-charging hybrid SC converters with more generality, a vector-based algorithmic approach was pub-

lished in [5]. This approach uses topology-specific Kirchhoff's voltage law (KVL) and capacitor charge-balance relationships to build a system of equations that can be solved for capacitance values that will result in full soft-charging of all flying capacitors. However, this analysis was restricted in the following manner [5]:

1. Converters were all evaluated for soft-charging based on hybridization with a *single* inductor at the *low-side* port (referred to as the output node in [5]). Converters with multiple inductors, or with inductors not directly connected to the low-side node, were not considered.

2. Only converters with two operating phases per switching period were considered. Multi-resonant converters, such as the multi-resonant-doubler (MRD) [17] and the cascaded series-parallel (CaSP) [18, 19] converters, are not directly analyzable using the method as presented.

While many converters falling into the above categories have since been analyzed for soft-charging capability by techniques such as those in [21–25], they have still not been treated using this more algorithmic approach. By adjusting the way we set up this system of equations, we can extend this analysis to a wider set of hybridized SC converters. In the next section, we will first present an overview of the method as presented in [5], before describing how it can be adapted to handle multiple inductors and multiple operating phases. In Section 2.4 - Section 2.6, we will demonstrate the adapted method for the following converters, with each serving as an exemplar topology exhibiting one of these new characteristics.

- **Multiple Inductors at the Low-Side Port**
  - 5-to-1 Dual Inductor Hybrid (DIH) Converter
  - 3-to-1 Symmetric Dual Inductor Hybrid (SDIH) Converter
- **Multiple Inductors with Tank Configuration**
  - 5-to-1 LC Dual Extended Tank Converter
- **Multiple Operating Phases (> 2)**
  - N-to-1 Cascaded Series-Parallel (CaSP) Converter, detailed further in Chapter 7

2.3 General Overview of the Nullspace Method

The overall soft-charging analysis examines the charge flow through input/output sources and capacitors in the converter, and determines the required change in capacitor voltage, Δv, in each phase as required by KVL. The resulting system of equations is then evaluated for a possible solution of capacitance values that satisfy both charge-balance and KVL constraints. In other words, the system is solved for $C = q/\Delta v$.

2.3.1 KVL Equations

First, a set of linearly independent KVL loops must be found for both operating phases of the converter. These KVL equations can be written in the form of a matrix-vector product, given by

$$\mathbf{A_j v^j} = 0 \tag{2.1}$$

Here, $\mathbf{A_j}$ is the reduced loop matrix of the jth phase [26], and $\mathbf{v^j}$ is the voltage vector,

$$\mathbf{v^j} = \begin{bmatrix} v_{\text{in}} \\ v_{\text{C}_1} \\ \vdots \\ v_{\text{N}_\text{C}} \\ v_{\text{out}} \end{bmatrix}. \tag{2.2}$$

The KVL equations for each phase must be satisfied over the *entire* phase (and thus at the *start* and *end* of each phase). Therefore, at the start of phase j,

$$\mathbf{A_j v^j} = 0. \tag{2.3}$$

At the end of phase j, the voltage vector has increased by the per-phase ripple voltage vector $\mathbf{\Delta v_j}$. As the voltages at the end of the phase must also satisfy the same KVL equation, we can state

$$\mathbf{A_j}(\mathbf{v^j} + \mathbf{\Delta v^j}) = 0. \tag{2.4}$$

Satisfying both these constraints requires that

$$\mathbf{A_j \Delta v^j} = 0. \tag{2.5}$$

Stated in circuit terminology, this means that the ripple voltages on the sources and capacitors must satisfy the same KVL loops as the DC voltages on these elements.

An additional KVL constraint can be placed on the converter by recognizing that the input source is modeled as a stiff voltage, and therefore $\Delta v_{\text{in}} = 0$. This can be included in the matrix-vector product by adding another row consisting of $\begin{bmatrix} 1 & 0 & \dots & 0 & 0 \end{bmatrix}$ to the bottom of $\mathbf{A_j}$. This results in the modified loop matrix, $\mathbf{A_{m,j}}$. The relationship in (2.4) can then be modified to

$$\mathbf{A_{m,j} \Delta v^j} = 0. \tag{2.6}$$

where j refers to the phase.

2.3.2 Charge Balance

Additional constraints based on charge flow and perioidc steady state can also be applied. In [5], as the converters under discussion were restricted to two-phase topologies, this could simply be stated as

$$\mathbf{\Delta v^1} = -\mathbf{\Delta v^2}. \tag{2.7}$$

This relationship results from the periodic steady-state requirement that each capacitor must charge and discharge the same amount over a single switching period.

2.3.3 Impact of Low-Side (Output) Inductor

The converters in [5] were analyzed assuming the single hybridizing inductor was placed at the output port. This removes any strict requirement on the output terminal's ripple voltage, $\mathbf{\Delta v^j_{out}}$. Any "mis-matched" ripple voltages can appear across this inductor, rather than across the capacitors where they would incur hard-charging losses. Mathematically, this means that $\mathbf{\Delta v^j_{out}}$ is unconstrained for all phases.

2.3.4 Solving for Possible Capacitance Solutions

The system of equations resulting from the above setup can then be solved used matrix nullspace manipulations.

First, the required voltage ripple vectors in each phase can be found by solving (2.6), here repeated explicitly for Phase 1 and Phase 2.

$$\mathbf{A_{m,1}\Delta v^1} = 0 \tag{2.8}$$

$$\mathbf{A_{m,2}\Delta v^2} = 0 \tag{2.9}$$

Solutions to (2.8) and (2.9) comprise the nullspace of $\mathbf{A_{m,1}}$ and $\mathbf{A_{m,2}}$, respectively. The sets of vectors, $\mathbf{w}$ and $\mathbf{u}$, can be defined as the basis vectors for these nullspaces. Therefore, any solution to (2.8) and (2.9) can be expressed as a linear combination of $\mathbf{w}$ and $\mathbf{u}$, respectively.

First, it can be helpful to define some basic dimensions for these vectors. Let the number of linearly independent KVL equations be r_1 for Phase 1 and r_2 for Phase 2[1]. As we are assuming the $\mathbf{A_{m,j}}$ matrices are full row-rank, we can find that $rank(\mathbf{A_{m,1}}) = r_1$ and $rank(\mathbf{A_{m,2}}) = r_2$ (assuming that the row dimension of $\mathbf{v^j}$, r_v, is always greater than r_1 or r_2)[2]. The nullity (or number of independent vectors in the nullspace) of $\mathbf{A_{m,j}}$ is then given by

$$nullity(\mathbf{A_{m,j}}) = (\text{number of columns of } \mathbf{A_{m,j}}) - rank(\mathbf{A_{m,j}}) \tag{2.10}$$

$$= r_v - r_j \tag{2.11}$$

where $r_j = rank(\mathbf{A_{m,j}})$. If we let $m = nullity(\mathbf{A_{m,1}})$ and $n = nullity(\mathbf{A_{m,2}})$, then we can define $\mathbf{\Delta v^1}$ and $\mathbf{\Delta v^2}$ in terms of linear combinations of $\mathbf{w}$ and $\mathbf{u}$, respectively, as

$$\mathbf{\Delta v^1} = a_1\mathbf{w_1} + a_2\mathbf{w_2} + ... + a_m\mathbf{w_m} \tag{2.12}$$

$$\mathbf{\Delta v^2} = b_1\mathbf{u_1} + b_2\mathbf{u_2} + ... + b_n\mathbf{u_n}. \tag{2.13}$$

[1] We are assuming that the $\mathbf{A_{m,j}}$ matrices are properly constructed, such that they contain only linearly independent equations. This can be carried out in a more automated manner using nodal or mesh analysis, but for a circuit with E elements and N nodes, we can find $E - (N - 1)$ independent KVL equations.

[2] The rank of a matrix is the minimum of the number of rows and the number of columns, where the number of columns is the row dimension of $\mathbf{v^j}$. Here, we are assuming that the number of columns will always be larger than the number of rows.

As $\mathbf{A_{m,1}}$ and $\mathbf{A_{m,2}}$ can have different row dimensions, m does not have to equal n.

Next, the charge balance relationship in (2.7) can be rearranged to the form in (2.14) in order to solve for the a and b coefficients.

$$\mathbf{\Delta v^1} + \mathbf{\Delta v^2} = 0 \tag{2.14}$$

Note here we are using the full voltage vector $\mathbf{v}$ which includes terms for Δv_{in} and Δv_{out}. The former term can be included as $\mathbf{\Delta v_{in}} = 0$ by definition. The latter term will be removed in the next step due to the assumed presence of an output inductor. We can then substitute (2.12) and (2.13) into (2.14) to obtain the following

$$(a_1\mathbf{w_1} + a_2\mathbf{w_2} + ... + a_m\mathbf{w_m}) + (b_1\mathbf{u_1} + b_2\mathbf{u_2} + ... + b_n\mathbf{b_n}) = 0 \tag{2.15}$$

which can be expressed in matrix form as

$$\left[\begin{array}{ccc|ccc} | & & | & | & & | \\ \mathbf{w_1} & \dots & \mathbf{w_m} & \mathbf{u_1} & \dots & \mathbf{u_n} \\ | & & | & | & & | \end{array}\right] \left[\begin{array}{c} a_1 \\ \vdots \\ a_m \\ \hline b_1 \\ \vdots \\ b_n \end{array}\right] = \mathbf{0} \tag{2.16}$$

By using this form, it becomes evident that we can solve for the vectors $\mathbf{a} = \begin{bmatrix} a_1 & \dots & a_m \end{bmatrix}^T$ and $\mathbf{b} = \begin{bmatrix} b_1 & \dots & b_n \end{bmatrix}^T$ by finding the nullspace of the concatenated matrix $\begin{bmatrix} \mathbf{W} & \mathbf{U} \end{bmatrix}$. However, (2.16) as written has no solution, and the nullspace of $\begin{bmatrix} \mathbf{W} & \mathbf{U} \end{bmatrix}$ is empty. From a circuit understanding, this results from the fact that a pure SC converter cannot be soft-charged – it can only be operated far enough into the fast switching limit (FSL) that the losses are dominated by the resistive elements in the circuit [1].

If an inductor is added to the output node, however, we can add an additional degree of freedom to this system. Now, the output voltage ripple is no longer constrained to be any specific value, and can in fact be discontinuous (i.e. $\mathbf{\Delta v^1}$ does not have to equal $\mathbf{\Delta v^2}$). As $\mathbf{w}$ and $\mathbf{u}$ represent vectors of the form (2.2), we can then discard the last entry corresponding to Δv_{out}. These modified $\mathbf{w}$ and $\mathbf{u}$ vectors are labeled $\bar{\mathbf{w}}$ and $\bar{\mathbf{u}}$, and we can now solve

$$\left[\begin{array}{ccc|ccc} | & & | & | & & | \\ \bar{\mathbf{w}}_\mathbf{1} & \dots & \bar{\mathbf{w}}_\mathbf{m} & \bar{\mathbf{u}}_\mathbf{1} & \dots & \bar{\mathbf{u}}_\mathbf{n} \\ | & & | & | & & | \end{array}\right] \left[\begin{array}{c} a_1 \\ \vdots \\ a_m \\ \hline b_1 \\ \vdots \\ b_n \end{array}\right] = \mathbf{0}. \tag{2.17}$$

As we have removed a row, this matrix has reduced rank compared to the one in (2.16), and now a nonzero solution exits. The resulting **a** and **b** vectors determine which linear combinations of the **w** and **u** vectors result in $\mathbf{\Delta v^1}$ and $\mathbf{\Delta v^2}$ solutions that satisfy both KVL and charge flow. These ripple voltage vectors can be found using (2.12) and (2.13), by substituting in the values for a and b that were found in (2.17).

Charge flow analysis can then be performed using the method detailed in [1] to determine the charge that must flow through each capacitor in each phase. A charge flow vector can be found in the form

$$\mathbf{q^j} = \begin{bmatrix} q_{\text{in}} & q_{\text{C}_1} & \dots & q_{\text{C}_{\text{N}_\text{C}}} & q_{\text{out}} \end{bmatrix}^j \tag{2.18}$$

where N_C is the number of flying capacitors and j is the operating phase.

The required capacitance, C_i, can then be calculated by

$$C_i = \frac{q_i^j}{\Delta v_{C_i}^j}, \tag{2.19}$$

for a given phase j. For a converter for which a solution exits, this ratio of charge to voltage ripple will be equal across all phases, and therefore only one phase needs to be solved for.

2.4 Extension 1: Multiple Inductors at the Low-Side Port

We now investigate several hybrid SC converters which have more than one inductor, but still place the inductor directly at the output node.

Before we introduce these topologies, it will be useful to first reference the 5-to-1 Dickson converter, shown in Fig. 2.5. Phase equivalent circuits are shown in Fig. 2.6. These equivalent circuits are very similar to the switch-capacitor-inductor networks present in the converters analyzed in the following section. For ease of reference, we define Fig. 2.6a as a "Phase 1 Configuration" and Fig. 2.6b as a "Phase 2 Configuration." These labels will be used for reference later in this section.

Dual Inductor Hybrid (DIH) Converter

The dual inductor hybrid converter [27, 28] is an example of a multi-inductor-at-the-output topology, which has seen increased popularity in data center power delivery applications. As described in [21], this converter is capable of achieving soft-charging with two-phase 50% duty cycle control (i.e. without the use of split-phase operation) for odd-N conversion ratios by following a specific sizing ratio for the capacitors. Using a modified version of the analysis presented in the previous section, we can obtain the same result.

Fig. 2.7 shows a 5-to-1 (i.e. N=5) DIH converter. The equivalent circuits for Phase 1 and Phase 2 are given in Fig. 2.8. While the DIH converter can also be operated with additional interleaved regulating phases in which both output inductors are shorted to ground, we can

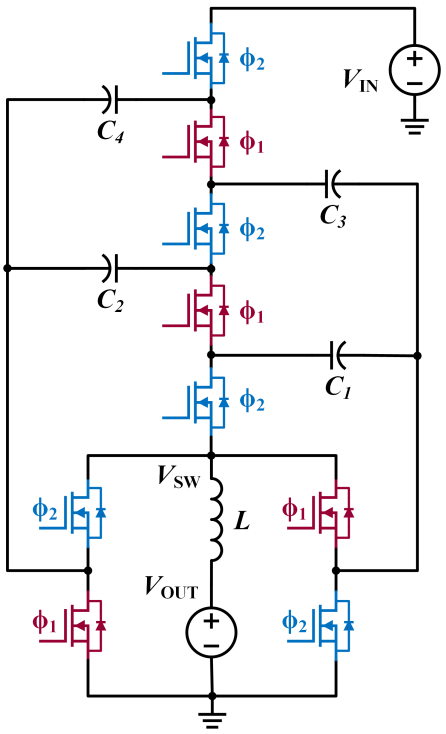


Figure 2.5: Schematic drawing of a 5-to-1 Dickson converter. The two-phase gate signals ϕ_1 and ϕ_2 are annotated on the schematic.

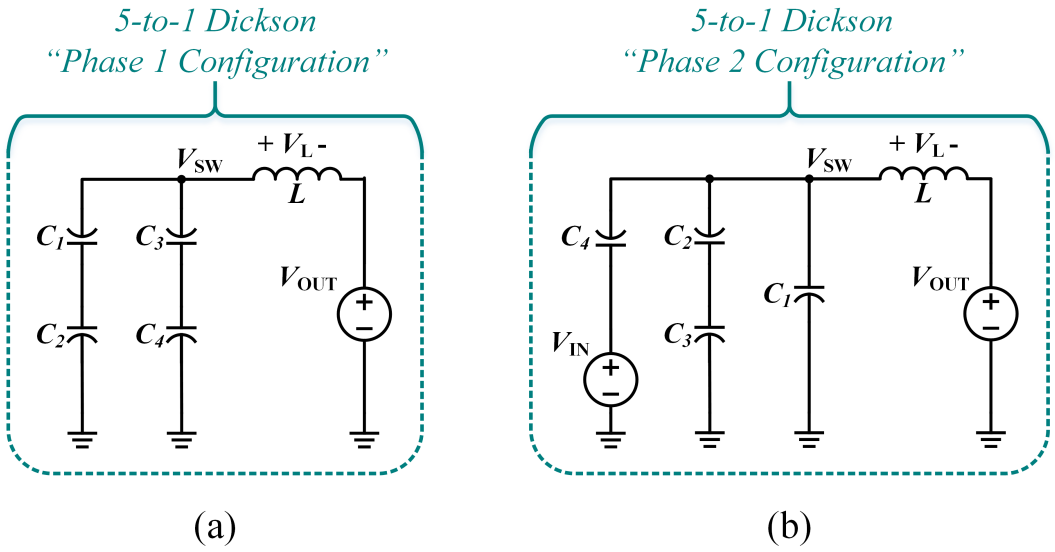


Figure 2.6: Phase equivalent circuits for the 5-to-1 Dickson converter. The switch-capacitor networks here will be repeated throughout the converters analyzed in the following sections.

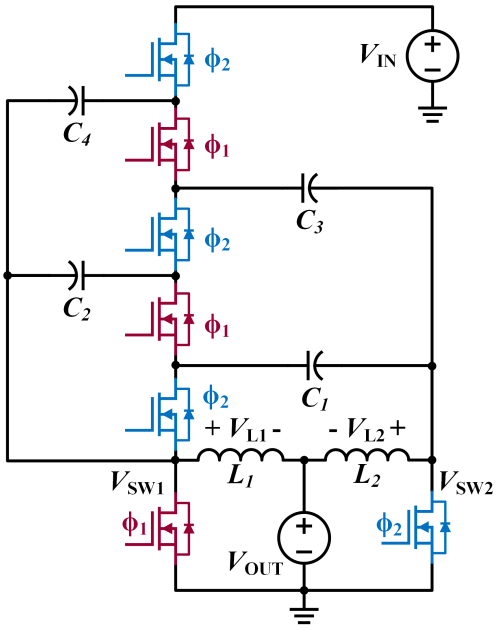


Figure 2.7: Schematic drawing of a 5-to-1 DIH converter. The two-phase gate signals ϕ_1 and ϕ_2 are annotated on the schematic. Regulating phases can be ignored for this analysis.

ignore these phases for the purpose of capacitor sizing. This is because the capacitor network does not undergo any charging or discharging during these phases. The switch-capacitor network is identical to that of the 5-to-1 Dickson converter (i.e. the topology in [29]), as shown by the teal brackets. The only difference is the additional inductor between the output and ground.

Through inspection of these equivalent circuits, we can see that the inductors are alternately connected to the switch-capacitor network or shorted to ground during Phase 1 and Phase 2. For a given phase, we can ignore the inductor that is shorted to ground, as it is not directly connected to the switch-capacitor network. We can therefore write the last row in our voltage vector in terms of $(v_{L_2} + v_{out})$ during Phase 1 and $(v_{L_1} + v_{out})$ during Phase 2, instead of simply v_{out}[3].

[3]Equivalently, we could write the last row of the voltage vector in terms of only v_{out}, and understand that the inductor we are assuming is placed between the switch node and the output during Phase 1 and Phase 2 is actually two separate inductors.

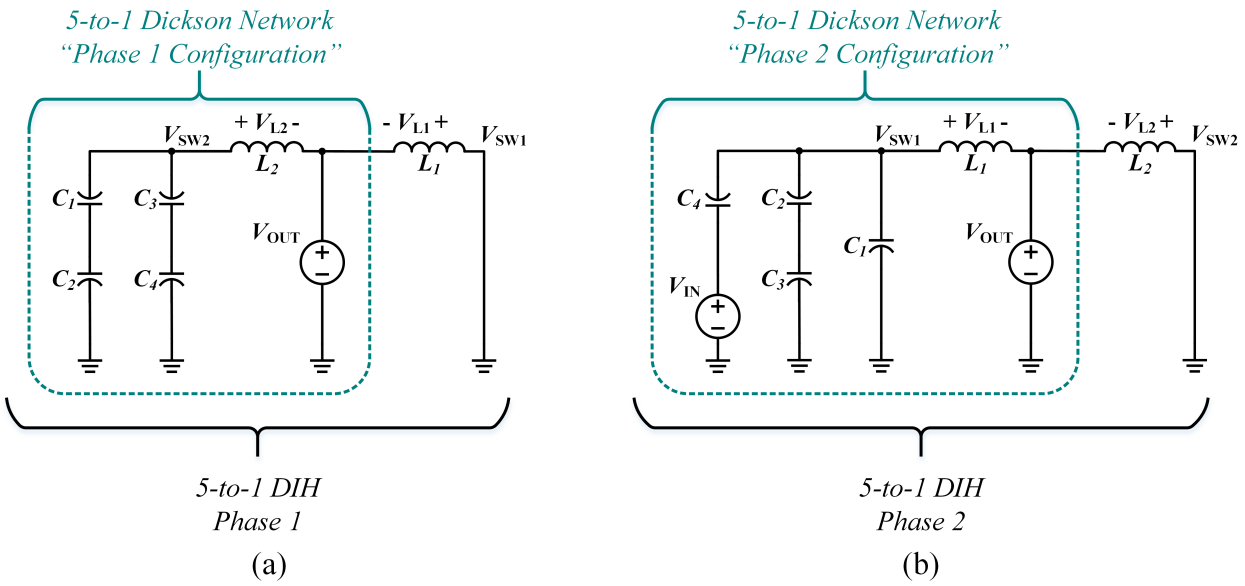


Figure 2.8: Phase equivalent circuits for the 5-to-1 DIH Converter. The switch-capacitor network configuration is the same as that in the 5-to-1 Dickson converter, as labeled by the teal bracket.

We can write the KVL equations for Phase 1 and Phase 2 as

$$\text{Phase 1:} \begin{cases} -V_{\mathrm{C}_1} + V_{\mathrm{C}_2} - (V_{\mathrm{L}_2} + V_{\mathrm{out}}) = 0 \\ -V_{\mathrm{C}_3} + V_{\mathrm{C}_4} - (V_{\mathrm{L}_2} + V_{\mathrm{out}}) = 0 \end{cases} \tag{2.20}$$

$$\text{Phase 2:} \begin{cases} V_{\mathrm{in}} - V_{\mathrm{C}_4} - (V_{\mathrm{L}_1} + V_{\mathrm{out}}) = 0 \\ V_{\mathrm{C}_1} - (V_{\mathrm{L}_1} + V_{\mathrm{out}}) = 0 \\ -V_{\mathrm{C}_2} + V_{\mathrm{C}_3} - (V_{\mathrm{L}_1} + V_{\mathrm{out}}) = 0 \end{cases} \tag{2.21}$$

These KVL equations can be put in matrix form $\mathbf{A}_j \mathbf{v}^j$ where v^j is now given by

$$\boldsymbol{v}^{\mathbf{j}} = \begin{bmatrix} v_{\mathrm{in}} \\ v_{\mathrm{C}_1} \\ \vdots \\ v_{\mathrm{N_C}} \\ (v_{\mathrm{out}} + v_{\mathrm{L}_k}) \end{bmatrix} \tag{2.22}$$

where k is the corresponding inductor connected between the switch-capacitor network and the output node for a given phase j. The modified $\mathbf{A_{m,j}}$ matrices are shown below, with the

additional row $\begin{bmatrix}1 & 0 & \dots & 0 & 0\end{bmatrix}$ shown appended to the bottom of the original $\mathbf{A_j}$ matrix.

$$\mathbf{A_{m,1}} = \left[\begin{array}{cccccc} 0 & -1 & 1 & 0 & 0 & -1 \\ 0 & 0 & 0 & -1 & 1 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \tag{2.23}$$

$$\mathbf{A_{m,2}} = \left[\begin{array}{cccccc} 1 & 0 & 0 & 0 & -1 & -1 \\ 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 1 & 0 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \tag{2.24}$$

We can now proceed with the rest of the analysis as described in Section 2.3. We can use the `null` command in MATLAB to find the following $\mathbf{w}$ and $\mathbf{u}$ vectors

$$\mathbf{u_1} = \begin{bmatrix} 0 \\ -0.3379 \\ 0.7168 \\ 0.3789 \\ 0.3379 \\ -0.3379 \end{bmatrix}, \ \mathbf{u_2} = \begin{bmatrix} 0 \\ 0.4141 \\ 0.2400 \\ 0.6541 \\ -0.4141 \\ -0.4141 \end{bmatrix} \tag{2.25}$$

$$\mathbf{w_1} = \begin{bmatrix} 0 \\ 0.5383 \\ 0.2024 \\ 0.6680 \\ 0.3320 \\ -0.3359 \end{bmatrix}, \ \mathbf{w_2} = \begin{bmatrix} 0 \\ -0.5383 \\ -0.2024 \\ 0.3320 \\ 0.6680 \\ 0.3359 \end{bmatrix}, \ \mathbf{w_3} = \begin{bmatrix} 0 \\ -0.2132 \\ -0.7370 \\ -0.2619 \\ 0.2619 \\ 0.5237 \end{bmatrix} \tag{2.26}$$

This results in the following $\mathbf{\Delta v^1}$ and $\mathbf{\Delta v^2}$ vectors.

$$\mathbf{\Delta v^1} = \begin{bmatrix} 0 \\ -0.3482 \\ 0.1741 \\ -0.1741 \\ 0.3482 \\ -0.5222 \end{bmatrix}, \ \mathbf{\Delta v^2} = \begin{bmatrix} 0 \\ 0.3482 \\ -0.1741 \\ 0.1741 \\ -0.3482 \\ 0.3482 \end{bmatrix} \tag{2.27}$$

Note that the rows corresponding to the capacitors (i.e. row 2 through row 4) are equal and opposite between the two voltage vectors. The Δv_{in} term is zero for both vectors, as designed. There is no required relationship between the Δv_{out} terms in the last row.

The Phase 1 and Phase 2 charge vectors, $\mathbf{q^1}$ and $\mathbf{q^2}$, respectively, are given by

$$\mathbf{q^1} = \begin{bmatrix} 0 & 1 & -1 & 1 & -1 & 2 \end{bmatrix} \tag{2.28}$$

$$\mathbf{q^2} = \begin{bmatrix} -1 & -1 & 1 & -1 & 1 & 3 \end{bmatrix} \tag{2.29}$$

The required capacitance ratios can then be found using (2.19). This results in the following capacitance vector for the 5-to-1 DIH converter, which matches with the general results obtained in [21].

$$\begin{bmatrix} C_1 \\ C_2 \\ C_3 \\ C_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 2 \\ 2 \\ 1 \end{bmatrix} \tag{2.30}$$

This is also the same capacitance vector required for the 5-to-1 Dickson converter to operate without soft-charging. This is because the DIH converter's phase equivalent circuits reduce to the same switch-capacitor plus output-inductor network as the Dickson converter, with the addition of one extra inductor. This inductor does not participate in the capacitor charging dynamics, and therefore does not impact the capacitor sizing result.

Symmetric Dual Inductor Hybrid (DIH) Converter

We can similarly analyze the symmetric dual inductor hybrid (SDIH) converter, which can be thought of as two interleaved DIH converters. The SDIH converter requires a higher number of capacitors compared to the DIH converter for a given N, but has several performance benefits that make it an attractive topology, as described in [30, 31]. The 3-to-1 SDIH converter has the same capacitor network as the 5-to-1 Dickson converter, as shown in Fig. 2.10.

We can write the KVL equations for Phase 1 and Phase 2 as

$$\text{Phase 1:} \begin{cases} V_{\text{in}} - V_{\text{C}_3} - (V_{\text{L}_2} + V_{\text{out}}) = 0 \\ -V_{\text{C}_1} + V_{\text{C}_4} - (V_{\text{L}_2} + V_{\text{out}}) = 0 \\ V_{\text{C}_2} - (V_{\text{L}_2} + V_{\text{out}}) = 0 \end{cases} \tag{2.31}$$

$$\text{Phase 2:} \begin{cases} V_{\text{in}} - V_{\text{C}_4} - (V_{\text{L}_1} + V_{\text{out}}) = 0 \\ V_{\text{C}_1} - (V_{\text{L}_1} + V_{\text{out}}) = 0 \\ -V_{\text{C}_2} + V_{\text{C}_3} - (V_{\text{L}_1} + V_{\text{out}}) = 0 \end{cases} \tag{2.32}$$

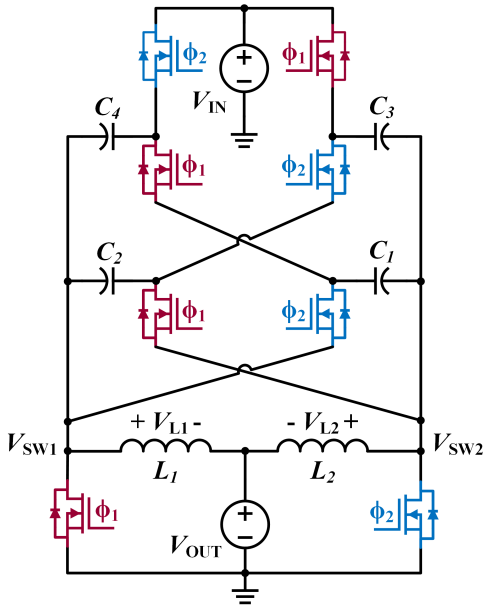


Figure 2.9: Schematic drawing of a 3-to-1 SDIH converter. The two-phase gate signals ϕ_1 and ϕ_2 are annotated on the schematic.

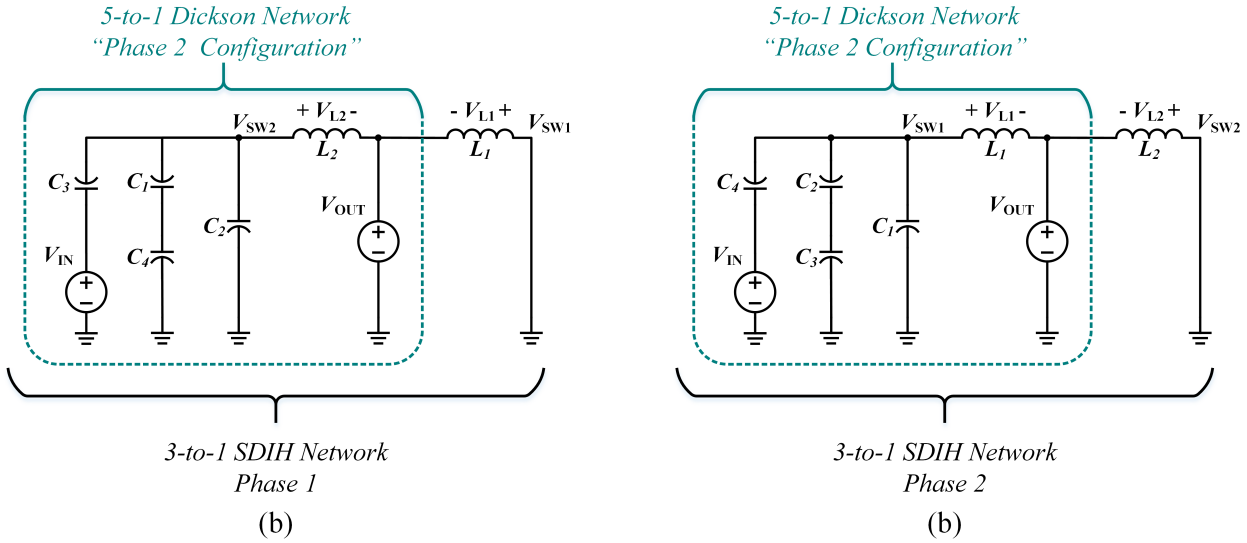


Figure 2.10: Phase equivalent circuits for the 3-to-1 SDIH converter. Due to the interleaved structure, the input is connected to the switch-capacitor network in both phases, and therefore the SDIH can be viewed as operating with the "Phase 2 Configuration" of the 5-to-1 Dickson converter for both of its own phases.

The resulting modified $\mathbf{A_{m,j}}$ matrices are shown below

$$\mathbf{A_{m,1}} = \left[\begin{array}{cccccc} 1 & 0 & 0 & -1 & 0 & -1 \\ 0 & -1 & 0 & 0 & 1 & -1 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \tag{2.33}$$

$$\mathbf{A_{m,2}} = \left[\begin{array}{cccccc} 1 & 0 & 0 & 0 & -1 & -1 \\ 0 & 1 & 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 1 & 0 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 \end{array}\right]. \tag{2.34}$$

Note that (2.34) is the same as (2.24), as the Phase 2 equivalent circuits for both the 5-to-1 DIH and the 3-to-1 SDIH converters are based on the same "Phase 2 Configuration" of the 5-to-1 Dickson converter. However, the $\mathbf{A_{m,1}}$ matrices differ, as the input is disconnected during Phase 1 for the 5-to-1 DIH converter, while it is connected in both Phase 1 and Phase 2 for the 3-to-1 SDIH converter.

If we try to solve for the $\mathbf{a}$ and $\mathbf{b}$ vectors using (2.17), we find that there are no solutions. This matches the results found in [22,30,31] stating that the SDIH converter does not have a specific capacitor sizing scheme under which it can achieve full soft-charging with two-phase switching. Instead, it must be operated with split-phase switching [29].

2.5 Extension 2: Multiple Inductors with Tank Configuration

Next, we can analyze a class of hybrid SC converters with multiple inductors, which are *not* connected directly to the output node. These types of converters are often termed "indirect" or "tank" style converters [32], as the inductor currents are zero-centered sinusoids.

2.5.1 Dual Extended LC Tank Converter

The dual extended LC tank converter [33] is one such topology, and the schematic for a 5-to-1 converter is shown in Fig. 2.11a. Applying the analysis in [5] is somewhat more complex, as the output node is now directly connected to the switched-capacitor network, rather than connected through an inductor. This means that some of the analysis steps require modification.

The first step is to write out the KVL equations for Phase 1 and Phase 2, using the phase equivalent circuits shown in Fig. 2.11a and Fig. 2.11b.

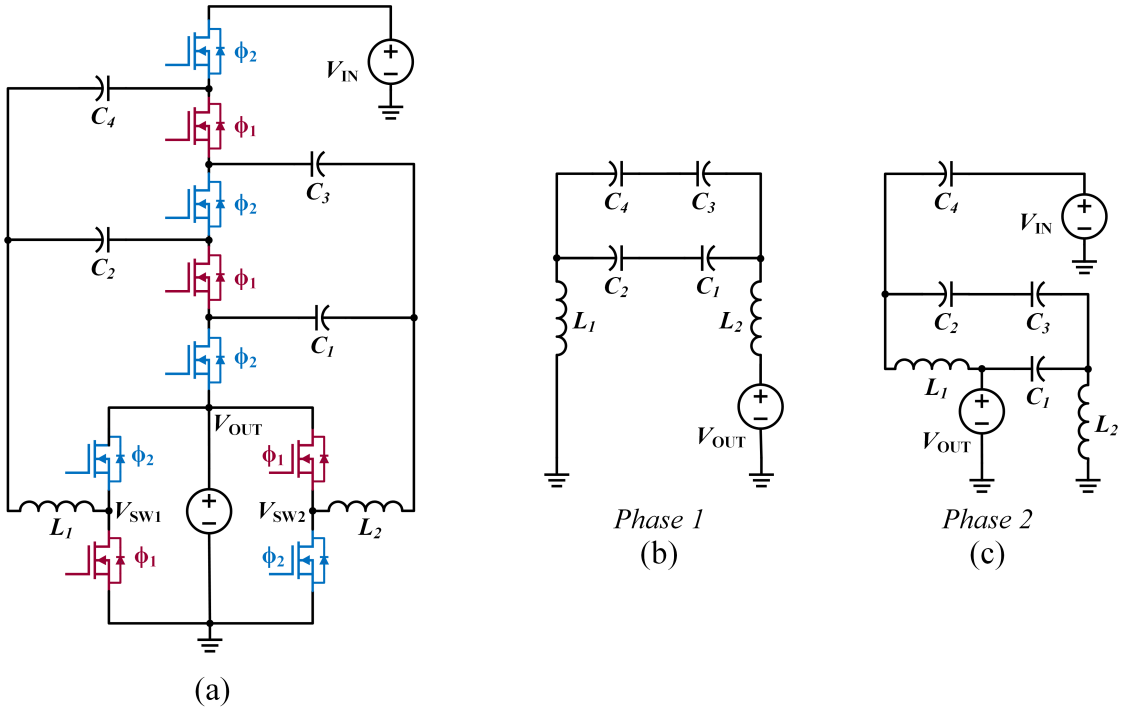


Figure 2.11: Schematic drawing of a 5-to-1 dual LC tank converter. The two-phase gate signals ϕ_1 and ϕ_2 are annotated on the schematic.

$$\text{Phase 1:} \begin{cases} V_{\mathrm{C}_1} - V_{\mathrm{C}_2} - V_{\mathrm{C}_3} + V_{\mathrm{C}_4} = 0 \\ -V_{\text{out}} - V_{\mathrm{C}_1} + V_{\mathrm{C}_2} + V_{\mathrm{L}_1} + V_{\mathrm{L}_2} = 0 \end{cases} \tag{2.35}$$

$$\text{Phase 2:} \begin{cases} V_{\text{in}} - V_{\mathrm{C}_4} - (V_{\mathrm{L}_1} + V_{\text{out}}) = 0 \\ V_{\mathrm{C}_1} - (V_{\mathrm{L}_2} + V_{\text{out}}) = 0 \\ -V_{\mathrm{C}_2} + V_{\mathrm{C}_3} - (V_{\mathrm{L}_1} + V_{\text{out}}) = 0 \end{cases} \tag{2.36}$$

Because we cannot lump the inductor and output together as a single node now, we will use a modified voltage vector as shown in (2.37), which now contains entries for v_{L_1} and v_{L_2}. The voltage ripples across these inductors are still unconstrained, so the corresponding rows in the new $\mathbf{w}$ and $\mathbf{u}$ vectors can be eliminated, as was done with the v_{out} node in the previous examples. However, the output node is now directly connected to the switch-capacitor network, and is no longer unconstrained. We can, however, treat it similarly to the input source, and assume that it is a stiff voltage with no ripple (i.e. $\Delta v_{\text{out}} = 0$). This then requires us to add *two* rows to the modified loop matrices $\mathbf{A}_j$, one corresponding to $\Delta v_{\text{in}} = 0$ and one corresponding to $\Delta v_{\text{out}} = 0$, as is shown in (2.38) and (2.39). Furthermore, because

the input and output nodes are now treated the same, we have positioned these rows one after the other in (2.37).

$$\boldsymbol{v}^{\mathbf{j}} = \begin{bmatrix} v_{\text{in}} \\ v_{\text{out}} \\ v_{C_1} \\ \vdots \\ v_{\text{C}_{\text{N}_\text{C}}} \\ v_{\text{L}_1} \\ v_{\text{L}_2} \end{bmatrix} \tag{2.37}$$

The KVL equations in (2.35) and (2.36) can be re-expressed as the modified loop matrices, $\mathbf{A_{m,1}}$ and $\mathbf{A_{m,2}}$.

$$\mathbf{A_{m,1}} = \left[\begin{array}{cccccccc} 0 & 0 & 1 & -1 & -1 & 1 & 0 & 0 \\ 0 & -1 & -1 & 1 & 0 & 0 & 1 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \tag{2.38}$$

$$\mathbf{A_{m,2}} = \left[\begin{array}{cccccccc} 1 & -1 & 1 & 1 & -1 & -1 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 & 0 & -1 \\ \hline 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{array}\right] \tag{2.39}$$

We can now find the vectors $\mathbf{w}$ and $\mathbf{u}$ by solving for the nullspace of the loop matrices, as described in (2.8) and (2.9). Previously we discarded the last row of $\mathbf{w}$ and $\mathbf{u}$, as it corresponded to the unconstrained Δv_{out} term. Now, we must now discard the last *two* rows, which correspond to the unconstrained inductor voltage ripple terms, Δv_{L_1} and Δv_{L_2}.

Once we have these modified $\bar{\mathbf{w}}$ and $\bar{\mathbf{u}}$ vectors, we can solve for the $\mathbf{a}$ and $\mathbf{b}$ vectors as defined in (2.17). After obtaining these vectors, we can solve for the $\mathbf{\Delta v^1}$ and $\mathbf{\Delta v^2}$ as shown in (2.12) and (2.13), respectively.

However, when we carry out these calculations, we find that we no longer get a single column solution for $\mathbf{\Delta v^1}$ and $\mathbf{\Delta v^2}$. Instead, we find that

$$\boldsymbol{\Delta v_1}^{\mathbf{1}} = \begin{bmatrix} 0 \\ 0 \\ -0.1860 \\ 0.3343 \\ -0.2196 \\ 0.3680 \\ -0.3680 \\ 0.1860 \end{bmatrix}, \ \boldsymbol{\Delta v_2}^{\mathbf{1}} = \begin{bmatrix} 0 \\ 0 \\ 0.2791 \\ 0.3136 \\ 0.4575 \\ 0.1351 \\ -0.1351 \\ -0.2791 \end{bmatrix}, \ \boldsymbol{\Delta v_3}^{\mathbf{1}} = \begin{bmatrix} 0 \\ 0 \\ 0.3096 \\ -0.3510 \\ -0.2752 \\ 0.2338 \\ -0.2338 \\ -0.3096 \end{bmatrix} \tag{2.40}$$

$$\boldsymbol{\Delta v_1}^{\mathbf{2}} = \begin{bmatrix} 0 \\ 0 \\ 0.1860 \\ -0.3343 \\ 0.2196 \\ -0.3680 \\ 0.3680 \\ -0.1860 \end{bmatrix}, \ \boldsymbol{\Delta v_2}^{\mathbf{2}} = \begin{bmatrix} 0 \\ 0 \\ -0.2791 \\ -0.3136 \\ -0.4575 \\ -0.1351 \\ 0.1351 \\ 0.2791 \end{bmatrix}, \ \boldsymbol{\Delta v_3}^{\mathbf{2}} = \begin{bmatrix} 0 \\ 0 \\ -0.3096 \\ 0.3510 \\ 0.2752 \\ -0.2338 \\ 0.2338 \\ 0.3096 \end{bmatrix} \tag{2.41}$$

As expected, the first two rows in each vector are equal to zero, as $\Delta v_{in} = \Delta v_{out} = 0$. In addition, each of capacitor entries in the column vectors in $\mathbf{\Delta v^1}$ are equal and opposite to the capacitor entries in the column vectors in $\mathbf{\Delta v^2}$.

Note that any one of $\boldsymbol{\Delta v_1}^{\mathbf{1}}...\boldsymbol{\Delta v_3}^{\mathbf{1}}$ (or equivalently $\boldsymbol{\Delta v_1}^{\mathbf{2}}...\boldsymbol{\Delta v_3}^{\mathbf{2}}$) is a possible solution that 1) satisfies KVL and 2) satisfies charge balance on the capacitors. However, not all of these ripple vectors will result in a corresponding capacitance vector that is 1) all positive, and 2) finite.

Because the solution space for this converter is much larger than the other examples demonstrated, we can slightly modify our approach to check if a specific capacitance vector satisfies all conditions. A common capacitor sizing for this desired capacitance vector, $\mathbf{C_{des}}$, would be

$$\mathbf{C_{des}} = \begin{bmatrix} C_{\text{des},1} \\ C_{\text{des},2} \\ C_{\text{des},3} \\ C_{\text{des},4} \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} \tag{2.42}$$

Next, we can find the charge flow quantities for the capacitors in Phase 1 and Phase 2, and use these to calculate the $\mathbf{\Delta v^j}$ voltage ripple vector that would result from this combination of capacitance and charge. The charge flow vectors for the 5-to-1 dual extended LC converter are given in the form below, to match that of the $\mathbf{\Delta v^j}$ vector.

$$\mathbf{q^j} = \begin{bmatrix} q_{\text{in}} & q_{\text{out}} & q_{\text{C}_1} & \cdots & q_{\text{C}_{\text{N}_\text{C}}} & q_{\text{L}_1} & q_{\text{L}_2} \end{bmatrix} \tag{2.43}$$

Phase 1 and Phase 2 quantities can be found as

$$\mathbf{q^1} = \begin{bmatrix} 0 & 2 & 1 & -1 & 1 & -1 & -2 & 2 \end{bmatrix} \tag{2.44}$$

$$\mathbf{q^2} = \begin{bmatrix} -1 & 3 & -1 & 1 & -1 & 1 & 2 & -2 \end{bmatrix}. \tag{2.45}$$

We can now find the per-phase voltage ripples that would result as a combination of (2.42) and either (2.44) or (2.45). Note, the rows corresponding to v_{L_1} and v_{L_2} can be removed, as they do not matter for determining the capacitor ripple voltages. We can therefore find this modified voltage vector $\boldsymbol{\Delta \bar{v}_{des}}^{\boldsymbol{j}}$ given by

$$\boldsymbol{\Delta \bar{v}_{des}}^{\boldsymbol{j}} = \begin{bmatrix} \Delta v_{\mathrm{in}} \\ \Delta v_{\mathrm{out}} \\ \Delta v_{\mathrm{C_{des,1}}} \\ \vdots \\ \Delta v_{\mathrm{C_{des,N_C}}} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \frac{q_{\mathrm{C_1,j}}}{C_1} \\ \vdots \\ \frac{q_{\mathrm{C_{des,N_C},j}}}{C_{\mathrm{des,N_C}}} \end{bmatrix}. \tag{2.46}$$

We would like to check if this solution lies in the subspace spanned by the solutions $\boldsymbol{\Delta v_1}^{\boldsymbol{j}} \ldots \boldsymbol{\Delta v_3}^{\boldsymbol{j}}$. To do this, we can again ignore the rows corresponding to the inductor voltage ripples to ensure that we are not restricting our solution set by ripple voltages that are in fact unconstrained. Therefore, we can instead look at the subspace spanned by $\boldsymbol{\Delta \bar{v}_1}^{\boldsymbol{j}} \ldots \boldsymbol{\Delta \bar{v}_3}^{\boldsymbol{j}}$, where these vectors have had the rows corresponding to L_1 and L_2 removed.

In order to check if the vector of desired capacitances, $\boldsymbol{C_{des}}$ produces a voltage ripple solution that lies within this span, we can check if the rank of the space defined by $\boldsymbol{\Delta \bar{v}_1}^{\boldsymbol{j}} \ldots \boldsymbol{\Delta \bar{v}_3}^{\boldsymbol{j}}$ is the same as the rank defined by $\boldsymbol{\Delta \bar{v}_1}^{\boldsymbol{j}} \ldots \boldsymbol{\Delta \bar{v}_3}^{\boldsymbol{j}}$, and $\boldsymbol{\Delta \bar{v}_{des}}^{\boldsymbol{j}}$, as shown in (2.47). If the rank is the same, then that means that the ripple voltage vector resulting from $\boldsymbol{C_{des}}$ is a linear combination of the voltage vectors $\boldsymbol{\Delta \bar{v}_1}^{\boldsymbol{j}} \ldots \boldsymbol{\Delta \bar{v}_3}^{\boldsymbol{j}}$, and therefore is also a solution that satisfies KVL and charge balance.

Performing this check, we can see that the capacitance vector given in (2.42) does satisfy this system of equations, and therefore is a valid capacitor sizing scheme, as corroborated in [22, 33].

$$rank\left(\begin{bmatrix} | & & | \\ \boldsymbol{\Delta \bar{v}_{1j}} & \ldots & \boldsymbol{\Delta \bar{v}_{3j}} \\ | & & | \end{bmatrix}\right) = rank\left(\left[\begin{array}{ccc|c} | & & | & | \\ \boldsymbol{\Delta \bar{v}_{1j}} & \ldots & \boldsymbol{\Delta \bar{v}_{3j}} & \boldsymbol{\Delta \bar{v}_{des}}^{\boldsymbol{j}} \\ | & & | & | \end{array}\right]\right) \tag{2.47}$$

2.6 Extension 3: Multiple Operating Phases (> 2)

The analysis presented in [5] used charge balance for a two-phase converter to state that a given capacitor's voltage ripple in Phase 1 must be equal and opposite to its voltage ripple in Phase 2. However, this is not necessarily true for multi-resonant topologies, in which a

capacitor may charge or discharge over multiple phases. Therefore, mulitple sets of a and b coefficients would need to be solved, each corresponding to a null space equation relating to some charge balance relationship for two or more phases. This can be expressed as a relationship between the different per-phase voltage ripple vectors, in the form

$$\boldsymbol{\Delta}\mathbf{v}^{\boldsymbol{j}} = -(\boldsymbol{\Delta}\mathbf{v}^{\boldsymbol{k}} + \boldsymbol{\Delta}\mathbf{v}^{\boldsymbol{l}}), \tag{2.48}$$

where j, k, and l correspond to different operating phases. The final $\boldsymbol{\Delta}\mathbf{v}$ solution would then have to lie in the union of all sets of solutions, in order to be able to satisfy every phases' ripple voltage KVL requirements. Note, the same general assumptions of a stiff voltage source at the input terminal and an unconstrained inductor voltage apply.

Chapter 7 applies a very simplified version of this method to the CaSP converter, and so we refer to this section for an example of this methodology.

2.7 Chapter Summary

This chapter explored the concepts of hard-charging and soft-charging in pure SC and hybrid SC converters. In addition, several extensions were described for use with the methodology presented in [5], allowing for the analysis of the soft-charging capability of converters with multiple inductors, with inductors not at the low-side node, and with more than two operating phases.

Chapter 3

Split-Phase Switching Overview

As shown in the previous chapter, there are many hybrid switched-capacitor (SC) converters that can achieve soft-charging of all flying capacitors by adding a single inductor at the low-side port. However, this is not the case for all topologies, where there can exist a loop of capacitors whose voltage ripple cannot be forced across a series-connected inductor, nor whose voltage ripples naturally cancel out against each other. These topologies may instead require multiple inductors, so that every capacitor's charge and discharge path is accounted for. Alternatively, they can be operated with control schemes that involve more phases than the standard two-phase operation. One such control method is split-phase switching [29], in which capacitors are removed from the switch-capacitor network in such a way that they charge and discharge the exact amount required to avoid any capacitor voltage mismatches at phase transitions.

This chapter will provide an intuitive understanding of split-phase switching and illustrate how the control scheme ensures the flying capacitors do not undergo hard-charging. There has been a significant amount of prior work published about how to calculate these required sub-phase timings, and for the sake of clarity and conciseness, we will refer the reader to these works in Section 3.3. Additional timing analysis will also be provided in Chapter 4 for the dual inductor hybrid (DIH) converter (a Dickson-variant topology).

3.1 Hard-Charged Two-Phase Resonant Dickson Converter Operation

Even-N (i.e. N:1) single-ended Dickson converters are an example of a topology that cannot achieve full soft-charging with two-phase operation and a single inductor. While Section 2.4 showed that a capacitance vector resulting in soft-charged operation can be found for two-phase odd-N Dickson converters, there is no set of capacitance values that can result in soft-charged operation for two-phase even-N converters[1], necessitating the use of split-phase

[1]Odd Dickson converters have an even number of flying capacitors, while even Dickson converters have an odd number of flying capacitors. The manner in which these capacitors are configured in different branches

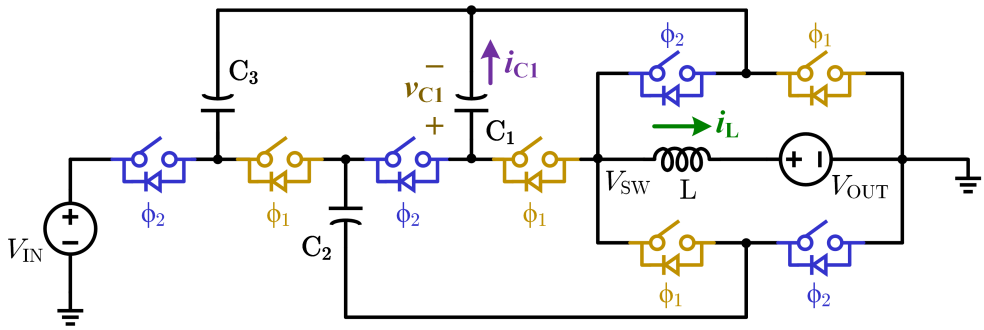


Figure 3.1: Schematic drawing of the 4-to-1 resonant Dickson converter, operated with two-phase gate signals, ϕ_1 and ϕ_2.

control. This technique was first demonstrated on a single-ended Dickson converter that was operated high above its natural resonant frequency [29], though the control technique has since been demonstrated on the resonant Dickson converter [34, 35], as well as other Dickson-derived topologies [11, 22, 27, 28, 30, 31, 36, 37].

Fig. 3.1 shows a schematic drawing of 4-to-1 step-down single-ended Dickson converter. Here, we assume all flying capacitors are equal, i.e. $C_1 = C_2 = C_3 = C_0$. First, we will examine two-phase operation, to investigate the root cause of the hard-charging seen by the flying capacitors. Fig. 3.2 shows simplified equivalent circuits for Phase 1 and Phase 2. By performing charge flow analysis [1] and using the principle of capacitor charge balance, it

therefore differs between the odd and even variants, resulting in different soft-charging behavior.

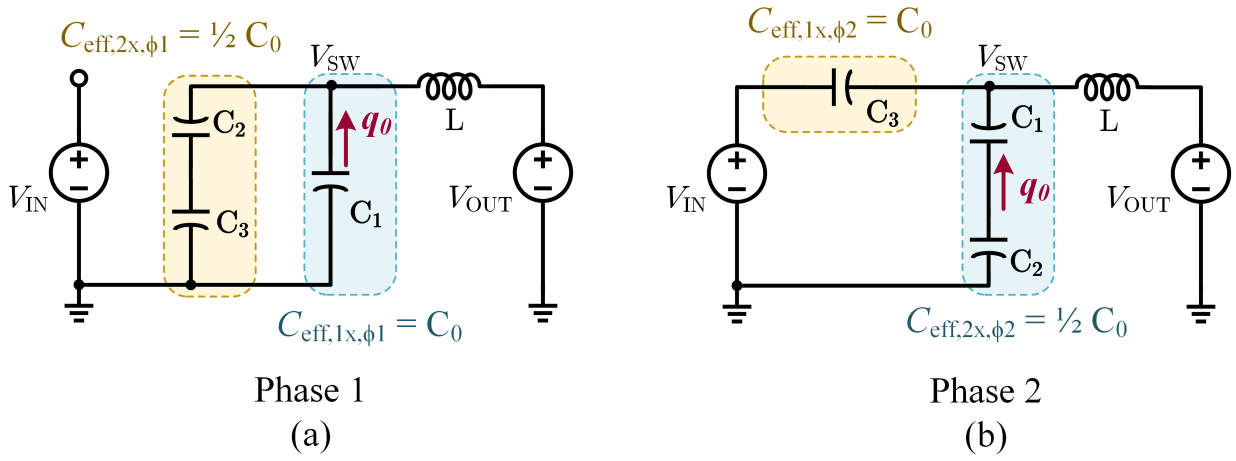


Figure 3.2: Simplified Phase 1 and Phase 2 equivalent circuits for the 4-to-1 resonant Dickson converter. The effective branch capacitances are labeled, as is the charge into and out of C_1.

can be seen that capacitor C_1 discharges by a total charge of q_0 in Phase 1, and charges by a total charge of q_0 in Phase 2. Note that in Fig. 3.2, the arrow indicates the direction of charging, and therefore the polarity of the q_0 term.

During Phase 1, C_1 is directly connected to the switch-node V_{SW}, and the total effective capacitance of its branch is therefore $C_{\text{eff,1x},\phi 1} = C_0$. During Phase 2, however, C_1 and C_2 are connected in series across the switch-node, and the total effective capacitance of this branch is now $C_{\text{eff,2x},\phi_2} = \frac{1}{2}C_0$. Here, the subscript "1x" refers to the single-capacitor connection, and the subscript "2x" refers to the series-capacitor connection. These branches will have equivalent impedances[2]

$$Z_{\text{eff,1x}} = \frac{1}{j\omega C_0} \tag{3.1}$$

$$Z_{\text{eff,2x}} = \frac{2}{j\omega C_0} \tag{3.2}$$

The "1x" and "2x" branches will then act as a current divider for the inductor output current. Due to its lower impedance, the "1x" branch will carry more current, whose magnitude can be expressed in terms of the output current as

$$i_{\text{C}_{\text{eff,1x}}} = \frac{Z_{\text{eff,2x}}}{Z_{\text{eff,1x}} + Z_{\text{eff,2x}}} i_L \tag{3.3}$$

$$= \frac{2}{3} i_L. \tag{3.4}$$

Similarly, the magnitude of the current through the "2x" branch can be given by

$$i_{\text{C}_{\text{eff,2x}}} = \frac{1}{3} i_L. \tag{3.5}$$

However, we have previously stated that 1) C_1 must conduct a total charge of magnitude q_0 during Phase 1 and Phase 2, and 2) that C_1 is connected to the switch-node for the same amount of time during Phase 1 and Phase 2, assuming two-phase 50% operation. If we calculate the total charge into or out of a capacitor over some time period T, as given by

$$q_{\text{C}} = \int_T i_{\text{C}}(t)\, dt, \tag{3.6}$$

we can see that these two requirements are contradictory.

[2]Note, the concept of impedance is generally used for sinusoidal steady-state circuit analysis, and calculating impedance in terms of $j\omega$ is strictly only applicable to circuits driven with a steady-state AC signal. While it is therefore releavant to the resonant Dickson converter presented here, this impedance notation would not be strictly applicable to regulating converters where there are no steady-state sinusoidal waveforms, and would need to be modified using complex frequency. However, we present these simpler impedance definitions as an educational tool to illustrate the motivation for split-phase control.

Specifically, these two conditions would require that the charge out of C_1 in Phase 1 and into C_1 in Phase 2 (i.e. $q_{C_1,\phi 1}$ and $q_{C_1,\phi 2}$, respectively), would have to satisfy the following set of equations

$$|q_{C_1,\phi 1}| = \int_0^{T_{SW}/2} \frac{2}{3} i_L(t)\, dt \tag{3.7}$$

$$|q_{C_1,\phi 2}| = \int_{T_{SW}/2}^{T_{SW}} \frac{1}{3} i_L(t)\, dt \tag{3.8}$$

$$|q_{C_1,\phi 1}| = |q_{C_1,\phi 2}| = q_0 \tag{3.9}$$

This set of solutions is unsolvable, as there is no way for the integration of *unequal* currents over *equal* time periods to result in the same total charge. This is the inherent reason why split-phase control is required, as we can see that in order for (3.7) to result in the same charge as (3.8), the integration limits must be taken over a *shorter* amount of time. This is equivalent to saying that when C_1 is directly connected to the switch-node, it should be allowed to conduct for a shorter amount of time than when it is connected in series with C_2. The control signals required to effect this are termed split-phase control.

If the converter is operated with equal two-phase operation, it will exhibit the waveforms shown in Fig. 3.3. Here, we are showing resonant operation, where the inductor and capacitor currents are half-wave resonant. This resonant frequency is a function of the effective impedance seen at the switch-node and the output inductance [38]. As previously described, the current through capacitor C_1 in Phase 1 will have a larger magnitude than the current in Phase 2 (and therefore a larger peak value, $I_{C_1,\phi 1}$, compared to $I_{C_1,\phi 2}$), and C_1 will therefore discharge by a larger amount. As charge balance *must* be satisfied, large current impulses will occur at the boundaries of Phase 2, in which charge is rapidly redistributed so that the total Phase 2 charge is equal and opposite to that of Phase 1. These large current pulses result in step discontinuities on the capacitor voltage waveform, v_{C_1}.

Stated equivalently, the charge defined by the area of the sinusoidal portion of i_{C_1} during Phase 1 will result in a larger capacitor peak-to-peak voltage ripple than in Phase 2, as the current during Phase 1 has a higher peak value. This will result in Phase 1 and Phase 2 having mis-matched peak-to-peak capacitor voltage ripples, as shown in Fig. 3.3. These mismatched voltage ripples result in rapid charge redistribution at the phase transition, and the capacitor therefore exhibits large step discontinuities to jump between the different voltage levels.

The impulse currents associated with hard-charging lead to large capacitor charge sharing losses, as well as increased component current stress and worsened electromagnetic interference (EMI) performance. Therefore, split-phase control is a very attractive technique to mitigate these effects.

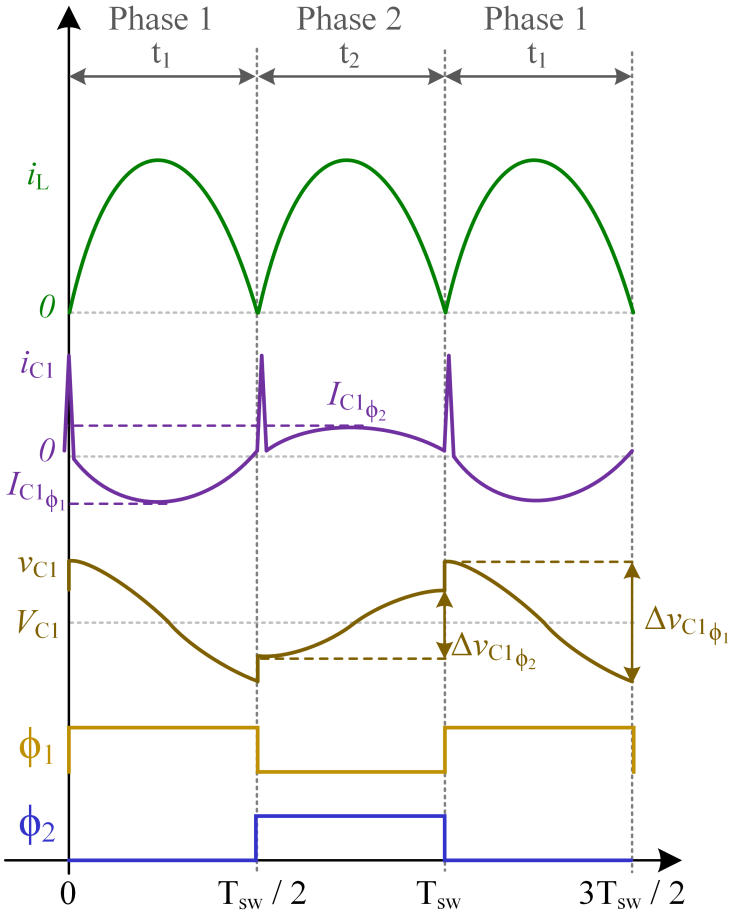


Figure 3.3: Operating waveforms for the 4-to-1 resonant Dickson converter, under two-phase control. The inductor current, i_L; C_1 capacitor current, i_{C_1}, and voltage, v_{C_1}; and phase control signals, ϕ_1 and ϕ_2 are illustrated.

3.2 Soft-Charged Split-Phase Resonant Dickson Converter Operation

Even-N resonant Dickson converters can be operated with split-phase control in order to softly charge all flying capacitors. To do this, each main phase is *split* into two separate sub-phases. Certain capacitors can then be added or removed from the switch-capacitor network in a staggered manner in order to ensure that they do not over-charge or discharge. Fig. 3.4 shows a schematic drawing of a 4-to-1 resonant Dickson converter operated with split-phase control. The gate signals labeled ϕ_{1a} and ϕ_{2a} will be ON for only a portion of ϕ_1 and ϕ_2.

Fig. 3.5 shows the simplified per-phase equivalent circuits when operating with split-phase

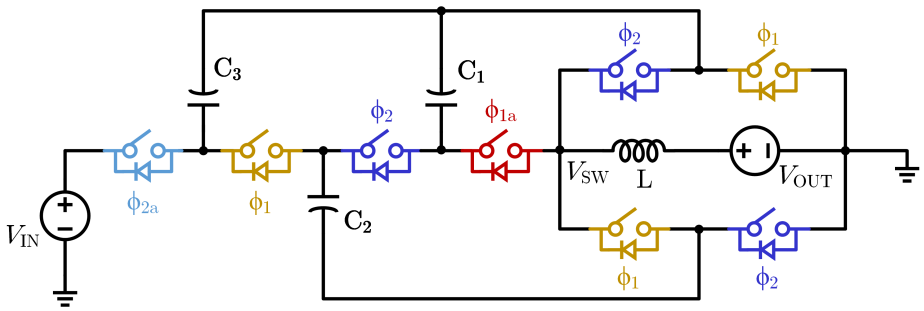


Figure 3.4: Schematic drawing of the 4-to-1 resonant Dickson converter, operated with split-phase gate signals, ϕ_{1a}, ϕ_{1b}, ϕ_{2a}, and ϕ_{2b}.

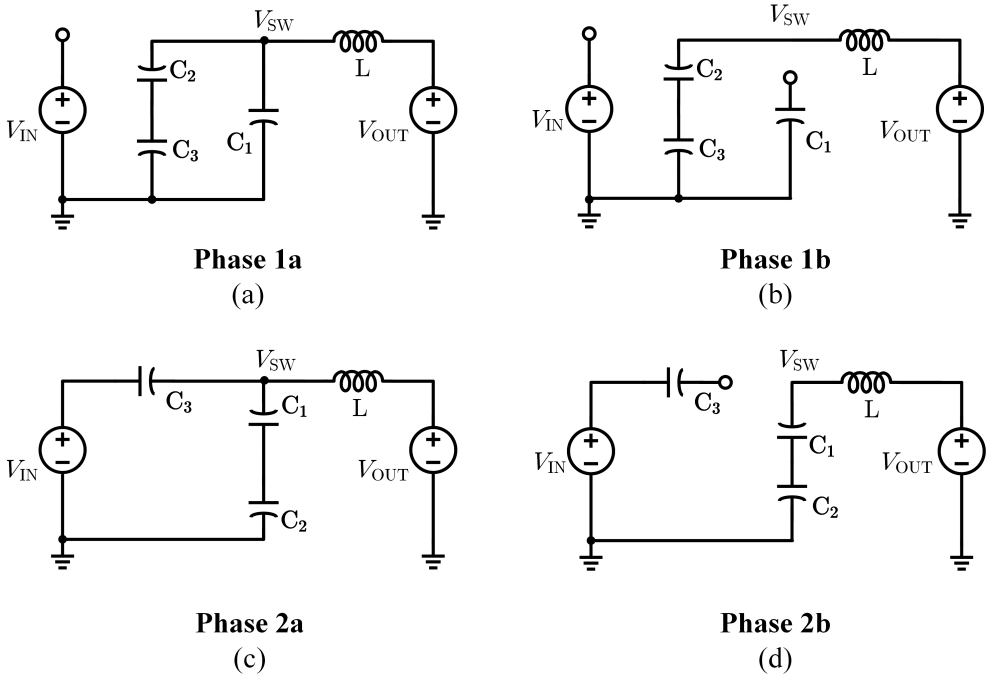


Figure 3.5: Simplified Phase 1a, Phase 1b, Phase 2a, and Phase 2b equivalent circuits for the 4-to-1 resonant Dickson converter.

control. The Phase 1a and Phase 2a configurations in Fig. 3.5a and Fig. 3.5c correspond to Phase 1 and Phase 2 in Fig. 3.2, in which all capacitors are connected. In addition, the time duration of Phase 1a and 1b (or Phase 2a and 2b) together is equal to the time duration of the two-phase Phase 1 (or Phase 2). As discussed previously, when C_1 is connected directly to the switch-node (i.e. not in series with another capacitor), it should only be allowed to conduct for a portion of the total Phase 1 duration to ensure that it does not over-discharge. Phase 1a corresponds to the time duration where C_1 is connected, while Phase 1b corresponds to the time duration where it is disconnected, as shown in Fig. 3.5b. C_3 experiences similar behavior as C_1, as it also moves from a series-connected branch to a single-connected branch over the course of a single switching period. Therefore, C_3 should only be allowed to conduct for a portion of Phase 2, and is disconnected during Phase 2b as shown in Fig. 3.5d. Capacitor C_2 is always series-connected with another capacitor, and sees the same branch impedance during both phases. It can therefore remain connected to switch-node for the entire duration of Phase 1 and Phase 2.

The operating waveforms for the 4-to-1 resonant Dickson converter under split-phase control are shown in Fig. 3.6. The capacitor current, i_{C_1}, does not have large impulse currents any longer. While the current is discontinuous, this does not have any impact on the soft-charging capability of the capacitor. In addition, the capacitor voltage, v_{C_1}, is smooth, without any large step discontinuities. The peak-to-peak capacitor ripple voltages $\Delta v_{C_1,\phi 1}$ and $\Delta v_{C_1,\phi 2}$ are also equal, signifying that Phase 1 and Phase 2 discharge and charge C_1 by an equal amount, without requiring additional pulsed charge transfer at the phase transitions in order to satisfy charge-balance.

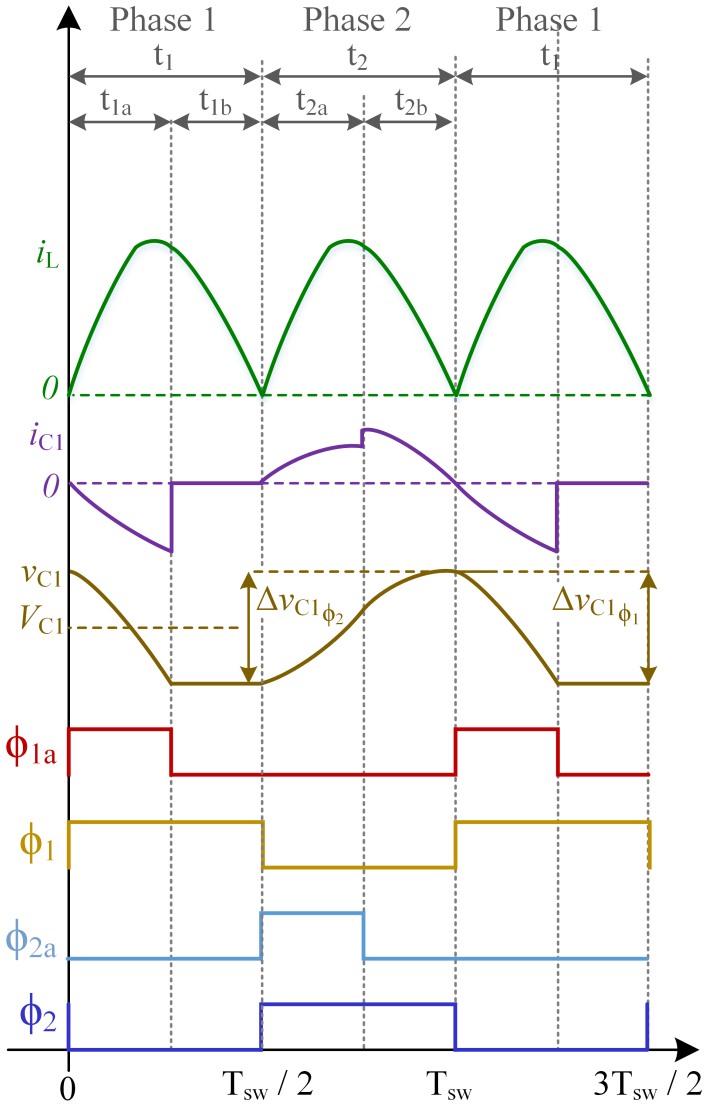


Figure 3.6: Operating waveforms for the 4-to-1 resonant Dickson converter, under split-phase control. The inductor current, i_L; C_1 capacitor current, i_{C_1}, and voltage, v_{C_1}; and phase control signals, ϕ_{1a}, ϕ_{1b}, ϕ_{2a}, and ϕ_{2b} are illustrated.

3.3 Split-Phase Timing Calculation

While the motivation for split-phase switching can easily be understood using basic circuit analysis techniques, actually calculating the time these split-phase capacitors should remain connected to the overall switch-capacitor network can be much more complex. These time durations also depend heavily on assumptions made about the inductor (and therefore capacitor) currents, as will be shown in Section 4.4. Specifically, whether one assumes a constant inductor current, a triangular inductor current, or a sinusoidal current can significantly change the calculated a and b sub-phase durations. Furthermore, changing the order of the a and b phases in the switching sequence can also have an effect on the required split-phase timings.

The original demonstration of split-phase control [29] operated the Dickson converter far above resonance, so that the inductor current could be considered constant. Under this assumption, the split-phase time durations can be sized proportional to the amount of charge delivered to the load during each sub-phase. General N-level split-phase time durations for odd- and even-N single-ended Dickson converters are tabulated in [22], assuming a constant output current[3]. A full analysis of split-phase time durations for both resonant (i.e. large current ripple) and above-resonant operation was also carried out for both even- and odd-N single-ended Dickson converters in [38]. For reference, calculated split-phase timings derived in that work are repeated here in Table 3.1 for even-N Dickson converters, both for above-resonant (i.e. small ripple) and resonant operation.

Table 3.1: Calculated split-phase timings for the hybrid even-N single-ended Dickson topology for small ripple and resonant operation, from [38].

		Small Ripple	Resonant
Even-N	t_{1a}	$\frac{(N+2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N+2} \cdot cos^{-1}(\frac{-1}{N-1})\right]$
	t_{1b}	$\frac{(N-2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-2} \cdot cos^{-1}(\frac{1}{N+1})\right]$
	t_{2a}	$\frac{(N+2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N+2} \cdot cos^{-1}(\frac{-1}{N-1})\right]$
	t_{2b}	$\frac{(N-2)}{4N} \cdot T_{sw}$	$\sqrt{\frac{LC_0}{4}}\left[\sqrt{N-2} \cdot cos^{-1}(\frac{1}{N+1})\right]$

[3]While odd Dickson converters can be fully soft-charged with two-phase operation using specific capacitor sizing, other capacitor sizing schemes (such as all flying capacitors having the same capacitance) require three-phase split-phase operation [38].

Chapter 4

Effects of Split-Phase Sub-Phase Ordering

4.1 Introduction

One SC converter family that is of great interest for hybridization is the family of Dickson-derived converters, explored in more detail in [22]. Originally implemented as a pure SC converter [39, 40], the Dickson converter exhibits the theoretical minimum switch stress compared to other SC topologies [41, 42], allowing it to operate with very efficient switch utilization. However, achieving full soft-charging of all flying capacitors is non-trivial in Dickson-derived converters, requiring either multiple inductors (the number of which can scale with increasing conversion ratio) [13, 43–47]; specific capacitance ratios for the flying capacitors or the avoidance of specific odd or even conversion ratios [21, 22, 33, 48, 49]; or the use of more complex control schemes such as split-phase control [29] or N-phase clocking [50].

Split-phase control is a modified control scheme that introduces additional sub-phases to the conventional two-phase control scheme, so that certain capacitors are removed from or added to the switch-capacitor network at specific times in their charge and discharge cycles. Due to its generality regardless of flying capacitance values or conversion ratio, split-phase control has emerged as a prominent method to achieve soft-charging, and has been applied to other topologies besides the resonant Dickson converters presented in [29, 34, 35]. This includes a resonant Cockcroft-Walton converter [51], a regulating Dickson converter [36], the interleaved-input Dickson-variant in [11, 22, 37, 52], the dual inductor hybrid (DIH) converter [27, 28], and the symmetric dual inductor hybrid (SDIH) converter [30, 31]. Several of these topologies are also capable of regulation through the addition of free-wheeling phase intervals where one or more inductors are shorted to ground, as demonstrated in [36]. This has made them popular for high step-down point-of-load applications where the output voltage must be controlled to a specific value.

However, the exact implementation of split-phase control has several nuances, and the way in which capacitors are added or removed from the switch-capacitor network can have

significant implications for overall circuit operation. In the initial demonstration of split-phase control in [29], it was shown that the order of the main phases and sub-phases did not matter for achieving soft-charging, assuming ideal switches. However, the authors did acknowledge that certain phase orderings could result in negative switch blocking voltages at certain times during the switching period (potentially requiring the use of bidirectional switches). To avoid this, the initial hardware demonstration on a *step-down* Dickson converter in [29] *removed* certain capacitors from the switch-capacitor network partway through each main phase, rather than *inserting* them. This sub-phase ordering was also used in the regulating Dickson converter presented in [36]. However, in subsequent *step-up* Dickson converter implementations presented in [34,35], the split-phase capacitors were instead *inserted* into the switch-capacitor network. Although the authors of [34,35] discuss how this ordering results in the zero-voltage-switching turn-on of the split-phase switches, they do not fully justify the change in phase-ordering compared to the previous step-down works.

Split-phase control has also been applied with both capacitor-insertion and capacitor-removal ordering for other Dickson-derived topologies. In [27,28], a step-down DIH converter was operated with split-phase control so that capacitors were inserted partway through the main phases. However, this required the converter to operate under capacitor voltage ripple restrictions to avoid reverse-biasing the split-phase switches. To resolve this ripple limitation, an alternate split-phase ordering scheme wherein capacitors were removed from the switch-network (as was done in [29, 36]), was presented in [53], which allowed for operation with higher capacitor ripple.

However, a full analysis of the effects of split-phase ordering was not explored in any of the previous works, nor was an analytical methodology presented to determine the best phase order for step-up versus step-down operation, in terms of the switch stress and reverse-bias conditions. This chapter therefore extends previous work in [53] in order to provide a more rigorous analysis of the connection between split-phase sub-phase orderings and switch blocking voltages. The implications of phase-ordering on maximum capacitor voltage ripple, peak switch voltage stress, and switch reverse biasing are also discussed. We demonstrate that it is more optimal to operate step-up converters by *inserting* split-phase capacitors partway through each main phase, while it is more optimal to operate step-down converters by *removing* split-phase capacitors partway through each main phase. Operating under these guidelines avoids reverse-bias switch conduction, significantly increasing the achievable capacitor voltage ripple and subsequently improving passive utilization and power density.

4.1.1 Split-Phase Switching

First proposed in [29], split-phase switching can be used to ensure full soft-charging of all flying capacitors in Dickson-derived topologies. Here, soft-charging refers to the lossless charge redistribution of all flying capacitors during phase transitions, in which an inductive or controlled current source is placed in the capacitor charge/discharge path [3]. Doing so allows any voltage mismatch between capacitors to appear across the inductive load, rather than across switch or parasitic resistance where it would result in $C\Delta V^2$ losses.

While many hybrid SC converters can achieve full soft-charging through the use of one or more inductors at the low-side node [5], for many Dickson-type converters there can still be internal capacitor loops that do not contain these inductors, and therefore experience voltage mismatch. Split-phase control can then be used to ensure full soft-charging, by introducing sub-phases in which certain capacitors are periodically disconnected from the switch-network at an optimal time in their charge and discharge curve. This prevents these capacitors from charging or discharging beyond the amount required to ensure continuous capacitor voltages at phase transitions, resulting in no voltage mismatch.

In split-phase control, the standard two-phase circuit states (in which all capacitors are connected) are denoted as a phases, while the introduced sub-phases are denoted as b phases. The main phases, Phase 1 and Phase 2, are thus *split* into the sub-phases $[1a, 1b]$ and $[2a, 2b]$. While the analysis presented in [29] was restricted to a single-inductor resonant Dickson converter, the split-phase technique has been extended to various other Dickson derived converters, such as the interleaved-input Dickson-variant [11, 22, 37, 52], the dual inductor hybrid (DIH) converter [27,28,54], and the symmetric dual inductor hybrid (SDIH) converter [30, 31].

The corresponding phase-equivalent circuits for all of these topologies can be represented by simplified equivalent capacitor networks, as shown in Fig. 4.1. A defining characteristic of

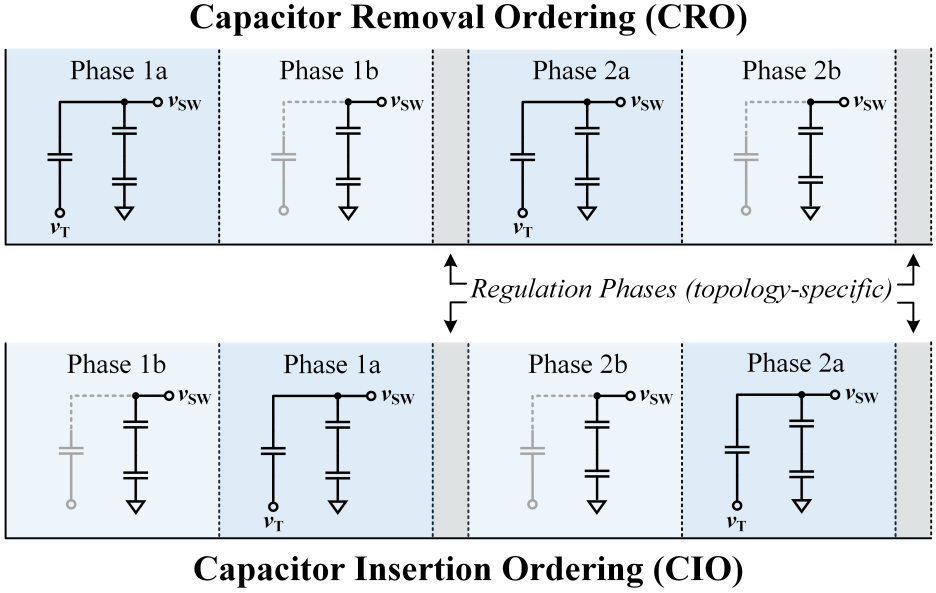


Figure 4.1: General illustration of sub-phase a and b capacitor network configurations for split-phase operation. Capacitor removal ordering (i.e. $a \rightarrow b$, top), and capacitor insertion ordering (i.e. $b \rightarrow a$, bottom) are illustrated. Optional regulation phases in which all capacitors are disconnected are shown in between Phase 1 and Phase 2.

a converter requiring split-phase is the presence of impedance-mismatched capacitor branches connected to a switch-node. For all the Dickson-derived converters discussed here, this impedance mismatch is due to the connection of one (or more) branches of series-connected capacitors, and one (or more) branches of single capacitors. In the a phases, the single capacitor branch shown in Fig. 4.1 is connected to both the main switch-capacitor network through the switch-node, v_{SW}, as well as either ground or the high-side input, generalized as some terminal voltage v_{T}. In the b phases, one node of this single-capacitor branch is left unconnected, so that the capacitor cannot undergo any charging or discharging.

As discussed in [29], complete soft-charging operation can be achieved regardless of the switching sequence, so that the sequences ($1a \rightarrow 1b \rightarrow 2a \rightarrow 2b$) and ($1b \rightarrow 1a \rightarrow 2b \rightarrow 2b$) both result in negligible capacitor charge sharing loss. To more easily compare phase-order configurations across a wide variety of Dickson-derived converter topologies, we therefore introduce a generalized terminology and apply it to both fixed-ratio and regulating converters. Fig. 4.1 shows the two possible phase orderings explored previously. Here, $a \rightarrow b$ ordering is termed capacitor removal ordering (CRO), as split-phase capacitors are connected at the start of each main phase and then removed at a later time. Conversely, $b \rightarrow a$ ordering is termed capacitor insertion ordering (CIO), as split-phase capacitors are connected into the network partway through each main phase. Regulation phases can also be inserted between Phase 1 and Phase 2 to allow the converter to achieve output voltages that differ from the native switch-capacitor network conversion ratio. This is done by disconnecting all capacitors from the network and connecting the output inductor(s) to ground (as done in [36]). Since all flying capacitors are disconnected during this time, schematics for these phases are omitted from Fig. 4.1 for simplicity.

While the ordering of phases does not impact the soft-charging capability of the converter, it does impact the blocking voltages seen by the switching devices. Specifically, $a \rightarrow b$ ordering versus $b \rightarrow a$ results in different blocking voltages seen by the switches undergoing split-phase transitions, potentially imposing large reverse voltages across these devices. As noted in [29], this can result in restrictions on switch implementations – such as requiring bidirectional switches – or limited capacitor voltage ripple such that the negative voltage across the switching devices is less than their threshold voltage, as done in [27, 28]. Furthermore, the phase ordering impacts the dc voltage across the flying capacitors, and thereby also affects the peak switch voltage seen on all devices, not just those undergoing split-phase transitions.

This work, therefore, seeks to provide a more rigorous analysis of split-phase switching in Dickson-derived converters, which includes these secondary effects of phase-ordering on converter operation. A general framework for selecting the correct phase ordering to maximize converter performance is presented, allowing for large capacitor ripple operation and subsequently greater passive component utilization and power density. As will be shown in the following sections, step-down converters should be operated under CRO control and step-up converters should be operated under CIO control in order to avoid reverse-biasing split-phase switches.

4.2 Resonant Dickson Converter

The effects of different split-phase ordering schemes can be intuitively demonstrated by considering an $N = 4$ resonant Dickson converter, as shown in Fig. 4.2. This topology is the original fixed-ratio hybridized Dickson topology [29], and does not include any freewheeling regulating phases. This analysis can also be applied to more complex Dickson-derived topologies, as will be described later.

Fig. 4.2a and Fig. 4.2b show the resonant Dickson operated as a step-down (4-to-1) and step-up (1-to-4) converter, respectively. Switches marked with an asterisk ($*$), i.e. S_5 and S_8, require split-phase switching, and will only conduct for a portion of their respective phase. For both configurations, all non-split-phase devices (i.e. S_1 - S_4, S_6, and S_7) are operated with the same control signals with 50% duty cycle. Devices S_1, S_3, and S_7 are ON during Phase 1, and S_2, S_4, and S_6 are ON during Phase 2. However, the control of the split-phase devices S_5 and S_8 can be modified by varying whether they are ON or OFF at the start of each main phase – that is, by changing the order of the a and b sub-phases.

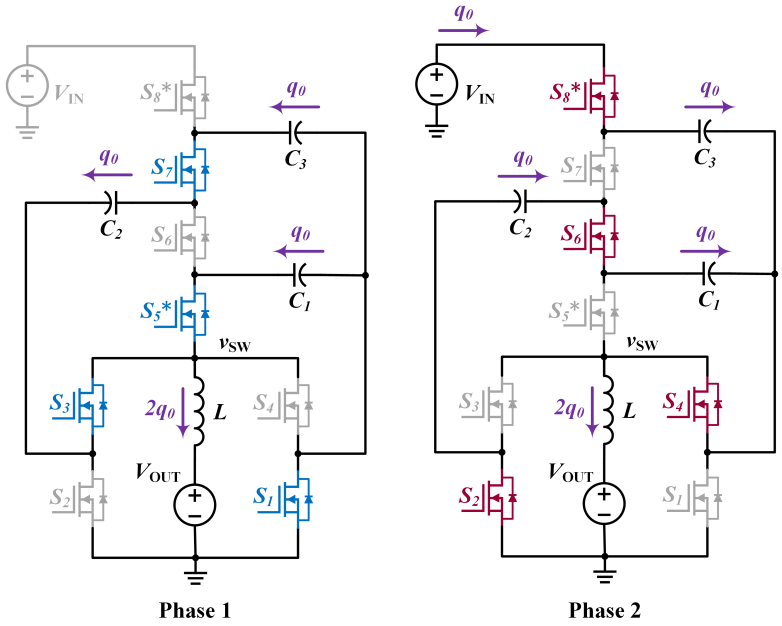
By performing charge-flow analysis as described in [1, 22], the charge through each capacitor and voltage source can be found in terms of the total charge through the high-side source, q_0. It is important to note that the charge through each capacitor found using this method is the total charge transferred during the *entirety* of Phase 1 (i.e. Phase 1a and 1b) or Phase 2 (i.e. Phase 2a and 2b). Split-phase operation then divides this total charge across the a and b phases[1]. When operated with split-phase control, the Dickson converter is commonly sized so that all capacitors are selected to be equal, such that $C_1 = C_2 = C_3 = C_0$. This results in symmetric split-phase timing between Phase 1 and Phase 2, as well as minimal impedance mismatch between the series-connected and single-capacitor branches shown in Fig. 4.1.[2] Because each capacitor experiences a total charge transfer of q_0 during each phase, equal capacitance sizing also results in equal voltage ripple $\Delta V_C = q_0/C_0$ across all capacitors.

From Fig. 4.2, it can be seen that the per-phase direction of charge flow in each capacitor is opposite for step-down versus step-up operation – that is, a capacitor that is charging in Phase 1 in a step-down converter will be discharging in the same phase in a step-up converter. This results in different ripple behavior across both the capacitors and the switch node, v_{SW}, which ultimately affects which sub-phase ordering will be optimal in terms of switch blocking voltages.

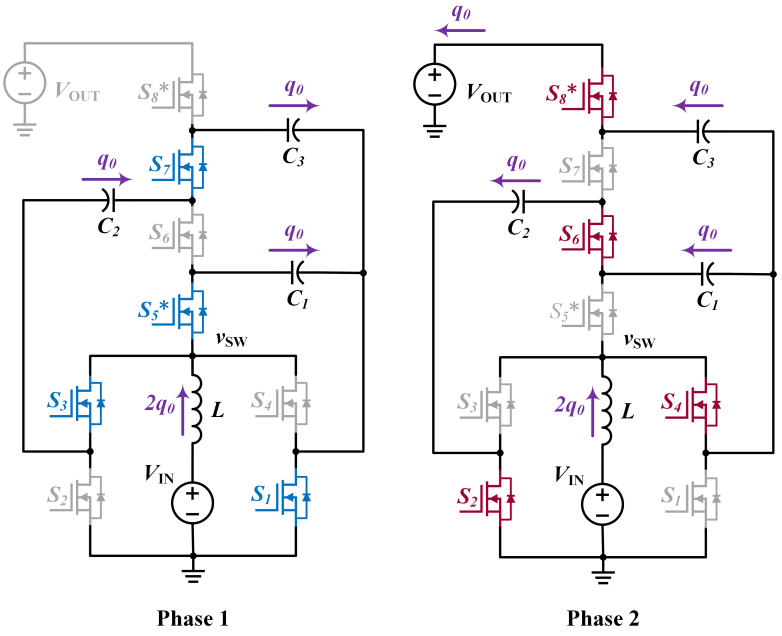
The charging and discharging behavior of each capacitor for both a step-down and step-up $N = 4$ resonant Dickson converter is presented in Table 4.1. While only Phase 1 operation

[1]The application of charge flow is done assuming soft-charged two-phase operation. In hard-charging operation, certain capacitors charge and discharge different amounts throughout each main phase, resulting in additional q_0 redistribution at phase transitions to maintain charge balance. This occurs through large impulse-type capacitor currents. Since split-phase control results in soft-charging, performing charge flow analysis on two-phase operation is simply a bookkeeping shortcut to determine the summed a and b charge for each overall Phase 1 or Phase 2.

[2]Different capacitance values could also be used, but this adds greater split-phase timing complexity in higher order networks.



(a) **Step-down operation**, where $V_{\text{HI}} = V_{\text{IN}}$ and $V_{\text{LO}} = V_{\text{OUT}}$.



(b) **Step-up operation**, where $V_{\text{HI}} = V_{\text{OUT}}$ and $V_{\text{LO}} = V_{\text{IN}}$.

Figure 4.2: Annotated charge flow diagram for the step-down and step-up configurations of an $N = 4$ resonant Dickson converter, with circuit states shown for Phase 1 and Phase 2. Switches S_5 and S_8 are only ON for a portion of their respective phases.

Table 4.1: Capacitor Voltages During Phase 1

	Phase 1 State	Initial Voltage	Final Voltage
		Step-Down	
C_1	Discharging	$V_{C1} + \frac{\Delta V_C}{2}$	$V_{C1} - \frac{\Delta V_C}{2}$
C_2	Charging	$V_{C2} - \frac{\Delta V_C}{2}$	$V_{C2} + \frac{\Delta V_C}{2}$
C_3	Discharging	$V_{C3} + \frac{\Delta V_C}{2}$	$V_{C3} - \frac{\Delta V_C}{2}$
		Step-Up	
C_1	Charging	$V_{C1} - \frac{\Delta V_C}{2}$	$V_{C1} + \frac{\Delta V_C}{2}$
C_2	Discharging	$V_{C2} + \frac{\Delta V_C}{2}$	$V_{C2} - \frac{\Delta V_C}{2}$
C_3	Charging	$V_{C3} - \frac{\Delta V_C}{2}$	$V_{C3} + \frac{\Delta V_C}{2}$

is tabulated for simplicity, similar trends can be found when analyzing Phase 2. Here, V_{C_i} denotes the mid-range voltage of capacitor C_i, i.e. the value mid-way between the minimum and maximum voltage seen across capacitor C_i (as defined in [22, 32])[3]. Each capacitor voltage then ripples around this mid-range voltage by $\pm\Delta V_C/2$, such that the minimum voltage across a capacitor will be $V_{C_i} - \Delta V_C/2$ and the maximum voltage will be $V_{C_i} + \Delta V_C/2$.

Table 4.1 then summarizes the initial and final voltages during Phase 1 for each capacitor for both step-down and step-up operation, and notes whether the capacitor is being charged or discharged. As discussed previously, the behavior of the converter under soft-charged split-phase operation can be described by the charge flow illustrated in Fig. 4.2. The capacitor peak-to-peak voltage ripple is given by the per-phase charge flow, $\Delta V_C = q_0/C_0$, and does not depend on the ordering of the sub-phases. However, the mid-range voltages V_{C_i} *do* change as a function of sub-phase ordering, and must be calculated accordingly. This process is shown in detail for the DIH converter in Section 4.3.2. Values for the capacitor mid-range voltages for an even-N Dickson converter are also provided in [38].

For an $N = 4$ resonant Dickson converter, capacitors C_1 and C_3 are operated with split-phase control. Fig. 4.3 shows the Phase 1 and Phase 2 equivalent circuits. The dotted lines connected to C_1 and C_3 represents the disconnection of these split-phase capacitors during the b phases of Phase 1 and Phase 2, respectively. During Phase 1, C_1 is directly connected to the switch node, v_{SW}, while in Phase 2, the series connection of C_1 and C_2 is connected across

[3]This mid-range voltage is often distinct from the time-averaged DC voltage across a capacitor, such as in multi-resonant hybrid SC topologies like the flying capacitor multilevel converter [32].

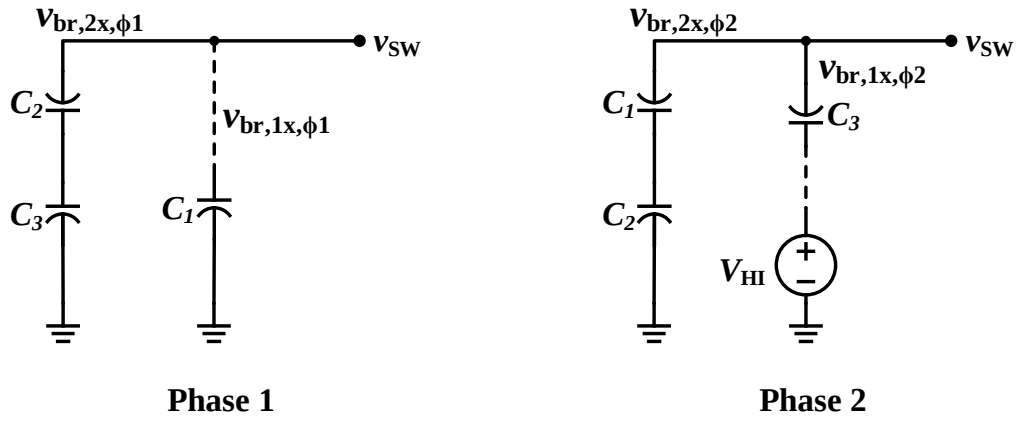


Figure 4.3: Phase 1 and Phase 2 equivalent circuits for the Dickson converter in Fig. 4.2a and Fig. 4.2b.

v_{SW}. Capacitor C_3 exhibits the opposite behavior, being series-connected to C_2 in Phase 1 and directly connected to v_{SW} in Phase 2. Capacitors C_1 and C_3 therefore are connected to the switch-node with different branch impedances during Phase 1 and Phase 2 (since the effective capacitance of the two series-connected capacitors is $C_0/2$ compared to C_0 for a single capacitor). However, as found in the charge flow analysis in Fig. 4.2, the charge that flows through C_1 and C_3 has the same magnitude in Phase 1 and Phase 2. Imposing the same total charge on C_1 and C_3 for both phases requires that they be connected to the switch-node for different time durations. However, in traditional two-phase Dickson converter operation, Phase 1 and Phase 2 are each on for 50% of the total switching period. This is the inherent reason split-phase operation is required in order to eliminate charge-sharing losses.

The time at which these split-phase capacitors should be connected or disconnected from the rest of the network can be determined by inspecting the branch voltages, $v_{br,1x}$ and $v_{br,2x}$, where the subscript 1x represents a single capacitor and 2x represents two capacitors connected in series. The general equations for the branch voltages during Phase 1 are given as

$$v_{br,1x,\phi_1}(t) = v_{C1}(t) \tag{4.1}$$
$$v_{br,2x\phi_1}(t) = v_{C3}(t) - v_{C2}(t), \tag{4.2}$$

where the ϕ_1 subscript denotes Phase 1 operation, as shown in Fig. 4.3.

The initial and final voltages of $v_{br,1x,\phi_1}$ and $v_{br,2x,\phi_1}$ in each phase can be found by appropriately summing the initial and final capacitor voltages given in Table 4.1, and are tabulated in Table 4.2. The polarity of the ripple terms (i.e. ΔV_C) is opposite for step-down and step-up operation, resulting in opposite-polarity ripple along each capacitor branch, and therefore the switch-node. That is, as a phase progresses in time, $v_{SW}(t)$ *decreases* by a total

Table 4.2: Branch Voltages During Phase 1

	Step-Down	**Step-Up**
Initial Voltages		
$v_{\text{br,1x},\phi_1}$	$V_{\text{C1}} + \frac{\Delta V_{\text{C}}}{2}$	$V_{\text{C1}} - \frac{\Delta V_{\text{C}}}{2}$
$v_{\text{br,2x},\phi_1}$	$\left(V_{\text{C3}} + \frac{\Delta V_{\text{C}}}{2}\right) - \left(V_{\text{C2}} - \frac{\Delta V_{\text{C}}}{2}\right)$	$\left(V_{\text{C3}} - \frac{\Delta V_{\text{C}}}{2}\right) - \left(V_{\text{C2}} + \frac{\Delta V_{\text{C}}}{2}\right)$
Final Voltages		
$v_{\text{br,1x},\phi_1}$	$V_{\text{C1}} - \frac{\Delta V_{\text{C}}}{2}$	$V_{\text{C1}} + \frac{\Delta V_{\text{C}}}{2}$
$v_{\text{br,2x},\phi_1}$	$\left(V_{\text{C3}} - \frac{\Delta V_{\text{C}}}{2}\right) - \left(V_{\text{C2}} + \frac{\Delta V_{\text{C}}}{2}\right)$	$\left(V_{\text{C3}} + \frac{\Delta V_{\text{C}}}{2}\right) - \left(V_{\text{C2}} - \frac{\Delta V_{\text{C}}}{2}\right)$
$\Delta v_{\text{br,1x},\phi_1}$	$-\Delta V_{\text{C}}$	$+\Delta V_{\text{C}}$
$\Delta v_{\text{br,2x},\phi_1}$	$-2\Delta V_{\text{C}}$	$+2\Delta V_{\text{C}}$
v_{SW}	Decreasing	Increasing

change of $2\Delta V_{\text{C}}$ for step-down operation, while it *increases* by a total change of $2\Delta V_{\text{C}}$ for step-up operation.

The effect of the capacitor branch voltages on the split-phase switch blocking voltage is demonstrated in Fig. 4.4 and Fig. 4.5. Fig. 4.4 shows a simplified schematic drawing of the Phase 1 circuit configuration, applicable to both step-up and step-down operation. The branch voltage $v_{\text{br,1x},\phi_1}$ is applied to the drain terminal of device S_5, denoted by v_{d5}. Similarly, the branch voltage $v_{\text{br,2x},\phi_1}$ is applied to the source terminal, denoted by v_{s5}, and is therefore equal to the switch-node voltage v_{SW} during the entirety of Phase 1. Switch S_5 undergoes split-phase switching, and is ON during Phase 1a and OFF during Phase 1b. When S_5 is ON, the voltage across it is 0 V (assuming an ideal switch), and $v_{\text{d5}} = v_{\text{s5}} = v_{\text{SW}}$, where v_{SW} is the switch-node voltage. However, when S_5 is turned OFF during Phase 1b, the branch voltages $v_{\text{br,1x},\phi_1}$ and $v_{\text{br,2x},\phi_1}$ deviate once C_1 is disconnected from the switch-node and remains at a fixed voltage, while the series-connected C_2 and C_3 branch follows v_{SW}. Because these branch voltages now deviate from each other, a voltage equal to $v_{\text{ds5}} = v_{\text{br,1x},\phi_1} - v_{\text{br,2x},\phi_1}$ is applied across S_5. The polarity of this voltage depends on *when* $v_{\text{br,1x},\phi_1}$ and $v_{\text{br,2x},\phi_1}$ are allowed to deviate, i.e. the ordering of the a and b phases.

Fig. 4.5 shows the Phase 1 branch voltage waveforms, $v_{\text{br,1x},\phi_1}$ and $v_{\text{br,2x},\phi_1}$, for both step-up and step-down converters using both phase orderings ($1a \rightarrow 1b$) and ($1b \rightarrow 1a$). As noted in Table 4.2 and labeled in Fig. 4.5, the branch containing C_1 only needs to transition

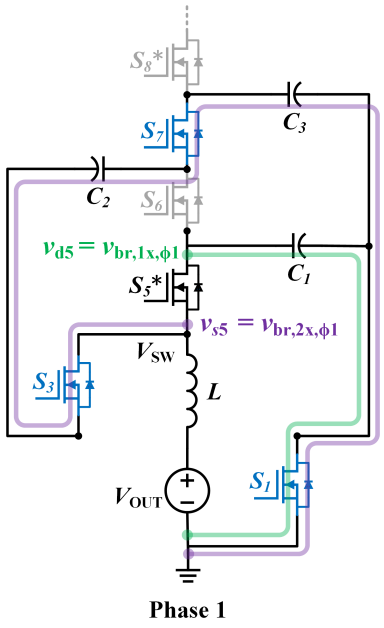


Figure 4.4: Phase 1 equivalent circuit, showing switch S_5 terminal voltages. The drain voltage of S_5, v_{d5}, equals the branch voltage $v_{br,1x,\phi_1}$. The source voltage of S_5, v_{s5}, equals the branch voltage $v_{br,2x,\phi_1} = v_{SW}$. S_5 is OFF during Phase 1b.

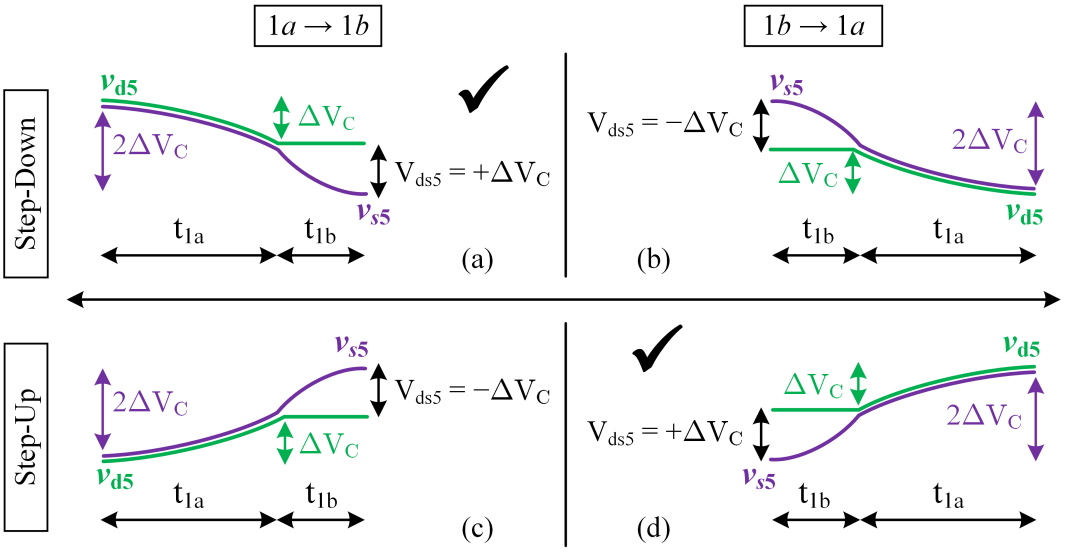


Figure 4.5: Phase 1 source and drain voltages for device S_5, as labeled in Fig. 4.4. Device S_5 is turned OFF for all b phases. The branch voltage behavior is shown for both $1a \rightarrow 1b$ and $1b \rightarrow 1a$ phase orderings for step-down and step-up operation. Note that $v_{s5} = v_{SW}$ for the entirety of Phase 1.

its voltage by a magnitude of ΔV_{C} during Phase 1, while the branch containing C_2 and C_3 undergoes a change of magnitude $2\Delta V_{\mathrm{C}}$. Since $v_{\mathrm{br,1x},\phi_1}$ must equal $v_{\mathrm{br,2x},\phi_1}$ during the a phase, $1a \rightarrow 1b$ ordering requires that $v_{\mathrm{br,1x},\phi_1}$ start at the same voltage as $v_{\mathrm{br,2x},\phi_1}$, while $1b \rightarrow 1a$ ordering requires that $v_{\mathrm{br,1x},\phi_1}$ end at the same voltage as $v_{\mathrm{br,2x},\phi_1}$. Allowing the branch voltages to deviate at the start of Phase 1 – as opposed to the end – impacts the blocking voltage experienced by device S_5, resulting in different optimal phase orderings for step-down and step-up conversion with respect to switch stress.

Step-Down Operation

During step-down operation, v_{SW} is monotonically decreasing across Phase 1, regardless of the a and b ordering. If $1a \rightarrow 1b$ ordering is used (as shown in Fig. 4.5a), when C_1 is disconnected at the split-phase transition, its voltage will remain at a higher value than that of the series connection of C_2 and C_3, since its voltage transition is only of magnitude ΔV_{C}. The voltage difference across switch S_5, $v_{\mathrm{ds5}} = v_{\mathrm{br,1x},\phi_1} - v_{\mathrm{br,2x},\phi_1}$, will therefore be positive during Phase 1b, resulting in a positive blocking voltage across the switch. This is the preferred behavior – as noted by the checkmark – since the body diode of the device will naturally be reverse-biased. The maximum blocking voltage for S_5 during Phase 1 is then given by $V_{\mathrm{ds5}} = +\Delta V_{\mathrm{C}}$.

However, if $1b \rightarrow 1a$ ordering is used (as shown in Fig. 4.5b), $v_{\mathrm{br,1x},\phi_1}$ must equal $v_{\mathrm{br,2x},\phi_1}$ at the end of Phase 1, and therefore the voltage of C_1 must start Phase 1 at a value ΔV_{C} lower than the peak voltage of $v_{\mathrm{br,2x},\phi_1}$. This means that $v_{\mathrm{ds5}} = v_{\mathrm{br,1x},\phi_1} - v_{\mathrm{br,2x},\phi_1}$ will be negative. The maximum (in magnitude) blocking voltage for S_5 during this time is then $V_{\mathrm{ds5}} = -\Delta V_{\mathrm{C}}$. This is undesirable, since this negative voltage can cause body-diode conduction in S_5. This essentially forces the converter to operate in the a phase configuration for a significant portion of Phase 1, and therefore into an operating condition similar to hard-charged two-phase operation.

Step-Up Operation

This behavior is reversed for step-up operation, where v_{SW} monotonically increases during Phase 1. Here, $1a \rightarrow 1b$ ordering (as shown in Fig. 4.5c) similarly requires $v_{\mathrm{br,1x},\phi_1} = v_{\mathrm{br,2x},\phi_1}$ at the beginning of the phase. However, when C_1 is disconnected, it will hold a fixed voltage ΔV_{C} less than the peak of $v_{\mathrm{br,2x},\phi_1}$. The voltage across S_5 will then be negative, thereby incurring reverse conduction and hard-charging losses if ΔV_{C} exceeds the reverse conduction threshold of the device. However, if $1b \rightarrow 1a$ is instead used (as shown in Fig. 4.5d), then $v_{\mathrm{br,1x},\phi_1} = v_{\mathrm{br,2x},\phi_1}$ at the end of the phase, and the voltage on C_1 will be fixed at a value greater than $v_{\mathrm{br,2x},\phi_1}$ for the duration of Phase 1b. This results in a positive voltage across S_5, preventing the device from undergoing reverse-biasing conditions as desired (as shown by the checkmark in Fig. 4.5.)

Summary

While the previous analysis was only described for Phase 1 operation, the switch-node behavior is equivalent for Phase 2 (i.e. monotonically decreasing for step-down operation and increasing for step-up operation). Therefore the same procedure holds for analyzing the behavior of the corresponding split-phase capacitor and switch, C_3 and S_8 (as shown in Fig. 4.2). In summary, if the switch-node voltage is decreasing, the split-phase capacitors (i.e. those that are only connected for part of each main phase) should be removed from the switch-capacitor network partway through that phase. If the switch-node voltage is increasing, however, the split-phase capacitors should be added to the switch-capacitor network partway through that phase. **This means that $a \rightarrow b$ ordering should be used for step-down converters, while $b \rightarrow a$ ordering should be used for step-up converters.**

4.3 Dual Inductor Hybrid Converter

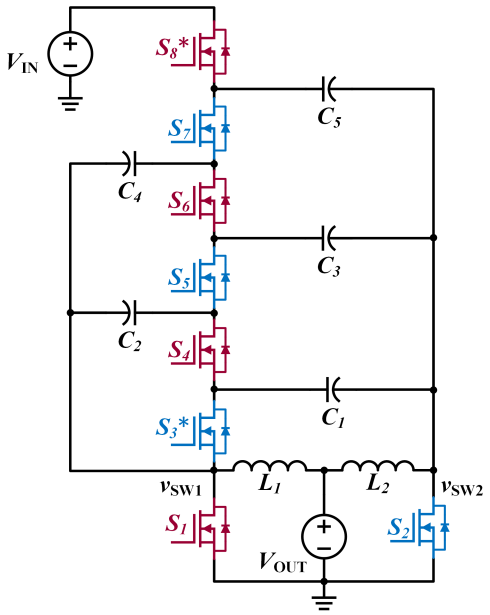


Figure 4.6: Schematic drawing of a dual inductor hybrid (DIH) converter with an $N = 6$ capacitor network, and an inherent 12:1 step-down ratio. Switches S_3 and S_8 require split-phase switching and are marked with an asterisk (*).

The effects of split-phase ordering can similarly be seen in the following analysis of the dual inductor hybrid (DIH) converter, proposed in [21, 27, 28]. While this converter can be operated with full soft-charging for odd conversion ratios using specific flying capacitor sizing [21, 27], all other cases require the use of split-phase control to achieve soft-charging

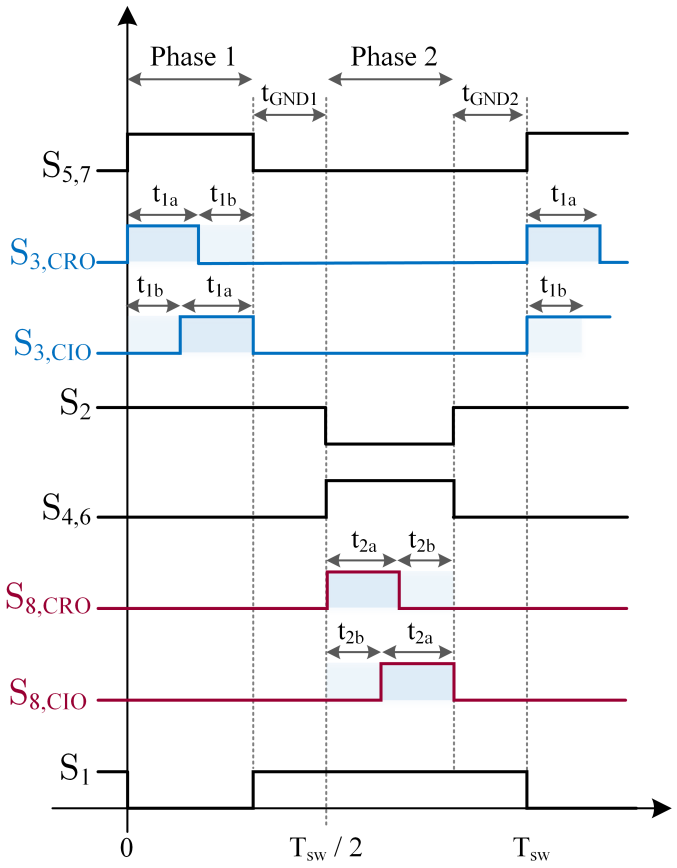


Figure 4.7: Gate signals for CRO and CIO control schemes applied to the DIH converter. The split-phase switches are controlled with $S_{3,\mathrm{CRO}}$ and $S_{5,\mathrm{CRO}}$ for CRO control and with $S_{3,\mathrm{CIO}}$ and $S_{5,\mathrm{CIO}}$ for CIO control. All other switches have identical gate signals for both control schemes.

for both odd and even conversion ratios [22]. Making all flying capacitors equal is a natural choice here, as the converter can then be operated in a symmetric manner where the time durations of Phases 1a and 2a (and Phases 1b and 2b) are the same, due to the symmetric LC networks presented to both switch-nodes.

Fig. 4.6 shows a schematic diagram of a step-down DIH converter with a switch-capacitor network that produces a 6-to-1 (or $N = 6$) conversion ratio at each switch node, v_{SW1} and v_{SW2}, and an overall 12-to-1 step-down at the output if operated with no additional regulating phases. This voltage can be further stepped down by the introduction of phases in which the switch-capacitor network is disconnected and the v_{SW} terminals of the two inductors are grounded.

Fig. 4.7 shows the corresponding switch gate signals for both CRO and CIO control. The times t_{xa} and t_{xb} represent the duration of the a and b phases, while t_{GNDx} represent the

duration of the regulation phases. As can be found using the analysis techniques presented in [25, 29], S_3 and S_8 must operate with split-phase timings. These switches therefore must turn ON or OFF partway through Phase 1 and Phase 2, depending on whether the split-phase capacitors C_1 and C_5 are being inserted into the network (CIO) or removed from it (CRO). Only the control signals for these switches will change between CRO and CIO control, while all other switches will operate with the same 50% duty cycle waveforms. Fig. 4.8 shows the equivalent circuit for each operating phase.

When operated with the regulation phases shown in Fig. 4.8(c) and (f), the output voltage of the converter can be regulated down to

$$V_{\mathrm{OUT}} = D \cdot \frac{V_{\mathrm{IN}}}{6} \tag{4.3}$$

by modifying the on-time of Phase 1 (and Phase 2) with respect to the switching period. Here, D is defined as

$$D = \frac{t_{1\mathrm{a}} + t_{1\mathrm{b}}}{T_{\mathrm{SW}}} = \frac{t_{2\mathrm{a}} + t_{2\mathrm{b}}}{T_{\mathrm{SW}}} \tag{4.4}$$

where $T_{\mathrm{SW}} = t_{1a} + t_{2a} + t_{\mathrm{GND}_1} + t_{2a} + t_{2b} + t_{\mathrm{GND}_2}$, as shown in Fig. 4.7. The duty cycle as defined can only operate at a maximum value of $D = 0.5$, as that results in Phase 1 ($t_{1\mathrm{a}} + t_{2\mathrm{a}}$) and Phase 2 ($t_{2\mathrm{a}} + t_{2\mathrm{b}}$) each having a time duration of half the overall switching period, $T_{\mathrm{SW}}/2$.

The effect of CRO versus CIO control on the split-phase switch blocking voltages – as well as on the blocking voltages of all converter switches in general – can now be explored. Because the DIH converter has primarily been used for large step-down conversion in point-of-load applications [21, 27, 28, 54], only step-down operation will be presented for simplicity.

For this analysis, it is assumed that the a and b phase times are independent of phase order, which is true assuming a small inductor current ripple. Section 4.4 shows that the a and b phase time durations can change as a function of phase orderings for regulated Dickson-derived converters in the presence of non-negligible current ripple. However, as discussed earlier, the capacitor peak-to-peak voltage ripples are invariant to both phase ordering and phase time durations for a given switching frequency. While the reverse-bias and peak switch blocking conditions *do* depend on sub-phase ordering, they *do not* change with changing a and b phase time durations, and therefore are still valid under large ripple conditions.

4.3.1 Charge Flow Analysis

In order to find the capacitor voltages at the start and end of each phase, charge flow analysis can be used, as was demonstrated for the $N = 4$ resonant Dickson converter example (Fig. 4.2). Fig. 4.9 presents this analysis for the step-down $N = 6$ DIH converter. Fig. 4.9 show the overall charge through the capacitors for the entirety of Phase 1 and Phase 2, respectively. From the annotated charge flow, it can be seen that all capacitors must conduct equal quantities of charge, q_0, over the combination of Phases [1a,1b] and Phases [2a,2b].

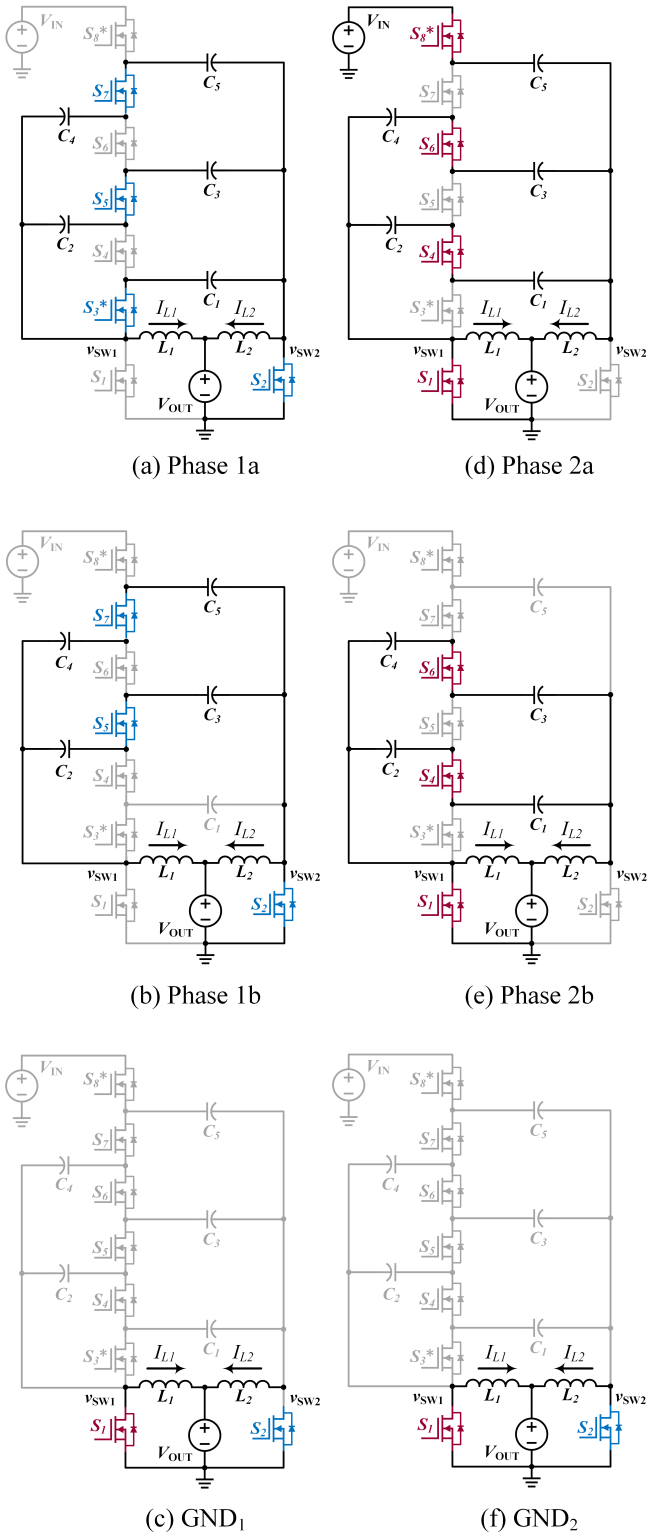


Figure 4.8: Phase equivalent circuit states for the step-down $N = 6$ DIH converter.

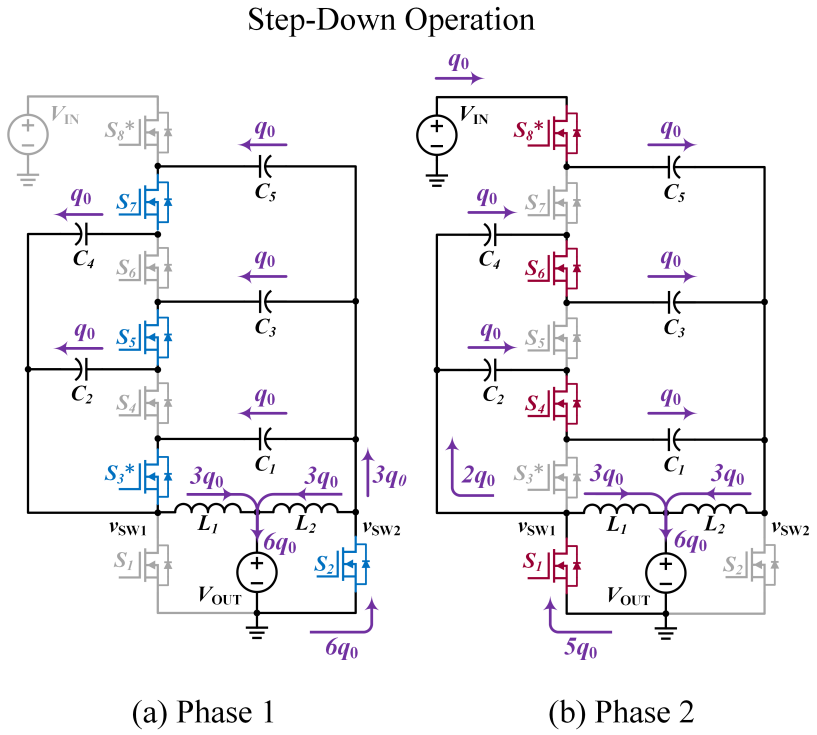


Figure 4.9: Charge flow for the step-down $N = 6$ DIH converter, for the entirety of (a) Phase 1 and (b) Phase 2. Soft-charging operation is assumed.

This total charge flow is split across the a and b sub-phases, with the split-phase capacitors only conducting during the a phase in which they are connected.

The charge flow depicted in Fig. 4.9 also represents the overall charge flow, including input and output terminals, for the DIH converter operating at $D = 0.5$ (i.e. with no regulating phases). Table 4.3 also summarizes the charge through each capacitor, inductor, and dc source for the DIH converter during Phase 1 and Phase 2. The capacitors do not conduct during the regulating GND phases, and therefore the total charge into and out of each capacitors is always q_0, even during regulating operation (i.e. $D < 0.5$). By summing the total output charge across Phase 1 and Phase 2 for the $D = 0.5$ case shown here, the same maximum conversion ratio as presented in (4.3) can be found as

$$\frac{V_{\text{OUT,max}}}{V_{\text{IN}}} = \frac{q_{\text{IN}}}{q_{\text{OUT}}} = \frac{1}{12}. \tag{4.5}$$

The conversion ratio can be regulated down from (4.5) by adding regulating phases, GND_1 and GND_2, in between Phase 1 and Phase 2. The overall operating sequence would then be $(1a \rightarrow 1b \rightarrow GND_1 \rightarrow 2a \rightarrow 2b \rightarrow GND_2)$ for CRO control and $(1b \rightarrow 1a \rightarrow GND_1 \rightarrow 2b \rightarrow 2a \rightarrow GND_2)$ for CIO control. During each regulating phase, the inductors

continue to conduct currents I_{L1} and I_{L2} to the output. The output voltage can then be regulated to (4.3) by decreasing the ON-time of Phases 1 and 2 with respect to the overall switching period – i.e. by reducing the conversion ratio D, as in a regular buck converter.

Table 4.3: Split-Phase Charge Flow

Charge	1a + 1b	2a + 2b
q_{IN}	0	$+q_0$
q_{C1}	$-q_0$	$+q_0$
q_{C2}	$+q_0$	$-q_0$
q_{C3}	$-q_0$	$+q_0$
q_{C4}	$+q_0$	$-q_0$
q_{C5}	$-q_0$	$+q_0$
q_{L1}	$+3q_0$	$+3q_0$
q_{L2}	$+3q_0$	$+3q_0$
q_{OUT}	$+6q_0$	$+6q_0$

If all capacitors have the same capacitance C_0 (so that the split-phase control timing is symmetric across Phase 1 and Phase 2), they will each see an identical voltage ripple of magnitude $\Delta V_C = q_0/C_0$. The polarity of this ripple depends on the direction of charge flow. Here, the left-side capacitor network (i.e. C_2 and C_4) is charged while the right-side capacitor network (i.e. C_1, C_3, and C_5) is discharged, and vice versa. Based on the direction of charge flow depicted in Fig. 4.9, the initial and final capacitor voltages in each phase can be found in a similar manner to that presented in Section 4.2. Table 4.4 gives expressions for the capacitor voltages at the start and end of Phase 1. The initial and final voltages of each capacitor in Phase 2 – while not shown here – are simply the final and initial voltages of each capacitor in Phase 1, as required by capacitor charge balance. Here, V_{C_i} indicates the DC mid-range voltage present on capacitor C_i. While each flying capacitor will see a voltage that swings from $V_{C_i} - \Delta V_C/2$ to $V_{C_i} + \Delta V_C/2$, it is important to recognize that V_{C_i} is itself a function of ΔV_C, as will be shown in Section 4.3.2. Furthermore, the peak-to-peak voltage ripple across each capacitor can be expressed in terms of the input or output current, as shown in (4.6). Therefore, both ΔV_C and the DC mid-range voltages V_{C_i} are functions of load [23]:

$$\Delta V_C = \frac{q_0}{C_0} = \frac{I_{IN}T}{C_0} = \frac{DI_{OUT}T}{N \cdot C_0}. \tag{4.6}$$

During Phase 1, C_1 operates as a split-phase capacitor. For step-down operation using CRO control, this means that it is connected during Phase 1a, and disconnected during Phase 1b. Its voltage must therefore transition entirely within Phase 1a, while all other

Table 4.4: Capacitor Voltages During Phase 1

	State	Initial Voltage	Final Voltage
C_1	Discharging	$V_{C1} + \frac{\Delta V_C}{2}$	$V_{C1} - \frac{\Delta V_C}{2}$
C_2	Charging	$V_{C2} - \frac{\Delta V_C}{2}$	$V_{C2} + \frac{\Delta V_C}{2}$
C_3	Discharging	$V_{C3} + \frac{\Delta V_C}{2}$	$V_{C3} - \frac{\Delta V_C}{2}$
C_4	Charging	$V_{C4} - \frac{\Delta V_C}{2}$	$V_{C4} + \frac{\Delta V_C}{2}$
C_5	Discharging	$V_{C5} + \frac{\Delta V_C}{2}$	$V_{C5} - \frac{\Delta V_C}{2}$

capacitors can transition their voltages over Phase 1a and Phase 1b. During Phase 2, C_5 operates as a split-phase capacitor, and will complete its voltage transition entirely within Phase 2a, while all other capacitors will transition their voltages over Phase 2a and Phase 2b. During the regulation phases, GND_1 and GND_2, all capacitors are disconnected, and hold a constant voltage.

4.3.2 Capacitor Mid-Range Voltages

The flying capacitor mid-range voltages can be found using the method presented in [22] for both CRO and CIO control, illustrating their dependence on split-phase ordering. In order to ensure soft-charging, the capacitor voltages must continuously satisfy all KVL loops in the circuit at the start and end of each phase. This ensures that there are no step discontinuities in capacitor voltage, which would lead to hard-charging [5]. These KVL loops can be written as a system of equations, allowing the capacitor mid-range voltages to be easily solved for. While the method presented in Section 4.2 can be used to determine when reverse bias conditions on the split-phase switches are present, the following analysis is carried out to further elucidate the dependency of capacitor mid-range voltages on the capacitor voltage ripple, ΔV_C.

When using this method, it is helpful to note the following:

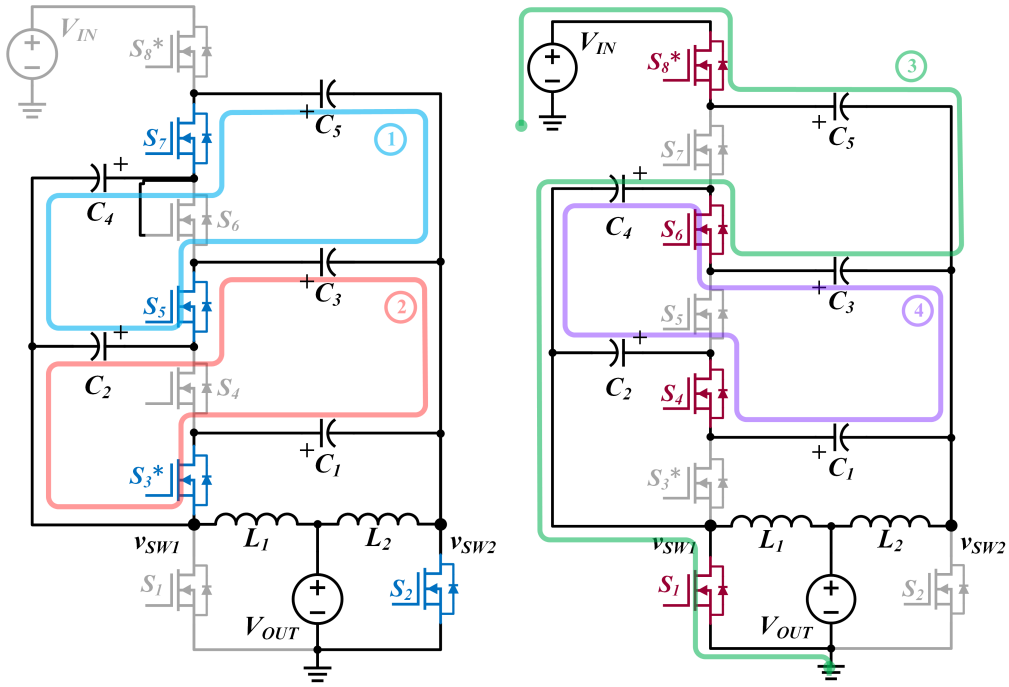
1. Expressions for the mid-range DC voltages should be found for sub-phases where all capacitor branches are connected, so that the capacitor relationships are fully represented. **This means that *a* phases should be used to draw KVL loops**. Equations from both Phase 1 and Phase 2 are needed.

2. The KVL loops should be written for either the **start or end of each main phase**—and not at the $a \rightarrow b$ or $b \rightarrow a$ transition—as the capacitor voltages will have just com-

pleted an entire voltage transition across all sub-phases at these times. This voltage swing can easily be found using charge flow, while the partial voltage swing at the split-phase transitions is both unnecessary and much more involved to calculate.

3. To fully define the system, **an additional constraint relating switch node voltages, v_{SW1} and v_{SW2}, is also needed**.

There are $N - 1 = 5$ capacitors for the $N = 6$ converter shown in Fig. 4.6. Therefore, five equations are required to solve for the five unknown capacitor mid-range voltages. Four of these equations (describing the capacitor voltage relationships) can be found using the KVL loops shown in Fig. 4.10, and the capacitor values at the start and end of each phase tabulated in Table 4.5.



(a) Phase 1 KVL Loops

(b) Phase 2 KVL Loops

Figure 4.10: KVL loops for determining mid-range DC voltages, in (a) Phase 1 and (b) Phase 2. For CRO control, the loops should be evaluated at the start of Phase 1a (i.e. the overall start of Phase 1). For CIO control, the loops should be evaluated at the end of Phase 1a (i.e. the overall end of Phase 1).

Table 4.5: Capacitor Voltages for KVL Loops in Fig. 4.10 and Fig. 4.12

	CRO				CIO			
Use for	$V_{C_i,CRO}$	$V_{ds,blocking,CRO}$	$V_{C_i,CRO}$	$V_{ds,blocking,CRO}$	$V_{ds,blocking,CIO}$	$V_{C_i,CIO}$	$V_{ds,blocking,CIO}$	$V_{C_i,CIO}$
Capacitor	$1a$ Start	$1b$ End	$2a$ Start	$2b$ End	$1b$ Start	$1a$ End	$2b$ Start	$2a$ End
C_1	$V_{C1}+\frac{\Delta V_C}{2}$	$V_{C1}-\frac{\Delta V_C}{2}$	$V_{C1}-\frac{\Delta V_C}{2}$	$V_{C1}+\frac{\Delta V_C}{2}$	$V_{C1}+\frac{\Delta V_C}{2}$	$V_{C1}-\frac{\Delta V_C}{2}$	$V_{C1}-\frac{\Delta V_C}{2}$	$V_{C1}+\frac{\Delta V_C}{2}$
C_2	$V_{C2}-\frac{\Delta V_C}{2}$	$V_{C2}+\frac{\Delta V_C}{2}$	$V_{C2}+\frac{\Delta V_C}{2}$	$V_{C2}-\frac{\Delta V_C}{2}$	$V_{C2}-\frac{\Delta V_C}{2}$	$V_{C2}+\frac{\Delta V_C}{2}$	$V_{C2}+\frac{\Delta V_C}{2}$	$V_{C2}-\frac{\Delta V_C}{2}$
C_3	$V_{C3}+\frac{\Delta V_C}{2}$	$V_{C3}-\frac{\Delta V_C}{2}$	$V_{C3}-\frac{\Delta V_C}{2}$	$V_{C3}+\frac{\Delta V_C}{2}$	$V_{C3}+\frac{\Delta V_C}{2}$	$V_{C3}-\frac{\Delta V_C}{2}$	$V_{C3}-\frac{\Delta V_C}{2}$	$V_{C3}+\frac{\Delta V_C}{2}$
C_4	$V_{C4}-\frac{\Delta V_C}{2}$	$V_{C4}+\frac{\Delta V_C}{2}$	$V_{C4}+\frac{\Delta V_C}{2}$	$V_{C4}-\frac{\Delta V_C}{2}$	$V_{C4}-\frac{\Delta V_C}{2}$	$V_{C4}+\frac{\Delta V_C}{2}$	$V_{C4}+\frac{\Delta V_C}{2}$	$V_{C4}-\frac{\Delta V_C}{2}$
C_5	$V_{C5}+\frac{\Delta V_C}{2}$	$V_{C5}-\frac{\Delta V_C}{2}$	$V_{C5}-\frac{\Delta V_C}{2}$	$V_{C5}+\frac{\Delta V_C}{2}$	$V_{C5}+\frac{\Delta V_C}{2}$	$V_{C5}-\frac{\Delta V_C}{2}$	$V_{C5}-\frac{\Delta V_C}{2}$	$V_{C5}+\frac{\Delta V_C}{2}$

*$V_{ds,blocking}$ refers to the voltage across the split-phase switches during the "b" phase of their active main phase.

CRO Control

For CRO control (i.e. $a \rightarrow b$), Phase 1 and Phase 2 both begin with a sub-phases, so the KVL loops should be written for capacitors at the *start* of Phase 1a and Phase 2a. Table 4.5 provides the voltage across all flying capacitors at these times, highlighted in gray for easy reference.

Using the loops labeled ① and ②, and the corresponding capacitor voltages in Table 4.5 the following expressions can be found:

$$-\left(V_{\mathrm{C2}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C3}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C4}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C5}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)=0 \tag{4.7}$$

$$\left(V_{\mathrm{C1}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C2}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C3}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)=0 \tag{4.8}$$

Similarly, loops ③ and ④ can be expressed as:

$$-\left(V_{\mathrm{C3}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C4}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C5}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)-V_{\mathrm{IN}}=0 \tag{4.9}$$

$$\left(V_{\mathrm{C1}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C2}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C3}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C4}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)=0 \tag{4.10}$$

The final equation required to define the system can be found by deriving a relationship between v_{SW1} and v_{SW2}. During Phase 1a, v_{SW1} is connected to the equivalent circuit shown in Fig. 4.11a, while v_{SW2} is connected to the equivalent circuit shown in Fig. 4.11b. As each capacitor has the same capacitance, C_0, these two capacitor networks present the same effective capacitance to each switch node (i.e. $C_0/2+C_0/2+C_0=2C_0$). These switch nodes are connected to equivalent inductors $L_1 = L_2 = L_0$ in the DIH converter [27], resulting in equal current ripple and better interleaving on the output. Therefore, during Phase 1 and Phase 2, equivalent capacitor networks are connected to equivalent switch nodes, and because all capacitors conduct equal charge through the same capacitance, the voltages at the switch-nodes v_{SW1} and v_{SW2} must follow the same trajectories during each of their respective phases, as discussed in Chapter 4 of [55]. This results in v_{SW1} and v_{SW2} operating with identical waveforms that are phase-shifted 180° with respect to each other.

The switch-node voltage v_{SW1} at the start of Phase 1a and the switch-node voltage v_{SW2} at the start of Phase 2a therefore must be equal, since these two points correspond to the peak of their respective waveforms, shifted 180° apart. These voltages can be found in terms of the capacitor mid-range voltages, as follows:

$$v_{\mathrm{SW1}}|_{\mathrm{1a,start}} = (V_{\mathrm{C1}}+\frac{\Delta V_{\mathrm{C}}}{2}) \tag{4.11}$$

$$v_{\mathrm{SW2}}|_{\mathrm{2a,start}} = (V_{\mathrm{C2}}+\frac{\Delta V_{\mathrm{C}}}{2})-(V_{C1}-\frac{\Delta V_{\mathrm{C}}}{2}) \tag{4.12}$$

By setting $v_{\mathrm{SW1}}|_{\mathrm{1a,start}} = v_{\mathrm{SW2}}|_{\mathrm{2a,start}}$, the last equation to fully define this system of equations can be found as:

$$2V_{\mathrm{C1}} - V_{\mathrm{C2}} = \frac{\Delta V_{\mathrm{C}}}{2} \tag{4.13}$$

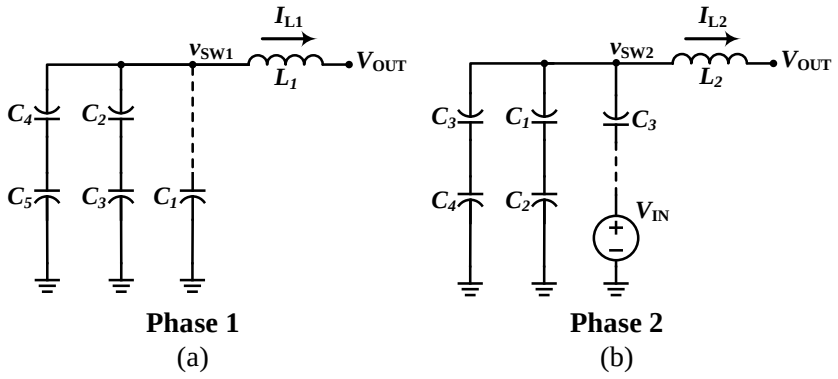


Figure 4.11: Equivalent circuits for the DIH converter in (a) Phase 1 and (b) Phase 2.

The system of equations defined by (4.7)-(4.10) and (4.13) can be expressed in matrix form, using the general form:

$$\mathbf{A_{(N-1)\times(N-1)}}\vec{V_{\mathrm{C}}} = \vec{b} \tag{4.14}$$

where $\vec{V_{\mathrm{C}}}$ is a vector of the capacitor mid-range voltages from C_1 to C_{N-1}, and N is the conversion-ratio of the capacitor network.

For the $N = 6$ DIH converter in Fig. 4.6, this matrix expression is equal to

$$\begin{bmatrix} 0 & -1 & 1 & 1 & -1 \\ 1 & 1 & -1 & 0 & 0 \\ 0 & 0 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & 0 \\ 2 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{\mathrm{C1}} \\ V_{\mathrm{C2}} \\ V_{\mathrm{C3}} \\ V_{\mathrm{C4}} \\ V_{\mathrm{C5}} \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\Delta V_{\mathrm{C}}}{2} \\ V_{\mathrm{IN}} - \frac{\Delta V_{\mathrm{C}}}{2} \\ 0 \\ \frac{\Delta V_{\mathrm{C}}}{2} \end{bmatrix} \tag{4.15}$$

This system can be solved for $\vec{V_C}$ to find the capacitor mid-range voltages:

$$\begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{bmatrix} = \begin{bmatrix} \frac{V_{IN}}{6} + \frac{2\Delta V_C}{6} \\ \frac{V_{IN}}{3} + \frac{\Delta V_C}{6} \\ \frac{V_{IN}}{2} \\ \frac{2V_{IN}}{3} - \frac{\Delta V_C}{6} \\ \frac{5V_{IN}}{6} - \frac{2\Delta V_C}{6} \end{bmatrix} \tag{4.16}$$

As shown in [22], this can be generalized for an even N-level converter with equal flying capacitance as:

$$V_{C_i,\text{CRO,even}} = i \cdot \frac{V_{IN}}{N} + \frac{\Delta V_C}{2} \cdot \frac{N-2i}{N} \tag{4.17}$$

Note that [22] did not discuss the effect of phase-ordering, and only $a \to b$ ordering for step-down operation was assumed.

CIO Control

A similar analysis can be carried out for CIO control (i.e. $1b \to 1a$), in which Phase 1 and Phase 2 now begin with b sub-phases. However, as previously noted, the KVL loops should be written 1) for the phases where all capacitors are connected (i.e. the a phases), and 2) at either the start or the end of the main phases. Therefore, the KVL loops for CIO should be analyzed at the *end* of Phase 1a and Phase 2a—that is, at the end of the full Phase 1 and Phase 2. These voltages are tabulated in Table 4.5 and highlighted in gray for easy reference.

Using the loops ① and ② in Fig. 4.10, and the corresponding capacitor voltages in Table 4.5 for CIO control, the following expressions can be found:

$$-\left(V_{C2} + \frac{\Delta V_C}{2}\right) + \left(V_{C3} - \frac{\Delta V_C}{2}\right) + \left(V_{C4} - \frac{\Delta V_C}{2}\right) - \left(V_{C5} + \frac{\Delta V_C}{2}\right) = 0 \tag{4.18}$$

$$\left(V_{C1} - \frac{\Delta V_C}{2}\right) + \left(V_{C2} + \frac{\Delta V_C}{2}\right) - \left(V_{C3} - \frac{\Delta V_C}{2}\right) = 0 \tag{4.19}$$

Using the loops ③ and ④, the Phase 2 KVL loops can be written as:

$$-\left(V_{\mathrm{C3}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C4}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C5}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)-V_{\mathrm{IN}}=0 \tag{4.20}$$

$$\left(V_{\mathrm{C1}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C2}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)-\left(V_{\mathrm{C3}}+\frac{\Delta V_{\mathrm{C}}}{2}\right)+\left(V_{\mathrm{C4}}-\frac{\Delta V_{\mathrm{C}}}{2}\right)=0 \tag{4.21}$$

Notice that (4.18)-(4.21) are similar to (4.7)-(4.10), except that the polarity of the ΔV_{C} term is opposite. An expression equating the switch node voltages is again needed to write a complete system of equations, and can also be written at the end of Phase 1a and Phase 2a. The last equation can then be given by:

$$2V_{\mathrm{C1}}-V_{\mathrm{C2}}=-\frac{\Delta V_{\mathrm{C}}}{2} \tag{4.22}$$

Equation (4.22) is also the same as (4.13), except for the opposite polarity of the ΔV_{C} term. Writing this system of equations in matrix form will yield the same $\mathbf{A}$ matrix as in (4.15). However, the $\vec{b}$ vector has the same magnitudes but opposite polarity for the ΔV_{C} term. $\vec{V_C}$ can then be solved for the $N=6$ case as:

$$\vec{V_{\mathrm{C}}}=\begin{bmatrix}\frac{V_{\mathrm{IN}}}{6}-\frac{2\Delta V_{\mathrm{C}}}{6}\\ \frac{V_{\mathrm{IN}}}{3}-\frac{\Delta V_{\mathrm{C}}}{6}\\ \frac{V_{\mathrm{IN}}}{2}\\ \frac{2V_{\mathrm{IN}}}{3}+\frac{\Delta V_{\mathrm{C}}}{6}\\ \frac{5V_{\mathrm{IN}}}{6}+\frac{2\Delta V_{\mathrm{C}}}{6}\end{bmatrix} \tag{4.23}$$

This can be generalized for an even N-level converter with equal flying capacitance as:

$$V_{\mathrm{C}_i,\mathrm{CIO,even}}=i\cdot\frac{V_{\mathrm{IN}}}{N}-\frac{\Delta V_{\mathrm{C}}}{2}\cdot\frac{N-2i}{N} \tag{4.24}$$

The general mid-range voltage for odd-level converters can be similarly found. Reference [22] presented an expression for the odd DIH converter (again assuming $a\rightarrow b$ ordering), given as:

$$V_{\mathrm{C}_i,\mathrm{CRO,odd}}=i\cdot\frac{V_{\mathrm{IN}}}{N}+\frac{\Delta V_{\mathrm{C}}}{2}\cdot\frac{N-2i+(-1)^i}{N+1}. \tag{4.25}$$

This can similarly be extended for CIO control as

$$V_{\mathrm{C}_i,\mathrm{CIO,odd}} = i \cdot \frac{V_{\mathrm{IN}}}{N} - \frac{\Delta V_{\mathrm{C}}}{2} \cdot \frac{N - 2i + (-1)^i}{N+1}, \tag{4.26}$$

where the polarity of the ΔV_{C} term is similarly reversed.

Comparing the capacitor mid-range voltages in (4.16) and (4.23), it can be seen that V_{C_1} and V_{C_2} have a higher voltage for CRO control, while V_{C_4} and V_{C_5} have a higher voltage for CIO control, assuming equal ΔV_{C}. However, V_{C_4} and V_{C_5} have a higher DC bias, and therefore their respective peak capacitor energies (equal to $\frac{1}{2}CV_{\mathrm{C,pk}}^2$), will dominate the overall converter capacitor energy. Thus, if the two control schemes are operating at the same ΔV_{C}, CRO will result in a lower capacitor energy storage requirement.

4.3.3 Split-Phase Switch Blocking Voltage

The split-phase switches S_3 and S_8 will experience a non-zero voltage during the b phases in which they are OFF. As described in Section 4.2, CIO control can result in a negative blocking voltage across the split-phase switches for step-down operation, which can impede desired operation. The split-phase switch blocking voltages during the b phases, $V_{\mathrm{ds3,1b}}$ and $V_{\mathrm{ds8,2b}}$, can be found using the method presented in Section 4.2. The capacitor KVL loops for each b phase are shown in Fig. 4.12. These can be used along with the capacitor voltages in Table 4.5 to solve for the blocking voltages across the split-phase switches during their respective b phases to determine if any undergo reverse bias conditions, and if so, under what conditions.

CRO Control

The voltage across S_3 and S_8 can now be found during their respective OFF times during the b phases using Fig. 4.12 and the voltages in Table 4.5, highlighted in blue. S_3 is ON during Phase 1a, and then turns OFF during Phase 1b. The voltage across S_3 will increase from 0 V (at the $1a \rightarrow 1b$ phase transition) to its maximum positive value over Phase 1b, as given by:

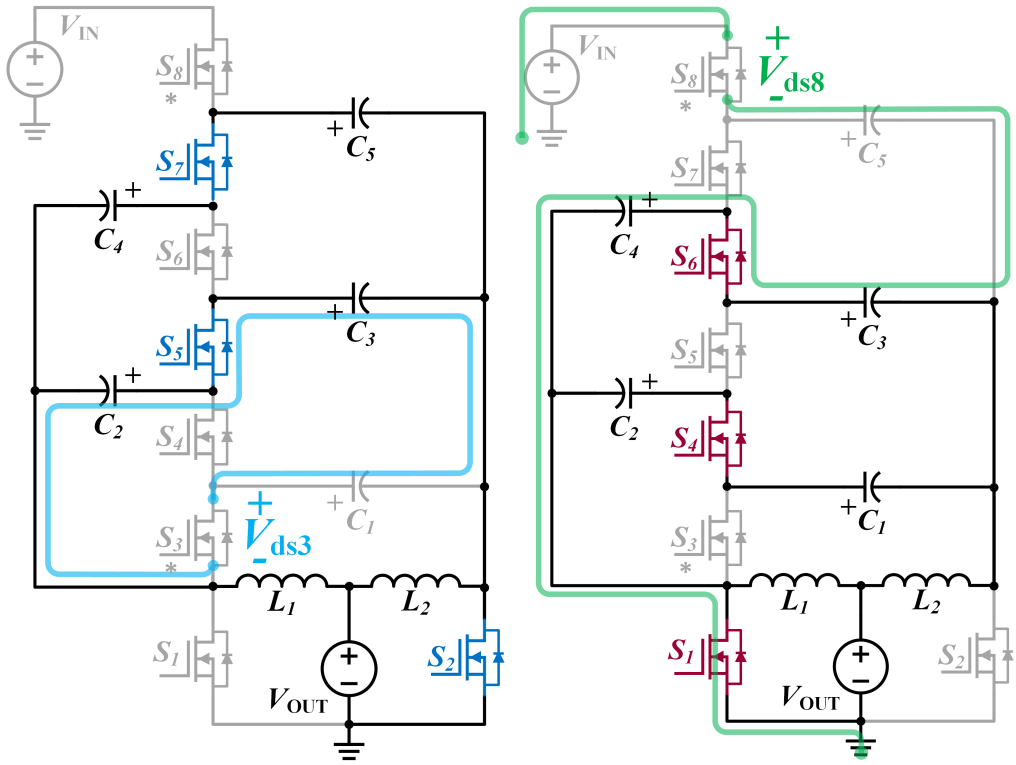
$$V_{\mathrm{ds3}}|_{\mathrm{1b,end}} = +\Delta V_{\mathrm{C}} \tag{4.27}$$

Similarly, S_8, is ON during Phase 2a and is then turned OFF at the start of Phase 2b. The voltage across S_8 then increases from 0 V to its maximum positive value over Phase 2b, given by:

$$V_{\mathrm{ds8}}|_{\mathrm{2b,end}} = +\Delta V_{\mathrm{C}} \tag{4.28}$$

CIO Control

Under CIO control, the Phase 1 split-phase switch, S_3, will also be OFF during Phase 1b. However, it experiences a negative blocking voltage during this time, which will slowly ramp



(a) Phase 1 v_{ds3} (b) Phase 2 v_{ds8}

Figure 4.12: Voltage loops to calculate split-phase switch blocking voltage for (a) Phase 1b and (b) Phase 2b. For CRO control, (a) should be evaluated at the *end* of Phase 1b (i.e. the overall end of Phase 1). For CIO control, (b) should be evaluated at the *start* of Phase 1b (i.e. the overall start of Phase 1).

up to 0 V at the $1a \rightarrow 1b$ phase transition when S_3 turns on. The most negative voltage will appear across S_3 at the start of Phase 1 (specifically, at the start of Phase 1b).

Using the capacitor voltages (highlighted in blue) in Table 4.5 and the KVL loops shown in Fig. 4.12, the minimum switch voltage across S_3 during Phase 1b can be found as:

$$V_{ds3}|_{1b,start} = -\Delta V_C \tag{4.29}$$

Similarly, the Phase 2 split-phase switch, S_8, will see its most negative voltage at the start of Phase 2 (at the start of Phase 2b). The voltage $V_{ds8,b}$ can be found as:

$$V_{ds8}|_{2b,start} - \Delta V_C \tag{4.30}$$

In a practical circuit implementation, either a bidirectional switch is needed or this negative voltage must be restricted to be less than the turn-on threshold of the body diode

of the device (0.7 V in Silicon and approximately 2 V in Gallium Nitride technologies). Otherwise, the body diode will turn on and the converter will be pushed into hard-charging operation. Because this voltage is a function of ΔV_{C}, the allowable capacitor voltage ripple is then limited by switch reverse threshold voltage. However, because the blocking voltage across the split-phase switches is positive during the b phases for CRO control, there is no such restriction on the allowable capacitor ripple, making this the preferred operation for high ripple designs.

4.3.4 Overall Switch Stress

Peak V_{ds} Switch Voltage

The method for finding capacitor mid-range voltages presented in the previous section can also be used to find the peak blocking voltage on each switch as a function of capacitor voltage ripple, ΔV_{C}. The mid-range voltages V_{C_i} were shown to vary depending on the a and b sub-phase ordering, and therefore the switch blocking voltages of *all* devices (not just split-phase switches) will also vary as a function of ordering. While the following analysis is presented only for the step-down case, a similar anlaysis could be done for the DIH converter operating in a step-up configuration.

Table 4.6 gives the peak V_{ds} voltage for each switch as a function of V_{IN} and ΔV_{C} for the $N = 6$ DIH converter shown in Fig. 4.6, for both CRO control and CIO control (assuming a fixed ΔV_{C}). In practice, CIO control will not be able to operate at as high a ΔV_{C} as CRO control due to the reverse-bias condtions on the split-phase switches. The lower switch V_{ds} values are highlighted in green. A lower switch V_{ds} is favorable, as this means lower voltage switches can be used, which has implications for better switch FOM and better efficiency [56, 57].

These switching devices can be grouped into sub-sets with shared characteristics, as noted below:

1. Only S_3 and S_8 exhibit higher peak switch stress operating under CRO control compared to CIO control. However, S_8 is connected to the input, so it may be desirable to size this for the input voltage, V_{IN}, for startup considerations [11, 37].

2. The voltage across S_5 and S_6 is constant across Phases $[2a, 2b]$ and Phases $[1a, 1b]$, respectively. While these switches do not see the capacitor voltage ripple on them, the DC switch blocking voltage is a function of the capacitor mid-range voltages, which *does* depend on the capacitor ripple, and decreases with increasing ΔV_{C} for CRO control. These switches, therefore, will actually see reduced voltage stress in high-ripple designs optimized for power density. Furthermore, S_5 and S_6 are "internal switch pairs," which will be repeated as the switch-capacitor network is extended for higher level counts. At high conversion ratios, these switches would therefore represent the majority of overall devices.

Table 4.6: $V_{\text{ds,pk}}$ for N = 6 DIH

Switch	CRO $V_{\text{ds,pk}}$	Time of Peak	Theoretical Value	Experimental Value
S_1	$\frac{1}{6}V_{\text{IN}} + \frac{5}{6}\Delta V_{\text{C}}$	$1a$ start	$\frac{1}{6}V_{\text{IN}} + \frac{7}{6}\Delta V_{\text{C}}$	$1b$ start
S_2	$\frac{1}{6}V_{\text{IN}} + \frac{5}{6}\Delta V_{\text{C}}$	$2a$ start	$\frac{1}{6}V_{\text{IN}} + \frac{7}{6}\Delta V_{\text{C}}$	$2b$ start
S_3	$\frac{1}{3}V_{\text{IN}} + \frac{4}{6}\Delta V_{\text{C}}$	$2a$ start	$\frac{1}{3}V_{\text{IN}} + \frac{2}{6}\Delta V_{\text{C}}$	$2b$ start
S_4	$\frac{1}{3}V_{\text{IN}} + \frac{1}{6}\Delta V_{\text{C}}$	$1a$ end ($1b$ start)	$\frac{1}{3}V_{\text{IN}} + \frac{2}{6}\Delta V_{\text{C}}$	$1b$ start *and* $1a$ end
S_5	$\frac{1}{3}V_{\text{IN}} - \frac{2}{6}\Delta V_{\text{C}}$	$2a$, $2b$	$\frac{1}{3}V_{\text{IN}} + \frac{2}{6}\Delta V_{\text{C}}$	$2b$, $2a$
S_6	$\frac{1}{3}V_{\text{IN}} - \frac{2}{6}\Delta V_{\text{C}}$	$1a$, $1b$	$\frac{1}{3}V_{\text{IN}} + \frac{2}{6}\Delta V_{\text{C}}$	$1b$, $1a$
S_7	$\frac{1}{3}V_{\text{IN}} + \frac{1}{6}\Delta V_{\text{C}}$	$2a$ start ($2b$ end)	$\frac{1}{3}V_{\text{IN}} + \frac{2}{6}\Delta V_{\text{C}}$	$2b$ start *and* $2a$ end
S_8	$\frac{1}{6}V_{\text{IN}} + \frac{5}{6}\Delta V_{\text{C}}$	$1b$ end, GND_1	$\frac{1}{6}V_{\text{IN}} + \frac{1}{6}\Delta V_{\text{C}}$	$1a$ end, GND_1

3. All other switches (i.e. $S_{4,7}$ and $S_{1,2}$) have a lower peak V_{ds} for CRO control than CIO control, and therefore a lower voltage stress (with the accompanying benefits in terms of loss and device selection which this entails).

Maximum Allowable Ripple

Maximum ripple limits for several Dickson-derived converters were characterized in [22], but without consideration of the effect of CRO versus CIO control on this limit. As discussed previously, the maximum ripple limit for step-down operation with CIO control results from the reverse-bias condition placed on the switches, where $V_{\text{ds,3}} = V_{\text{ds,8}} = -\Delta V_{\text{C}}$. This negative voltage across the switches must not exceed the threshold voltage of the device, otherwise the switch will turn on, resulting in improper operation. This limit on the peak-to-peak ripple for CIO control can be represented by:

$$\Delta_{\text{CIO,max}} = V_{\text{threshold}} \tag{4.31}$$

While this restriction is not present in CRO control for the step-down DIH converter, there is still a maximum ripple condition due to the requirement that *no* switch can enter

a reverse-bias condition, which puts a limit on the minimum switch V_{ds} voltage than can be appropriately handled. For the DIH converter, this limit is first reached for the base switches S_1 and S_2. The minimum blocking voltage seen by these switches occurs at the end of Phase 1b and Phase 2b, respectively. The KVL loop describing the blocking voltage across S_1 can be found using Fig. 4.12(a) and the values in Table 4.5 for CRO control, and is given by:

$$V_{\text{ds1}} + \left(V_{\text{C2}} + \frac{\Delta V_{\text{C}}}{2}\right) - \left(V_{\text{C3}} - \frac{\Delta V_{\text{C}}}{2}\right) = 0. \tag{4.32}$$

This results in a maximum allowable ripple of

$$\Delta_{\text{CRO,max}} = \frac{V_{\text{IN}}}{7}. \tag{4.33}$$

A similar equation can be written for S_2, and results in the same maximum allowable ripple, corroborating with results obtained in [22].

Total Switch Stress, $(V \cdot A)_{\text{norm}}$

The overall switch stress for the $N = 6$ DIH converter can be analyzed for both CRO control and CIO control, where the per-device switch stress is found by multiplying the peak switch blocking voltage by the rms switch current, i.e. $V_{\text{ds,pk}} \cdot I_{\text{ds,rms}}$. The switch stress for all devices can then be summed to obtain an overall switch performance metric, which commonly serves as a proxy for total switching loss or device area; that is, a lower overall VA rating can result in a more efficient or smaller volume converter [1, 42, 58, 59].

The peak switch voltages in Table 4.6 are functions of V_{IN} and ΔV_{C}. As the capacitor voltage ripple, V_{C}, depends on the output current I_{OUT}, switching frequency f_{SW}, and flying capacitance C_0—as given by the modified form of (4.6) repeated below

$$\Delta V_{\text{C}} = \frac{D I_{\text{OUT}}}{N f_{\text{SW}} C_0} \tag{4.34}$$

—the voltage ripple values in Table 4.6 can also be put in terms of output power (or output current) at the specified operating conditions, as given by:

$$P_{\text{OUT}} = V_{\text{OUT}} \cdot \left(\Delta V_{\text{C}} \cdot \frac{N f_{\text{SW}} C_0}{D}\right). \tag{4.35}$$

This means that the peak switch stress $V_{\text{ds,pk}}$ can also be expressed as a function of these fundamental operating conditions.

Next, the rms current for each switch can be found. Here, we assume zero ripple on the output inductors for simplicity, so that the output current and inductor currents are all constant. Then, the current through each switch will be a square wave with an on-time corresponding to the switch's conduction time. If the effect of inductor current ripple is

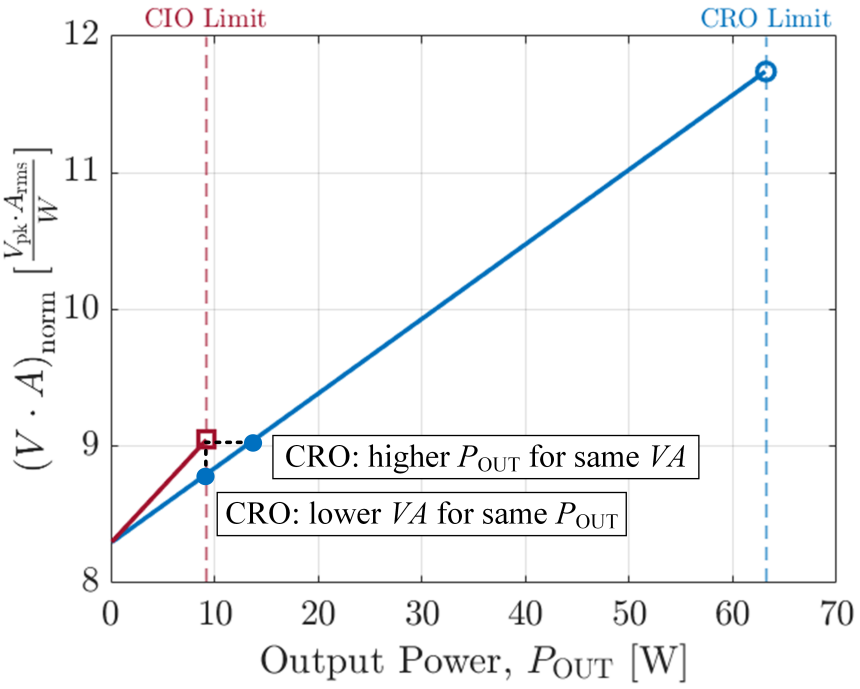


Figure 4.13: Maximum normalized switch stress $(V \cdot A)_{\text{norm}}$ voltage as a function of output power, P_{OUT}, for CRO and CIO timing schemes for step-down operation. The limit $\Delta_{\text{CRO,max}}$ is found assuming a maximum reverse blocking voltage of 1 V. The output power corresponding to the maximum capacitor voltage ripple conditions are illustrated by the CRO and CIO limit lines.

included, the overall switch stress values will change slightly due to the corresponding change in switch rms current. Fig. 4.13 plots the total switch stress of all devices against output power for both CRO and CIO control for the operating conditions given in Table 4.7, for step-down operation. The switch stress VA_{norm} is normalized by the corresponding output power, and given by

$$(V \cdot A)_{\text{norm}} = \frac{V_{\text{ds,rms}} I_{\text{ds,pk}}}{P_{\text{OUT}}}. \tag{4.36}$$

The maximum ripple limits defined in (4.31) and (4.33) for CIO and CRO control are also plotted in Fig. 4.13 for the conditions given in Table 4.7, with vertical dotted lines. For the same f_{SW}, C_0, and input/output conversion, CRO control is able to reach a much higher maximum power, making it more advantageous for high power density designs. Additionally, as shown by the annotations in Fig. 4.13, for the step-down DIH converter CRO control is able to operate with a lower total switch stress than CIO control for a given output power, and is therefore expected to result in lower overall switch losses. Similarly, for the same

Table 4.7: Operating Parameters

Parameter	Symbol	Value
Input voltage	V_{IN}	48 V
Output voltage	V_{OUT}	2 V
Switching frequency	f_{sw}	300 kHz
Flying capacitance	C_0	640 nF
Inductance	L_0	1 μH

overall switch stress, CRO control can achieve a higher maximum output power than CIO control, due to the lower peak voltages across the switches. Note that these results only hold for step-down operation, and would be reversed for step-up operation.

Furthermore, for the purpose of illustration, a threshold voltage $V_{\text{threshold}} = 1V$ is used to calculate the CIO limit. However, the CRO limit is calculated according to (4.32), assuming the maximum ripple occurs when $V_{\text{ds,1}}$ exactly equals 0 V, rather than allowing $V_{\text{ds,1}}$ to go slightly negative as limited by $V_{\text{threshold}}$. This limit was used as a more conservative estimate of maximum ripple, as in many cases it is not desirable to allow the switches to undergo any reverse biasing. However, this results in a somewhat undersized evaluation of the maximum output power capable with CRO control if all devices are allowed to withstand a reverse bias of $V_{\text{threshold}}$.

4.3.5 Experimental Validation

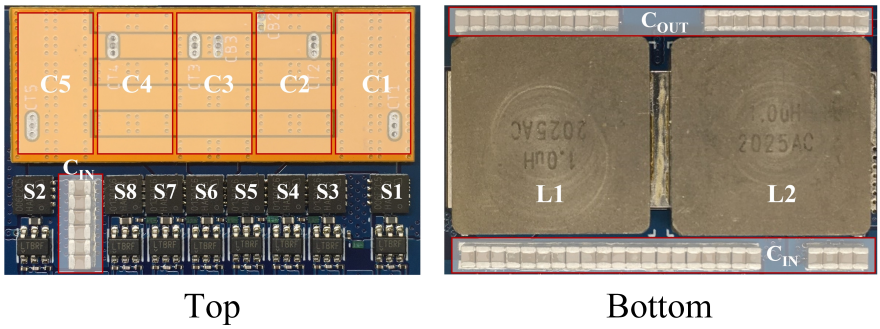


Figure 4.14: Annotated photograph of the 48 V input, $N = 6$ DIH converter hardware prototype. Dimensions: 23.2mm × 35.5mm × 5.7mm.

A hardware prototype of an $N = 6$ DIH converter designed for a 48 V input voltage was used to validate the previous analysis. Full details of the hardware prototype construction

Table 4.8: Power Stage Components

Part	Details	Part Number
S_1, S_2	0.65 mΩ, 25 V, Si	IQE006NE2LM5CGATMA1
$S_3 - S_8$	1.35 mΩ, 40 V, Si	IQE013N04LM6CGATMA1
$C_1 - C_5$	64 × 10 nF, 50 V, C0G	GRM1885C1H103JA01D
L_1, L_2	1 μH, 1.86 mΩ, 41 A	IHLP-6767DZ-11
C_{IN}	30 × 4.7 μF, 50 V, X5R	CL21A475KBQNNNE
C_{OUT}	22 × 4.7 μF, 50 V, X5R	CL21A475KBQNNNE
$U_1 - U_8$	80 V, 2.4A	LTC4440 gate driver

can be found in [53]. Fig. 4.14 shows an annotated photograph of the prototype, with dimensions labeled. The converter was tested at a 48-to-2 V step-down conversion, with a switching frequency of 300 kHz and a maximum output current of 26 A, and was designed to operate close to the maximum ripple condition using CRO control. The operating conditions are the same as those summarized in Table 4.7.

In order to approximate near zero-current ripple conditions and therefore better match the calculated split-phase durations derived in [29], relatively large inductors as compared to the flying capacitors (1 μH) were used. The converter could therefore achieve soft-charging of all flying capacitors using the idealized ratio of $t_{\text{xa}} : t_{\text{xb}} = 2 : 1$, where $t_{\text{1a}} = t_{\text{2a}} = t_{\text{a}}$ and $t_{\text{1b}} = t_{\text{2b}} = t_{\text{b}}$. However, the capacitors were sized with a flying capacitance of 640 nF such that the converter operated under high capacitor ripple conditions to better illustrate the benefits of CRO control. Table 4.7 summarizes the operating parameters used.

Because split-phase *a* and *b* sub-phase timings can vary with varying capacitance, Class I (C0G) flying capacitors were used for this prototype to better match the calculated theoretical values, while also providing improved stability with age, temperature and voltage [60,61]. Silicon MOSFETs were used instead of Gallium Nitride devices, due to their comparable figures-of-merit at the voltage range demonstrated here. Each switch was controlled by an independent level-shifting gate driver, with power delivered to all high-side switches using a conventional cascaded bootstrap. The power stage components are listed in Table 4.8. More details about the prototype construction and bootstrap design can also be found in [53].

At a switching frequency of 300 kHz, the maximum output power was limited by the flying capacitor voltage ripple, as discussed in Section 4.3.4. Fig. 4.15 shows the flying capacitor voltages when operating with a peak-to-peak ripple of 6.2 V at $V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 2$ V, and $I_{\text{OUT}} = 26$ A. Using (4.34), this capacitor voltage ripple theoretically corresponds to an output current of $I_{\text{OUT}} = 28.5$ A, assuming lossless operation where $P_{\text{IN}} = P_{\text{OUT}}$. At the actual converter operating efficiency of 93.1%, this corresponds to an output current of 26 A delivered to the load.

The converter was operated slightly under the calculated maximum ripple voltage of $V_{\text{IN}}/7 = 6.9$ V, in order to provide additional margin for V_{ds1} and V_{ds2} to remain above

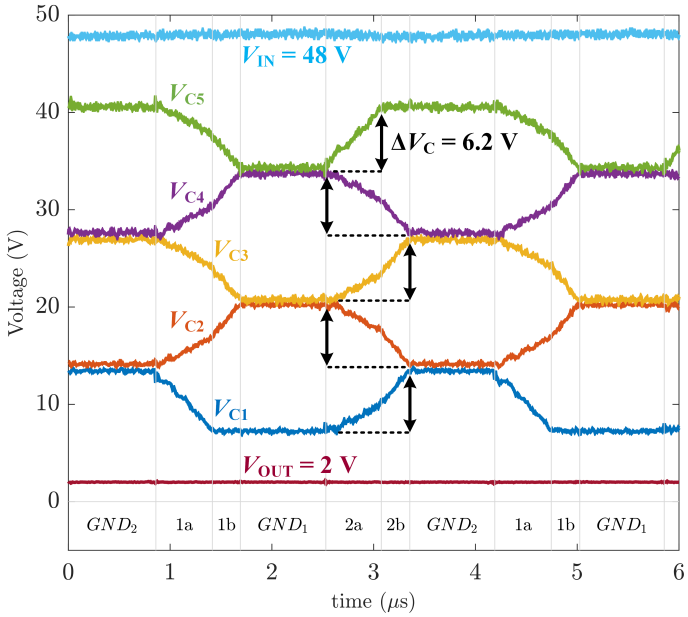


Figure 4.15: Measured flying capacitor waveforms at $V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 2$ V, $I_{\text{OUT}} = 26$ A, and $f_{\text{sw}} = 300$ kHz. The capacitors are operating near their theoretical maximum ripple, with a peak-to-peak voltage swing of 6.2 V across all flying capacitors.

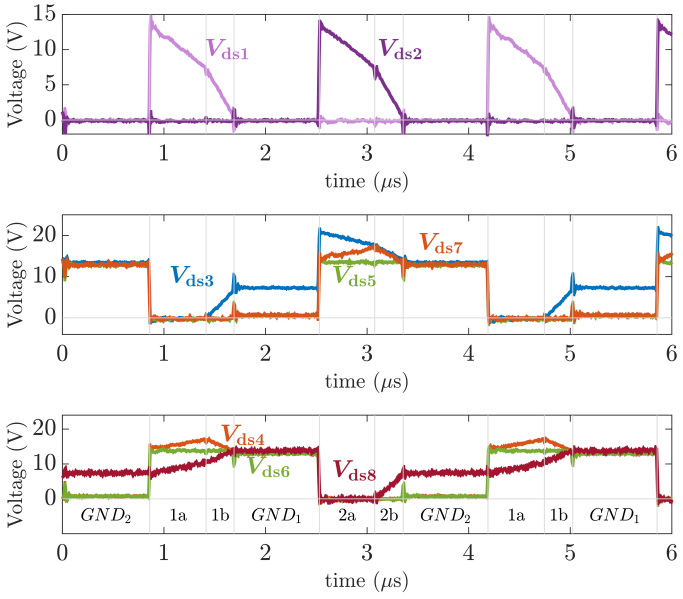


Figure 4.16: Measured switch V_{ds} waveforms at $V_{\text{IN}} = 48$ V, $V_{\text{OUT}} = 2$ V, $I_{\text{OUT}} = 26$ A, and $f_{\text{sw}} = 300$ kHz. All switches exhibit positive blocking voltages over the entire switch period, due to the use of CRO control.

0 V once accounting for parasitic voltage drops. However, this capacitor ripple voltage is significantly larger than the ripple demonstrated in [28], which used CIO control for step-down operation. The smooth capacitor voltages shown in Fig. 4.15 also validate the presence of complete soft-charging for all flying capacitors.

Fig. 4.16 shows the corresponding switch $V_{\rm ds}$ waveforms at this same operating condition. As expected, $V_{\rm ds,1}$ and $V_{\rm ds,2}$ almost reach 0 V at the end of Phase 1b and Phase 2b, respectively. The peak values of all switches—as well as the peak split-phase switch blocking voltages during their respective b phases—match well with the theoretical values given in Table 4.6 when evaluated at the observed operating condition of $\Delta V_{\rm C} = 6.2$ V, as shown in Table 4.9. In addition, these values occur at the predicted phase times given in Table 4.6 for CRO control. The capacitor mid-range voltages also match well with the theoretical values given in (4.16).

Table 4.9: Switch and Capacitor Voltages for $N = 6$ DIH

Switch Peak Voltages		
	Theoretical	Measured
$V_{\rm ds1,pk}$	13.2	13.3 V
$V_{\rm ds2,pk}$	13.2	13.3 V
$V_{\rm ds3,pk}$	20.1	20.6 V
$V_{\rm ds4,pk}$	17.0	17.0 V
$V_{\rm ds5,pk}$	13.9	13.8 V
$V_{\rm ds6,pk}$	13.9	13.8 V
$V_{\rm ds7,pk}$	17.0	17.2 V
$V_{\rm ds8,pk}$	13.2	13.5 V
Split-Phase Switch Blocking Voltages		
	Theoretical	Measured
$V_{\rm ds3}\vert_{\rm 1b,end}$	6.2	6.3
$V_{\rm ds8}\vert_{\rm 2b,end}$	6.2	6.3
Capacitor Mid-Range Voltages		
	Theoretical	Measured
$V_{\rm C1}$	10.1	10.3
$V_{\rm C2}$	17.0	17.2
$V_{\rm C3}$	24.0	23.8
$V_{\rm C4}$	31.0	31.0
$V_{\rm C5}$	37.9	37.6

*$\Delta = 6.2$ V, using CRO control

Efficiency measurements (excluding gate drive power losses) were also taken across load current, as shown in Fig. 4.17. At 300 kHz, the converter was able to achieve a maximum output power of 52 W (corresponding to $I_{\rm OUT} = 26$ A). This is slightly less than the theoret-

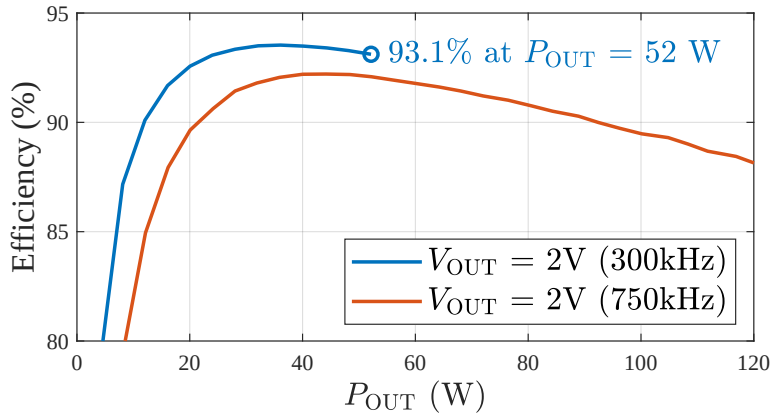


Figure 4.17: Measured efficiency curve for $V_{\mathrm{IN}} = 48$ V, $V_{\mathrm{OUT}} = 2$ V, at a switching frequency of $f_{\mathrm{SW}} = 300$ kHz and 750 kHz. The output power is limited by the maximum allowable fly capacitor voltage at 300 kHz, while the output power is thermally limited at 750 kHz.

ically calculated maximum power, due to converter losses. As previously described, in order to increase the maximum power at this input and output voltage, either f_{SW} or C_0 would need to be increased in order to increase the current at which S_1 and S_2 become reverse-biased. The efficiency curve at 750 kHz in Fig. 4.17 demonstrates this, as the converter is able to reach a maximum output power of 120 W. This operating condition is actually limited by the thermal performance of the converter, rather than the capacitor peak-to-peak voltage ripple.

4.4 Effect of Sub-Phase Ordering on Split-Phase Time Durations for the DIH Converter

For a Dickson-variant converter operating high above the natural resonance of its LC network, the inductor current(s) can be assumed to have small ripple. Under this condition, split-phase timings can be derived using the method presented in [29]. This assumption is reasonable for operation in deep continuous conduction mode, which is typical for a point-of-load converter such as DIH converter shown in Fig. 4.6.

It is still possible to achieve soft-charging even with large inductor current ripple, as described in [28] for triangular current ripple and in [31] for both large capacitor and inductor current ripple. However, the split-phase timings need to be appropriately adjusted to ensure that the required charge is delivered to the load in each sub-phase. The effect of different current ripple approximations for differeent split-phase orderings is demonstrated below for the DIH converter.

4.4.1 Constant Inductor Current ($\Delta i_{\mathrm{L}} = 0$)

The phase durations of each a and b phase can be expressed in terms of the effective capacitance, voltage swing, and per-phase current through the capacitor network. Assuming all flying capacitor have value C_0, the total effective capacitance seen by the non-grounded inductor can be found for each sub-phase as

$$C_{\mathrm{eff}\{1\mathrm{a},2\mathrm{a}\}} = \left(\frac{N-2}{2}\right)\left(\frac{C_0}{2}\right) + C_0 \tag{4.37}$$

$$C_{\mathrm{eff}\{1\mathrm{b},2\mathrm{b}\}} = \left(\frac{N-2}{2}\right)\left(\frac{C_0}{2}\right) \tag{4.38}$$

where N is the order of the capacitor network. Due to the symmetry of the converter topology, the time durations $t_{1\mathrm{a}}$ and $t_{1\mathrm{b}}$ of Phase 1a and 2a are equal, as are $t_{1\mathrm{b}}$ and $t_{2\mathrm{b}}$.

The current through the capacitor network in each phase will simply be the current through the non-grounded inductor. For example, as shown in Fig. 4.8, the capacitor network conducts a current I_{L1} in Phase 1a, while it conducts a current of I_{L2} in Phase 2a. The duration of each a and b phase can then be expressed in terms of (4.37) and (4.38), by rearranging the standard equation for current through a capacitor, $i_{\mathrm{C}} = C\frac{d}{dt}v_{\mathrm{C}}(t)$. Here, i_{C} represents the current through the entire active switch-capacitor network.

$$t_{i,\mathrm{a}} = \frac{C_{\mathrm{eff}_{i,\mathrm{a}}} \cdot \Delta V_{\mathrm{C}}}{I_{L_i}} \tag{4.39}$$

$$t_{i,\mathrm{b}} = \frac{C_{\mathrm{eff}_{i,\mathrm{b}}} \cdot \Delta V_{\mathrm{C}}}{I_{L_i}} \tag{4.40}$$

where i is the respective operating phase.

The relationship between the a and b phases for complete soft-charging can then be found using (4.37)-(4.40), assuming constant inductor current:

$$t_{i,\mathrm{a}} = \left(\frac{N+2}{N-2}\right) \cdot t_{i,\mathrm{b}} \tag{4.41}$$

For the specific case of the $N = 6$ converter shown in Fig. 4.6, the following expressions can be found for the Phase 1a and Phase 1b time durations:

$$t_{1\mathrm{a}} = \frac{2C_0 \cdot \Delta V_{\mathrm{C}}}{I_{L1}}, \tag{4.42}$$

$$t_{1\mathrm{b}} = \frac{C_0 \cdot \Delta V_{\mathrm{C}}}{I_{L1}}. \tag{4.43}$$

where $2C_0$ is the total effective capacitance seen by L_1 during Phase 1a, and C_0 is the remaining effective capacitance after C_1 has been disconnected during Phase 1b. Equation (4.41) simplifies to $t_{i,\mathrm{a}} = 2t_{i,\mathrm{b}}$. This matches the a and b phase timing used in [28], but with

reverse phase ordering. As noted previously, the sub-phase time durations do not depend on phase ordering under the small current ripple approximation, as I_{L1} is assumed to have the same value during Phase 1 as I_{L2} during Phase 2.

Fig. 4.18 shows a graphical illustration of why the phase ordering does not impact the calculated phase time durations. Here, we are only showing half of the total switching period, focusing on Phase 1 and its corresponding (optional) regulation phase, though this analysis also applies to Phase 2. As the current is assumed to be constant, the total charge delivered during t_a will be $q_a = t_a \cdot I_L$, independent of the phase ordering.

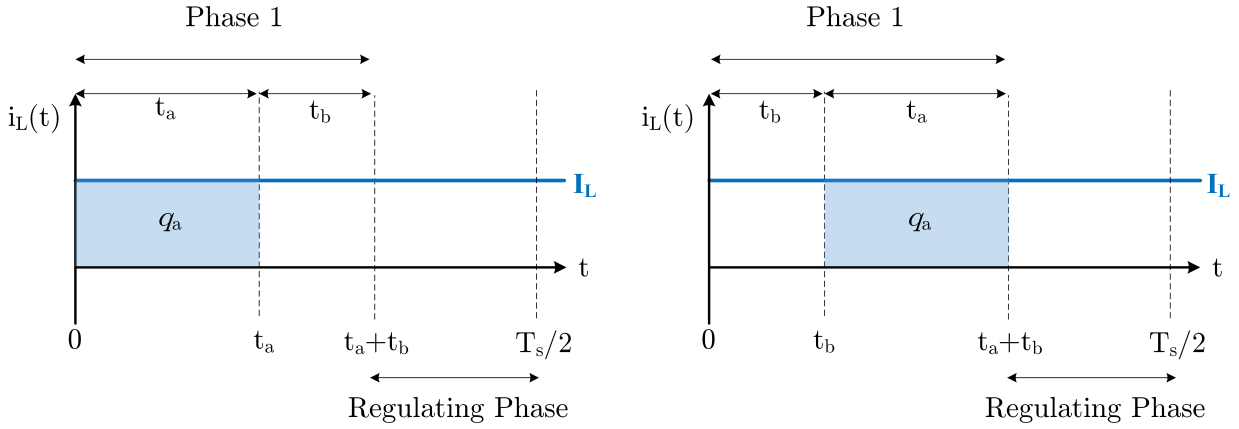


Figure 4.18: Calculation of Phase a charge assuming a constant current, I_L. Under this assumption, the ordering of the a and b sub-phases does not have an impacted on the calculated sub-phase timings.

4.4.2 Split-Phase Timing Analysis - Linear Current Ripple

If we now assume that the inductor(s) have some peak-to-peak triangular current ripple, Δi_L, centered around an average value I_{avg} which is equal to the constant value I_L from the previous example, we will see that the phase times are now dependent on sub-phase ordering as illustrated in Fig. 4.19 and Fig. 4.20.

Fig. 4.19 shows the case where CRO control is used, in the presence of a triangular inductor current. Fig. 4.19a shows what the equivalent charge accumulated during the a phase would be using the ideal timing t_a, which is calculated assuming a constant inductor current. Because the a phase starts at the minimum value of the inductor current, $I_{L,min}$, the calculated timing t_a is an *under-estimate* of the required time to deliver the required charge, $q_{a,ideal}$. Therefore, the a phase timing needs to be increased, as shown in Fig. 4.19b.

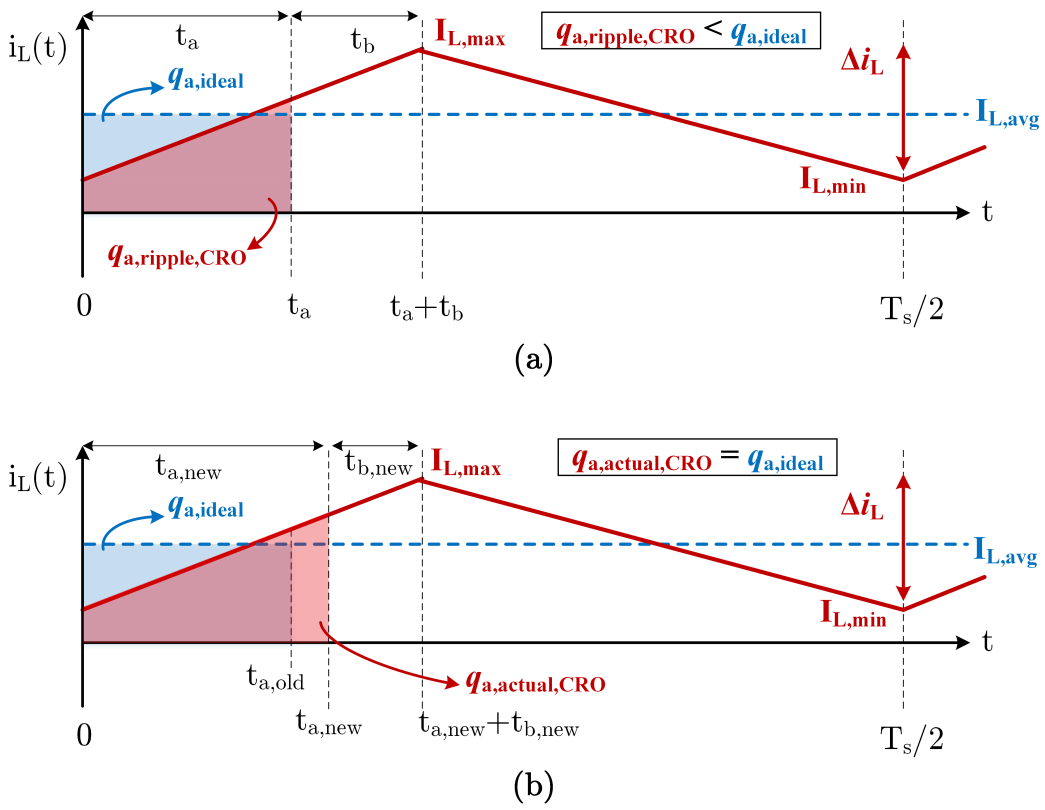


Figure 4.19: Required adjustments to t_a and t_b sub-phase timings for CRO ($a \rightarrow b$) ordering. If Phase 1 starts with an a sub-phase, the constant-current derived timings are an under-estimate of the required Phase 1a timing.

An equivalent analysis can be carried out for the case where CIO control is used in the presence of a triangular inductor current. Fig. 4.19a shows what the equivalent charge accumulated during the a phase would be using the ideal timing t_a. Now, because the a phase starts mid-way through Phase 1, and ends at the maximum value of the inductor current, $I_{L,max}$, the calculated timing t_a is an *over-estimate* of the require time to deliver the required charge, $q_{a,ideal}$. Therefore, the a phase timing needs to be decreased, as shown in Fig. 4.19b.

In [28], calculated values for $t_{a,new}$ were provided for the DIH converter operating with CIO control, using the following equations describing the inductor average and peak-to-peak ripple values in terms of converter operating parameters. As the DIH converter has two output inductors, the average current of a single inductor is given by

$$I_{L,avg} = \frac{I_{OUT}}{2}. \tag{4.44}$$

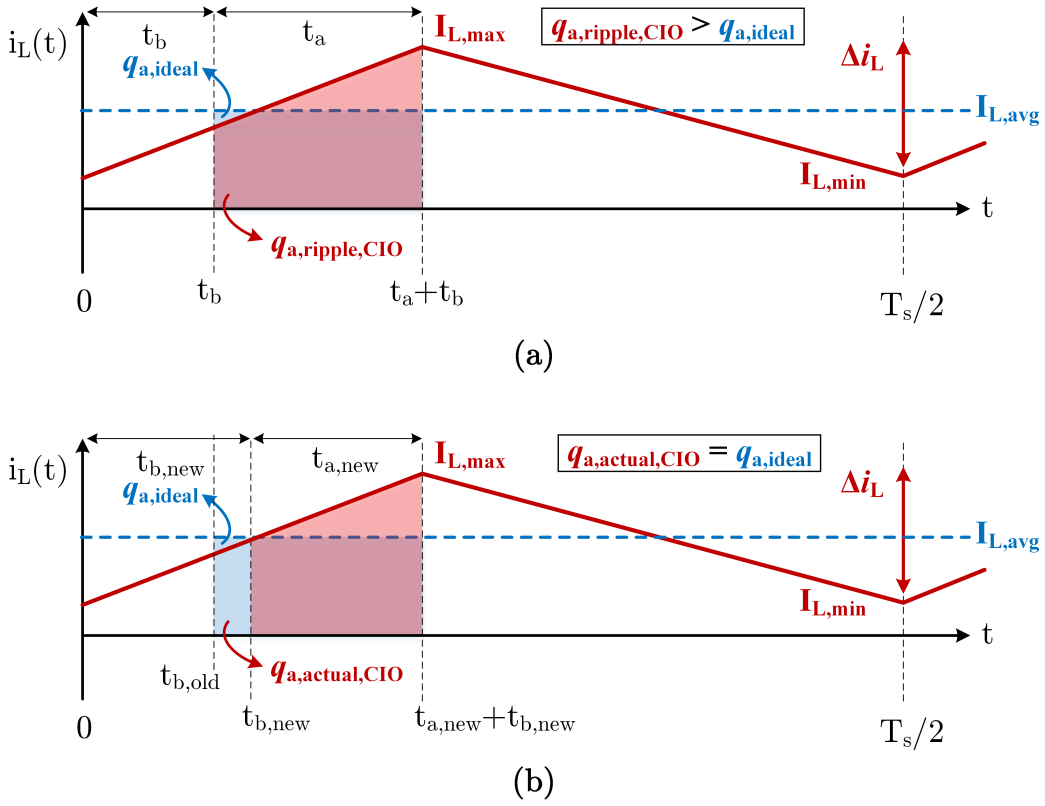


Figure 4.20: Required adjustments to t_a and t_b sub-phase timings for CIO ($b \rightarrow a$) ordering. If Phase 1 starts with the b sub-phase, the constant-current derived timings are an over-estimate of the required Phase 1a timing.

Similar to a buck converter, the peak-to-peak inductor current ripple is given by

$$\Delta i_L = \frac{(V_{SW} - V_{OUT})DT_{SW}}{L} \tag{4.45}$$

where V_{SW} is the voltage of the switch-node, V_{out} is the output voltage, T_{SW} is the switching period, L is the inductance, and D is the duty cycle, given by

$$D = \frac{t_a + t_b}{T_{SW}}. \tag{4.46}$$

The modified $t_{a,new}$ was then found for CIO control in [28], and is repeated below for refrence.

$$t_{a,new,CIO} = \frac{-I_{L,min} + \sqrt{I_{L,min}^2 + \frac{(V_{SW} - V_{OUT})(N-2)}{LN} \cdot (I_{L,avg} DT_{SW})}}{\frac{(V_{SW} - V_{OUT})}{L}}. \tag{4.47}$$

A similar analysis procedure can be used to calculate the $t_{\mathrm{a,new}}$ sub-phase time for CRO control, which is the more advantageous sub-phase ordering scheme to use for a step-down Dickson-derived converter. The modified timing is presented below, and only differs from (4.47) by the $(N+2)$ term, instead of $(N-2)$.

$$t_{\mathrm{a,new,CRO}} = \frac{-I_{\mathrm{L,min}} + \sqrt{I_{\mathrm{L,min}}^2 + \frac{(V_{\mathrm{SW}} - V_{\mathrm{OUT}})(N+2)}{LN} \cdot (I_{\mathrm{L,avg}} D T_{\mathrm{SW}})}}{\frac{(V_{\mathrm{SW}} - V_{\mathrm{OUT}})}{L}}. \tag{4.48}$$

Note that for step-down control, CRO control results in longer t_{a} durations than CIO control, and therefore results in the output current being distributed across more conduction paths for a greater portion of the overall switching period. This can have implications for overall converter losses, potentially reducing switch conduction losses compared to operation with shorter t_{a} durations.

4.4.3 Split-Phase Timing Analysis - Large Inductor and Capacitor Ripple

If both the capacitor and inductor see large ripple conditions, than the timing analysis becomes much more complex, as described in [31]. Fig. 4.21 graphically illustrates the reason for this additional variation in sub-phase timing. Fig. 4.21a shows the updated timing, $t_{\mathrm{a,new}}$ assuming triangular ripple current. This timing had to be increased compared to the ideal t_{a}. However, for the full ripple case shown in Fig. 4.21b, the corresponding updated timing $t_{\mathrm{a,full-ripple}}$ is closer to the ideal timing, as the sinusoidal current waveform during Phase 1 will accumulate more charge under it than the linear ramp shown in Fig. 4.21a.

However, when considering the full 2nd-order behavior of the switch-capacitor network and inductor, these timings may not easily be calculable with closed form solutions, and will instead require the use of numeric solvers, as in [31].

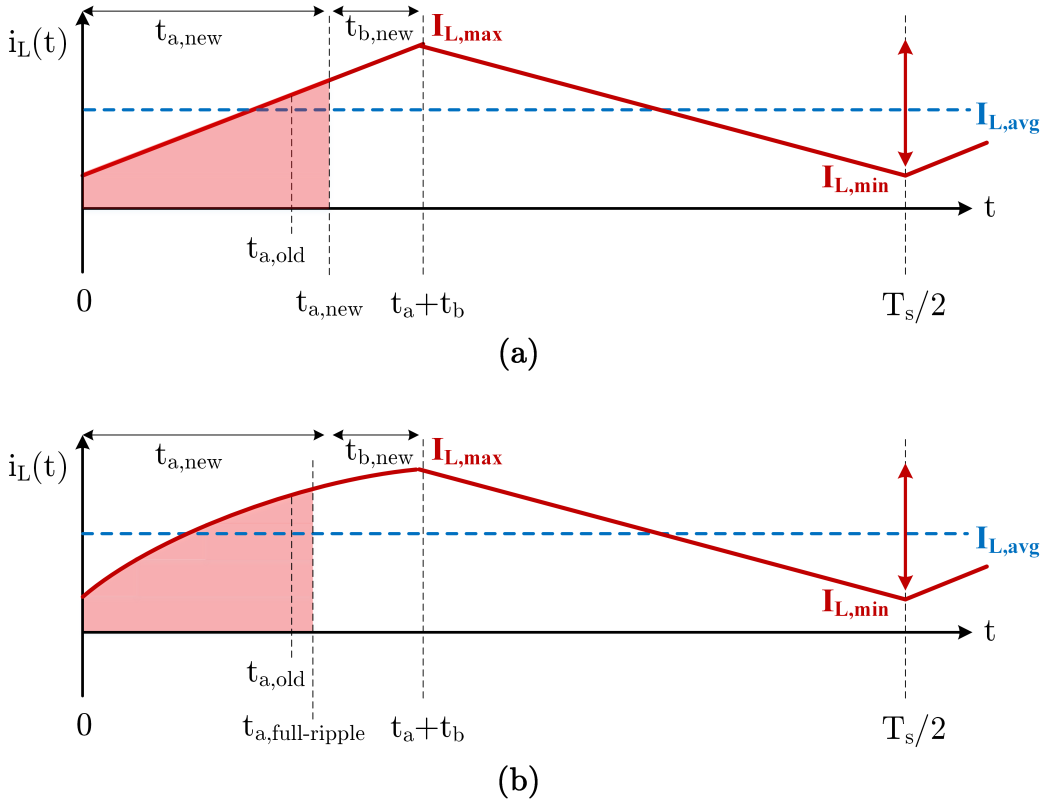


Figure 4.21: Difference in required timing assuming (a) triangular inductor current ripple and small capacitor voltage ripple, and (b) both large inductor current ripple and large capacitor voltage ripple, including the 2nd-order *LC* tank effects.

Chapter 5

Active Splitphase Control Using Capacitor Voltage Discontinuity Detection

5.1 Introduction

As described previously, the Dickson converter can achieve very efficient switch utilization [1] and exhibits the theoretical minimum switch stress compared to other SC converters [42]. However, while other hybrid SC topologies can softly charge all flying capacitors through the proper placement of one or more inductors [3,4] – thereby avoiding the large impulse currents and corresponding losses associated with hard capacitor charge redistribution – soft-charging in the Dickson converter is not as straightforward, and may require the use of split-phase switching.

Previous work has presented different analytical approaches for calculating the required split-phase timings under various assumptions, such as negligible or linear inductor current ripple [28,29,62]. While [31] presents a full-ripple second-order LC analysis, all of these above methods assume constant capacitance and inductance values. In practice, these assumptions may break down if operating under large-ripple conditions or if using Class II multi-layer ceramic capacitors (MLCCs) and soft-saturating magnetics, whose values derate as a function of operating conditions. As a result of these real-world impacts, the necessary timings required for full-soft charging can deviate substantially from the calculated values found using analytical methods. Furthermore, while the higher fidelity calculation methods may be able to produce more accurate results, they can become quite complex to implement in hardware as they require the use of extensive lookup tables collected across the full range of operating conditions.

This chapter therefore presents an active split-phase control technique that detects hard-charging events on the flying capacitors and continuously tunes the switch gating signals to achieve soft-charging, as a continuation of the work presented in [63]. This control technique

is demonstrated on an 8-to-1 resonant Dickson converter and an 8-to-1 Hybrid Interleaved-Input Single Inductor Dickson (HISID) converter, both of which were implemented with Class II MLCCs and a soft-saturating composite inductor. The control technique is shown to converge on soft-charging split-phase timings. A similar active control method has been recently proposed specifically for regulating Dickson converters [64], wherein the capacitor voltages are sensed during the "quiet" regulating phases where the capacitor network is left open-circuited, such that no charge flows. While this allows for simplified circuitry and low-bandwidth sensing, these phases do not exist in resonant fixed-ratio converters, necessitating other detection methods such as the one presented in this work. Moreover, while this hard-charging detection technique is validated here with resonant capacitor voltage waveforms, it is general in approach and can be tuned to detect hard-charging events in a wide variety of circuit topologies and operating modes.

5.2 Theory of Operation

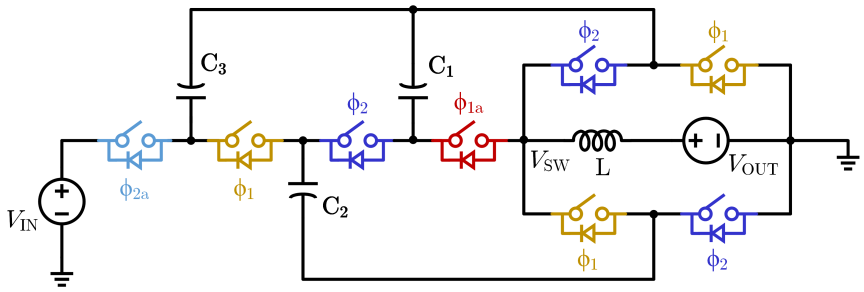


Figure 5.1: Schematic drawing of a 4-to-1 single-inductor resonant Dickson converter, with operating phases labeled. The control signals ϕ_1 and ϕ_2 are the main phase signals, while ϕ_{1a} and ϕ_{2a} are the split-phase control signals.

For the sake of demonstration, the control method is described for a 4-to-1 resonant Dickson topology, but can easily be extended to N-to-1 Dickson converters. Fig. 5.1 shows a schematic drawing of the 4-to-1 topology, with gating signals as labeled. The converter is operated with two main phases, Phase 1 and Phase 2, with durations of t_1 and t_2 and gating signals ϕ_1 and ϕ_2. Both phases operate with 50% duty cycle. To achieve soft-charging, two additional sub-phases, Phase 1a and Phase 2a, can be introduced with durations t_{1a} and t_{2a} and gating signals ϕ_{1a} and ϕ_{2a}, as shown in Fig. 5.2. For the 4-to-1 topology shown in Fig. 5.1, these sub-phases ensure that C_1 and C_3 are disconnected once their voltages have reached the values that satisfy the KVL loop defined by the next phase equivalent circuit, as described in [29]. If the capacitor voltages deviate from these values at the start of the next phase, hard charge redistribution will occur, resulting in increased losses. For a general N-to-1 Dickson converter with $N-1$ flying capacitors, only capacitors C_{N-1} and

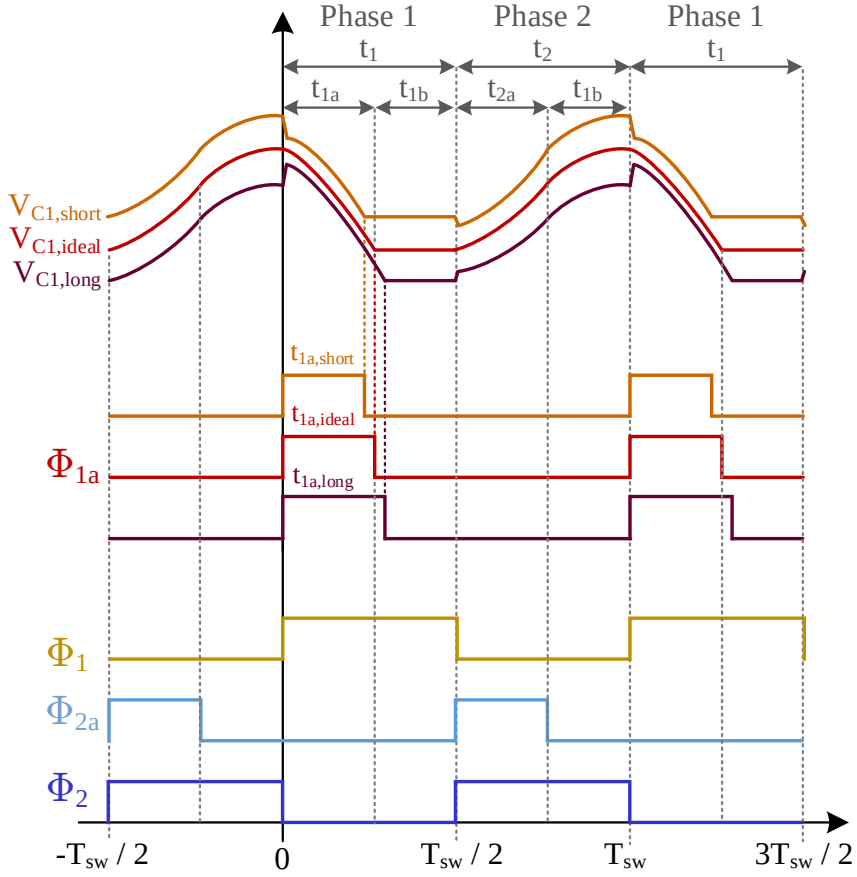


Figure 5.2: Gating signals for the converter in Fig. 5.1. The capacitor voltage across C_1 is also shown for soft-charging operation (correct timing) and hard-charging operation (too long or too short timing).

C_1 will require split-phase switching, making the analysis easily extendable to higher-order conversion ratios.

In an ideal Dickson converter, Phase 1 and Phase 2 (and their corresponding sub-phases) are equivalent, such that the phase time durations satisfy $t_{1a} = t_{2a} = t_a$ and $t_{1b} = t_{2b} = t_b$. This work therefore only senses the voltage of the low-side split-phase capacitor, C_1, and then modifies both t_{1a} and t_{2a} simultaneously. However, these split-phase times could be modulated independently to allow for parasitic deviations or component tolerance mismatch between the two split-phase branches, though this is not explored in this work. Finally, the converter is assumed to operate with a fixed frequency, such that only t_{1a} and t_{2a} are changed by the feedback loop, while t_1 and t_2 remain constant.

Fig. 5.2 shows characteristic capacitor voltage waveforms for C_1 for both soft-charging and hard-charging operation. When the split-phase time duration t_{1a} is correctly tuned,

the capacitor voltage will exhibit a smooth continuous waveform throughout the switching period, as demonstrated by $V_{C_1,\text{ideal}}$. However, if t_a is off in either direction, the capacitor voltage will experience sharp discontinuities as hard charge redistribution occurs when the converter enters the next operating phase. The polarity of these discontinuities corresponds to whether the previous timing was too short or too long. A steep negative slope – as demonstrated by $V_{C_1,\text{short}}$ – corresponds to split-phase time durations t_{1a} and t_{2a} that are too short, while a steep positive slope – as demonstrated by $V_{C_1,\text{long}}$ – corresponds to split-phase time durations that are too long. The proposed control method is designed to detect these discontinuities, and based on the polarity, appropriately increase or decrease the split-phase times.

This technique is similar to the zero-voltage-switching (ZVS) detection methods presented in [65,66]. The methods are somewhat analogous, as here the control detects a resonant soft-charged capacitor voltage versus a discontinuous hard-charged capacitor voltage, while the ZVS control in the referenced works detects a resonant drain-to-source voltage versus a discontinuous hard-switching drain-to-source voltage. However, these ZVS detection methods are only designed for ground-referenced switches, while the proposed method can handle the floating voltages characteristic of flying capacitors in hybrid SC converters.

5.2.1 Analog Circuitry

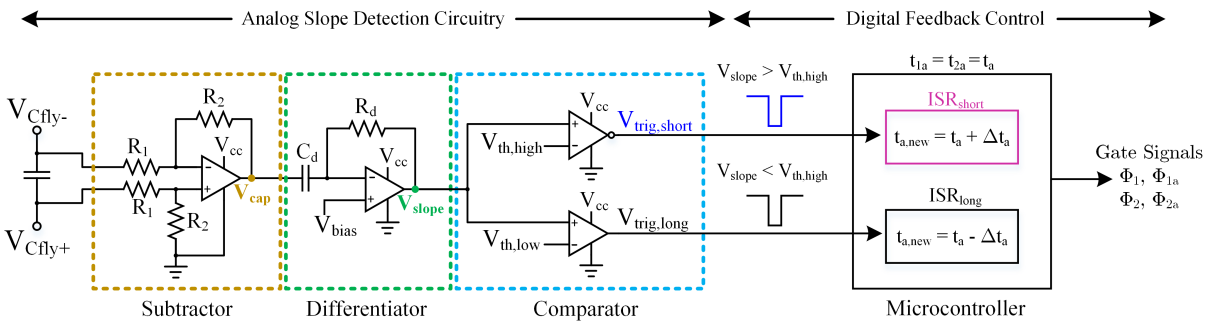


Figure 5.3: Schematic of the active split-phase control circuitry, including the analog slope detect circuitry and the controller logic. The "short" timing path is color-coded to match the experimental waveforms shown in Fig. 5.10.

The control architecture is presented in Fig. 5.3. The analog circuity is powered by a single supply of $V_{\text{cc}} = 5$ V. The first stage consists of a subtractor circuit, which converts the differential flying capacitor voltage to a single-ended voltage, given by $V_{\text{cap}} = \frac{R_2}{R_1} \cdot (V_{\text{Cfly}+} - V_{\text{Cfly}-})$. This voltage is then fed into an active differentiator circuit, whose output is proportional to the slope of the input, given by $V_{\text{slope}} = -R_d C_d \frac{dV_{\text{cap}}}{dt} + V_{\text{bias}}$. The signal is biased around $V_{\text{bias}} = 2.5$ V so that it is centered between the comparator supply rails, where V_{bias} is created using a simple resistor divider powered from the V_{cc} rail.

When a hard-charging event occurs at the Phase 2-to-Phase 1 transition (as labeled in Fig. 5.2), the steep slope present in V_{Cfly} and V_{cap} generates a large pulse on V_{slope}. This signal is then compared to two different threshold voltages, $V_{\text{th,high}}$ and $V_{\text{th,low}}$, to determine whether the hard-charging event is caused by too short or too long of split-phase timing. These thresholds are also set using simple resistor dividers supplied by the V_{cc} rail, and are only tuned during initial circuit design. The threshold levels should be set so that the detection circuit triggers the comparators correctly at low current, as the magnitude of the pulse will be at its lowest at light load.

As an example, if the split-phase timing is too short, the upward pulse on V_{slope} will go above $V_{\text{th,high}}$, generating a falling edge on $V_{\text{trig,short}}$. This then triggers an external interrupt in the microcontroller, so that the phase timing can be updated. Fig. 5.4 illustrates the output of each stage of the control circuitry for the case where the split-phase time duration, t_a, is too short. Similarly, if the split-phase timing is too long, V_{slope} will exhibit a downward pulse that will go below $V_{\text{th,low}}$, generating a falling edge on $V_{\text{trig,long}}$ and triggering the corresponding external interrupt.

Note that while V_{slope} is fed into the positive terminal of both comparator channels, the inverted comparator output is used to generate $V_{\text{trig,short}}$, while the non-inverted comparator output is used to generate $V_{\text{trig,long}}$. This is done to simplify the hysteresis resistor network used to prevent oscillations around the trigger level (not shown in Fig. 5.3).

In practice, the capacitor voltage discontinuities can be larger at the Phase 2-to-Phase 1 transition compared to the Phase 1-to-Phase 2 transition (as shown in Fig. 5.2), in part due to parasitic effects. This results in a larger corresponding pulse in V_{slope}, which is easier to sense. However, the control could be adjusted to monitor both phase transitions to detect hard-charging events at twice the frequency, though a more conservative control approach may be to only adjust duty cycle timings once per switching cycle, such that Phase 1 and Phase 2 remain symmetrical within one switching period.

5.2.2 Microcontroller Feedback

Depending on which comparator channel triggers the controller, the duration of t_a will be increased or decreased. For example, a falling edge on $V_{\text{trig,short}}$ will trigger the interrupt service routine, ISR_{short}, which will increase the split-phase time t_a by a step-size Δt_a. Similarly, ISR_{long} will decrease t_a by Δt_a, as shown in Fig. 5.3. This step-size can be tuned to achieve the desired trade-off between the control convergence speed and overshoot behavior.

As mentioned previously, the amplitude of the pulse on V_{slope} will increase with load current. Therefore, to increase the sensitivity of the hard-charging detection circuitry at light load, the trigger thresholds should be set as close to the level of the soft-charged V_{slope} waveform as possible. However, as can be seen in Fig. 5.4, at other times in the switching period V_{slope} can exceed this threshold level even when not in the presence of a hard-charging event, due to the sinusoidal shape of the capacitor voltage waveform. To account for this, the V_{slope} signal is only monitored by the controller during a time t_{window}, centered around

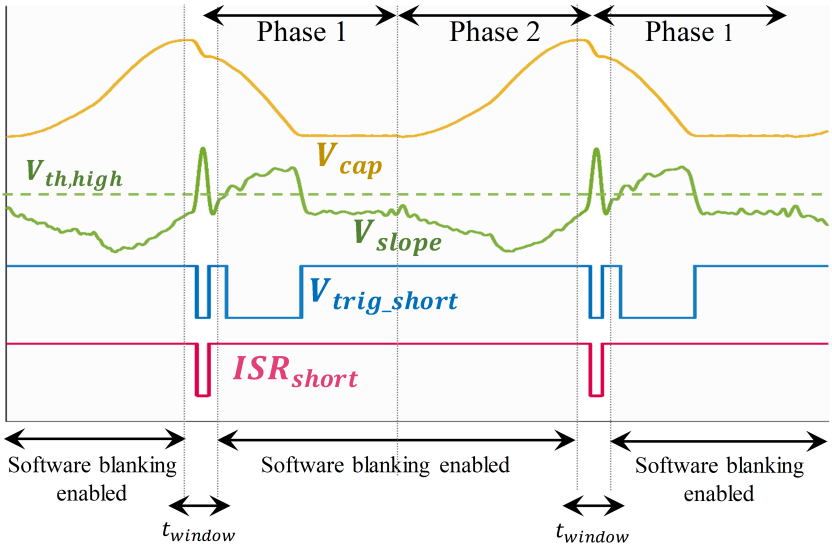


Figure 5.4: Simplified control circuit waveforms, corresponding to the case where t_a is too short. The output of each control stage is plotted. A blanking window is implemented in code to isolate only the V_{slope} pulses at the Phase 2-to-Phase 1 transition.

the peak of V_{cap} at the Phase 2-to-Phase 1 transition. A software-enabled blanking window ignores any other comparator triggers, so that the controller will only modify t_a in this window, regardless of whether $V_{\text{slope}} > V_{\text{th,high}}$ at other times during the switching period. Fig. 5.4 illustrates this software blanking window for the case where the split-phase timing is too short. The threshold $V_{\text{th,high}}$ is set near the base of the upward pulse on V_{slope}, allowing for the circuitry to detect hard-charging events across a wide load range. Extra filtering, such as additional high-pass filters, can be added to push down the noise floor of V_{slope} to allow for easier detection of hard-charging events. However, this can further attenuate the amplitude of the pulse and also requires more circuit stages, presenting a trade-off for the designer.

The control uses a hysteretic approach to converge onto the split-phase timing that results in soft-charging. Because $V_{\text{th,high}} \neq V_{\text{th,low}}$, when converging on split-phase timing from a hard-charging condition, the converter will enter a hysteresis band defined by these thresholds, preventing oscillatory behavior and allowing the control to more easily maintain a steady state timing.

5.3 8-to-1 Single-Ended Dickson Hardware Prototype

The hard-charging detection circuitry was validated on an 8-to-1 resonant Dickson converter, as shown in Fig. 5.5. The converter was designed with a derated flying capacitance of 4 μF and an inductance of 680 μH, while the switches were implemented with 25 V Si MOSFETs. The hard-charging detection circuitry was implemented as a daughterboard

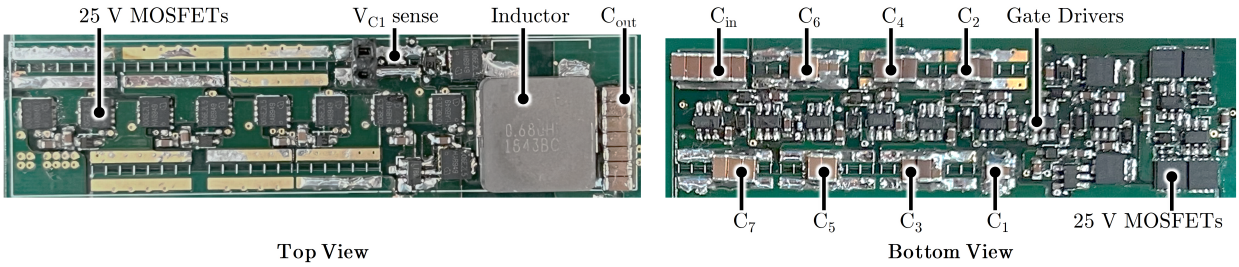


Figure 5.5: Annotated photograph of the 8-to-1 Dickson power stage, with main components labeled. Dimensions: 2.8 in (7.0 cm) x 0.7 in (1.8 cm).

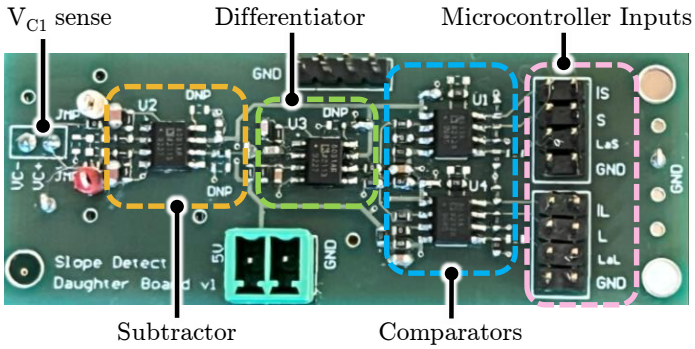


Figure 5.6: Annotated photograph of the single-sided control daughterboard. Dimensions: 2.8 in (7.0 cm) x 1.1 in (2.8 cm).

mounted on top of the 8-to-1 Dickson converter. Fig. 5.6 shows an annotated photograph of the daughterboard, highlighting the individual stages of the control circuitry. Table 5.1 gives a full list of the main components for the 8-to-1 Dickson power stage and the control daughterboard, as labeled in Fig. 5.5 and Fig. 5.6. The experimental setup was tested at an input voltage of 48 V and an unregulated output voltage of 6 V, up to an output current of 10 A (60 W), as summarized in Table 5.2. The total power draw of the control circuitry from the V_{cc} rail was 90 mW across the load range. The threshold levels $V_{th,high}$ and $V_{th,low}$ were tuned during initial circuit design, and were implemented using 0.1 V hysteresis to prevent comparator oscillation. For ease of prototyping, the analog stages were designed with discrete single-channel operational amplitifers and comparators.

Table 5.1: Power Stage and Control Components

8-to-1 Dickson Power Stage Components

Component	Part Number	Description
Switches	IQE006NE2LM5	Si MOSFET, 25 V, 0.65 mΩ
Gate Driver	LT4440-5	80 V, high-side
Inductor	IHLP5050EZERR68M01	680 nH, 54 A I_{sat}, 1.7 mΩ
Fly Capacitors		4 μF derated
C_1	C2012X7R1V225K085AC	2 × 2.2 μF ± 10%, 35 V X7R 0805
C_2	CGA5l3X7R1V225K160AB	2 × 2.2μF ± 10%, 35 V, X7R 1206
C_3	CGA5l3X7R1V225K160AB	1 × 2.2 μF ± 10%. 35 V, X7R 1206
	C3216X5R1V475K085AB	1 × 4.7 μF ± 10%, 35 V, X5R 1206
C_4	CGA5l3X7R1V225K160AB	3 × 2.2 μF ± 10%, 35 V, X7R 1206
C_5	C3216X5R1H106K160AB	2 × 10 μF ± 10%, 50 V, X5R 1206
C_6	C3216X5R1H106K160AB	2 × 10 μF ± 10%, 50 V, X5R 1206
	CGJ4J3X7R1E105K125AB	1 × 0.68 μF ± 10%, 50 V, X5R 1206
C_7	C3216X5R1H106K160AB	3 × 10 μF ± 10%, 50 V, X5R 1206

Control Board Components

Component	Part Number	Description
Subtractor op-amp	AD8091	145 V/μs, 110 MHz
Differentiator op-amp	AD8091	145 V/μs, 110 MHz
Comparator	AD8611	Ultrafast 4 ns Single-Supply
Controller	F28379D	Delfino Experimenter Kit

Control Biasing Components

Component	Value
Voltage divider resistor, R_1	49.9 kΩ, 0.1%
Voltage divider resistor, R_2	4.99 kΩ, 0.1%
Filter resistor, R_d	4.99 kΩ, 0.1%
Filter capacitor, C_d	3 × 220 pF

Table 5.2: 8-to-1 Resonant Dickson Converter Operating Parameters

Parameter	Description	Value
Power Stage		
V_{in}	Input Voltage	48 V
V_{out}	Output voltage	6 V
$I_{\text{load,max}}$	Full load current	10 A
f_{sw}	Switching frequency	67.5 kHz
Control Biasing		
V_{bias}	Bias voltage	2.5 V
$V_{\text{th,high}}$*	High threshold	2.58 V
$V_{\text{th,low}}$*	Low threshold	2.43 V
P_{ctrl}	Control power	90 mW

*with 0.1 V hysteresis

5.3.1 Analog Circuitry Design Considerations

As the control scheme uses analog circuitry to sense voltage discontinuities, certain additional circuit components should be used, besides those listed in Fig. 5.3 and Table 5.1. For example, the operational amplifiers in the subtractor and differentiator stages may need a small capacitance (∼20 pF) connected across the inverting input and the output (i.e. in parallel with R_2 and R_{d}, respectively), in order to prevent oscillations at the output. Similarly, the comparator stage should be operated with some small amount of hysteresis to prevent oscillations on the output that can feed back into the sensing circuitry. The following section demonstrates how to implement this using a resistor network, and shows experimental waveforms demonstrating operation with this hysteresis band.

Hysteresis Circuitry

The output comparators were operated with the hysteresis network shown in Fig. 5.7, in order to improve comparator stability and prevent output oscillations. The input signal, V_{slope}, was fed into the positive terminal of the comparator for both the "too short" and "too long" comparator channels. This was done so that the bias resistor network (i.e. R_1 and R_2) used to set up the comparator's reference voltage did not load the input signal. The resistors R_3 and R_4 set up the hysteresis voltage, centered around the reference formed by R_1 and R_2.

The value of resistors R_1 through R_4 can be calculated according to the following equa-

tions, based on the desired reference voltage and hysteresis band [67],

$$V_{\mathrm{REF}} = \frac{R_1}{R_1 + R_2} \cdot V_{\mathrm{CC}} \tag{5.1}$$

$$V_{\mathrm{HYST}} = \frac{R_3}{R_4} \cdot (V_{\mathrm{OH}} - V_{\mathrm{OL}}) = V_{\mathrm{TH}} - V_{\mathrm{TL}} \tag{5.2}$$

$$V_{\mathrm{TH}} = \frac{(R_3 + R_4) \cdot V_{\mathrm{REF}} - R_3 \cdot V_{\mathrm{OL}}}{R_4} \tag{5.3}$$

$$V_{\mathrm{TL}} = \frac{(R_3 + R_4) \cdot V_{\mathrm{REF}} - R_3 \cdot V_{\mathrm{OH}}}{R_4} \tag{5.4}$$

Here, V_{REF} is the reference voltage for the comparator, V_{TH} is the high threshold, V_{TL} is the low threshold, and V_{HYST} is the hysteresis voltage band.

Fig. 5.8 shows experimental waveforms for the output of the differentiator, V_{slope} and the output of the corresponding comparator, V_{trig} for (a) "too short" and (b) "too long" of t_{a} values. The comparator output can be observed to only transition when the input signal goes above V_{TH} or when the input signal goes below V_{TL}.

5.3.2 Control Circuit Tradeoffs

The daughterboard was designed for control validation, and therefore used separate ICs for each stage. However, total board area could be significantly reduced by combining both the subtractor and differentiator stages as well as the comparator stages into single ICs, reducing the total number of discrete ICs from four to two.

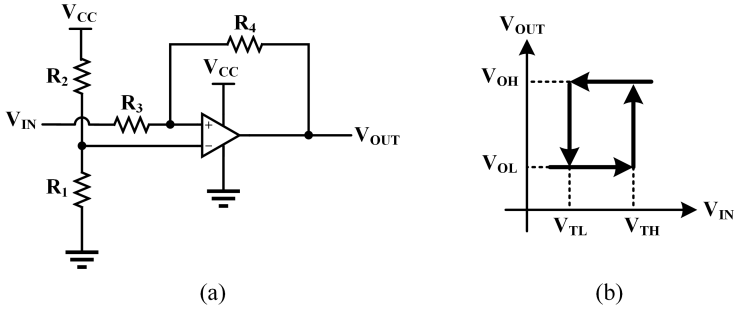


Figure 5.7: Theory of operation for a single-supply comparator: (a) Schematic drawing of a single-supply comparator configured with hysteresis. The signal, V_{IN}, is fed into the noninverting input. (b) Comparator input-output transfer characteristics (note that the reference voltage on the inverting input biases the circuit operation entirely within the first quadrant.)

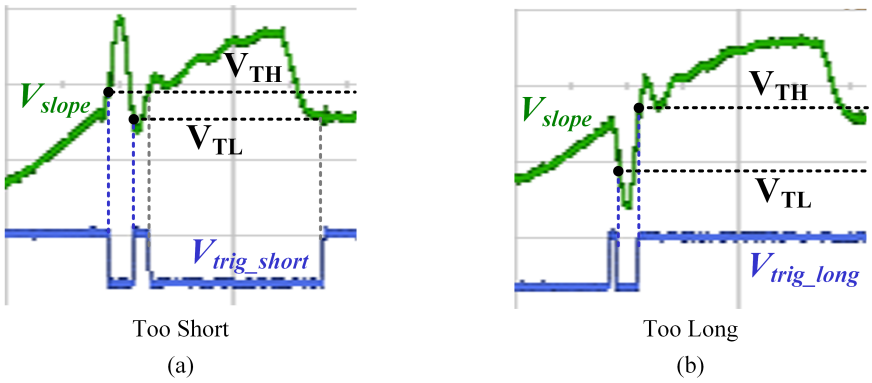


Figure 5.8: Operating waveforms showing the output of the differentiator, V_{slope}, and the output of the corresponding comparator, V_{trig} for (a) too short of t_{a} and (b) too long of t_{b}. The low threshold, V_{TL}, and the high threshold, V_{TH} are annotated.

While the subtractor operational amplifier should have a high enough slew rate to faithfully replicate the steep discontinuities on the capacitor voltage waveform, the slew rate requirement on the differentiator may not be as stringent depending on the converter operating parameters. Therefore, the designer could choose to use different operational amplifier ICs for the subtractor and differentiator stages to reduce the total power draw of the control circuitry. These specifications can be set to achieve the desired trade off between power consumption and filter performance.

Experimental V_{slope} waveforms are plotted in Fig. 5.9 for a range of load currents, I_{load}. Fig. 5.9 (a) shows the case where the split-phase time t_a is too short, and V_{slope} sees an upwards pulse at the phase transitions. The magnitude of the pulse increases with load current. Fig. 5.9 (b) shows the case where the split-phase time t_a is too long, and V_{slope} sees a downwards pulse at the phase transitions. As mentioned previously, the pulse at the Phase 1-to-Phase 2 transition can have a lower magnitude compared to the pulse at the Phase 2-to-Phase 1 transition, due to parasitic and component tolerance effects not fully elaborated upon in this work. The comparator threshold levels, $V_{\text{th,high}}$ and $V_{\text{th,low}}$, are also plotted, and are set as close to the base of the pulse as possible to allow the control to trigger at low current. Spurious triggering at other points in the switching period is prevented by the control windowing described in Section II. B.

5.3.3 Experimental Waveforms with Active Control

Fig. 5.10 shows experimental waveforms for the converter before, during, and after convergence to a soft-charging state when operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with too short of a t_a value, resulting in downward step discontinuities on the capacitor voltage, V_{cap}. Once the control is enabled, the circuitry detects the resulting large upward pulse on V_{slope}, causing $V_{\text{trig,short}}$ to be pulled low and

ISR_{short} to be triggered. The ISR increases the split-phase times t_{1a} and t_{2a} by a step size Δt_a until the converter reaches a timing that results in smooth, soft-charged capacitor voltage waveforms. The software blanking window ignores any comparator triggering outside of the phase transition window, t_{window}. After convergence, the controller continues to ignore comparator falling edges outside of t_{window}, and will remain in this steady-state condition unless perturbed. Similarly, Fig. 5.11 shows experimental waveforms before, during, and after convergence when the converter is initialized with too long of a t_a timing, again at 48 V input, 6 V output, and 5 A load current. This improper timing results in an upward step discontinuity on V_{cap}, which triggers ISR_{long} once the control is enabled. The converter is similarly able to converge on the correct split-phase timing, resulting in smooth capacitor voltages.

The converter was also tested with various load steps while operating under closed-loop control, to test the ability of the control loop to re-converge on soft-charging timing when perturbed. Fig. 5.12a shows a load step from 25% to 75% of full load (i.e. 2.5 A to 7.5 A). As I_{load} ramps up, the split-phase timing becomes too long for the new load condition, resulting in ISR_{long} triggering for a time $t_{\text{control}} = 85.5$ μs after the load step. At this point, V_{cap} no longer exhibits hard-charging, and the converter takes an additional 126.5 μs to reach a new steady state, resulting in a total settling time $t_{\text{settle}} = 212$ μs (approximately 14 switching cycles).

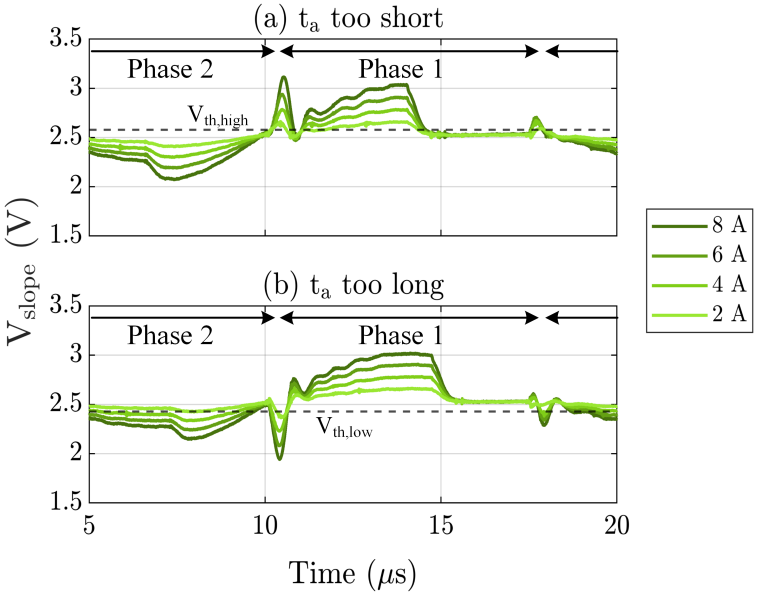


Figure 5.9: Experimental V_{slope} waveforms across several values of I_{load}, for (a) "too short" t_a and (b) "too long" t_a. At the Phase 2-to-Phase 1 transition, a short t_a results in an upwards pulse on V_{slope}, while a long t_a results in a downwards pulse. The comparator trigger thresholds $V_{\text{th,high}}$ and $V_{\text{th,low}}$ are also plotted.

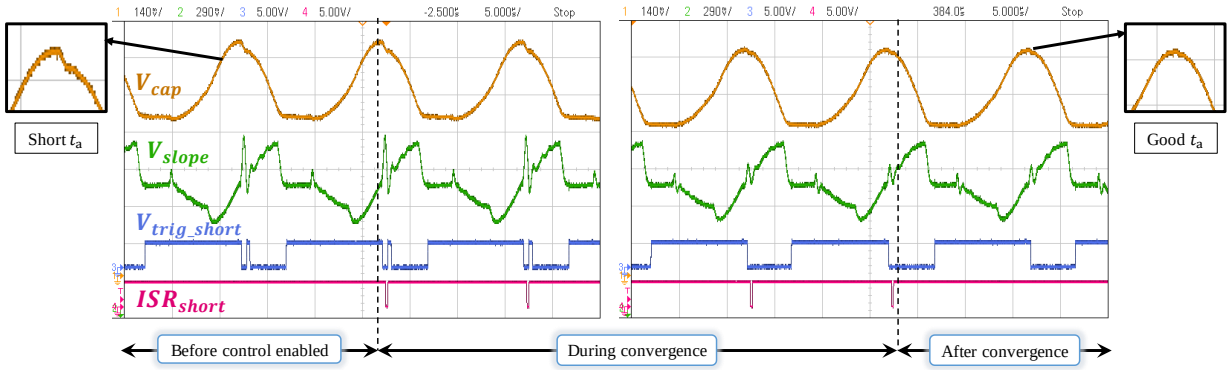


Figure 5.10: Experimental waveforms for the converter operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with a split-phase time t_a, which is shorter than that required for soft-charging. After control is enabled, the converter converges on smooth capacitor voltage waveforms.

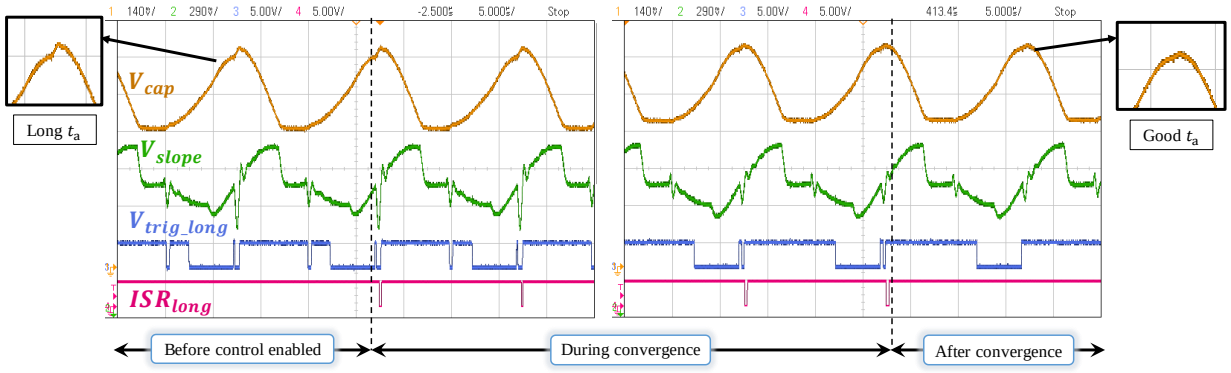
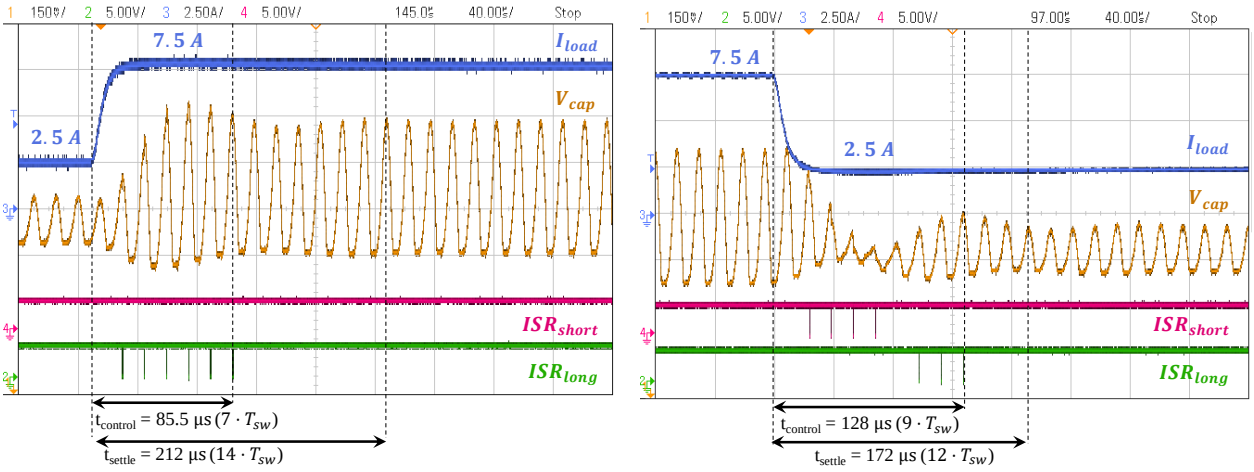


Figure 5.11: Experimental waveforms for the converter operating at 48 V input, 6 V output, and 5 A load current. The converter is initialized with a split-phase time t_a, which is longer than that required for soft-charging. After control is enabled, the converter converges on smooth capacitor voltage waveforms.

Fig. 5.12b shows a similar load step from 75% to 25% of full load (i.e. 7.5 A to 2.5 A). As I_{load} ramps down, the split-phase timing is initially too short, triggering ISR_{short}. The control slightly overshoots, resulting in ISR_{long} triggering briefly. After 128 μs, the capacitor voltage converges to smooth waveforms, and the converter then takes an additional 44 μs to reach its new steady state condition, for a total settling time of $t_{\text{settle}} = 172\mu s$ (approximately 12 switching cycles).

The above hardware waveforms demonstrate that the control loop can converge on the correct split-phase timing required for soft-charging in the case of 1) incorrect timing initial-

ization, and 2) load perturbations, thereby allowing the converter to achieve soft-charging across a wide range of operating conditions.



(a) Step-up load transient: 2.5 A to 7.5 A.

(b) Step-down load transient: 7.5 A to 2.5 A.

Figure 5.12: System waveforms for both step-up and step-down load transients. For a load step of (a) 2.5 A to 7.5 A, the control takes 85.5 μs to converge on soft-charged split-phase timing, and an overall total of 212 μs (approximately 14 switching periods, T_{sw}) to settle to its new steady state condition. For a load step of (b) 7.5 A to 2.5 A, the control takes 128 μs to converge on soft-charged split-phase timing, and an overall total of 172 μs (approximately 12 switching periods, T_{sw}) to settle to its new steady state condition.

5.4 8-to-1 Hybrid Interleaved-Input Single-Inductor Dickson (HISID) Converter Hardware Prototype

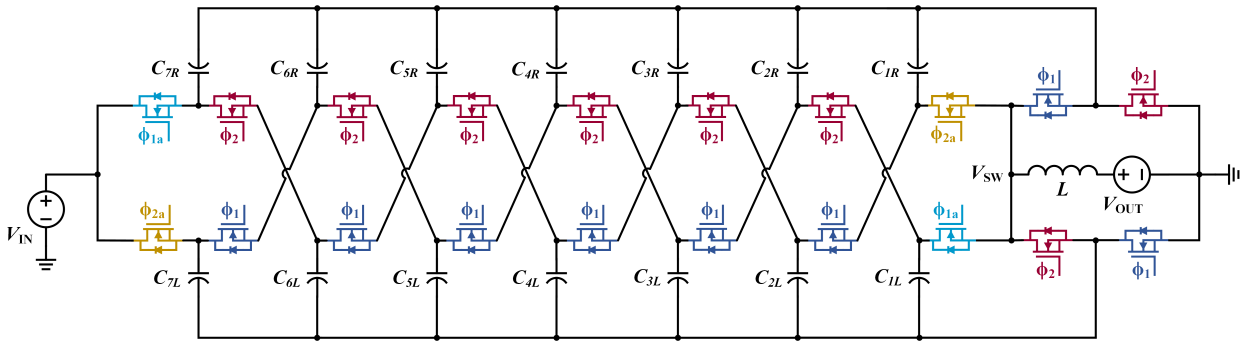


Figure 5.13: Schematic drawing of an 8-to-1 HISID converter. The switches are labeled with their control signals, where ϕ_1 and ϕ_2 are 50% duty cycle control signals, and ϕ_{1a} and ϕ_{2a} are the split-phase control signals.

As previously mentioned, the control technique is general in nature, and can be applied to other Dickson-derived topologies that require the use of split-phase switching, as well as at switching frequencies above the natural resonant frequency of the converter. One such topology is the hybrid interleaved-input single-inductor Dickson (HISID) converter [11, 22, 37], shown in Fig. 5.13. This converter requires split-phase switching on the switches labeled with gate signals ϕ_{1a} and ϕ_{2a}. All other switches are operated with 50% duty cycle control signals.

5.4.1 Hardware Prototype

An annotated photograph of the 8-to-1 hardware used for validation of the control technique is shown in Fig. 5.14. More details about the power stage design can be found in [52]. A summarized listing of the main power stage components is given in Table 5.3.

Similar to the single-ended Dickson converter, this topology can be operated at or above resonance, due to the presence of a single inductor at the output node. When operated above resonance, the inductor current is no longer fully half-wave resonant, and moves into continuous conduction mode (CCM). The resulting operation is similar to that of a CCM buck, although the inductor current in the HISID has a DC offset with some rectified sinusoidal ripple, as opposed to triangular ripple.

Table 5.4 summarizes the operating conditions used to validate the control technique on the hardware prototype. The resonant frequency is 43 kHz, and the converter is operated at approximately 2.8× this value, resulting in a switching frequency of 120 kHz. At this operating point, the capacitor voltage waveforms are no longer sinusoidal, but appear more

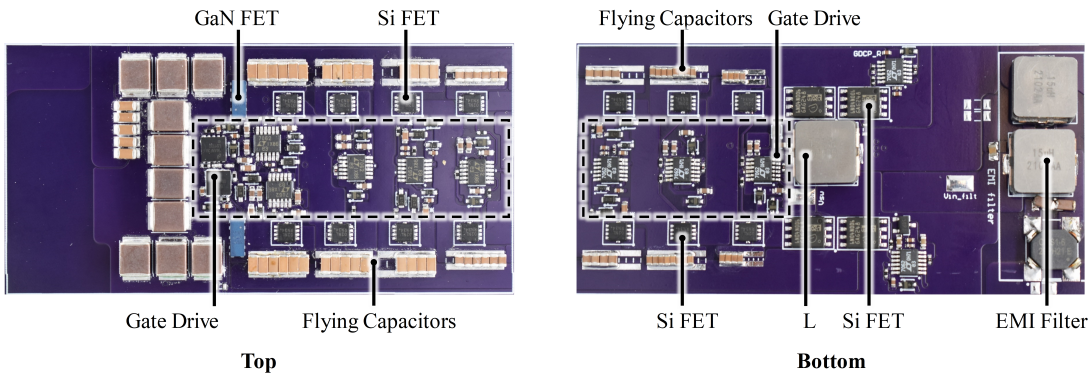


Figure 5.14: Annotated photograph of the hardware prototype, showing the main power components as noted in [52].

Table 5.3: Component Listing of the 8-to-1 HISID Hardware Prototype

Component		Part Number	Description
Power Stage Components			
Input Switches		EPC EPC2206	GaN, 80 V, 2.5 mΩ
Central String Switches		ON Semiconductor NVTFS002-N04CL	Si, 40 V, 3.5 mΩ
Output Bridge Switches		Infineon IAUC100-N04S6L014	Si, 40 V, 1.4 mΩ
Flying Capacitors	C_{1X}, C_{2X}	Murata GRT188R61H225ME13D	X5R, 50 V, 2.2 μF (×4, ×8)
	C_{3X}, C_{4X}	TDK CGA4J3X5R1H475K125AB	X5R, 50 V, 4.7 μF (×4, ×6)
	C_{5X}, C_{6X}, C_{7X}	TDK CGA5L3X5R1H685K160AB	X5R, 50 V, 6.8 μF (×4, ×5, ×7)
Inductor	L	Vishay Dale IHLP4040DZERR56M01	0.56 μH, 49 A I_{sat}
Gate Drive Components			
GaN Gate Driver		Texas Instruments LM5113QDPRRQ1	90 V, high and low-side
Si Gate Driver		Analog Devices Inc. LTC7062IMSE	Dual high-side driver

triangular. In general, the converter waveforms will become more linear as the switching frequency is increased farther and farther above resonance.

5.4.2 Experimental Waveforms with Active Control

Fig. 5.15 shows experimental waveforms for the converter before, during, and after convergence to a soft-charging state when operating at 48 V input, 6 V output, and 10 A load current. The converter is initialized with too short of a t_a value, resulting in downward step discontinuities on the capacitor voltage, V_{cap}. As the converter is operating at 2.8× the fresonant frequency, the capacitor voltages are now triangular in shape.

The sensing and control circuitry works in much the same way it did for the resonant Dickson converter in Section 5.3.3. One modification is the addition of a high-pass filter stage directly after the differentiator stage, so that a filtered version of V_{slope} (i.e. $V_{\text{slope,HP}}$)

Table 5.4: 8-to-1 HISID Converter Operating Parameters

Parameter	Description	Value
V_{in}	Input Voltage	48 V
V_{out}	Output voltage	6 V
$I_{\text{load,max}}$	Full load current	20 A
C_0	Flying capacitance*	6 μF
L	Inductance	560 μH
f_{res}	Resonant frequency	43 kHz
f_{sw}	Switching frequency†	120 kHz

* Per flying capacitor, derated value
† 2.8× the resonant frequency.

is used as the input to the comparators. This is done to increase the prominence of the peak on the differentiator signal when step-discontinuities are present in the capacitor voltage. Section 5.4.3 provides more details on the design of this filter.

As can be seen in Fig. 5.15, the control circuitry detects this large upward pulse on $V_{\text{slope,HP}}$. Once $V_{\text{slope,HP}}$ goes above the threshold of the comparator (i.e. V_{TH}), the output signal $V_{\text{trig,short}}$ goes low. Here, only a small pulse is seen on $V_{\text{trig,short}}$. This is because

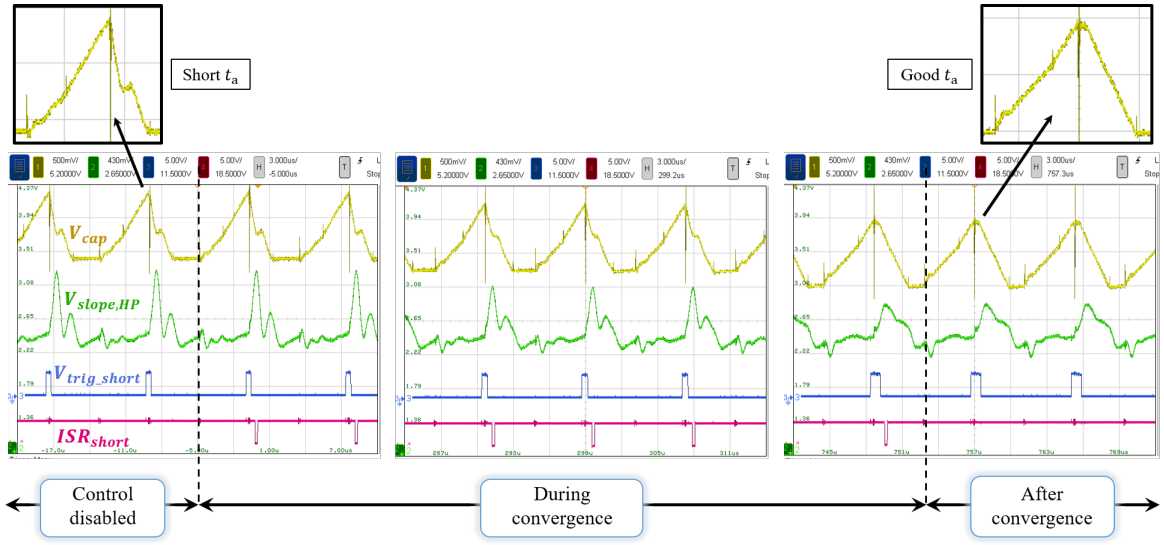


Figure 5.15: Experimental waveforms for the HISID converter operating at 48 V input, 6 V output, and 10 A load current. The converter is initialized with a split-phase time t_a which is too short. After control is enabled, the converter converges on smooth capacitor voltage waveforms. As the operating frequency is high above resonance, the capacitor waveforms are more triangular than sinusoidal.

the comparator is disabled for most of the period, except for a small window around the phase transition. This is done using a latch-enable signal generated by the microcontroller, and can be thought of as a hardware-implemented window, similar to the software window described in Section 5.2.1. These falling edges on $V_{\text{trig,short}}$ trigger ISR_{short}, which then increases the split-phase times t_{1a} and t_{2a} until the converter converges on a soft-charged operating condition.

5.4.3 Modifications to Sensing Circuitry

When the converter is operating around its resonant frequency, the capacitor voltage waveforms are sinusoidal. Therefore, the output of the differentiator stage (i.e. $V_{\text{slope}} = -dV_{\text{cap}}/dt$)

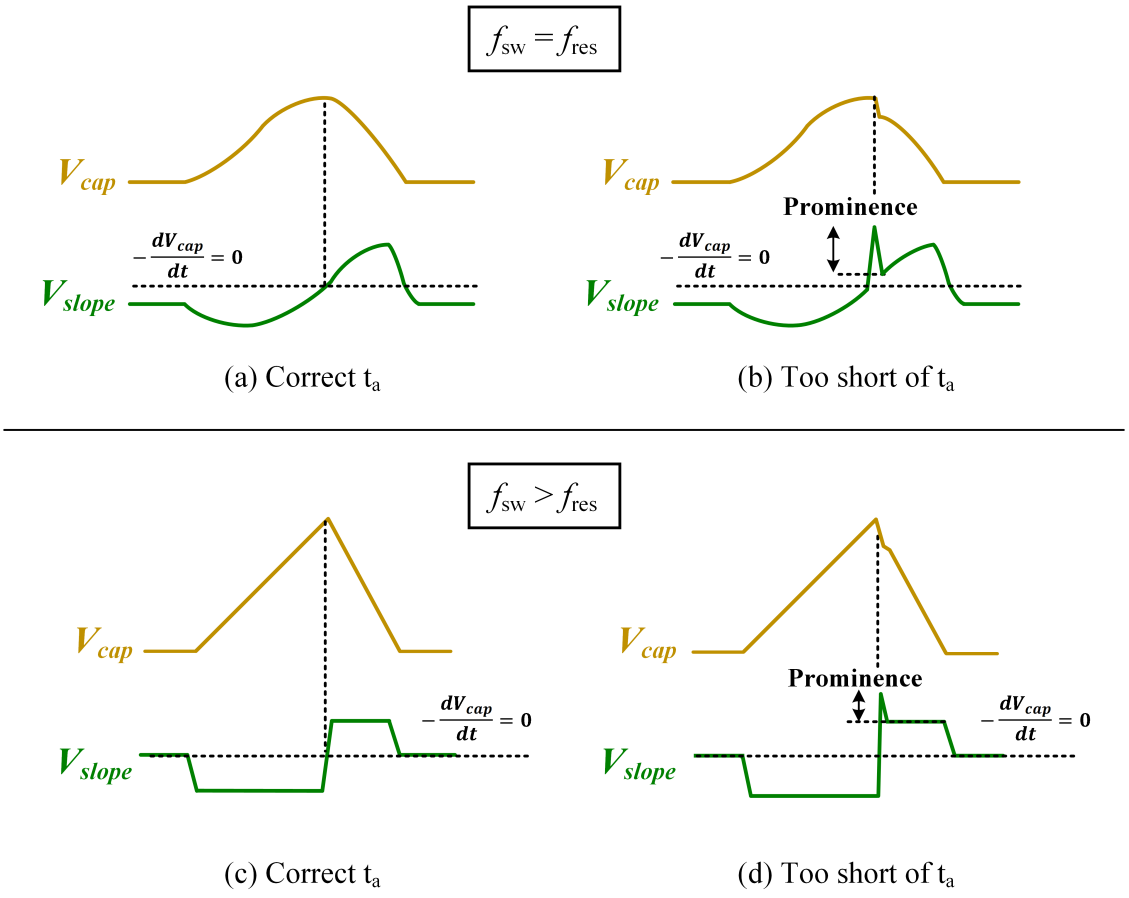


Figure 5.16: Capacitor voltage, V_{cap}, and differentiator output, $V_{\text{slope}} = -dV_{\text{cap}}/dt$, waveforms for the converter (a-b) operating near the resonant frequency (i.e. $f_{\text{sw}} = f_{\text{res}}$); and (c-d) operating high above resonance (i.e. $f_{\text{sw}} > f_{\text{res}}$). The effect on the V_{cap} waveform is shown on the ability of the circuit to detect peaks on V_{slope}.

is also sinusoidal, and has a zero-crossing[1] right at the peak of V_{cap}, as shown in Fig. 5.16a. When operated with correct timing, the capacitor voltage waveform is a smooth sinusoid over Phase 1 and Phase 2, and therefore the signal V_{slope} is also sinusoidal during this time, with a phase-shift of 90°.

Fig. 5.16b now shows the V_{cap} and V_{slope} waveforms when the sub-phase timing t_{a} is too short. The step discontinuity in V_{cap} results in a large peak on V_{slope}. This peak has some prominence above the next highest adjacent signal level, as labeled in the figure. Because this peak occurs near the "zero-crossing" of the V_{slope} waveform, the next highest adjacent signal is still significantly lower than the peak, allowing for easier peak detection, as well as more aggressive comparator threshold settings.

However, as the converter operates farther above the resonant frequency, the capacitor voltage waveforms become more triangular, leading to a more trapezoidal V_{slope} waveform, as shown in Fig. 5.16c for soft-charged operation. In addition, at these higher frequencies, V_{slope} transitions across the $dV/dt = 0$ boundary much faster as the capacitor transitions between charging and discharging.

Fig. 5.16d now shows the V_{cap} and V_{slope} waveforms when the sub-phase timing, t_{a}, is too short. The step discontinuity in V_{cap} again results in a large peak on V_{slope}. However, because of the trapezoidal shape of the waveform, the prominence of this peak is often reduced. In addition, the top and bottom values of the trapezoidal V_{slope} waveform depend directly on the slope of V_{cap}, and will therefore increase as the load current increases and the capacitor charges and discharges more per phase. This means that the reference level for the base of the peak will also move up and down with load, which is not ideal for a control circuit that should be able to track soft-charging across a wide range of operating conditions.

To solve this problem, a high-pass filter was placed on the output of the differentiator in order to preserve the prominence of the large peaks corresponding to step-discontinuities in V_{cap}, while pushing down the rest of the V_{slope} floor. The output of this filter, $V_{\text{slope,HP}}$, is much less trapezoidal, and it is therefore easier to set threshold levels that will work across the entire load range. Fig. 5.17 shows an updated schematic drawing of the analog slope detection circuitry. The two resistors R_{hp} bias the output at $V_{\text{CC}}/2$. The corner frequency of the high-pass filter depends on $\frac{1}{2}R_{\text{hp}}$, as these resistors appear in parallel for an ac signal. The high-pass filter frequency is then set by

$$f_{\text{HP}} = \frac{1}{2\pi(R_{\text{hp}}||R_{\text{hp}})C_{\text{hp}}}. \tag{5.5}$$

Fig. 5.18 shows experimental waveforms for the converter operating at similar "too short" conditions (a) with no high-pass filter and (b) with a high-pass filter inserted between the differentiator and comparator stages. In Fig. 5.18a, the prominence of the peak at the step-discontinuity is somewhat low. Furthermore, the comparator threshold would have to be set at the annotated V_{th}, as soft-charged waveforms at this current level would still result

[1]This "zero-crossing" is actually biased at $V_{\text{CC}}/2$ voltage for the single-supply implementation of the control circuitry used here.

in the same top and bottom voltages for the trapezoidal V_{slope} signal. Fig. 5.18b shows the output of the differentiator and high-pass filter, $V_{\text{slope,HP}}$, at a similar operating condition. The prominence of the peak is greatly increased, and the threshold level can also be set much closer to the "dV/dt = 0" bias level, as annotated.

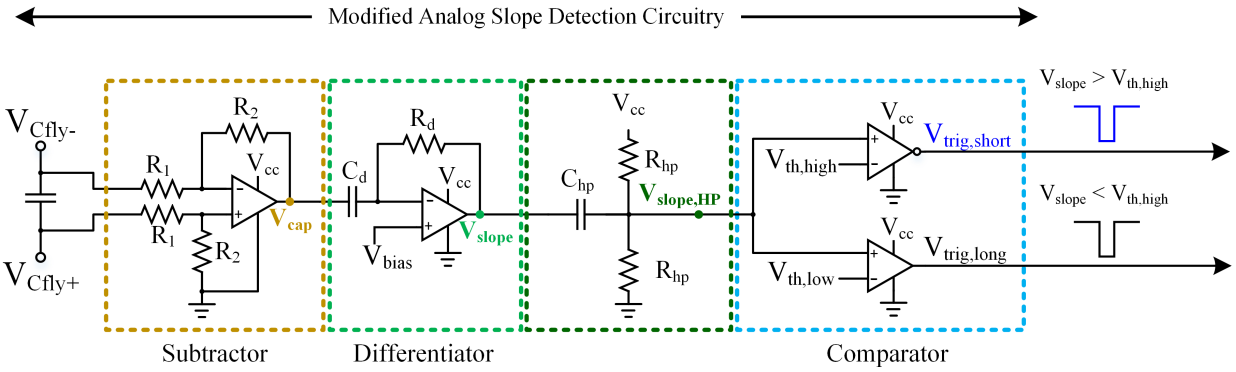
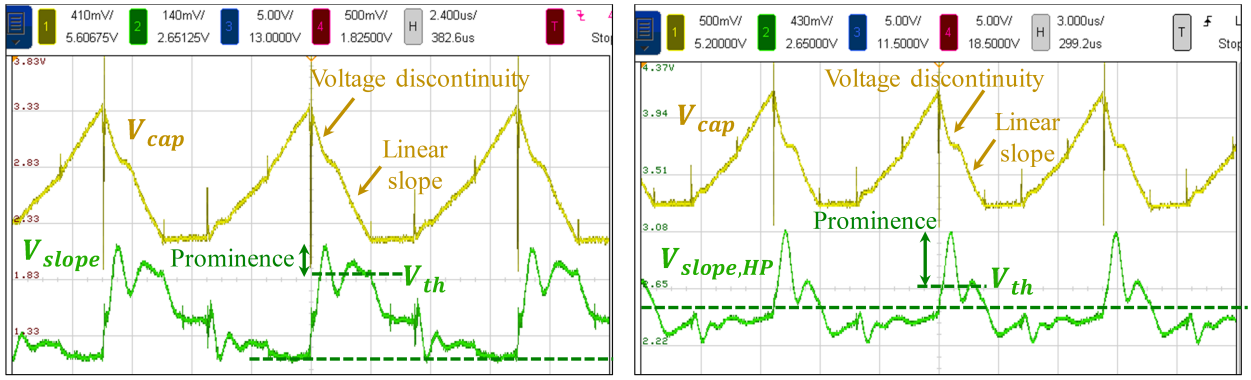


Figure 5.17: Modified analog slope detect circuit, showing the high-pass filter placed between the differentiator and comparator stages.



Without high-pass filter (a)

With high-pass filter (b)

Figure 5.18: V_{cap}, V_{slope}, and $V_{\text{slope,HP}}$ waveforms for the converter operating at $V_{\text{in}} = 48$ V, $V_{\text{out}} = 6$ V, $I_{\text{out}} = 10$ A, with too short of t_{a} timing. The input signal to the comparator is shown (a) without an additional high-pass filter (i.e. V_{slope} directly), and (b) with an additional high-pass filter (i.e. $V_{\text{slope,HP}}$).

While the high-pass filter was added using purely passive elements for ease of prototyping on an existing daughterboard, it could be implemented as a separate active buffered high-pass filter to prevent the downstream comparator circuitry from loading the signal and

effecting the biasing. Additionally, the differentiator stage could be instead implemented with a 2nd-order circuit, such as a Sallen-Key filter, to achieve the same effect without increasing the number of stages. The high-pass filter shold not affect the control detection significantly when the converter is operating at resonance, and therefore this modified slope detect circuitry could be used across a wide frequency range.

5.5 Possible Extensions and summary

Certain Dickson converter variants require the use of split-phase switching to soft-charge all flying capacitors. While the split-phase timing can be calculated analytically, in practice this can be complex or inaccurate due to component tolerances and variable operating conditions. This chapter therefore presented the design and validation of an active control circuitry which detects hard-charging events in the capacitor voltage waveforms and tunes the split-phase timing accordingly to achieve soft-charging. The control was validated on both an 8-to-1 single-ended Dickson converter operating at resonance as well as an 8-to-1 HISID converter operating high above resonance. The control was able to correctly detect improper split-phase timing and converge on soft-charging operating conditions. Furthermore, when operating under closed-loop control, the converter was able to maintain soft-charging timing even under changing load conditions. This technique can account for component value deviations in Class II capacitors or soft-saturation magnetics, and enables operation over a wider range of conditions. In addition, the technique can also be applied to a variety of converter topologies and operating frequencies, as demonstrated.

In addition, any converter experiencing capacitor hard-charging can be tuned used this circuit, even if it would not ordinarily operate with split-phase control. The control circuitry can be used to sense voltage step discontinuities on the capacitors, and stagger the manner in which different capacitors are connected to the switch-node. An example of this type of operation will be demonstrated in Chapter 7.

Chapter 6

Passive Volume Analysis Using Peak Energy Storage Requirements

6.1 Introduction of Methodology

This chapter introduces a framework to analytically calculate the total passive volume of resonant switched-capacitor (ReSC) converters, by calculating the peak energy storage requirements for the capacitors and inductors. The proposed framework builds upon conventional vectorized descriptions of switched capacitor converters in [1, 5, 22, 58], which are derived from fundamental charge-balance and zero volt-second principles. Certain assumptions are made to make the analysis more tractable, as well as more easily extendable to a large variety of ReSC converter variants. These are listed below.

6.1.1 Assumptions

1. Periodic steady-state (PSS) conditions are assumed on all capacitors and inductors, requiring that the time-averaged capacitor current $\langle i_{\mathrm{C}} \rangle$ and average inductor voltage $\langle v_{\mathrm{L}} \rangle$ are zero over the full switching period.

2. Ideal circuit elements are assumed, with no parasitic loss elements. This assumption is valid for moderate- to heavy-load operation, and where ohmic losses have minimal impact on the large-signal dynamics of a converter designed for high efficiency (e.g. $\eta \geq 95\%$).

3. Phase durations are chosen so each phase begins and ends with the same inductor current, implying zero inductor volt-seconds within each phase. This constraint is justified in [32].

4. Input and output bypass capacitance is assumed large with respect to the flying capacitors, thus the input and output sources can be considered ideal as is done in many existing models and analyses [1, 5, 58, 68–70]. Finite input/output bypass capacitors

may be included as part of a comprehensive analysis that facilitates port voltage ripple constraints [71,72]. However, this adds significant analytical complexity and is omitted here for conciseness.

This analysis technique was first published in [32]. This chapter is therefore a continuation of that methodology, and extends the analysis to several additional hybrid switched-capacitor converters. The analysis as presented in [32] applies not only to two-phase ReSC converters, but also to certain multi-resonant converters with more than two phases in a switching period, such as the flying capacitor multi-level (FCML) converter. The FCML converter was amenable to being analyzed with the method in [32] without modification, as each capacitor completes its entire charge and discharge cycle across only two phases, independent of conversion ratio. This means that in many ways the analysis is quite similar to more conventional two-phase ReSC converters.

However, certain multi-resonant topologies such as the multi-resonant-doubler (MRD) converter [73] and the Cascaded Series-Parallel (CaSP) converter [18, 19] require a more complex treatment, due to load-dependencies in the topological vectors required to calculate overall peak passive energy storage requirements. The inclusion of these adjustments can also allow the analysis to be used for certain resonant dickson-derived converter topologies that require the use of split-phase switching [29]. These converters can be though of as a class of pseudo-multi-resonant converters, as the standard two-phase control signals are *split* into sub-phases in order to softly charge all flying capacitors. This also introduces similar load-dependencies in the topological vectors.

The analysis is based on the construction of several key topological vectors, which can be obtained through charge flow analysis [1] and basic circuit analysis. Table 6.1 defines the required vectors necessarily for this analysis. Example calculations of these vectors are carried out for an N:1 series-parallel converter throughout the next sections, as well.

6.2 Topological Vectors

To begin, several topologically-defined vectors are obtained. These are normalized to inherent converter operating parameters, such as the high-side port voltage, V_{HI}, current I_{HI}, and power P_{HI}, as well as the converter switching frequency, f_{SW}, and switching period, T_{SW}. These vectors will now be defined, and calculated for an N:1 series-parallel converter.

6.2.1 Charge Flow Matrices: $\boldsymbol{a_{\mathbf{C}}}$, $\boldsymbol{a_{\mathbf{L}}}$,

As is typical for purely capacitor-based converters [1], periodic steady-state analysis of ReSC structures also begins by assessing charge flow through the converter. To do so, charge flow quantities through all circuit elements are normalized to the amount of charge periodically conducted by the high-side port, q_{HI}, as

$$q_{\text{X},ji} = q_{\text{HI}}\, a_{\text{X},ji} \tag{6.1}$$

Table 6.1: Definitions of Required Topological Vectors

Parameter	Definition
N	Conversion ratio, $N:1$ for $N \in \{\mathbb{N} \geq 2\}$.
N_{C}	Number of flying capacitors (excludes terminal input / ouput capacitors).
N_{P}	Number of operating phases within a switching period.
$a_{\mathrm{C},ji}$	Per-phase charge through the ith capacitor during the jth phase, normalized to the total high-side charge q_{HI}.
$a_{\mathrm{L},ji}$	Per-phase charge through the ith inductor during the jth phase, normalized to the total high-side charge q_0.
$a_{\mathrm{S},ji}$	Per-phase charge through the ith switch during the jth phase, normalized to the total high-side charge q_0.
v_i	Mid-range dc voltage for the ith capacitor, normalized to the high-side voltage V_{HI}.
c_i	Capacitance of the ith capacitor, normalized to an arbitrary scaling capacitance C_0
κ_j	Effective capacitance seen by the low-side inductor(s) during phase j, normalized to C_0.
$\omega_{0,j}$	Natural angular resonant frequency of the equivalent LC network during phase j.
t_j	Time duration of phase j.
τ_j	Time duration of phase j, normalized to the full switching period, T_{SW}.

where X is the circuit element type (e.g., capacitor, C or inductor, L), j is the phase index, and i is the element index.

The charge quantity q_{HI} is itself an operating parameter defined as

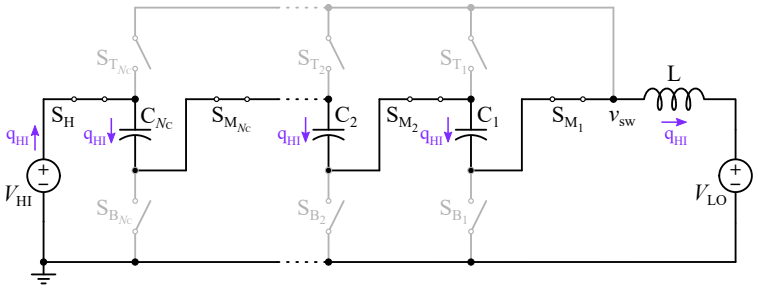
$$q_{\text{HI}} = \frac{I_{\text{HI}}}{f_{\text{SW}}} = I_{\text{HI}} T_{\text{SW}} \tag{6.2}$$

where I_{HI} is the average high-side port current and f_{SW} is the periodic switching frequency (with associated switching period T_{SW}). Subsequently the normalized charge flow matrix, $\boldsymbol{a_X}$, is comprised of topologically-dependent entries which are invariant of operating point (i.e., power level, voltage, and switching frequency). Then, q_{HI} can be used to scale the charge conducted through all elements in unison, while preserving their relative relationships.

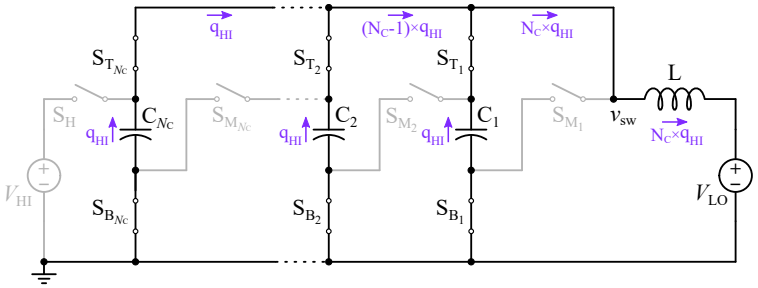
Periodic steady-state requires the capacitors conduct zero net charge per full switching period, as described by

$$\sum_{j=1}^{N_{\text{P}}} a_{\text{C},ji} = 0, \tag{6.3}$$

where N_{P} is the number of operating phases. Utilizing this characteristic, values for $\boldsymbol{a}_{\text{C}}$, and subsequently $\boldsymbol{a}_{\text{L}}$, can then be obtained by inspection.



(a) Phase 1: Series connection



(b) Phase 2: Parallel connection

Figure 6.1: Charge flow in an N:1 Series-Parallel converter.

For example, Fig. 6.1 depicts the periodic steady-state charge flow through an N:1 series-parallel step-down converter operating with two switching phases ($N_{\mathrm{P}} = 2$) and with $N_{\mathrm{C}} = N - 1$ flying capacitors. During phase 1, charge q_{HI} is provided by the high-side source V_{HI}, and is admitted by all series-connected flying capacitors. In adherence with (6.3), each flying capacitor must then release charge q_{HI} during phase 2.

Subsequently, the normalized capacitor charge values, $a_{\mathrm{C},ji}$, for the series-parallel topology are

$$\begin{aligned} \boldsymbol{a}_{\mathrm{C}_{[N_{\mathrm{P}}\times N_{\mathrm{C}}]}} &= \begin{bmatrix} \frac{q_{\mathrm{C},11}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},12}}{q_{\mathrm{HI}}} & \cdots & \frac{q_{\mathrm{C},1N_{\mathrm{C}}}}{q_{\mathrm{HI}}} \\ \\ \frac{q_{\mathrm{C},21}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},22}}{q_{\mathrm{HI}}} & \cdots & \frac{q_{\mathrm{C},2N_{\mathrm{C}}}}{q_{\mathrm{HI}}} \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & \cdots & 1 \end{bmatrix} \end{aligned} \tag{6.4}$$

where the first row's entries correspond to phase 1 and the second row's entries correspond to phase 2. The charge matrices $\boldsymbol{a}_{\mathrm{L}}$ and $\boldsymbol{a}_{\mathrm{S}}$ are similarly determined. The vector $\boldsymbol{a}_{\mathbf{L}}$ is shown below.

$$\begin{aligned} \boldsymbol{a}_{\mathrm{L}_{[N_{\mathrm{P}}\times 1]}} &= \begin{bmatrix} \frac{q_{\mathrm{L},1}}{q_{\mathrm{HI}}} \\ \\ \frac{q_{\mathrm{L},2}}{q_{\mathrm{HI}}} \end{bmatrix} \\ &= \begin{bmatrix} 1 \\ N_{\mathrm{C}} \end{bmatrix} \end{aligned} \tag{6.5}$$

Also apparent from Fig. 6.1, the charge admitted by V_{LO} over both phases is equal to $q_{\mathrm{LO}} = (N_{\mathrm{C}} + 1)\, q_{\mathrm{HI}}$, yielding the converter's voltage conversion ratio:

$$\frac{V_{\mathrm{HI}}}{V_{\mathrm{LO}}} = \frac{I_{\mathrm{LO}}}{I_{\mathrm{HI}}} = \frac{q_{\mathrm{LO}} f_{\mathrm{sw}}}{q_{\mathrm{HI}} f_{\mathrm{sw}}} = \frac{(N_{\mathrm{C}} + 1)\, q_{\mathrm{HI}}}{q_{\mathrm{HI}}} = N. \tag{6.6}$$

Moreover, converter power throughput, P_{HI}, may be expressed in terms of the average high-side charge q_{HI} as

$$P_{\mathrm{HI}} = I_{\mathrm{HI}} V_{\mathrm{HI}} = \frac{q_{\mathrm{HI}}}{T_{\mathrm{sw}}} V_{\mathrm{HI}}. \tag{6.7}$$

6.2.2 Mid-Range Flying Capacitor Voltage Vector: $\boldsymbol{v}$

Each flying capacitor's mid-range voltage is defined as the dc value symmetrically centered between the maximum and minimum voltage, as dictated by ripple. This value can be

distinct from the time-average dc voltage, especially in multi-phase or split-phase operated converters, as discussed in Section 7.2.4. For the ReSC converters discussed here, the mid-range voltages can be derived from an assumption of zero average voltage across the inductor (i.e., zero volt-seconds) within each phase. Under this assumption, the inductor may be treated as a short circuit when applying average KVL loops to each phase. Subsequently the absolute mid-range voltages of each flying capacitor, V_{C_i}, may be expressed with respect to the high-side voltage, V_{HI}, as

$$V_{\mathrm{C}_i} = V_{\mathrm{HI}}\, v_i, \tag{6.8}$$

where v_i represents the normalized (to V_{HI}) mid-range voltage.

By applying per-phase *average* KVL to the N:1 series-parallel depicted in Fig. 6.1, during phase 2 each flying capacitor is connected in parallel with—and thus holds a voltage equal to—V_{LO}. Using the conversion ratio relationship established in (6.6), the normalized capacitor voltage vector, $\boldsymbol{v}$, is defined as

$$\begin{aligned} \boldsymbol{v}_{[1\times N_{\mathrm{C}}]} &= \begin{bmatrix} \dfrac{V_{\mathrm{C}_1}}{V_{\mathrm{HI}}} & \dfrac{V_{\mathrm{C}_2}}{V_{\mathrm{HI}}} & \cdots & \dfrac{V_{\mathrm{C}_{N_{\mathrm{C}}}}}{V_{\mathrm{HI}}} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{1}{N} & \dfrac{1}{N} & \cdots & \dfrac{1}{N} \end{bmatrix}. \end{aligned} \tag{6.9}$$

Modification for Load-Dependent Mid-Range Voltages

As previously discussed, certain multi-resonant topologies such as the MRD and CaSP converters – as well as certain resonant Dickson converters operated with split-phase switching – will exhibit load-dependent mid-range voltages. The analysis presented in [32] can be extended to account for this. An example calculation of this modified mid-range vector is presented for the CaSP converter in Section 7.2.4. Here, we describe the general construction of this vector.

We can construct this vector by defining a modified mid-range voltage vector, $v_{\mathrm{m},i}$, that has both a non-ripple-dependent and ripple-dependent term. The peak-to-peak capacitor voltage ripple is proportional to load, so this ripple-dependent term also depends on I_{HI}. This modified vector is then given by

$$v_{\mathrm{m},i} = v_{\mathrm{o},i} + k_i \cdot \frac{1}{2}\Delta v_{\mathrm{pp},i}, \tag{6.10}$$

where $\Delta v_{\mathrm{pp},i}$ is the peak-to-peak voltage ripple on capacitor i. This expression can be defined in terms of fundamental operating parameters and topological vectors, as given by

$$\Delta v_{\mathrm{pp},i} = \frac{\hat{q}_{\mathrm{C},i}}{C_i} = \frac{q_{\mathrm{HI}}\,\hat{a}_{\mathrm{C},i}}{C_0 c_i}. \tag{6.11}$$

Here, k_i is a vector of coefficients describing the dependence of the mid-range voltage on the peak-to-peak voltage ripple, $\Delta v_{\mathrm{pp},i}$, for the ith capacitor. This vector is normalized by

the high-side source, V_{HI}. The equation is written in terms of half the peak-to-peak ripple to match the form of the ripple term in the capacitor energy equation—presented in the upcoming sections as (6.41)—as this helps with the simplification process.

For a topology whose mid-range voltages are not dependent on capacitor ripple, $v_{\mathrm{o},i}$ is equal to the original v_i vector. Equivalently, for the converters discussed earlier, such as the series-parallel converter, the k_i vector is all zeros.

6.2.3 Capacitance Vector: $\boldsymbol{c}$

While some topologies have no strict constraints on capacitance sizing (e.g. the FCML converter), others require specific relative sizing to prevent hard-charging and retain simplified clocking schemes, as derived in [5, 22, 31, 54] for example. The absolute capacitance of each flying capacitor, C_i, is normalized to a single capacitance value, C_0, as

$$C_i = C_0\, c_i \tag{6.12}$$

and by doing so, the required relative capacitor relationships are preserved as the single value C_0 changes—a useful feature for the analytical passive component volume minimization performed in Section 6.4.4.

Considering the exemplar series-parallel topology, all capacitors conduct equal charge in each phase, and must express identical voltage ripple characteristics when connected in parallel during Phase 2. Thus, by $Q = CV$ (and to ensure soft-charging behavior) each capacitor must be equal in value, yielding

$$\begin{aligned} \boldsymbol{c}_{[1\times N_{\mathrm{C}}]} &= \begin{bmatrix} \dfrac{C_1}{C_0} & \dfrac{C_2}{C_0} & \cdots & \dfrac{C_{N_{\mathrm{C}}}}{C_0} \end{bmatrix} \\ &= \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}. \end{aligned} \tag{6.13}$$

6.2.4 Lumped Equivalent Capacitance Vector; $\boldsymbol{\kappa}$

During each switching phase j, the inductor forms a second-order resonant impedance network with the connected flying capacitors, which have an equivalent lumped capacitance, $C_{\mathrm{eq},j}$. This value is then normalized with respect to C_0, yielding $\boldsymbol{\kappa}$:

$$C_{\mathrm{eq},j} = C_0\, \kappa_j. \tag{6.14}$$

In Phase 1 of the example series-parallel converter (Fig. 6.1), all capacitors are connected in series and the equivalent capacitance seen by the inductor is

$$C_{\mathrm{eq},1} = C_1 || C_2 || \cdots || C_{N_{\mathrm{C}}} = \frac{1}{N_{\mathrm{C}}}\, C_0 \tag{6.15}$$

whereas in Phase 2 all capacitors are connected in parallel relative to the inductor and the equivalent capacitance is

$$C_{\mathrm{eq},2} = C_1 + C_2 + \cdots + C_{N_{\mathrm{C}}} = N_{\mathrm{C}}\, C_0. \tag{6.16}$$

More generally, the normalized equivalent capacitance vector, $\boldsymbol{\kappa}$, is defined and shown for the series-parallel topology as

$$\boldsymbol{\kappa}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \frac{C_{\mathrm{eq},1}}{C_0} \\ \frac{C_{\mathrm{eq},2}}{C_0} \end{bmatrix} = \begin{bmatrix} \frac{1}{N_\mathrm{C}} \\ N_\mathrm{C} \end{bmatrix}. \tag{6.17}$$

This section has obtained fundamental topology-dependent parameters, demonstrated on an N:1 series-parallel converter. However, in order to fully characterize the large signal behaviour of a ReSC converter both at and above resonance, switching-frequency dependencies must also be derived. Section 6.3 explores how phase timings and current waveforms depend on switching frequency.

6.3 Phase Timings

A "direct" ReSC converter can be switched at its natural resonant switching frequency, $f_{\mathrm{sw},0}$, to achieve zero current switching (ZCS) at each phase transition. However, dissimilar to "indirect" or LC-tank topologies, the switching frequency of a direct topology may also be increased without incurring increased circulating currents [74]. Subsequently, we define a free parameter, Γ, as the ratio of the actual switching frequency, f_sw, to the natural resonant switching frequency

$$\Gamma = \frac{f_\mathrm{sw}}{f_{\mathrm{sw},0}} = \frac{T_{\mathrm{sw},0}}{T_\mathrm{sw}}. \tag{6.18}$$

Resonant ZCS is obtainable at $\Gamma = 1$ (i.e., at-resonance operation), while for $\Gamma > 1$ (i.e., above-resonance operation) the inductor enters continuous conduction mode (CCM). In practice, values of $\Gamma < 1$ (i.e., below-resonance operation) would only be implemented with a modified discontinuous conduction mode (DCM) or dynamic off-time modulation (DOTM) [75, 76], otherwise SSL losses would reemerge. The motivation for operation above resonance operation has been explored in [6, 12, 69, 74, 77–79] as a method for reducing conduction losses and improving overall efficiency. However, for several topologies—including the FCML converter and resonant N-phase implementations of Cockcroft-Walton and Dickson converters [51, 80]—the phase durations depend heavily on the relationship between the natural resonant switching frequency and the implemented f_sw.

Continuous closed-form expressions are derived for phase-timing durations which minimize the peak, peak-to-peak, and rms inductor current both at resonance and for arbitrary frequencies above resonance. The presented analysis yields a robust method for explicitly determining the phase durations.

Phase Duration Vector: $\boldsymbol{\tau}$

Each phase duration, t_j, can be defined in terms of the full switching period, T_{sw}, using a normalization parameter, τ_j,

$$t_j = T_{\text{sw}}\,\tau_j \tag{6.19}$$

where T_{sw} defines the sum of all N_{P} phase durations

$$T_{\text{sw}} = \sum_{j=1}^{N_{\text{P}}} t_j. \tag{6.20}$$

The normalized phase duration vector, $\boldsymbol{\tau}$, is deduced from the resonance of the inductor current $i_L(t)$ for each topology and is a function of Γ.

When operating at the resonant switching frequency, $f_{\text{sw},0}$ (i.e., $\Gamma = 1$), each phase is half-wave resonant with $i_{\text{L}}(t)$ starting and ending at 0 A. Thus the phase duration, t_j, equals half the duration of the natural resonant period, $T_{0,j}$, of the lumped LC resonant tank in the jth phase or

$$t_j|_{\Gamma=1} = T_{\text{sw},0} \cdot \tau_j|_{\Gamma=1} = \frac{T_{0,j}}{2} \tag{6.21}$$

as per (6.19).

The natural angular frequency, $\omega_{0,j}$, associated with $T_{0,j}$ can be expressed as

$$\omega_{0,j} = \frac{1}{\sqrt{L \cdot C_0 \kappa_j}} = \frac{2\pi}{T_{0,j}} = \frac{\pi}{t_j|_{\Gamma=1}} \tag{6.22}$$

since parameter κ_j defines the lumped equivalent capacitance.

Calculating the phase durations, t_j, for operation above resonance (i.e., $\Gamma > 1$) requires further analysis. Within each phase j, if the inductor is subjected to zero volt-seconds, then it forms a symmetrically centered sinusoidal segment[1], as depicted in Fig. 6.2. Continuity in $i_{\text{L}}(t)$ between adjacent phases (including $j = N_{\text{P}}$ and $j = 1$) can be expressed mathematically as

$$I_{\text{pk},j} \cos\left(\omega_{0,j} \frac{t_j}{2}\right) = I_{\text{pk},j+1} \cos\left(\omega_{0,j+1} \frac{-t_{j+1}}{2}\right), \quad \forall j \leq N_{\text{P}} \tag{6.23}$$

where $I_{\text{pk},j}$ is the peak current in phase j.

Furthermore during phase j, the inductor conducts charge $q_{\text{L},j}$, where

$$\begin{aligned} q_{\text{L},j} &= \int_{\frac{t_j}{2}}^{\frac{t_j}{2}} I_{\text{pk},j} \cos(\omega_{0,j}\, t)\, dt \\ &= \frac{2 I_{\text{pk},j}}{\omega_{0,j}} \sin\left(\omega_{0,j} \frac{t_j}{2}\right) = q_{\text{HI}}\, a_{\text{L},j}, \quad \forall j \leq N_{\text{P}} \end{aligned} \tag{6.24}$$

[1]Appendix A in [32] shows that timings calculated under this assumption always satisfy both charge balance and inductor current continuity in periodic steady-state.

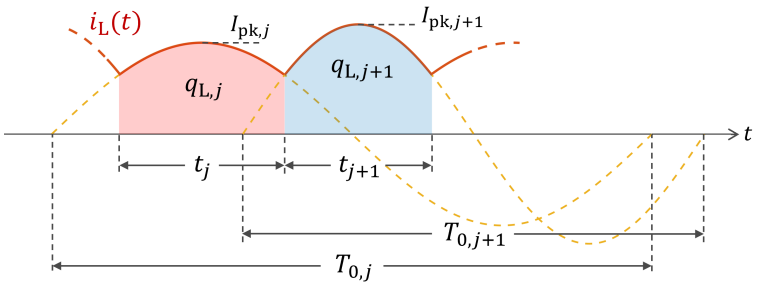


Figure 6.2: Two adjacent phases of the inductor current waveform, $i_L(t)$, operating above resonance. Each phase constitutes a symmetrically centered sinusoidal segment with angular frequency governed by (6.22).

which relates to the known normalized charge flow matrix, $\boldsymbol{a}_{\mathrm{L}}$, and can be rearranged with respect to $I_{\mathrm{pk},j}$ as

$$I_{\mathrm{pk},j} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2\sin\left(\omega_{0,j}\frac{t_j}{2}\right)}, \quad \forall j \leq N_{\mathrm{P}}. \tag{6.25}$$

Combining the phase-to-phase current continuity (6.23) and per-phase charge flow (6.25) yields

$$\frac{a_{\mathrm{L},j}\, \omega_{0,j}}{\tan\left(\omega_{0,j}\frac{t_j}{2}\right)} = \frac{a_{\mathrm{L},j+1}\, \omega_{0,j+1}}{\tan\left(\omega_{0,j+1}\frac{t_{j+1}}{2}\right)}, \quad \forall j \leq N_{\mathrm{P}}. \tag{6.26}$$

Equation (6.26) can be solved using (6.22) and (6.19), to determine appropriate normalized phase durations, τ_j, for each phase. For all two-phase converters, τ_j is independent of Γ, as will be demonstrated for the series-parallel converter. However, these phase durations can vary with Γ for certain converters, such as the FCML converter [79]. For the MRD and CaSP converters explored throughout this chapter and Chapter 7, the τ vector is also independent of Γ. An example of this calculation is presented for the CaSP converter in Section 7.2.4. However, for the resonant Dickson converter operating with split-phase, these phase timings do not remain constant fractions of the overall switching period as the switching frequency increases above resonance, complicating the analysis.

Series-Parallel Converter

Consider the two-phase series-parallel topology with arbitrary conversion ratio N in Fig. 6.1 as an example. Substituting the normalized equivalent capacitance vector, κ_j, from (6.17), into the natural angular frequency, $\omega_{0,j}$, during each phase in (6.22) yields

$$\omega_{0,1} = \sqrt{N-1} \cdot \frac{1}{\sqrt{LC_0}} \tag{6.27}$$

and

$$\omega_{0,2} = \frac{1}{\sqrt{N-1}} \cdot \frac{1}{\sqrt{LC_0}} \tag{6.28}$$

with the corresponding relationship between these two frequencies as

$$\omega_{0,1} = (N-1)\,\omega_{0,2}. \tag{6.29}$$

Next, (6.29) and values for normalized inductor charge flow, $a_{\mathrm{L},j}$, given in (6.5) are substituted into the steady-state charge flow and inductor continuity constraint given by (6.26), yielding

$$\tan\left(\omega_{0,1}\frac{t_1}{2}\right) = \tan\left(\frac{\omega_{0,1}}{N-1} \cdot \frac{t_2}{2}\right). \tag{6.30}$$

The argument of each tangent is then equated to find a relationship between the two phase time durations

$$t_1 = \frac{1}{N-1}\,t_2. \tag{6.31}$$

For this two-phase topology

$$T_{\mathrm{sw}} = t_1 + t_2, \tag{6.32}$$

and therefore the normalized phase durations, τ_j, become

$$\begin{aligned} \boldsymbol{\tau}_{[N_{\mathrm{P}}\times 1]} &= \begin{bmatrix} \frac{t_1}{T_{\mathrm{sw}}} \\ \frac{t_2}{T_{\mathrm{sw}}} \end{bmatrix} \\ &= \begin{bmatrix} \frac{1}{N} \\ \frac{N-1}{N} \end{bmatrix} \end{aligned} \tag{6.33}$$

where $\boldsymbol{\tau}$ only varies with conversion ratio and not Γ.

In addition, substituting (6.29) and (6.31) into (6.23) reveals $I_{\mathrm{pk},1} = I_{\mathrm{pk},2}$—a consistent result for all two-phase converters considered in this work.

6.4 Passive Volume Calculation

To characterize passive component volume, and subsequently enable converter size minimization, expressions are derived for both total flying capacitor and inductor volume, as dictated by their peak energy storage requirements.

A direct energy method is demonstrated here, expanding on the flying capacitor analysis in [22], and using the phase timings derived in Section 6.3 to further obtain expressions for peak inductor energy. Dissimilar to [42], this approach circumvents the need to analytically generalize and integrate instantaneous power waveforms (i.e., $p(t) = v(t) \cdot i(t)$) for every passive component.

While the results of the proposed method and [42] are equivalent for operation at resonance, the proposed method generalizes the passive component requirements for arbitrary switching frequencies *above* resonance (i.e., $\Gamma > 1$) where both the peak flying capacitor voltage and inductor current are diminished.

6.4.1 Total Peak Flying Capacitor Energy Storage

To calculate the total flying capacitor energy storage requirement, consider the peak voltage expressed on each flying capacitor, as a function of load, while noting these events may not occur simultaneously in time for each flying capacitor. Moreover, since a flying capacitor may admit charge over multiple phases before achieving its peak voltage—as is the case for the MRD and CaSP topologies—a modified charge flow quantity $\hat{a}_{\mathrm{C},i}$ is defined describing the maximum deviation in stored charge on the ith flying capacitor throughout a full switching cycle. For converters in which each flying capacitor only admits charge during a single phase, $\hat{a}_{\mathrm{C},i}$ is defined as

$$\hat{a}_{\mathrm{C},i} = \max_{j \in [N_{\mathrm{P}}]} a_{\mathrm{C},ji}, \tag{6.34}$$

which for two-phase converters may be simplified to

$$\hat{a}_{\mathrm{C},i} = |a_{\mathrm{C},ji}| \qquad \forall j \in \{1, 2\} \tag{6.35}$$

since each capacitor must admit and release the same quantity of charge across both phases in periodic steady-state.

For converters such as the MRD and CaSP converter, $\hat{a}_{\mathrm{C},i}$ should be calculated using the more generalized expression

$$\hat{a}_{\mathrm{C},i} = \max_{x \in [N_{\mathrm{P}}]} \left(\sum_{j=1}^{x} a_{\mathrm{C},ji} \right) - \min_{x \in [N_{\mathrm{P}}]} \left(\sum_{j=1}^{x} a_{\mathrm{C},ji} \right) \tag{6.36}$$

which is applicable to any charge flow vector, a_{C}, so long as it satisfies the periodic steady state condition in (6.3).

The first term determines the peak positive (maximum) accumulated charge, while the second term determines the peak negative (minimum) accumulated charge. The difference between these values is the peak-to-peak charge ripple experienced by the capacitor.

Consider an example calculation of $\hat{a}_{\mathrm{C},1}$ for a capacitor C_1 that experiences some arbitrary normalized capacitor charge flow vector

$$a_{\mathrm{C},1} = \frac{q_{\mathrm{C},1}}{q_{\mathrm{HI}}} = \begin{bmatrix} 1 & -1 & -1 & 1 \end{bmatrix}. \tag{6.37}$$

A possible capacitor current waveform, $i_{\mathrm{C},1}(t)$, corresponding to this charge vector, and its associated voltage waveform, $v_{\mathrm{C},1}(t)$, are shown in Fig. 6.3, where a constant current during each phase is assumed for simplicity. The capacitor voltage ripple is centered around

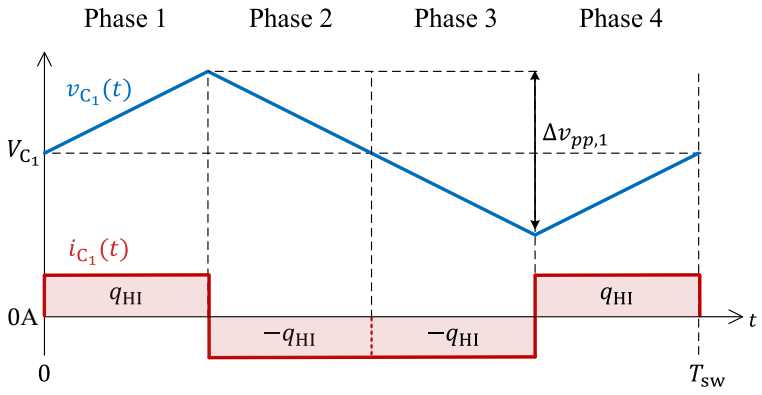


Figure 6.3: Exemplar capacitor voltage and current waveforms for the given normalized charge flow vector $a_{C,1}$ in (6.37). The capacitor is charged by quantity q_{HI} in phases 1 and 4, and discharged by quantity $-q_{HI}$ in Phases 2 and 3. For simplicity, constant capacitor current and linear capacitor voltage are shown.

the mid-range voltage, V_{C_1}, while the capacitor current is centered around zero to satisfy periodic steady-state conditions. The charge expelled or received per phase corresponds to the area under the current waveform during that phase, and has a magnitude of q_{HI} as per (6.1).

By inspecting Fig. 6.3 or evaluating (6.36), we can determine that the peak positive accumulated charge occurs at the end of phase $j = 1$, and the peak negative accumulated charge occurs at the end of phase $j = 3$.

$$\max_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) = \sum_{j=1}^{1} a_{C,ji} = 1 \tag{6.38}$$

$$\min_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) = \sum_{j=1}^{3} a_{C,ji} = -1. \tag{6.39}$$

Therefore, the modified charge quantity for this example evaluates to

$$\begin{aligned}\hat{a}_{C,1} &= \max_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) - \min_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right)\\ &= 1-(-1) = 2.\end{aligned}$$

This value can then be substituted into (6.40) to find the peak-to-peak voltage ripple, $\Delta v_{pp,1}$, for capacitor C_1 (also depicted in Fig. 6.3).

In general, the peak-to-peak voltage ripple, $\Delta v_{pp,i}$, on each flying capacitor, i, may be described as

$$\Delta v_{pp,i} = \frac{\hat{q}_{C,i}}{C_i} = \frac{q_{HI}\,\hat{a}_{C,i}}{C_0 c_i} \tag{6.40}$$

The peak energy storage requirement should be calculated for the phase j in which $E_{\mathrm{C,pk},i}$ is maximized for the ith capacitor. This can be expressed as

$$\begin{aligned} E_{\mathrm{C,pk},i} &= \max_{j\in[N_{\mathrm{P}}]} \left\{ \frac{1}{2} C_i \, V_{\mathrm{pk,C}_i}^2 \right\} \\ &= \frac{1}{2} C_0 c_i \cdot \left(V_{\mathrm{HI}} v_i + \frac{1}{2} \Delta v_{\mathrm{pp},i} \right)^2 \end{aligned} \tag{6.41}$$

where the peak capacitor voltage is the mid-range voltage plus half the peak-to-peak voltage ripple, or $V_{\mathrm{pk,C}_i} = V_{\mathrm{C}_i} + \frac{1}{2}\Delta v_{\mathrm{pp},i}$. The total peak flying capacitor energy over all N_{C} capacitors is then

$$E_{\mathrm{C,tot}} = \sum_{i=1}^{N_C} E_{\mathrm{C,pk},i}. \tag{6.42}$$

The total capacitor peak energy summed over every capacitor can then be manipulated into an expression based on operating conditions (C_0, V_{HI}, and q_{HI}) and basic topological vectors (c_i, v_i, and $\hat{a}_{\mathrm{C},i}$) as follows

$$\begin{aligned} E_{\mathrm{C,tot}} &= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \cdot \left(V_{\mathrm{HI}} v_i + \frac{1}{2} \Delta v_{\mathrm{pp},i} \right)^2 \\ &= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \cdot \left(V_{\mathrm{HI}} v_i + \frac{1}{2} \frac{q_{\mathrm{HI}} \hat{a}_{\mathrm{C},i}}{C_0 c_i} \right)^2 \\ &= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \left(V_{\mathrm{HI}}^2 v_i^2 + V_{\mathrm{HI}} v_i \frac{q_{\mathrm{HI}} \hat{a}_{\mathrm{C},i}}{C_0 c_i} + \frac{1}{4} \frac{q_{\mathrm{HI}}^2 \hat{a}_{\mathrm{C},i}^2}{C_0^2 c_i^2} \right) \\ &= \sum_{i=1}^{N_C} \left(\frac{1}{2} C_0 V_{\mathrm{HI}}^2 c_i v_i^2 \right) + \sum_{i=1}^{N_C} \left(\frac{1}{2} V_{\mathrm{HI}} q_{\mathrm{HI}} v_i \hat{a}_{\mathrm{C},i} \right) + \sum_{i=1}^{N_C} \left(\frac{q_{\mathrm{HI}}^2 \hat{a}_{\mathrm{C},i}^2}{8 C_0 c_i} \right) \end{aligned} \tag{6.43}$$

This can then be expressed as

$$E_{\mathrm{C,tot}} = \frac{C_0 V_{\mathrm{HI}}^2}{2} A_1 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}}{2} A_2 + \frac{q_{\mathrm{HI}}^2}{8 C_0} A_3 \tag{6.44}$$

where

$$A_1 = \sum_{i=1}^{N_{\mathrm{C}}} c_i v_i^2 \tag{6.45}$$

$$A_2 = \sum_{i=1}^{N_{\mathrm{C}}} v_i \hat{a}_{\mathrm{C},i} \tag{6.46}$$

$$A_3 = \sum_{i=1}^{N_{\mathrm{C}}} \frac{\hat{a}_{\mathrm{C},i}^2}{c_i} \tag{6.47}$$

This result is similar to that described in [22] where notation α, β, θ is used in place of A_1, A_2, and A_3. Furthermore, the impact of switching frequency on capacitor ripple, and therefore peak storage, is subsumed within q_{HI}, recalling (6.2) and (6.18).

Extension to Ripple-Dependent Mid-Range Voltages

As mentioned previously, certain multi-resonant topologies—e.g., the multi-resonant doubler [73] and the cascaded series-parallel [18]—or switching schemes—e.g., split-phase switching [22,29,53]—have mid-range voltages that are dependent on capacitor peak-to-peak ripple, and therefore on load.

The effect of this can be accounted for by incorporating the modified capacitor mid-range voltage vector, as described in Section 6.2.2, and repeated here for convenience.

$$v_{\text{m},i} = v_{\text{o},i} + k_i \cdot \frac{1}{2}\Delta v_{\text{pp},i}$$

We can now substitute (6.10) into (6.41) to find an updated equation for peak capacitor energy. The steps for this substitution are given below

$$\begin{aligned}
E_{\text{C,tot}} &= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \cdot \left(V_{\text{HI}} \left(v_{\text{o},i} + k_i \cdot \frac{1}{2}\Delta v_{\text{pp}_i} \right) + \frac{1}{2}\Delta v_{\text{pp}_i} \right)^2 \\
&= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \cdot \left(V_{\text{HI}} \left(v_{\text{o},i} + k_i \cdot \frac{1}{2} \frac{q_{\text{HI}} \hat{a}_{\text{C},i}}{C_0 c_i} \right) + \frac{1}{2} \frac{q_{\text{HI}} \hat{a}_{\text{C},i}}{2 C_0 c_i} \right)^2 \\
&= \sum_{i=1}^{N_C} \frac{1}{2} C_0 c_i \cdot \left(V_{\text{HI}} v_{\text{o},i} + (V_{\text{HI}} k_i + 1) \cdot \frac{1}{2} \frac{q_{\text{HI}} \hat{a}_{\text{C},i}}{C_0 c_i} \right)^2
\end{aligned} \tag{6.48}$$

This can be simplified to

$$\begin{aligned}
E_{\text{C,tot}} = {} & \frac{C_0 V_{\text{HI}}^2}{2} \sum_{i=1}^{N_C} c_i v_{\text{o},i}^2 + \frac{V_{\text{HI}} q_{\text{HI}}}{2} \sum_{i=1}^{N_C} v_{\text{o},i} \hat{a}_{\text{C},i} + \frac{q_{\text{HI}}^2}{8 C_0} \sum_{i=1}^{N_C} \frac{\hat{a}_{\text{C},i}^2}{c_i} \\
& + \frac{V_{\text{HI}}^2 q_{\text{HI}}}{2} \sum_{i=1}^{N_C} k_i v_{\text{o},i} \hat{a}_{\text{C},i} + \frac{V_{\text{HI}}^2 q_{\text{HI}}^2}{8 C_0} \sum_{i=1}^{N_C} \frac{k_i^2 \hat{a}_{\text{C},i}^2}{c_i} + \frac{V_{\text{HI}} q_{\text{HI}}^2}{4 C_0} \sum_{i=1}^{N_C} \frac{k_i \hat{a}_{\text{C},i}^2}{c_i}
\end{aligned} \tag{6.49}$$

where the first three terms of (6.49) are the same as (6.43), and the last three terms are new expressions that depend on the peak-to-peak capacitor ripple.

We can define additional A variables as we did in (6.45) - (6.47), as given below

$$A_4 = \sum_{i=1}^{N_\mathrm{C}} k_i v_{\mathrm{o},i} \hat{a}_{\mathrm{C},i} \tag{6.50}$$

$$A_5 = \sum_{i=1}^{N_\mathrm{C}} \frac{k_i^2 \hat{a}_{\mathrm{C},i}^2}{c_i} \tag{6.51}$$

$$A_6 = \sum_{i=1}^{N_\mathrm{C}} \frac{k_i \hat{a}_{\mathrm{C},i}^2}{c_i} \tag{6.52}$$

The total peak capacitor energy over all i capacitors can then be expressed as

$$E_{\mathrm{C,tot}} = \frac{C_0 V_{\mathrm{HI}}^2}{2} A_1 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}}{2} A_2 + \frac{q_{\mathrm{HI}}^2}{8C_0} A_3 + \frac{V_{\mathrm{HI}}^2 q_{\mathrm{HI}}}{2} A_4 + \frac{V_{\mathrm{HI}}^2 q_{\mathrm{HI}}^2}{8C_0} A_5 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}^2}{4C_0} A_6 \tag{6.53}$$

Note that if $k_i = 0$ for all i, then (6.53) simplifies back to (6.43), as expected. As long as a converter's mid-range voltages can be split apart into ripple-independent and ripple-dependent terms, the peak capacitor energy can be calculated in this manner. For example, this methodology could also be used to calculate the peak capacitor energy for a resonant Dickson converter operating with split-phase switching, provided the mid-range voltage vector is known.

6.4.2 Peak Inductor Energy Storage

Peak inductor energy storage can now be calculated, in a manner that also accounts for converter operation above resonance (i.e., $\Gamma > 1$). For simplicity, the inductor is assumed to have a constant inductance with applied current bias and to be saturation limited, as is often the case for low-loss ferrite materials. Consequently, the minimum inductor volume is proportional to the peak energy stored therein.

First, the per-phase resonance equation (6.22) is rearranged to give

$$L = \frac{1}{\omega_{0,j}^2 \kappa_j C_0} \tag{6.54}$$

and (6.18), (6.19), (6.21), and (6.22) are substituted into the peak inductor current in (6.25)

$$I_{\mathrm{pk},j} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2 \sin\left(\omega_{0,j} \frac{t_j}{2}\right)} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2 \sin\left(\frac{\pi}{2\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}. \tag{6.55}$$

Using (6.54) and (6.55), the peak inductor energy over all phases, j, can then be expressed as

$$E_{\mathrm{L,pk}} = \max_{j \in [N_\mathrm{P}]} \left\{ \frac{1}{2} L\, I_{\mathrm{pk},j}^2 \right\} = \frac{q_{\mathrm{HI}}^2}{2C_0} B_1 \tag{6.56}$$

where

$$B_1 = \max_{j\in[N_\mathrm{P}]} \left\{ \frac{a_{\mathrm{L},j}^2}{4\kappa_j} \cdot \frac{1}{\sin^2\left(\frac{\pi}{2\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)} \right\}. \tag{6.57}$$

For converters with τ_j independent of Γ, B_1 is simplified since $\tau_j = \tau_j|_{\Gamma=1}$. Furthermore, for all converters operating in resonant ZCS mode (i.e., $\Gamma = 1$), (6.57) reduces to

$$B_1\big|_{\Gamma=1} = \max_{j\in[N_\mathrm{P}]} \left\{ \frac{a_{\mathrm{L},j}^2}{4\kappa_j} \right\} \tag{6.58}$$

6.4.3 Volume Calculation

After the peak energy storage requirements are defined for all capacitors and inductors, using the methodology above, this total passive energy can be converter to a total passive volume using the respective energy densities of the passive components.

The total volume of the capacitive elements can be computed as

$$\mathrm{Vol}_{\mathrm{C,tot}} = \frac{E_{\mathrm{C,tot}}}{\rho_\mathrm{C}} \tag{6.59}$$

where ρ_C is the volumetric energy density ($\mathrm{J/m^3}$) of the chosen capacitor technology. Similarly, the total inductor volume can then be computed as

$$\mathrm{Vol}_\mathrm{L} = \frac{E_{\mathrm{L,pk}}}{\rho_\mathrm{L}} = \frac{q_\mathrm{HI}^2}{2\rho_L C_0} B_1 \tag{6.60}$$

where ρ_L is the volumetric energy density ($\mathrm{J/m^3}$) of the inductor.

6.4.4 Minimization of Passive Components

Passive components typically comprise a large majority of a converter's volume, and therefore it may be desirable to size the passive components such that they result in the minimum total passive volume. This can be considered a proxy for minimizing the converter's overall volume.

To carry out this minimization, an expression for total passive volume—as defined by peak energy storage requirements—is constructed using (6.59) and (6.60).

$$\mathrm{Vol}_\mathrm{tot} = \mathrm{Vol}_\mathrm{C} + \mathrm{Vol}_\mathrm{L} \tag{6.61}$$

Depending on whether the converter exhibits load-dependent mid-range voltages, the simple (6.43) or modified (6.53) expressions for $E_{\mathrm{C,tot}}$ can be used.

Assuming the former, the total passive volume can be expressed as

$$\mathrm{Vol}_\mathrm{tot} = \left(\frac{C_0 V_\mathrm{HI}^2}{2\rho_\mathrm{C}} A_1 + \frac{V_\mathrm{HI} q_\mathrm{HI}}{2\rho_\mathrm{C}} A_2 + \frac{q_\mathrm{HI}^2}{8\rho_\mathrm{C} C_0} A_3 \right) + \frac{q_\mathrm{HI}^2}{2\rho_\mathrm{L} C_0} B_1. \tag{6.62}$$

The total passive volume is then minimized by differentiating with respect to the normalized capacitance C_0

$$\left.\frac{\partial \mathrm{Vol}_{\mathrm{tot}}}{\partial C_0}\right|_{C_0=C_0^*} = 0 = \frac{V_{\mathrm{HI}}^2}{2\rho_{\mathrm{C}}} A_1 - \frac{q_{\mathrm{HI}}^2}{8\rho_{\mathrm{C}} C_0^{*2}} A_3 - \frac{q_{\mathrm{HI}}^2}{2\rho_{\mathrm{L}} C_0^{*2}} B_1 \tag{6.63}$$

which is solved explicitly for the minimizing normalized capacitance C_0^* as

$$C_0^* = \frac{q_{\mathrm{HI}}}{V_{\mathrm{HI}}} \sqrt{\frac{\frac{1}{4}A_3 + \frac{\rho_{\mathrm{C}}}{\rho_{\mathrm{L}}} B_1}{A_1}} \tag{6.64}$$

for a given Γ, V_{HI}, q_{HI}, and passive energy density ratio $\rho_{\mathrm{C}}/\rho_{\mathrm{L}}$. The composite terms A_1, A_3, and B_1 are all known functions of topology and a given choice of switching frequency (i.e., Γ). By then substituting C_0^* into (6.54), we obtain the corresponding inductance value, L^*, that results in our selected resonant frequency, $f_{\mathrm{sw},0}$, while minimizing passive volume.

Back substituting (6.64) into (6.62) and replacing q_{HI} using (6.2) yields the minimal achievable total passive component volume,

$$\mathrm{Vol}_{\mathrm{tot}}^* = \frac{P_{\mathrm{HI}}}{f_{\mathrm{sw}}\,\rho_{\mathrm{C}}} \left(\frac{A_2}{2} + \sqrt{A_1 \left(\frac{1}{4}A_3 + \frac{\rho_{\mathrm{C}}}{\rho_{\mathrm{L}}} B_1 \right)} \right). \tag{6.65}$$

Furthermore, (6.65) can be normalized with respect to power throughput, natural resonant switching frequency $f_{\mathrm{sw},0}$ (as per (6.18)), and capacitor energy density ρ_{C}. The resulting normalized minimum total passive component volume, M_{vol}^*, may be used to directly compare different topologies and is solely a function of the above-resonance parameter, Γ; the ratio of passive densities, $\rho_{\mathrm{C}}/\rho_{\mathrm{L}}$; and invariant topological parameters:

$$M_{\mathrm{vol}}^* = \frac{\mathrm{Vol}_{\mathrm{tot}}^*}{\left(\frac{P_{\mathrm{HI}}}{f_{\mathrm{sw},0}\,\rho_{\mathrm{C}}}\right)} = \frac{1}{\Gamma} \left(\frac{A_2}{2} + \sqrt{A_1 \left(\frac{1}{4}A_3 + \frac{\rho_{\mathrm{C}}}{\rho_{\mathrm{L}}} B_1 \right)} \right). \tag{6.66}$$

This is a similar normalized passive volume metric as obtained in [42], but now includes terms accounting for above resonance operation.

Extension to Ripple-Dependent Mid-Range Voltages

In the case of ripple-dependent mid-range voltages, the total passive volume can be expressed as

$$\mathrm{Vol}_{\mathrm{tot}} = \left(\frac{C_0 V_{\mathrm{HI}}^2}{2\rho_{\mathrm{C}}} A_1 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}}{2\rho_{\mathrm{C}}} A_2 + \frac{q_{\mathrm{HI}}^2}{8\rho_{\mathrm{C}} C_0} A_3 \right. \tag{6.67}$$

$$\left. + \frac{V_{\mathrm{HI}}^2 q_{\mathrm{HI}}}{2\rho_{\mathrm{C}}} A_4 + \frac{V_{\mathrm{HI}}^2 q_{\mathrm{HI}}^2}{8\rho_{\mathrm{C}} C_0} A_5 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}^2}{4\rho_{\mathrm{C}} C_0} A_6 \right) + \frac{q_{\mathrm{HI}}^2}{2\rho_{\mathrm{L}} C_0} B_1. \tag{6.68}$$

This new expression for passive volume can be minimized by differentiating with respect to the normalized capacitance C_0, as before.

$$\left.\frac{\partial \mathrm{Vol}_{\mathrm{tot}}}{\partial C_0}\right|_{C_0=C_0^*} = 0 = \frac{V_{\mathrm{HI}}^2}{2\rho_{\mathrm{C}}}A_1 - \frac{q_{\mathrm{HI}}^2}{8\rho_{\mathrm{C}}C_0^{*2}}A_3 - \frac{V_{\mathrm{HI}}^2 q_{\mathrm{HI}}^2}{8\rho_{\mathrm{C}}C_0^{*2}}A_5 - \frac{V_{\mathrm{HI}}q_{\mathrm{HI}}^2}{4\rho_{\mathrm{C}}C_0^{*2}}A_6 - \frac{q_{\mathrm{HI}}^2}{2\rho_{\mathrm{L}}C_0^{*2}}B_1 \tag{6.69}$$

In the case of $A_5 = A_6 = 0$, this equation simplifies back to the ripple-independent expression given in (6.63).

This expression can also be solved for the minimizing normalized capacitance C_0^* as

$$C_0^* = \frac{q_{\mathrm{HI}}}{V_{\mathrm{HI}}}\sqrt{\frac{\frac{1}{4}A_3 + \frac{V_{\mathrm{HI}}^2}{4\rho_{\mathrm{L}}^2}A_5 + \frac{V_{\mathrm{HI}}}{2}A_6 + \frac{\rho_{\mathrm{C}}}{\rho_{\mathrm{L}}}B_1}{A_1}} \tag{6.70}$$

which simplifies to (6.64) if $A_5 = A_6 = 0$. Note that now (6.70) contains terms that are dependent on V_{HI} inside the square root function, making it unwieldy to attempt the normalization method used for the ripple-independent case. However, it is still possible to compare absolute volume, or to normalize the results to some specific operating condition corresponding to a set of P_{HI} and f_{SW}. In addition, a similar normalization can be used as in [42,81] where the calculated absolute volume can be normalized to the basic 2-to-1 hybrid SC converter operating at the same P_{HI} and f_{SW}.

6.5 Comparison of ReSC Converter Passive Volume

Table 6.2: Operating Parameters for Passive Volume Comparison

Parameter	Description	Value
Power Stage		
V_{HI}	High-side Voltage	48 V
P_{HI}	High-side power	500 W
$f_{\mathrm{SW},0}$	Resonant frequency	100 kHz
ρ_{C}	Capacitor energy density	100 μJ / m^3
ρ_{L}	Inductor energy density	100 μJ / m^3

The minimum passive volume at the operating conditions summarized in Table 6.2 is plotted across a range of conversion ratios, N, in Fig. 6.4 for the Dickson (odd), Fibonnaci, cascaded series-parallel (CaSP) and series-parallel topologies.

The relative energy density ratio of capacitors to inductors in this plot is chosen as $\rho_{\mathrm{C}}/\rho_{\mathrm{L}} = 100$, following the empirical scaling trends analyzed in [2]. As corroborated with

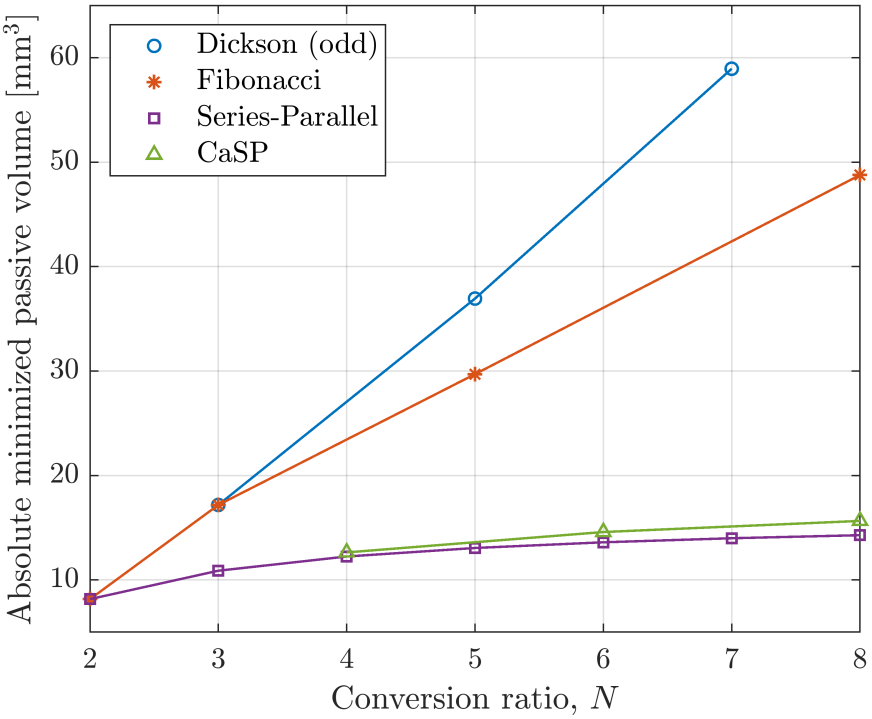


Figure 6.4: Minimized passive volume for the Dickson (odd), Fibonacci, Cascaded Series-Parallel (CaSP), and Series-Parallel converters, at the operating conditions summarized in Table 6.2. The converters are assumed to be operated at resonance.

the results obtained in [42], the Dickson converter exhibits the highest passive volume, while the series-parallel converter exhibits the lowest passive volume. The CaSP converter, which is a multi-resonant variant of the series-parallel, also exhibits quite low passive volume, that is only slightly higher than the series-parallel. This also matches trends published in [81], though that work did not include the correction factor for the ripple-dependent mid-range voltages on the capacitors.

6.6 Chapter Summary

This chapter presented an analytical framework to both calculate the passive volume based on peak energy storage requirements, followed by an optimization procedure to select the normalizing capacitance, C_0, and inductance, L, that will result in the overall minimized passive volume. The method presented in [32] was also extended here to incorporate hybrid SC topologies that have load-dependent mid-range capacitor voltages, through the use of the modified $v_{\mathrm{m,i}}$ vector. The step-by-step procedure for calculating the passive volume of the CaSP converter will be carried out in Chapter 7.

Chapter 7

The Cascaded Series-Parallel (CaSP) Converter

7.1 Introduction

Hybrid switched-capacitor (SC) and resonant switched-capacitor (ReSC) converter topologies can achieve high efficiency and high power density due to their efficient switch utilization and use of high energy density capacitors, as well as the use of resonant inductors to ensure full soft-charging. However, the number of components (switches and capacitors) increases proportionally with the conversion ratio, increasing circuit complexity and potentially reducing performance. Because of this, hybrid SC converters with multiple operating states per switching cycle are attractive for high-step down applications as they can achieve the same conversion ratio as two-phase SC converters with fewer capacitors and switches [82]. This makes multi-phase SC converters very attractive for use in large conversion ratio applications, where component count may otherwise be very high for topologies such as the series-parallel converter. This chapter discusses one such multi-resonant topology, called the cascaded series-parallel (CaSP) converter. This topology can be extended to any even-N conversion ratio greater than a 4-to-1 conversion (as all hybrid SC topologies converge to the same 2-to-1, single-flying-capacitor structure).

First, an overview of the theory of operation is presented, detailing the soft-charging capabilities and resonant behavior of the converter. Then, the passive volume analysis presented in Chapter 6 is applied to the CaSP converter, so that its performance can be compared to more conventional ReSC converters such as the Dickson and series-parallel topologies. Finally, high performance hardware prototypes are presented, at 6-to-1 and 8-to-1 step-down ratios. These prototypes were designed for a 48 V bus input, for data center intermediate bus power architectures.

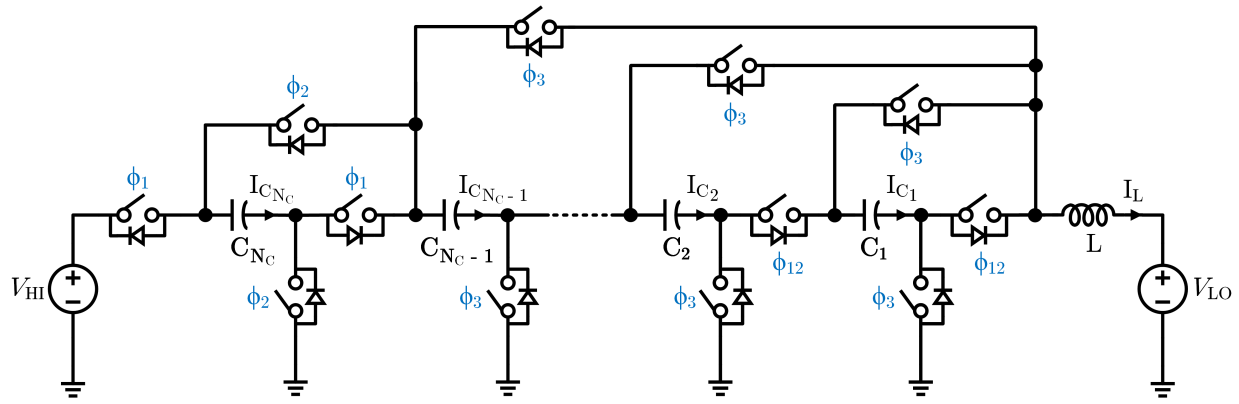


Figure 7.1: Schematic drawing of a general N-level Cascaded Series-Parallel (CaSP) converter, with switch control signals labeled. Here, N_C refers to the total number of flying capacitors.

7.2 Theory of Operation

Fig. 7.1 shows a general N-level Cascaded Series-Parallel (CaSP) converter. This topology can be viewed as a 2-to-1 stage merged with an $\frac{N}{2}$ series-parallel stage. The 2-to-1 stage both charges and discharges its single flying capacitor, C_{N_C}, entirely during the series-mode of the $\frac{N}{2}$ series-parallel converter. The CaSP can be operated as a step-down or step-up converter, depending on whether the high-side source, V_{HI}, or low-side source, V_{LO}, is used as the input. As the conventional two-phase series-parallel converter is able to achieve any conversion ratio $N > 2$, the CaSP converter can achieve any even-N conversion ratio of 4-to-1 or higher, due to the presence of the 2-to-1 stage at the high-side input, V_{HI}.

7.2.1 Charge Flow

Using the charge flow analysis presented in [1], the overall charge that must flow through each flying capacitor can be determined for each operating phase. Fig. 7.2 shows charge flow for a step-down converter, where V_{HI} is taken as the input, and V_{LO} is taken as the output. For a step-up converter, the overall charge relationships would remain the same, but charge would instead flow from V_{LO} to V_{HI}.

Fig. 7.2a shows the charge flow during Phase 1. During this phase, C_{N_C} is charged from the input, V_{HI}, by q_0. This charge also flows into the series-connected flying capacitors C_{N_C-1} through C_1, which comprise the $\frac{N}{2}$ series-parallel converter. During Phase 2, shown in Fig. 7.2b, the input is disconnected and C_{N_C} now discharges into the series-connection of C_{N_C-1} through C_1. During Phase 3, shown in Fig. 7.2c, the 2-to-1 flying capacitor has completed its charge and discharge cycle, and is disconnected from the rest of the switch-capacitor network. The output stage now operates in a parallel mode where C_{N_C-1} through C_1 are connected in parallel across the inductor and low-side source, V_{LO}. The CaSP con-

verter therefore will operate with three phases, independent of conversion ratio N. This is dissimilar to multi-resonant converters like the multi-resonant doubler (MRD) converter, where the number of phases scales with N as each capacitor is sequentially charged and discharged [73].

The charge during phase j can be recorded in the form of a charge flow vector given by

$$\boldsymbol{q}^{\mathbf{j}} = \begin{bmatrix} q_{\text{in}} & q_{\text{C}_1} & \cdots & q_{\text{C}_{\text{N}_\text{C}-1}} & q_{\text{C}_{\text{N}_\text{C}}} & q_{\text{out}} \end{bmatrix} \tag{7.1}$$

where charge into the positive terminal of a source or capacitive element is defined as positive. For a step-down converter, as shown here, q_{in} is equivalent to q_{HI}, and q_{out} is equivalent to q_{LO}.

For the N:1 CaSP converter shown in Fig. 7.2, these charge vectors are

$$\begin{bmatrix} \boldsymbol{q^1} \\ \boldsymbol{q^2} \\ \boldsymbol{q^3} \end{bmatrix} = \begin{bmatrix} -q_0 & q_0 & q_0 & \cdots & q_0 & q_0 \\ 0 & q_0 & q_0 & \cdots & -q_0 & q_0 \\ 0 & -2q_0 & -2q_0 & \cdots & 0 & 2(N_\text{C}-1)q_0 \end{bmatrix} \tag{7.2}$$

The total input and output charges can then be found by summing down the first and last columns of (7.2), as

$$q_{\text{in}} = -q_0 \tag{7.3}$$

$$q_{\text{out}} = 2N_\text{C} \cdot q_0 \tag{7.4}$$

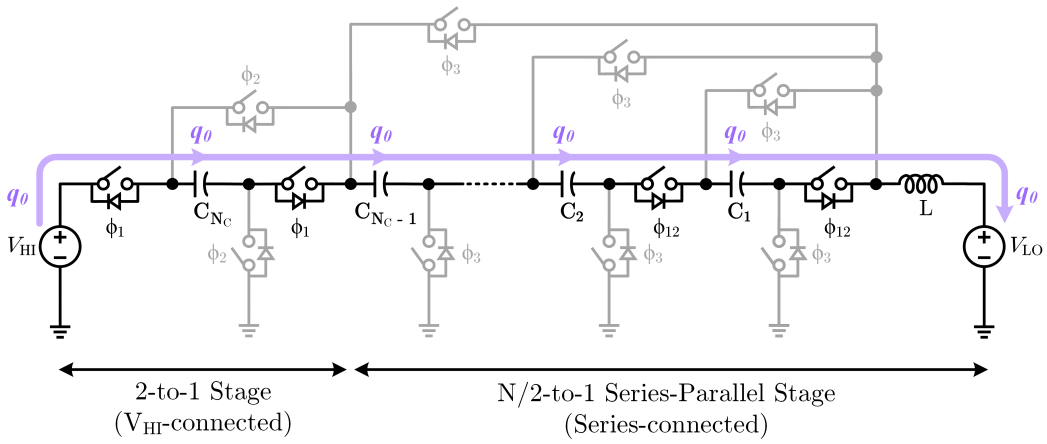
The conversion ratio N of the converter can then be found in terms of N_C by assuming lossless operation, i.e. $P_{\text{in}} = P_{\text{out}}$. The absolute value of (7.3) can be used, as the negative sign only signifies that the direction of power flow is out of the input source.

$$\begin{aligned} \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{in}}}{I_{\text{out}}} = \frac{q_{\text{in}}}{q_{\text{out}}} &= \frac{q_0}{2N_\text{C} \cdot q_0} \\ &= \frac{1}{2N_\text{C}} \end{aligned} \tag{7.5}$$

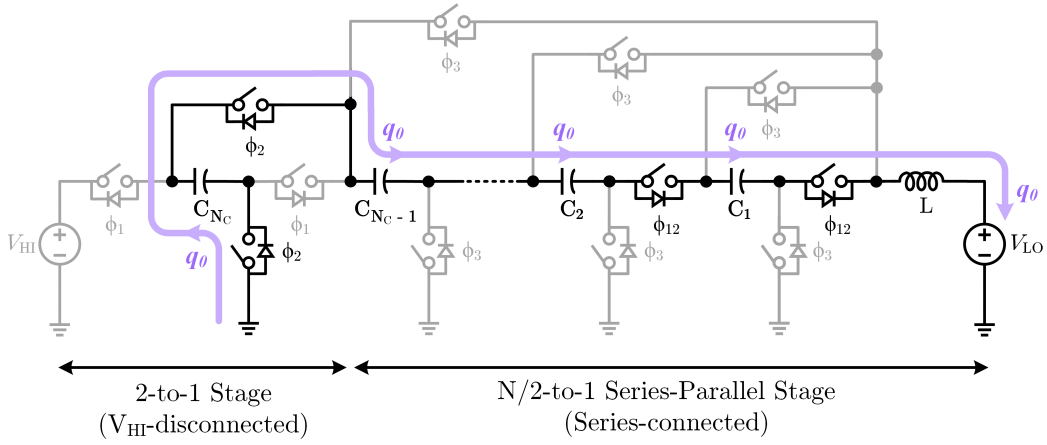
7.2.2 Soft-Charging Capability

The CaSP is similar to the series-parallel converter in operation, and can achieve full soft-charging of all flying capacitors. Similar to the series-parallel, all capacitors that are connected in parallel (over at least one phase) must have the same capacitance. The flying capacitor $C_{\text{N}_\text{C}-1}$, however, is only ever series-connected with the rest of the capacitors and the output inductor, and therefore can be any value in order to achieve soft-charging.

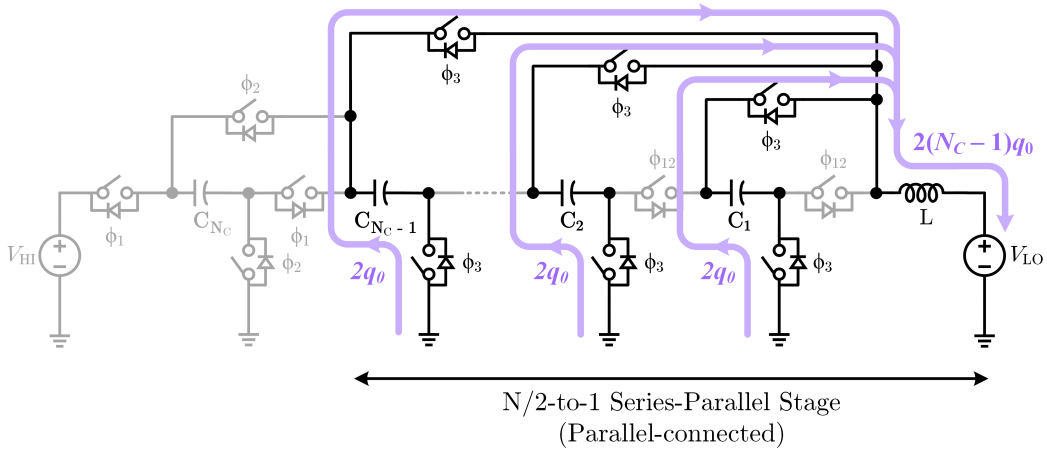
An algorithmic approach using matrix subspaces was developed in [5] to determine whether a given two-phase series-capacitor converter could be converted into a soft-charging hybrid SC converter through the addition of a single inductor at the low-side port. This approach can be extended to multi-resonant converters, such as the CaSP and MRD converters, as shown here.



(a) Phase 1 equivalent circuit.



(b) Phase 2 equivalent circuit.



(c) Phase 3 equivalent circuit.

Figure 7.2: Charge flow shown for the N-level CaSP converter for each operating phase.

The first step in the analysis is to write the defining KVL equations for each phase in the form of a matrix-vector product, given by

$$\mathbf{A_j v^j} = 0 \tag{7.6}$$

Here, $\mathbf{A_j}$ is the reduced loop matrix of the jth phase [26], and $\mathbf{v^j}$ is the voltage vector,

$$\mathbf{v^j} = \begin{bmatrix} v_{\text{in}} \\ v_{\text{C}_1} \\ \vdots \\ v_{\text{N}_\text{C}} \\ v_{\text{out}} \end{bmatrix}. \tag{7.7}$$

KVL analysis requires that at the start of phase j,

$$\mathbf{A_j v^j} = 0. \tag{7.8}$$

At the end of phase j, the voltage vector has increased by the per-phase ripple voltage vector $\mathbf{\Delta v_j}$, so that

$$\mathbf{A_j}(\mathbf{v^j} + \mathbf{\Delta v^j}) = 0. \tag{7.9}$$

Satisfying both this constraints requires that

$$\mathbf{A_j \Delta v^j} = 0. \tag{7.10}$$

Stated in circuit terminology, this means that the source and capacitor ripple voltages must also satisfy the same KVL loops as the dc terms.

An additional KVL constraint can be placed on the converter by recognizing that the input source is modeled as a stiff voltage, and therefore $\Delta v_{\text{in}} = 0$. This can be included in the matrix-vector product by adding another row consisting of $\begin{bmatrix} 1 & 0 & \dots & 0 & 0 \end{bmatrix}$ to the bottom of $\mathbf{A_j}$. This results in the modified loop matrix, $\mathbf{A_{m,j}}$.

Additional constraints based on charge flow can also be applied. In [5], this was straightforward as the analysis was restricted to two-phase converter operation. Periodic steady-state operation requires that each capacitor charges the same amount that it discharges over a single switching period. This can easily be stated in terms of the ripple voltage vector $\mathbf{\Delta v^j}$ for a two-phase converter, where

$$\mathbf{\Delta v^1} = -\mathbf{\Delta v^2} \tag{7.11}$$

Finally, due to the presence of the inductor at the output (or low-side port), this terminal has no strict requirement on ripple voltage. Any "mis-matched" capacitor ripple can appear across the inductor, without disruption to the rest of the circuit. Therefore, $\mathbf{\Delta v_{out}^j}$ is unconstrained for all phases.

Reference [5] then performs matrix null space manipulations to find the possible capacitance combinations across all flying capacitors that will satisfy both these KVL and

charge-flow constraints. However, a significant portion of this setup is based upon the relationship defined in (7.11), which is only applicable for two-phase converters. This makes it non-trivial to extend this methodology to hybrid SC converters with multiple operating phases, where capacitors may charge and discharge over multiple phases. However, we can carry out intuitive hand calculations using this method as a framework, in order to determine a flying capacitance ratio that will ensure soft-charging for the CaSP converter.

Similar to [5], we can construct the voltage vectors and KVL loops for a pure multi-phase SC converter (i.e. ignoring the presence of the inductor). If we can obtain a capacitance vector that satisfies all the above constraints when $\mathbf{\Delta v_{out}^{j}} = 0$, then the pure SC converter can be successfuly hybridized by a single inductor at the output (low-side) terminal. First, we can write the KVL equations in terms of the ripple voltage vector, $\mathbf{\Delta v^{j}}$, for each phase j as follows

$$\text{Phase 1:} \left\{ \Delta v_{\text{in}}^{1} - \Delta v_{\text{C}_{\text{N}_\text{C}}}^{1} - \Delta v_{\text{C}_{\text{N}_\text{C}-1}}^{1} - ... - \Delta v_{\text{C}_1}^{1} - \Delta v_{\text{out}}^{1} = 0 \right. \tag{7.12}$$

$$\text{Phase 2:} \left\{ \Delta v_{\text{C}_{\text{N}_\text{C}}}^{2} - \Delta v_{\text{C}_{\text{N}_\text{C}-1}}^{2} - ... - \Delta v_{\text{C}_1}^{2} - \Delta v_{\text{out}}^{2} = 0 \right. \tag{7.13}$$

$$\text{Phase 3} \begin{cases} \Delta v_{\text{C}_{\text{N}_\text{C}-1}}^{3} - \Delta v_{\text{C}_{\text{N}_\text{C}-2}}^{3} = 0 \\ \vdots \\ \Delta v_{\text{C}_1}^{3} - \Delta v_{\text{out}}^{3} = 0 \end{cases} \tag{7.14}$$

As discussed, there is no requirement on $\mathbf{\Delta v_{out}^{j}}$, and loops with this term place no constraint on the capacitance values. For the CaSP converter, the only restriction results from the KVL loops along parallel capacitors in Phase 3, described by (7.14). Capacitors $C_{\text{N}_\text{C}-1}$ through C_1 are therefore required to have the same voltage ripple.

Next, the required capacitance for these flying capacitors can be found using their respective charge flow vectors, given in Section 7.2.1, by applying

$$\Delta v_{\text{C}_i}^{j} = \frac{q_{\text{C}_i}^{j}}{C_i}, \tag{7.15}$$

where $\Delta v_{\text{C}_i}^{j}$ is the voltage ripple in a given phase j for capacitor i. From (7.2) it can be seen that each capacitor discharges $2q_0$ into the load during Phase 3. Therefore the required capacitance ratios can be solved for by

$$\Delta v_{\text{C}_{\text{N}_\text{C}-1}}^{3} = \Delta v_{\text{C}_{\text{N}_\text{C}-2}}^{3} = ... = \Delta v_{\text{C}_1}^{3} \tag{7.16}$$

$$\frac{q_{C_{\text{N}_\text{C}-1}}^{3}}{C_{\text{N}_\text{C}-1}} = \frac{q_{C_{\text{N}_\text{C}-2}}^{3}}{C_{\text{N}_\text{C}-2}} = ... = \frac{q_{C_1}^{3}}{C_1}$$

$$\frac{-2q_0}{C_{\text{N}_\text{C}-1}} = \frac{-2q_0}{C_{\text{N}_\text{C}-2}} = ... = \frac{-2q_0}{C_1}$$

Solving these equations results in the solution $C_{\mathrm{N_C}-1} = C_{\mathrm{N_C}-2} = ... = C_1 = C_0$, where C_0 is an arbitrary scaling capacitance. However, as there is no KVL loop which places a constraint on the ripple voltage $\mathbf{\Delta v^j_{C_{N_C}}}$, there is no specific capacitance ratio that $C_{\mathrm{N_C}}$ must satisfy to ensure soft-charging, as long as this capacitance results in the converter operating at or above its resonant frequency. The dependence of this resonant frequency on the capacitance values of all the flying capacitors will be explored in the next section. The methodology presented in [83] presents a more intuitive, graphical analysis technique that results in the same capacitor sizing relationships.

While operation slightly below the resonant frequency may still result in soft-charged operation (i.e. without capacitor voltage mismatches at phase transitions), the output impedance of the converter would be increased compared to the case where $f_{\mathrm{sw}} \geq f_{\mathrm{res}}$ due to the presence of increased circulating circuits, and therefore increased loss [5].

7.2.3 Zero-Current Switching Operation

The CaSP converter can be operated at a specific resonant frequency, such that the inductor and capacitor currents are half-wave resonant. When operated in this manner, the inductor current (and therefore switch currents) reach zero at each phase transition, resulting in zero-current switching (ZCS) of the switches. The resonant frequency can be determined by the per-phase resonance of each equivalent LC-network connected to the output (or low-side) port. The different phase time durations must be sized correctly based on these different resonant frequencies in order to operate under ZCS conditions.

Fig. 7.3 shows generalized N-level waveforms for the CaSP converter inductor and flying capacitors. The capacitors are charged and discharged with half-wave currents. The current through the inductor is always positive, as the flying capacitors deliver charge to the load during all phases. Fig. 7.3 also provides simplified equivalent circuit schematics for each phase.

- During Phase 1, the resonant frequency of the LC-network is determined by the effective capacitance of the series combination of $C_{\mathrm{N_C}}$ to C_1, and the low-side inductor, L. The resonant frequency of Phase 1 can then be expressed as

$$f_{\mathrm{res,1}} = \frac{1}{2\pi\sqrt{LC_{\mathrm{eq,1}}}}, \quad \text{where} \tag{7.17}$$

$$C_{\mathrm{eq,1}} = \frac{1}{\frac{1}{C_1} + ... + \frac{1}{C_{\mathrm{N_C}}}} \tag{7.18}$$

- During Phase 2, the high-side source V_{HI} is disconnected from the switch-capacitor network. However, the effective capacitance presented to the low-side inductor remains the same (i.e. $C_{\mathrm{eq,2}} = C_{\mathrm{eq,1}}$), as all flying capacitors are still connected in series. The resonant frequency is therefore the same as Phase 1 (i.e. $f_{\mathrm{res,2}} = f_{\mathrm{res,1}}$), as given by (7.17).

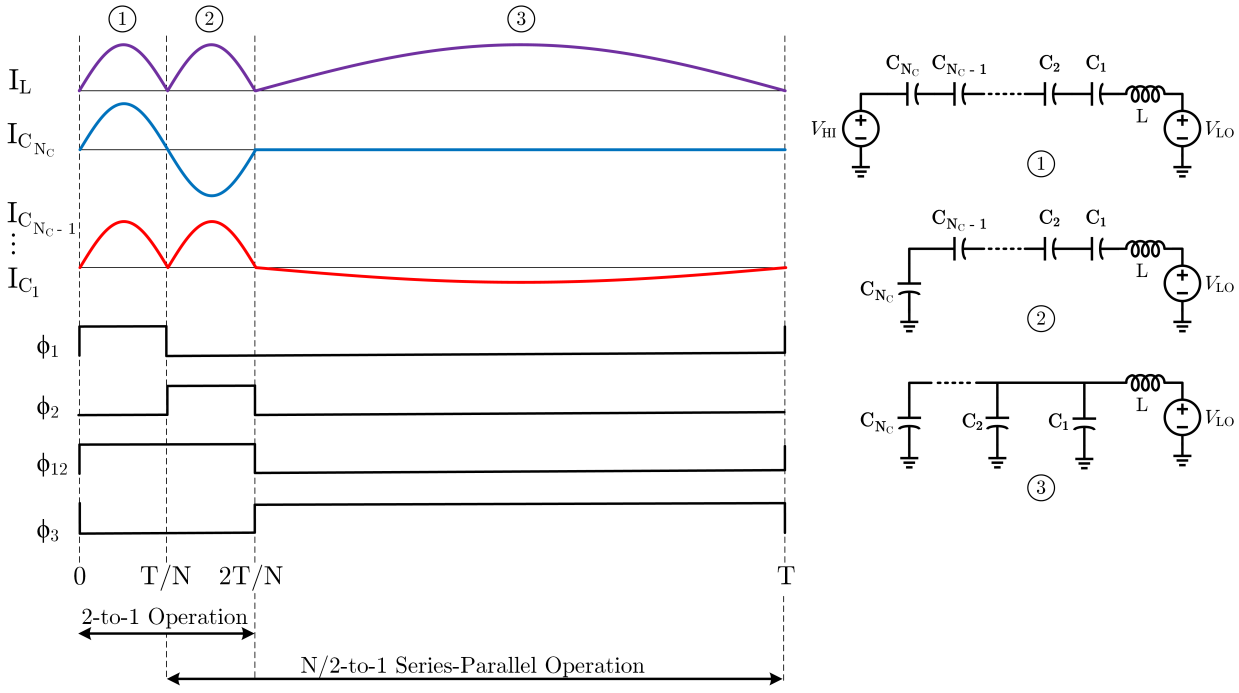


Figure 7.3: Inductor and capacitor current waveforms for an N-level Cascaded Series-Parallel (CaSP) converter.

- During Phase 3, the high-side flying capacitor, $C_{\mathrm{N_C}}$ is disconnected from the LC-newtork. The remaining capacitors, $C_{\mathrm{N_C}-1}$ through C_1 are now connected in parallel. The resonant frequency can then be expressed as

$$f_{\mathrm{res},3} = \frac{1}{2\pi\sqrt{LC_{\mathrm{eq},3}}}, \quad \text{where} \tag{7.19}$$

$$C_{\mathrm{eq},3} = (C_1||C_2||...||C_{\mathrm{N_C}-1}) \tag{7.20}$$

As shown in Fig. 7.3, as the capacitor and inductor waveforms each only transit half a sine-wave curve, each phase duration should be half the natural resonant period of the effective LC network during that respective phase. That is,

$$t_{\phi_1} = t_{\phi_2} = \frac{1}{2f_{\mathrm{res},1}} = \frac{1}{2}\cdot 2\pi\sqrt{LC_{\mathrm{eq},1}} \tag{7.21}$$

$$t_{\phi_3} = \frac{1}{2f_{\mathrm{res},3}} = \frac{1}{2}\cdot 2\pi\sqrt{LC_{\mathrm{eq},3}} \tag{7.22}$$

where t_{ϕ_1}, t_{ϕ_2}, and t_{ϕ_3} are the Phase 1, Phase 2, and Phase 3 time durations, respectively.

As described in Section 7.2.1, full soft-charging conditions require that all parallel-connected capacitors must have the same flying capacitance. This can be expressed by

$C_{N_C-1} = ... = C_1 = C_0$, where C_0 represents some normalizing capacitance. Given this constraint, the per-phase effective capacitances can be expressed as

$$C_{eq,1} = C_{eq,2} = \frac{1}{\frac{1}{C_{N_C}} + \frac{(N_C - 1)}{C_0}} \tag{7.23}$$

$$C_{eq,3} = (N_C - 1)C_0 \tag{7.24}$$

Fig. 7.4 shows current waveforms and the corresponding charge quantity into or out of each capacitor, as well as the resultant current and charge flow into the output inductor. In order for the charge delivered to the load during Phase 3 to be $2(N_C - 1)$ times that in Phase 1 or Phase 2, the phase time durations must satisfy the relationship

$$t_{\phi_1} = t_{\phi_2} = \frac{1}{2(N_C - 1)} t_{\phi_3}. \tag{7.25}$$

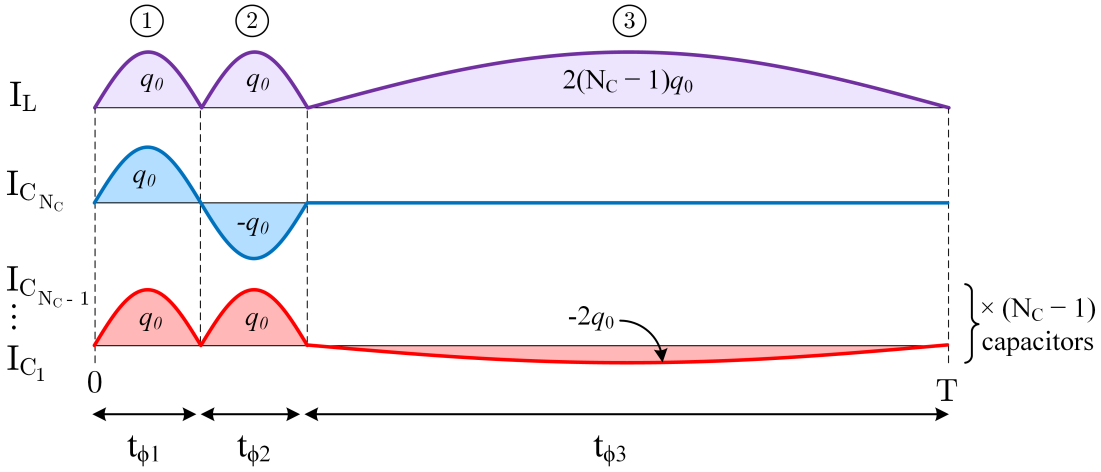


Figure 7.4: Inductor and capacitor current waveforms, along with corresponding charge delivered in each phase.

We can then solve for the required C_{N_C} value to allow the converter to operate resonantly with ZCS-type current waveforms by putting (7.25) in terms of the equivalent capacitances given in (7.23) and (7.24), as follows.

$$\frac{1}{2(N_{\mathrm{C}}-1)} f_{\mathrm{res},1} = f_{\mathrm{res},3} \tag{7.26}$$

$$\frac{1}{2(N_{\mathrm{C}}-1)} \frac{1}{\sqrt{L \cdot \left(\dfrac{1}{\dfrac{1}{C_{\mathrm{N_C}}} + \dfrac{N_{\mathrm{C}}-1}{C_0}} \right)}} = \frac{1}{\sqrt{L(N_{\mathrm{C}}-1)C_0}} \tag{7.27}$$

This can be solved to find the required value of $C_{\mathrm{N_C}}$ for resonant operation.

$$C_{\mathrm{N_C}} = \frac{1}{3(N_{\mathrm{C}}-1)} C_0 \tag{7.28}$$

The $C_{\mathrm{N_C}}$ capacitance value obtained using (7.28) and the relationship $N_{\mathrm{C}} = \frac{N}{2}$ from (7.5) for the 6-to-1 and 8-to-1 implementations of the CaSP converter result in values of $\frac{1}{6}C_0$ and $\frac{1}{9}C_0$, respectively, which match with those given in [18, 19].

Intuitively, $C_{\mathrm{N_C}}$ requires a lower capacitance than the other flying capacitors because it is charged and discharged at a higher frequency. Furthermore, as will be shown in Section 7.2.4, $C_{\mathrm{N_C}}$ sees approximately $\frac{N}{2}V_{\mathrm{out}}$ (neglecting the effect of ripple), while the rest of the flying capacitors only see V_{out}. Therefore, the capacitor with the highest voltage rating also requires the lowest capacitance value, which can allow capacitor $C_{N_{\mathrm{C}}}$ to be realized with a similar volume as exhibited by capacitors $C_{N_{\mathrm{C}}-1}$ to C_1, despite its higher voltage rating.

Above-Resonant Operation

While these capacitor ratios must be exactly met in order to achieve perfect resonant operation and ZCS operation for all switches, the converter's sensitivity to component tolerance can be decreased by operating the converter above resonance. As noted in [12, 84], the output impedance, R_{out}, of the converter is very similar for matched or mismatched conditions *above* resonance, though it does show some deviation around the resonant frequency. Given at or above-resonance operation, the relationships given in (7.28) only set the minimum ratio between $C_{\mathrm{N_C}}$ and the other flying capacitors. Furthermore, the strict capacitance matching requirement on the parallel flying capacitors can also be relaxed when the converter is operated above resonance, as any voltage mismatch between capacitors will be reduced as switching frequency increases. This allows for the use of Class 2 ceramic capacitors despite their dc-bias derating and temperature-varying characteristics. This can help the converter achieve much higher power density due to the increased capacitance density compared to Class 1 ceramic capacitors.

Operating above resonance can also decrease conduction losses in the circuit, as the inductor current sees reduced ripple for a given average output current. However, when

operated above resonance, the inductor current will be in continuous conduction mode, with a half-wave ripple superimposed upon a dc offset. Therefore, the inductor current will never reach zero at phase transitions, and the converter will lose the ability to achieve ZCS. However, the reduced ripple on the inductor also reduces the rms conduction losses across parasitic elements in the capacitors, inductors, and switches (such as capacitor ESR, inductor DCR, and switch $R_{\text{ds,on}}$) [5] [84]. At heavy load, this reduced conduction loss can be more significant than any increased loss due to the lack of ZCS, especially at the lower switching frequencies at which ReSC converters can be operated while still maintaining high efficiency.

7.2.4 Topological Quantities for Passive Volume Calculation

General topological vectors can be derived for the CaSP converter, as described in Chapter 6. These can then be used to calculate the minimized passive volume for the CaSP converter, operated at or above resonance. Table 7.1 summarizes the number of phases and flying capacitors for the CaSP converter for N:1 operation. As the CaSP converter comprises a 2-to-1 staged merged with an $\frac{N}{2}$ series-parallel stage, it is only capable of even-N conversion ratios. The case where $N = 2$ collapses to the standard two-phase doubler topology.

Table 7.1: General Parameters for the N-Level CaSP

Description	Parameter	Expression
Conversion Ratio	N	even $N \in \{\mathbb{N} \geq 4\}$
Number of Phases	N_{P}	3
Number of Flying Capacitors	N_{C}	$\frac{N}{2}$

Capacitor Charge Flow Matrices: $\boldsymbol{a}_{\text{C}}$

The matrix $\boldsymbol{a}_{\mathbf{C}}$ contains elements $a_{\text{C}_{ji}}$ which represent the charge flow through capacitor i in phase j, normalized by the total high-side charge flow, q_{HI}. The charge flow can be found as described in Section 7.2.1. For the N:1 CaSP converter in Fig. 7.2, the total high-side

charge flow can be found to be $q_{\mathrm{HI}} = q_0$. Then, the charge flow matrix can be calculated as

$$\boldsymbol{a}_{\mathrm{C}\,[N_{\mathrm{P}}\times N_{\mathrm{C}}]} = \begin{bmatrix} \frac{q_{\mathrm{C},11}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},12}}{q_{\mathrm{HI}}} & \dots & \frac{q_{\mathrm{C},1\mathrm{N_C}}}{q_{\mathrm{HI}}} \\ \vdots & \ddots & \ddots & \vdots \\ \frac{q_{\mathrm{C},\mathrm{N_P}1}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},\mathrm{N_P}1}}{q_{\mathrm{HI}}} & \dots & \frac{q_{\mathrm{C},\mathrm{N_P}\mathrm{N_C}}}{q_{\mathrm{HI}}} \end{bmatrix} \tag{7.29}$$

$$= \begin{bmatrix} 1 & 1 & \dots & 1 \\ 1 & 1 & \ddots & -1 \\ -2 & -2 & \dots & 0 \end{bmatrix} \tag{7.30}$$

where $\boldsymbol{a}^T_{\mathrm{C}_{N_C-1}} = ... = \boldsymbol{a}^T_{\mathrm{C}_1} \begin{bmatrix} 1 & 1 & -2 \end{bmatrix}$ and $\boldsymbol{a}^T_{\mathrm{C}_{N_C}} = \begin{bmatrix} 1 & -1 & 0 \end{bmatrix}$.

Inductor Charge Flow Matrix: $\boldsymbol{a}_{\mathrm{L}}$

The following analysis reduces the inductor charge flow matrix to dimensions of $N_{\mathrm{P}} \times 1$, as the CaSP converter has only one inductor. As the inductor sees the same charge delivered to the output (or low-side port), its per-phase charge flow is the same as that given for q_{out} in (7.2).

$$\boldsymbol{a}_{\mathrm{L}\,[N_{\mathrm{P}}\times 1]} = \begin{bmatrix} \frac{q_{\mathrm{L},1}}{q_{\mathrm{HI}}} \\ \frac{q_{\mathrm{L},2}}{q_{\mathrm{HI}}} \\ \frac{q_{\mathrm{L},3}}{q_{\mathrm{HI}}} \end{bmatrix} \tag{7.31}$$

$$= \begin{bmatrix} 1 \\ 1 \\ 2(N_{\mathrm{C}}-1) \end{bmatrix} \tag{7.32}$$

Capacitance Vector: $\boldsymbol{c}$

The capacitance vector is given by the relationships found in Section 7.2.3, based on resonant timing. While other values for $C_{\mathrm{N_C}}$ can also result in soft-charging, here we are interested in describing the resonant operation of the converter, and will therefore use the timings and capacitance values defined in Section 7.2.3.

$$\boldsymbol{c}_{\,[1\times N_{\mathrm{C}}]} = \begin{bmatrix} C_1 & C_2 & \dots & C_{\mathrm{N_C}-1} & C_{\mathrm{N_C}} \end{bmatrix} \tag{7.33}$$

$$= \begin{bmatrix} 1 & 1 & \dots & 1 & \frac{1}{3\cdot(N_{\mathrm{C}}-1)} \end{bmatrix} \tag{7.34}$$

Capacitor Mid-Range Voltage Vector: $\boldsymbol{v}$

Each flying capacitor's mid-range voltage is defined as the dc value symmetrically centered btween the maximum and minimum voltage, as dictated by the capacitor voltage ripple. For multi-phase converters such as the CaSP converter, this value can deviate significantly from the time-average dc voltage, as charging and discharging events may occur during only a small portion of the overall switching period.

The absolute mid-range voltages, V_{C_i}, can be defined in terms of the high-side voltage, V_{HI}. However, as discussed in Section 6.2.2, certain topologies–such as the CaSP converter–exhibit capacitors whose mid-range voltage is not only not equal to the time-averaged dc value, but is also dependent on load, and therefore on the capacitor peak-to-peak ripple voltage itself.

The mid-range voltages can be derived from an assumption of zero average voltage across the inductor (i.e., zero volt-seconds) within each phase [32]. Under this assumption, the inductor may be treated as a short circuit when applying average KVL loops to each phase. Subsequently the absolute mid-range voltages of each flying capacitor, V_{C_i}, may be expressed with respect to the high-side voltage, V_{HI}, as

$$V_{\mathrm{C}_i} = V_{\mathrm{HI}}\, v_i, \tag{7.35}$$

where v_i represents the normalized (to V_{HI}) mid-range voltage.

By applying per-phase *average* KVL to the N:1 CaSP converter depicted in Fig. 7.1 and Fig. 7.2, we can derive a set of equations that can be solved for the mid-range voltage. For simplicity, we will derive this set of equations for an 8-to-1 CaSP converter.

$$\text{Phase 1:} \left\{ V_{\mathrm{IN}} - V_{\mathrm{C}_4} - (V_{\mathrm{C}_3} - \frac{\Delta V_{\mathrm{C}_3}}{4}) - (V_{\mathrm{C}_2} - \frac{\Delta V_{\mathrm{C}_2}}{4}) - (V_{\mathrm{C}_1} - \frac{\Delta V_{\mathrm{C}_1}}{4}) - (V_{\mathrm{OUT}}) = 0 \right. \tag{7.36}$$

$$\text{Phase 2:} \left\{ V_{\mathrm{C}_4} - (V_{\mathrm{C}_3} + \frac{\Delta V_{\mathrm{C}_3}}{4}) - (V_{\mathrm{C}_2} + \frac{\Delta V_{\mathrm{C}_2}}{4}) - (V_{\mathrm{C}_1} + \frac{\Delta V_{\mathrm{C}_1}}{4}) - (V_{\mathrm{OUT}}) = 0 \right. \tag{7.37}$$

$$\text{Phase 3} \begin{cases} V_{\mathrm{C}_3} - V_{\mathrm{OUT}} = 0 \\ \vdots \\ V_{\mathrm{C}_1} - V_{\mathrm{OUT}} = 0 \end{cases} \tag{7.38}$$

The inductor voltage term does not appear in these equations, as $\langle V_{\mathrm{L}} \rangle = 0$. The KVL equations written in (7.36) - (7.38) can also be thought of as the KVL loops at a time t when the capacitors have completed half of their respective charge flows per-phase[1]. Therefore,

[1]Due to the half-wave resonant shape of the waveform at and above resonance, this occurs at a time t_{mid} halfway into each phase (i.e. at $\frac{1}{2}t_{\phi,1}$ for Phase 1) for the CaSP converter.

by noting whether a capacitor starts a phase fully discharged or charged, and then adding in half the total charge accumulated during that phase, the capacitor average KVL values can be found. For example, we know capacitor C_4 starts Phase 1 fully discharged through charge flow, at a voltage given by $V_{\mathrm{C}_4,\mathrm{min}} = V_{\mathrm{C}_4} - \frac{1}{2}\Delta V_{\mathrm{C}_4}$. It then fully charges over the course of Phase 1, so halfway through Phase 1 it must be halfway-charged, and at a voltage given by $V_{\mathrm{C}_4,\phi 1,\mathrm{mid}} = V_{\mathrm{C}_4} - \frac{1}{2}\Delta V_{\mathrm{C}_4} + \frac{1}{2}\Delta V_{\mathrm{C}_4} = V_{\mathrm{C}_4}$.

Similarly, we know capacitor C_3 also starts Phase 1 fully discharged. However, it will charge a total of $2q_0$ over Phase 1 and Phase 2, so the charge delivered halfway through Phase 1 represents only $\frac{1}{4}$ of its total charge accumulated. Therefore, we can find $V_{\mathrm{C}_3,\phi 1,\mathrm{mid}} = V_{\mathrm{C}_3,\mathrm{min}} + \frac{1}{4}\Delta V_{\mathrm{C}_3} = (V_{\mathrm{C}_3} - \frac{1}{4}\Delta V_{\mathrm{C}_3})$ as shown in (7.36) - (7.38).

We can then derive the modified mid-range voltage vector, accounting for the ripple dependence of the mid-range voltage of C_4 (or the high-side capacitor), and rearrange it into the form given by

$$v_{\mathrm{m},i} = v_{\mathrm{o},i} + k_i \cdot \frac{1}{2}\Delta v_{\mathrm{pp},i}. \tag{7.39}$$

For a general N:1 CaSP converter, we find that

$$\mathbf{v_o} = \frac{1}{N}\begin{bmatrix}1 & 1 & ... & N_\mathrm{C}\end{bmatrix}, \tag{7.40}$$

$$\mathbf{k} = \begin{bmatrix}0 & ... & 0 & 6\end{bmatrix}^T, \tag{7.41}$$

where $\mathbf{\Delta v_{pp}} = \begin{bmatrix}\Delta v_{\mathrm{pp},1} & \dots & \Delta v_{\mathrm{pp},\mathrm{N_C}}\end{bmatrix}$ and we perform element-wise multiplication between $\mathbf{k}$ and $\mathbf{\Delta v_{pp}}$.

Lumped Equivalent Capacitance Vector: $\boldsymbol{\kappa}$

Using the equations for the required capacitance for resonant operation derived in Section 7.2.3, we can derive the effective capacitance vector, $\boldsymbol{\kappa}$, as described in Chapter 6. This is given by

$$\boldsymbol{\kappa}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \dfrac{1}{4(N_\mathrm{C}-1)} \\ \\ \dfrac{1}{4(N_\mathrm{C}-1)} \\ \\ (N_\mathrm{C}-1) \end{bmatrix}. \tag{7.42}$$

Phase Duration Vector: $\boldsymbol{\tau}$

Similarly, we can derive the phase duration $\boldsymbol{\tau}$ vector for at and above resonant operation. As the converter moves into above-resonant operation, the phase-to-phase charge ratios through each capacitor and into the load must remain the same (i.e. Phase 3 see will always see $2(N_\mathrm{C}-1)\times$ the charge in Phase 1 flowing through the inductor). If we assume that

the inductor current starts and ends each phase with the same value (as described in [32]), then we find the inductor current peaks are all the same as well, and the phase timings will not change above resonance. Note, this is unlike the flying capacitor multilevel converter (FCML), which sees different magnitude current peaks through the inductor in different phases, and exhibits variable phase timing above resonance as shown in [32]. For the CaSP converter, the charge quantity q_0 only ever flows through one equivalent capacitance network; that is, in Phase 1 and Phase 2, q_0 flows into a series-combination of C_1 to $C_{\mathrm{N_C}}$ in both phases. However, in the FCML, the same charge quantity q_0 flows through a network with an effective capacitance C_0 in Phase 1, and through a network with an effective capacitance $\frac{1}{2}C_0$ in Phase 2. This results in different peak current magnitudes between Phase 1 and Phase 2, resulting in different phase timing once the converter starts operating farther into continuous conduction mode (CCM) at frequencies higher than the resonant frequency.

$$\boldsymbol{\tau}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \dfrac{1}{2N_\mathrm{C}} \\ \dfrac{1}{2N_\mathrm{C}} \\ \dfrac{N_\mathrm{C}-1}{N_\mathrm{C}} \end{bmatrix} \tag{7.43}$$

The passive volume can then be calculated following the methodology in Chapter 6. A plot comparing the overall passive volume of the CaSP converter, odd-level Dickson, Fibonacci, and series-parallel converters is presented in Chapter 6, as well. The CaSP converter exhibits very similar passive volume as the series-parallel (which can obtain the theoretical minimum [42]), but can achieve the same conversion ratio with significantly fewer capacitors and switches, as will be described in the next section.

7.2.5 Comparison with Other Topologies

The CaSP converter can be compared to several other standard hybrid SC topologies using common performance metrics, as will be demonstrated for both the 6-to-1 and 8-to-1 implementations.

6-to-1 ReSC Comparison

Table 7.2 compares the component count and voltage ratings for several different switched-capacitor topologies that can be augmented with resonant inductor(s) and operated in a resonant mode. The CaSP converter has the lowest number of components of all the 6-to-1 converters in Table 7.2, and the same number of components as the lower conversion-ratio 5-to-1 Fibonacci converter. This is of note as the 5-to-1 Fibonacci converter demonstrates the maximum gain possible in a two-phase switched-capacitor converter, with 10 switches

Table 7.2: Comparison of the number and voltage rating of components for 6-to-1 and 5-to-1 resonant switched-capacitor converters.

Topology	Conversion Ratio	Number of Switches	Switch Rating	Number of C_{fly}	C_{fly} Rating	Number of Inductors
Proposed Topology	6-to-1	10	$4\times3V_o$ $2\times2V_o$ $4\times V_o$	3	$1\times3V_o$ $2\times V_o$	1
Series-Parallel	6-to-1	16	$3\times5V_o$ $2\times4V_o$ $2\times3V_o$ $2\times2V_o$ $7\times V_o$	5	$5\times V_o$	1
Switched Tank (Dickson)	6-to-1	16	$2\times2V_o$ $14\times V_o$	5	$1\times5V_o$ $1\times4V_o$ $1\times3V_o$ $1\times2V_o$ $1\times V_o$	3
FCML	6-to-1	12	$12\times V_o$	5	$1\times\ 5V_o$ $1\times\ 4V_o$ $1\times\ 3V_o$ $1\times\ 2V_o$ $1\times\ 1V_o$	1
Fibonacci	5-to-1	10	$2\times3V_o$ $4\times2V_o$ $4\times V_o$	3	$1\times3V_o$ $1\times2V_o$ $1\times V_o$	1

and 3 flying capacitors [85, 86]. The CaSP converter also requires lower voltage capacitors compared to the FCML and Switched Tank (Dickson-derived) converters.

Using the methodology provided in [42], the total passive volume and switch stress of the converter can be found, and then compared with other hybrid SC converters as shown in Fig. 7.5. The switch stress relates to how much voltage the switches must block and how much current they must conduct, and is a good indication of the efficiency of the topology. The passive component volume is proportional to the amount of reactive energy that needs to be processed and stored in the converter, and reflects the power density of the topology. Dissimilar to the analysis method presented in [32] and summarized in Chapter 6, the passive component volume shown in Fig. 7.5 does not take into account the effect of the ripple-dependent mid-range voltages of the flying capacitors in the CaSP converter. In addition, the switch-stress presented here does not take into account the peak switch voltage, but rather uses the dc voltage. However, these results can still be used as good first-order approximations of the passive volume and switch stress. Reference [81] also uses

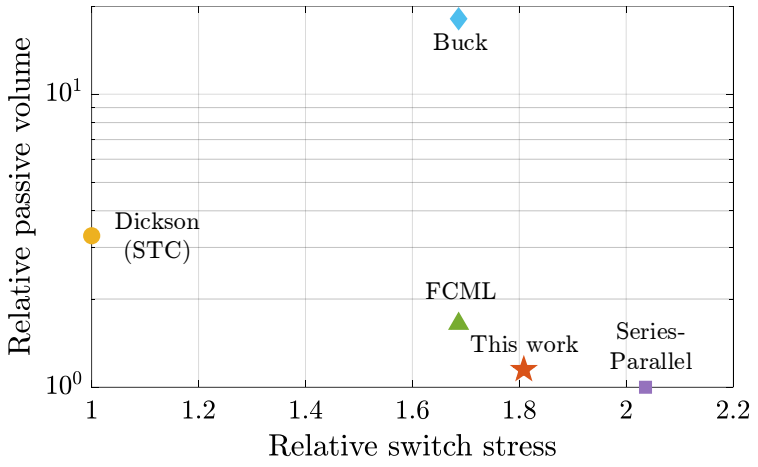


Figure 7.5: Relative passive volume vs. normalized switch stress for several 6-to-1 converters, using the method proposed in [42].

this methodology to calculate the passive volume and switch stress over all N.

The results shown in Fig. 7.5 are generated assuming $\frac{\rho_C}{\rho_L} = 100$, where ρ_C is the energy density of the capacitor(s) and ρ_L is the energy density of the inductor(s). The switch stress and passive volume are normalized to the theoretical lowest possible value (achievable by the base 2-to-1 converter) to allow for a comparison across topologies. In this plot, the ideal converter would be situated near the origin, and exhibit both low passive volume and low switch stress. The buck converter operating at a conversion ratio of 6-to-1 is also plotted to provide a benchmark for comparison with the presented hybrid converters.

Looking at Table 7.2 and Fig. 7.5, it can be seen that the 6-to-1 CaSP converter has much lower passive volume and therefore potentially higher power density compared to the Switched Tank (Dickson-derived) converter, though it has higher switch stress. The CaSP converter has lower switch stress compared to the series-parallel topology, while its passive volume is only slightly higher. This is of note as the passive volume of the series-parallel topology is known to be at the theoretical lower limit [42]. This means that the CaSP converter can achieve similar theoretical performance to the series-parallel converter even with a greatly reduced number of capacitors and switches (and their associated gate drive circuitry). Furthermore, as devices might not be able to be sized exactly to the theoretical VA rating due to limited availability of different voltage ratings, in a physical implementation topologies with different theoretical VA ratings may end up using the same device. This practical concern is most apparent in low-voltage Silicon power transistors, where discrete transistor products below 25 V were not readily available at the time of testing, and are even now limited to 15 V or higher. In applications such as 48 V conversion, the series-parallel converter is very attractive despite its high theoretical switch stress, due to both the limited available switch voltage ratings in this application space as well as the low output impedance

exhibited by the converter due to its many parallel current paths [24]. The CaSP converter operates in a similar manner to the series-parallel topology, and has the potential to exhibit very high performance in this application space compared to Dickson-based topologies due to its low passive volume and low number of components, as the disadvantage of switch utilization is relatively mild considering the actual switches available.

8-to-1 ReSC Comparison

Table 7.3: Comparison of number and voltage rating of components for 8-to-1 resonant switched-capacitor converters

Topology	Number of Switches	Switch Rating	Number C_{fly}	C_{fly} Rating	Number of Inductors	R_{out}
CaSP	13	$4 \times 4V_o$ $2 \times 3V_o$ $2 \times 2V_o$ $5 \times V_o$	4	$1 \times 4V_o$ $3 \times V_o$	1	1.75
MRD [73]	10	$4 \times 4V_o$ $3 \times 2V_o$ $3 \times V_o$	3	$1 \times 4V_o$ $1 \times 2V_o$ $1 \times V_o$	1	2.75
Series-Parallel	22	$3 \times 7V_o$ $2 \times 6V_o$ $2 \times 5V_o$ $2 \times 4V_o$, $2 \times 3V_o$ $2 \times 2V_o$ $9 \times V_o$	7	$7 \times 7V_o$	1	1.25
Switched-Tank (Dickson) [60]	22	$6 \times 2V_o$ $16 \times V_o$	7	$1 \times 7V_o$ $1 \times 6V_o$ $1 \times 5V_o$ $1 \times 4V_o$ $1 \times 3V_o$ $1 \times 2V_o$ $1 \times V_o$	4	0.8
Fibonacci	13	$2 \times 5V_o$ $4 \times 3V_o$ $3 \times 2V_o$ $4 \times V_o$	4	$1 \times 4V_o$ $1 \times 3V_o$ $1 \times 2V_o$ $1 \times V_o$	1	2.165

The 8-to-1 CaSP converter can be compared to several other 8-to-1 hybrid SC topologies, in a similar manner as was done for the 6-to-1 CaSP converter. Table 7.3 compares the

component count and output impedance for several different resonant 8-to-1 SC topologies. For simplicity, the same on-resistance is assumed for all switches, but this can be adjusted based on available switch technology for the required operating voltages. The component count (and number of required gate drivers) can greatly affect the power density and volume that a converter can achieve. The output impedance of the converter directly relates to the efficiency of the converter, and incorporates both conduction loss and the capacitor charging/discharing loss. For soft-charged SC converters, the capacitor charging/discharging loss is no longer present and the output impedance will depend on the conduction losses due to the resistance of the switches, as well as the ESR of the capacitors and the PCB trace resistance [5].

While the CaSP converter has three more switches and one more capacitor than the topology presented in [73], it has a much lower output impedance. This is due to the fact that the converter operates in the parallel mode for a greater proportion of the switching cycle, and has three parallel conduction paths compared to only one in [73].

The 8-to-1 Fibonacci converter uses the minimum possible number of switches and capacitors to achieve this conversion ratio in a two-phase SC converter. Although the 8-to-1 CaSP converter has the same number of components as the Fibonacci, its multi-phase operation allows it to achieve a lower output impedance. The CaSP converter also only requires about half the number of switches and capacitors as the series-parallel and switched-tank (Dickson) converter [60]. However, the CaSP converter's output impedance is only slightly higher than that of the series-parallel topology. While the switched-tank topology's output impedance is slightly less than half of that of the CaSP converter, it requires higher voltage-rated capacitors, which can negatively impact power density.

In summary, the CaSP converter has been shown to achieve a good balance between output impedance (and therefore efficiency) and number of components (and therefore power density).

7.3 Hardware Prototypes

Various hardware prototypes were constructed, to both validate the CaSP operating principle and achieve high overall performance. These converters were designed for fixed-ratio intermediate bus converters applications for the 48 V bus in data centers. For this application space, high efficiency and high power density are of great importance in order to ensure 1) low losses—and therefore heat dissipation—thereby additionally reducing the amount of energy and volume spent on cooling solutions; and 2) a small physical footprint that allows for either more dense packing of server point-of-load power supplies on each motherboard, or leaves additional empty volume for passive cooling.

As the exact intermediate bus voltage can depend on the specific application requirements, two prototypes of different conversion ratios were built, both designed for a 48 V input. A 6-to-1 CaSP converter designed for a nominal output voltage of 8 V and an output current of 40 A was designed and tested. The prototype achieved 99.0% peak efficiency

(98.5% with gate drive loss) and 2230 W/in^3 power density, both of which were among the highest of existing work [18].

Next, an 8-to-1 CaSP converter designed for a nominal output voltage of 6 V and an output current of 70 A was designed and tested. Several additional layout and component selection improvements were made between the development of the 6-to-1 and 8-to-1 hardware prototypes in order to obtain a higher output current capability, even at a higher conversion ratio. This prototype achieved 98.6% peak efficiency (98.1% with gate drive loss), 95.3% full-load efficiency (95.2% with gate drive loss), and 2140 W/in^3 power density [19].

These hardware prototypes are operated slightly above resonance to account for component non-idealities and reduce the converter output impedance and conduction loss. This also allows for the use of Class 2 ceramic capacitors, greatly increasing the power density of the hardware prototypes.

7.3.1 6-to-1 CaSP Prototype

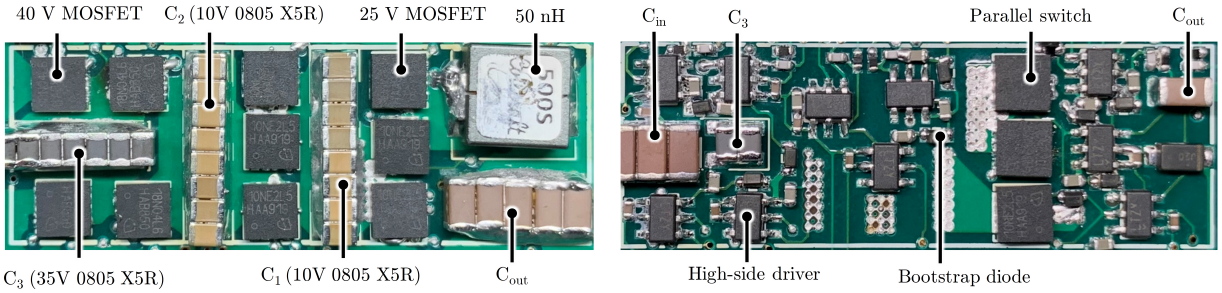


Figure 7.6: Photograph of the 6-to-1 prototype converter. Dimensions: 1.38 × 0.46 × 0.22 inch (3.5 × 1.17 × 0.56 cm).

Fig. 7.6 shows an annotated photograph of the hardware prototype, with key components labeled. The PCB stack-up consists of 4 layers, with 4 oz copper on the outer layers (the location of the critical conduction path) and 3 oz copper on the inner layers. As the maximum theoretical voltage a switch can see in this topology is $3V_o$, relatively low-voltage switches can be used (40 V and 25 V). Silicon devices are used for this prototype, as at these low voltages the performance of Si can match that of GaN. The high-current path devices ($Q_8 - Q_{10}$) are paralleled to reduce conduction losses. Each floating switch is driven by a floating high-side gate driver powered using the cascaded bootstrap method [87], from a 9 V source. The total gate drive current was measured with a Yokogawa WT310 digital power meter, while the power stage voltage, current, and efficiency was measured with a Yokogawa WT3000E precision power meter for the most accurate results at the high efficiencies obtained. Table 7.8 lists the key power-stage components used.

Table 7.4: Main Power Stage Component Listing for 6-to-1 Prototype converter

Component	Description	Device	Value
Q1-Q4	40 V Si switches	Infineon BSZ018N04LS6	40 V, 40 A, 1.8 mΩ
Q5-Q10	25 V Si switches	Infineon BSZ010NE2LS5	25 V, 40 A, 1.0 mΩ
L	Resonant inductor	Coilcraft SLC7530S-500MLB	50 nH, 50 A I_{sat}, 0.123 mΩ
C1	Flying Capacitors	Murata GRM21BR61A476ME15L	16 × 47 μF* 10 V X5R 0805
C2	Flying Capacitors	Murata GRM21BR61A476ME15L	16 × 47 μF* 10 V X5R 0805
C3	Flying Capacitors	TDK C2012X5R1V226M125AC	16 × 22 μF* 35 V X5R 0805
	Gate driver	Analog Devices LTC4440-5	80 V, 1.1 A peak output current
	Bootstrap diode	ON Seminconductor NSR0340V2T1G	40V, 250 mA, Schottky
	Controller	TI TMS320F28069	

*The capacitance listed here is the nominal value before dc derating.

Table 7.5: Converter Operating Conditions

Parameter	Nominal	Range
Input Voltage	48 V	40 - 54 V
Output Voltage	8 V	6.7 - 9 V
Output Current	40 A	
Measured P_{out}	310 W	260 - 350 W
Switching Frequency	68 kHz	65 - 75 kHz
Dimensions	1.38 inch × 0.46 inch × 0.22 inch (3.5 cm × 1.17 cm × 0.56 cm)	
Box Volume	0.139 in^3 (2.29 cm^3)	

Table 7.5 lists the operating conditions for the prototype. The gate drive signals were programmed with a constant deadtime of 44 ns. The converter was tested up to 40 A output current, and achieved a peak efficiency of 99.0% and a full-load efficiency of 97.1% (98.5% and 97.0% with gate drive loss included, respectively) for a 48-to-8 V step-down conversion operating at 68 kHz, slightly above resonance. The power density at full-load was 2230 Win^3 with a box volume of 0.139 in^3 (2.29 cm^3). Efficiency curves for 48-to-8 V operation from 0 A to 40 A are given in Fig. 7.7. Efficiency curves were also taken for additional voltage levels within the expected range of a 48 V nominal intermediate bus for datacenter applications. Efficiency sweeps for 40-to-6.7 V and 54-to-9 V operation are shown in Fig. 7.9 and Fig. 7.10. The switching frequency was increased slightly at higher input voltages, to account for the greater capacitance derating with increased DC-bias. This was done to ensure that the converter continued to operate above resonance. Table 7.6 lists the efficiency and power density of the converter for all tested input voltage and frequency conditions.

The high efficiency achieved by the converter decreases the impact of load regulation, as

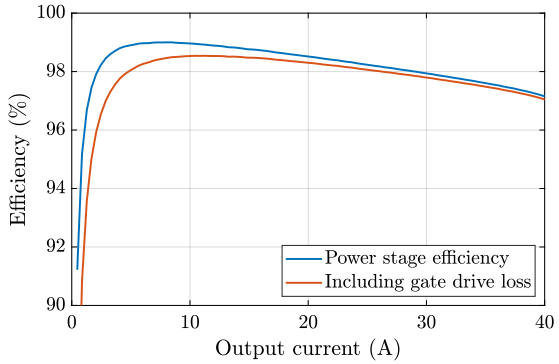


Figure 7.7: Measured efficiency 54 to 9 V, f_{sw} = 75 kHz.

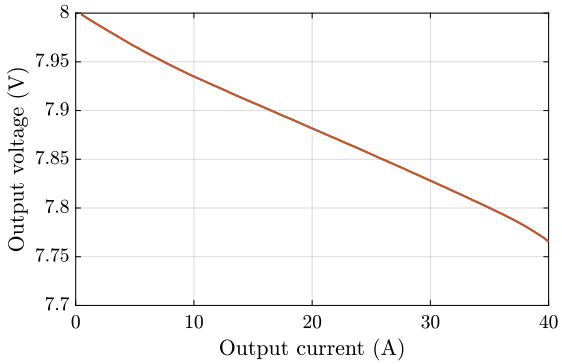


Figure 7.8: Load regulation curve 48 to 6 V, f_{sw} = 68 kHz.

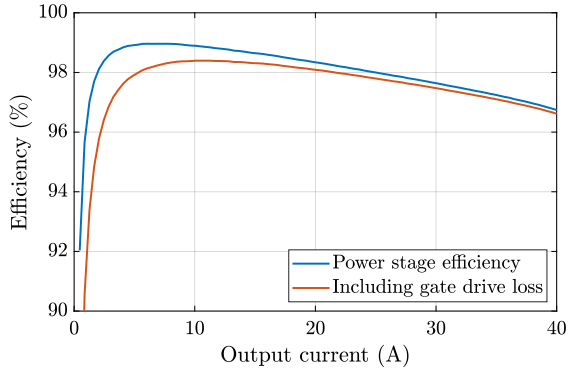


Figure 7.9: Measured efficiency 40 to 6.7 V, f_{sw} = 65 kHz.

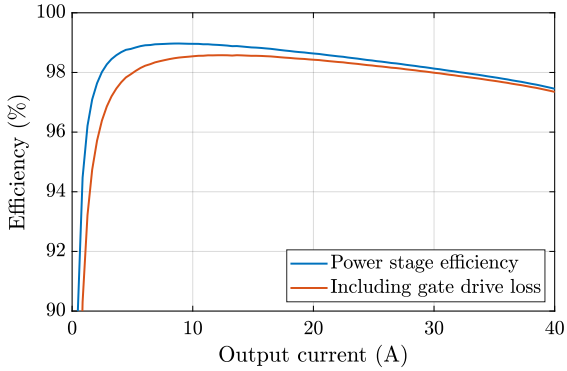


Figure 7.10: Measured efficiency 54 to 9 V, f_{sw} = 75 kHz.

Table 7.6: Measured Converter Performance

Metric	$\boldsymbol{V_{in}}$ **= 40 V** $\boldsymbol{f_{sw}}$ **= 65 kHz**	$\boldsymbol{V_{in}}$ **= 48 V** $\boldsymbol{f_{sw}}$ **= 68 kHz**	$\boldsymbol{V_{in}}$ **= 54 V** $\boldsymbol{f_{sw}}$ **= 75 kHz**
Peak Efficiency	99.0% (98.4% with gate loss)	99.0% (98.5% with gate loss)	99.0% (98.5% with gate loss)
Full-Load Efficiency	96.7% (96.6% with gate loss)	97.1% (97.0% with gate loss)	97.4% (97.3% with gate loss)
Power Density	1840 W/in^3	2230 W/in^3	2510 W/in^3

even though the converter operates in an open-loop fixed-ratio mode, it exhibits an output droop of only 234 mV (2.9% of V_{out}) at full-load as shown in Fig. 7.8.

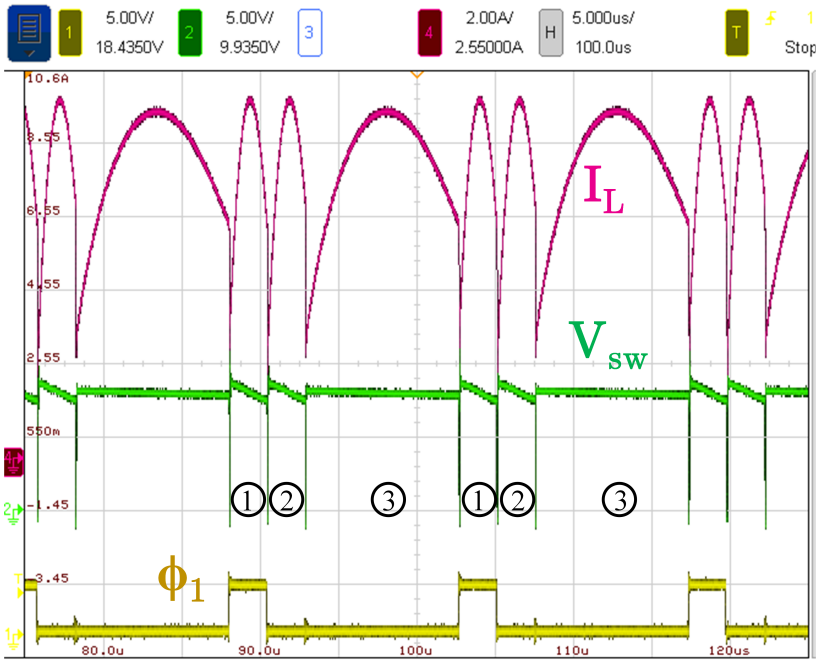


Figure 7.11: Inductor current, switch node voltage, and Phase 1 (ϕ_1) gate signal waveforms for 48-to-8 V.

Fig. 7.11 shows inductor current, I_L, switch node voltage, V_{sw}, and the Phase 1 gate drive signal for a 48 V input voltage. The three operating phases are labeled over two switching periods. As mentioned previously, the converter is operated above resonance to account for component tolerances and reduce conduction loss, as can be seen by the non-zero current at phase transitions.

Fig. 7.12 shows a thermal image of the converter operating at full-load at 48 V input. Even at 40 A output, the converter temperature did not exceed 59C due to the low loss of the converter over its entire operating range. A bench-top fan was used to supply air cooling over the PCB.

Fig. 7.13a and Fig. 7.13b show the transient response of the converter for a step-up and step-down current load-step. Fig. 7.13a shows a transient from 10 A to 40 A at 48 V input. The inductor current stabilizes after approximately 200 μs after the initial ramp up in load current, while the voltage undershoot lasts less than 100 μs and then reaches its new steady state after approximately 160 μs.

Fig. 7.13b shows a transient from 40 A to 10 A at 48 V input. The inductor current stabilizes after approximately 120 μs after the initial ramp down in load current, while the voltage overshoot lasts less than 100 μs and then reaches its new steady state after approximately 200 μs.

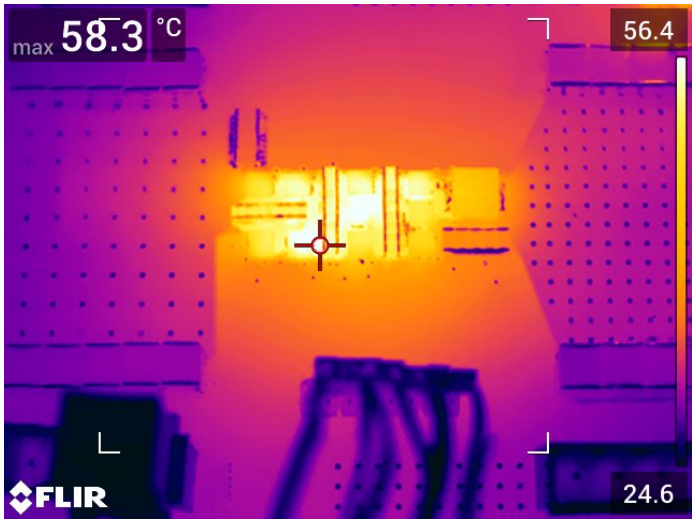
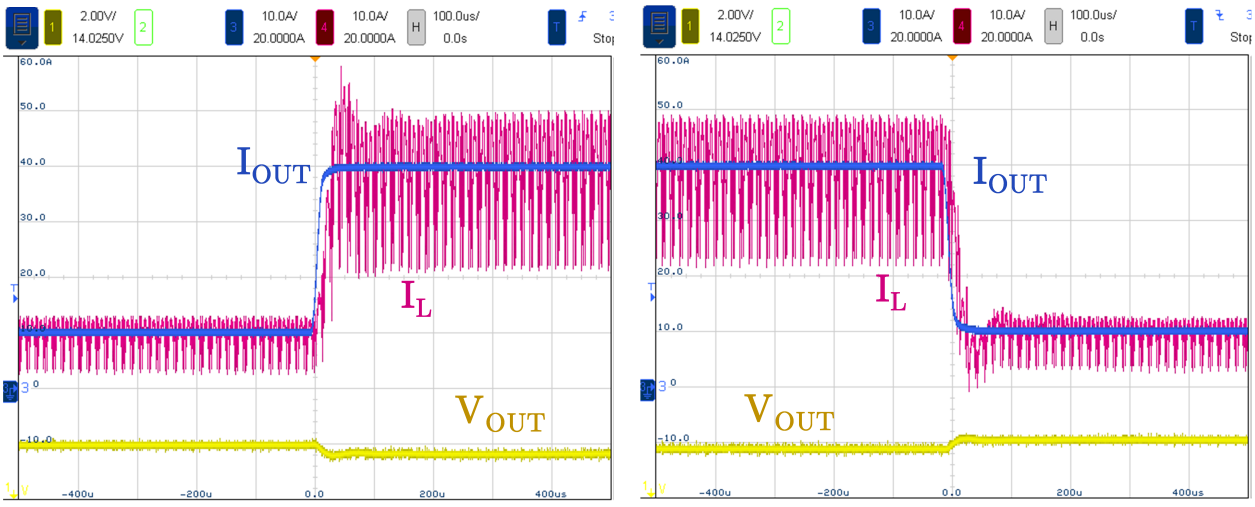


Figure 7.12: Thermal image at full-load (40 A) for 48-to-8 V operation with fan cooling.



(a) Load-step up from 10 A to 40 A.

(b) Load-step down from 40 A to 10 A.

Figure 7.13: Load transient response of the converter for a (a) step-up and (b) step-down transition at 48 V to 8 V operation.

Comparison with Contemporaneous Work

Table 7.7: Comparison of this work and existing high step-down ratio bus converters

Reference	Topology	Voltage conversion	Output current (A)	Power density (W/in^3)	Full-load efficiency (%)	Peak efficiency (%)	Notes
This Work	**CaSP**	**48-to-8 V**	**40**	**2230**	**97.0%**	**98.5%**	**fixed-ratio, Si MOSFET**
		54-to-9 V	**40**	**2510**	**97.3%**	**98.5%**	
Switched Tank [13]	Resonant Dickson	54-to-9 V	50	750	97.18%*	98.55%*	fixed-ratio, GaN FET
Vicor VTM Current Multiplier [88]	Sine Amplitude	48-to-8 V	30	∼900	95.7%	95.8%	fixed-ratio
		55-to-9.2 V	30		95.8%	95.9%	
EPC9205 [89]	Buck	48-to-8 V	14	1300	93.2%	94.7%	GaN FET
Google Switched Tank (4-to-1) [60]	Resonant Dickson	54-to-13.5 V	50	500	97.41%	98.61%	4-to-1, fixed-ratio, Si MOSFET

*Not explicitly stated if efficiency number includes gate drive loss

Table 7.7 compares this work with some of the best existing works. The efficiencies given include gate drive loss unless otherwise noted. The converter was tested at both 48-to-8 V and 54-to-9 V operating conditions to allow for a more equal comparison with prior work. The proposed topology has the highest power density of all the listed converters, and at 54-to-9 V operation the power density is almost 2× higher than the next most power dense converter (the EPC2905 buck [89]). The proposed topology's peak and full-load efficiencies are also higher than the EPC9205 buck converter, highlighting the potential efficiency advantages of the ReSC approach compared to more conventional approaches. The proposed topology also achieves a higher full-load efficiency compared to the Vicor VTM Current Multiplier [88], even at at higher full-load current. The power density and peak efficiency of the proposed converter are also higher as well, although the Vicor is a highly integrated product that may have more auxiliary circuitry compared to a prototype converter.

The proposed topology also has considerably higher power density and similar efficiencies compared to the 6-to-1 switched tank converter in [13]; however, [13] does not explicitly state whether their efficiencies include gate drive losses, which are often excluded in reported efficiencies for ReSC converters. Compared to the Google Switched Tank 4-to-1 converter [60], the proposed topology achieves roughly the same full and peak efficiencies for a larger conversion ratio (6-to-1 compared to 4-to-1).

7.3.2 8-to-1 CaSP Prototype

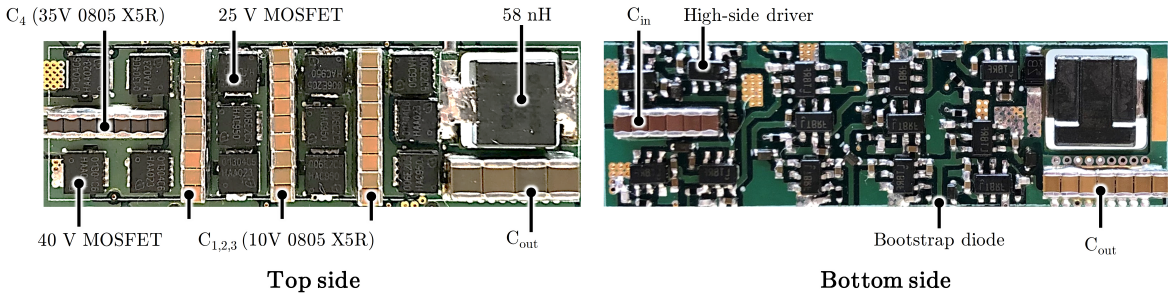


Figure 7.14: Photograph of the converter. Dimensions: 1.76 × 0.51 × 0.21 inch (4.47 × 1.30 × 0.53 cm).

Fig. 7.14 shows an annotated photograph of the hardware prototype. The PCB stack-up consists of 6 layers, with 4 oz copper on the output layers (where the primary current conduction paths are located) and 2 oz copper on the inner layers. As the inductor is the tallest component, a hole was routed in the PCB to recess the inductor in order to achieve a more uniform height, and thereby improve the power density as calculated by box volume.

The power-stage and gate drive components are listed in Table 7.8. 40 V and 25 V Si devices are used since eGaN FETs do not generally outperform silicon MOSFETs significantly at these low voltages, as they have similar on-resistance and footprints and only slightly lower input-output capacitance [84]. Lower on-resistance devices compared to those used in [73] were used, further improving high-load efficiency. Although these devices have slightly higher output capacitance, the operating frequency of the converter is relatively low (50 kHz), so switching losses are not a dominating factor over the converter operating range.

Although Q_5 and Q_7 have an ideal voltage rating of $3V_o$ (or 18 V for $V_{\text{out}} = 6$ V), 40 V devices were used in the physical implementation. This was done to take advantage of the ability to operate soft-charged SC converters with high capacitor ripple without sacrificing efficiency, as the switches see the capacitor voltage ripple on top of their theoretical blocking voltage. Increasing the voltage rating of the devices increases the energy utilization of the capacitors and allows for lower capacitance to be used, increasing power density. Additionally, this allows for more headroom on the devices when operating at the high end of the input voltage (e.g. at 60 V the devices must block 22.5 V). Each floating switch is driven by a floating high-side gate driver powered by the cascaded bootstrap method [90] [87], derived from a single ground-referenced 9 V supply.

Table 7.9 lists the main operating parameters of the converter. The minimum switching frequency is determined by the value of the flying capacitors and the inductor. However, as discussed previously, the prototype is operated at a frequency slightly higher than resonance to counteract the effects of component tolerance variations, as well as to to reduce the RMS current of the switches, capacitors, and inductor. Although this results in the loss of ZCS, the converter is conduction loss limited at heavy load, so ZCS is not essential for obtaining

Table 7.8: Main Power Stage Component Listing for 8-to-1 Prototype converter

Component	Description	Device	Parameters
Q_1-Q_4, Q_5, Q_7	40 V Si switches	Infineon IQE013N04LM6CG	40 V, 1.35 mΩ
Q_6, Q_8-Q_{13}	25 V Si switches	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
L	Resonant inductor	Pulse FP0805R1-R06-R	58 nH, 83 A I_{sat}, 0.17 mΩ
C_1	Flying Capacitor	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
C_2	Flying Capacitor	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
C_3	Flying Capacitor	Murata GRM21BR61A476ME15L	18 × 47 μF* ±20% 10 V X5R 0805
C_4	Flying Capacitor	TDK C2012X5R1V226M125AC	14 × 22 μF* ±20% 35 V X5R 0805
C_{in}	Input Capacitor	TDK C2012X7S2A105M125AB	6 × 1 μF* ±20% 100 V X7S 0805
C_{out}	Output Capacitor	Murata GRM21BR61A476ME15L	7 × 47 μF* ±20% 10 V X5R 0805
	Kemet C1210C107M4PAC7800	4 × 100 μF* ±20% 16 V X5R 1210	
	Gate driver	Analog Devices LTC4440-5	80 V, high-side
	Bootstrap diode	ON Seminconductor NSR0340V2T1G	40V, 250 mA, Schottky
	Controller	TI TMDSDOCK28379D Experimenter Kit	

*The capacitance listed here is the nominal value before dc derating

high efficiency. For the capacitor values used in the prototype, $f_{\text{res}} = f_{\text{sw,min}} = 40$ kHz. The actual operating frequency for the converter at 48-to-6 V conversion was selected as 50 kHz, as it resulted in the the best efficiency performance while still operating sufficiently above f_{res}.

Measured operating waveforms of the inductor current and switch node voltage are shown in Fig. 7.15. The operating phases are labeled. As can be seen, the inductor current does not reach zero before the next operating phase begins, illustrating the reduced ripple current resulting from operating slightly above resonance.

During Phase 1 and 2 the switch-node voltage slopes downwards due to the increasing voltage across the series-connected flying capacitors as they are being charged. The negative spikes in V_{sw} at the switching transitions are due to body diode conduction in Q_{12} and Q_{13}.

The converter efficiency was measured up to 70 A for 40 - 60 V input, the expected range of a 48 V nominal bus for data center applications. The power stage voltage, current,

Table 7.9: Converter Operating Conditions

Parameter	Nominal	Range
Input Voltage	48 V	40 - 60 V
Output Voltage	6 V	5 - 7.5 V
Output Current	70 A	
Measured P_{out}	400 W	330 - 500 W
Switching Frequency	50 kHz	50 - 55 kHz

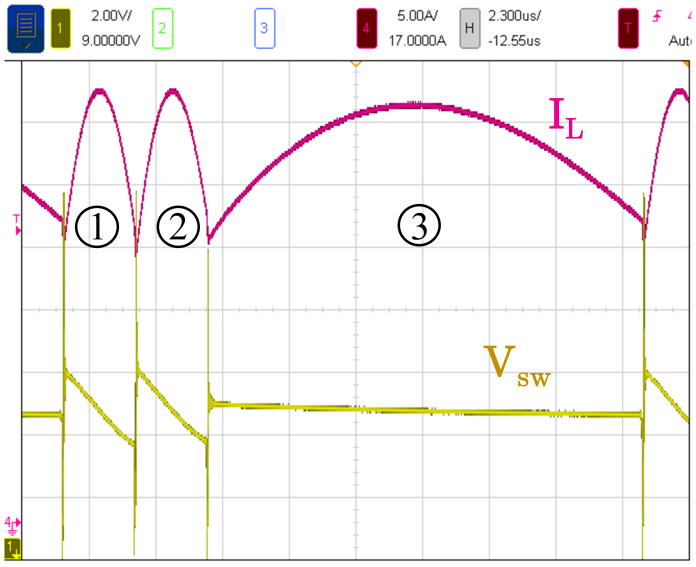


Figure 7.15: Inductor current and switch node voltage for 48-to-6 V operation at 30 A.

and efficiency were measured with a Yokogawa WT3000E precision power meter to ensure accurate results at the high efficiencies obtained.

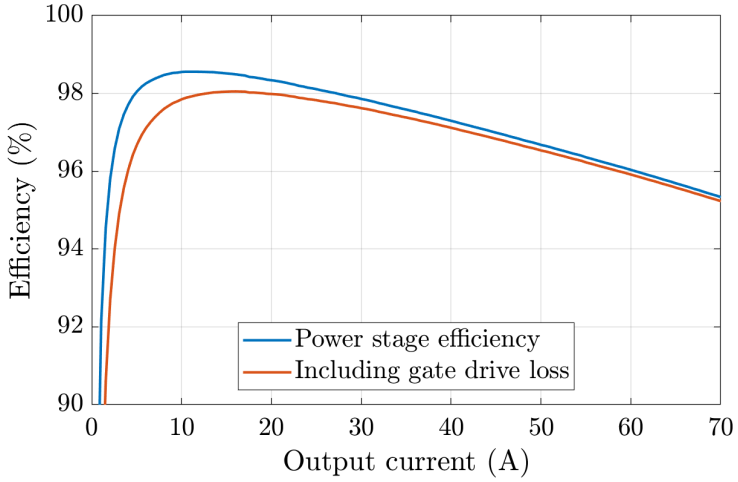


Figure 7.16: Measured efficiency at 48 to 6 V, f_{sw} =50 kHz.

At 48-to-6 V operation, the converter reached a maximum output power of 400 W, resulting in a power density of 2140 W/in^3 as calculated by the box volume of the converter power stage and gate drive circuitry. Fig. 7.16 shows the efficiency curves for this operating point with and without gate drive losses. The converter achieved a peak efficiency of 98.6%

(98.1% with gate drive loss included) and a full-load efficiency of 95.3% (95.2% with gate drive loss included).

The system efficiency curves (including the gate drive loss) are also given for $V_{\text{in}} = 40$ V to $V_{\text{in}} = 60$ V in Fig. 7.17. At 60-to-7.5 V operation, the converter reached a maximum output power of 500 W, resulting in a power density of 2680 W/in^3. At this operating point, the converter was able to achieve a peak efficiency of 98.4% (97.9% with gate drive loss included) and a full-load efficiency of 96.0% (95.9% with gate drive loss included). The full-load efficiency is improved at higher input voltages compared to the 48 V nominal input, as the increased output voltage means the conduction loss for a given load current will be a smaller proportion of the overall converter power. Table 7.10 lists the power stage and system efficiencies (including gate drive losses) for $V_{\text{in}} = 40$ V to $V_{\text{in}} = 60$ V.

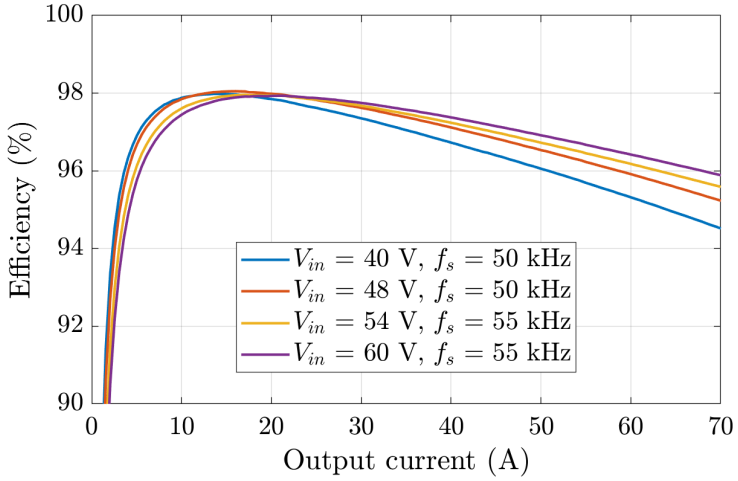


Figure 7.17: Efficiency curves including gate drive loss for $V_{\text{in}} = 40$ V to $V_{\text{in}} = 60$ V.

Table 7.10: Converter Efficiency Across V_{in}

V_{in}	Peak Efficiency (%)	Full-Load Efficiency (%)
40 V	98.6% (98.0% with gate drive)	94.6% (94.5% with gate drive)
48 V	98.6% (98.1% with gate drive)	95.3% (95.2% with gate drive)
54 V	98.4% (98.0% with gate drive)	95.7% (95.6% with gate drive)
60 V	98.4% (97.9% with gate drive)	96.0% (95.9% with gate drive)

The operating frequency of the converter at 54 V and 60 V input was increased (from 50 kHz to 55 kHz) to account for a slightly higher resonant frequency due to capacitor derating at increased voltage. The switching frequency was also increased in order to reduce the capacitor ripple seen by the switches for the MRD prototype presented in [17]. As 40 V FETs were used for the $3V_o$-rated switches in this prototype, there is still significant margin between these devices' peak operating voltages and the rated switch voltage.

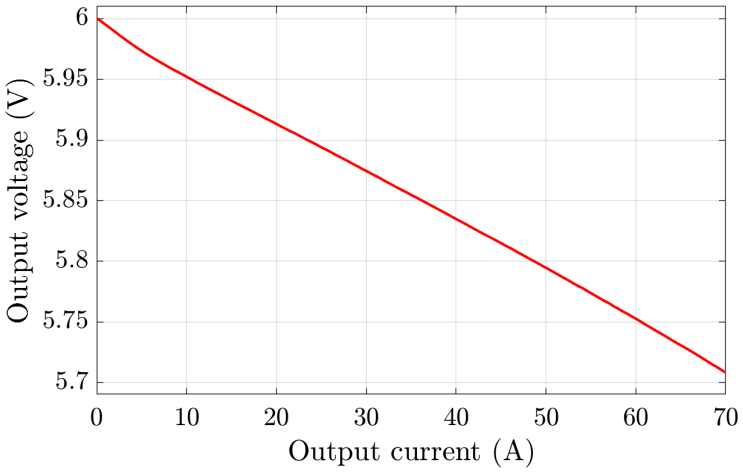


Figure 7.18: 48-to-6 V load regulation curve.

Fig. 7.18 shows the load regulation curve for the converter operating at 48-to-6 V operation. Even though the converter operates in an open-loop fixed-ratio mode, its high efficiency helps to decrease the impact of load regulation. At 48 V input, the converter exhibits a low output impedance of 4.2 mΩ and an output droop of 292 mV (4.9% of V_{out}) across the entire load range.

Fig. 7.19 shows a thermal image of the converter operating at full-load at 48 V input. The temperature of the prototype remained under 59°C during the entire load sweep when using a bench-top CPU fan to air cool the PCB.

The converter was also able to handle large load transients, as shown in Figs. 7.20a and 7.20b. The output voltage did not show significant undershoot or overshoot, and both it and the inductor current waveforms stabilized on the order of 100 μsec.

Capacitor Tolerances

As shown in Table 7.8, all flying capacitors used are Class 2 ceramic capacitors and have a tolerance of ±20%. As the converter is always operated above resonance, the capacitor values do not have to be perfectly matched.

To demonstrate the converter's robustness to capacitance variation, the board was tested with 2× additional 0805 capacitors for C_1, representing roughly a 15% increase in capac-

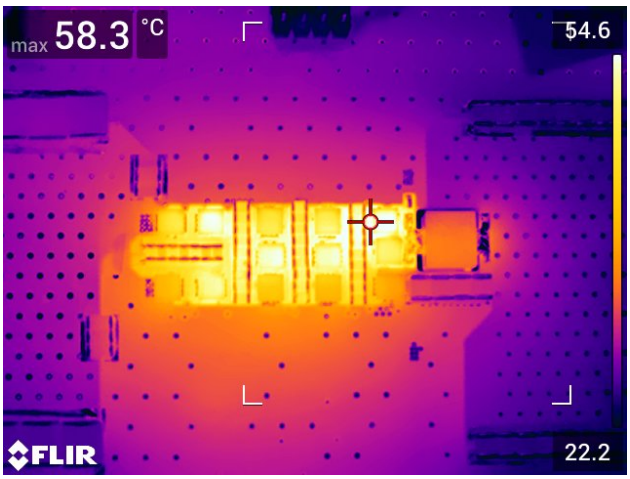
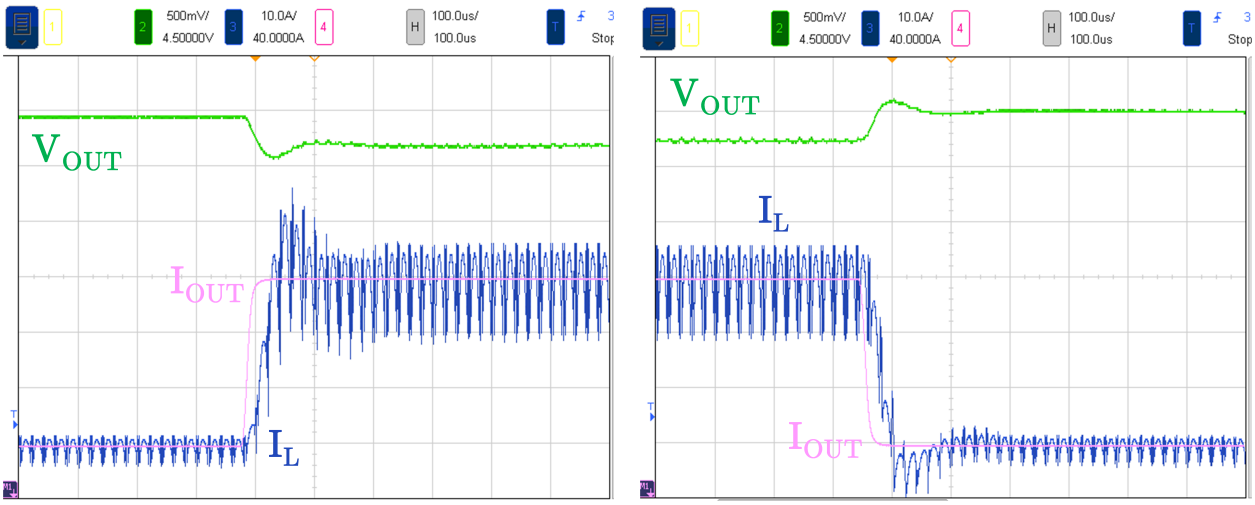


Figure 7.19: Thermal image at 48 V_{in} and 70 A.



(a) Load-step up from 10 A to 40 A.

(b) Load-step down from 40 A to 10 A.

Figure 7.20: Load transient response of the converter for a (a) step-up and (b) step-down transition at 48 V to 6 V operation.

itance. The converter efficiency was then measured across V_{in} = 40 - 60 V at the same operating frequencies as shown in Fig 7.17. At all operating conditions, the new efficiency curves were within 0.05% of the original curves.

Comparison with Contemporaneous Work

Table 7.11 compares this work with some of the best existing contemporaneous 8-to-1 works. The proposed converter can achieve a similar peak efficiency to [73], but can obtain higher output current (70 A compared to 40 A) and greater power density. Additionally, at 40 A the proposed converter has a system efficiency of 97.3%, compared to 95.9% [73]. The LLC converter in [91] takes advantage of a large step-down transformer to achieve a high full-load efficiency at a very high output current; however its power density is not as high as the hybrid SC topologies in this paper. Both the hybrid SC topologies and the LLC topology can achieve higher output current, power density, and efficiency compared to the buck topology presented in [89], showcasing the limitations of conventional buck topologies in high step-down applications.

Table 7.11: Comparison of this work and existing 8-to-1 converters

Reference	Topology	Voltage conversion	Output current (A)	Power density (W/in^3)	Full-load efficiency (%)	Peak efficiency (%)
This Work	**CaSP**	**48-to-6 V**	**70 A**	**2140**	**95.1%**	**98.0%**
MRD [73]	MRD	48-to-6 V	40 A	1675	95.9%	98.0%
EPC AppNote014 [91]	LLC	48-to-6 V	150 A	1100	96.9%,	98.0%
EPC9205 [89]	Buck	48-to-6 V	14 A	$\leq$900	91.8%	93.9%

7.4 CaSP Split-Phase Switching

As noted in Section 7.2.2, for an N:1 CaSP converter, capacitors $C_{\text{N}_\text{C}-1}$ through C_1 (i.e. the parallel-connected capacitors in Phase 3) should have the same capacitance, otherwise hard-charging will occur. However, in practical applications, these flying capacitors may be implemented with Class 2 dielectrics, whose capacitance can vary as a function of DC-bias, temperature, or aging. As described in [12, 84], the CaSP converter can be operated above resonance, so that the effect of component tolerance mismatch is reduced. For example, the hardware prototypes presented in Section 7.3 were able to achieve very high performance while using Class 2 multi-layer ceramic capacitors and operating above resonance.

However, for the experimental results provided, the switching frequency of these converters scaled with the input voltage, in order to handle the additional dc-bias derating on the

flying capacitors, which results in lowered effective flying capacitance and therefore a higher resonant frequency for the converter. The switching frequency then needed to be increased manually in order to maintain above-resonant operation.

In addition, it may be beneficial for certain applications to operate the CaSP converter at resonance, so it can achieve ZCS on the switches. This might be particularly useful at light load conditions. Therefore, if at-resonance operation is desired, or if the converter should be able to adapt to different dc-bias conditions, it may be useful to implement an active control scheme that can handle capacitor mismatch. To this end, we can explore how to adapt the concept of split-phase switching to the CaSP converter in order to account for mismatched parallel capacitors. These mismatched capacitance values will result in voltage discontinuities, similar to those discussed in Chapter 3 for Dickson converters operating without (or with incorrect) split-phase timings.

The impacts of capacitance impact can be explored on the 6-to-1 CaSP topology shown in Fig.7.21. Gate signals ϕ_1, ϕ_2, and ϕ_{12} are the same as for normal operation described earlier in this chapter. The signals ϕ_{3a} and ϕ_{3b} are the modified "split-phase" gating scheme, and can be independently delayed from the normal ϕ_3 turn-on time, in order to handle mismatch in either direction on the parallel capacitors.

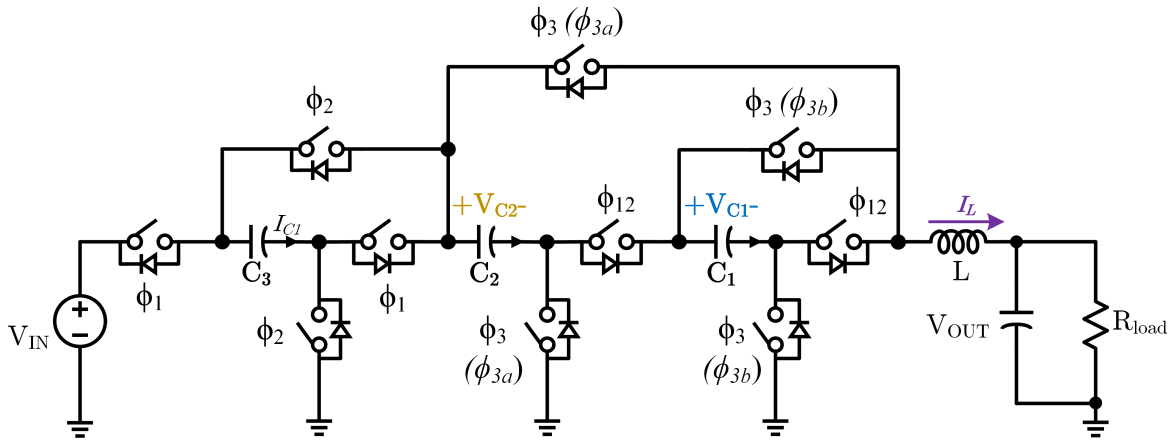


Figure 7.21: 6-to-1 CaSP converter operated with and without split-phase signals. Gate signals ϕ_1, ϕ_2, and ϕ_{12} are the same as for normal operation described earlier in this chapter. The signals ϕ_{3a} and ϕ_{3b} are the modified "split-phase" gating scheme, used to handle component mismatch on the parallel capacitors.

Fig 7.22 shows operating waveforms for the 6-to-1 CaSP converter shown in Fig 7.21, both for the case where the capacitors are matched ($C_1 = C_2$, shown in dark blue and gold), and for the case where C_2 is 1.2× larger than C_1 (shown in light blue and light gold). The gate signals use the standard operating scheme, as shown in Fig. 7.3. As capacitor C_2 has a larger capacitance than C_1, yet must conduct the same charge q_0 according to charge flow analysis, it will see a smaller voltage ripple than capacitor C_2. Therefore, when

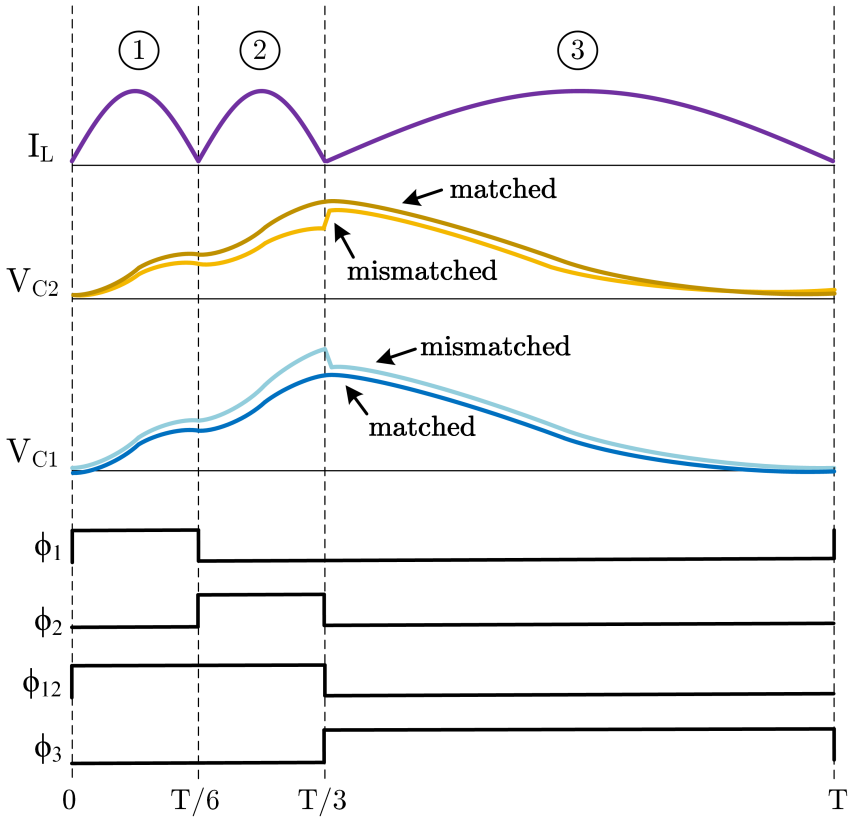


Figure 7.22: Converter operating waveforms using the normal control sequence for the CaSP 6-to-1 converter. Dark blue and gold waveforms are for the case where $C_1 = C_2$. Light blue and gold waveforms are for the case where $C_2 = 1.2 \times C_1$. The mismatched capacitance leads to voltage step discontinuities on C_1 and C_2, leading to hard-charging.

the two capacitors are connected in parallel at the start of Phase 3, both capacitors will see a large step discontinuity in their voltage waveforms, as capacitor C_2's voltage jumps up and capacitor C_1's voltage jumps down until they are matched. This is similar to the behavior seen in a hard-charged Dickson converter, where the voltage mismatch occurs due to differenes in impedance between different capacitor branches connected to the switch-node. Therefore, we can adapt the concept of split-phase switching here, to adjust the times at which C_1 and C_2 are connected to the switch-node.

As V_{C_2} sees a smaller voltage ripple than V_{C_1}, it should not be connected to the switch-node until V_{C_1} has resonated down to a lower value. Once the voltage of C_1 has losslessly discharged through the inductor, L, by the required amount, it can be connected in parallel with C_1 without any voltage mismatch, and therefore without any hard-charging. Therefore, the control signal which connects C_2 to the switch-node (i.e. ϕ_{3a}) can be *delayed* in relation to ϕ_{3b}, which connects C_1 to the switch-node.

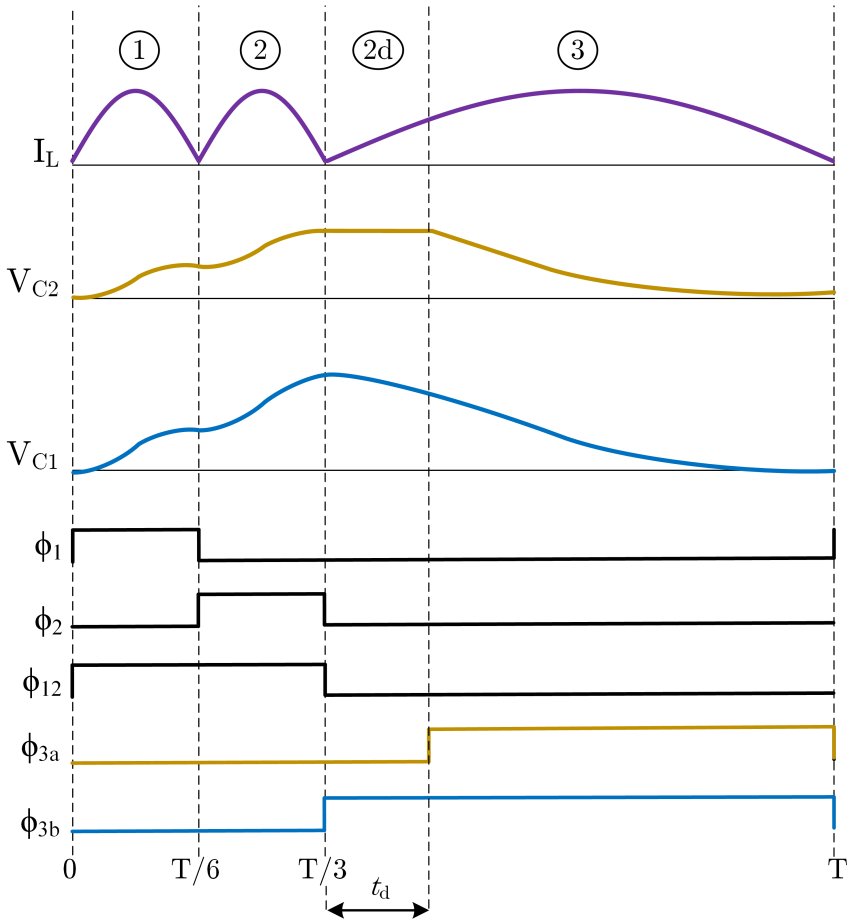


Figure 7.23: Converter operating waveforms using the modified control sequence for the CaSP 6-to-1 converter. Here, the ϕ_{3a} and ϕ_{3b} gate signals are used to handle the capacitance mismatch of $C_2 = 1.2 \times C_1$. The capacitor waveforms are now smooth and continuous, representing full soft-charging.

Fig. 7.22 shows the converter waveforms when operating with this "split-phase" control enabled. The converter can now be considered to be operating with a sub-phase $2d$ of duration t_d, which represents the delayed connection of C_2 to the switch-node. Note that this sub-phase does not have a specific capacitor configuration associated with it, as the a and b sub-phases did for split-phase switching on Dickson-type converters. For example, the ϕ_{3b} gate signal could have been delayed by t_d if C_1 was instead larger than C_2, and ϕ_{3a} could have turned on normally.

7.4.1 Experimental Validation

The control technique was validated using Class 1 capacitors to force mismatched conditions, using open-loop control. Fig. 7.24 shows an annotated photograph of the hardware prototype, and Table 7.12 provides the capacitor and inductance values used. The parallel capacitors, C_1 and C_2, were mismatched by 20%, with C_2 having the larger value. Full operating conditions are listed in Table 7.13.

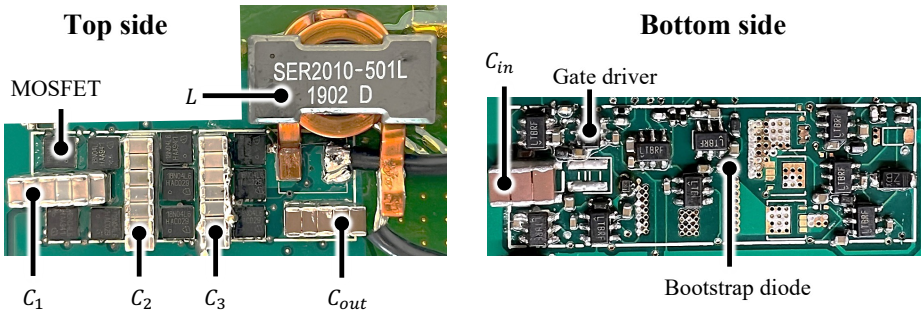


Figure 7.24: 6-to-1 CaSP converter, populated with Class 1 capacitors to validate the control technique on mismatched capacitance conditions.

Table 7.12: Main Power Components for Hardware Validation of Split-Phase Control on the 6-to-1 CaSP Converter

Component	Device	Implementation	Effective C_{fly} (μF)
C_1	Murata GRM31C5C1E474JE01L	52× 0.47 μF 25 V C0G	11 μF
C_2	Murata GRM31C5C1E474JE01L	57× 0.47 μF 25 V C0G	13.3 μF
C_3	Murata GRM31C5C1E474JE01L	4× 0.47 μF 25 V C0G	1.84 μF
L	Coilcraft SER2010-501ML	500 nH, I_{sat} = 81 A	

*The capacitance of C_2 is approximately 20% higher than C_1.

Table 7.13: Operation Conditions for Hardware Validation

Description	Parameter	Nominal
Input Voltage	V_{IN}	48 V
Output Voltage	V_{OUT}	6 V
Output Current	I_{OUT}	4 A
Switching Frequency	f_{SW}	65 kHz

Fig. 7.25 shows the converter operating at the resonant frequency, with the phase timings as derived in Section 7.2.3. Because C_2 has the larger capacitance, it has a smaller voltage ripple, and the voltage across V_{C_2} must jump up at the onset of Phase 3 (when the capacitors are connected in parallel) to accommodate for this.

By delaying the time when C_2 is connected, as shown in Fig. 7.26, the voltage on V_{C_1} can be allowed to softly resonate down until it reaches the same voltage as V_{C_2}, at which point the two capacitors can be connected in parallel without any step discontinuities or hard charge redistribution events.

While the control technique was demonstrated here as open-loop control, this voltage mismatch can be actively sensed and tuned for, using the circuitry described in Chapter 5. The polarity of the voltage mismatch can be used to determine which capacitor needs to be connected for a shorter amount of time, in a similar manner to the active split-phase control technique previously described.

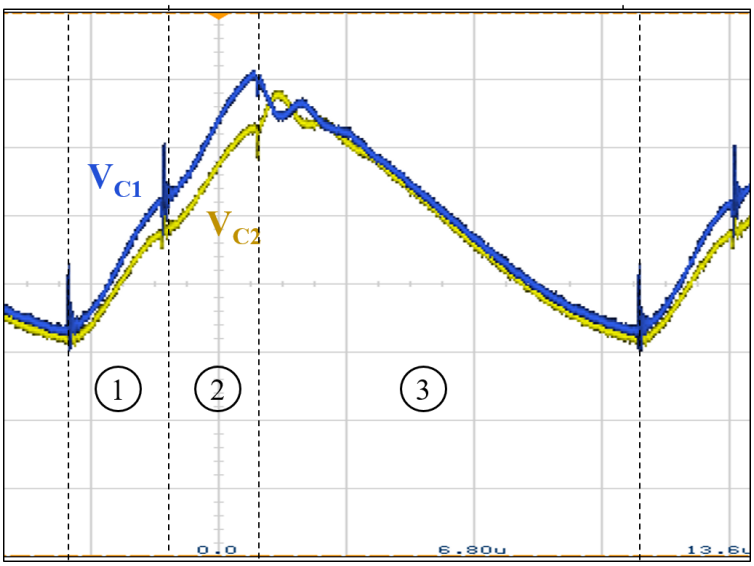


Figure 7.25: Capacitor voltage waveforms for the parallel-connected capacitors C_1 and C_2, using the standard CaSP control waveforms shown Fig. 7.22. As these capacitances are mismatched, there are hard-charging voltage discontinuities at the onset of Phase 3.

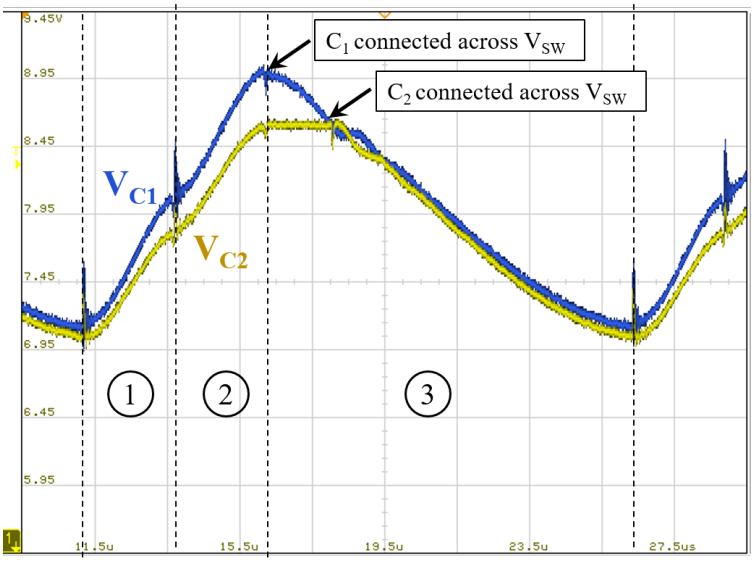


Figure 7.26: Capacitor voltage waveforms for the parallel-connected capacitors C_1 and C_2, using the modified split-phase CaSP control waveforms shown in Fig. 7.23. By delaying the connection of C_2 to the switch-node, V_{SW}, smooth voltage transitions can be achieved (i.e. no hard-charging).

7.5 Chapter Summary

Here, we have presented both theoretical analysis, general discussion, and high-performance hardware prototypes for the cascaded series-parallel (CaSP) converter. This topology is well suited to large conversion-ratios, as the multi-phase operation allows the converter to achieve the same voltage-step as conventional two-phase hybrid switched-capacitor converters with fewer switches and capacitors. Hardware prototypes designed for 48 V data center intermediate bus converter applications were presented, along with various practical details about the physical implementation of the CaSP converter. In addition, we discussed the benefits of operating multi-resonant converters slightly above resonance to reduce conduction losses, and component tolerance, as well as proposed a new control technique to account for any component mismatch should the converter be operated at or near resonance.

Chapter 8

Conclusion

This final chapter summarizes the topics presented throughout this work, and discusses some potential extensions to these techniques.

8.1 Future Work

As the demand for high performance hardware in application spaces such as data centers, automotive power trains, space and aeronautical propulsion, and many others increases, there will be a greater need for converters that 1) have inherent beneficial characteristics such as low passive volume and switch stress, 2) are demonstrated with high performance hardware that takes advantage of high-energy-density Class 2 multilayer ceramic capacitors and high-saturation-current inductors, and 3) can be robustly controlled with active tuning techniques that can handle any component tolerance mismatch conditions resulting from the use of the aforementioned types of passive components. Hybrid switched-capacitor (SC) converters can achieve very good performance in all three of these areas, as demonstrated throughout this work.

8.1.1 Active Tuning Techniques

As described in Chapter 7, the split-phase switching concept can be applied to hybrid switched-capacitor converters that would not normally be operated with it, in order to handle component tolerance mismatching between capacitors that msut satisfy specific capacitance ratios. As described in [5], many hybrid SC converters require specific capacitor sizing schemes in order to achieve soft-charging. While exactly matching this capacitance ratios is not as critical when operating above the natural resonant frequency of the converter, capacitance mismatch can have more impact near resonance. In addition, for converters such as the series-parallel, where the capacitors requiring specific capacitance ratios are connected in parallel, the dc-bias derating effects may not be very large as the capacitors all see the same voltage. However, for converters where these capacitors see different voltages or differ-

ent voltage ripples, the effects of voltage de-rating on capacitors implemented with Class 2 multilayer ceramic capacitors may be more significant.

Furthermore, as described in Chapter 7, the CaSP converter prototype hardware detailed here was operated at higher frequency when the input voltage was increased, in order to account for the lower capacitance seen at these higher dc biases. This type of modulation could be achieved using similar active sensing techniques to the one described in Chapter 7, to ensure that the converter switching frequency remains a certain ratio above the resonant frequency.

8.1.2 Customized Magnetics

Many of the hardware prototypes discussed throughout this work used off-the-shelf magnetics. The performance of these could potentially be increased by using more customized magnetics, as well as using coupled inductors for multi-inductor topologies. The active tuning techniques presented here for split-phase operation are especially attractive for this latter case, as coupled inductors can exhibit duty-cycle and current-dependent effective inductance, which would affect the split-phase timings required to achieve soft-charging. However, this effect could be sensed and mitigated using active split-phase control.

8.1.3 Split-Phase Switching Schemes

As discussed in Chapter 4, there are many naunces to applying split-phase control to real-world hardware, due to the characteristics of real switches, capacitors, and inductors. However, there is great value in investigating split-phase control in more detail, and looking at switching schemes that may reduce the number of split-phase sub-phases, or can sequence them in interesting patterns. In any case, the effects of these new control schemes should be investigated with respect to switching stress, peak passive component energy storage, and the complexity of split-phase timing calculations. The modifications made to the passive volume analysis technique presented in Chapter 6 can be adapted to converters operating with split-phase, as these converters also experience ripple-dependent mid-range capacitor voltages. However, additional work will have to be done to account for the non-half-wave-resonant waveforms seen by split-phase switches and capacitors, due to their disconnection in their respective b phases.

8.1.4 Multi-Resonant Operation of Hybrid Switched-Capacitors

The cascaded series-parallel (CaSP) converter described in Chapter 7 can be though of as a multi-resonant version of a series-parallel converter. Similar topologies can also be derived from other base hybrid SC topologies, and may also exhibit attractive performance. For example, the N-phase clocking schemes presented in [50] can be thought of as a similar transformation from a two-phase Dickson converter or Cockroft-Walton converter to a multi-

resonant topology. Similar switching schemes may be able to be derived from other base two-phase hybrid SC converters, like the Fibonacci converter.

8.2 Conclusion

Hybrid switched-capacitor (SC) converters exhibit the traditional benefits of pure SC converters, such as efficient utilization of switches and the use of energy-dense capacitors, along with lossless capacitor charge transfer due to the use of one or more augmenting inductors. In addition, increased performance can be obtained by using more complex control schemes than the traditional two-phase control common with pure switched-capacitor converters. Two classes of these control schemes were explored in this work: 1) split-phase switching for Dickson-derived converters, and 2) multi-resonant operation of hybrid SC converters. Both of these control techniques are able to achieve improved performance in many metrics, compared to their conventional two-phase counterparts. For example, split-phase control allows the Dickson converter to be operated with soft-charging, while multi-resonant operation allows for reduced component count and switch stress. These techniques can continue to be further extended to push the performance limits of hybrid SC converters.

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