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***Abstract*—This paper proposes an ultra-high-current 48-V-to-1-V hybrid switched-capacitor (SC) voltage regulator, named the switching bus converter, with a single-stage vertical power delivery architecture for next-generation ultra-high-power processors (e.g., GPUs, CPUs, ASICs, etc.). The proposed topology consists of two 2-to-1 SC front-ends and four 10-branch series-capacitor-buck modules, merged through four switching buses. Compared to the existing dc-bus-based architecture, the proposed switching-bus-based architecture eliminates the need for dc bus capacitors, reduces the switch count, and guarantees complete soft-charging operation. Through a topological comparison, this paper reveals that the proposed topology achieves the lowest normalized switch stress and the smallest normalized passive component volume among existing 48-V-to-1-V hybrid SC demonstrations, showing great potential for both higher efficiency and higher power density than prior hybrid SC solutions. A hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards to validate the functionality and performance of the proposed switching bus converter. It was tested up to 1500-A output current and achieved 92.7% peak system efficiency, 85.7% full-load system efficiency (including gate drive loss), and 759 W/in^3 power density (by box volume), pushing the performance limit of the state-of-the-art 48-V-to-1-V solutions towards higher efficiency and higher power density.**

***Index Terms*—Coupled inductor, hybrid switched-capacitor (SC) converter, point-of-load (PoL), switching-bus-based architecture, ultra-high current processor, vertical power delivery (VPD), voltage regulation module (VRM).**

I. Introduction

High-performance processors (e.g., graphics processing units [GPUs], central processing units [CPUs], application-specific integrated circuits [ASICs], etc.) serve as the engine of data center computing platforms and the foundation for technical progress in areas such as artificial intelligence, deep learning, autonomous vehicles, and numerous other applications. In recent years, the electric power consumption of processors has increased dramatically and is approaching 1000 W due to the fast-growing demand for greater computational power. For example, as shown in Fig. 1, the thermal design power (TDP) of NVIDIA data center GPUs has grown by 10 times in the past decade, from 106 W to 1000 W. And just in the past three years alone, the TDP has more than doubled.

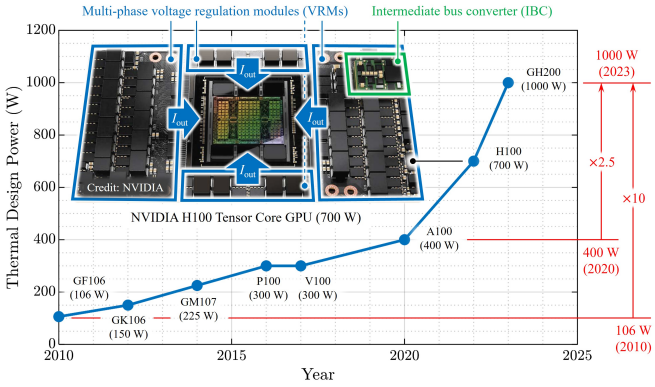

Fig. 1: The past decade has witnessed rapid growth in the thermal design power (TDP) of NVIDIA data center GPUs [1]. The picture of NVIDIA H100 tensor core GPU [2] shows the existing two-stage lateral power delivery (LPD) architecture where the current flowing out of the voltage regulation modules (VRMs) needs to travel a long distance to the processor pins, leading to a large power distribution network (PDN) and high PDN losses.

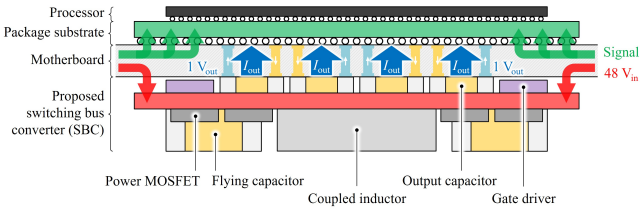

Fig. 2: Single-stage vertical power delivery (VPD) architecture for next-generation ultra-high-power processors with the proposed 48-V-to-1-V switching bus converter (SBC). In this VPD solution, the SBC on the bottom side of the motherboard can vertically deliver an ultra-high current to the processor on the top side through vias, which can greatly reduce the PDN size and PDN losses.

As power levels increase, the 48-V bus architecture is gradually replacing the legacy 12-V dc bus in modern data centers since the power distribution losses (i^2R losses) decrease by sixteen-fold with the quadrupling of the bus voltage. This makes the design of the voltage regulation modules (VRMs) responsible for the 48 V to point-of-load (PoL) power conversion more challenging with a quadrupled voltage conversion burden. In addition to a large conversion ratio of 48-to-1 or higher, the VRMs for next-generation ultra-high power

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processors should be capable of sourcing ultra-high current ($\geqslant$ 1000 A) at low supply voltage ($\leqslant$ 1.0 V) and achieving high power density, high efficiency, and fast dynamic response.

To address these challenges, multiple solutions have been proposed in previous literature for 48-V-to-PoL power conversion in data centers, including transformer-based solutions [3]–[8] and hybrid switched-capacitor (SC) solutions [9]–[25]. Relying on highly optimized LLC converters [26], transformer-based solutions can achieve high performance with integrated magnetics and planar matrix transformers which leverages flux cancellation [27]. Although galvanic isolation is achievable in transformer-based topologies, it is typically not necessary for 48-V-to-PoL applications [28]. As an emerging family of topologies, hybrid SC converters can leverage both the greatly superior energy density of capacitors compared to magnetic components [29], [30] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [31].

Both transformer-based and hybrid SC solutions can be developed with either a two-stage architecture [4], [5], [12], [14], [15], [18], [22] or a single-stage architecture [6]–[11], [13], [16], [17], [19]–[21], [23]–[25]. In the two-stage architecture, the 48-V bus voltage needs to be first stepped down to a lower dc bus voltage (e.g., 12/8/6 V) with a fixed-ratio intermediate bus converter (IBC) such as LLC converters [4], [5], [27] and resonant SC converters [32]–[35], and then regulated down to 1 V at the point-of-load (PoL) with multi-phase VRMs. In the single-stage architecture, as its name suggests, the 48-V bus voltage is directly regulated down to 1 V within one conversion stage without an intermediate dc bus.

The picture of the NVIDIA H100 tensor core GPU [2] in Fig. 1 shows the existing two-stage lateral power delivery (LPD) architecture where the current flowing out of the VRMs needs to travel a long distance to the processor pins, leading to a large power distribution network (PDN). With a load current beyond 1000 A, the high PDN resistance can lead to a dramatic voltage drop and unacceptable conduction losses, which significantly limits processor performance, reduces system energy efficiency, and hinders data center decarbonization. Moreover, the resulting low efficiency necessitates a larger size of the thermal management solution, which is presently a bottleneck of system densification.

In pursuit of a more efficient and compact alternative to the existing two-stage LPD solution for next-generation ultra-high-power processors, this paper proposes an ultra-high-current 48-V-to-1-V hybrid SC voltage regulator, named the switching bus converter (SBC), to address the aforementioned challenges through single-stage vertical power delivery (VPD), as illustrated in Fig. 2. In this single-stage VPD solution, the proposed SBC is placed on the bottom side of the motherboard directly underneath the processor so that it can deliver the ultra-high current vertically to the top side through vias, which greatly reduces the PDN size and PDN losses and saves the valuable topside area on the motherboard for high-speed communication and memories. Moreover, merging two conversion stages into one single stage reduces power conversion losses and eliminates the need for dc bus capacitors, which effectively improves overall system efficiency and power density.

More specifically, the proposed topology merges two 2-to-1 SC front-ends and four 10-branch series-capacitor-buck (SCB) modules through four switching buses. Revealed by a topological comparison, the proposed topology exhibits the theoretical potential of achieving both higher efficiency and higher power density than existing 48-V-to-1-V hybrid SC demonstrations. To validate its theoretical potential, a hardware prototype was built with custom four-phase coupled inductors and gate drive daughterboards and tested up to 1500 A of output current. The prototype achieved a peak system efficiency of 92.7%, a full-load system efficiency of 85.7%, and a power density of 759 W/in^3 at 1500-A output current and 1-V output voltage. This article expands upon our earlier conference publications [36], [37] with additional explanations for the design and optimization of the four-phase coupled inductor, an in-depth loss analysis of the hardware prototype, as well as a more comprehensive performance comparison with the state-of-the-art academic and industry solutions.

The remainder of this paper is organized as follows: First, Section II introduces the topology and operating principles of the proposed switching bus converter, explains the advantages of the proposed switching-bus-based architecture over the existing dc-bus-based architecture, and demonstrates the theoretical potential of the proposed topology through a topological comparison. Section III presents the 1500-A hardware prototype and discusses the key design considerations for the four-phase coupled inductor and the gate drive circuitry. Section IV demonstrates measured performance, loss analysis, and performance comparison with state-of-the-art academic works and commercial products. Finally, Section V summarizes the contribution of this paper.

II. Switching Bus Converter

A. Proposed Topology and Operating Principles

Fig. 3 shows the schematic drawing of the proposed switching bus converter, which merges two 2-to-1 SC front-ends (i.e., Stage 1) with four 10-branch series-capacitor-buck (SCB) modules (i.e., Modules A-D in Stage 2) through four intermediate buses (i.e., Switching buses A-D). As illustrated in the key waveforms and control signals in Fig. 4, the intermediate bus voltages $v_{\rm swA}$–$v_{\rm swD}$ always switch between two voltage levels rather than being dc. Therefore, this type of intermediate bus interfacing two conversion stages is referred to as a *switching bus*, the concept of which was first introduced in [19]. It should be noted that although the SC front-ends and SCB modules are referred to as Stage 1 and Stage 2 in the schematic drawing to facilitate understanding, the proposed topology is still considered a single-stage architecture since there is no intermediate dc bus.

Each SCB module consists of five submodules and operates in a two-phase fashion with a 180° phase shift between neighboring branches. The control signals of Modules C and D are 90° phase shifted with respect to those of Modules A and B to ensure the four-phase symmetric interleaving of $\phi_{\rm 1A}$, $\phi_{\rm 1C}$, $\phi_{\rm 2A}$, and $\phi_{\rm 2C}$, and of $\phi_{\rm 1B}$, $\phi_{\rm 1D}$, $\phi_{\rm 2B}$, and $\phi_{\rm 2D}$, which enables the use of four-phase coupled inductors illustrated with the grey boxes. All flying capacitor voltages and inductor currents

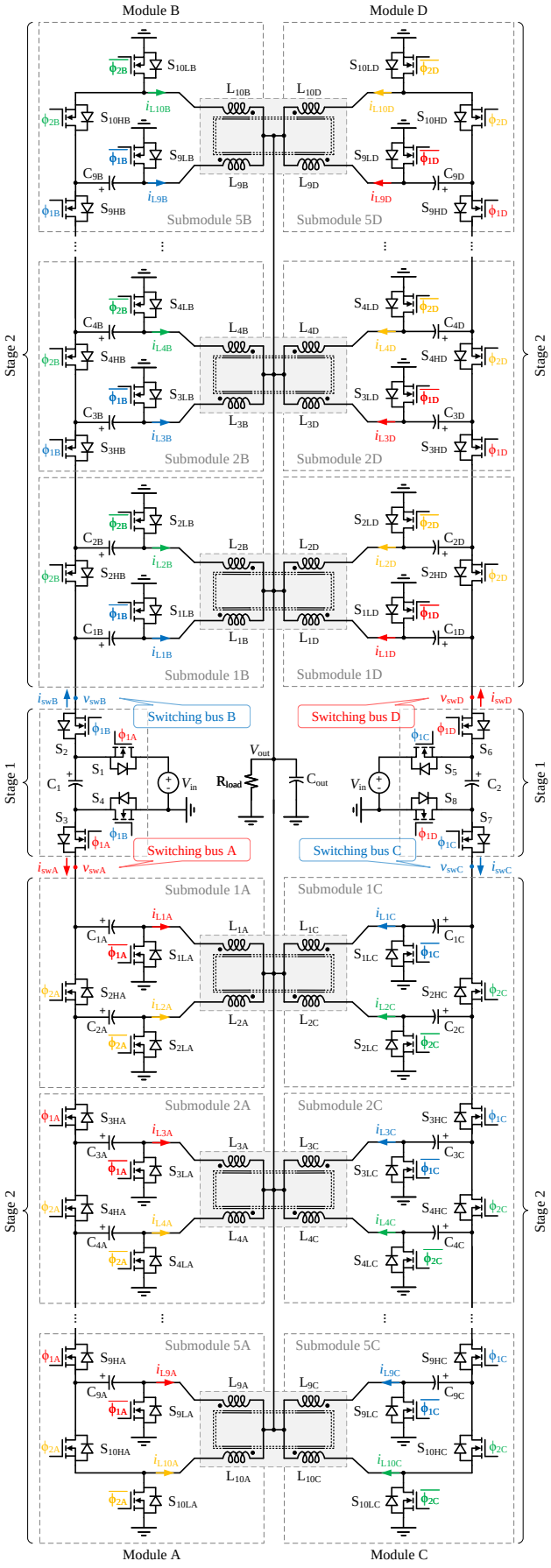

Fig. 3: Schematic drawing of the proposed switching bus converter (SBC).

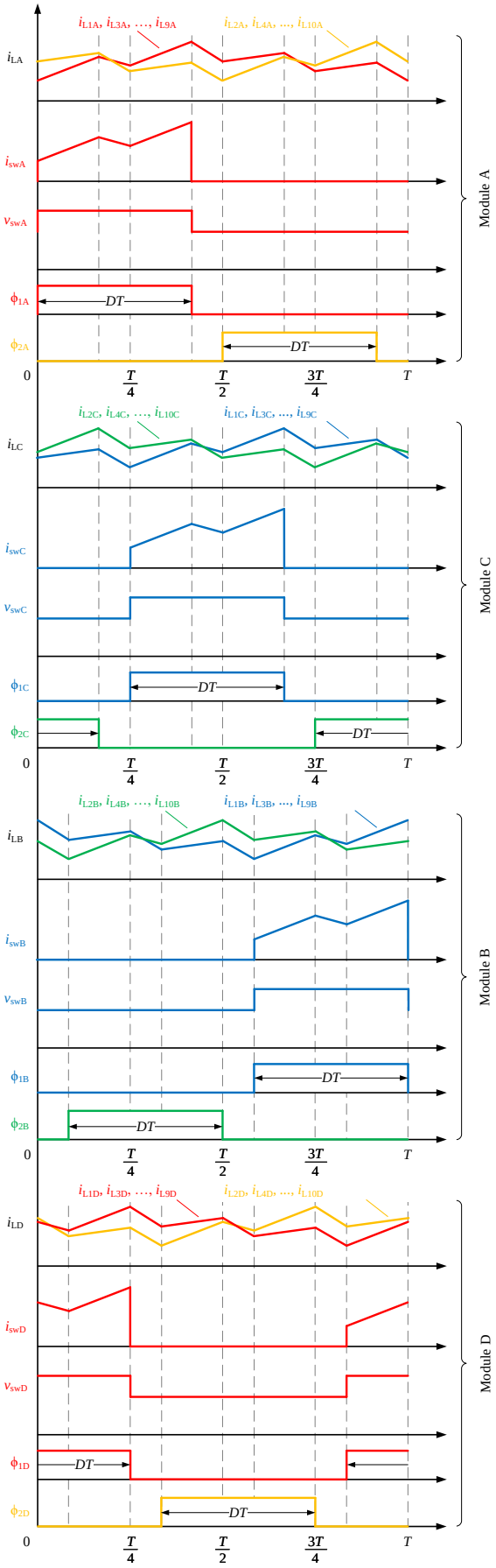

Fig. 4: Key waveforms and control signals.

TABLE I: Topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations

Year	Reference	SC Stage Conversion Ratio (K_{SC})	Buck Stage Conversion Ratio (K_{buck})	Buck Stage Duty Ratio (D)	Normalized Switch Stress (M_{S})	Normalized Passive Component Volume (M_{P})
2020	Crossed-coupled QSD buck [10]	4:1	12:1	0.083	24.2	2.08
2020	DIH [11]	6:1	8:1	0.125	14.7	2.40
2021	CaSP [13]	6:1	8:1	0.125	23.5	2.02
2022 2024	LEGO [15] Mini-LEGO [22]	6:1	8:1	0.125	17.6	2.41
2024	SDIH [21]	6:1	8:1	0.125	14.7	2.40
2022	MLB [17]	8:1	6:1	0.167	23.7	2.03
2022	VIB [18]	8:1	6:1	0.167	14.3	2.07
2023	MSC [24]	8:1	6:1	0.167	15.1	1.95
2022	Dickson^2 [19]	9:1	5.33:1	0.188	14.8	1.90
2024	16-to-1 SBC [23]	16:1	3:1	0.333	10.2	1.69
2024	This work	20:1	2.4:1	0.417	8.99	1.56

in the proposed topology are naturally balanced because of the negative feedback mechanism of the series-capacitor-buck (SCB) converter, as explained in [38] and [39]. The low-side switches $\mathrm{S_{1LX-10LX}}$ ($\mathrm{X = A, B, C, D}$) can operate with zero-voltage switching (ZVS) turn-ON, provided continuous forward inductor current and sufficient deadtime.

In existing dc-bus-based two-stage architectures [4], [5], [12], [14], a large dc bus capacitor is typically required to maintain a stiff dc bus voltage, which hinders converter miniaturization. In [18], the intermediate bus capacitance was reduced by allowing a significant ripple on the bus voltage. However, this led to the hard-charging between the intermediate bus capacitor and flying capacitors, which induced additional charge-sharing losses. Similarly, in [15], [22], filter capacitors were required on the intermediate buses to filter the high-frequency pulsating current from the buck stage, which led to undesired hard-charging operation and additional charge-sharing losses. In contrast, the proposed switching-bus-based architecture allows the intermediate buses to switch between two voltage levels, thus eliminating the need for intermediate bus capacitors, while guaranteeing complete soft-charging operation for all flying capacitors as well. In addition, the switching-bus-based architecture enables a reduction in the number of switches, since one redundant switch is removed on each switching bus while the two stages are merged [23].

It is worth noting that the switching bus concept can be generalized to enable the combination of different SC topologies. As a result, a family of regulated hybrid SC topologies can be generated. For example, the Dickson^2 converter [19], where the concept of a switching bus was first introduced, merges a 3-to-1 Dickson front-end and three 3-branch SCB modules through three switching buses. Other examples include the MLB converter [16] and the CaSP converter [13]. In addition to regulated hybrid SC topologies, the switching bus concept has also been adopted in fixed-ratio multi-resonant SC converters [35] for 48-V-to-12-V data center applications.

B. Topological Comparison

In this section, a topological comparison is performed to show the theoretical potential of the proposed topology compared to existing 48-V-to-1-V hybrid SC demonstrations. The topological comparison is based on two metrics: a) normalized switch stress as an indicator of efficiency and b) normalized passive component volume as an indicator of power density.

The normalized switch stress, denoted as M_{S}, is defined as the total switch volt-ampere (VA) stress normalized to the output power, expressed by the following equation:

$$M_{\mathrm{S}} = \frac{\sum\limits_{\text{switches}} V_{\mathrm{ds},i} I_{\mathrm{d(rms)},i}}{V_{\mathrm{out}} I_{\mathrm{out}}}, \tag{1}$$

where $V_{\mathrm{ds},i}$ represents the peak blocking voltage across switch i assuming no capacitor voltage ripple, and $I_{\mathrm{d(rms)},i}$ is the RMS value of the current through switch i assuming no inductor current ripple. The M_{S} value serves as an indicator of the VA stress experienced by the switches in a given topology when transferring one per-unit watt of power from input to output. A lower normalized switch stress is preferable because it indicates lower switching losses, lower conduction losses, and smaller switch sizes, which contribute to higher efficiency and higher power density.

The normalized passive component volume, denoted as M_{P}, can be assessed with an energy-based approach by analyzing the peak energy stored in each passive component [30], [40]. The M_{P} value reflects the overall volume of passive components required to meet given ripple requirements on inductor currents and flying capacitor voltages while transferring one per-unit watt of power from input to output. A smaller normalized passive component volume is preferred, as it indicates higher power density. Detailed derivations and analyses of the normalized passive component volume can be found in [41].

A topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations is presented in Table I and visualized in Fig. 5. The M_{P} values in Table I

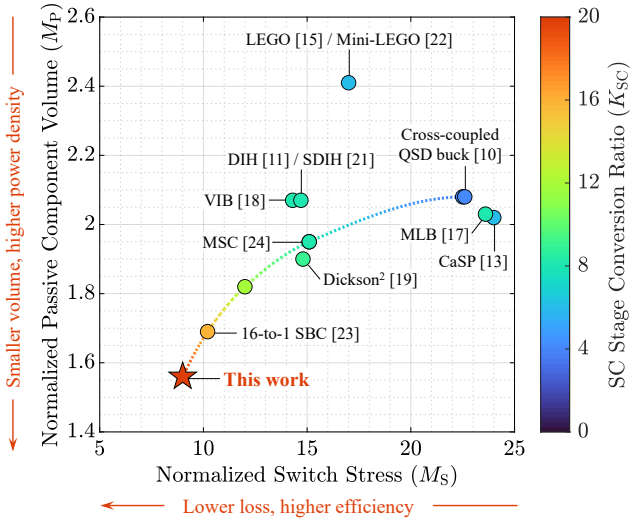

Fig. 5: Normalized switch stress (M_S), normalized passive component volume (M_P) and SC stage conversion ratio (K_{SC}) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. A lower normalized switch stress is more desirable since it indicates lower losses and higher efficiency. A smaller normalized passive component volume is preferable, as it implies a smaller converter volume and higher power density. The proposed switching bus converter topology can be extended to different SC stage conversion ratios by changing the number of submodules in Stage 2, as illustrated with the dashed curve. Each dot on the dashed curve represents an implementation of the switching bus converter at a SC stage conversion ratio corresponding to its color.

and Fig. 5 were calculated assuming the use of discrete, uncoupled inductors. A regulated hybrid SC topology typically consists of a SC stage for fixed-ratio voltage step-down and a multi-phase buck-type stage for the remainder of the voltage conversion task, output voltage regulation, and soft-charging operation [41]. A larger SC stage conversion ratio (K_{SC}) alleviates the conversion burden on the following buck-type stage and enables buck-type stage efficiency improvement and inductor size reduction. Due to the fact that inductors are much less energy dense compared to capacitors [42] and typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden, which contributes to overall converter volume reduction and efficiency improvement. The proposed switching bus converter topology can be extended to different SC stage conversion ratios by changing the number of submodules in Stage 2. For 48-V-to-1-V conversion, the allowed SC stage conversion ratios are $K_{SC} = 4, 8, 12, 16, 20$. Given that a larger SC stage conversion ratio enables higher performance, this work adopts the maximum allowable SC stage conversion ratio $K_{SC(max)} = 20$. It is worth noting that such a large SC stage conversion ratio is enabled by the two-phase operation of the SCB modules and is not achievable with the conventional multi-phase operation [23].

As shown in Table I and Fig. 5, the proposed topology stands out as it achieves the lowest normalized switch stress and the smallest normalized passive component volume with the largest SC stage conversion ratio, indicating its great potential for both higher efficiency and higher power density compared to prior hybrid SC solutions.

III. Hardware Implementation and Design Considerations

This section introduces a 48-V-to-1-V hardware prototype designed and constructed to validate the functionality and performance of the proposed topology. Fig. 6 presents the photograph of the prototype, with the top view showing the power stage and the bottom view showing the gate drive circuitry. Fig. 7 annotates the submodules and main circuit components of the prototype, which shows its good modularity and extendibility. Table II lists the main circuit components.

To optimize the use of the prototype's box volume, all flying capacitors are stacked in two layers, aligning with the height of the coupled inductors. The stacked flying capacitors also function as effective natural heat sinks, as they are connected to power MOSFETs through thermally conductive PCB traces. Moreover, the distributed switch and capacitor network contribute to an inherent heat-spreading mechanism. The 2-mm thick PCB has 6 layers, with 6-oz copper on the two outer layers and 2-oz copper on the four inner layers.

A. Four-Phase Coupled Inductor

As introduced in Section II-A, each group of the four inductors highlighted with grey boxes in Fig. 3 can be implemented as a four-phase coupled inductor. Compared to discrete inductors, coupled inductors can achieve faster transient response without sacrificing steady-state current ripple [43] and can achieve core volume reduction through dc flux cancellation [17].

In pursuit of high performance, a four-phase coupled inductor presented in Fig. 8 comprising two pieces of magnetic cores and four pieces of one-turn copper windings was customized for this hardware prototype. The magnetic cores were fabricated with DMEGC DMR96A Mn-Zn ferrite material [44]. To minimize conduction losses on the vertical output current path, each winding is connected to the output bus bar on the back of the PCB through plated through holes.

The subsequent part of this subsection details the key design considerations and optimizations of the four-phase coupled inductor. The per-phase steady-state inductance (L_{ss}) and transient inductance (L_{tr}) [45], [46] of a symmetric four-phase coupled inductor operating at a duty ratio between 0.25 and 0.5 can be expressed as

$$L_{ss} = \frac{\left(1-\frac{\alpha}{3}\right)(1+\alpha)}{1+\left(\frac{1}{D}+\frac{3}{D'}-2\right)\frac{\alpha}{6}} L \tag{2}$$

$$L_{tr} = (1+\alpha)\, L, \tag{3}$$

where D is the duty ratio, $D' = 1 - D$, L and M are the self and mutual inductances of the coupled inductor, and α is the coupling coefficient defined as

$$\alpha = \frac{3M}{L}. \tag{4}$$

In this design, the four phases of the coupled inductor are negatively coupled to achieve dc flux cancellation, meaning that the mutual inductance (M) is negative, resulting in a

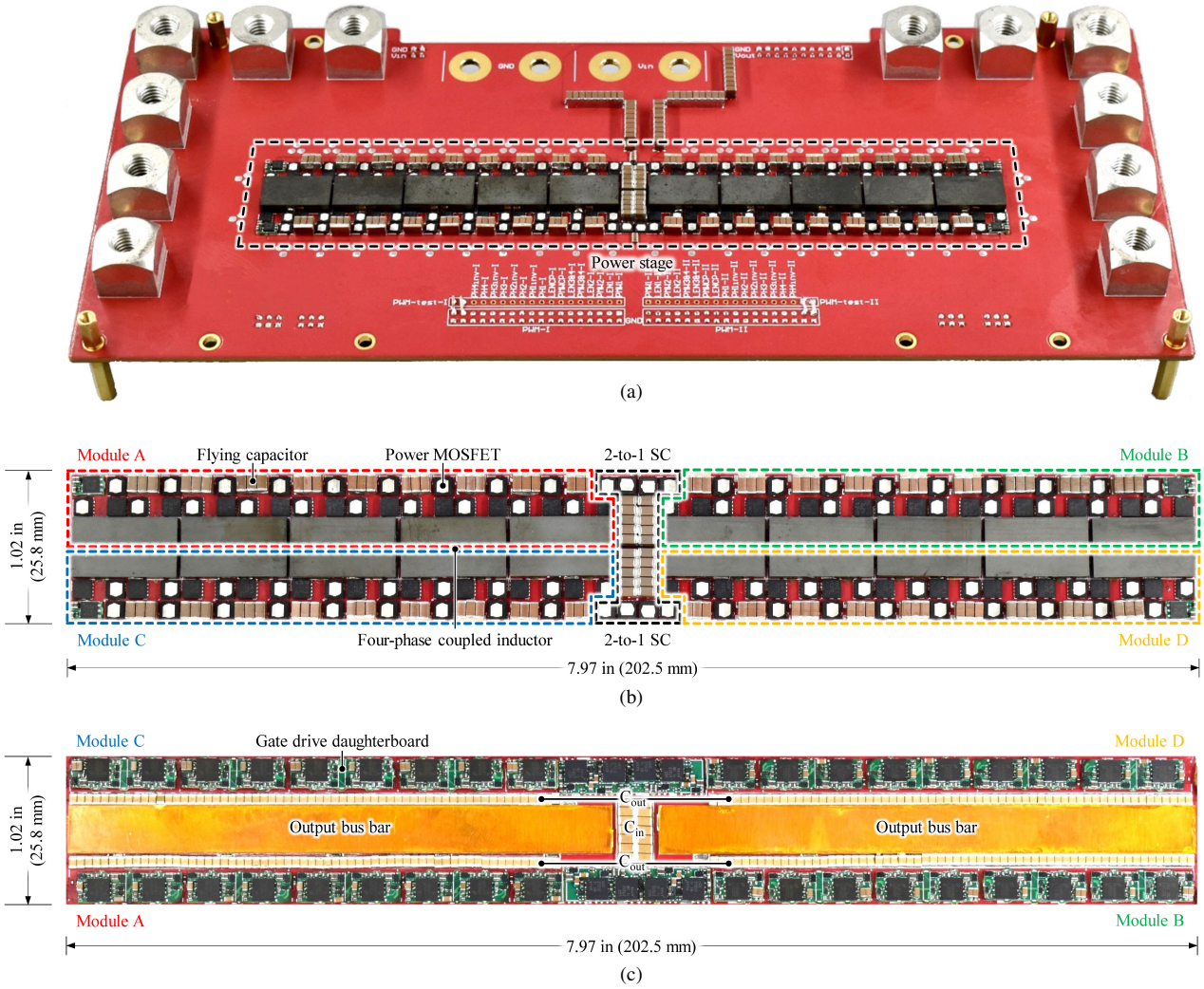

Fig. 6: Photograph of the hardware prototype. Converter dimensions: $7.97 \times 1.02 \times 0.244$ in^3 ($202.5 \times 25.8 \times 6.2$ mm^3). (a) Complete view. (b) Top view showing the power stage. (c) Bottom view showing the gate drive circuitry.

TABLE II: Component list of the hardware prototype

Component (X = A, B, C, D)	Part number	Parameters
MOSFET S_{1-8}	Infineon IQE013N04LM6CGSC	40 V, 1.35 mΩ, dual-side cooling
MOSFET $S_{2HX-10HX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
MOSFET $S_{1LX-10LX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
	Infineon IQE004NE1LM6	15 V, 0.45 mΩ
Flying capacitor $C_{1,2}$	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 µF*×20 (in parallel)
Flying capacitor C_{1X-6X}	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 µF*×6 (in parallel)
Flying capacitor C_{7X-9X}	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 µF*×6 (in parallel)
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 µF*×14 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 µF*×248 (in parallel)
Gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
Low-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink
High-side gate driver in Stage 2	Texas Instruments LM27222	3-A peak source, 4.5-A peak sink

* The capacitance listed in this table is the nominal value before dc derating.

negative coupling coefficient. In (4), the coupling coefficient (α) has been normalized and is a design variable that can vary between 0 and -1. A coupling coefficient closer to -1 indicates stronger magnetic coupling.

In practical design problems, the per-phase steady-state inductance (L_{ss}) of a coupled inductor needs to be greater than or equal to a minimum value ($L_{\text{ss(min)}}$) in order to meet given current ripple requirements, i.e., to ensure the per-phase peak-to-peak current ripple does not exceed the specified upper limit $\Delta i_{\text{L,pp(max)}}$. This minimum steady-state inductance value can

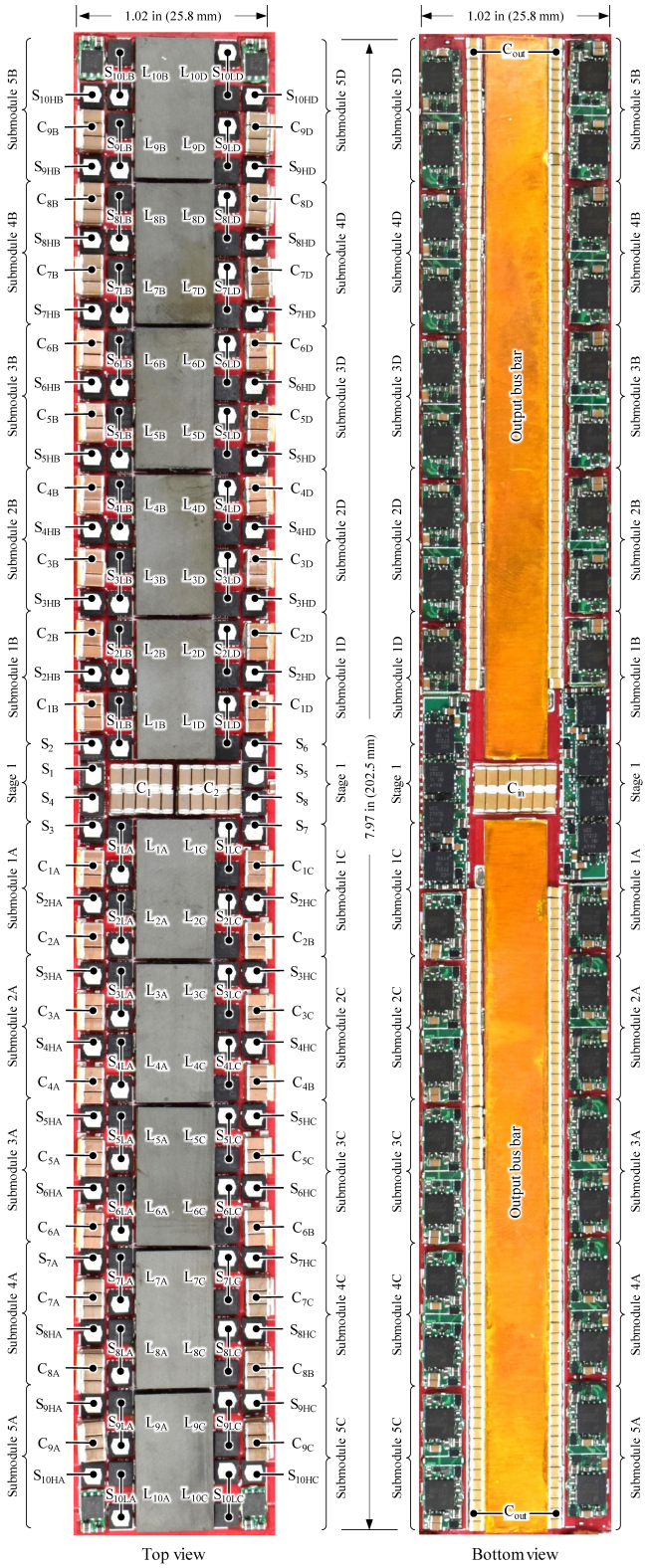

Fig. 7: Submodules and key circuit components of the hardware prototype.

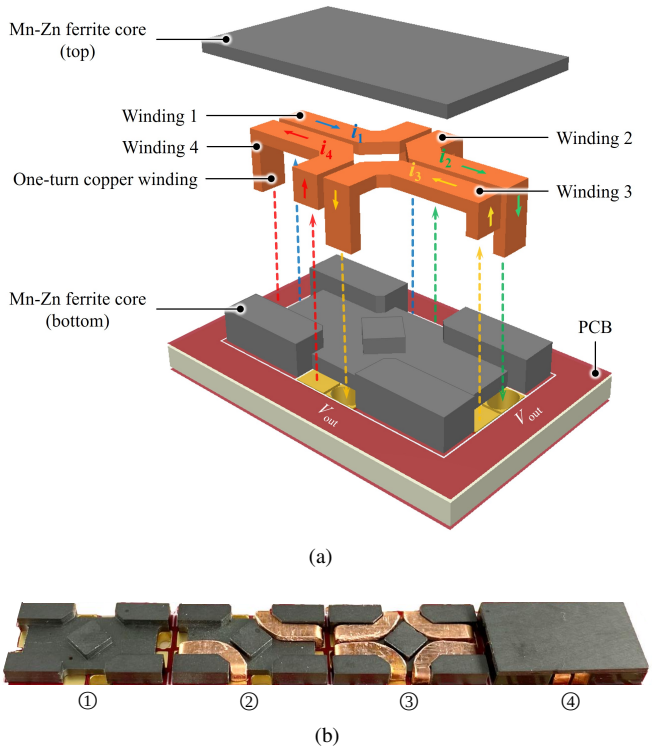

Fig. 8: Custom four-phase coupled inductor. Dimensions: $18.5 \times 10.5 \times 3.2$ mm^3. (a) 3D rendering of the coupled inductor with current paths annotated. Each winding is connected to the output bus bar on the back of the PCB through plated through holes in order to minimize conduction losses on the output current path for VPD. (b) Coupled inductor assembly with two pieces of Mn-Zn ferrite cores and four pieces of one-turn copper windings: ①→ ②→ ③→ ④ .

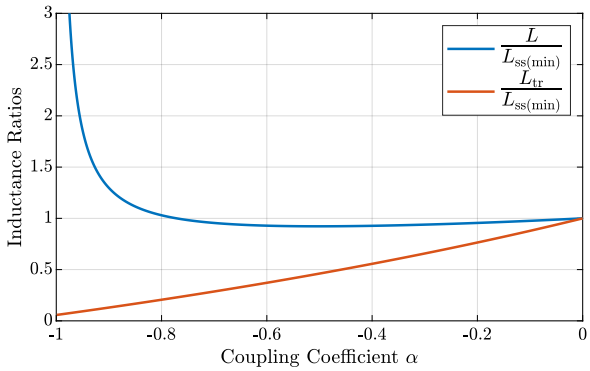

Fig. 9: Ratios of the self and transient inductances to the steady-state inductance ($\frac{L}{L_{ss}}$ and $\frac{L_{tr}}{L_{ss}}$) as functions of the coupling coefficient (α) when the duty ratio (D) is 0.417. Magnetic coupling becomes stronger as α varies from 0 towards -1.

be calculated as

$$L_{\mathrm{ss(min)}} = \frac{D' V_{\mathrm{out}}}{f_{\mathrm{sw}} \Delta i_{\mathrm{L,pp(max)}}}, \tag{5}$$

where f_{sw} is the switching frequency and V_{out} is the output voltage. Since $L_{\mathrm{ss(min)}}$ is a design target that needs to be satisfied, it is fixed in the following optimization procedure.

Fig. 9 shows the ratios of the self and transient inductances to the minimum steady-state inductance ($\frac{L}{L_{\mathrm{ss(min)}}}$ and $\frac{L_{\mathrm{tr}}}{L_{\mathrm{ss(min)}}}$) when $D = 0.417$, which can be obtained from (2) and (3) as

$$\frac{L}{L_{\mathrm{ss(min)}}} = \frac{1 + \left(\frac{1}{D} + \frac{3}{D'} - 2\right)\frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3}\right)(1+\alpha)} \tag{6}$$

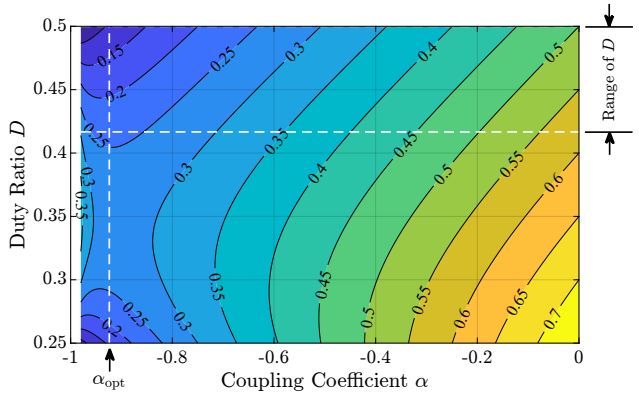

Fig. 10: Optimization of the coupling coefficient (α) with a duty ratio (D) varying between 0.417 and 0.5. The color and contour lines of this figure show the value of the normalized cost function ($\hat{f}(\alpha, D)$) defined in (8).

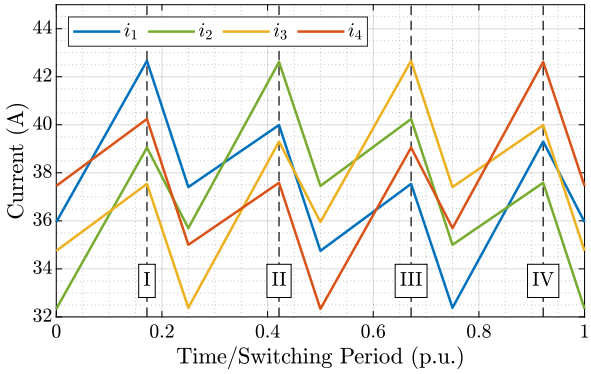

Fig. 11: Simulation waveforms of winding currents for the four-phase coupled inductor at full load, with a per-phase average current of 37.5 A and other operating conditions listed in Table III. The directions of the winding currents are illustrated in Fig. 8(a). The magnetic cores are most prone to saturation at Moments I–IV when the current in one phase reaches its peak value, as annotated with the dashed line. The magnetic flux density distributions in the bottom core at Moments I and II are shown in Fig. 12.

$$\frac{L_{\text{tr}}}{L_{\text{ss(min)}}} = \frac{1 + \left(\frac{1}{D} + \frac{3}{D'} - 2\right)\frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3}\right)}. \tag{7}$$

As can be seen, the transient inductance (L_{tr}) always decreases with stronger coupling (i.e., with a coupling coefficient α closer to -1), which contributes to a faster transient response. However, with a coupling coefficient beyond -0.8, the self-inductance (L) required to maintain the minimum steady-state inductance ($L_{\text{ss(min)}}$) increases dramatically. For a coupled inductor with a fixed length of air gap, a higher self-inductance typically requires a larger core volume. This implies that the self-inductance can serve as a proxy for the core volume in the optimization of gapped coupled inductors. Given $L_{\text{ss(min)}}$, a coupled inductor design that requires a smaller self-inductance (L) is preferable, as it indicates a smaller core volume.

For a smaller core volume and a faster transient response, the self-inductance (L) and the transient inductance (L_{tr}) both need to be minimized. To strike a trade-off between these two conflicting objectives, a cost function is defined for this optimization problem as the geometric mean of L and L_{tr}:

$$f(\alpha, D) = \sqrt{L L_{\text{tr}}}, \tag{8}$$

which needs to be minimized. With (5)-(7) inserted, equation (8) can be rearranged as

$$f(\alpha, D) = \frac{D' + \left(\frac{D'}{D} + 3 - 2D'\right)\frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3}\right)\sqrt{1+\alpha}} \cdot \frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp(max)}}}. \tag{9}$$

Since V_{out}, f_{sw} and $\Delta i_{\text{L,pp(max)}}$ are fixed in each design, $f(\alpha, D)$ can be normalized by $\frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp(max)}}}$ as

$$\hat{f}(\alpha, D) = \frac{f(\alpha, D)}{\frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp(max)}}}} = \frac{D' + \left(\frac{D'}{D} + 3 - 2D'\right)\frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3}\right)\sqrt{1+\alpha}}. \tag{10}$$

It is worth noting that this normalized cost function ($\hat{f}(\alpha, D)$) is dimensionless and design-independent, which makes it widely applicable for the optimization of gapped coupled inductors. Apparently, minimizing $f(\alpha, D)$ is equivalent to minimizing $\hat{f}(\alpha, D)$.

TABLE III: Key parameters and operating conditions of the four-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.91
Per-phase steady-state inductance*	260 nH
Per-phase transient inductance	31.8 nH
Overall transient inductance (40 phases)	0.80 nH
Per-phase dc resistance	0.16 mΩ
Output voltage	1.0 V
Switching frequency	220 kHz
Nominal duty ratio	0.417
Per-phase peak-to-peak current ripple*	10.2 A
Per-phase average current at full load	37.5 A
Height	3.2 mm

* Four-phase average value at $D = 0.417$.

The nominal duty ratio of the proposed topology for 48-V-to-1-V conversion is 0.417, and the maximum allowable duty ratio during transients is 0.5. To minimize the normalized cost function ($\hat{f}(\alpha, D)$) while ensuring that the peak-to-peak current ripple never exceeds $\Delta i_{\text{L,pp(max)}}$ when the duty ratio (D) varies between 0.417 and 0.5, the optimum coupling coefficient (α_{opt}) can be obtained as

$$\alpha_{\text{opt}} = \underset{\alpha \in [-1,0]}{\text{argmin}} \Big(\underbrace{\max_{D \in [0.417, 0.5]} \hat{f}(\alpha, D)}_{\text{worst-case scenario for each } \alpha} \Big). \tag{11}$$

Fig. 10 illustrates this optimization process by sweeping α and D within the range of interest, with the color and contour lines showing the value of $\hat{f}(\alpha, D)$. According to Fig. 10, the optimum coupling coefficient (α_{opt}) for this design is -0.92, which minimizes $\hat{f}(\alpha, D)$ and thus minimizes $f(\alpha, D)$.

The four-phase coupled inductor illustrated in Fig. 8 was designed around this optimum coupling coefficient $\alpha_{\text{opt}} = -0.92$, with manufacturing tolerances taken into consideration. Table III summarizes key parameters and operating conditions of this four-phase coupled inductor.

The current handling capability of the designed four-phase

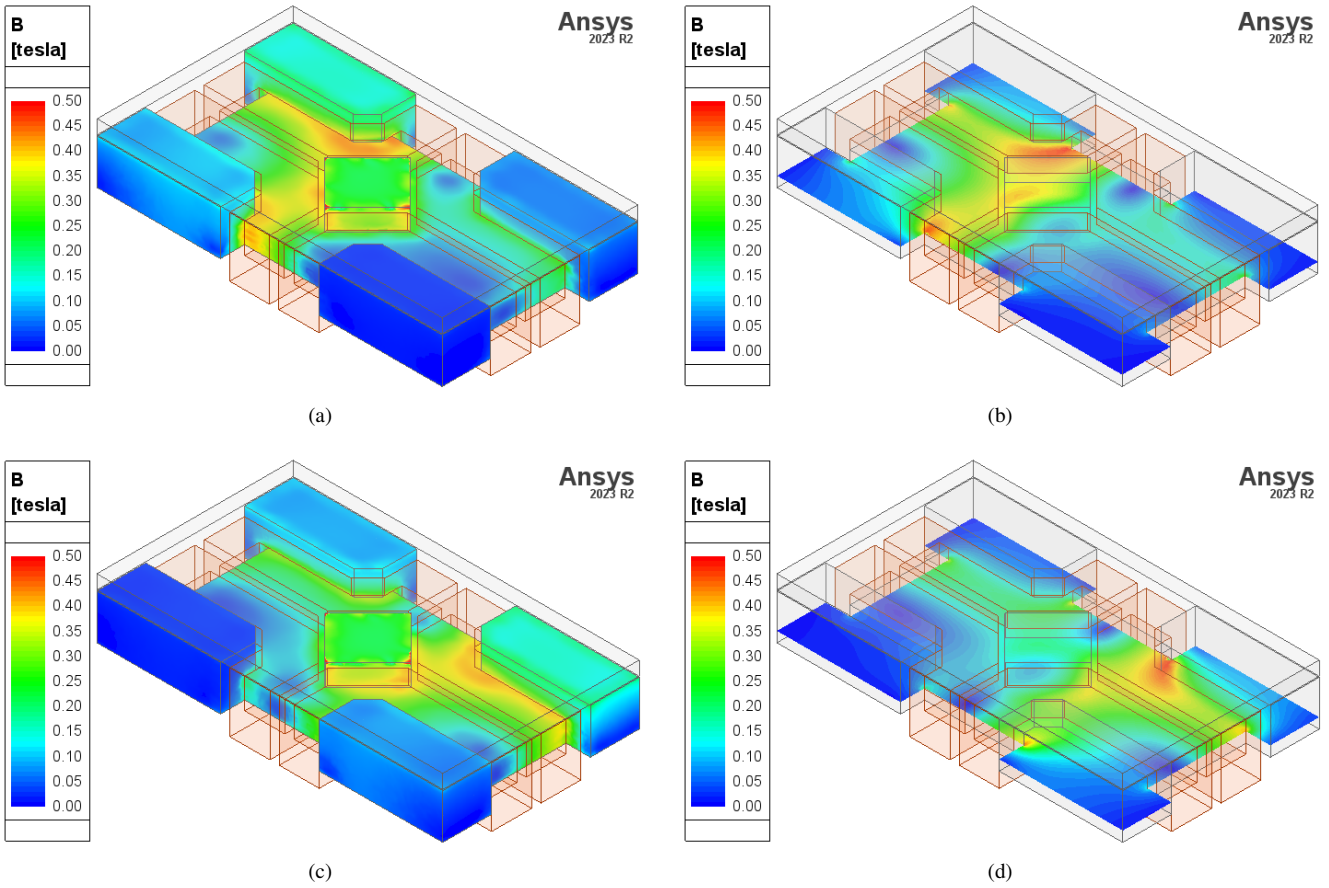

Fig. 12: Magnetic flux density distributions in the bottom core at Moments I and II, as annotated in Fig. 11, when the magnetic cores are most prone to saturation. The magnetic flux density distributions at Moments III and IV are omitted since they are identical to those at Moments I and II after being rotated by 180° around the center of the bottom core. (a) Surface flux density distribution at Moment I. (b) Cross-sectional flux density distribution at Moment I. (c) Surface flux density distribution at Moment II. (d) Cross-sectional flux density distribution at Moment II.

coupled inductor is verified by circuit and finite element method (FEM) simulations using PLECS and Ansys, respectively. Fig. 11 shows the simulation waveforms of the four-phase interleaved winding currents at the full-load conditions listed in Table III, with the directions of the winding currents illustrated in Fig. 8(a). As annotated in Fig. 11, the magnetic cores are most prone to saturation at Moments I–IV when the current in one phase reaches its peak value. Fig. 12 shows the Ansys FEM simulation results of the magnetic flux density distributions in the bottom core. Figs. 12(a) and (b) depict the surface and cross-sectional magnetic flux density distributions in the bottom core at Moment I. Since current i_1 reaches its peak at Moment I and is the highest among the four winding currents, the magnitude of the magnetic flux density around Winding 1, as annotated in Fig. 8(a), is the highest. The saturation magnetic flux density of the core material (DMR96A [44]) is 540 mT at 25 °C and 430 mT at 100 °C. As Figs. 12(a) and (b) show, only a small portion of the bottom core around Winding 1 saturates at Moment I. Similarly, Figs. 12(c) and (d) depict the magnetic flux density distributions at Moment II when i_2 reaches its peak, showing marginal saturation around Winding 2. Because of the symmetry of the core geometry, the magnetic flux density distributions at Moments III and IV, after being rotated by 180° around the center of the bottom core, are identical to those at Moments I and II. Therefore, the magnetic flux density distributions at Moments III and IV are omitted in Fig. 12. In summary, the FEM simulation results presented in Fig. 12 demonstrate that the four-phase coupled inductor is capable of handling the 37.5-A per-phase average current at the full-load conditions listed in Table III.

B. Gate Drive Circuitry

One practical implementation challenge of the proposed topology is the gate drive circuitry for the high-side switches in the SCB modules in Stage 2 (i.e., $S_{2\mathrm{HX}-10\mathrm{HX}}$, $\mathrm{X} = \mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}$). Due to a large number of high-side switches in the SCB modules, conventional cascaded bootstrapping suffers from accumulative voltage drops across bootstrap diodes, leading to higher gate drive losses and gate drive voltage mismatch along the cascaded bootstrap chain [47]. To ensure that all high-side switches can be fully enhanced, the ground-referenced power supply V_{drvH} needs to be higher than the required gate drive voltage for full enhancement, such that there remains sufficient voltage at each switch after the diode voltage drop. For switching devices that only allow a narrow range of gate drive voltage, such as GaN transistors, low-dropout (LDO) regulators are typically required to tightly

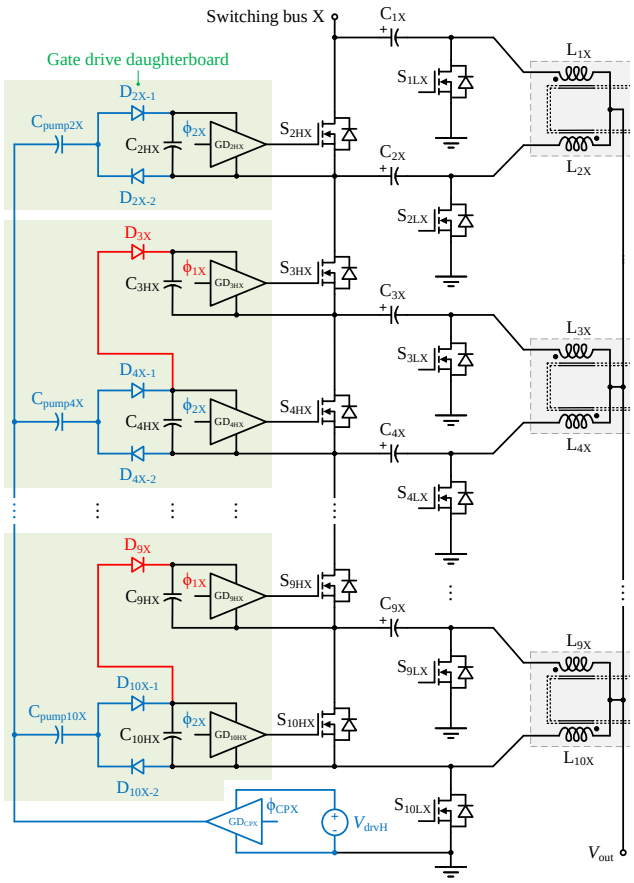

Fig. 13: Hybrid gate drive circuit customized for the high-side switches in Module X (X = A, B, C, D), where switches $S_{2HX,4HX,\cdots,10HX}$ are powered with gate-driven charge pump circuits, and switches $S_{3HX,5HX,\cdots,9HX}$ are powered with cascaded bootstrap circuits. (a) Schematic drawing. (b) Control signals.

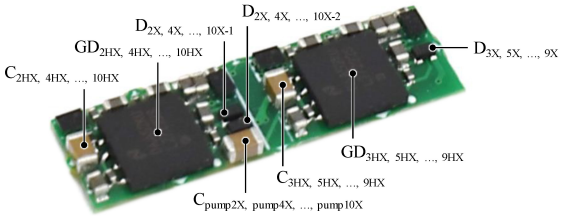

Fig. 14: Photograph of the custom gate drive daughterboard for powering the switches in Module X (X = A, B, C, D), including high-side and low-side switches. Dimensions: $18.5 \times 5.5 \times 1.0$ mm^3.

regulate the local gate drive voltage at the required level, which further increases gate drive losses and circuit complexity.

To address this challenge, this paper customized a new gate drive circuit for the proposed topology by hybridizing

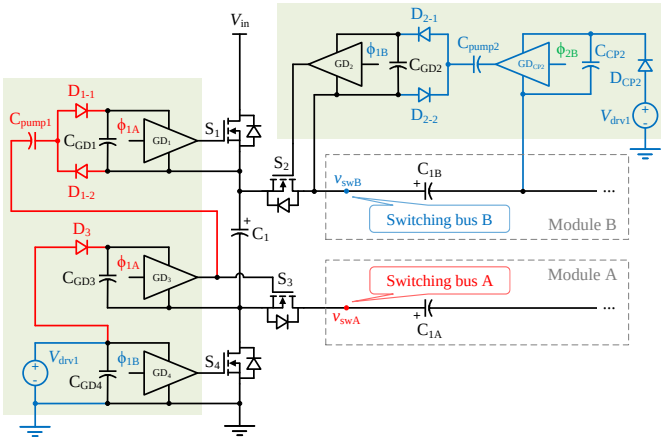

Fig. 15: Gate drive circuitry for switches S_{1-4} in Stage 1. S_1 and S_2 are powered with gate-driven charge pump circuits. S_3 is powered with cascaded bootstrapping through a low voltage-drop diode D_3. Control signals ϕ_{1A}, ϕ_{1B} and ϕ_{2B} are illustrated in Fig. 4. The gate drive circuitry for switches S_{5-8} is the same.

gate-driven charge pumps [47] and cascaded bootstrapping, as shown in Fig. 13(a). In this hybrid gate drive circuit, switches $S_{2HX,4HX,\cdots,10HX}$ are powered with gate-driven charge pump circuits, and switches $S_{3HX,5HX,\cdots,9HX}$ are powered with cascaded bootstrap circuits. Fig. 13(b) illustrates the control signals of the hybrid gate drive circuit. Charge-pump capacitors $C_{pump2X,pump4X,\cdots,pump10X}$ are charged by flying capacitors $C_{2X,4X,\cdots,10X}$ when $\phi_{CPX} = 0$, and local decoupling capacitors $C_{2HX,4HX,\cdots,10HX}$ are charged by the additional gate driver GD_{CPX} when $\phi_{CPX} = 1$. To ensure proper operation, ϕ_{CPX} must be high when $\phi_{2X} = 1$. Otherwise, charge-pump capacitors $C_{pump2X,pump4X,\cdots,pump10X}$ will be overcharged by flying capacitors $C_{1X,3X,\cdots,9X}$ through high-side switches $S_{2HX,4HX,\cdots,10HX}$ when $\phi_{2X} = 1$. Therefore, as can be seen in Fig. 13(b), the pulse width of ϕ_{CPX} is greater than that of ϕ_{2X} to ensure ϕ_{CPX} always encompasses ϕ_{2X}. This hybrid gate drive circuit was implemented as the green daughterboard presented in Fig. 14 with good modularity. In the hardware prototype presented in Figs. 6 and 7, the gate drive daughterboards were mounted on the bottom side of the red power board underneath the power MOSFETs.

Another solution to powering the high-side switches in the SCB modules is the synchronous bootstrap technique [48], which was adopted in an earlier version of the proposed topology [25]. The idea of synchronous bootstrapping is to reduce the voltage drops in the bootstrap circuit by replacing bootstrap diodes with active FETs. Though effective and widely applicable, the synchronous bootstrap circuit has a high component count when implemented with discrete components, which complicates hardware implementation and reduces overall reliability. In contrast, the proposed hybrid gate drive circuit is simpler and more robust.

Fig. 15 illustrates the gate drive circuitry for Stage 1. The high-side switches S_1, S_2, S_5 and S_6 are powered with the gate-driven charge pump circuit proposed in [47]. S_3 and S_7 are powered with cascaded bootstrapping through a low voltage-drop diode.

TABLE IV: Key parameters and test conditions of the hardware prototype

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Maximum tested output current	1500 A (37.5 A/phase)
Switching frequency	220 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	6.5 V
Low-side gate drive voltage of Stage 2	5.3 V
Prototype box volume*	1.98 in^3
Power density by box volume	759 W/in^3

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.

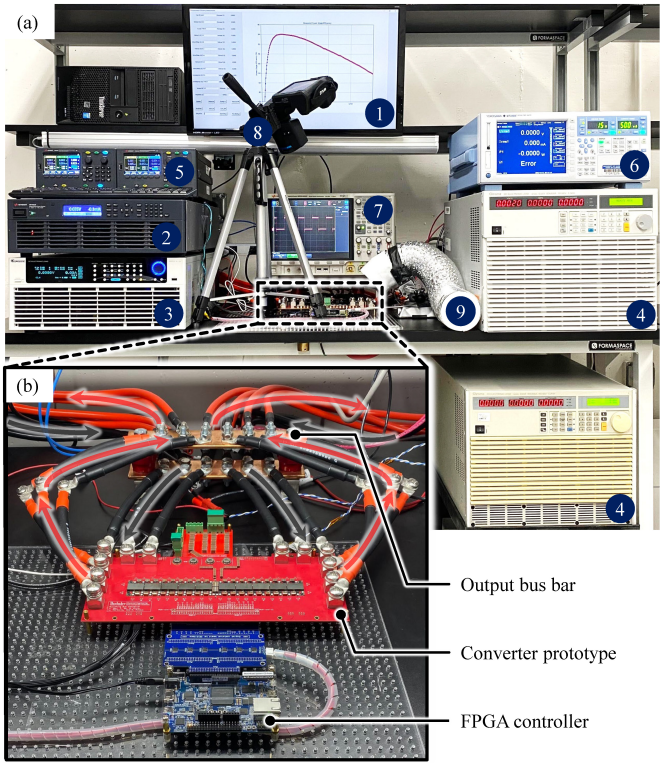

Fig. 16: Experimental setup for automated efficiency measurement with remote control of equipment. (a) Bench setup. (b) Prototype under test. List of equipment: ① Monitor for displaying measurement results. ② Keysight RP7962A regenerative power system (500 V/±40 A). ③ Chroma 63206A-60-1000 dc electronic load (60 V/1000 A). ④ Chroma 63203 dc electronic load (80 V/600 A) ×2. ⑤ Keysight E36312A triple output programmable dc power supply used to power the control and gate drive circuitry. ⑥ Yokogawa WT3000E precision power analyzer used to measure the input voltage, input current, and output voltage. ⑦ Keysight oscilloscope. ⑧ FLIR thermal camera. ⑨ Air inlet of the air cooling system.

IV. Experimental Results and Performance Comparison

To validate the functionality and performance of the proposed switching bus converter, the hardware prototype was tested with an output current of up to 1500 A for 48-V-to-1-V conversion. Table IV lists the key parameters and test conditions of the hardware prototype, with the experimental setup for automated efficiency measurement shown in Fig. 16. A 1000-A Chroma 63206A-60-1000 dc electronic load and two 600-A Chroma 63203 dc electronic loads were used to sink the ultra-high output current of the converter. The input voltage, input current, and output voltage were measured with a high-precision Yokogawa WT3000E power analyzer. The output current was measured by the dc electronic loads. A FLIR thermal camera was used to monitor the surface temperature of the prototype.

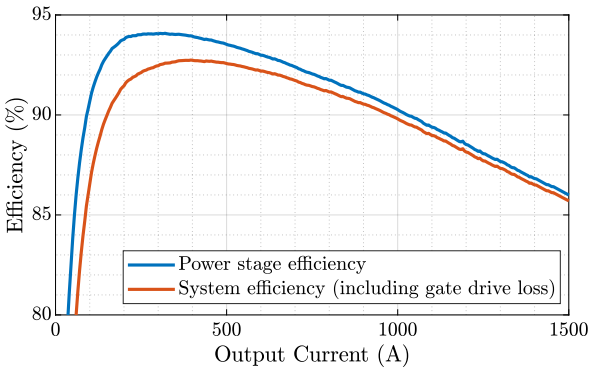

Fig. 17: Measured 48-V-to-1-V efficiency. Peak efficiency: 94.1% at $I_{\text{out}} = 320$ A (92.7% at $I_{\text{out}} = 395$ A including gate drive loss). Heavy-load efficiency: 87.7% (87.3% including gate drive loss) at $I_{\text{out}} = 1300$ A. Full-load efficiency: 86.0% (85.7% including gate drive loss) at $I_{\text{out}} = 1500$ A.

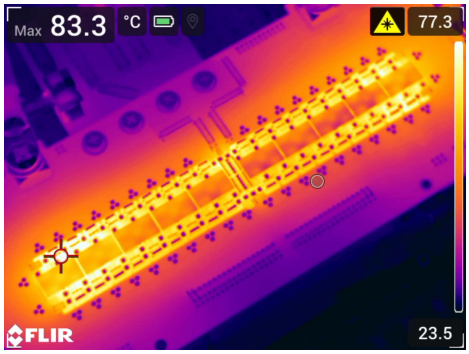

Fig. 18: Thermal image at equilibrium with air cooling only ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 1300$ A). The air blew from the top-right corner of this thermal image to the bottom-left corner.

A. Measured Performance

Fig. 17 presents the measured efficiency from the hardware prototype for 48-V-to-1-V conversion. It achieved a peak power stage efficiency of 94.1% at 320-A output current, a heavy-load power stage efficiency of 87.7% at 1300-A output current, and a full-load power stage efficiency of 86.0% at 1500-A output current. With gate drive loss included, it achieved 92.7% peak system efficiency at 395-A output current, 87.3% heavy-load system efficiency at 1300-A output current, and 85.7% full-load system efficiency. At 1500-A output current, the hardware prototype achieved a power density of 759 W/in^3 by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry).

Fig. 18 shows the thermal image of the prototype running continuously at an output current of 1300 A with air cooling only. It should be noted that the current hardware prototype does not incorporate any heat sink, heat spreader, or any other type of thermal management system. For continuous operation above 1300 A and converter temperature below 85 °C, either

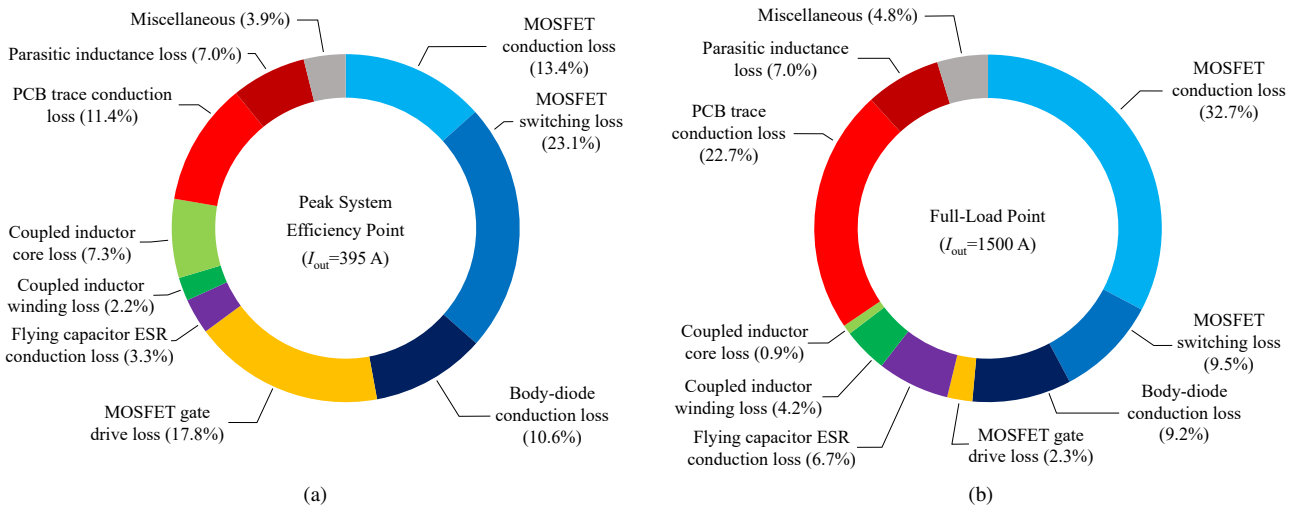

Fig. 19: Loss breakdown of the hardware prototype. (a) Loss breakdown at the peak system efficiency point. (b) Loss breakdown at the full-load point.

improved heat-sinking in air-cooled systems, or incorporation of liquid-cooling technology is needed. For example, a custom cold plate can be designed for the prototype utilizing the space above the switches between the flying capacitors and coupled inductors and leveraging the dual-side cooling package of the power MOSFETs.

It is worth noting that the theoretical high-performance potential of the proposed topology illustrated in Fig. 5 hasn't been fully realized in this hardware prototype. Although the voltage stresses on the high-side switches (i.e., S_{2HX}–S_{10HX} [X = A, B, C, D]) and low-side switches (i.e., S_{1LX}–S_{10LX} [X = A, B, C, D]) in Stage 2 are only 4.8 V and 2.4 V, respectively, the best switching devices available on the market for this application when the prototype was built are rated at 25 V (Infineon IQE006NE2LM5 and IQE006NE2LM5CG). If implemented with lower voltage devices with lower $R_{ds(on)}$ and smaller C_{oss}, this prototype would be able to achieve better performance. Currently, there are already 15-V MOSFETs in dual-side cooling packages (Infineon IQE004NE1LM7SC and IQE004NE1LM7CGSC) with both better electrical characteristics and higher thermal performance. With the advancement of device technologies, the theoretical potential of the proposed topology can be further unleashed in the future.

B. Loss Analysis

Fig. 19 presents a comprehensive loss breakdown of the hardware prototype at both the peak system efficiency point and full-load point. This loss analysis was conducted to offer a deeper understanding of the sources of power losses in the prototype and to identify potential avenues for performance improvement. The MOSFET conduction loss was simulated with the measured duty ratio at the corresponding output current and with the ON-resistance ($R_{ds(on)}$) provided by the datasheets. The MOSFET switching loss incorporates the C_{oss} loss and the overlap loss, estimated with the datasheet parameters. The coupled inductor core loss was simulated with an electric-thermal co-simulation in ANSYS. The PCB trace resistance and parasitic commutation loop inductance were estimated with finite element analysis (FEA) using ANSYS.

At the peak system efficiency point, frequency-dependent losses—including MOSFET switching loss, body-diode conduction loss, MOSFET gate drive loss, coupled inductor core loss, and parasitic inductance loss—predominate the total loss. Conversely, conduction losses such as MOSFET conduction loss, body-diode conduction loss, flying capacitor ESR conduction loss, coupled inductor winding loss, and PCB trace conduction loss become more dominant at the full-load point.

C. Performance Comparison with the State of the Art

Tables V and VI compare the performance of this work to that of the state-of-the-art 48-V-to-1-V academic works and commercial products, respectively. Compared to existing solutions, this laboratory prototype achieved the highest output current with outstanding efficiency and power density, even when benchmarked against highly optimized commercial power modules with advanced packaging.

Fig. 20 visually illustrates the system performance of the state-of-the-art 48-V-to-1-V academic hybrid SC works and commercial products that report their measured system efficiencies (including gate drive loss). The performance of each solution is visually represented by two dots: the bottom-right dot denotes the performance at the peak system efficiency point, and the top-left dot denotes the performance at the full-load point. Solid dots represent the performance of academic works, while hollow dots correspond to the performance of commercial products. As can be seen in Fig. 20, this prototype pushes the performance limit toward the upper right corner, which represents higher efficiency and higher power density.

V. Conclusion

This paper introduces an ultra-high-current 48-V-to-1-V switching bus converter with a single-stage VPD architecture for next-generation processors. The proposed topology merges two 2-to-1 SC front-ends with four 10-branch SCB modules

TABLE V: Performance comparison between this work and the state-of-the-art 48-V-to-1-V academic works

Year	Reference	Output Current	Operating Frequency*	Power Density**	Power Stage Efficiency	System Efficiency†
2024	This work	1500 A (37.5 A/phase)	220 kHz	759 W/in^3 (by box volume)	Peak efficiency: 94.1% Heavy-load efficiency: 87.7% Full-load efficiency: 86.0%	92.7% 87.3% 85.7%
2024	16-to-1 SBC [23]	500 A (31.3 A/phase)	150 kHz	464 W/in^3 (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2024	Mini-LEGO [22]	240 A (20 A/phase)	1.5 MHz	1390 W/in^3 (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2024	SDIH [21]	105 A (52.5 A/phase)	750 kHz	598 W/in^3 (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2023	MSC [24]	450 A (28.1 A/phase)	400 kHz	621 W/in^3 (by box volume)	Peak efficiency: 93.1% Full-load efficiency: 86.2%	91.7% 85.8%
2022	Dickson^2 [19]	270 A (30 A/phase)	280 kHz	360 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [18]	450 A (28.1 A/phase)	417 kHz	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [17]	60 A (30 A/phase)	250 kHz	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [15]	450 A (37.5 A/phase)	1 MHz	294 W/in^3 (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [10]	40 A (20 A/phase)	125 kHz	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%‡ Full-load efficiency: 92.7%‡	N/A N/A
2020	Sigma [7]	80 A	1 MHz	420 W/in^3 (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

* Switching frequency of the voltage regulation stage.
** The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.
† Gate drive loss is included in the calculation of system efficiency. ‡According to direct correspondence with the author.

TABLE VI: Performance comparison between this work and existing 48-V-to-1-V commercial products

Release Year	Reference	Output Current	Operating frequency*	Power Density**	System Efficiency†
2024	This work	1500 A	220 kHz	759 W/in^3	Peak: 92.7%, Full-load: 85.7%
2021	Analog Devices LTM4664 [49]	50 A	350 kHz	415 W/in^3	Peak: 90.8%, Full-load: 88.0%
2019	Flex Power Modules BMR482 (satellite) [50]	110 A	600 kHz	306 W/in^3	Peak: 92.1%, Full-load: 87.4%
2018	Bel Power Solutions ST4-1V0M07G [51]	70 A	450 kHz	167 W/in^3	Peak: 91.5%, Full-load: 90.5%
2016	Texas Instruments LMG5200POLEVM-10 [52]	50 A	600 kHz	N/A	Peak: 90.7%, Full-load: 87.6%
2012 2015	Vicor PRM48AF480T400A00 [53] +2×VTM48EF012T130C01 [54]‡	200 A	1.03 MHz 1.20 MHz	236 W/in^3	Total efficiency: 89.7%‡

* Switching frequency of the voltage regulation stage.
† Gate drive loss is included in the calculation of system efficiency.
**Power density calculated by the box volume.
‡Recommended and provided by Vicor's online Power System Designer.

through four switching buses, achieving a very large SC stage conversion ratio of 20-to-1. In contrast to the existing dc-bus-based architecture, the proposed switching-bus-based architecture eliminates the need for dc bus capacitors, reduces the switch count, and guarantees complete soft-charging operation. Furthermore, a topological comparison reveals that the proposed topology, when compared to existing 48-V-to-1-V hybrid SC demonstrations, achieves the lowest normalized switch stress and the smallest normalized passive component volume with the largest SC stage conversion ratio compared to existing 48-V-to-1-V hybrid SC demonstrations. This suggests that the proposed topology holds great promise for simultaneously achieving higher efficiency and power density than prior hybrid SC solutions.

To validate the theoretical potential of the proposed topology, a hardware prototype with good modularity and extendability was designed and constructed with customized coupled magnetics and gate drive circuitry. A four-phase coupled inductor was optimized for a good trade-off between size and transient performance, with the range of duty ratio taken into consideration. In addition, an efficient, simple, and robust hybrid gate drive circuit was designed to overcome the accumulative diode voltage drops of conventional cascaded bootstrapping. This hybrid gate drive circuit powered the high-

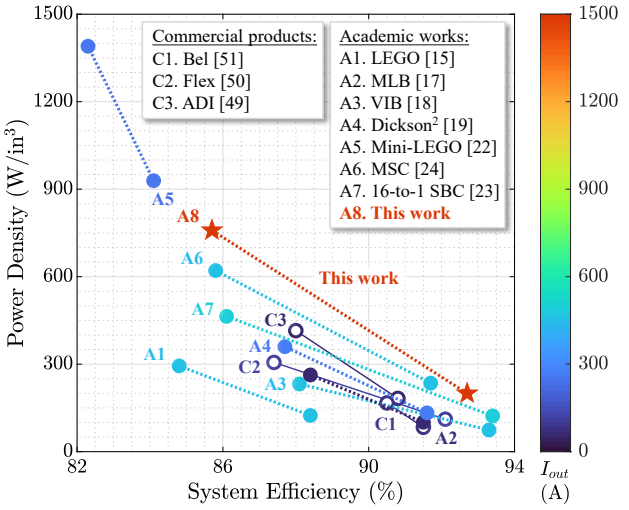

Fig. 20: Performance comparison between this work and the state-of-the-art 48-V-to-1-V academic hybrid SC works and commercial products. The performance of each solution is visually represented by two dots, with the bottom-right dot denoting the performance at the peak system efficiency point and the top-left dot denoting the performance at the full-load point. The system performances of academic works and commercial products are illustrated with solid and hollow dots, respectively.

side switches in the SCB modules and was implemented as modular gate drive daughterboards.

The hardware prototype was tested up to 1500-A output current for 48-V-to-1-V conversion and achieved 92.7% peak system efficiency, 85.7% full-load system efficiency (including gate drive loss), and 759 W/in^3 power density (by box volume) without any heat sink and with air cooling only. The outstanding performance of this laboratory prototype pushes the performance limit of the state-of-the-art 48-V-to-1-V solutions, including academic works and commercial products, towards higher efficiency and higher power density.

VI. Acknowledgement

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