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SPARK GAP TRIGGER AMPLIFIER WITH 1-msec RECOVERY TIME

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SPARK GAP TRIGGER AMPLIFIER WITH 1-msec RECOVERY TIME

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ABSTRACT

A spark-gap trigger amplifier with 1-msec recovery time has been developed for experiments using spark chambers with fast recovery time. The system utilizes a spark gap operating under the ambient pressure as the high-current fast switching element, and is entirely self-contained. The system is capable of operating at 1 kHz for 1 sec burst, or 400 Hz continuously.

INTRODUCTION

Advances in the state of the art of spark chamber design, such as wire spark chambers and low-energy chambers, have reduced the recovery time of the chambers to 1 msec. A spark chamber usually is driven by an energy-storage element, often a capacitor, and a high-current switch, often a spark gap or in some cases a hydrogen thyratron. To trigger a spark gap a trigger pulse of a few kV is needed. To preserve the efficiency of the spark chambers, a short delay between the scintillator and the output of the pulse amplifier, is required. Since spark chambers have been operated with 1 msec dead time, a compatible pulse amplifier is needed to complete the chain of operation.

DESIGN OBJECTIVES

Since the previous spark-gap trigger amplifier[1] has been operating very successfully and serving its purposes well, the design criteria have been generally the same. However, the following objectives have been added:

a. Dead time of 1 msec between pulses.

b. A protective system to prevent almost all damage that might be caused inadvertently.

c. A system for recharging the spark gap in 20 μsec or less.

d. A spark gap that requires the least time to recover with the least amount of air flushing.

e. Output energy per pulse of 100 mJ or more.

f. The possibility of future increase energy by a factor of 2.

SEQUENCE OF OPERATION

Figure 1 is a block diagram of the entire system. The main amplifier consists of the preamplifier and the spark gap. A −0.5-V trigger pulse goes into the trigger input of the preamplifier; 19 nsec later a −8-kV pulse goes to the trigger electrode of the spark gap. Another 16 nsec later, the megawatt output pulse appears across the output connectors. Part of the output energy is used to trigger the timing circuit, which provides the preset dead time of 1 msec, 2.5 msec, or 10 msec, after which driving pulses are fed to the SCR charging circuit, recharging the spark gap so that it is ready for another cycle of operation. The protective circuit keeps count of the pulsing rate of the spark gap as well as the dry-air flushing pressure to determine whether operation of the system is within safe limit. The rest of the blocks are power supplies of the system.

THE PREAMPLIFIER

The trigger amplifier shown in Fig. 2 employs one avalanche transistor, four silicon-controlled rectifiers (SCR's), and one planar triode to amplify the −0.50-V trigger pulse to a −8-kV pulse to trigger the spark gap which is the final stage of the amplifier.

One selected avalanche transistor (Motorola type 2N2222) is used as the input stage. The transistor is selected to run safely at 1 mA bias. Operating bias current is 300 μA. The delay of this stage is about 2 nsec. The amplified output pulse amplitude is approximately 200 V, with a rise time of about 1 nsec.

A 10:1 transformer is used to couple the amplified trigger signal to the following SCR stage. The transformer provides four separate

windings driving the four SCR's, which are connected in series. Four 1-MΩ resistors are used to form a voltage-equalizing network for the SCR string to insure that each SCR has the same voltage across it; 500 V is applied across the SCR string. The delay of this stage is less than 7 nsec, and the rise time, driving the cathode of the ML8538, is 10 nsec. The SCR's were selected with the system described in the appendix.

A Machlett-type ML8538 is used in this stage. The grid is grounded to provide shielding from the spark gap. The cathode is connected to the anode of the first SCR through a dc decoupling capacitor. When the SCR string is turned on, a negative pulse is imposed across the cathode and ground, making the tube turn on. The plate voltage falls by 10% to 90% in about 10 nsec, driving the corona lamp and trigger electrode of the spark gap.

After more than 10^8 pulses, the leakage current of the tube has increased from a few μA to 100 μA. The leakage current across the tube (with the filament off) is a good measure of the condition of the tube. The 10^8 pulses were obtained by pulsing the tube at 400 Hz, 1 sec on and 1 sec off, driving the spark gap, with 8 kV anode voltage on the tube. It was found that, operated at 10 kV, the tube lasted only for approximately 10^6 pulses. The life of a tube for this application is considered to reach the end when the power dissipation of the tube exceeds 4 W. With a plate load resistor of 2 MΩ, this means an 800-V drop (10%) in anode voltage. The increase in leakage current is believed to be due to the sputtering of cathode material onto the internal structure of the tube every time it is pulsed.

SPARK GAP

The spark gap used in this pulser has a positive and a negative electrode, and the trigger electrode is located midway between the two main electrodes. The trigger electrode normally is grounded through the 20-kΩ resistor. When the negative 8-kV pulse pulls the trigger electrode down to a negative potential, the positive electrode arcs over to the trigger electrode, pulling it up to positive 5 kV; it then arcs over to the negative 5kkV electrode, completing the circuits. The operating dc potential is 10 kV; however, the two storage capacitors do lose their charges when the spark gap is closing and the spark gap, just like any other switch, has it resistance. As a result the peak amplitude of the output pulse is approximately 8 kV, with R_L equal to 50 Ω. A plot of output pulse amplitude vs load resistance is given in Fig. 3.

The corona lamp is aimed at the trigger electrode, and photons are emitted from the corona lamp when it fires at about 1 kV. Photoelectrons are knocked off from the potentially negative-going trigger electrode, and then an avalanche of electrons follows, bridging the trigger electrode and the positive electrode, and hence the negative electrode. This process helps the spark gap to break down with shorter delay and jitter time.[1]

The main electrode of the spark gap are shaped like bullets with the round end faced down to a flat tip. The trigger electrode is like a screwdriver with the tapered end flattened out and grooved on the sides. See Fig. 4 for detail. The grooves on the trigger electrode have no effect on the spark gap operation; however, the sharp edges of the grooves ensure that sparks will jump across the surface area of the electrodes evenly, thus avoiding hot spots due to minor misalignment of the spark gap. The

flat surfaces of the main electrodes are used to provide more conducting area than a round electrode, thus helping to prolong the life of the spark gap. Under a 1-sec on, 2-sec off 400-Hz burst operating condition, the rise time of the output pulse increased to 20 nsec after 10^8 pulses. The gap spacing and the dead time required under various conditions are given on Table 1.

The operating repetition rate and the off time in between bursts have effects on the life of the spark gap. At lower repetition rates and longer pauses between bursts, the electrodes have more time to cool off, hence a longer life of the spark gap can be expected.

The air flushing has three functions. It carries the particles away from the spark gap area, helps to cool off the electrodes faster, and helps to expel ozone from the spark gap chamber. The spark gap, with air flushing, operating at less than 10 pulses per second, is expected to last beyond 10^9 pulses.

The spark gap is entirely enclosed in a gastight chamber (see Fig. 5). Air flushing is provided by one inlet and two outlets. The small hole at the end of the inlet tubing creates a jet-action air stream blowing at the spark gap. The high-speed air stream is quite effective in deionizing the gap.

The spark gap chamber can be regarded as hydrogen safe, because of the slightly pressurized atmosphere inside the chamber and because of its gastight characteristic.

A 250-Ω load is built into the chamber. Thus without any external load, the output pulse has a decay-time constant of 625 nsec. The 250-Ω load is made out of eight resistor strings all connected in parallel.

After the spark gap has been triggered, part of the output signal is picked off from the internal resistance load and fed to a delay circuit. Either 10 msec, 2.5 msec, or 1 msec afterwards (depending on the dead-time setting) the spark gap is charged up again and ready for another cycle. The time between the initial trigger pulse at the input of the pre-amplifier and the output pulse at the output connectors is approximately 35 nsec. Figure 6 shows the time relation of the trigger and output pulses.

TIMING AND SCR DRIVING CIRCUIT

The trigger pulse picked off from the spark gap is a negative pulse, hence an inverting transformer is used to provide a positive pulse to trigger the timing circuit. A one-shot multivibrator is used to delay the trigger signal for the dead time selected, which then triggers another one-shot multivibrator, providing a 10-μsec pulse which is amplified and fed to SCR_1 through a 2:1 stepdown transformer. The delayed trigger signal is also used to trigger another one-shot multivibrator which provides a further 40-μsec delay for the trigger signal, which then triggers a one-shot multivibrator providing a 10-μsec pulse that is amplified and fed to SCR_2 through a 2:1 stepdown transformer. The amplitude of the pulses driving into the SCR's is 6 V. The positive 20-V supply to this circuit goes through the pressure switch. For the 1-msec and 2.5-msec dead-time setting air pressure has to be present to activate the switch connecting the 20-V supply to this circuit. The operating current for this circuit is approximately 100 mA. See Fig. 7.

CHARGING CIRCUIT

Two SCR's are used as two switches in this circuit (see Fig. 8). The first SCR is connected between the dc power supply and a choke that is connected in series with the capacitor, C.

When the driving signal from the timing circuit goes to SCR_1, the SCR turns on and begins to charge up C. By the end of this charging phase, the voltage across C is twice that of the dc power supply, hence SCR_1, being back-biased, turns off. The time required to charge up C_1 is given by the expression $t = \pi\sqrt{LC_1}$. The period of this cycle has been chosen to fall into the best operating region of the SCR used. The peak current through SCR_1 is about 105 A_1, with L approximately 7 μH; the half-sine-wave current pulse has a base width of 30 μsec. However, 40 μsec is assigned to the first charging period, Forty μsec after SCR_1 is turned on, SCR_2 is activated, discharging C_1 into the primary of the resonant charging transformer, T_2, which steps up the 200-V pulse to ±5 kV across the two 5000-pF capacitors on each side of the spark gap. The ±5 kV is kept constant by means of the trickle-charge power supplies derived from the Cockcroft-Walton voltage multiplier.

The ±5-kV pulses go through two diode strings to charge up the two 5000-pF capacitors. The leakage currents of these two diode strings must be kept low to avoid voltage sagging in low-repetition-rate pulsing. Unitrode's USR 15 has been found to have an average leakage current of 70×10^{-9} A at 40° C and 1.7×10^{-6} A at 60° C at the rated piv. With its fast recovery time, typically 200 nsec, it is satisfactory for this purpose. Figure 9 shows the ±5-kV charging waveform across the two 5000-pF capacitors.

THE RESONANT CHARGING CAPACITOR

The 11-μF capacitor, C_1, undergoes two pulsings during each charging cycle. When SCR_1 is turned on, the capacitor is charged up to 200 V in 30 μsec with a current pulse of 105 A peak. When SCR_2 is turned on, discharging the capacitor into the transformer, the fall time is 16 μsec, with a current pulse of 230 A peak. Under such pulsing conditions, a Mylar film capacitor with dc voltage rating of 400 to 600 V is fairly susceptible to damage. To make sure this capacitor will operate reliably for more than 10^9 pulses and beyond, a Maxwell-type 30024 H. V. oil-impregnated Mylar pulse capacitor is used at a greatly derated voltage level. The capacitor has been pulsed at 270 V, 220 A and at 400 V, 110 A for more than 10^9 pulses, with rise and fall times at 20 μsec and 60 μsec respectively, without any sign of failure. The temperature rise of the capacitor case is approximately 8° C at the end of the 1-kHz, 1-sec-on–1-sec-off pulsing tests.

THE RESONANT CHARGING TRANSFORMER

To acquire low leakage inductance and high breakdown voltage characteristic, the charging transformer is tape wound. The maximum flux swing of the core is utilized without flux resetting. The efficiency of the transformer is 50%. The contradictory requirements of function and cost have been compromised in the construction of the transformer. Figure 10 is a photograph of the transformer.

OVERLOAD PROTECTION CIRCUIT

In the experimental field, there is always the possibility of wrong connections during the setup. Since the unit is a closed-loop system, it may recycle at the highest possible frequency and burn itself up. Also a continuous high-frequency pulse train might be fed into the unit by mistake, and damage the system. To insure against these possibilities, two protective circuits are built into the system; see Fig. 11.

A pressure switch is used to make sure that 7 psi of air is present before the system responds to triggering at the 1-msec and 2.5-msec dead-time settings. If during the operation the air pressure drops below 3 psi, the system shuts itself off. No air, however, is required at 10-msec dead-time setting. The pressure switch controls the supply voltages to the SCR driver and the avalanche transistor stage. This guards against external high frequency triggering and internal recycling without air flushing at the two shorter dead-time settings.

To guard against continuous high-frequency triggering at the 1-msec dead-time setting with the presence of air flushing, a one-shot multivibrator is used to count the pulses; if the number exceeds 2000 over a period of 2 sec, the voltage going to the avalanche transistor stage is cut off. Resetting is necessary in this case.

THE POWER SOURCE

Figure 12 is the circuit diagram of the main power source.

Two in-line filters are used at the input of the 117-V power line to keep transient pulses from going through either way. The line voltage is in series with the bridge rectifier to prevent surge current from

damaging the diodes when the system is turned on. A triac connected in parallel with the 22-Ω resistor is turned on 200 msec after the main switch is activated, by-passing the 22-Ω resistor. The driving signal of the triac is supplied by the 100-kHz chopper.

A series regulator is used to supply 110 V dc to the 100-kHz dc-to-dc inverter. The line regulation of the supply is less than 4% in the 100-V to 130-V range, and the load regulation is less than 2% in the 1-A to 3-A load current range. The regulator is short-circuit protected. The tripping circuit shuts off the regulator at an average load current exceeding 7 A. The sensing circuit, however, is insensitive to pulse current as high as 130 A having a cycle compatible with that of the charging period in this system.

100-kHz INVERTER

An oscillator operating on 36 V dc is used to drive two high-voltage transistors which chop up the 110-V dc supply at 100 kHz. Various windings on the secondary of the chopper transformer provide 6.3 V to the filament of the ML8538, 20 V to the timing and driving circuit, 500 V to the trigger pulser, and 1000 V peak-to-peak to the Cockcroft-Walton voltage multiplier. All rectifier diodes are of the fast-recovery type. The idling current of the inverter is approximately 130 mA. With all standby loading connected, the current goes up to 300 mA. See Fig. 13.

COCKCROFT-WALTON VOLTAGE MULTIPLIER

This stage supplies ±5 kV for the trickle charge for the spark gap and +8 kV for the anode of the ML8538. Two 0.1-μF 600-V Mylar

capacitors are connected in series to form a 1200-V capacitor with two 22-MΩ resistors connected in parallel with the capacitors as a voltage bleeder. The diodes used have a typical recovery time of 200 nsec. The regulation of the voltage multiplier is approximately 4% with a load current of 1 mA. The efficiency of the multiplier is estimated to be 70%. Figure 14 is the circuit diagram of the voltage multiplier.

ACKNOWLEDGMENT

The author thanks Q. A. Kerns and Robert F. Tusting for their direction in the earlier development of the system, D. A. Mack and Dr. B. Leskovar for their support and discussion of the project, Eric Young and R. A. Walton for their technical and mechanical assistance.

APPENDIX

The four SCR's used in the preamplifier were selected with the system described below, as shown in Fig. 15.

DELAY AND RISE-TIME MEASUREMENT

A sampling scope (Tektronix 567) was used. The extra 2-ft cable monitoring the trigger input was used to offset the 3-nsec delay time plus rise time of the avalanche transistor stage. With the test setup, the driving current into the gate of the SCR was approximately 1 A, the delay was less than 8 nsec, and the rise time was less than 10 nsec. The peak output pulse amplitude was approximately 80 V, indicating an output current pulse of 8 A. R was set at the maximum resistance position. E_s was set at 130 V. Any unit not falling within 10% of the above figures should be rejected.

FORWARD BLOCKING VOLTAGE MEASUREMENT

With R set at the maximum resistance position, E_s was increased until the current meter made an abrupt jump upward. With E_s back down to the level reached just prior to the breakdown, the voltage across the SCR was measured and designated as the forward blocking voltage. No external triggering was used in this measurement. It was found that most of the SCR's tested under the foregoing conditions had a forward blocking voltage from 130 to 145-V. Units with forward blocking voltage below 130 V should be rejected for this particular application. With 100 V (the manufacturer's rated V_{Fx}) across the SCR's, the leakage current is about 25 μA for most of the devices. With the maximum standoff

voltage across the SCR, the leakage current was in the range of 32 to 37 μA.

HOLDING CURRENT MEASUREMENT

With E_s set at the previously measured forward blocking voltage and the SCR pulsed at 100 Hz, R was gradually decreased from its maximum resistance position until the current meter jumped up to a certain reading and stayed there; this indicated the SCR was being held conducting. This current was recorded for each SCR and designated as the holding current, which has been found to be around 35 to 45 mA. The manufacturer's rated maximum holding current, I_{Hx}, is 5 mA, with a gate-to-cathode resistance of 1 kΩ. But in this case the gate-to-cathode dc resistance is close to zero, which accounts for the difference. It actually works out better for this application because the devices are expected to unlatch and recover after each pulsing.

REFERENCES

1. Quentin A. Kerns and Harold W. Miller, Spark Gap Trigger Amplifier, IEEE Trans. Nucl. Sci. NS-12[1], pp. 391-399 (1965).

2. G. N. Glasoe and J. V. Lebacoz, Pulse Generator (McGraw-Hill Book Company, New York 1948).

Table I. Various operating conditions of the spark gap.

Note: Spark gap in open air; energy per pulse = 120 mJ; dc operating voltage = 10 kV; resistive load = 50 Ω.

Spark gap spacing (d)[b]	Pulsing frequency (Hz), 1-sec burst	Dry air flushing (ft^3/h)	Output pulse rise time (nsec)	Dead time (msec)
0.075	800	0	20	1
0.070	100	0	15	1
0.070	400	0	15	2.5
0.065	400	0	10	2.5
0.065	100	0	10	10
0.065[a]	1000	5	10	1
0.065[a]	400	2	10	2.5
0.065[a]	100	0	10	10

a. Spark gap in enclosed chamber.

b. (d) in inch. See Fig. 4.

FIGURE CAPTIONS

Fig. 1. Block diagram of the spark-gap trigger amplifier.

Fig. 2. Schematic diagram of the preamplifier and the spark gap.

Fig. 3. Output pulse amplitude as a function of load resistance.

Fig. 4. The spark gap.

Fig. 5. Spark-gap chamber.

Fig. 6. Upper trace: trigger pulse input;
lower trace: output pulse.

Fig. 7. Timing circuit and SCR driving circuit.

Fig. 8. Resonant charging circuit.

Fig. 9. ±5 kV Charging voltage waveform across the 5000-pF capacitors.

Fig. 10. Resonant charging transformer.

Fig. 11. Schematic diagram of overload-protection circuit.

Fig. 12. Schematic diagram of the dc power supply.

Fig. 13. Schematic diagram of the 100-kHz inverter.

Fig. 14. Schematic diagram of the Cockcroft-Walton voltage multiplier.

Fig. 15. Schematic diagram of the SCR test set up.

Fig. 16. The 1 msec recovery time spark gap trigger amplifier.

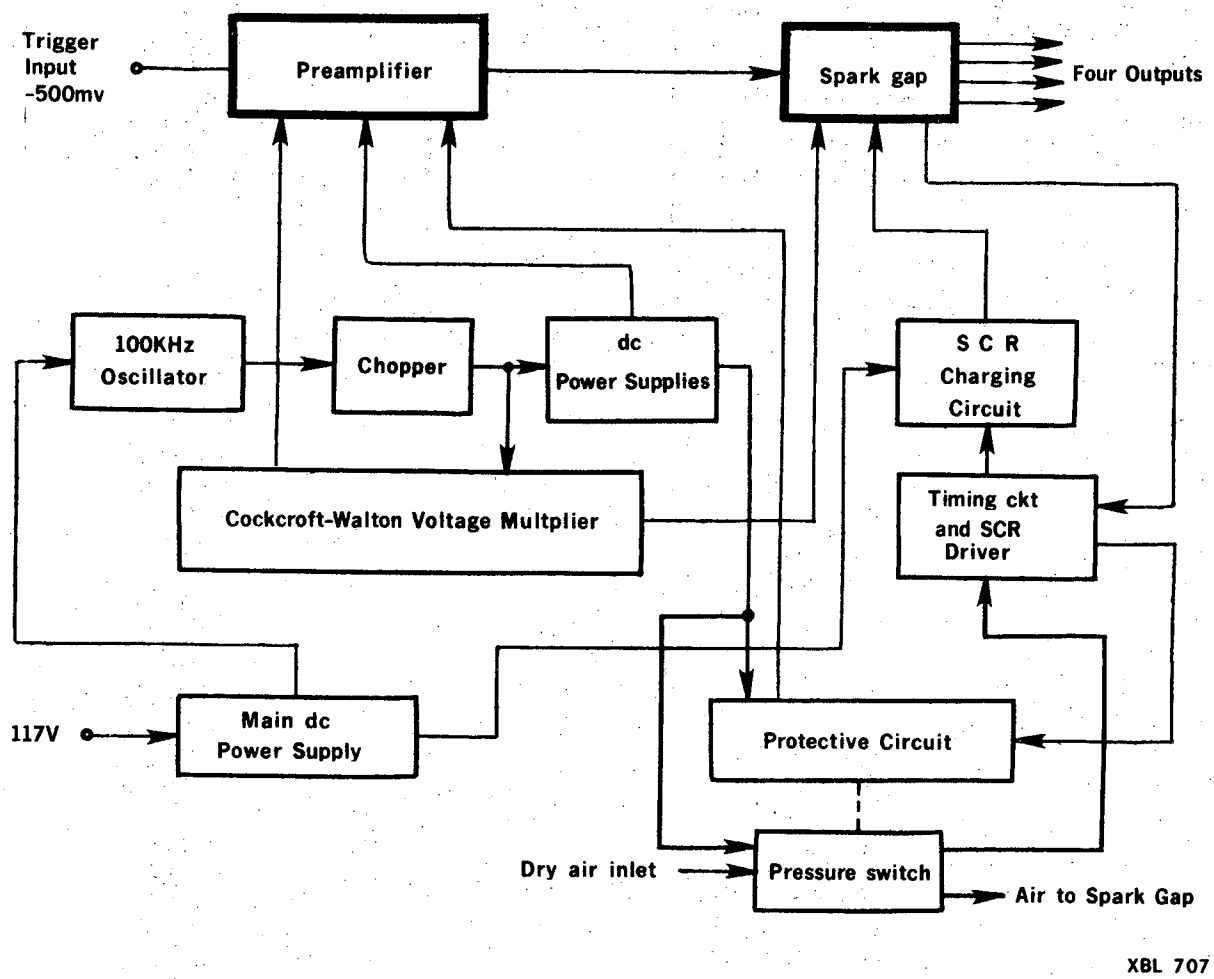

Trigger
Input
-500mv
Preamplifier
Spark gap
Four Outputs
100KHz
Oscillator
Chopper
dc
Power Supplies
S C R
Charging
Circuit
Cockcroft-Walton Voltage Multplier
Timing ckt
and SCR
Driver
117V
Main dc
Power Supply
Protective Circuit
Dry air inlet
Pressure switch
Air to Spark Gap
XBL 707 1548

Fig. 1

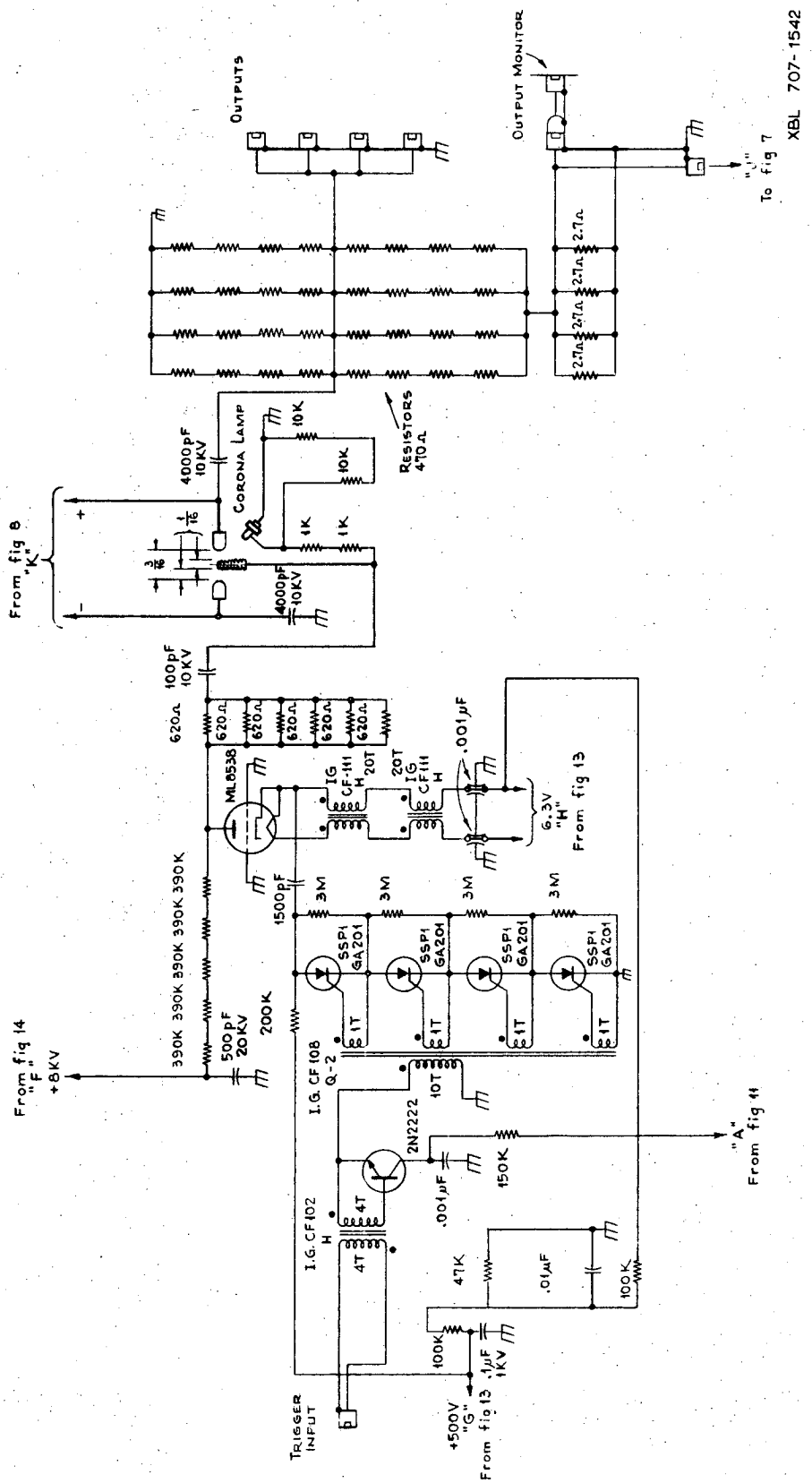

OUTPUTS
OUTPUT MONITOR
"J"
To fig 7
XBL 707-1542
2.7Ω
RESISTORS 470Ω
10K
4000pF 10KV
CORONA LAMP
1K
From fig 8 "K"
100pF 10KV
620Ω
ML8538
IG CF-111 H 20T
.001μF
6.3V "H" From fig 13
1500pF
3M
SSP1 GA201
1T
390K 390K 390K 390K 390K
500pF 20KV
200K
From fig 14 "F" +8KV
I.G. CF108 Q-2
10T
2N2222
150K
"A" From fig 11
I.G. CF102 H
4T
47K
.01μF
100K
.1μF 1KV
TRIGGER INPUT
+500V "G" From fig 13

Fig. 2

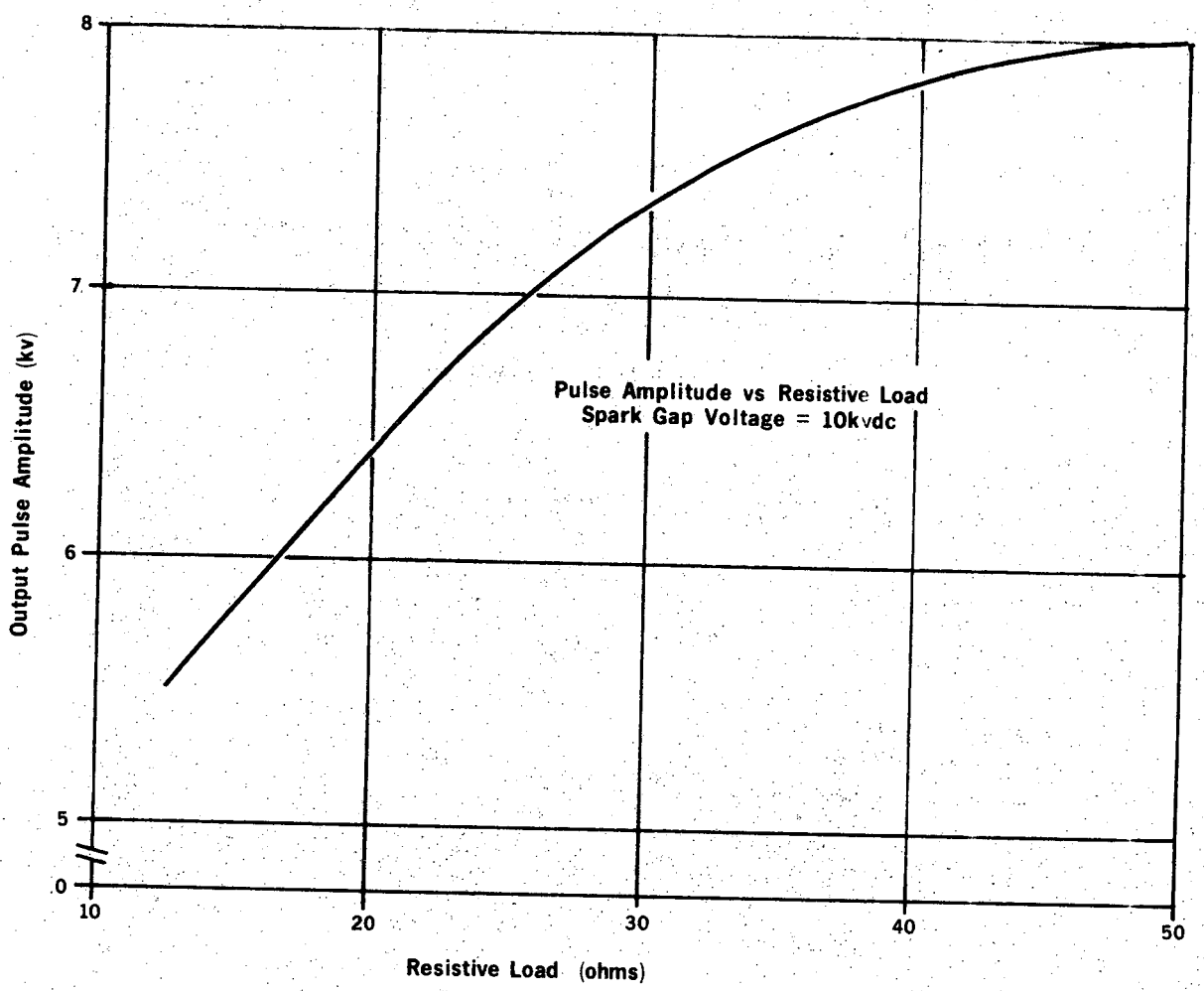
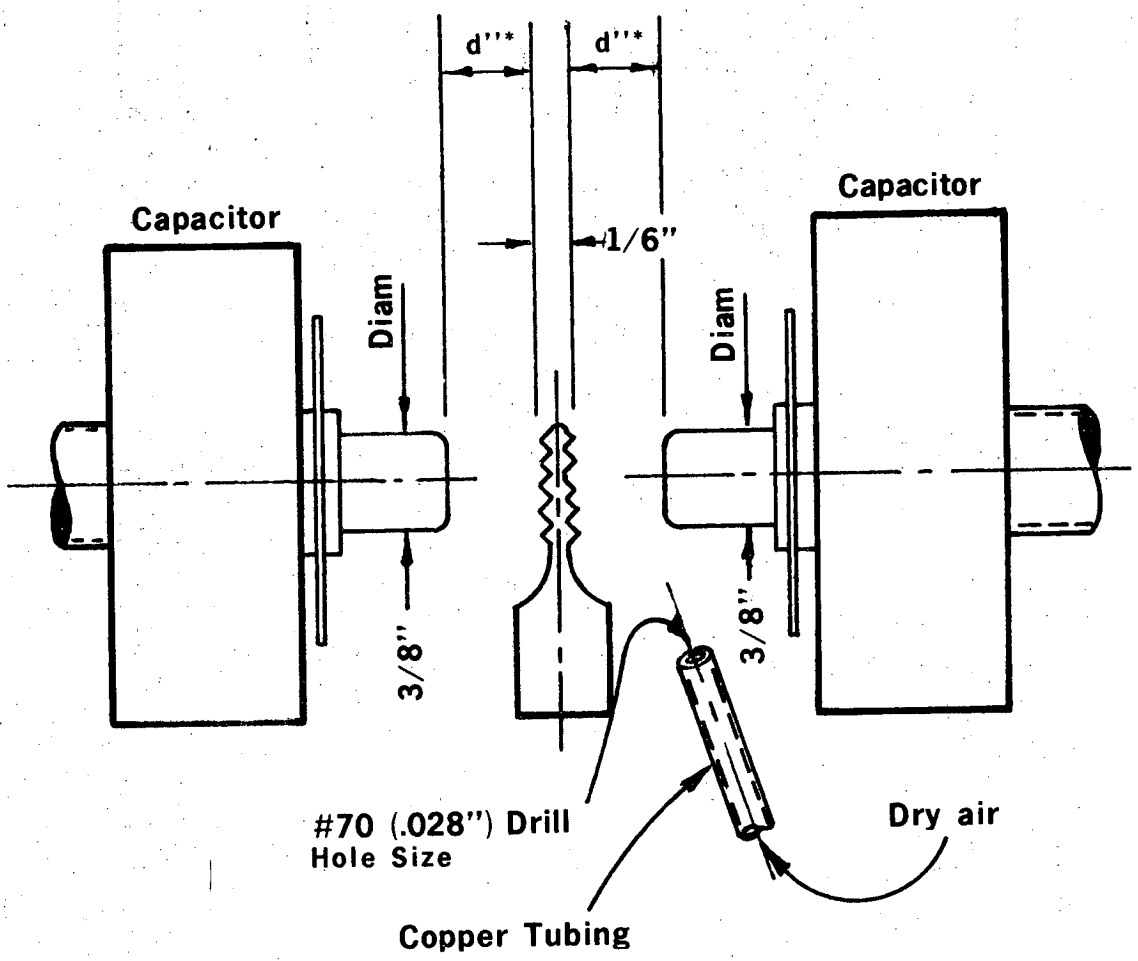

Pulse Amplitude vs Resistive Load
Spark Gap Voltage = 10kvdc
Output Pulse Amplitude (kv)
8
7
6
5
0
10
20
30
40
50
Resistive Load (ohms)
XBL 707 1539

Fig. 3



* See Table 1

XBL 707 1549

Fig. 4

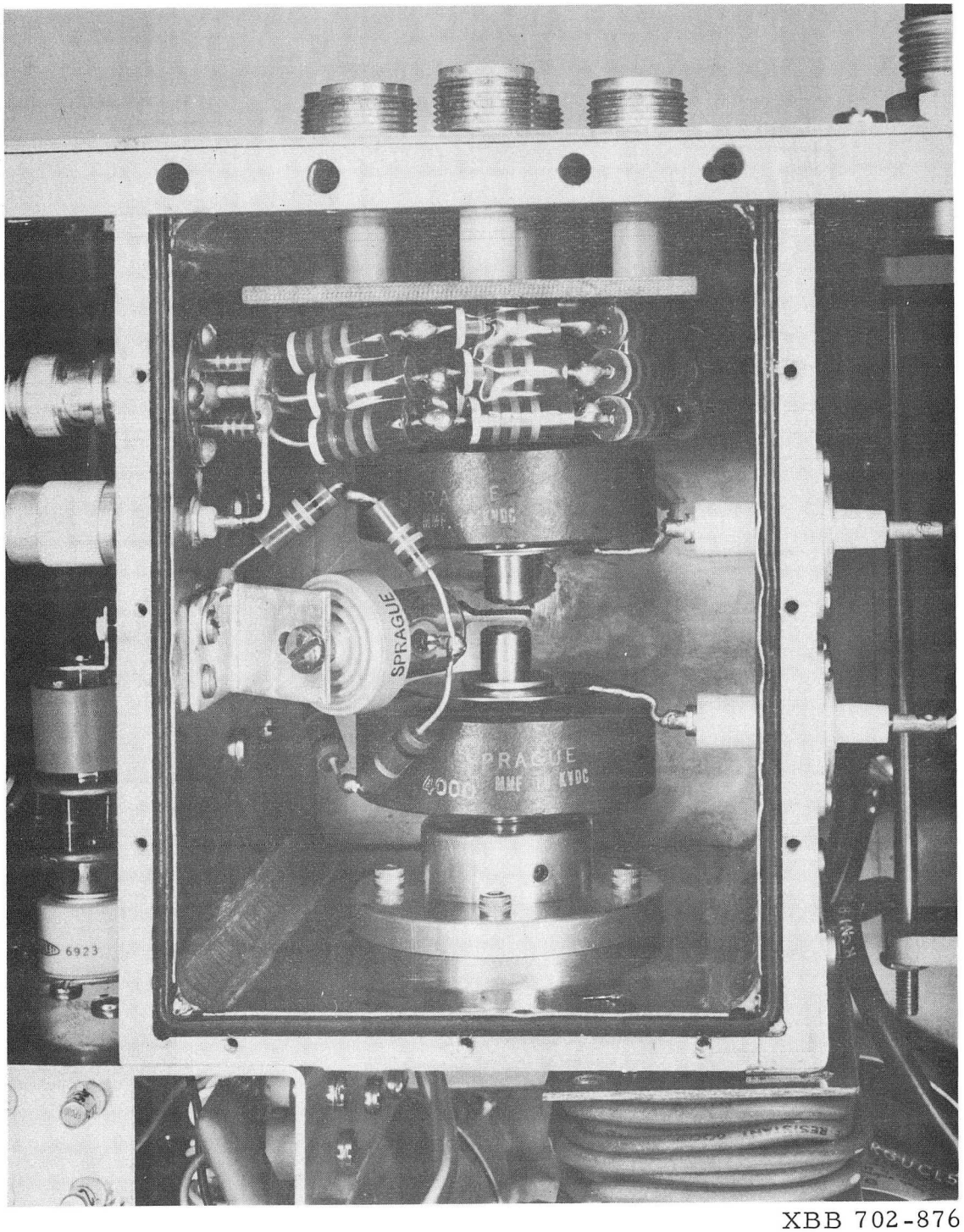


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Fig. 5

Fig. 6

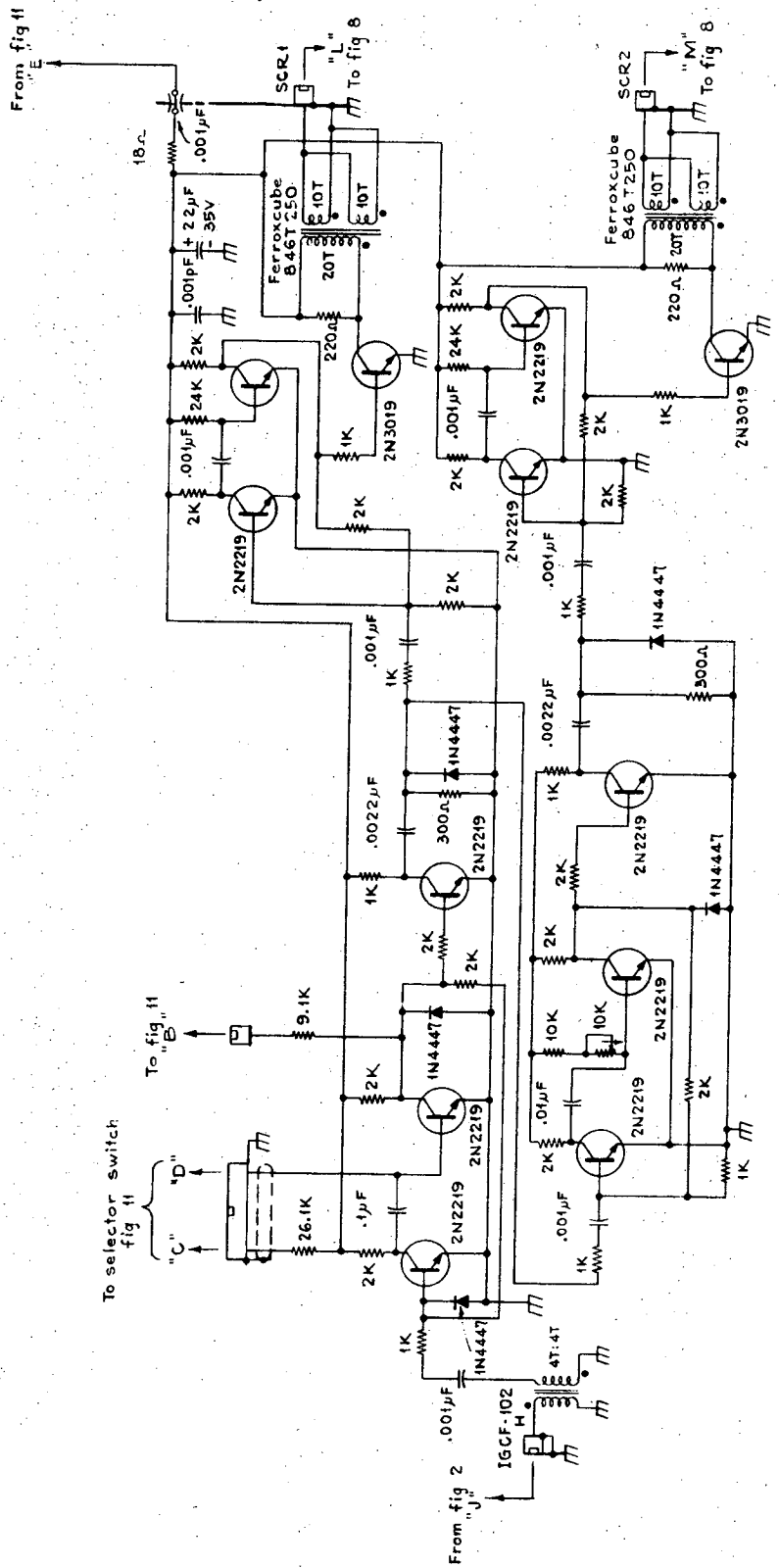

From fig 11 "E"
SCR1
"L" To fig 8
SCR2
"M" To fig 8
Ferroxcube 846T250
Ferroxcube 846T250
18Ω
.001μF
+ 22μF 35V
.001μF
10T
10T
20T
220Ω
2K
24K
.001μF
2K
1K
2N2219
2N3019
2N4447
300Ω
.0022μF
10K
.01μF
.1μF
26.1K
9.1K
To fig 11 "B"
To selector switch fig 11
"C"
"D"
IGCF-102
4T:4T
From fig 2 "J"
XBL 707-1540

Fig. 7

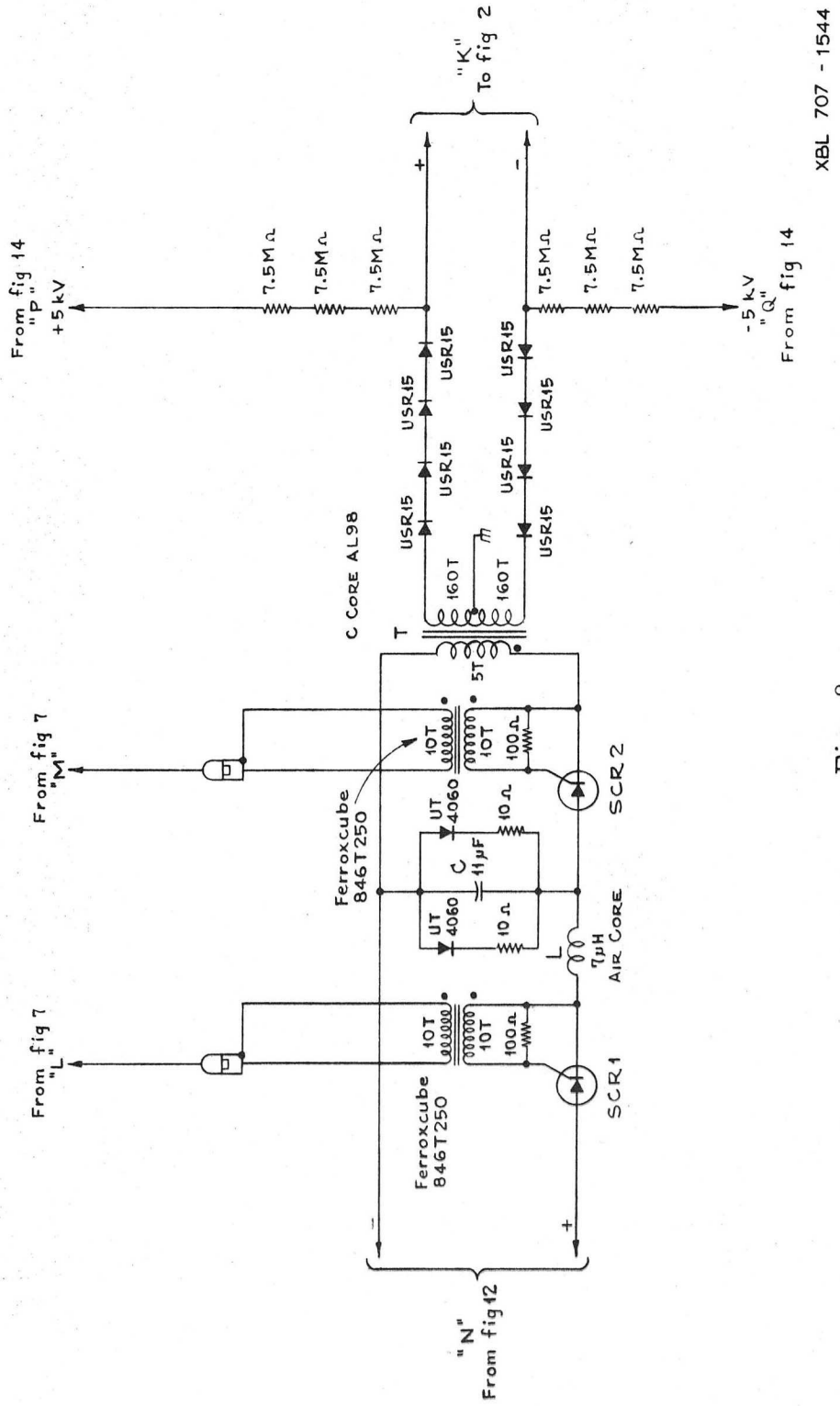
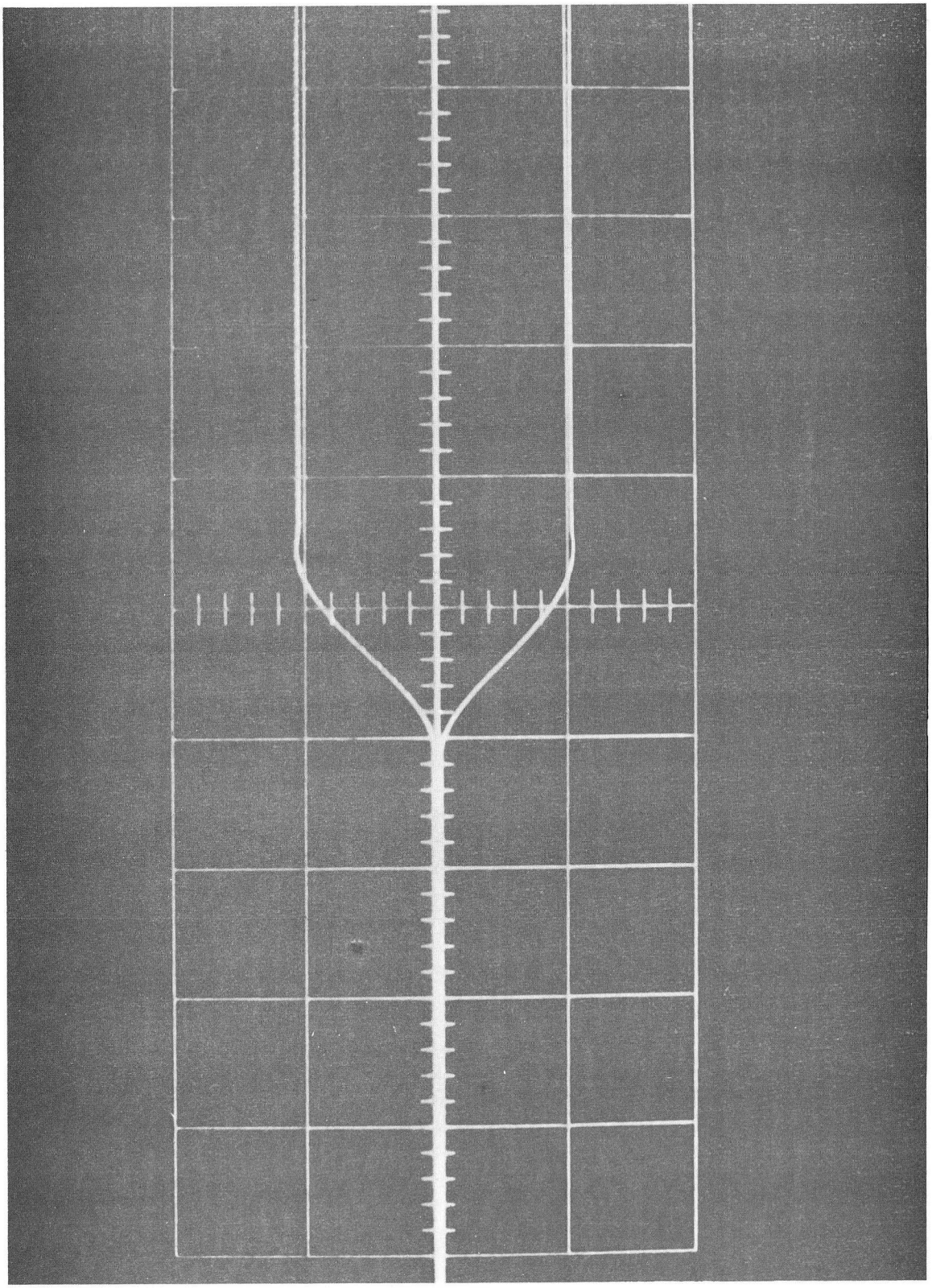

From fig 14
"P"
+5 kV
7.5MΩ
7.5MΩ
7.5MΩ
"K"
To fig 2
+
-
USR15
C CORE AL98
160T
m
T
5T
From fig 7
"M"
From fig 7
"L"
10T
10T
100Ω
Ferroxcube
846T250
UT
4060
10Ω
C
11μF
L
7μH
AIR CORE
SCR 2
SCR 1
"N"
From fig 12
-5 kV
"Q"
From fig 14
XBL 707 - 1544

Fig. 8



5 kV/div.

10 μsec/div.

XBB 702-1082A

Fig. 9

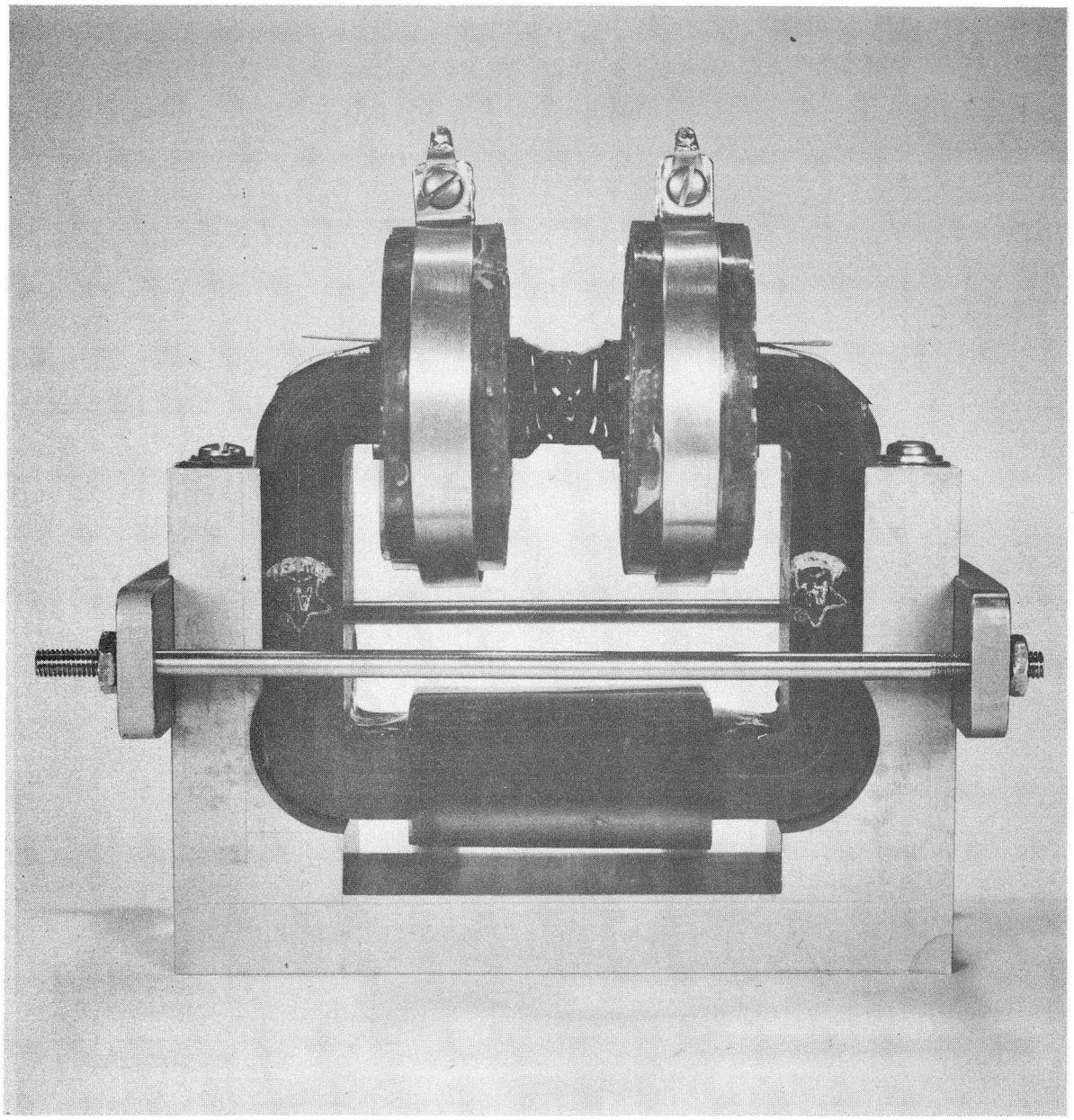


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Fig. 10

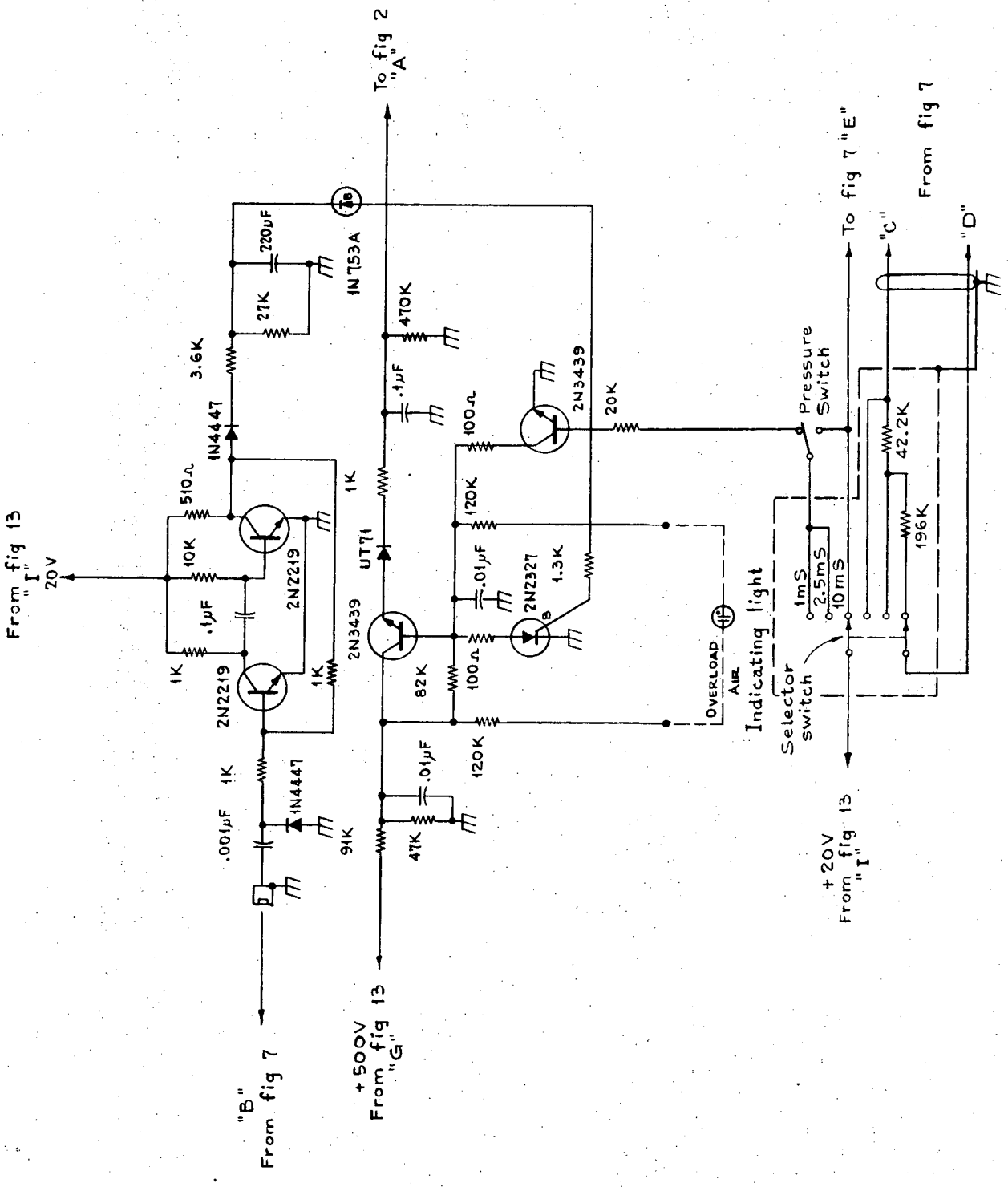

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Fig. 11

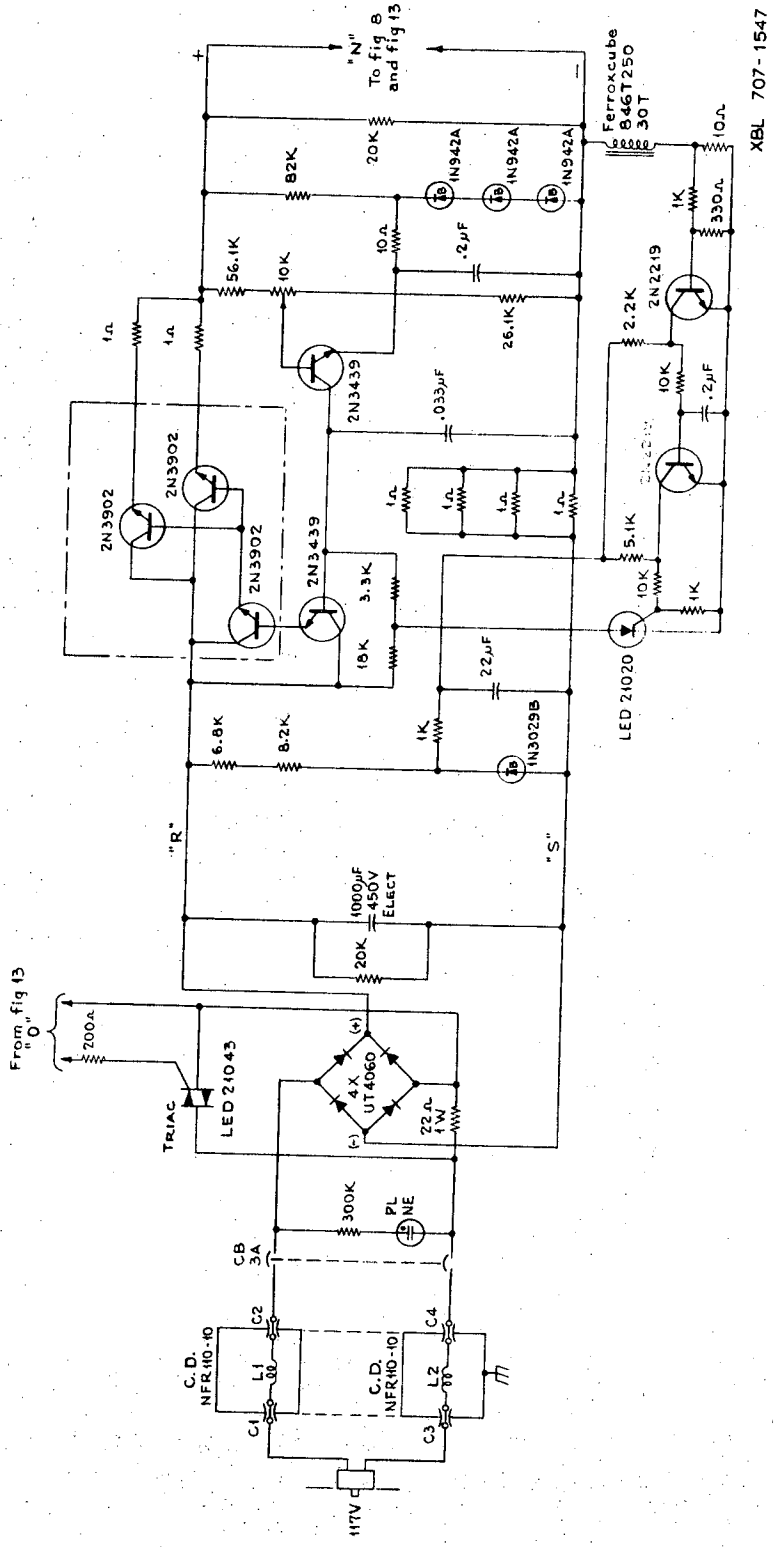

"N"
To fig 8 and fig 13
Ferroxcube 846T250 30T
XBL 707-1547
82K
20K
1N942A
1N942A
1N942A
10Ω
.2μF
56.1K
10K
26.1K
1Ω
2N3439
.033μF
2N3902
2N3902
2N3902
2N3439
3.3K
18K
22μF
1K
1N3029B
6.8K
8.2K
"R"
"S"
1000μF 450V ELECT
20K
From fig 13 "O"
200Ω
TRIAC
LED 21043
4 X UT4060
22Ω 1W
300K
PL NE
CB 3A
C.D. NFR410-10
C.D. NFR410-10
C1
C2
C3
C4
L1 100
L2 100
117V
LED 21020
5.1K
10K
1K
2N2219
2.2K
1K
330Ω
10Ω
10K
.2μF

Fig. 12

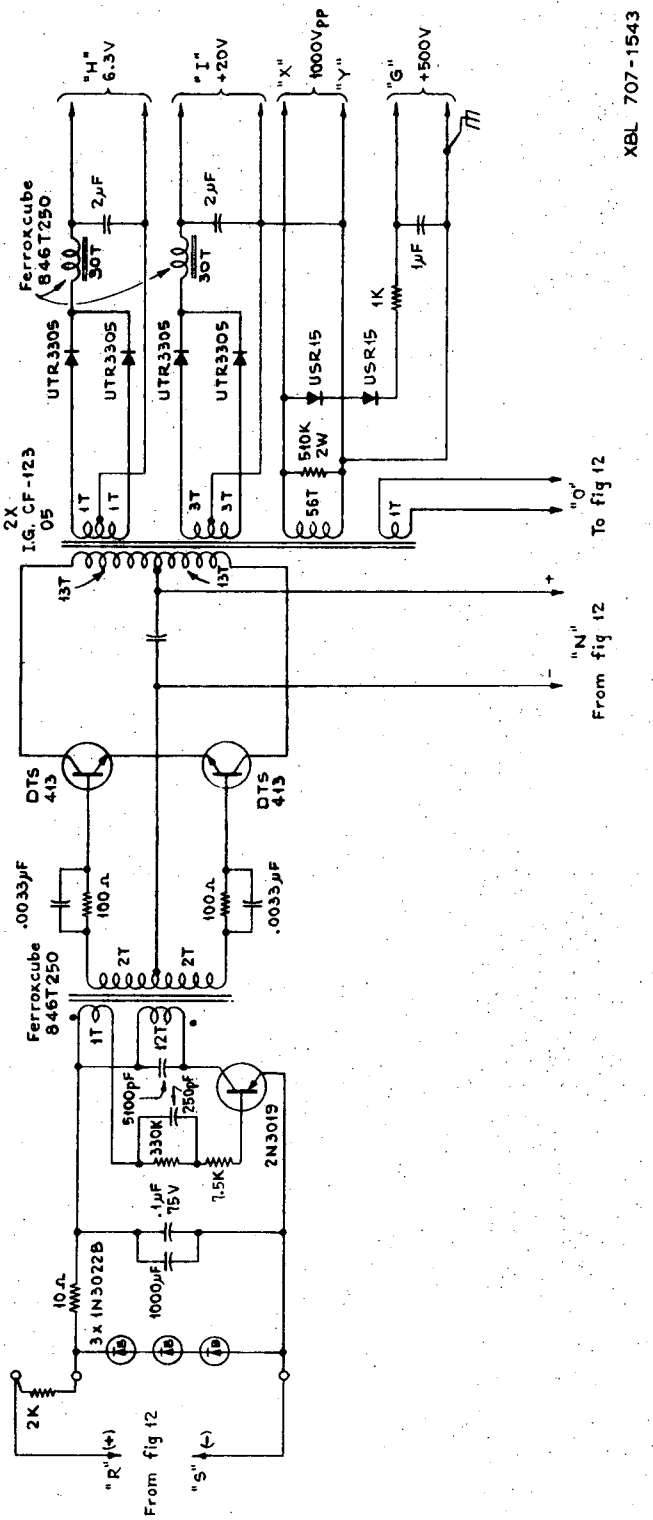

"H" 6.3V
"I" +20V
"X" 1000Vpp
"Y"
"G" +500V
Ferroxcube 846T250
30T
2μF
UTR3305
USR15
1K
1μF
510K 2W
56T
1T
3T
2X I.G. CF-123 05
13T
"O" To fig 12
"N" From fig 12
DTS 415
.0033μF
100Ω
2T
Ferroxcube 846T250
12T
5100pF
250pF
330K
2N3019
7.5K
.1μF 75V
1000μF
10Ω
3 x IN3022B
2K
"R" (+)
From fig 12
"S" (-)
XBL 707-1543

Fig. 13

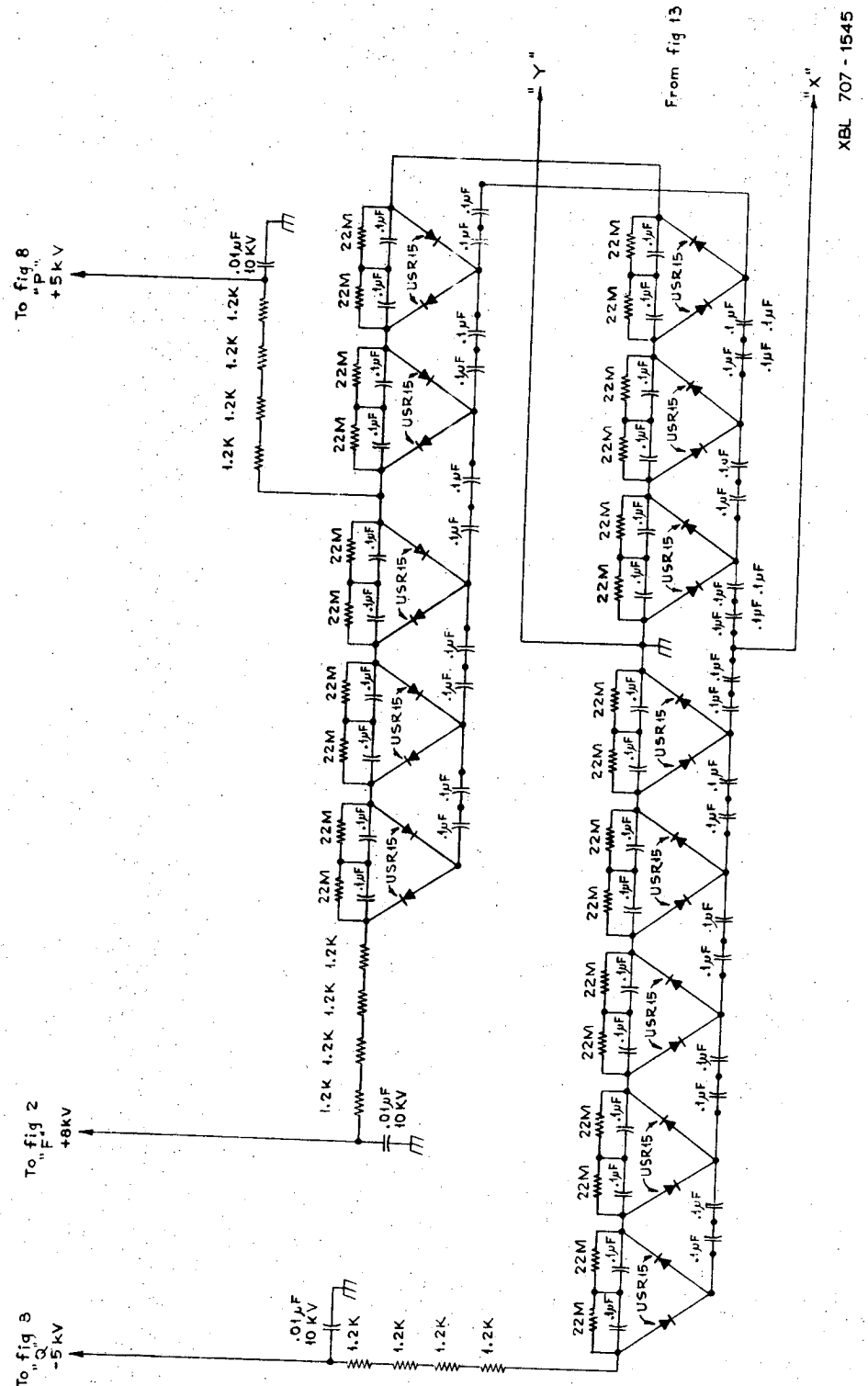
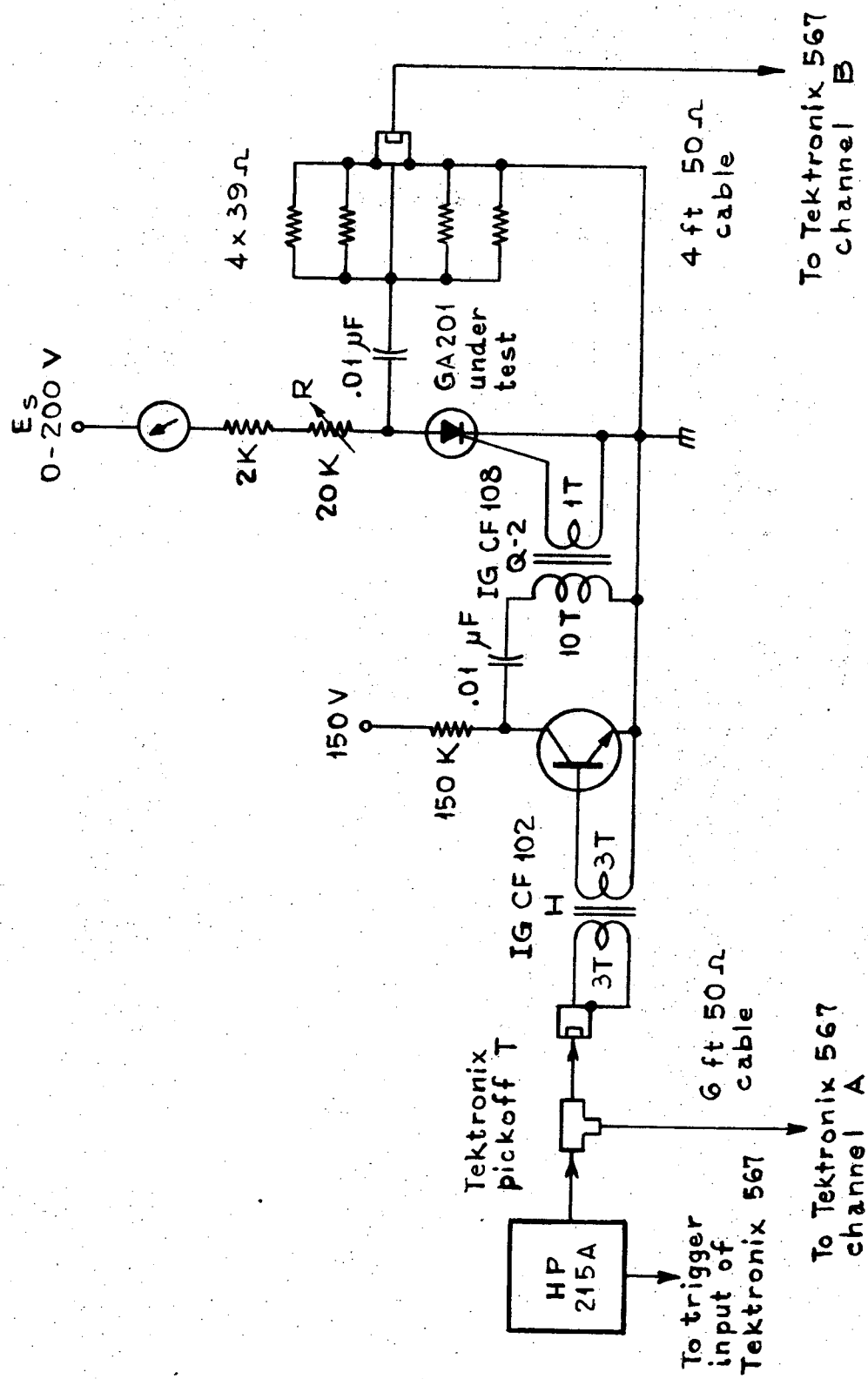
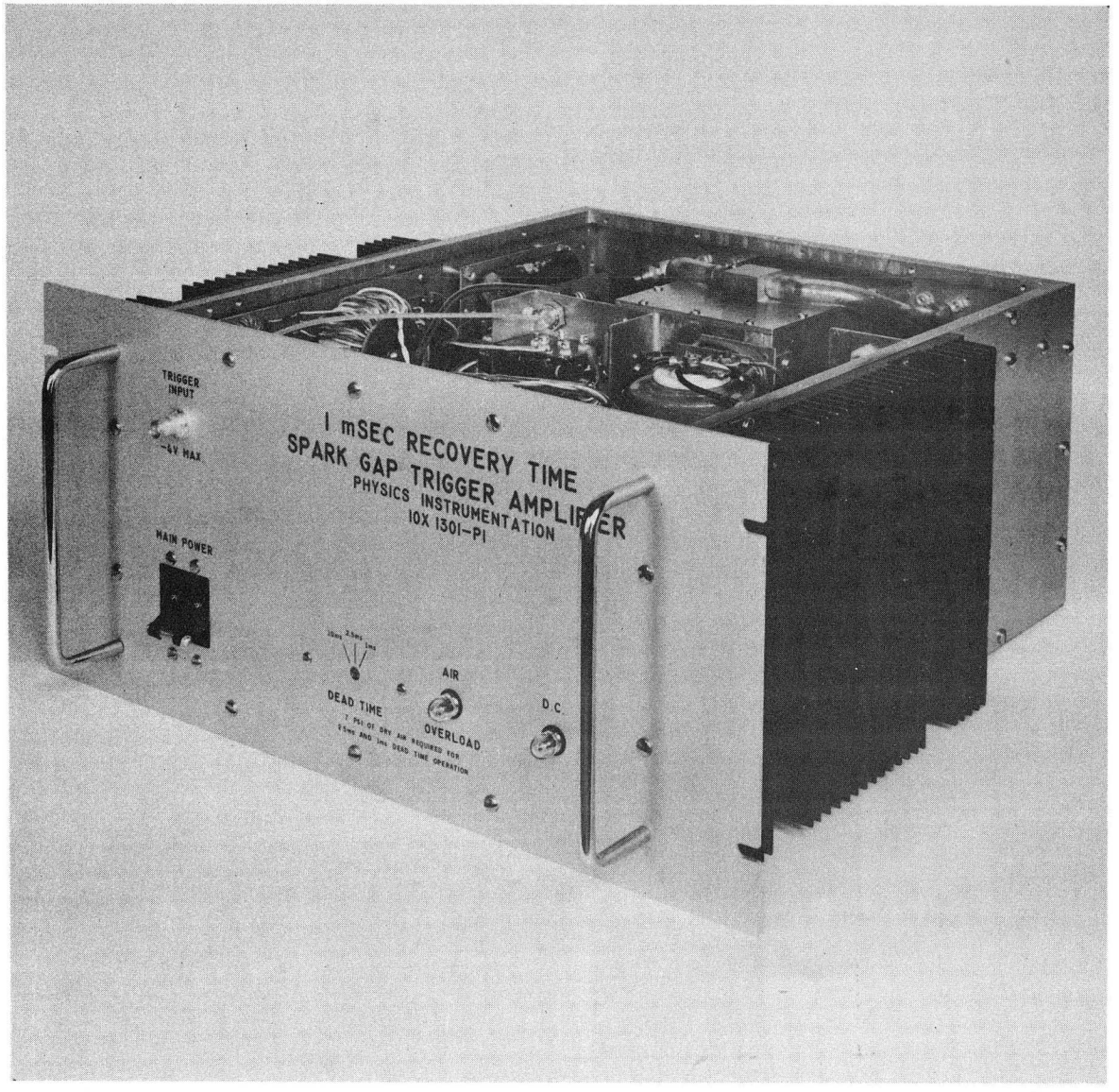

To fig 8 "P" +5kV
To fig 2 "F" +8KV
To fig 3 "Q" -5kV
From fig 13
"Y"
"X"
.01μF 10KV
1.2K
22M
.1μF
USR15
XBL 707-1545

Fig. 14



XBL 707-1546

Fig. 15



XBB 702-877

Fig. 16

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