UNIVERSITY OF CALIFORNIA SAN DIEGO

Ultra-Wideband mm-Wave I/Q CMOS Transmitters for High-Order QAM Waveforms

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Hasan Al-Rubaye

Committee in charge:

Professor Gabriel Rebeiz, Chair
Professor Peter Asbeck
Professor Gert Cauwenberghs
Professor William Hodgkisss
Professor Daniel Sievenpiper

2018

The dissertation of Hasan Al-Rubaye is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2018

DEDICATION

To my parents

EPIGRAPH

It is not the critic who counts; not the man who points out how the strong man stumbles, or where the doer of deeds could have done them better. The credit belongs to the man who is actually in the arena, whose face is marred by dust and sweat and blood; who strives valiantly; who errs, who comes short again and again, because there is no effort without error and shortcoming; but who does actually strive to do the deeds; who knows great enthusiasms, the great devotions; who spends himself in a worthy cause; who at the best knows in the end the triumph of high achievement, and who at the worst, if he fails, at least fails while daring greatly, so that his place shall never be with those cold and timid souls who neither know victory nor defeat.

—Theodore Roosevelt

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Chapter 2, in full, is a reprint of the material as it appears in: H. Al-Rubaye and G. M. Rebeiz, "W-band direct-modulation $>$ 20-Gb/s transmit and receive building blocks in 32-nm SOI CMOS", *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2277-2291, Sep. 2017. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in part, has been submitted for publication of the material as it may appear in: H. Al-Rubaye and G. M. Rebeiz, "A 200-Gbps I/Q Modulator in 45 nm SOI CMOS for Ultra-Wideband 5G Radios," submitted to the *IEEE European Solid-State Circuits Conference (ESSCIRC)*, 2018. The dissertation author was the primary investigator and author of this paper.

Chapter 3 is also, in part, contains material that is currently being prepared for submission for publication as may appear in: H. Al-Rubaye and G. M. Rebeiz, "Analysis and Design of Wideband CMOS IQ Modulators," *IEEE J. Solid-State Circuits*, in preparation. The dissertation author was the primary investigator and author of this material.

VITA

2013	B. S. in Electrical Engineering, University of Toronto, Canada
2013-2018	Graduate Research Assistant, University of California San Diego
2018	Ph. D. in Electrical Engineering, University of California San Diego

PUBLICATIONS

H. Al-Rubaye and G. M. Rebeiz, "A 20 Gbit/s RFDAC-based direct modulation W-band transmitter in 32 nm SOI CMOS", *in Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2016, pp. 1-4.

H. Al-Rubaye and G. M. Rebeiz, "W-band direct-modulation $>$ 20-Gb/s transmit and receive building blocks in 32-nm SOI CMOS", *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2277-2291, Sep. 2017.

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ABSTRACT OF THE DISSERTATION

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The continuing proliferation of wireless electronic devices, coupled with the promise of fifth generation mobile networks (5G) and Internet-of-Things (IoT) scale connectivity, will demand innovate design techniques and solutions on all network and device layers for both wireless and optical systems. Broadband and software-defined connectivity is at the forefront of research efforts to address these new challenges. The research projects presented in this dissertation explore the limits of current CMOS technology with the goal of achieving true DC-100 GHz software-defined transmitters, and with the maximum achievable instantaneous bandwidth. These transmitters will address new applications, such as short-range device-to-device communications, server-to-server connectivity in data centers, and fifth generation mm-wave

software-defined transceivers, while still supporting traditional mobile links and connectivity below 6 GHz.

Chapter 1

Introduction

The rise of the World Wide Web in the late second half of the twentieth century, along with the appearance of the first cellular networks and cellular phones, has had an unquestionably staggering impact on our "human experiment", and on our fundamental understanding of what, for example, constitutes a basic human need. In this new world where landline phones and hand-written letters were replaced with handheld wireless phones, E-mails and electronic Christmas cards, a new form of human communication was established and became highly sought after, for its novelty at first, and then for its efficacy afterwards. Just as we were starting to digest this new reality, smart-phone products started to appear in the early 2000's, combining cellular connectivity with global on-the-go data access; two activities that were thought of as separate before then; thus creating yet another mania and a new found "obsession" with keeping a constant online presence.

Social commentary aside, engineers were now faced with a new challenge and that is moving around more information at low cost and in an energy-efficient manner. This chapter discusses the fundamental concepts that govern data transmission at a basic level, and from the point of view of a circuit designer, while also attempting to set the theme for the rest of the dissertation.

1.1 Shannon–Hartley Theorem

The maximum rate at which information can be transmitted over a communication channel is governed by a fundamental formula commonly known as *Shannon's capacity theorem* [1] that states:

$$C = BW \cdot log_2(1 + SNR) \tag{1.1}$$

Where BW is the bandwidth of the channel, SNR is the signal-to-noise ratio and C is the channel capacity measured in bits per second and without error correction. As a practical numerical example, let BW = 1 GHz which is considered an extremely wide bandwidth by today's standards and SNR = 50 dB , then the maximum data rate achievable is 16.6 Gbps.

Examining industry-standard square constellations, it can be shown that 50 dB of SNR will guarantee an error-less transmission of a 16384-QAM constellation. The mathematical basis behind this calculation will be introduced in the second chapter of this dissertation. Nonetheless, 16384-QAM has a spectral efficiency of 14 bits per hertz, resulting in 14 Gbps transmission rate. The author is aware of only a few rare examples of systems that are capable of supporting such a complex modulation format. Using simpler and more common modulation formats, such as 64-QAM which renders the data rate at 6 Gbps, results in considerably lower rates than the fundamental limit.

The numerical example given above highlights the importance of using complex and spectrally-efficient modulation formats in order to increase the transmission rate and close the gap with the fundamental Shannon limit. To close the gap further, complex error-correction schemes are now implemented [2].

From fundamental physics, the quality factor of a resonator is given by the ratio of the energy stored in the resonator to the energy dissipated. In electronic circuits, resonators are formed by non-ideal inductive and capacitive elements, and thus have a finite quality factor (Q).

Interestingly, the quality factor is related to the bandwidth of the resonator:

$$Q = \frac{f_r}{\Delta f} \tag{1.2}$$

where f_r is the resonance frequency, and Δf is the full-width at half maximum, or the 3–dB bandwidth. Here again we make another observation, and that is to increase the BW variable as it appears in Shannon's equation, we must increase the carrier frequency for a given quality factor. Reducing the quality factor to increase the BW is another alternative, as long as the link does not become SNR limited, since reducing Q increases the loss in the resonator.

1.2 Implications

We have shown in the previous section that in order to increase the data rate in a wireless channel, for a given SNR, the carrier frequency must be increased and high-order spectrally-efficient modulation format must be employed.

Indeed, to achieve Gbps-speed links, wireless transceivers must operate at mm-wave frequencies beyond the traditional RF carriers below 6 GHz. This is one of the promises of future 5G networks. Furthermore, to achieve high spectral efficiency, the use of high order modulation formats (beyond 64-QAM) is on the rise, coupled with intelligent coding and modulation techniques such carrier aggregation (CA), Orthogonal Frequency Division Multiplexing (OFDM) signaling, and multiple-input multiple-output (MIMO) systems. All designed with the target of increasing the system bandwidth while keeping it robust to channel impairments.

1.3 CMOS Technology

CMOS technology continues to be the driving force behind the development of RF and mm-wave integrated circuit and systems. The continuous scaling in CMOS technology

motivated by the economics of scale has also benefited the performance of these devices. More specifically, the increasing transition frequency f_T of CMOS devices, has enabled the design of high-performance digital and mixed-signal circuits.

Analog and RF circuits, on the other hand, have been suffering from increasingly poor linearity due to short-channel effects and downscaling of supply voltages.

1.4 Thesis Overview and Contributions

Digitally-assisted techniques at RF frequencies leverage technology scaling and continue to improve as switches get faster, while offering attractive systems-on-chip (SoCs) integration where RF and analog blocks are seamlessly integrated with digital baseband circuitry. Chapter 2 presents an example of such an effort. A record data rate of 20 Gbps is achieved with a novel digital transmitter design in 32 nm CMOS SOI, operating at 90 GHz.

Chapter 3 presents a DC-60 GHz I/Q modulator/transmitter chip in 45 nm SOI CMOS, that can serve as a critical building block for next generation multi-standard and high-capacity wireless backhaul links. The modulator achieves 200 Gbps in 16-QAM (50 Gbaud/s), while consuming 200 mW, resulting in record 1 pJ/bit modulation efficiency.

Both projects presented in this dissertation attempted to push mm-wave transmitters to the boundaries of current CMOS technology and instrumentation limits, and resulted in state-of-the-art data rates.

Chapter 2

W-band Direct-Modulation > 20 Gbit/s Transmit and Receive Building Blocks in 32 nm SOI CMOS

2.1 Introduction

The continuous scaling in CMOS technology has led to the emergence of a relatively new class of digitally-assisted analog and RF circuit design techniques. Digital-like power amplifiers and modulators at RF [3–9] and mm-wave [10, 11] frequencies are one such example. This is driven by the increasing transition frequency f_T of CMOS devices, which enables the design of high-performance digital switches. Analog and RF circuit designers, on the other hand, are forced to cope with analog building blocks which suffer from poor linearity due to short-channel effects and downscaling of supply voltages. Digitally-assisted techniques at RF frequencies leverage technology scaling and continue to improve as switches get faster, while offering attractive systems-on-chip (SoCs) integration where RF and analog blocks are seamlessly integrated with digital baseband circuitry.

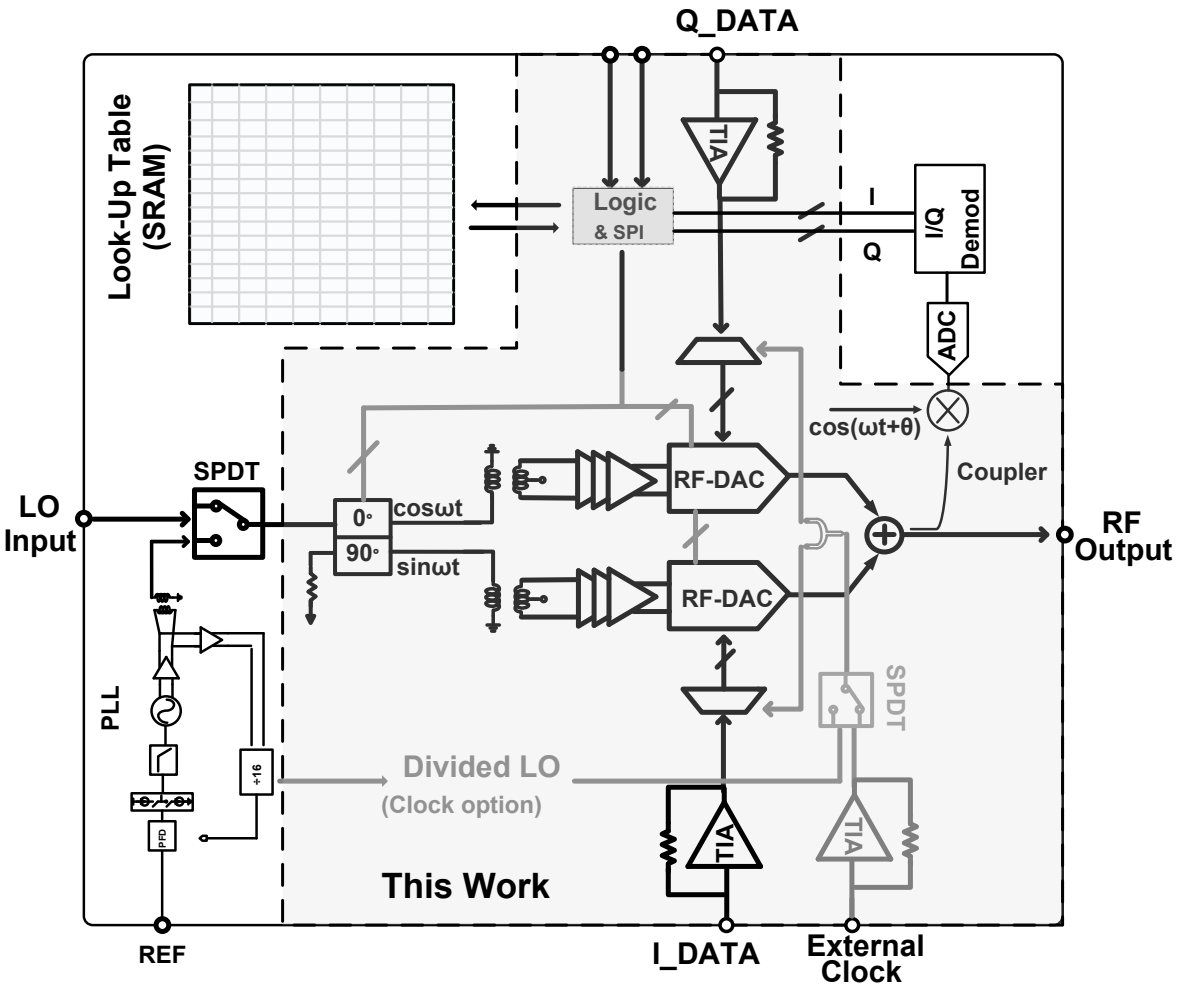


Figure 2.1: Block diagram of proposed W-band transmitter. Shaded circuit blocks are presented in this work.

More specifically, the increasing need for high data rate (Gbps) wireless links has created a new class of direct modulation RF transmitters which offer greater bandwidths than traditional heterodyne or zero-IF transmitters. Direct modulation RF transmitters perform the digital-to-analog conversion and modulation directly at the RF frequency, using RF digital-to-analog converters (RF-DACs), which maximize the available modulation bandwidth [6, 12]. Heterodyne transmitters require additional IF and RF filtering stages, while zero-IF transmitters require a low-pass filtering stage after the baseband DAC to remove the images above the Nyquist frequency. Theses filters are either implemented as active Gm-C stages - which suffer from limited linearity

and lead to an increased power consumption - or as passive filters built from lumped or distributed R/L/C components that tend to be lossy, bulky and are difficult to implement with high quality factor on CMOS backends, resorting to off-chip components. On the other hand, RF-DACs minimize or eliminate the need for filtering stages, which limit the bandwidth and degrade the EVM as will be discussed in section 2.2, also leading to reduced chip area and cost. Moreover, using an RF-DAC enables higher integration by employing the baseband data generator together with the transmitter on the same chip.

The output spectrum of an RF-DAC contains aliases at multiples of the baseband clock fs modulated with the carrier frequency. Without oversampling, non-return-to-zero (NRZ) baseband data will result in a zero-order-hold (ZOH) interpolation at the output, which translates to a sinc frequency response. The sinc function nulls occur at multiples of the clock rate away from the carrier frequency, and the first peak is 13-dB lower in magnitude. Alternatively, higher order interpolations or filtering can by synthesized by running the sampling clock higher than the Nyquist rate, at the expense of increased power consumption [5–9, 13]. Furthermore, adequate filtering can also be obtained using the output RF matching network, especially at high sampling clock frequencies where the clock harmonics fall out of band.

This work presents the design of building blocks for the proposed mm-wave transmitter solution shown in Fig. 2.1. The transmitter topology is based on a cartesian architecture consisting of two RF-DACs that are driven in quadrature and current-combined at the output. In order to minimize the transmit EVM and meet spectral mask requirements, a calibration scheme is proposed where the transmitter output is coupled and down-converted with a wideband receiver to determine required predistortion settings for the N-bit RF-DACs. The predistortion settings are then stored in an on-chip memory which serves as a look-up table in operation mode. Furthermore, reconfigurable high-speed digital retiming and deserializing circuitries are included to deserialize a single high-speed bit stream into N-bit streams, depending on the RF-DACs resolution. The transmitter chip presented in this work, is based on 2-bit RF-DACs and achieves BPSK, PAM4,

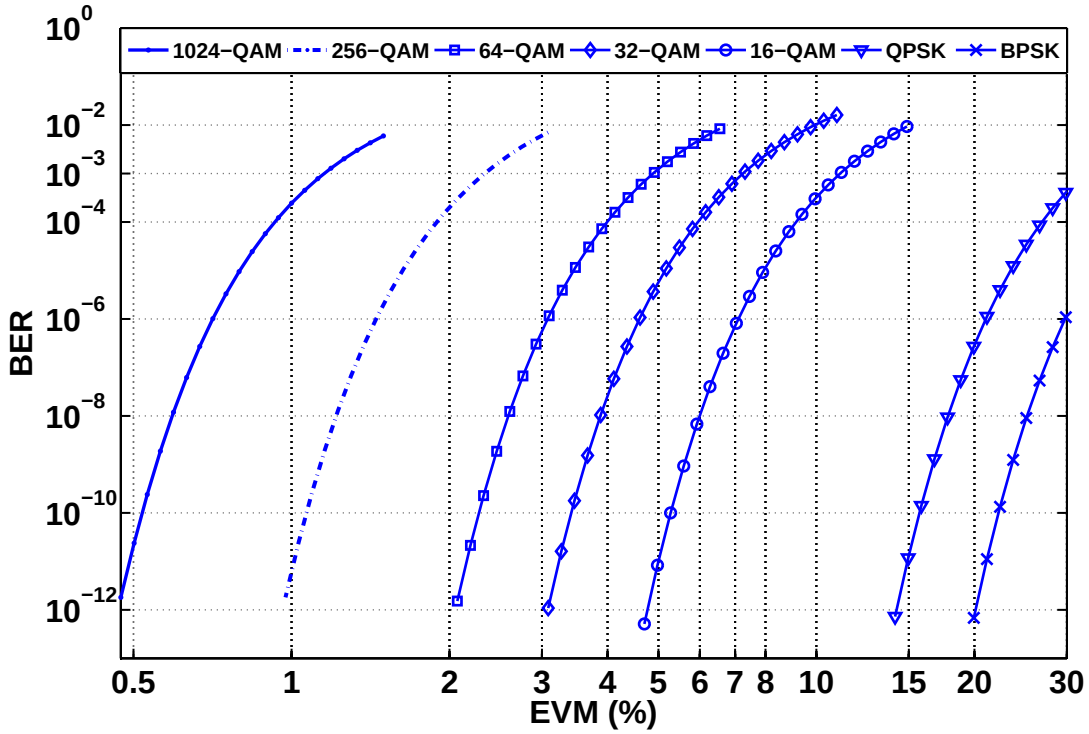


Figure 2.2: Bit Error Rate (BER) vs. Error Vector Magnitude (EVM) for popular m-QAM modulations.

QPSK and 16-QAM modulations, depending on the data rate and the RF-DACs mode of operation, and is implemented in 32 nm SOI CMOS process. The goal of this work is to investigate system architectures and circuit design techniques that lead to the highest possible data throughput at W-band while maintaining a bit-error-rate (BER) < 10^{-3}. Section 2.2 presents system analysis and simulations that dictated the design decisions followed. Section 2.3 introduces the circuit implementations of the 2-bit RF-DAC, W-band LO driver, wideband receiver and high-speed baseband digital drivers. Section 2.4 presents transmitter and receiver link measurements and section 2.5 concludes the paper.

2.2 System Analysis

2.2.1 System Architecture

A cartesian system architecture is employed in this work, as shown in Fig. 2.1. Cartesian systems are more favorable for high-performance mm-wave systems, due to the relative simplicity of generating and combining quadrature signals. More importantly, cartesian transmitters do not suffer from bandwidth expansion that is experienced in polar transmitters [11, 12], which require oversampling in the phase path, thus limiting the maximum achievable baud rate. Moreover, outphasing transmitters suffer from similar bandwidth expansion issues, since the transformation needed to synthesize the phase information is inherently a nonlinear operation.

2.2.2 BER and EVM Requirements

Since one of the applications of wideband mm-wave transceivers is in replacing fiber-optics in last-mile links and data centers, an upper limit of pre- forward-error-correction (FEC) BER of $< 10^{-3}$ is imposed in this work, which guarantees passing FEC limits [14], thus rendering the link error-free after implementing forward error correction. For M-ary QAM modulation, BER and SNR are related by [15]

$$P_b(M) = \frac{2}{log_2 M} P_{b,\sqrt{M}}(1 - \frac{1}{2} P_{b,\sqrt{M}}) \tag{2.1}$$

where P_b is the bit-error-probability, and $P_{b,\sqrt{M}}$ is

$$P_{b,\sqrt{M}} \backsimeq 2\frac{\sqrt{M}-1}{\sqrt{M}}.Q\left(\sqrt{3\frac{log_2 M}{M-1}\frac{BW}{BR}SNR}\right) \tag{2.2}$$

where BW is the signal bandwidth at baseband, BR is the bit rate and $Q(x)$ is the standard Q-function. The expression can be further simplified by assuming that the bandwidth BW occupied is equal to the baud rate, leading to

$$P_{b,\sqrt{M}} \backsimeq 2\frac{\sqrt{M}-1}{\sqrt{M}}.Q\left(\sqrt{3\frac{SNR}{M-1}}\right) \tag{2.3}$$

EVM is the most widely accepted standard to quantify the performance of wireless transmitters nowadays and therefore it is desirable to relate the EVM directly to the BER, then use the EVM to derive the required design specifications for the circuit blocks. EVM is defined as the ratio of the root-mean-square (RMS) constellation error to the peak constellation symbol. This is the most adopted definition in industry [16, 17], and is used in Vector Signal Analysis (VSA) softwares in commercial oscilloscopes. Assuming an SNR-limited link, such that any error in the received symbols is caused by additive white Gaussian noise, then SNR represents the average signal power to the average constellation error power. Since EVM is measured with respect to the peak constellation symbol, EVM and SNR are related by the maximum-to-average constellation ratio, such that,

$$EVM = 100\% \times \sqrt{\frac{\sqrt{M}+1}{3\,.SNR\,.(\sqrt{M}-1)}} \tag{2.4}$$

which leads to the simulation results given in Fig. 2.2 that show the EVM values for a given BER requirement and a choice of modulation format. It can be observed that the EVM requirements are highly relaxed for constant envelope modulations such as BPSK and QPSK, which make them fitting for very high frequency mm-wave and sub-THz transmitters (>100 GHz), where there is an abundance of frequency bandwidth but a limited output power available. Higher-order AM-based m-QAM modulations such as 16-QAM, 32-QAM and 64-QAM offer improved spectral efficiencies, at the cost of a rapid increase in SNR and linearity requirements. For example, the EVM requirement for 1e-6 BER changes from 20% for QPSK to 7% for 16-QAM. Modulation formats beyond 64-QAM demand stringent phase noise and dynamic range requirments, as will be shown in sections 2.2.4 and 2.4.3, and are perhaps best suited for transmitters with operating frequencies below 30 GHz.

An alternative definition of EVM normalizes the error vectors to the average symbol energy [18], which has the advantage of relating EVM to SNR simply by $EVM_{rms,avg} = 100\%/\sqrt{SNR}$ and is independent of the modulation format. EVM (or $EVM_{rms,peak}$) and $EVM_{rms,avg}$ are related by $EVM = EVM_{rms,avg} \times \sqrt{\frac{\sqrt{M}+1}{3(\sqrt{M}-1)}}$. Throughout this paper, unless otherwise stated, EVM refers to the first definition that normalizes to the peak symbol energy $EVM_{rms,peak}$.

2.2.3 Link Margin Analysis and Choice of Digital Modulation Technique

The difficulty of efficiently generating modulated waveforms, at mm-wave carrier frequencies with sufficiently high SNR to support high-order modulation formats, is exacerbated in cartesian mm-wave RF-DACs since there is 3 dB of inevitable loss when combining the quadrature outputs. Therefore, to achieve the lowest joule per bit energy efficiency, the transmitter in this work is designed to support modulation formats up to 16-QAM - while maintaining a SNR of at least 20 dB (Fig. 2.2). The required transmit power P_{TX} can be calculated using

$$P_{TX} = P_{RX} + FSPL - (G_{TX} + G_{RX}) \tag{2.5}$$

where P_{RX} is the required power at the receiver in order to maintain the targeted SNR over 30 GHz of bandwidth. Assuming a receiver noise figure of 20 dB, P_{RX} is estimated to be equal to -29 dBm. $FSPL$ is the free space loss and is 71 dB at a 1 meter distance, G_{TX} and G_{RX} are the transmit and receive antenna gains, respectively. Using (2.5), and assuming waveguide horn antennas with 20 dB of gain, the minimum required transmitter output power is found to be 2 dBm. In conclusion, RF-DACs with a minimum resolution of 2 bits and 2 dBm output power are needed for the transmitter, while a wideband design is required in the receiver with relaxed noise figure requirements.

2.2.4 EVM Degradation Sources and Design Challenges

There has been a number of contributions studying the effect of system non-idealities on the transmit EVM at mm-wave frequencies [19]. Sources of non-idealities such as non-linearity, in-band noise, IQ imbalance, and LO leakage have been studied extensively, and a number of design techniques were developed to tackle these challenges. This paper focuses on more fundamental and less explored limitations of the EVM.

Gain Ripple and Group Delay

In order to meet mask requirements and maximize spectral efficiency in wireless transmitters, pulse shaping filters are implemented, and such filters cause intersymbol interference (ISI) in the transmitted symbols. However, the overall BER is minimally affected since a complementary filter is implemented in the receiver to equalize the magnitude and phase distortion caused by the transmit filter.

However, for very wideband applications, it proves useful to model the effect of the transmit and receive channels frequency responses on the EVM. The channels can be modeled as non-ideal analog frequency filters with a certain magnitude ripple and non-linear phase response (non-constant group delay). The filter's non-ideal impulse response H_f leads to an increase in the ISI, thus degrading the EVM for a given SNR, such that [20]:

$$EVM_{rms,avg} = \sqrt{\frac{\sum_{k=-\infty,k\neq 0}^{k=\infty} |H_f(t_o + kT_s)|^2}{|H_f(t_o)|^2}} \tag{2.6}$$

Using an approximate, yet more accessible expression, the EVM is given by [21]:

$$EVM_{rms,avg} = \sqrt{\Delta a_{rms}^2 + [tan(\Delta\Phi_{rms}]^2} \tag{2.7}$$

where the Δa_{rms} is the root-mean-square value of the magnitude ripple, and $\Delta\Phi_{rms}$ is

the root-mean-square value of the deviation of the phase response from an ideal linear phase response, over the frequency of interest.

Frequency Synthesizer Phase Noise

There has been several research efforts in building W-band on-chip PLLs in CMOS and SiGe BiCMOS for radio and radar applications [22–26]. A significant performance edge has been documented in SiGe BiCMOS, due the lower transistor noise and lower $1/f$ flicker noise corner. This is in comparison with FET transistors where the corner frequency of highly-scaled FETs can reach tens of MHz. LO phase noise results in a frequency spreading of the carrier frequency that can be modeled as a Gaussian distribution. As a result, the EVM degradation is given by [18]:

$$EVM_{rms,avg} = \sqrt{2 - 2e^{-\sigma^2/2}} \tag{2.8}$$

where σ is the RMS phase error in radians, and is derived from the integrated LO phase noise. For small values of RMS phase error, and N being the division ratio needed to bring the VCO frequency down to the reference signal, if PN_{avg} is the average phase noise of the reference in dBc/Hz within the PLL bandwidth BW_{PLL}, then the $EVM_{rms,avg}$ can be approximated as:

$$EVM_{rms,avg} \approx \sigma \approx \sqrt{2.N^2.10^{PN_{avg}/10} BW_{PLL}} \tag{2.9}$$

For a PLL bandwidth of 10 MHz, and ignoring the phase noise contribution of the dividers in the loop, then to achieve lower than 3% $EVM_{rms,avg}$, a phase noise lower than -94 dBc/Hz and -104 dBc/Hz at 1 MHz and 10 MHz offsets are needed, respectively. Recently published SiGe BiCMOS PLL designs are capable of meeting these performance metrics [23, 27]. Unfortunately, mm-wave CMOS PLLs still lag in phase noise performance [22, 26], which is one of the fundamental reasons why modulation schemes higher in order than 64-QAM are not popular in mm-wave CMOS transceivers.

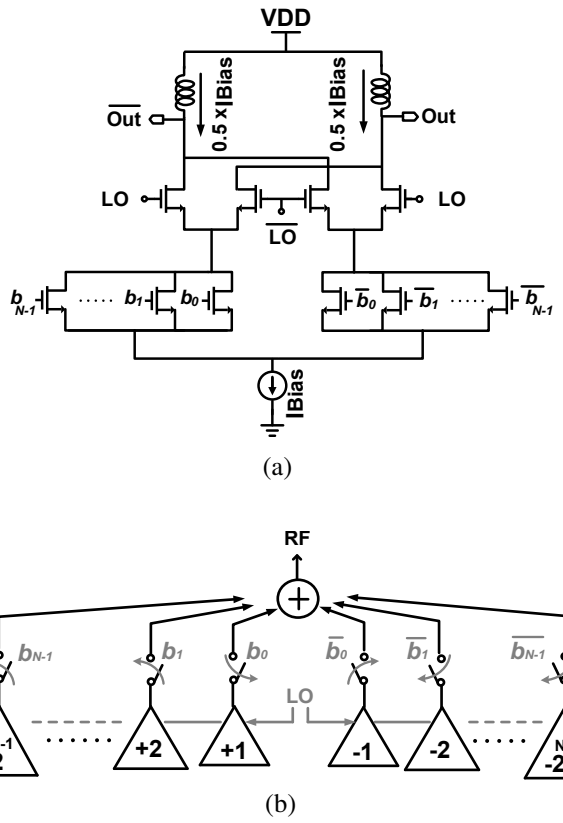


Figure 2.3: N-bit RF-DAC Design. (a) *N*-bit RF-DAC schematic design, (b) *N*-bit RF-DAC concept of operation.

LO Leakage

There are two sources that lead to LO leakage or carrier feedthrough in direct-conversion transmitters: IQ DC offsets in the modulator which translate into shifting in the origin point of the constellation diagram, and direct LO leakage from the LO to the RF port in the modulator - due to finite isolation between the two ports, or due to layout asymmetry in the upconversion mixer. LO leakage resulting from either source can be corrected for by applying a differential DC offset to the I and Q upconversion mixers. This requires a two-dimensional calibration, since the differential DC offsets required for the I and Q mixers are usually not equal [28].

For switching-mode modulators or RF-DACs, this can be achieved using digital predistortion by applying the appropriate digital words that represent the effect of a differential DC offset across the positive and negative terminals of the baseband switching stage in the modulator.

Typical LO leakage values at mm-wave frequencies range from -30 dBc to -24 dBc which translate to 3% - 6% $EVM_{rms,avg}$:

$$EVM_{rms,avg} = \sqrt{10^{LO_{lk}/10}} \tag{2.10}$$

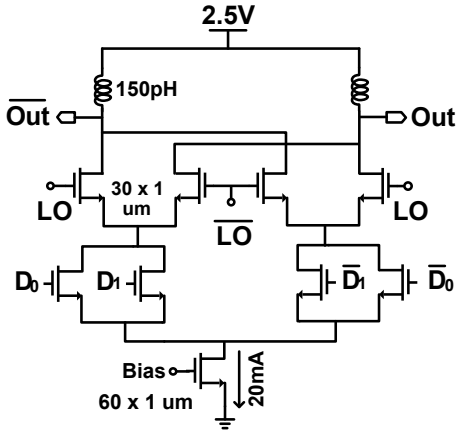
where LO_{lk} is the carrier leakage and is measured relative to the average power of the transmitted signal. The average transmitted power can be calculated using the peak-to-average power ratio (PAPR) of the corresponding m-QAM waveform. DC offsets in the receiver, resulting from LO leakage in the transmitter, can be removed with a high pass filter (e.g. DC block) or using digital baseband filtering. Nevertheless, LO leakage degrades the dynamic range of the transmitter and directly impacts its EVM and BER.

2.3 Building Blocks

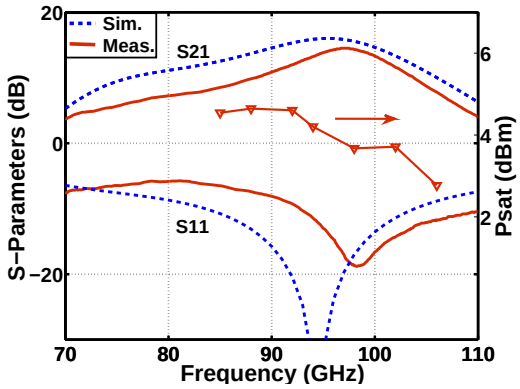
2.3.1 2-bit RF-DAC

A major performance limitation in the design of high-speed modulators is the dependency of the their input and output impedances on the digital codeword, which leads to distorting the output waveform at every switching event and, as a result, a degradation in the transmit EVM [12]. This work proposes the N-bit RF-DAC design shown in Fig. 2.3a to mitigate the aforementioned issue. The fixed current source at the bottom of the cell ensures that the biasing condition of the switching quad remains unchanged, thus fixing the output impedance of the RF-DAC, and making it independent of the digital-word transmitted [29].

For an N-bit RF-DAC, the switching transistors are size-segmented in a binary fashion. This is achieved in a single transistor layout by grouping the gate fingers into N groups with a progressively increasing number of fingers in each group that follows a binary 2^N sequence. For



(a)



(b)

Figure 2.4: 2-bit W-band RF-DAC. (a) schematic design of binary-weighted Gilbert cell, (b) simulated and measured small-signal gain S_{21}, input match S_{11}, and measured saturated output power P_{sat} of the entire transmitter chain (from LO port to RF port of Fig 2.1, without de-embedding).

N baseband inputs: $b_0, b_1, ..., b_{N-1}$, phase modulation is achieved by the switching of the most-significant bit b_{N-1}. Afterwords, amplitude modulation is achieved by switching the remaining bits $b_0, b_1, ..., b_{N-2}$. The RF-DAC output power can be written as

$$P_{out} = P_{sat} + 20log\left|\sum_{k=0}^{N-1} \frac{(-1)^{b_k}\, 2^k}{2^N - 1}\right| \tag{2.11}$$

where the sign bit b_{N-1} determines the phase of the output waveform, which can take

one of two values: 0° or 180°, and P_{sat} is the saturated output power. As an example, for a 4-bit RF-DAC, the minimum constellation symbol (occurs at 0001 or 1110) is approximately 24 dB below P_{sat} which is in agreement with the classical 6 dB per bit resolution in baseband DACs. As mentioned before, the dynamic range is limited by factors such as the SNR of the RF-DAC and the LO leakage.

The design shown in Fig. 2.3a, which is an alternative constant-current RF-DAC topology to the one presented in [10,12], allows the segmented transistors to be driven by the 1 V thin-oxide SOI CMOS transistors rather than the thick-oxide transistors, thus permitting the DAC to switch at higher speeds. Another advantage of this circuit is that allows the modulator to operate deep in saturation, without the need for back-off. Therefore, the switching quad transistors are driven differentially by an LO amplifier, and into saturation. Since it is not necessary to back-off to produce amplitude modulation, the modulator can be made efficient at peak output power.

This topology can be thought of as an outphasing amplifier (Fig. 2.3b), where the amplifiers are biased in Class-A and are 180° out-of-phase at all times, which leads to poor efficiency for any constellation outputs other than the peaks. It does, however, allow for the fastest operation since the output impedance is fixed and is not dependent on the digital-word, which would otherwise cause amplitude and phase distortion in the EVM constellation.

The 2-bit RF-DAC design implemented in this work is shown in Fig. 2.4a. Fig. 2.4b presents the simulated and measured small-signal parameters of the transmitter chain, along with the measured saturated output power of 3-5 dBm at 85-105 GHz. The S_{21} of the transmitter is measured by setting the digital input to a static value of ($D_0 = 1$, $D_1 = 1$), thus effectively enabling a single arm of the Gilbert cell. The output matching network of the modulator is reduced to low-Q shunt 150 pH inductors on both sides of the differential output. The minimal matching at the output of the RF-DAC is used to achieve the highest possible bandwidth with minimal gain ripple and phase distortion, at the expense of reduced output power and efficiency. Measurements show 6% peak efficiency for the modulator stage, and 1.6% efficiency for the

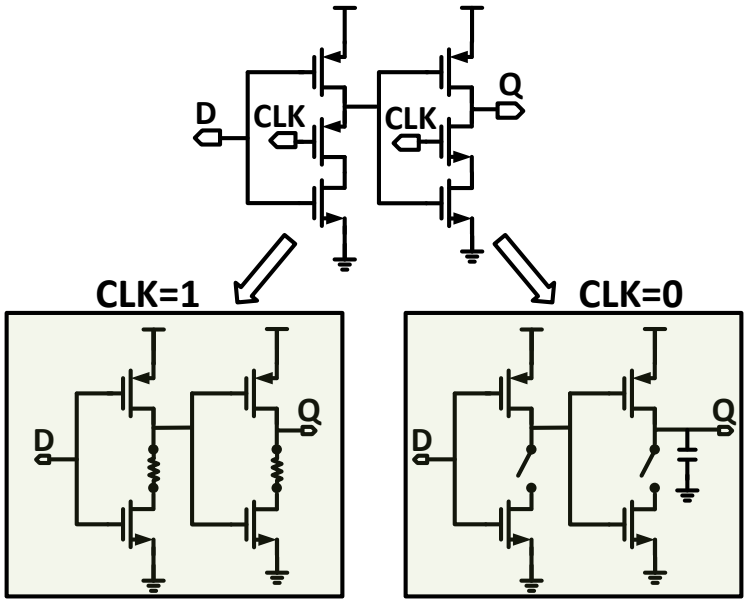


Figure 2.5: TSPC Latch concept of operation.

entire I/Q transmitter.

2.3.2 High-Speed Digital

The digital blocks are based on True Single-Phase Clocked (TSPC) logic [30, 31]. TSPC logic is capable of operating at higher speeds compared to static CMOS logic, and at a more moderate power consumption than the CML logic family.

TSPC Latch

The basic building block for TSPC logic is the latch shown in Fig. 2.5. When the CLK is high (1V), the latch is in the *transparent mode* and can be modeled as two inverters in series; and the input logic is buffered to the output. When the CLK is low (0V), both inverters are disabled, and the latch is in *hold mode*. Only the pull-up PMOS transistors are still active, while the pull-down NMOS transistors are disconnected. As a result, the latch output remains at the same logic level irrespective of the input logic *D*. An edge-triggered TSPC flip-flop can be built

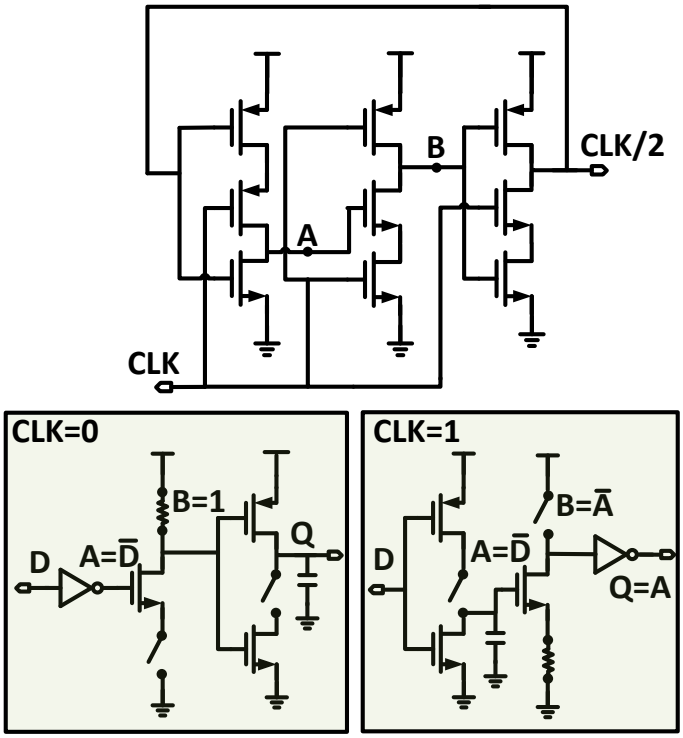


Figure 2.6: TSPC divider concept of operation.

by adding a second latch which is activated at the opposite clock level from the first latch. The flip-flop is used as a retimer to align all the high-speed baseband data with the respect to the clock.

TSPC Divider

The TSPC digital divider is consists of nine-transistors as shown in Fig. 2.6. A closer look at the circuit reveals that it resembles a flip-flop in feedback. When CLK=0, the three-transistor circuit from the input to node A is a negative D-latch with inverted output. When CLK=1, the six-transistor circuit from node A to the output is a positive D-latch. Therefore, with the feedback connection, the circuit is capable of dividing digital clocks at higher speeds than traditional CMOS digital dividers, due to the small capacitive loads arising from the low transistor count in the topology.

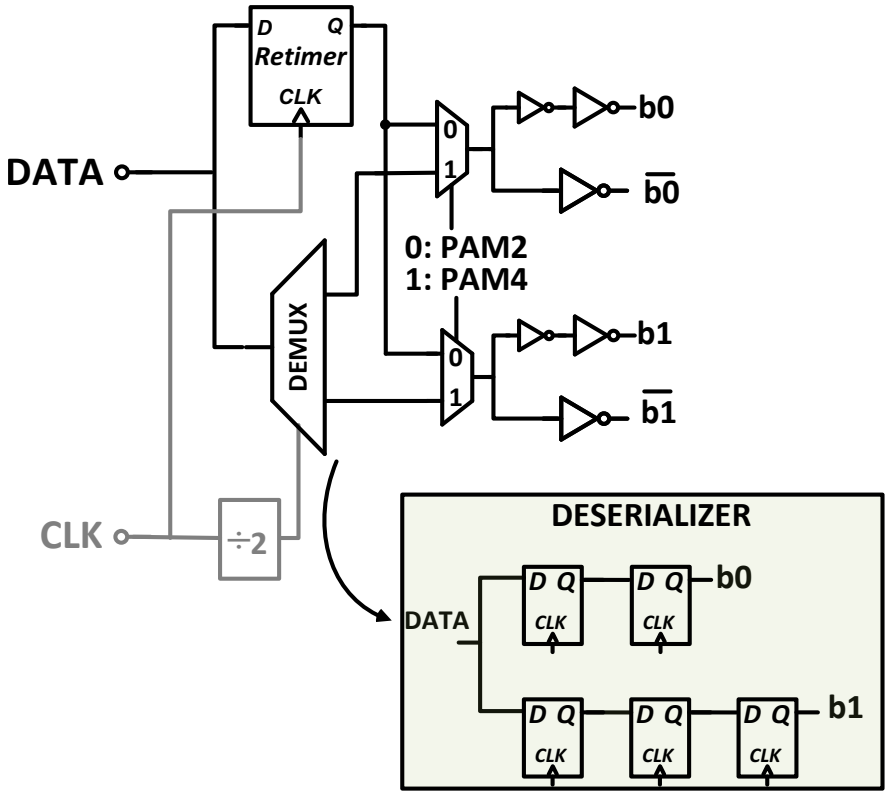
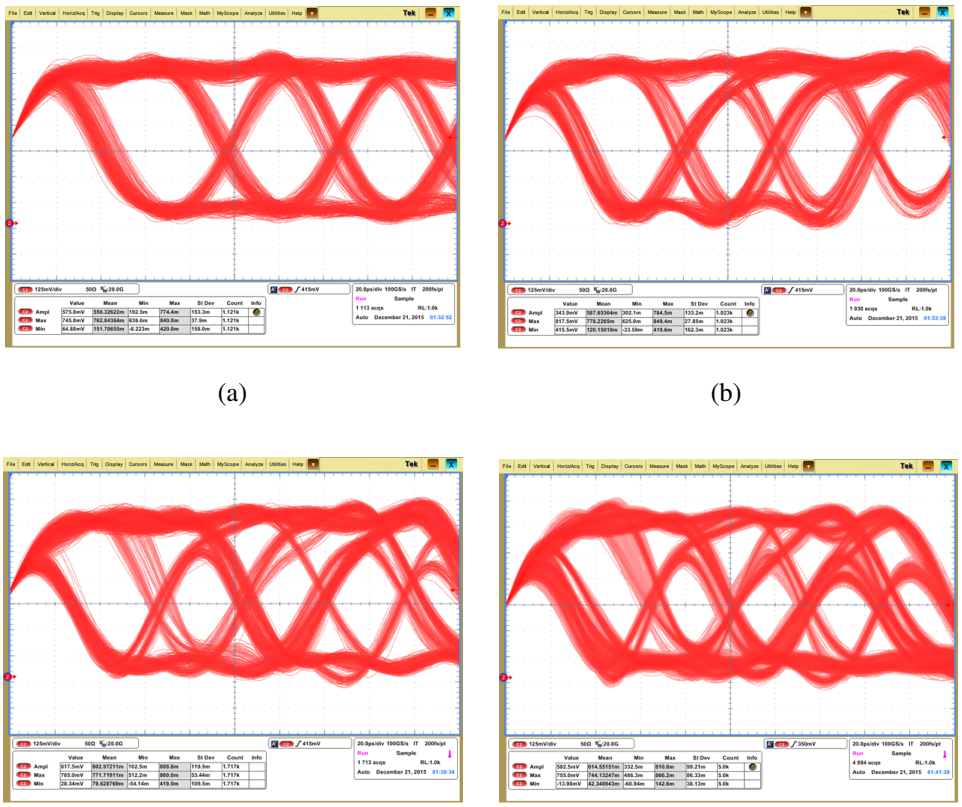


Figure 2.7: TSPC-based digital driver (retimer/deserializer) design.

Deserializer Design

To drive the baseband inputs of the 2-bit RF-DAC, NRZ PRBS data are fed into the chip from an external source. It is desirable to be able to dynamically change the operation mode of the RF-DAC and, consequently, the choice of the modulation format for the transmitter. The digital driver in Fig. 2.7 accepts an NRZ PRBS data stream and retimes it the with clock while - in parallel - also deserializes the incoming data into two streams, each at half of the data rate. Two switches select between passing the deserialized data, or passing the two identical retimed data streams which effectively turns the 2-bit RF-DAC into a one-bit RF-DAC. This capability allows the transmitter to seamlessly change its modulation scheme.

Measurement results in Fig. 2.8 and Fig. 2.9 show that the digital driver is capable of retiming and demultiplexing PRBS31 data streams faster than 30 Gbps and 20 Gbps, respectively.



(a) (b)

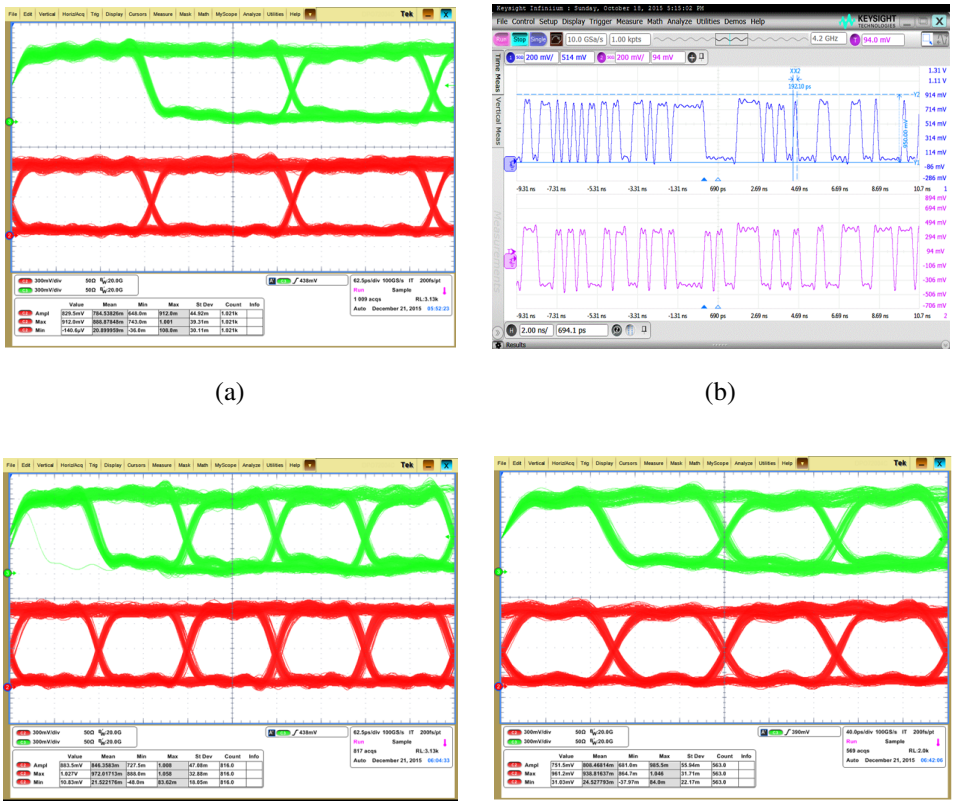
(c) (d)

Figure 2.8: Retimer eye diagram measurements: (a) 20 Gbps, (b) 24 Gbps, (c) 28 Gbps, (d) 30 Gbps.

This performance makes the digital blocks in this design sufficient to support 60 Gbps and 40 Gbps data rates in QPSK and 16-QAM operating modes in the transmitter.

2.3.3 W-band LO Driver

To drive the RF-DAC into saturation at reasonable LO power levels, the RF-DAC is preceded by an LO amplifier consisting of three differential cascode stages (Fig. 2.11). All the LO amplifier stages are biased in class-A and operate under saturation, so as to reduce the I/Q amplitude imbalance introduced by the I/Q coupler. Transistor sizes in each stage are incrementally increased by a factor of 1.5 to ensure saturating the amplifier stages while providing sufficient output power to drive the RF-DAC. Fig. 2.12 presents the simulated and measured



(a) (b)

(c) (d)

Figure 2.9: Deserializer measurements: (a) 10 Gbps, (b) real-time data at 10 Gbps, (c) 16 Gbps, (d) 20 Gbps.

S-parameters of the LO amplifier. Small-signal gain > 10 dB is obtained from 90-110 GHz with a peak gain of 20 dB at 100 GHz. The differential amplifier consumes 40 mW from a 1 V supply. To generate the quadrature signal, a 50 Ω-matched varactor-tuned transformer-based quadrature coupler [32] is used (Fig. 2.10). The accumulation-mode MOS varactors are externally controlled with analog voltages. Inevitably, the coupler produces quadrature amplitude errors which are corrected by the saturated LO amplifiers. Any AM-PM distortion resulting from saturating the driver amplifiers can be corrected by re-tuning the varactors.

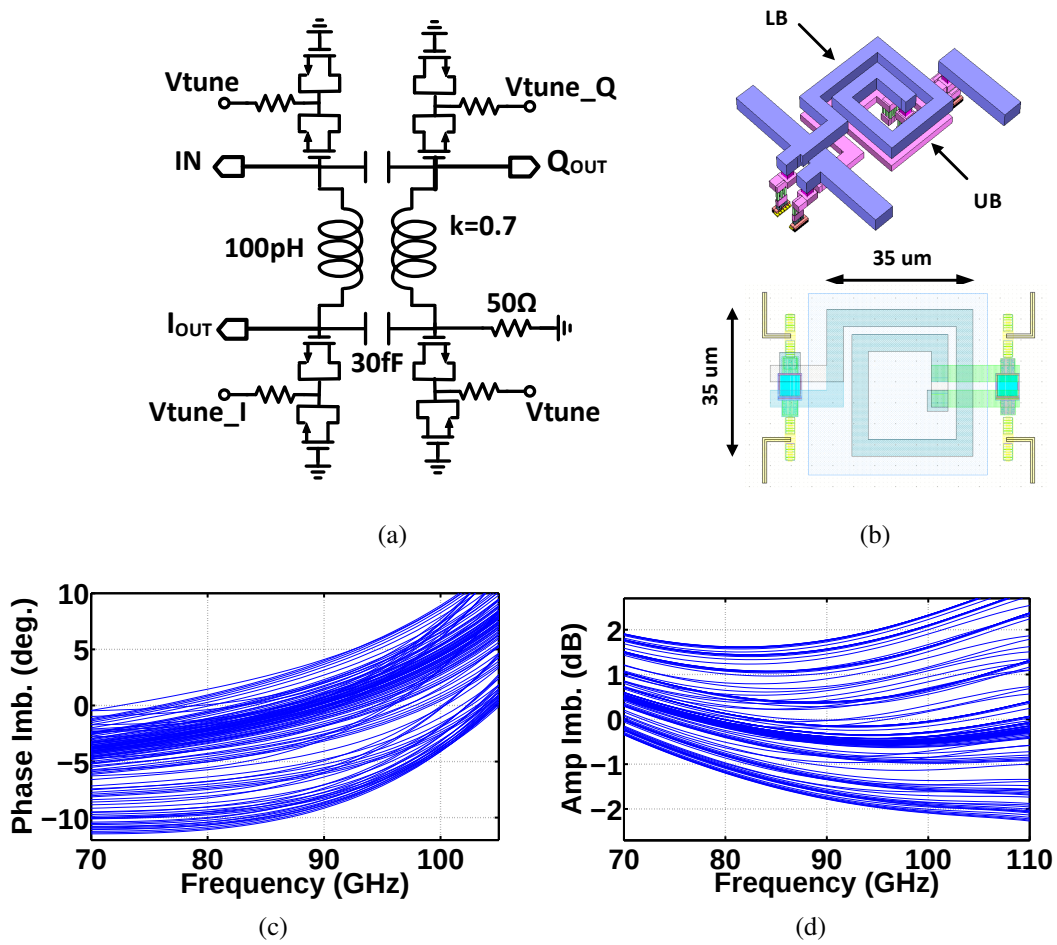


Figure 2.10: I/Q Coupler design. (a) schematic design of the transformer-based coupler, (b) IQ coupler layout (bottom) and EM-simulated structure (top), (c) simulated quadrature phase, and (d) amplitude imbalance across different varactor tuning settings.

2.3.4 W-band Wideband Receiver

This section discusses the design procedure for a wideband W-band receiver. Since the receiver is meant to be used in the feedback path (Fig. 2.1), it should be capable of downconverting and amplifying wideband modulated signals centered around any carrier frequency within the band. Ideally, the receiver will cover the entire W-band (75-110 GHz), within its 3-dB bandwidth.

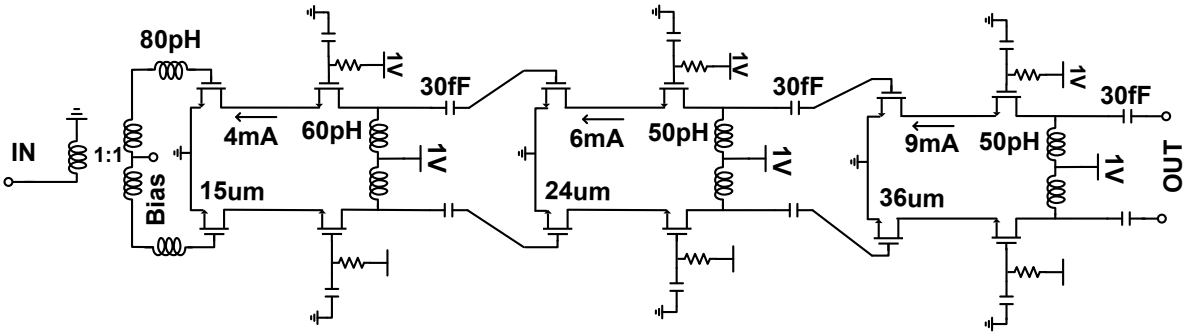


Figure 2.11: W-band LO amplifier.

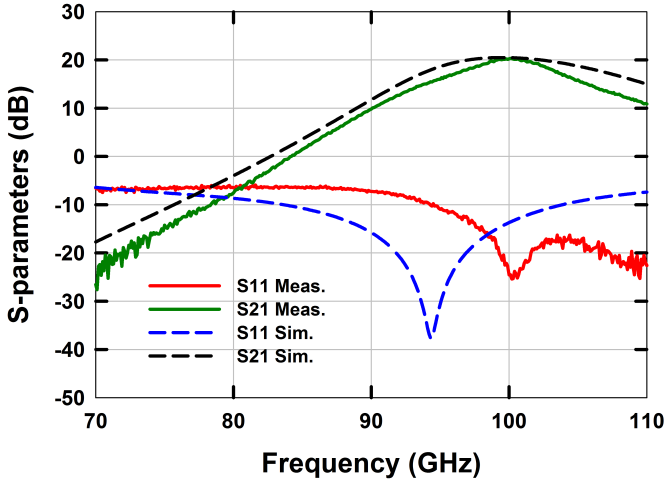
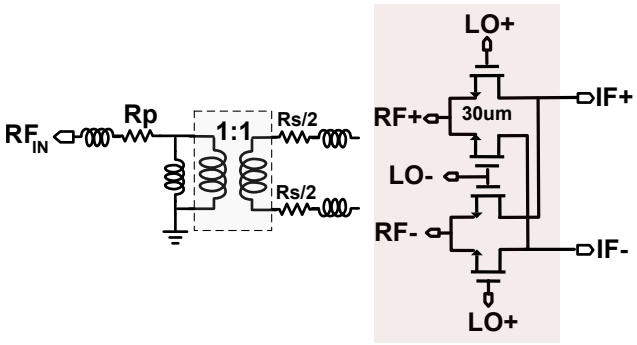


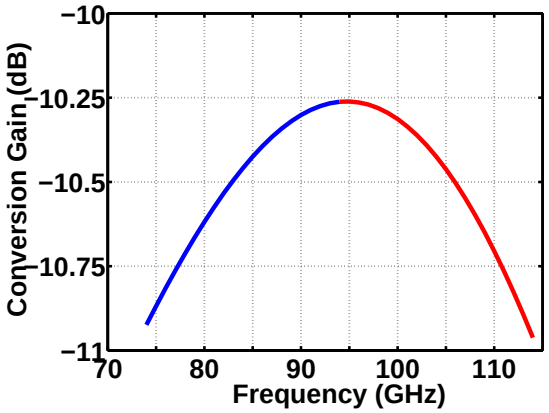
Figure 2.12: Measured and simulated LO amplifier S-parameters.

Wideband Passive Mixer

Passive mixers have become the standard design choice for RF receivers. This is due to the poor linearity of active mixers and their high $1/f$ noise, an issue which is exacerbated in short-channel devices as discussed earlier. Passive mixers offer superior linearity especially if their output is presented with a low impedance, forcing them to operate in current mode. Furthermore, they exhibit little $1/f$ noise, since no DC current flows through the devices, a useful feature for direct conversion systems. Passive mixers at mm-wave frequencies, however, are not as common due to their high conversion loss. A passive mixer is employed in this work, motivated by the low on-resistance of the devices in 32 nm SOI, and by the inherently wider bandwidth



(a)



(b)

Figure 2.13: W-band passive mixer. (a) Passive mixer schematic including the input matching balun, (b) simulated mixer conversion gain, showing symmetric gain around 94 GHz and a 3-dB bandwidth greater than 30 GHz.

offered by passive mixers when compared to active mixers. Assuming the parasitic capacitance of the switches resonate with the inductance presented by the input balun (Fig. 2.13a), and since it is not possible to generate a square LO waveform at W-band frequencies, the single-ended input impedance for the passive mixer architecture can be expressed as [33]

$$Z_{in}(\omega) \simeq R_{SW} + \frac{1}{16}\left(Z_{TIA}\left(\omega - \omega_{LO}\right)\right) \tag{2.12}$$

where R_{SW} is switch on-resistance and Z_{TIA} is the input impedance of the transimpedance amplifier . The impedance looking into the receiver is then

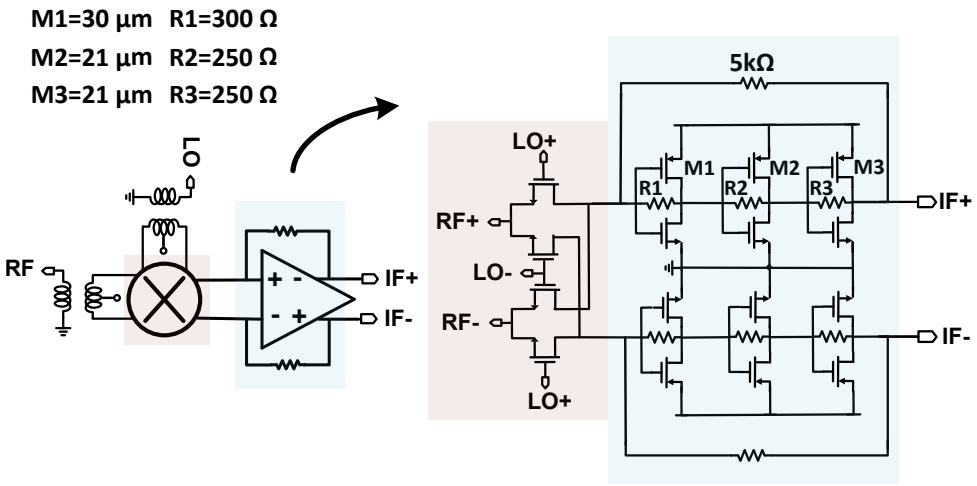


Figure 2.14: W-band receiver design, consisting of a passive mixer (left) and 3-stage CMOS-inverter TIA.

$$Z_{in,RX}(\omega) = R_p + R_s + 2Z_{in}(\omega) \tag{2.13}$$

where the factor of 2 accounts for the differential input impedance of the passive mixer, which is dominated by the switch resistance. In fact, it is desirable to choose the switches sizes such that $Z_{in,RX}(\omega) \sim 50\ \Omega$ to achieve a wideband impedance match. It is also desirable to reduce the contribution from the TIA input impedance, that is to suppress the image current appearing $\omega_{LO} - \omega_{RF}$. The impedance created at the image can cause different high- and low-side conversion gains [33] - an unwelcome effect as discussed in section 2.2.4. For $L_p = L_s \sim 250$ pH, which are the inductor values needed to resonate out the reactive part of the mixer input impedance, and for a quality factor $Q = 12$ at 90 GHz, then $Z_{diff}(\omega) \sim 24\ \Omega$ is needed. This translates into $R_{SW} \sim 12\ \Omega$ or a 30 μm device width in 32 nm SOI including layout parasitics. The mixer conversion gain simulation in Fig. 2.13b shows 10 dB of loss over the entire bandwidth, with symmetric upper- and lower- sideband gains around 94 GHz carrier frequency. The high conversion loss is expected, since about 3.9 dB of loss arises from the mixing operation [34], and an additional loss of ~ 3 dB is attributed to the on-resistance of the switches which form a voltage divider with the TIA input resistance leading to $10log_{10}(\frac{Re\{Z_{TIA}\}}{R_{SW}+Re\{Z_{TIA}\}})$ of loss and ~ 2

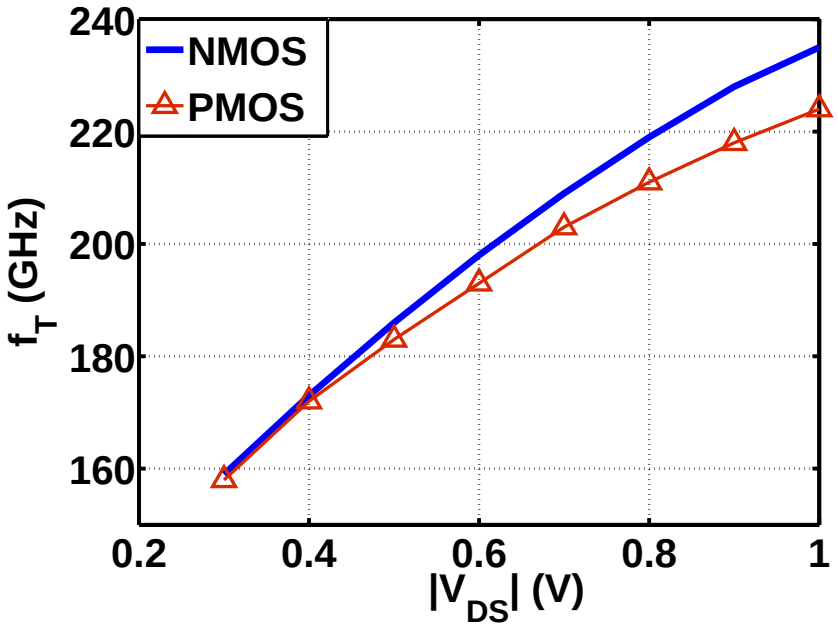


Figure 2.15: Cadence simulation of the transition frequency f_T of 30 µm NMOS and PMOS devices in 32 nm CMOS SOI, including all the parasitics up to the top metal layer.

dB loss of the input balun. Furthermore, if there is time period t_{ov} where both switches are on, (i.e. overlap in the differential driving), then the conversion gain is degraded by $20log_{10}(cos\frac{\pi t_{ov}}{T_{LO}})$ [35]. The switching transistors are biased near threshold (0.3V) to minimize t_{ov} without significantly increasing the required LO power to fully switch on the transistors. The simulated mixer IP1dB is +13 dBm, which allows the mixer to sample a high dynamic-range signal without distortion.

Wideband IF-Amplifier

Traditionally, PMOS devices needed to be sized larger in order match the transconductance of NMOS devices for a given bias current, which increased the output capacitance and consequently affected the bandwidth of the CMOS inverter design. Another concern with the inverter is the smaller available voltage headroom, since the devices are biased at half the supply voltage. The closing gap in speed between NMOS and PMOS devices [36] led to the revival of the CMOS inverter stage (Fig. 2.14). Moreover, the simulation in Fig. 2.15 reveals that both the NMOS and PMOS devices in 32 nm CMOS SOI maintain a high f_T as the drain-source

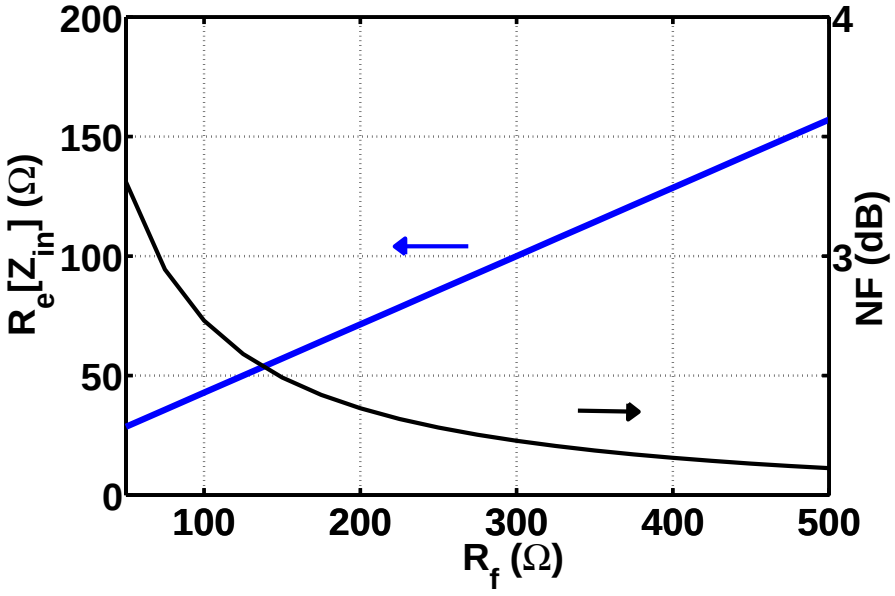


Figure 2.16: Simulation of noise figure and input impedance of a single CMOS inverter stage, based on (2.15).

voltage V_{DS} is reduced, as long as the device remains in saturation. This is in agreement with the observation that nanoscale FETs have weak dependence on V_{DS} as long as they are biased at peak f_T condition (0.2-0.4 $mA/\mu m$) [37].

The inverter also offers a superior linearity performance when compared to an NMOS stage with a resistive load, since the combination of the NMOS and PMOS devices help maintain a constant transconductance for different input swings. Furthermore, the inverter leads to the same noise for half the bias current, since the additional noise by the PMOS device is suppressed by an increased effective transconductance $g_{m.eff} = g_{m,p} + g_{m,n}$. The noise figure of a single inverter stage is given by [35]

$$F = 1 + \left| \frac{R_f + Z_{in}}{g_m R_f + 1} \right|^2 \frac{\gamma g_m + 1/Z_L}{Re\{Z_{in}\}} \tag{2.14}$$

where R_f is the feedback resistance, Z_{in} is the input impedance and Z_L is the load impedance. Recognizing that $g_m R_f \gg 1$, and assuming $\gamma = 1$, with some mathematical manipulation, the expression can be simplified to

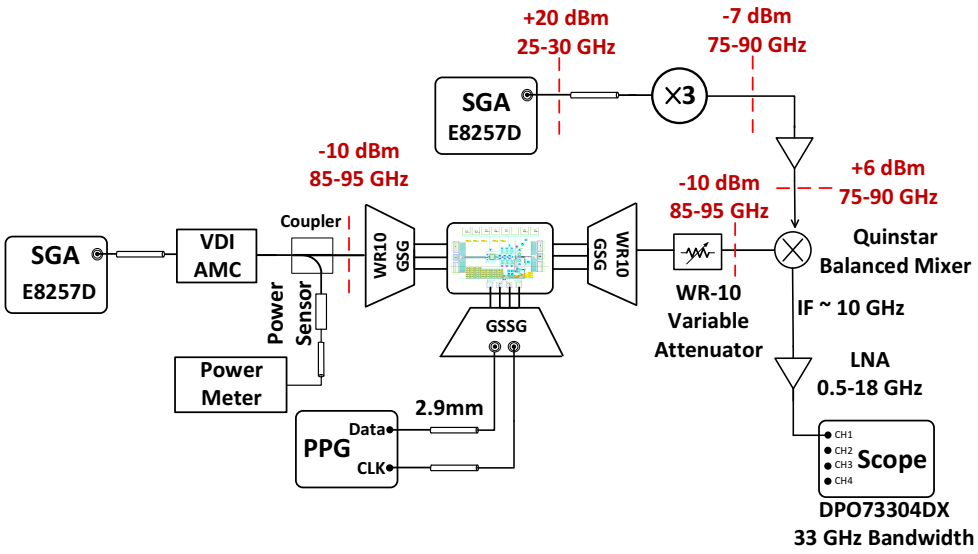


Figure 2.17: RF-DAC measurement setup.

$$F = 1 + \left|1 + \frac{R_{in}}{R_f}\right|^2 \frac{R_L + 3/g_m}{R_f} \tag{2.15}$$

Fig. 2.16 shows that the optimum feedback resistor value is 300 Ω, for a $g_m = 0.05\ S$ and $Z_L = 50\ \Omega$, while maintaining S_{11} > -10 dB. This results in a simulated gain and NF of 8 dB and 2.3 dB, respectively. For a three inverter stages design, we expect:

$$F \approx F_1 + F_2/(g_{m1}^2 Z_{in1} Z_{in2}) \tag{2.16}$$

where the power gain of the first stage is $g_m^2 Z_{in1} Z_{in2}$. Equation (2.16) predicts a 3.3 dB NF for the TIA, with overall gain S_{21} > 20 dB. Cadence simulations show a minimum NF value of 3.5 dB. The discrepancy at higher frequencies can be attributed to ignoring the effects of the reactive elements such as C_{gs} and C_{gd} in the matching networks, leading to optimistic predictions from the analysis. Inductors can be used at the input and output matching networks to resonate out the capacitances. No resonant elements are used in this particular design in favor of compactness and to maintain a wide bandwidth.

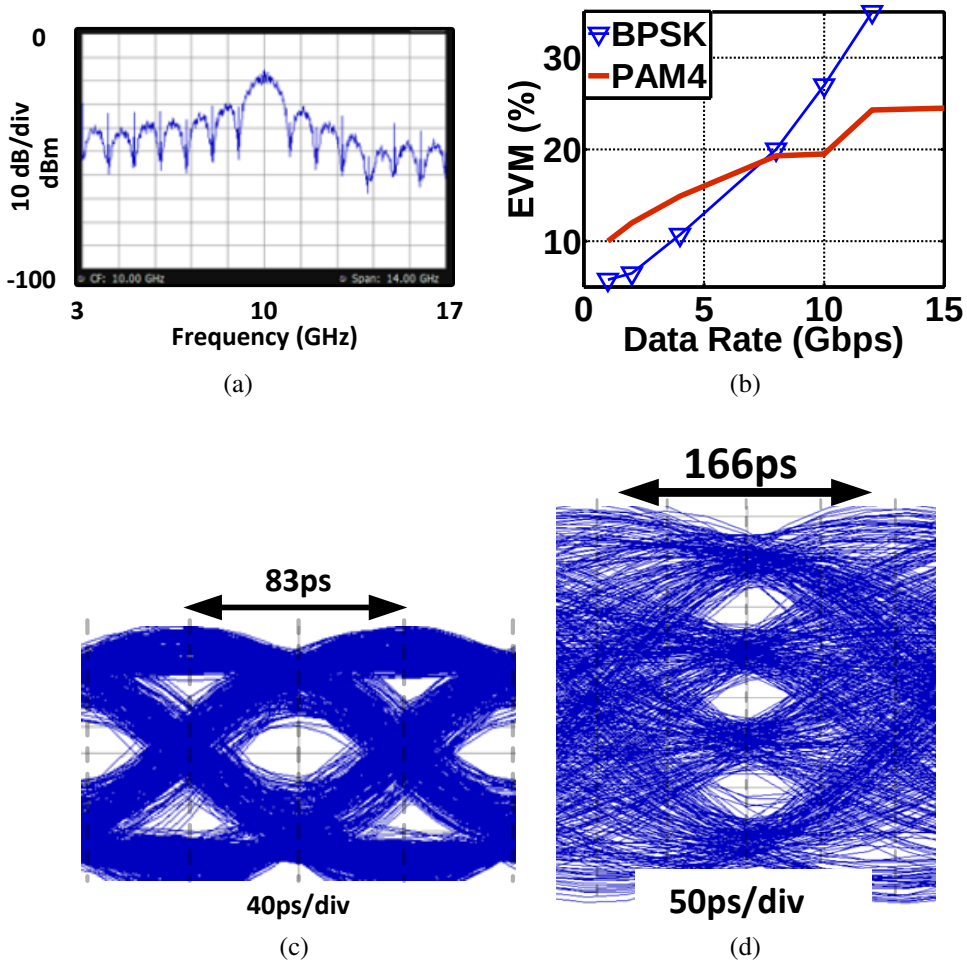


Figure 2.18: RF-DAC measurements. (a) 1 Gbps BPSK oscilloscope output spectrum, (b) EVM vs. data rate measurement results for the 2-bit RF-DAC, (c) 12 Gbps BPSK eye diagram, (d) 12 Gbps PAM4 output.

2.4 Measurements

2.4.1 RF-DAC Measurements

A breakout of the RF-DAC shown in Fig. 2.4a was measured by applying an external W-band LO signal using the VDI AMC-335 multiplier chain through a WR-10 waveguide probe (Fig. 2.17). The PRBS31 data and clock input are obtained from a Tektronix 30 Gb/s two-channel programmable pattern generator PPG3002. The modulated RF output is then downconverted using an external Quinstar QMB waveguide balanced mixer to a 10 GHz IF. The modulated IF

output is then directly applied to a real-time 100 GS/s DPO73304DX Tektronix scope with 33 GHz of analog bandwidth. The constellation diagram, frequency spectrum, and eye diagrams are then observed using the SignalVu VSA software.

Fig. 2.18a presents a 1 Gbps RF-DAC output spectrum in PAM2/BPSK mode, after downconversion to 10 GHz, over 14 GHz frequency span. The spectrum follows the sinc function discussed earlier, with clear nulls at multiples of the 1 GHz sampling clock. Fig. 2.18c and Fig. 2.18d present the eye diagrams at maximum data rates obtained in PAM2/PAM4 modes, both at 12 Gbps, with an SNR of 9 and 13 dB, respectively. Fig. 2.18b gives a summary of the measured EVM in BPSK and PAM4 modes, for different data rates.

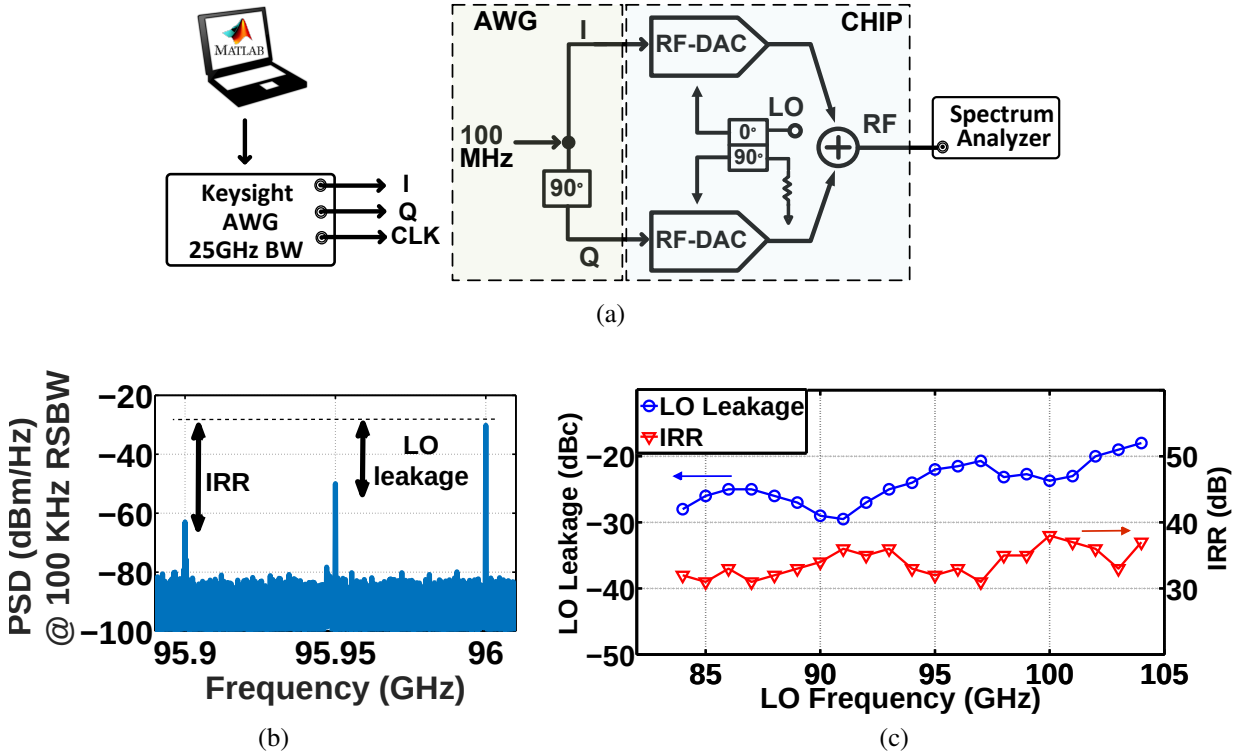


Figure 2.19: SSB transmitter measurement setup. (a) Hartley modulator setup, (b) screenshot from the spectrum analyzer highlighting IRR and LO leakage at 96 GHz (after downconversion), (c) IRR and LO leakage at different carrier frequencies showing an increasing carrier leakage with frequency.

2.4.2 Transmitter Measurements

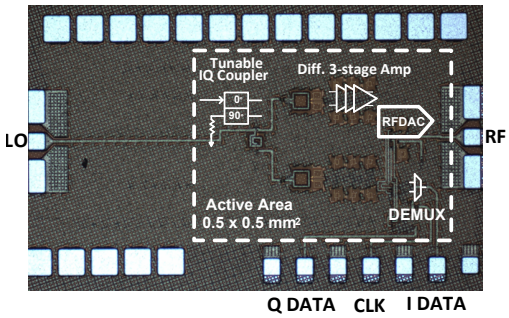
Evaluating Transmitter Impairements

The measurement setup in Fig. 2.19a depicts the I/Q transmitter configuration as a single-sideband (SSB) transmitter, to evaluate the quadrature phase and amplitude imbalance, by means of measuring the sideband suppression or image rejection ratio (IRR) of the SSB transmitter. A 100 MHz tone is generated using an arbitrary waveform generator (AWG) that is controlled in software by Matlab, such that the first channel of the AWG generates the 100 MHz sinusoidal tone and the second channel generates the Hilbert transform (quadrature signal in the case of a single tone) of the signal in channel 1. The two channels are synchronized and phase adjusted such that the two quadrature signals arrive at the I and Q input data pads of the die with correct phases. The output of the transmitter is then downconverted to an intermediate frequency in order to display the output spectrum on a spectrum analyzer. Fig. 2.19b depicts an example spectrum where the lower sideband is suppressed, and the IRR and LO leakage can be readily calculated.

Fig. 2.19c shows the measured sideband suppression and LO leakage as a function of the LO frequency. Sideband suppression is measured by tuning the varactors of the I/Q coupler presented in section 2.3.3 each time the LO frequency is changed, in order set the optimum coupler tuning voltages that achieve the highest sideband suppression value. SSB suppression better than 30 dB over the entire band is achieved. Furthermore, Fig. 2.19c shows that the LO leakage can vary from -30 dBc to -18 dBc, which can lead to a worst case $EVM_{rms,avg}$ of approximately 13% (2.10). Additionally, measurements demonstrate that the carrier feedthrough shows an increasing trend with the carrier frequency. This is to be expected since the capacitive coupling through the gate-drain capacitance in the switching quad transistors becomes the dominant mechanism for the leakage at mm-wave frequencies.

Digital I/Q Modulator Measurements

A similar measurement setup is used to measure the I/Q transmitter chip (Fig. 2.20a). Two PRBS data sequences representing I/Q data and a full-rate clock are obtained from the PPG and enter the chip through a 50 GHz GSGSGSG probe, using 2.4 mm coaxial cables. External wideband phase shifters are used to compensate for any phase mismatch between the different cables.



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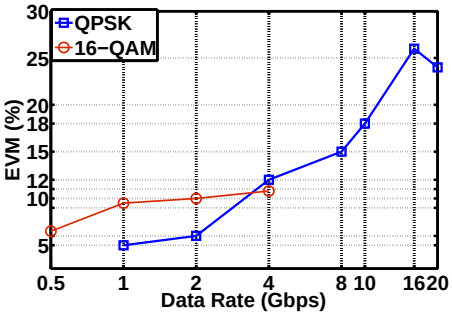

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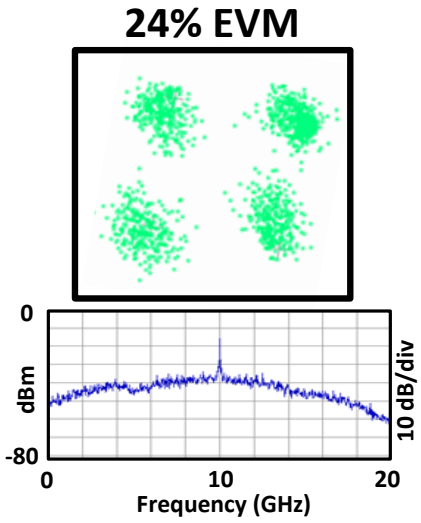

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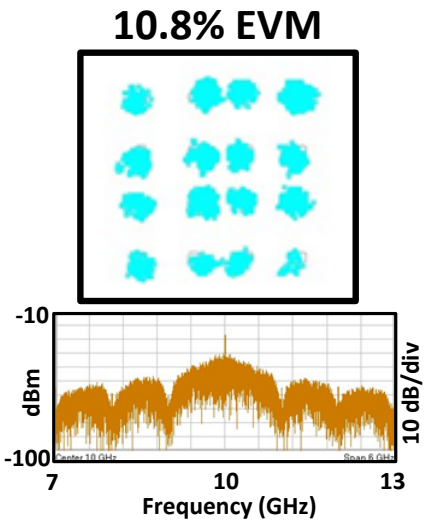

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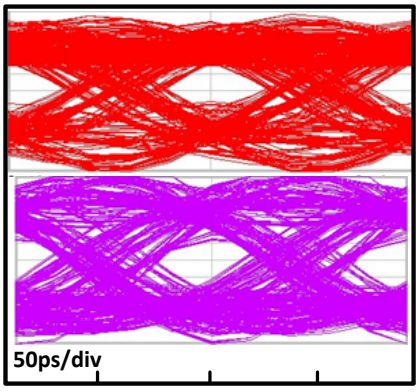

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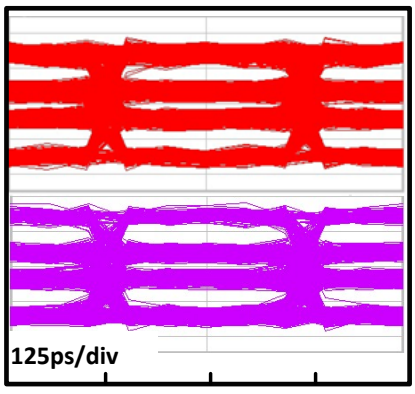


(f)

Figure 2.20: Transmitter measurements. (a) 32nm SOI transmitter chip micrograph, (b) QPSK and 16-QAM data rate measurements, (c) EVM and frequency spectrum for 20 Gbps QPSK, (d) EVM and frequency spectrum for 4 Gbps 16-QAM, (e) captured 10 Gbps I and Q eye diagrams during the 20 Gbps QPSK operation, (f) 2 Gbps I and Q eye diagrams for 4 Gbps 16-QAM.

Fig. 2.20 presents QPSK and 16-QAM real-time EVM, constellation and eye diagram measurements for a 95 GHz LO carrier, at different data rates and up to a maximum of 20 Gbps in QPSK and 4 Gbps in 16-QAM. At 20 Gbps QPSK, the RF output occupies 20 GHz of bandwidth (85-105 GHz) and is downconverted with an 85 GHz LO source to a 10 GHz IF. The constellation shows an EVM of 24%, which corresponds to 3e-5 of expected BER value (Fig. 2.2). This is, to our knowledge, the highest data rate ever reported for a digital CMOS transmitter below 100 GHz. In 16-QAM mode, the peak data rate is 4 Gbps with 10.8% EVM or an estimated BER of 8e-4, if an SNR-limited EVM is assumed. The eye diagrams shown in Fig. 2.20f reveal an unequal spacing between the amplitude levels, which indicates that the output power of the RF-DAC deviates from (2.11). This is due to the strongly non-linear behaviour of the modulator under saturation and also due to the limited isolation between the I and Q paths which degrades the EVM and the effective number of bits of the I and Q RF-DACs to less than two bits per DAC. The transmitter has 4 dBm of output power and consumes 220 mW. Table 2.1 presents a comparison with state-of-the-art W-band transmitters in silicon.

In order to test the transmitter performance in a practical physical link setting, the setup in Fig. 2.21 was constructed. The output of the transmitter was connected to a a WR-10 waveguide horn antenna through a waveguide probe. A waveguide-based W-band receiver connected to another horn antenna was placed half-meter away from the transmitter, and in its line of sight (Fig. 2.22a). The down-converted IF output was then connected to a real-time scope, and the EVM values for QPSK constellations at different data rates were measured. As expected, the maximum data rate fell to 12 Gbps (Fig. 2.22b), limited by the SNR of the link.

Table 2.1: Comparison with mm-Wave Transmitters Below 100 GHz In Silicon-Based Technologies.

Reference	**[10]**	**[11]**	**[32]**	**[38]**	**[39]**	**[29]**	**[40]**	**[41]**	**[42]**	**This Work**
Technology	45 nm SOI	40 nm CMOS	0.18µm BiCMOS	65 nm CMOS	45 nm SOI	0.13µm BiCMOS	65 nm CMOS	40 nm CMOS	45 nm SOI	32 nm SOI
Frequency [GHz]	90	60	88	68/102	94	77	60	78.5	100	94
Modulation	ASK OOK	QPSK 16QAM	16QAM 32QAM	16QAM	64QAM	QPSK	QPSK 16QAM	64QAM	QPSK 9QAM	BPSK PAM4 QPSK 16QAM
Integration Level	On Wafer	On Wafer	Antennas and Die on a PCB TX+RX phased array	WG Horn Antenna TX+RX	Thru-silicon WG	TX+RX (Loop back)	Antennas and Die on a PCB	On Wafer	Antennas on Die	On Wafer
Peak Data Rate [Gbps]	15	3.5/7	10/8.75 (1 m link) (Ext. AWG)	56 (Ext. AWG)	1	18	3.5/6	3	10/4 (189 mm link)	12/12 20/4
Pout [dBm]	19	5.3	> 6	-8.4	> 10	9	9.6	12	16.9	4
TX Power Consumption [W]	0.89	0.04*	0.25	0.26	2.1 (0.8*)	~ 0.4	0.38	0.1	1.27/ 0.93	0.11/ 0.22

* RF-DAC/PA core power consumption only.

2.4.3 Receiver Measurements

TIA Measurements

The S-parameters of the CMOS inverter-based TIA, presented in section 2.3.4, were measured with a VNA up to 67 GHz. The results are shown in Fig. 2.23a. The TIA exhibits 22 dB of peak gain and a small-signal 3-dB bandwidth of 25 GHz. Using a Keysight 346C (10 MHz - 26.5 GHz) noise source and E4448A spectrum analyzer, the noise figure was also measured (Fig. 2.23b). Measured noise figure is $\backsim$1 dB higher than simulated, which is attributed to the inaccuracy of the transistor noise model. The high noise figure at DC frequencies is due to flicker noise and the AC coupling used, while the noise figure increase at higher frequencies is predicted

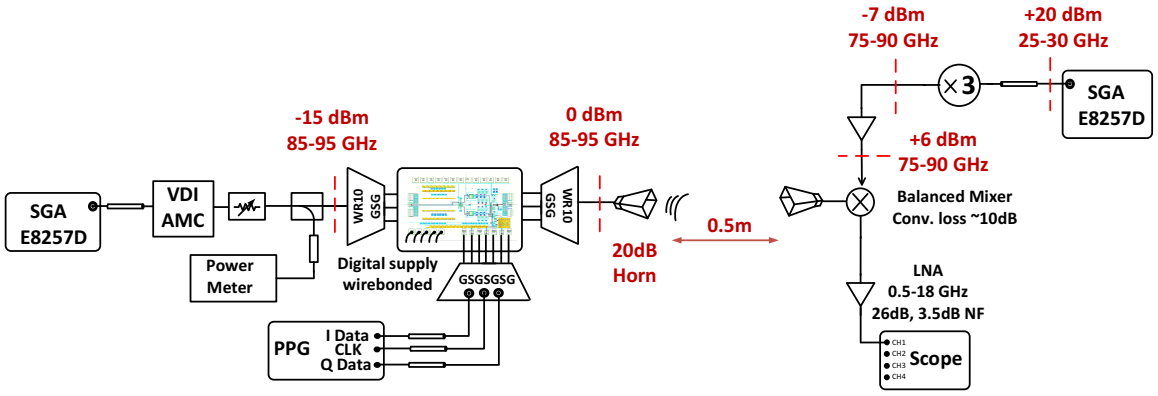
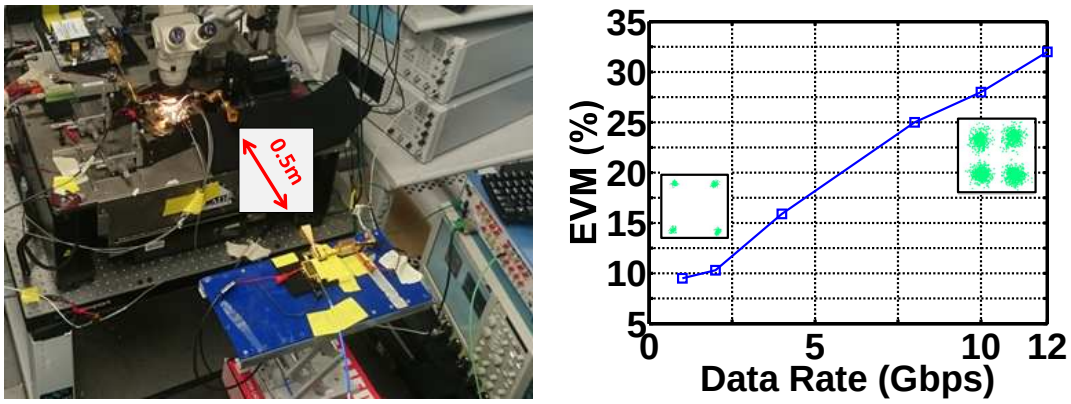


Figure 2.21: 0.5-meter link measurement setup.



(a) (b)

Figure 2.22: Transmitter measurements for a 0.5-meter link. (a) Measurement setup photograph, (b) 0.5-meter QPSK link measurement results.

by equations (2.15-2.16) since the effective input impedance decreases (Fig. 2.16). Furthermore, large-signal probe measurements revealed an OP1dB of 0 dBm. The TIA consumes 18 mW from a 1 V supply.

Simulated and measured group delay (Fig. 2.23c) show good agreement and a flat group delay response up to 60 GHz. Using (2.7), the group delay is expected to lead to 0.2° rms phase error or an equivalent degradation in EVM of 0.35%. No signifcant gain ripple is observed, and therefore the maximum baud rate supported by the TIA is limited by its 3-dB bandwidth.

Moreover, eye diagram measurements were carried out, to further validate the measurement results of the TIA noise figure, gain and bandwidth. A 65 GSa/s Keysight M8195A arbitrary

waveform generator was used to generate multi-level baseband signals that are fed to the TIA. The TIA output was then connected to a 33 GHz Keysight real-time oscilloscope, and the eye diagrams were captured in Fig. 2.24. Good eye openings were obtained up to 40 Gbps with NRZ input waveforms and 30 Gbps with PAM-4.

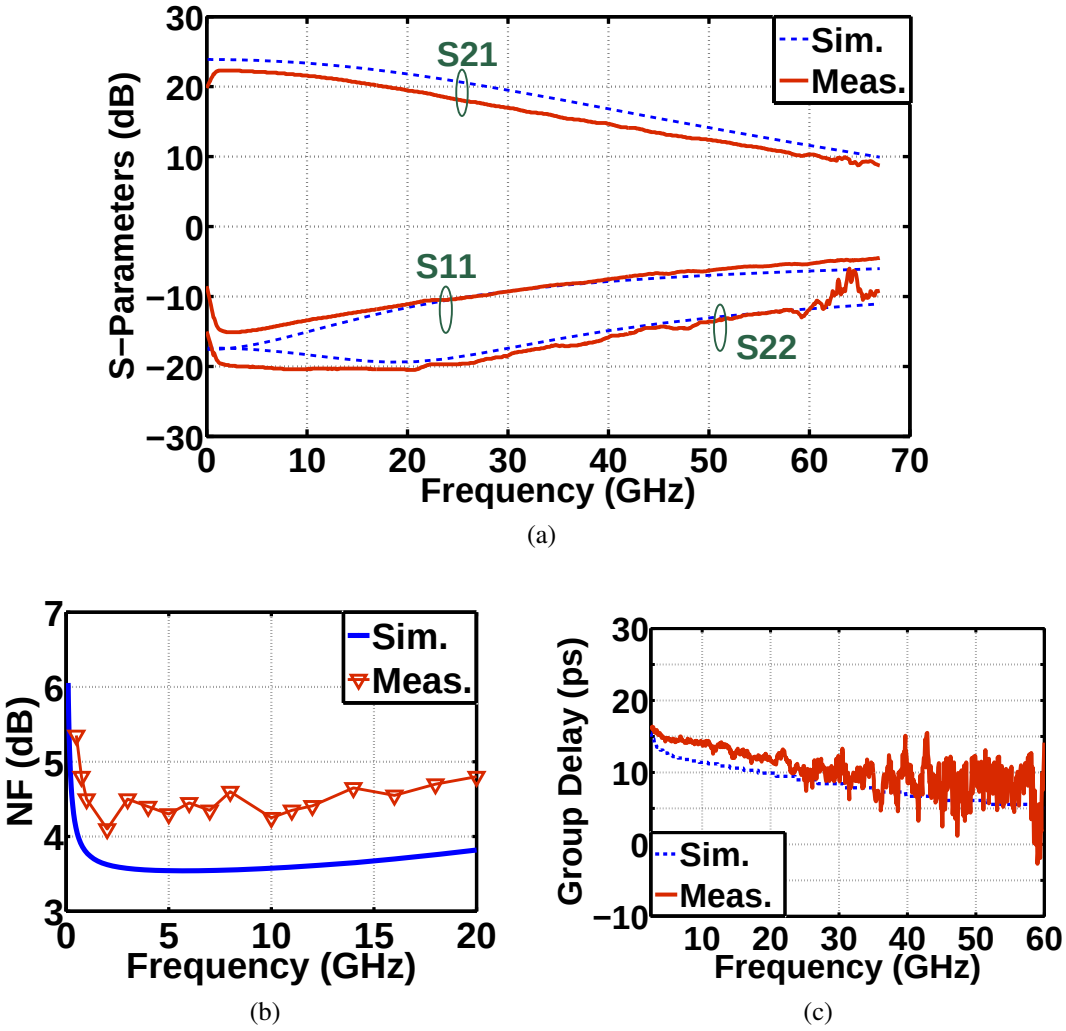


Figure 2.23: TIA measurements. (a) S-parameters up to 67 GHz, (b) noise figure, (c) group delay measurement.

Receiver Measurements

A breakout test cell of the receiver in Fig. 2.14 was measured. The receiver is comprised of the wideband passive mixer and the wideband TIA discussed earlier, and is therefore expected to have a sufficiently wide bandwidth to cover the entire W-band. To verify, the conversion gain was first measured (Fig. 2.25a). The measurement reveals that the receiver exhibits a very wide (> 30 GHz) bandwidth with approximately 10 dB of conversion gain. The ripple in the measured conversion gain is a measurement artifact, and is due to measurement uncertainties in the power meter reading and in the output power of the W-band VDI multiplier used to generate the input RF signal. Furthermore, the noise figure was measured (Fig. 2.25b), and large-signal measurements reveal a -10 dBm input P1dB, limited by the TIA.

In order to prove that the receiver has sufficient bandwidth and dynamic range to down-convert wideband modulated signals, as intended in the system proposed in Fig. 2.1, modulated QAM signals are generated using the arbitrary waveform generator M8195A at an IF of 10 GHz, the output is mixed with an 85 GHz signal and the RF signal centered at 95 GHz is fed into the RF input of the receiver. The signal is then downconverted and amplified using the on-chip receiver. The receiver capable of downconverting > 50 Gbps PRBS9 data sequence with low EVM values. EVM measurements are shown in Fig. 2.26.

It is worth noting that the phase noise of a continuous wave (CW) signal from the Keysight E8267D signal generator used in the experiments is ~ -110 dBc/Hz at 100 KHz offset, in the 10-20 GHz frequency region [43]. This imposes a lower EVM limit of approximately 1% (2.9), where the multiplication factor $N = 8$ to arrive to W-band frequencies. This leads to a BER close to or greater than 1e-3 for 1024-QAM or higher order m-QAM modulation schemes. For reference, 1024-QAM and 2048-QAM constellation measurements are shown in Fig. 2.26e and Fig. 2.26f at 10 Gbps and 5.5 Gbps, respectively, with 1e-2 expected BER values.

2.5 Conclusion

A state-of-the-art W-band transmitter and receiver chips using 32 nm CMOS SOI were presented. The 94 GHz transmitter consists of two current-combined RF-DACs that are driven in quadrature, and is capable of supporting multiple modulation schemes including BPSK, PAM4, QPSK and 16-QAM with max. data rates of 12, 12, 20 and 4 Gbps, respectively, all with EVM values that are expected to achieve $< 10^{-3}$ of uncoded BER. The receiver chip demonstrated greater than 30 GHz of bandwidth enabled by a wideband passive mixer and a CMOS-inverter based TIA design. Receiver measurements proved its capability to support highly complex modulated waveforms (> 256-QAM) and at very high data rates, up to 60 Gbps in 64-QAM. Future work may include increasing the resolution of the mm-wave RF-DACs, in order to support more spectrally-efficient modulation formats, and to implement digital predistortion and filtering.

2.6 Acknowledgment

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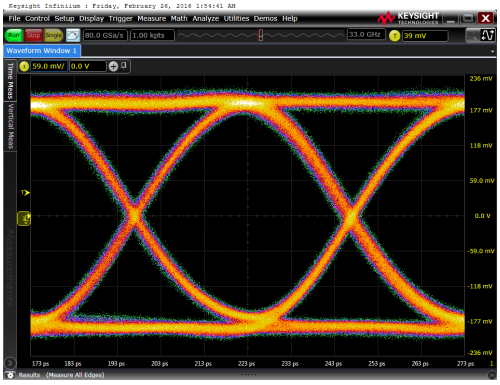
Chapter 2, in full, is a reprint of the material as it appears in: H. Al-Rubaye and G. M. Rebeiz, "W-band direct-modulation $>$ 20-Gb/s transmit and receive building blocks in 32-nm SOI CMOS", *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2277-2291, Sep. 2017. The dissertation author was the primary investigator and author of this paper.



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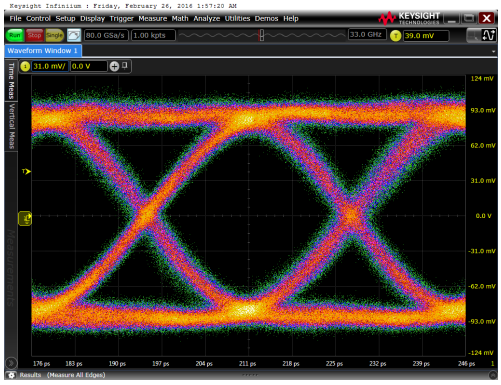

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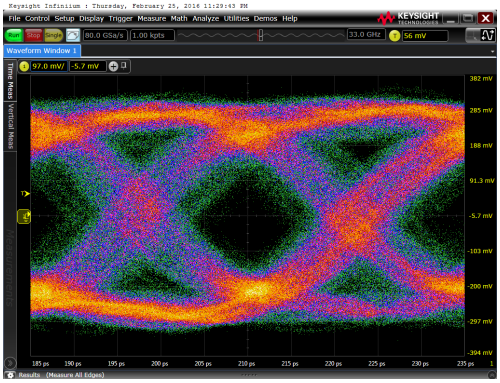

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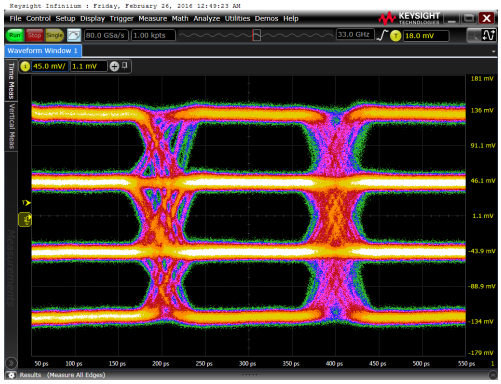

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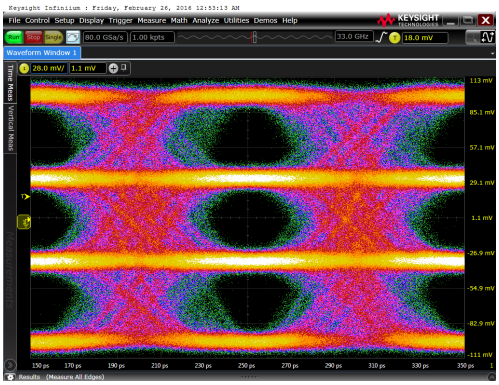

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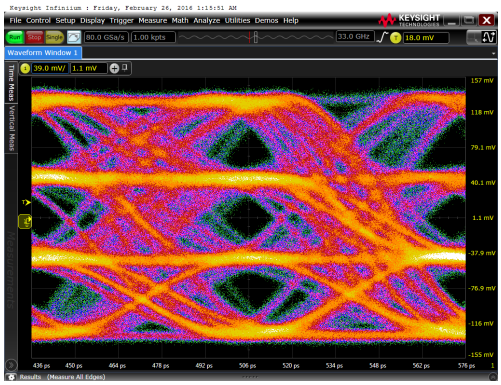
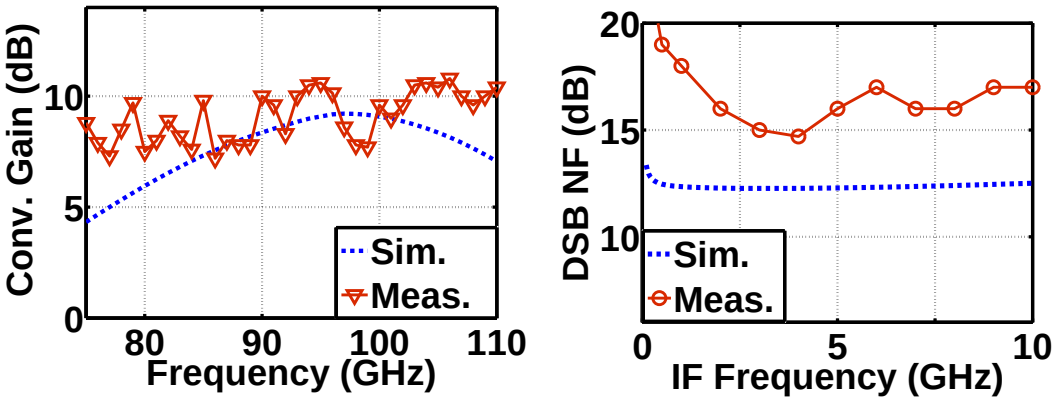


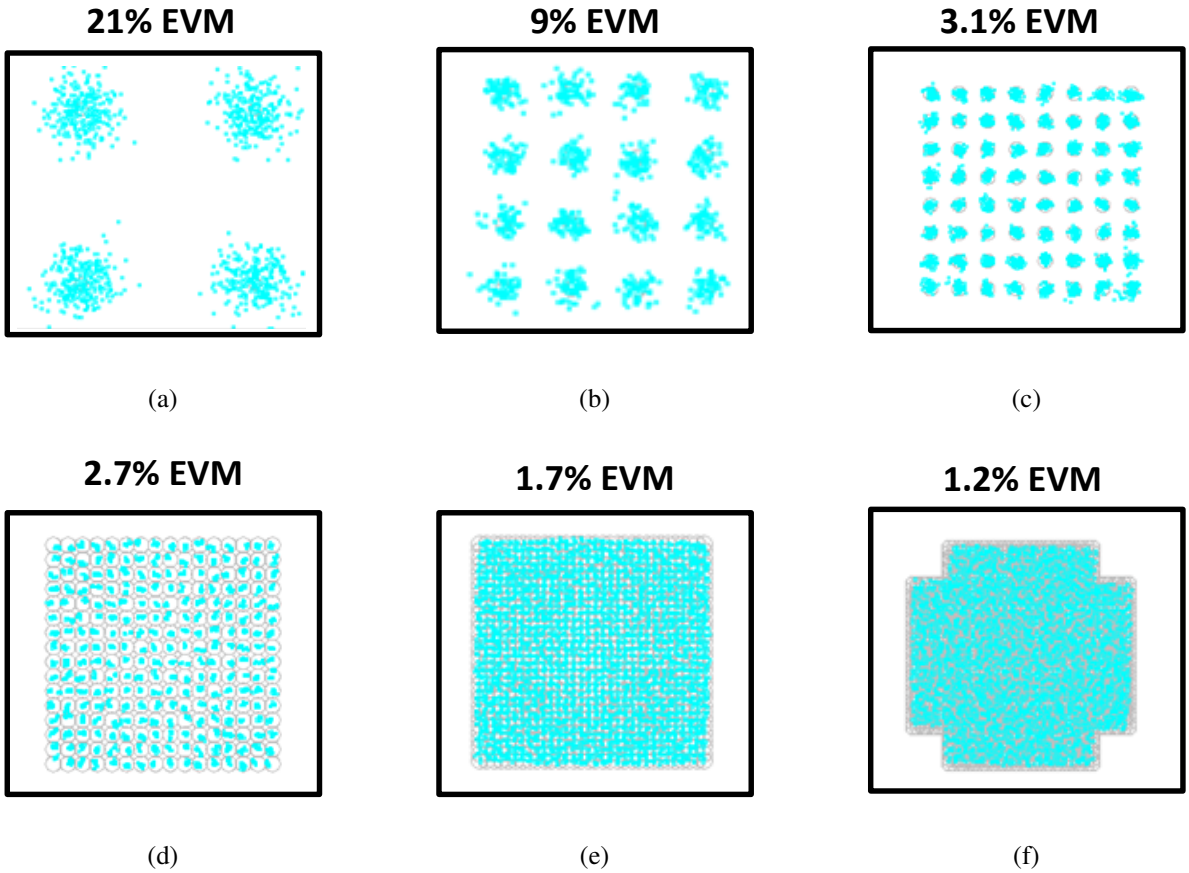
(f)

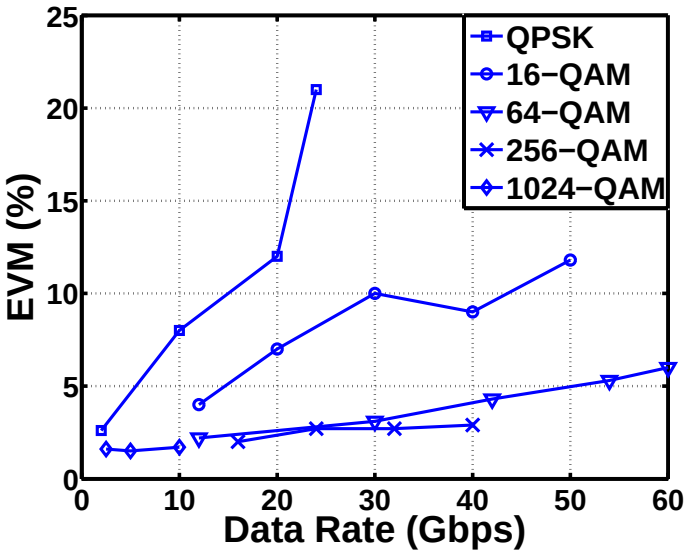
Figure 2.24: IF amplifier eye diagram measurements. (a) 20 Gbps NRZ, (b) 30 Gbps NRZ, (c) 40 Gbps NRZ, (d) 4 Gbps PAM-4, (e) 20 Gbps PAM-4, (f) 30 Gbps PAM-4.



(a) (b)

Figure 2.25: W-band receiver measurements. (a) conversion gain, (b) noise figure.





(g)

Figure 2.26: W-band receiver measurement results. (a) 24 Gbps QPSK, (b) 40 Gbps 16-QAM, (c) 30 Gbps 64-QAM, (d) 32 Gbps 256-QAM, (e) 10 Gbps 1024-QAM, (f) 5.5 Gbps 2048-QAM, (g) EVM vs. data rate.

Chapter 3

Analysis and Design of Wideband I/Q CMOS Modulators

3.1 Introduction

Direct conversion architectures have become the design of choice for wideband and multi-standard radios. Non-zero intermediate frequency (IF) architectures suffer from the image problem and thus require either image-reject filters or image-rejection designs; which come at the cost of larger footprint and greater power consumption. Furthermore, the intermediate frequency used in heterodyne radios limits the maximum bandwidth that can be handled by the transceiver , while also complicating the frequency planning and limiting the radio reconfigurability, as needed by multi-band and multi-standard radios [44, 45].

Direct-conversion and direct-modulation transmitters while offering the highest modulation bandwidth and configurability they, however, suffer from well-known non-ideal effects such as I/Q imbalance and LO leakage (or carrier feedthrough) that limit their dynamic range. These effects have become more prominent in deeply scaled CMOS technologies due to their limited voltage headroom and worse device matching properties. Currently, these effects are mitigated

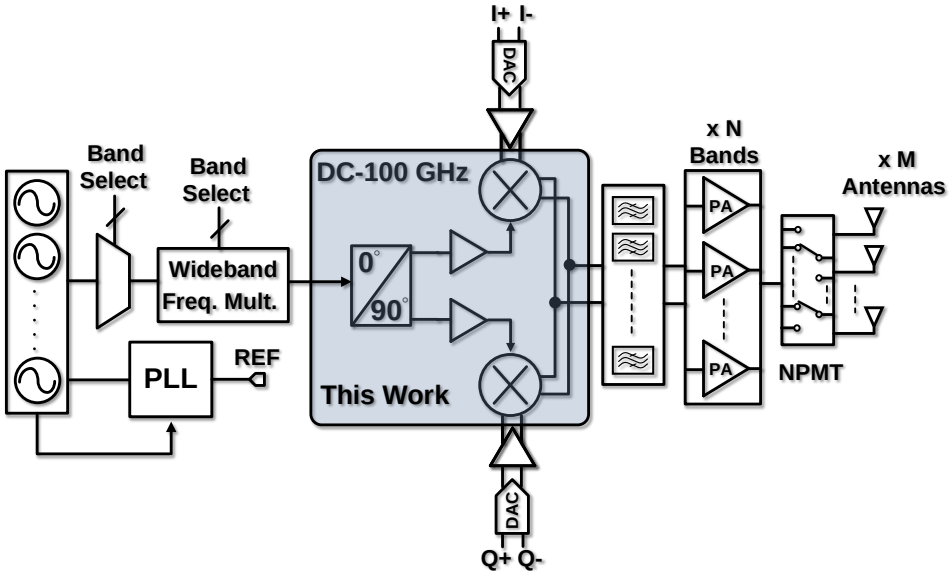


Figure 3.1: Wideband DC-100 GHz software-defined transmitter.

in the digital domain with adaptive digital calibration to maintain good spectral purity and low bit-error rate (BER) under various operating conditions.

Concurrently, future mm-wave systems for 5G and beyond will leverage MIMO techniques and wideband high-order modulation schemes to support the increasing data traffic, and direct-conversion transmitters are well-suited for these wideband and complex solutions by minimizing the number of stages in the radio chain, while also offering a much needed flexibility in frequency planning. Unfortunately, the LO leakage challenge is expected to worsen with MIMO, since each antenna will utilize its own transceiver with its own independent leakage and I/Q imbalance impairments, making the digital correction of these transceivers a power hungry solution if an adequate analog performance is not attained from the core mm-wave blocks. Furthermore, low carrier feedthrough and I/Q imbalance is needed to support high dynamic range levels as required by high-order modulation schemes which strive to maximize the spectral efficiency.

Similarly, achieving low levels of I/Q imbalance remain a challenge for direct-conversion Cartesian or polar transmitters, where amplitude and phase mismatches between the I/Q paths of direct-conversion radios cause mirror-frequency interference (self-interference). Furthermore,

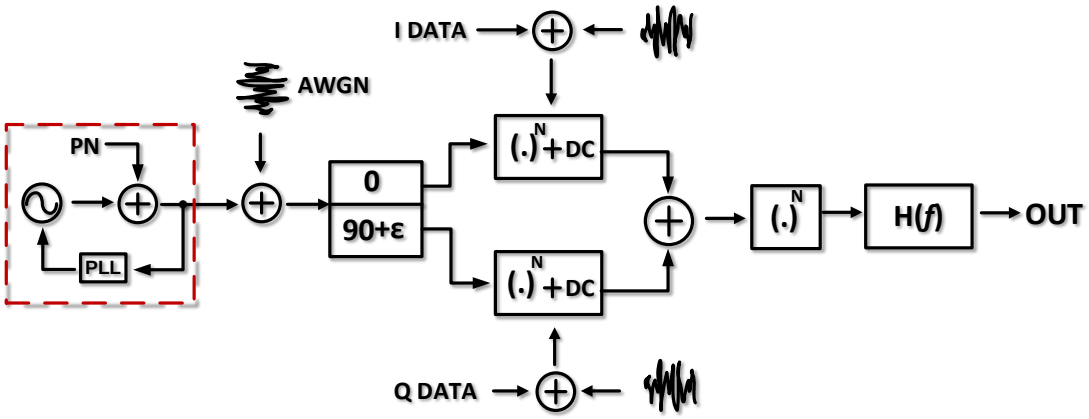


Figure 3.2: Generic Cartesian transmitter block diagram.

I/Q imbalance and LO leakage cause additional IMD terms at the power amplifier (PA) output, complicating the performance of PA digital predistorters, deeming the original predistorter coefficient estimates invalid if not accounted for properly [46, 47]. In conclusion, wideband mm-wave I/Q modulators with low levels of carrier feedthrough and I/Q imbalance, in deeply-scaled CMOS technologies, are highly desirable and will play an instrumental role in future mm-wave radios.

Software-defined radios promise the highest degree of reconfigurability and support of multi-wireless standards, where the entire radio chain is made digital with the exception of the analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) [48]. However, it is still not clear whether an acceptable performance can be achieved with mm-wave RF-DACs without a significant power penalty incurred in the digital domain [11, 49]. Fig. 3.1 presents one viable solution for future mm-wave software-defined transmitters, where traditional baseband DACs are employed with an ultra-wideband DC-100 GHz wideband front-end. Wideband synthesizers and frequency multipliers for instrumentation and software-defined transceivers have been demonstrated before [50–52]. A bank of bandpass filters and power amplifiers may be used to meet the strict SNR and ACPR specifications, and to relax the design requirements for the baseband DACs (less resolution and sampling rate) and thus reducing the overall system power

consumption.

This work presents a DC-63 GHz I/Q modulator fabricated in GlobalFoundaries 45nm CMOS SOI process. The goals of this work are threefold: (1) Present system and circuit analysis of direct-conversion radio transmitters and I/Q modulators highlighting bottlenecks and design tradeoffs. (2) Present a state of the art 200-Gbps DC-63 GHz I/Q modulator where the circuit performance has been pushed to the boundaries of current CMOS technology and instrumentation limits. (3) Introduce new potential applications of ultra-wideband I/Q modulators such as carrier aggregation across different mm-wave bands.

Section 3.2 will present the system analysis, section 3.3 discusses the circuit analysis and design, section 3.4 presents the measurement results and section 3.5 concludes the paper.

3.2 System Analysis

Constellation diagrams are used to characterize the performance of radio transmitters, since they present a qualitative visual tool to capture various transmitter impairments. Error Vector Magnitude (EVM) is used to quantitatively characterize distortions in constellation diagrams. Fig. 3.2 presents the block diagram of a Cartesian I/Q transmitter along with the major sources of impairments that degrade the system EVM and BER. These effects include, I/Q amplitude and phase mismatch, carrier feedthrough, LO phase noise, wideband additive white Gaussian noise (AWGN), non-linear distortion in the modulator and power amplifier, and lastly the non-ideal frequency response of the channel that results in inter-symbol interference (ISI).

EVM impairments have been studied previously in the literature [19, 49]. This work revisits these impairments in more details, with particular emphasis on I/Q transmitters and modulators, and will also attempt to offer insight to the circuit designer to address these issues beforehand. The goal of this section it to introduce a methodology to build optimum wideband and high dynamic range I/Q modulators for a given EVM or BER requirement.

3.2.1 EVM

For N number of symbols, the EVM at the kth symbol is given by:

$$EVM_{k,avg} = \left[\frac{E\left\{ |\vec{e}(k)|^2 \right\}}{E\left\{ |\overrightarrow{d}(k)|^2 \right\}} \right]^{0.5} \tag{3.1}$$

where $\overrightarrow{d}(k_i)$ is the ideal modulation vector, $\overrightarrow{e}(k_i)$ is the error vector, and $E\{\}$ is the expectation of ensemble averages. all the peaks have been normalized to one. Here we distinguish again between two definitions of EVM [49],

$$EVM_{peak} = \frac{EVM_{avg}}{C} \tag{3.2}$$

where C is the Crest factor of the particular waveform, thus EVM_{peak} normalizes to error vector to the peak constellation symbol. we will employ both EVM definitions throughout this paper. For m-QAM square modulations without root-raised-cosine (RRC) filtering applied, the crest factor is at a minimum value of

$$C = \sqrt{\frac{3(\sqrt{M}-1)}{\sqrt{M}+1}} \tag{3.3}$$

The corresponding EVM_{rms} values are simply the root-mean-square values across the N symbols within a given transmitted packet. EVM_{max}, not to be confused with EVM_{peak}, is the worst case EVM across the N symbols tested, and correlates strongly with the BER.

3.2.2 Linearity of Short-Channel CMOS

Traditionally, I/Q modulators operated in deep back-off to avoid non-linear distortion and maintain high spectral purity. More recently, with the increasing demand for ultra-wideband transmitters and the advancement of digital predistortion techniques, modulators must operate increasingly close to their P1dB point in order to maintain a high SNR and dynamic range across

very wide bandwidth. Thus, AM-AM and AM-PM effects will be studied in this section from both system-level and device-level perspectives, with the goal of finding an optimum back-off level to improve the transmit performance. Fig. 3.3 shows the effect of non-linear effects AM-AM and AM-PM on a 64-QAM constellation with 30 dB SNR. The constellations shown are based on a MATLAB simulation over 10^6 random symbols.

In these constellations, the AM-AM gain compression is assumed to be purely related to odd-order harmonics.

$$g_c \propto g_3 v_{gs}^2 \tag{3.4}$$

while AM-PM compression is related to even-order harmonics

$$\phi \propto g_2 v_{gs}^2 \tag{3.5}$$

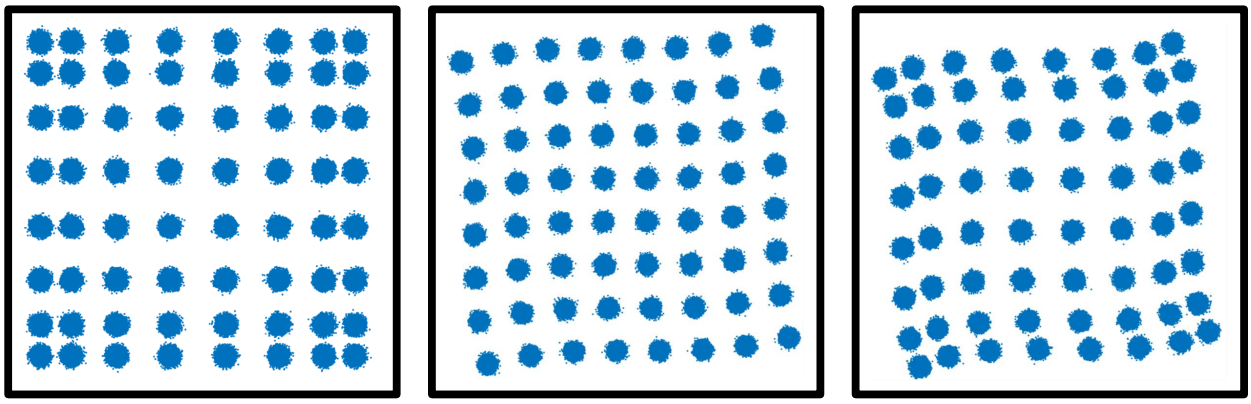
which are well-known modeling expressions [53], and will be explained further in later sections in the context of short-channel FETs. It can be observed that nonlinearity in the I and Q paths as shown in Figs. 3.3a-3.3c produces a different distortion effect in the constellation than simply distorting the IQ envelope (Figs. 3.3d-3.3f).

AM-AM

For short-channel FET devices, the current-voltage relationship is given by

$$i_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{V_{ov}^2}{1 + \theta V_{ov}} \tag{3.6}$$

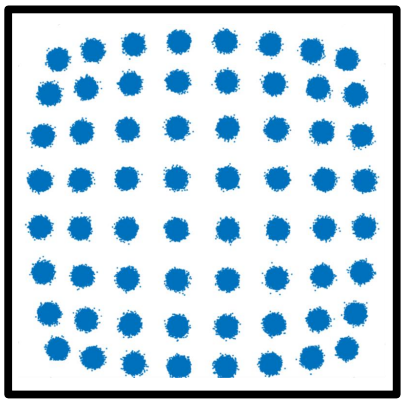
where θ is a fitting factor that captures mobility degradation and velocity saturation effects in short-channel devices. To find the third-order non-linearity causing amplitude and gain compression, a simple Taylor series expansion can be used, leading to the simple input voltage compression point formula



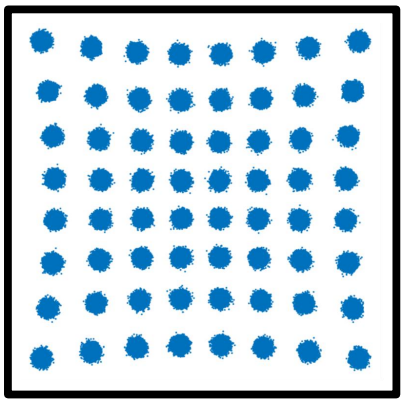
(a) 4.34 %

(b) 2.72 %

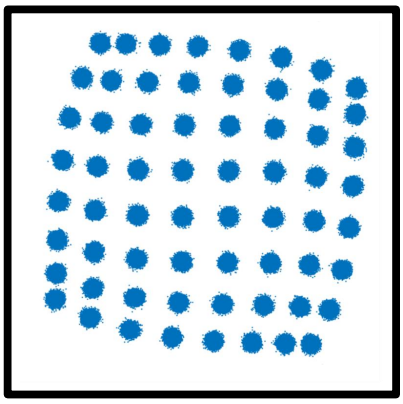
(c) 4.65 %



(d) 3.66 %



(e) 3.93 %



(f) 4.39 %

Figure 3.3: Simulated linearity-limited constellations with $EVM_{rms,peak}$ values labeled. (a) I/Q modulator AM-AM, (b) I/Q modulator AM-PM, (c) I/Q modulator AM-AM and AM-PM, (d) PA radial AM-AM compression, (e) PA radial AM-AM expansion, (f) PA radial AM-AM comprssion with AM-PM.

$$V_{IP1dB} = \sqrt{0.145 V_{ov} \frac{2+\theta V_{ov}}{6\theta} (1+\theta V_{ov})^2} \tag{3.7}$$

As an example, at a bias condition of approximately 0.1 mA/μm, the overdrive voltage $V_{ov} \backsim$0.1 V, and therefore IP1dB is approximately -10 dBm into a 50 Ω load in 45nm SOI CMOS. This is a coarse approximation that ignores memory affects and, more critically, assumes soft nonlinearity at the input with no voltage clipping at the output limited by the supply voltage. Nonetheless, these assumptions were found to give a good qualitative prediction of the circuit

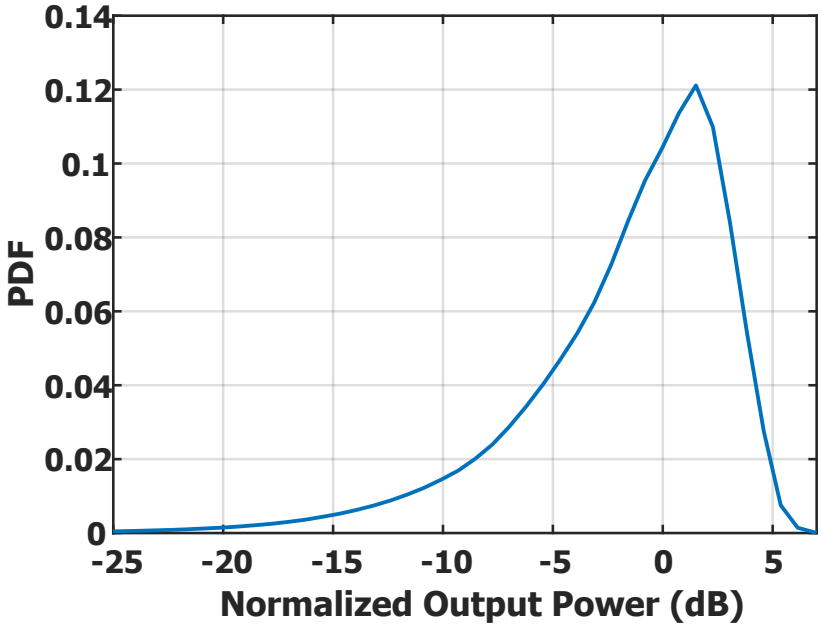


Figure 3.4: Probability distribution function of a 64-QAM modulation with a roll-off factor α =0.22.

performance as will be demonstrated in the following sections.

Next, we attempt to predict EVM degradation due to AM-AM compression. For a voltage compression factor, in linear scale, g_c , such that $g_c \leq 1$, and $g_c = 10^{\Delta_{dB}/20}$, then since g_c is a function of the input voltage v_{in}, then

$$EVM_{AM-AM} = \frac{|\vec{a}_{error}|}{|\vec{a}_{ideal}|} = \left| \frac{\vec{a}_{ideal} - g_c(v_{in}) \cdot \vec{a}_{ideal}}{\vec{a}_{ideal}} \right| = |1 - g_c(v_{in})| \tag{3.8}$$

For example, at the OP1dB point of operation ($\Delta_{dB} = -1$), the "spot" EVM at that point equals 10.87% . Where this is the EVM normalized to the average power EVM_{avg}. To evaluateEVM_{rms}, we must take into account the probability distribution function (PDF) of the input voltage, so that, in general, for an m-QAM signal:

$$EVM_{rms} = \sum_{k=1}^{M} P(k) \cdot \left|1 - g_{c,k}\right| \tag{3.9}$$

Therefore the maximum EVM (EVM_{max}), and consequently the BER, is strongly dependent on the operating condition of the modulator/transmitter with regards to the P1dB point. On the other hand, EVM_{rms} depends on the probability distribution of the symbols and the resulting PAPR of the waveform post filtering. In its simplest form, $P(k) = 1/M$; $P(k) \leq 1 \; \forall k$, if no-filtering is used and all constellation points are equally probable.

As a rule-of-thumb applying RRC filtering increases PAPR by 2-5 dB, and is a strong function of the roll-off factor and less so on the filter length and the oversampling factor. Fig. 3.4 presents an example of the probability distribution function (PDF) of a 64-QAM signal with RRC filtering applied.

Often in calculating the EVM, the receiver attempts to minimize the EVM value by scaling and rotating the reference constellation by a constant linear factor; as opposed to simply comparing directly to the reference constellation. It follows that a complex scaling factor g_0 is needed in equation (3.9) such that

$$EVM_{rms} = \sum_{k=1}^{M} P(k) \cdot \left| \frac{g_0 - g_{c,k}}{g_0} \right| \tag{3.10}$$

Which results in significantly lower EVM values. This correction factor was used in calculating EVM values in Fig. 3.3. Note that the $P(k)$ factor is the probability value of a constellation symbol k and differs from the PDF distribution that is due to the RRC filter.

AM-PM

Under large signal conditions, the change in the gate-source capacitance, as a function of the input voltage, cause AM-PM distortion and thereby disturbs the constellations, as has been shown in Fig. 3.3. AM-PM distortion is a strong function of the bias point of the transistor. It can be shown that for a pure class A and class B operations, the effective capacitance does not change with the voltage swing, and therefore the AM-PM distortion is minimum.

On the other hand, Class AB suffers from a significant change in the effective capacitance, and therefore AM-PM distortion is prominent in this class [54, 55]. Since in most cases efficiency specs are relaxed for modulators - in comparison to power amplifiers - they are biased in class A in order to operate linearly and maintain a good modulation accuracy. Note that, however, a transconductance stage biased in class-A will operate in class AB if the gate is overdriven, such that the drive voltage swing increases enough to bring the instantaneous voltage at the gate below the threshold voltage.

For simple common-source stage, the phase shift ϕ at frequency ω_o, and for a source resistance R_s [54]

$$\phi = tan^{-1}\left(-R_s\omega_o\left(C_{gs0} - \frac{1}{2}C_{gs2}\right)\right) \tag{3.11}$$

where C_{gs0} and C_{gs2} are the Fourier coefficients of the gate-source capacitance and depend intrinsic gate-source capacitance, the bias point, and input voltage amplitude v_i, and can be readily calculated from [54]. The C_{gd} effect can be ignored in cases where the Miller effect is not dominant, which is the case in the Gilbert-cell modulator used in this work.

Assuming that the rotation in the constellation vector, caused by the AM-PM response is $\phi_{AM-PM}(v_{in}(t))$, such that $\phi_{AM-PM}(t)$ =$\phi(t) - \phi(t)_{back-off}$, the degraded signal can be expressed as:

$$\overrightarrow{d}^*(t) = \overrightarrow{d}(t) + \overrightarrow{e}(t) = \overrightarrow{d}(t)e^{j[\phi(t)_{back-off} + \phi_{AM-PM}(t)]} \tag{3.12}$$

Then it can be shown that for small $\phi_{AM-PM}(t)$ values,

$$EVM_k = \phi_{AM-PM}(k) \tag{3.13}$$

To evaluate rms EVM, EVM_{rms}, we again include the PDF to account for the different

compression experienced by the different constellation points. Generally, for an m-QAM signal:

$$EVM_{rms} = \sum_{k=1}^{M} P(k) \cdot EVM(k) \tag{3.14}$$

Where again, the reference constellation is rotated byϕ_0 value that minimizes EVM_{rms}. It is worth noting that in most cases AM-PM distortion occurs before AM-AM compression is observed, but AM-AM compression dominates the degradation in EVM and BER.

3.2.3 Carrier Feedthrough

As discussed in section 3.1, carrier feedthrough limits the dynamic range of modulators and as a consequence limits the highest order modulation that can be transmitted. Carrier feedthrough C_{FT} in I/Q modulators can be generally attributed to device and layout mismatches. At mm-wave frequencies, however, C_{FT} is dominated by coupling through device parasitics and in the supply interconnects as well as through the silicon substrate [49]. These effects can be effectively mitigated by applying DC offsets across the differential transconductance pairs. Beyond that, the leakage is dominated by the second-order non-linear distortion, that produces data-dependent DC components that mix with the carrier frequency driving the switching quad ($C_{FT} \propto g_2 v_{gs}^2$).

In general, to minimize carrier feedthrough, a combination of symmetric layout techniques and external bias trimming control must be employed, and will lead to leakage levels as low as -50 dBc or better.

3.2.4 ISI and Equalization

The impact of limited bandwidth in producing intersymbol intereference (ISI) and its effect on EVM and BER was presented before in [15, 49]. There is a fundamental trade-off between noise and bandwidth, and therefore it becomes desirable to build I/Q modulators with

programmable bandwidth, such that the two performance metrics can be traded-off dynamically, allowing the support of both spectrally efficient high-order modulation formats, in addition to simpler modulations over wider bandwidths.

Digital equalization is especially successful at compensating for ripples in the frequency response. However, equalization for ISI that is attributed to severe bandwidth limitation, or nulls in the frequency response, leads to boosting the noise in the system; and while the distortion due to ISI is improved, the dynamic range becomes SNR limited, degrading the overall modulation accuracy [56]. This is specially true in analog (continuous-time) linear equalization (CTLE) or analog pre-emphasis and digital feed-forward equalization which operate by applying the inverse analog or digital (FIR) filter that compensates the channel response. Other non-linear approaches such as decision-feedback equalization, while addressing the aforementioned trade-off, are not well suited for high-order modulation schemes and are limited in speed, but remain an active research topic [57]. In other words, equalization does not replace wideband, linear and low-noise analog design, but rather assists in compensating the non-ideal frequency responses of the channel, as will be demonstrated in the measurements section of this work (section 3.4.3).

3.2.5 ACPR

In addition to EVM and BER, spectral purity of the modulated waveform is of utmost importance. The spectral quality is quantitatively measured with the adjacent power ratio (ACPR). ACPR is defined as the ratio of the power integrated over an assigned bandwidth ($\triangle B_{ACP}$) in the adjacent/alternate channel (at an offset f_1) to the total desired transmission power over bandwidth BW [15]:

$$ACPR = \frac{\int_{f_1}^{f_1+\triangle B_{ACP}} PSD(f)df}{\int_{f_o-BW/2}^{f_o+BW/2} PSD(f)df} \tag{3.15}$$

where PSD is the power spectral density. The simplest form for evaluating linearity is by

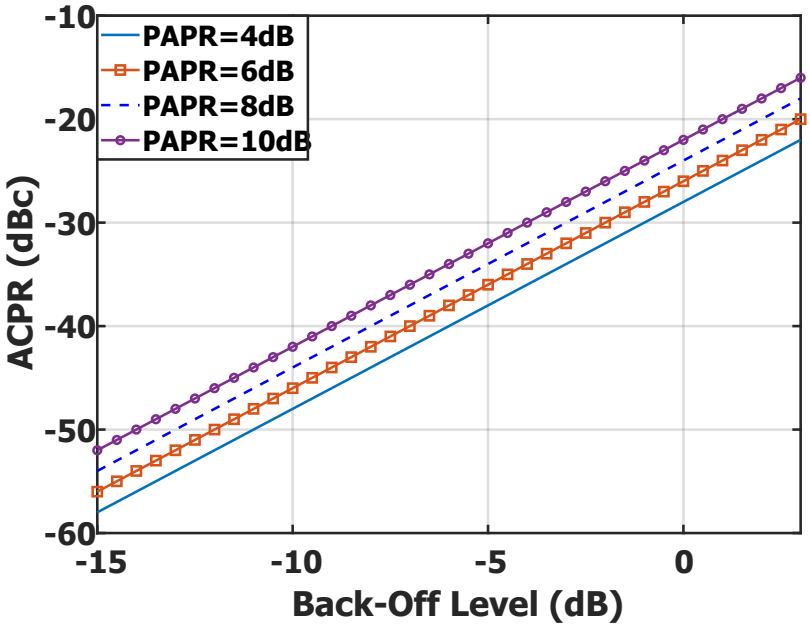


Figure 3.5: ACPR vs Back-off level.

using the two-tone test, where the intermodulation term IM_3 is in fact equal to

$$IM_3[dBc] = 2(P_{tone} - OIP3) \tag{3.16}$$

where P_{tone} is the average power of the two tones. Since ACPR is concerned with the ratio of the spur on one side, to the *total* signal power (in this case the power of both tones), we expect the ACPR to be 3-dB better than IM3:

$$ACPR[dBc] = 2(P_{tone} - OIP3) - 3dB \tag{3.17}$$

In general, it can be shown that the ACPR of a transmitted modulated signal is related to the transmitter's OP1dB through

$$\begin{aligned} ACPR_{TX}[dBc] &= 2(P_{TX} - OP1dB) - 32 \\ &+ PAPR + 10log\left(\frac{\triangle B_{ACP}}{BW}\right) \end{aligned} \tag{3.18}$$

where P_{TX} is the average output power of the transmitter, and the $(P_{TX} - OP1dB)$ term will defined as the back-off level. Fig. 3.5 presents the simulation results based on (3.18), which assumes that the ACPR is linearity-limited, and not limited by the system noise. Again, finding the relationship between ACPR and EVM would require knowing the probability distribution function of the waveform.

For example, at OP1dB the IM3 is approximately 20 dB lower than the signal, which results in EVM_{avg} equal to 10% at that instant. The rms EVM EVM_{rms}, however, is much lower given the low probability of peak output power events. Note that for ultra-wideband modulators the integrated noise is large enough to dictate the lower-end of the dynamic range. In other words, for ultra-wideband circuits operating in back-off, the integrated noise power may often be greater than the IM3 spurs.

3.2.6 EVM and BER

The relationship between BER and EVM in SNR-limited links was presented in [49]. Fig. 3.6a presents the simulation results of BER versus RMS EVM_{peak} ($EVM_{rms,peak}$) for 64-QAM. Three different cases are simulated with 6×10^{10} bits tested in each. First, an SNR limited case was studied where the only impairment added to the signal was white noise (AWGN) with various power levels. The simulation are in good agreement with the theoretical results presented in [49]. Similarly, phase noise and AM-AM compression cases were tested separately.

It can be observed from fig. 3.6a that the same EVM_{rms} value can lead to remarkably different BER outcomes depending on the dominant source of EVM impairment. This can be intuitively explained by Figs. 3.6b-3.6d, where three constellations are presented, all have the same $EVM_{rms,peak} = 3\%$ ($EVM_{rms,avg} = 4.6\%$). The constellations presented, however, exhibit different EVM_{max} values, with 3.6b having an $EVM_{max} = 9.1\%$, 3.6c has an $EVM_{max} = 13.3\%$, and 3.6d with $EVM_{max} = 13.3\%$ as well. This discrepancy in EVM_{max} values translates to different BER values.

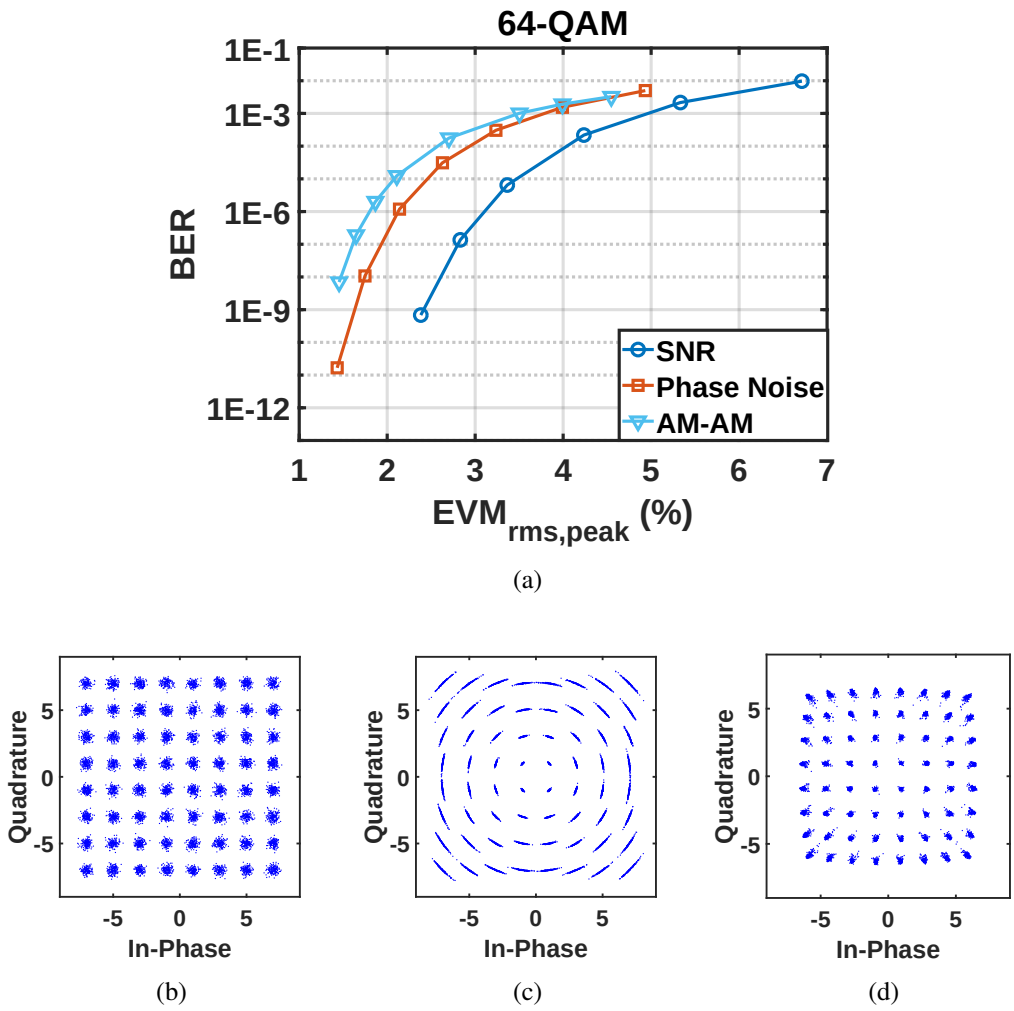


Figure 3.6: Simulation of BER vs. RMS EVM for 64-QAM under different impairment: (a) simulation results, (b) noise-limited constellation, (c) phase noise limited constellation, and (d) nonlinear compression limited constellation.

Fig. 3.7 presents a methodology for selecting the optimum back-off level for wideband modulators. There generally exists an optimum back-off level to minimize the BER, increasing the back-off level beyond that increases the carrier feedthrough and degrades the SNR and leads to worse EVM and BER. Reducing the back-off level increases the non-linear distortion and degrades the BER.

On the other hand, given the continuous advancement of efficient forward error correction (FEC) [58] and digital predistortion [59] techniques, operating the system near its P1dB operation

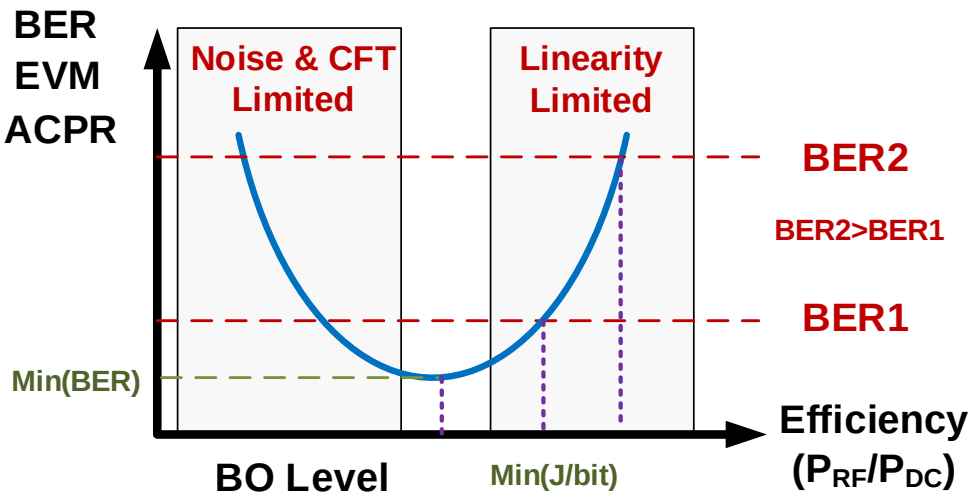


Figure 3.7: Modulator optimization scheme. A BER=1E-3 limit will be imposed throughout this work.

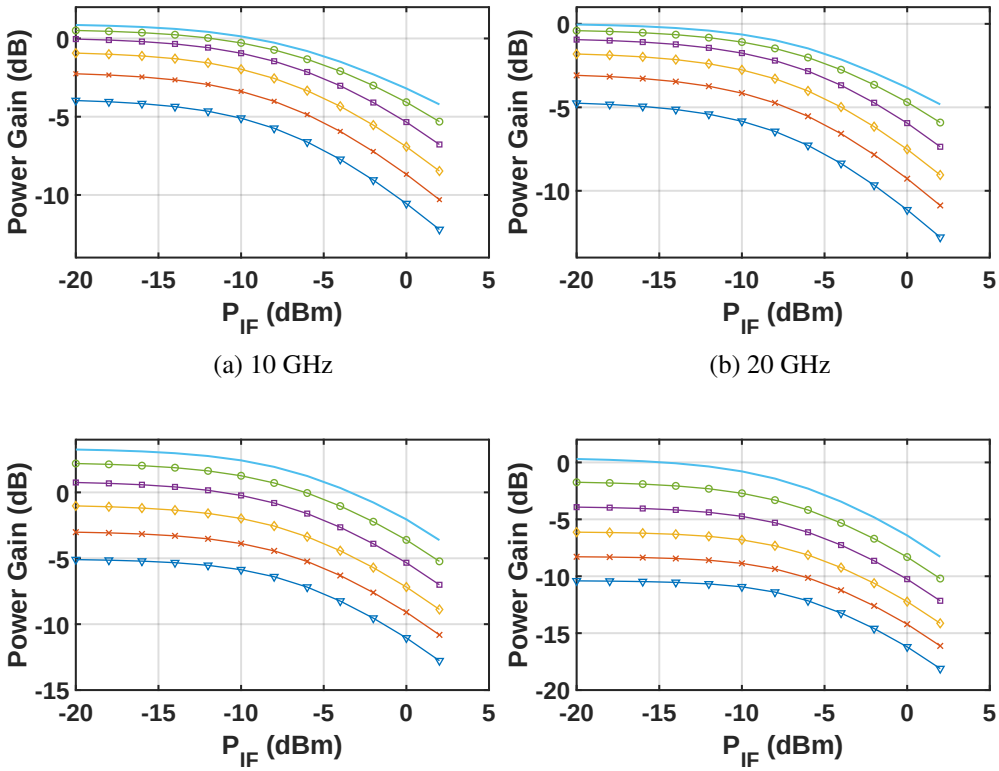
point has becomes a very attractive proposition, since it increases the overall system efficiency and its dynamic range, thereby optimizing the joule-per-bit system efficiency.

3.3 Circuits Analysis and Design

3.3.1 Wideband Double-Balanced Mixer

A double-balanced mixer or Gilbert cell will form the basis for the high-speed and wideband I/Q modulator presented in this work. In addition to its superior LO and IF suppression properties, the double-balanced mixer architecture has been shown to allow the highest modulation bandwidth in comparison to other architectures [10].

Double-balanced mixers, on the other hand, have higher power consumption with worse noise figure in comparison with single-balanced mixers, for a given supply voltage. For mm-wave applications, however, the use of differential transconductance stages becomes irreplaceable since they provide virtual grounds locally within the transistor layout. This is in contrast with single-ended designs where the parasitics of the interconnects to the ground dominate the performance by degenerating the gain stages, and thus degrading the gain and noise performance.



(a) 10 GHz (b) 20 GHz

(c) 60 GHz (d) 100 GHz

Figure 3.8: Mixer conversion gain simulations with P_{LO} values ranging from -8 dBm to +2 dBm in 2 dB increments at (a) $f_{LO} = 10$ GHz, (b) $f_{LO} = 20$ GHz, (c) $f_{LO} = 60$ GHz and (d) $f_{LO} = 100$ GHz.

The voltage gain of the mixer driving a 50 Ω load is given by

$$\begin{aligned} A_v &= 20 \times log(\tfrac{2}{\pi} g_m \times R_p || R_L) \\ &+ \quad 20 \times log(\tfrac{R_{term}}{R_{term}+R_s}) \end{aligned} \tag{3.19}$$

where $g_m = 51mS$, R_D is the load resistance, $R_{term} = 75\Omega$ is the termination resistor at the input. This resistance value was found to give a good balance between input matching and gain, especially since the resistor value drop with frequency, so starting with a greater resistance extends the input matching to higher frequencies. For the given bias condition the voltage gain was found to be -4.67 dB. The power gain G equals 3.3 dB and is given by:

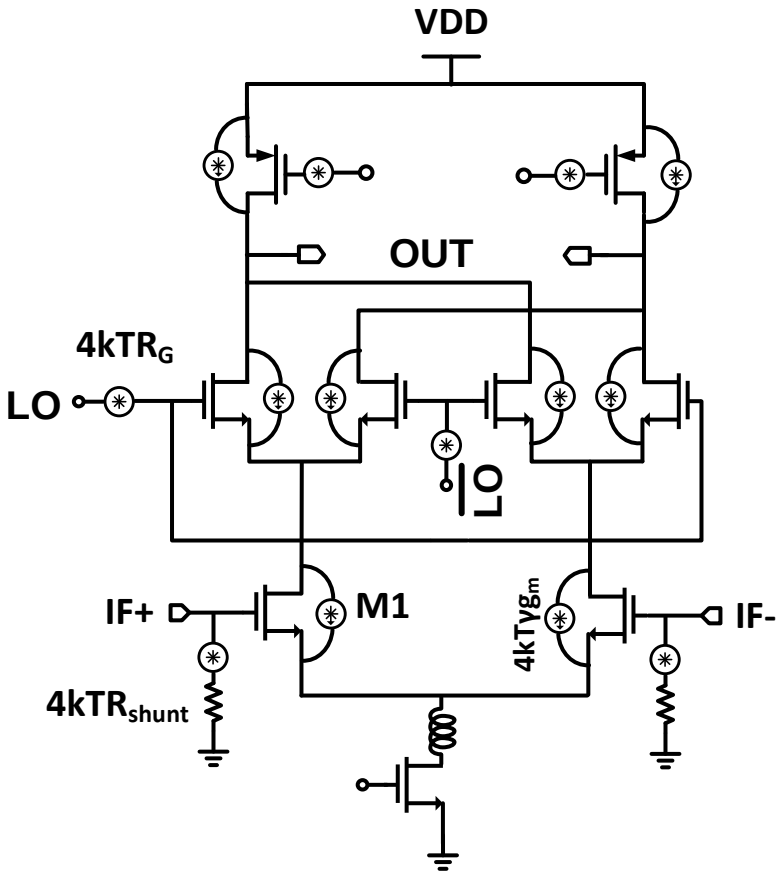


Figure 3.9: Gilbert Cell noise analysis.

$$G = A_v + 20 \times log_{10}(\frac{R_{term}}{R_p||R_L}) \tag{3.20}$$

The minimum LO power required to fully steer the current through the switches is $\sqrt{2}V_{ov} = 350$ mV or 1 dBm for this design. Higher LO drive power may be required to reduce the noise contribution from the switches, as well as increasing the conversion gain of the mixer. Fig. 3.8 presents the simulated conversion gain for at different carrier frequencies and under different LO power drive conditions. As expected, the conversion gain improves with increasing P_{LO} up to +2 dBm, above which little or no improvement was observed in the simulated conversion gain.

Fig. 3.9 presents the double-balanced Gilbert cell with active PMOS loads that is used in this work, along with its various noise sources. The output noise appearing at one output terminal

$\overline{v_{n,out}^2}$ is given by:

$$\begin{aligned}\overline{v_{n,out,SE}^2} &= 4kTR_s\cdot A_v^2 + 4kTR_G\cdot A_v^2 \\ &+ 4kTR_{G_p}(g_{mp}R_L)^2 + 4kTR_L \\ &+ \tfrac{1}{2}(4kT\gamma g_m)(R_p||R_L)^2 + \tfrac{1}{2}(4kT\gamma g_{mp})R_L^2\end{aligned} \tag{3.21}$$

Therefore, the noise figure NF is given by,

$$NF = 1+\frac{R_s}{R_{term}}+\frac{R_L+R_{G_p}(g_{mp}R_L)^2+\frac{\gamma g_m}{2}(R_p||R_L)^2+\frac{\gamma g_{mp}}{2}R_L^2}{A_v^2R_s} \tag{3.22}$$

and is approximately equal to 12 dB, which sets the minimum noise figure achievable by the modulator. For simplicity, the noise contribution from the switching quad transistors has been ignored. This is a valid assumption so long as the LO drive power is maintained sufficiently large, which is greater than 0 dBm in this case.

The noise contribution from the switching quad is significant when the differential pair transistors are simultaneously on, which can be minimized by to reducing the rise and fall time of the LO signal. Moreover, the analysis is valid only at low frequency where the capacitive and inductive parasitics effects may be ignored.

Fig. 3.10a presents the Gilbert cell mixer used to realize the wideband I/Q modulator. Source-follower buffers are first used to present a low-capacitance load for the quadrature generator, and thus maximizing its self-oscillation frequency. Fig. 3.10b presents the simulated conversion gain, IP1dB and noise figure at 1 GHz offset and at different carrier frequencies from 10 to 100 GHz. Active 50 Ω output matching is achieved using tunable PMOS loads to realize wideband output matching. Furthermore, the tunable active PMOS load allows per-emphasis in the modulator frequency response, by boosting the high-frequency gain while attenuating low-frequency gain as needed, thus compensating the low-pass frequency response of the following stages (Fig. 3.10c).

High frequency peaking is achieved with 130 pH and 30 pH shunt and series inductors, respectively. Fig. 3.10d presents the noise figure simulations from 10 - 100 GHz, under different LO power drive conditions. As expected, the noise figure decreases with increasing P_{LO}.

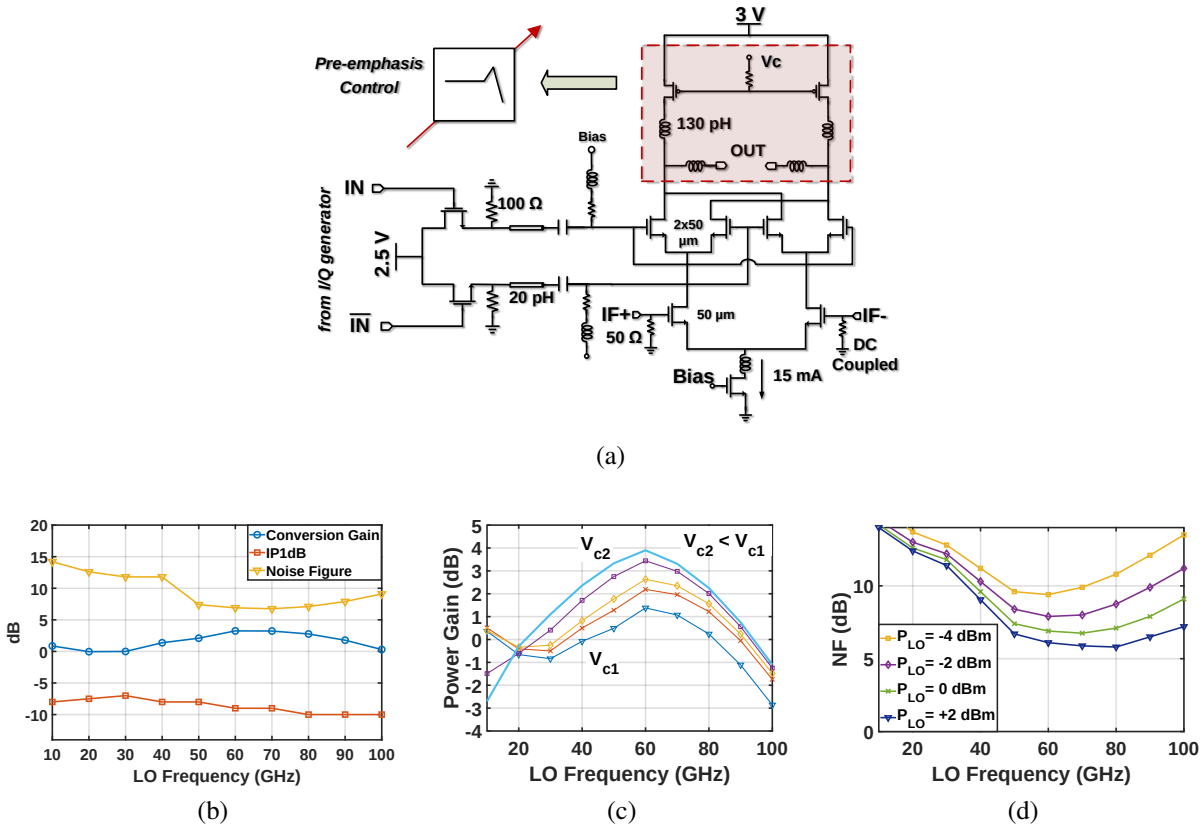
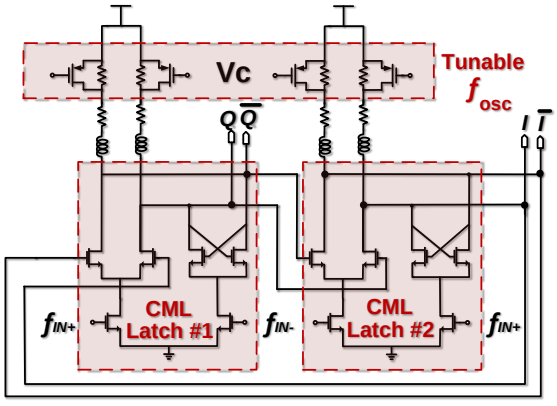


Figure 3.10: (a) DC-100 GHz buffered Gilbert-Cell balanced mixer, (b) mixer conversion gain, linearity and noise simulations up to 100 GHz, (c) mixer's simulated conversion gain as a function of the PMOS control voltage displaying peaking control by up to 3 dB at 60 GHz, (d) simulated noise figure for P_{LO} =-4 dBm to +2 dBm in 2 dB increments.

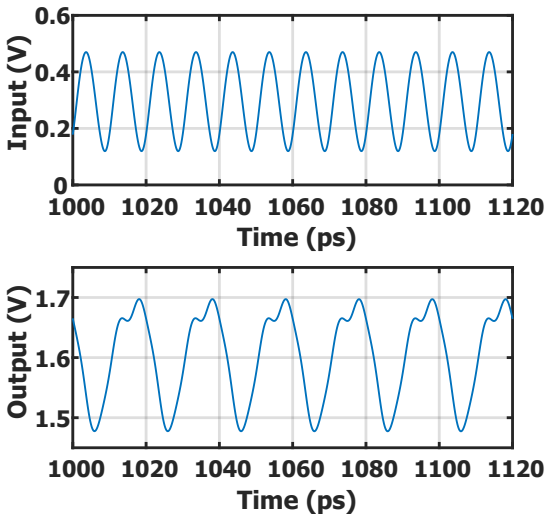
3.3.2 Programmable DC-120 GHz Divider

The generation of quadrature signals with low phase and amplitude errors remains a challenge for Cartesian transmitters. Using digital techniques, such as frequency dividers, proved to be the most successful but are limited in their frequency of operation [60]. For example, current-mode logic (CML) static CMOS dividers have been limited to around 30 GHz output frequency.

Dynamic and injection-locked dividers are capable of operating at mm-wave frequencies, but they suffer from narrow range of frequency operation.



(a)



(b)

Figure 3.11: (a) DC-50 GHz quadrature signal generator, (b) simulated transient at 100 GHz.

Fig. 3.11a presents the wideband quadrature (I/Q) signal generator, which consists of two CML latches in feedback. This traditional architecture is improved in two ways: first, the I/Q generator is loaded with source-follower stages (not shown - see Fig. 3.10a) to reduce the capacitive loading and boost its frequency of operation. Second, a novel inductive loading technique with tunable resistance is used. This controls the locations of the frequency poles and consequently the phase shift (and time delay) in the loop, allowing the control of the self-

oscillation frequency of the divider, while also introducing peaking control in the frequency response, further boosting the maximum frequency of division. A transient simulation of the divider driving the modulator is shown in Fig. 3.11b, where the input and output signals are at 100 and 50 GHz, respectively, proving the divider's capability of dividing frequencies up to at least 100 GHz.

Other known modern techniques such as dynamic CML dividers with load modulation [61] were not an option since they are not capable of operating at low frequencies, and they result in several narrow sensitivity bands; thus requiring elaborate calibration schemes, which may introduce spurs [62].

Frequency dividers exhibit sensitivity curves marked with a self-oscillation frequency f_{osc}. As the input frequency deviates from f_{osc}, the required input power needed for proper operation significantly increases, requiring wideband LO buffers which can increase the overall system power consumption. The self-oscillation frequency of a static divider is given by,

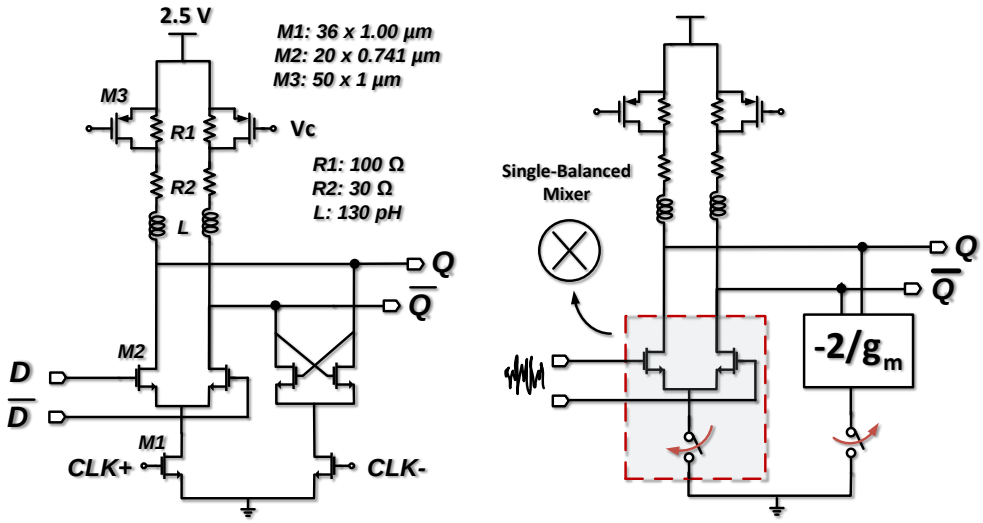
$$f_{osc} = \frac{1}{2t_{delay}} \tag{3.23}$$

where $t_{delay}$is the time delay through a single latch. For a generic static divider with a resistive load R_L, the t_{delay} when driving a capacitive load C_L can be shown to equal [61]

$$t_{delay} = R_L C_L \cdot ln\left(\frac{2I_{bias}R_L}{I_{bias}R_L - \sqrt{2}V_{ov}}\right) \tag{3.24}$$

where $R_L = R_{on,p}$ the on-resistance of the PMOS load for our particular design. It becomes evident that for a given capacitive load and voltage swing conditions, there is a direct trade-off between the the self-resonance frequency and the power consumption. This trade-off is relaxed in the programmable divider design, by reducing the R_{on} at higher frequencies, where the inductive load contributes to the impedance peaking, eliminating the need to increase the power consumption or I_{bias}. From Fig. 3.12a, in the lower frequency regime of operation, the PMOS

load is turned off, and $R_L = 130\ \Omega$, $C_L = 50$ fF, I_{bias}= 4 mA, and $V_{ov} = 200$ mV, therefore we estimate $t_{delay} \backsim 10$ ps, and $f_{osc} \backsim 50$ GHz.



(a) CML latch schematic.

(b) CML latch model.

Figure 3.12: CML latch analysis.

It is also of interest to find the maximum frequency of operation of static dividers $f_{div,max}$. In order to do so, we adopt the model shown in Fig. 3.12b, where before the latching action begin, and the divider starts operating as a digital circuit, it can be viewed as a mixer circuit with negative resistance load achieved by the cross-coupled pair at its output. The wideband noise at the input of the switching transistors at the top is mixed with the clock input at the bottom. For the circuit to divide properly, two conditions must be met: first, the output frequency must satisfy the loop equation. This condition is readily met, since the $f_{out} = f_{in}/2$ meets this criterion. Second, the mixer circuit must have sufficient gain to guarantee at least unity gain through the loop. At low frequency, this condition translates to

$$g_m R_L \geq 1 \tag{3.25}$$

As we approach $f_{div,max}$, the capacitive load at the output dominates, and most of the

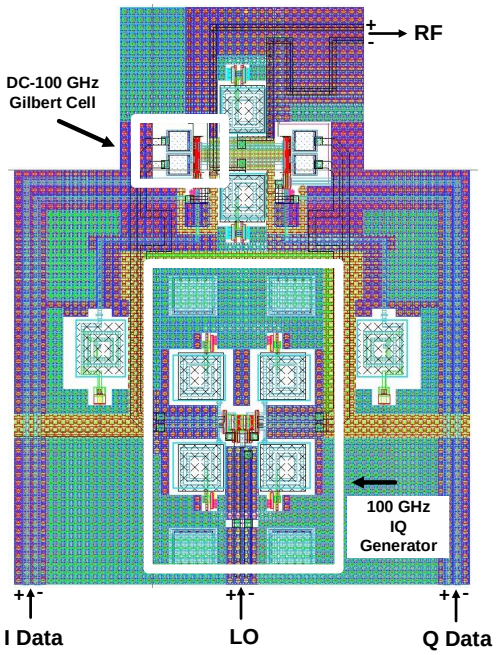


Figure 3.13: Symmetric I/Q modulator layout.

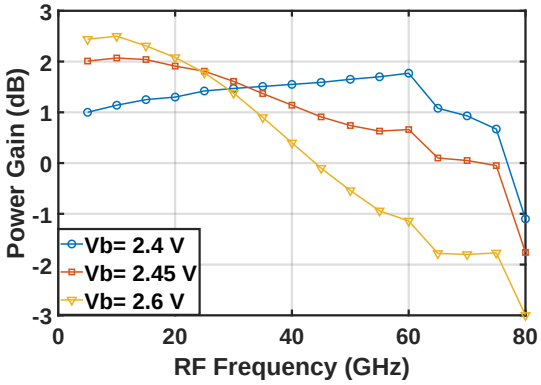
current generated by the transconductance stage flows through the capacitor. If we assume $C_L = C_{gs}$, such that latch drives another latch of similar size, then the second condition becomes

$$\frac{2}{\pi} g_m \left| \frac{1}{j\omega C_{gs}} \right| \geq 1 \tag{3.26}$$

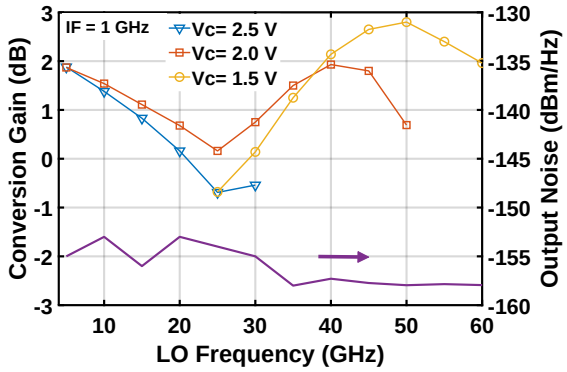
Neglecting the phase shift in the loop, and recalling that $f_t \backsim \frac{g_m}{C_{gs}}$, we then arrive at the approximate expression

$$f_{max,div} \leq \frac{2}{\pi} f_t \tag{3.27}$$

For a large inductor load, the highest simulated division frequency found to be 144 GHz. Since this is a process with an $f_t \backsim 240$ GHz, the calculated $f_{max,div}$ from (3.27) is approximately 153 GHz. If load inductor sized to resonate with the capacitive load, then at resonance



(a)



(b)

Figure 3.14: I/Q modulator simulations. (a) gain as a function of the PMOS control voltage, (b) gain and output noise at 1 GHz IF from DC-60 GHz - including the IQ generator - for different divider control voltage values V_c .

$$f_{max,div} \leq \frac{2}{\pi} Q^2 f_t \tag{3.28}$$

where Q is limited by the inductor Q factor and the gate resistance. Under these conditions, however, the divider will resemble a dynamic divider, operating within a narrow frequency range below which it fails to divide. Therefore, the divider should be carefully designed such that the "mixer" stage exhibits sufficient gain at all frequencies. Alternatively, tunable gain peaking techniques may be used, as is the case in this work.

3.3.3 DC-60 GHz I/Q Modulator

Current combining is used to combine the I and Q modulation paths, since it offers the highest bandwidth. Quadrature amplitude and phase mismatches are minimized by following symmetric layout strategies (Fig. 3.13) such that LO and data distribution is fully differential on chip with minimum mismatch. The fully differential layout ensures that mixers and divider circuits operate in a fully differential fashion, in order to maximize the transmitter speed by taking advantage of local on-chip ac ground, and desensitizing it to any common-mode ground and supply parasitics. Furthermore, common-mode rejection is achieved by a common-mode choke inductor at high frequencies, where the current mirror exhibits smaller output impedance, thereby boosting the common-mode rejection at high frequencies.

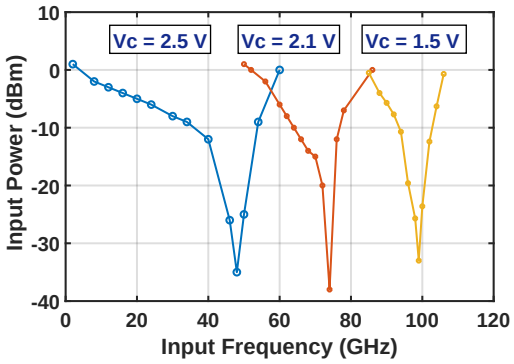
Any minimal amplitude mismatch that may rise from layout or variations in the transistors properties can be corrected by changing the modulator gain control using the current source available at the bottom of each Gilbert cell (Fig. 3.10a). Furthermore, LO leakage can be corrected using the external baseband DACs, which are DC coupled, thus enabling DC offsets between the differential IF inputs. Fig. 3.14 presents the conversion gain and output noise simulation results.

For the Gilbert cell $V_{ov} \backsim 0.15$ V, it follows then from (3.7) that $V_{IP1dB} = 0.137$ V or -9 dBm into a 75 Ω load, under a 0.1 mA/μm current density bias condition. Additionally, there is a 3 dB of inevitable combining loss when combining the I and Q modulation paths. This may be addressed using high frequency quadrature LO generators with 25% duty cycle [63, 64].

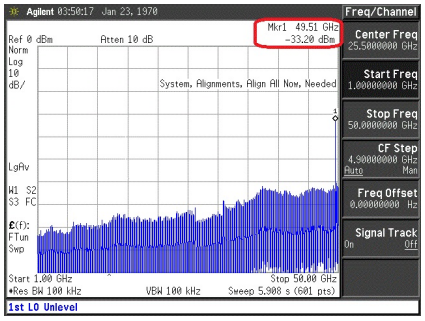
3.4 Measurements

3.4.1 Programmable DC-110 GHz Divider

To measure the self-oscillation frequency f_{osc} of the divider, a differential probe measurement was first carried out where the input signal was swept in frequency (DC-70 GHz), and in



(a)



(b)

Figure 3.15: Divider measurements. (a) measured sensitivity curves of the CML frequency divider for three different control voltage values, (b) measured CML divider output spectrum for $V_c = 1.5$ V.

power (up to 0 dBm) for a given divider tuning control voltage V_c. The outputs spectrum was then observed using the Keysight E4448A DC-50 GHz spectrum analyzer. The minimum power that was needed to divide the input frequency was then recorded and the result produced in Fig. 3.15. Furthermore, in the 70-110 GHz input frequency range, a WR-10 waveguide setup was used with the VDI AMC-335 multiplier chain serving as the 70-110 GHz signal source. An external downconversion mixer was used to cover the 50-55 GHz frequency range.

The final result is shown in Fig. 3.15a where it it can be seen that the self-oscillation frequency of the divider can be tuned in an analog fashion from 44 GHz to 99 GHz, depending on the control voltage applied to the PMOS transistors. This work presents the first DC-110 GHz CMOS static frequency divider with record self-oscillation frequency of 99 GHz (Fig. 3.15b), and allows the generation of a near-perfect quadrature LO drive from DC-55 GHz, while also

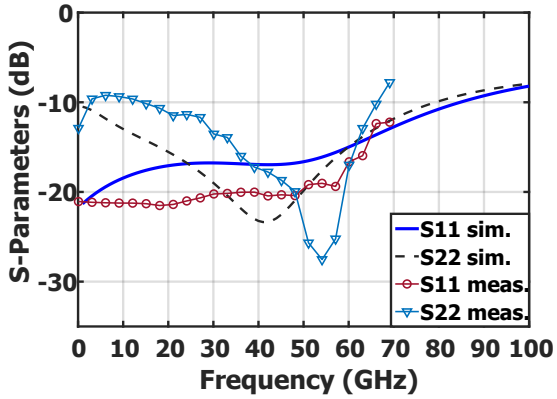


Figure 3.16: LO (port 1) and RF (port 2) return loss measurements of the double-balanced mixer.

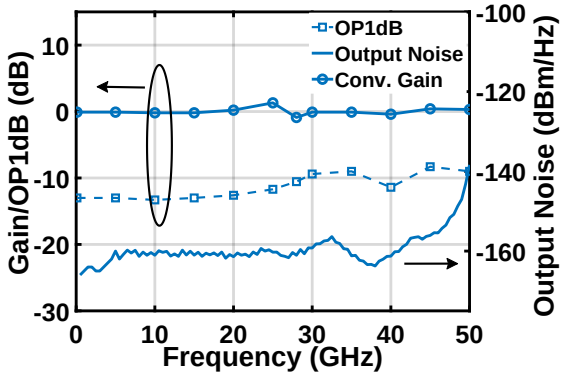


Figure 3.17: Double-balanced mixer measurements.

directly driving an I/Q modulator without the need for additional amplification stages.

3.4.2 Wideband Mixer Measurements

Fig. 3.16 presents the measured S-parameters of the LO and RF ports from DC-70 GHz, demonstrating the wideband matching at these ports. Matching at the IF ports is achieved using shunt 50 Ω resistors, and a return loss > 10 dB is measured up to 30 GHz. The simulated conversion gain and IP1dB at DC-70 GHz are -8 dB and 0 dBm, respectively, under 0 dBm LO power drive conditions.

The noise floor and linearity of the I/Q modulator dictate its dynamic range and are,

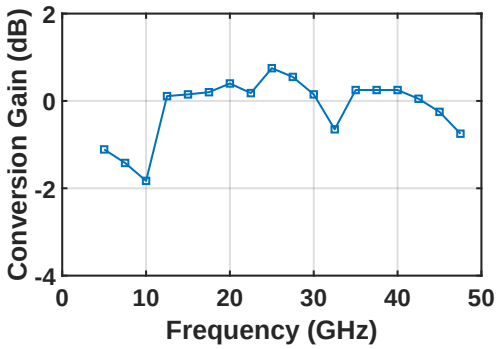


Figure 3.18: Measured mixer conversion gain for LO = 25 GHz.

therefore, critical parameters in the design of the mixers. The modulator dynamic range determines the maximum available modulation bandwidth for a given BER and a choice of modulation format. Fig. 3.17 presents the measured average conversion gain and OP1dB of 0 dB and -10 dBm from DC to 50 GHz (limited by the measurement setup). The conversion gain was evaluated by sweeping the LO frequency while fixing the IF frequency at 1 GHz.

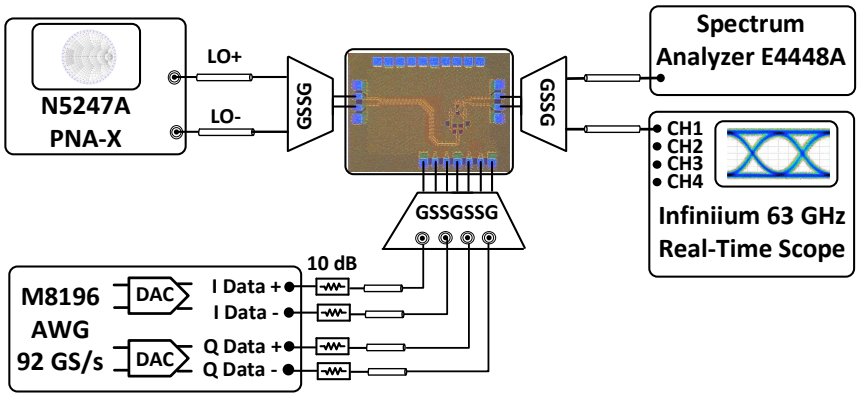
Also, the measured output noise floor in the same bandwidth is approximately -162 dBm/Hz, leading to 150 dB/Hz of dynamic range at the output. This is sufficient to support very high-order modulations (e.g. 1024 QAM) in 10 GHz of bandwidth with 50 dB of dynamic range (at P1dB).

Fig. 3.18 presents the measured conversion gain up to 50 GHz with a 25 GHz LO frequency. The mixer's conversion gain varies by less than 2 dB over the entire bandwidth, making it possible to support a minimum of 25 Gbaud baud rate when employed in the IQ modulator.

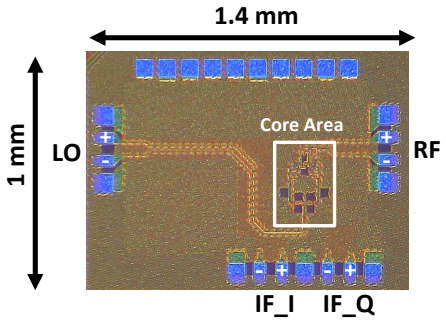
The noise floor of most commercial spectrum analyzers, without the pre-amplifier option, is in the 150 dBm/Hz range. Therefore, to correctly measure the output noise of the mixers, the noise floor of the spectrum analyzer must be overcome with external low-noise pre-amplifiers. In this experiment, three amplifiers were used with 25-40 dB gain range and covering the 0.5-50 GHz frequency spectrum in three parts: 0.5-18 GHz, 18-40 GHz and 40-50 GHz. The S-parameters of the amplifiers were then measured and de-embedded from the spectrum analyzer's noise floor

results.

Moreover, the far-out white noise of the signal source (Fig. 3.2) had to be accounted for in this low-noise measurement. To reduce the noise floor of the signal source to a low enough level, 10 dB attenuators were used in the LO path. At high LO frequencies, it was found that the cables loss was sufficient to achieve that attenuation level.



(a)



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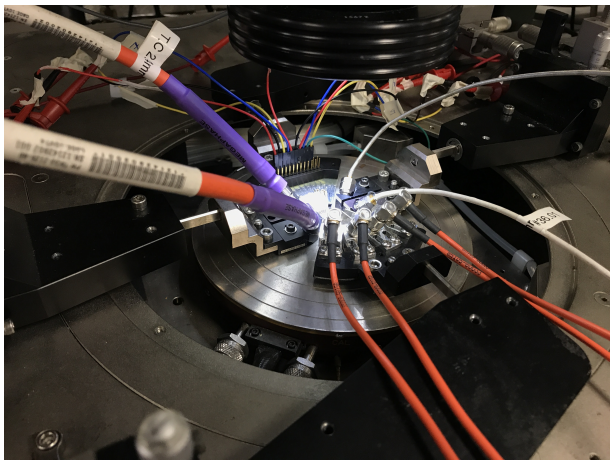


(c)

Figure 3.19: (a) Chip micrograph, (b) I/Q modulator measurement setup, (c) measurement setup photo.

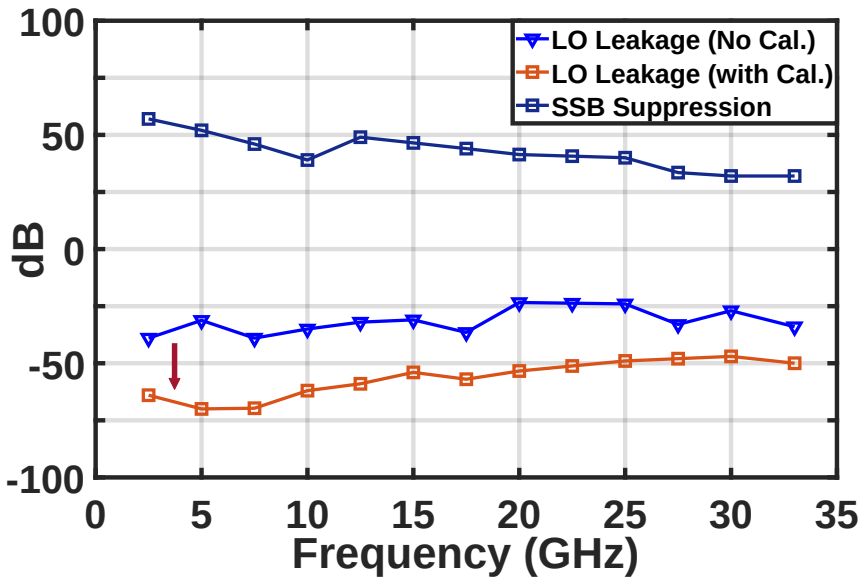


Figure 3.20: SSB and LO Leakage measurements.

3.4.3 I/Q Modulator Measurements

Fig. 3.19a presents the measurement setup used to evaluate the wideband I/Q modulator. The fully differential modulator chip occupies 1 x 1.4 mm^2 area and is fabricated in the Global-Foundaries 45 nm SOI CMOS process (Fig. 3.19b). The differential LO ports are driven by a 1 MHz - 70 GHz network analyzer (Keysight N5247A PNA-X). The differential and quadrature IF inputs are driven with two channels from the Keysight M8196 92GSa/s arbitrary waveform generator (AWG).

Four phase-matched SMA cables are connected to a 2.9 mm GSSGSSG probe for the quadrature I and Q data inputs, as shown in Fig. 3.19c. Wideband 10 dB attenuators are used at the output of the AWG channels in order to use the external DACs at their full scale, thus maximizing the dynamic range available from the DACs. The differential RF output signal is measured using an E4448A spectrum analyzer up to 50 GHz and a 160 GSa/s DC-63 GHz Keysight DSAZ634A real-time oscilloscope. The dynamic range of the oscilloscope is limited to approximately 35 dB at its widest capture bandwidth, and sets the dynamic range of the measurement setup.

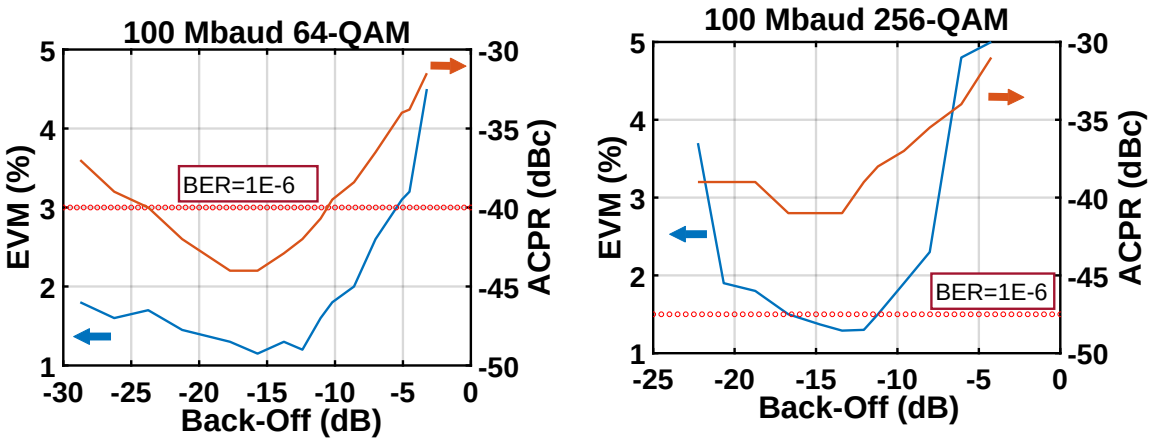
SSB Suppression and Carrier Feedthrough

In order to evaluate the dynamic range of the transmitter, it is configured as a single-sideband (SSB) transmitter to measure LO leakage and SSB suppression. Furthermore, SSB suppression will indicate the quality of the IQ generator in terms of its amplitude and phase mismatch. A 100 MHz tone is generated using an arbitrary waveform generator (AWG) that is controlled in software by MATLAB, such that the first channel of the AWG generates the 100 MHz sinusoidal tone and the second channel generates the Hilbert transform (quadrature signal in the case of a single tone) of the signal in channel 1. The two channels are synchronized and phase adjusted such that the two quadrature signals arrive at the I and Q input data pads of the die with correct phases. The output of the transmitter is then connected to a spectrum analyzer, and the LO leakage and SSB suppression can be readily calculated.

Fig. 3.20 shows the measured sideband suppression and LO leakage as a function of the LO frequency. Sideband suppression is measured by first determining the phase setting that accounts for the phase mismatch between the I and Q paths at 100 MHz that is due to the measurement setup, then the LO frequency is swept without changing any phase settings from the AWG, in order to measure the true performance of the chip. SSB suppression better than 30 dB over the entire band is achieved. Furthermore, Fig. 3.20 shows that the LO leakage can be as high as -25 dBc close to 35 GHz and prior to calibration. The increase in carrier feedthrough with frequency is expected, as has been discussed in section 3.2.3.

After calibration the leakage levels are significantly improved down to a worst-case level of -50 dBc. It is worth pointing out that the optimum calibration settings vary for each LO carrier, even though the IF frequency is fixed at 100 MHz. This is due to frequency dependent leakage mechanisms such as the direct LO to RF leakage through the transistor parasitics and supply network. The output of the transmitter is measured in a single-ended fashion, which further contributes to the carrier feedthrough numbers. This is because external or on-chip baluns are limited in bandwidth, and are not capable of covering the DC-60 GHz frequency range.

Given the worst-case SSB and carrier feedthrough of 35 dB and -50 dBc, a worst-case EVM of approximately 1.8 %, limiting the use of very-high order modulation formats such as 256-QAM and 1024-QAM to carrier frequencies below 20 GHz.



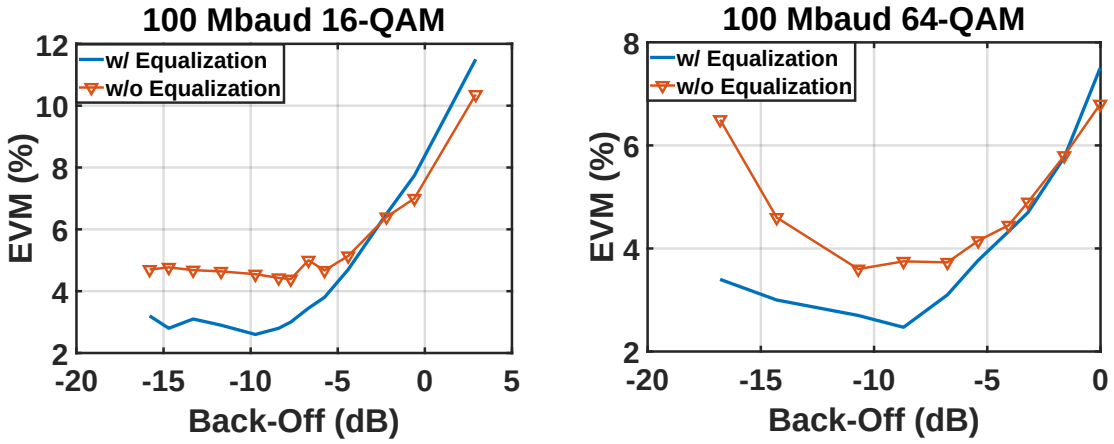
(a) (b)

Figure 3.21: EVM and ACPR measurements vs. back-off level at 5 GHz.

Linearity Measurements

Carrier feedthrough and limited SNR are the two main challenges for wideband direct-conversion transmitters. The dynamic range of the system is limited by these two factors and is determined in the modulation stage. Therefore, direct-conversion modulators must maintain low carrier leakage value while also adding contributing minimum noise. Furthermore, carrier leakage is weakly dependent on the RF output level, and therefore, it is desirable to maximize the modulator RF output power, by reducing the back-off level as long as the resulting non-linear distortion is within acceptable levels.

Fig. 3.21 presents measured EVM and ACPR results at a 5 GHz carrier for 64-QAM and 256-QAM. As expected, both ACPR and EVM are minimum at certain back-off levels, above which they degrade due to no-linear distortion. Increasing the back-off level degrade EVM and ACPR due to CFT and SNR degradation.



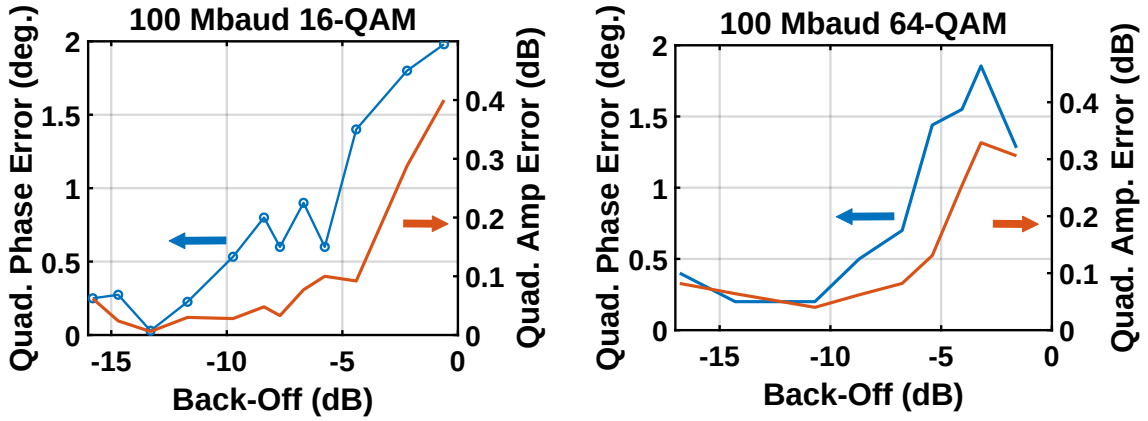
(a) (b)

Figure 3.22: Equalization effect at a 28 GHz carrier.

Also, it can be observed that for a given BER level, the back-off level required increases as the modulation order increases. In this particular case, 256-QAM required higher back-off levels compared to 64-QAM.

Fig. 3.22 shows the benefit of applying linear equalization to the measured EVM of 100 Mbaud signals at a 28 GHz carrier. In general, significant improvement in the measured EVM is observed, even over narrow modulation bandwidths. At 100 MHz bandwidth, the frequency response of the circuit can be assumed ideal, and therefore any ISI resulting from non-ideal amplitude and phase response of the channel arises from the measurement setup. Furthermore, as the back-off level decreases the EVM becomes dominated by non-linear effect and equalized and non-equalized results becomes comparable.

Fig. 3.23 presents the measured quadrature amplitude and phase errors as a function of the back-off level. Initially, the quadrature amplitude and phase errors are small owing to the accuracy of the digital CML IQ generator. As the input power to the transconductance stage increases, AM-AM and AM-PM distortion leads to data-dependent quadrature and phase errors. Simulations of the double-balanced mixer revealed 2 degrees of AM-PM at P1dB, which directly translates to phase errors in the Cartesian IQ transmitter.



(a) (b)

Figure 3.23: Quadrature amplitude and phase errors vs back-off level.

Single-Carrier Measurements

Single-carrier modulation measurements of the I/Q modulator were carried out up to 63 GHz. Since the differential signal source is limited to 70 GHz, the transmitter operates in direct-conversion mode up to 35 GHz and heterodyne with SSB rejection above 35 GHz.

Fig. 3.24 presents the measured EVM versus data rate for various frequency carriers and modulation formats up to 60 GHz. Measurements of the modulator proved its capability of supporting a maximum baud rate of 60 Gbaud/s in QPSK (120 Gbps), 50 Gbaud/s in 16-QAM (200 Gbps), 40 Gbaud/s in 32-QAM (200 Gbps), and 20 Gbaud/s in 64-QAM (120 Gbps). The measurement were carried out at 5-dB back-off and with an expected worst case BER better than 1e-3. To our knowledge, this the first demonstration of transmit data rates exceeding 100 Gbps in silicon technologies. Fig. 3.25 presents examples of measured constellations at 28 GHz.

Table 3.1 presents a comparison with state of the art modulators and transmitters. A significant improvement is demonstrated in the data throughput and energy/bit efficiency. The output power can be increased using wideband distributed amplifier topologies while maintaining record energy/bit efficiency.

Table 3.1: Comparison with state of the art ultra-wideband transmitters in silicon technologies.

Reference	[65]	[66]	[67]	**This Work**
Technology	45nm SOI	CMOS	65nm CMOS	45nm SOI
Frequency [GHz]	1-32	60	60	DC-60
Modulation (Data Rate/EVM) [Gb/s/%]	**16QAM** (26/7.9%) **32QAM** (30/6.9%) **64QAM** (12/4%)	**QPSK** (16/25%) **16QAM** (27.8/7%)	**16QAM** (28.16/<5%) **64QAM** (42.24/<5%) **128QAM** (12.32/<3%)	**16QAM** (200/12%) **32QAM** (200/7.6%) **64QAM** (120/6.5%) **256QAM** (16/1.7%)
Architecture	I/Q 2x6 bit RF-DACs	Digital-TX Polar RF-DACs	I/Q with calibration circuitry and external BB DACs	I/Q with external BB DACs
Dynamic Range (in 1 GHz)	-	18	38*	50
Peak Data Rate [Gbps]	26	27.8	42	200
OP1dB [dBm]	18**	5**	6.5	-10
Power Cons. [mW]	644	316*	169	200***
Energy Eff. [pJ/b]	16	11.4	3.57	1

* Estimated
** Psat
*** Including I/Q generation

Multi-Carrier Measurements

Single-channel wideband modulations are highly susceptible to channel impairments such as multi-path fading and are generally difficult to process efficiently in baseband. Therefore, carrier aggregation techniques are expected to continue to be a driving technology in future wideband communication systems. Inter-band carrier aggregation of mm-wave systems is of particular interest for ultra-high data rate scenarios.

Fig. 3.26 demonstrates an example of an ultra-wideband 5G carrier aggregation link, where 2 x 8 Gbaud 16-QAM signals are modulated with 28 GHz and 39 GHz carriers, resulting in a record aggregate data rate of 64 Gbps.

Fig. 3.27 presents another mm-wave carrier aggregation scenario where 28 GHz and 60 GHz carriers were simultaneously modulated, each at 100 Mbaud and in 16-QAM, resulting in 800 Mbps aggregate data rate. The transmitter operates in direct-conversion mode for the 28 GHz carrier and as an image-rejecting wideband-IF transmitter at 60 GHz.

Similarly, multi-carrier OFDM waveforms are expected to be highly used in mm-wave 5G due to their spectral efficiency and efficient MIMO implementation. Fig. 3.28 presents the measurement of a 100 MHz 64-QAM 52-subcarriers OFDM signal at 28 GHz, with -31.8 dB EVM at 10-dB back-off.

3.5 Conclusion

A state-of-the-art DC-60 GHz I/Q modulator/transmitter chip in 45 nm SOI CMOS was presented. The 1.4 mm^2 modulator consists of a wideband quadrature signal generator, wideband buffers and two current-combined DC-100 GHz low-noise double-balanced mixers driven in quadrature. The I/Q modulator achieves 200 Gbps in 16-QAM (50 Gbaud/s), while consuming 200 mW, resulting in record 1 pJ/bit modulation efficiency. In addition to backhaul links, the modulator is an attractive and cost-effective alternative to short-range optical links for data center interconnects (DCI) applications. Future work may include increasing the modulator output power to alleviate the need for an additional power amplifier stage.

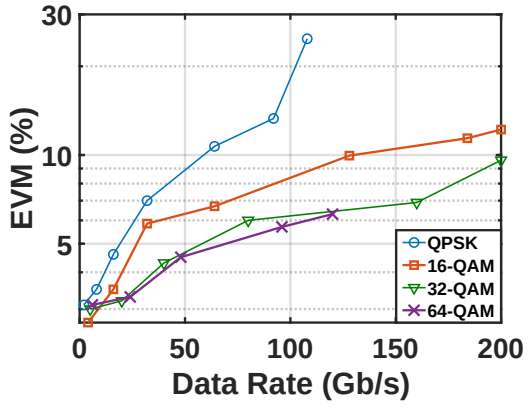
3.6 Acknowledgment

This work was supported by the UCSD Center for Wireless Communications (CWC) and Global Foundries.

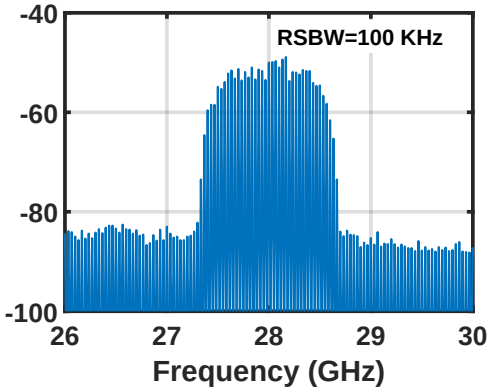
Chapter 3, in part, has been submitted for publication of the material as it may appear in: H. Al-Rubaye and G. M. Rebeiz, “A 200-Gbps I/Q Modulator in 45 nm SOI CMOS for

Ultra-Wideband 5G Radios," submitted to the *IEEE European Solid-State Circuits Conference (ESSCIRC)*, 2018. The dissertation author was the primary investigator and author of this paper.

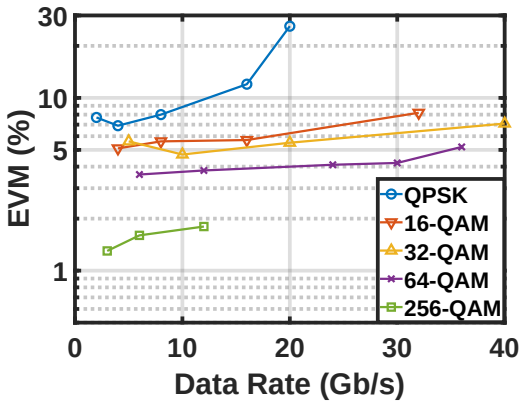
Chapter 3 is also, in part, contains material that is currently being prepared for submission for publication as may appear in: H. Al-Rubaye and G. M. Rebeiz, "Analysis and Design of Wideband CMOS IQ Modulators," *IEEE J. Solid-State Circuits*, in preparation. The dissertation author was the primary investigator and author of this material.



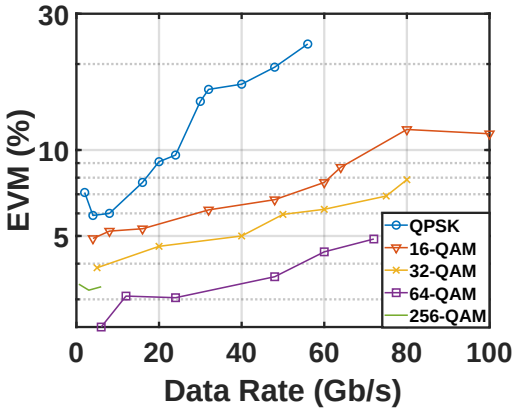
(a) 28 GHz



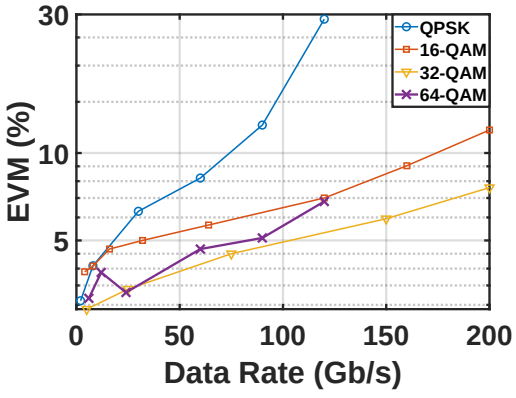
(b)



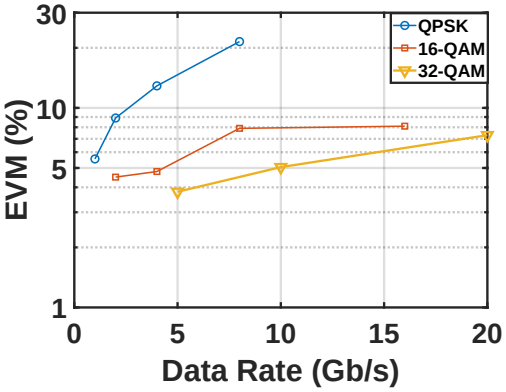
(c) 5 GHz



(d) 15 GHz



(e) 35 GHz



(f) 60 GHz

Figure 3.24: (a) Measured EVM vs. baud rate for different modulation formats at a 28 GHz carrier, (b) Measured output spectrum of a 1-Gbaud 16-QAM modulated signal with a root-raised-cosine filter applied (roll-off factor $\alpha = 0.15$), (c) 5 GHz measurements, (d) 15 GHz measurements, (e) 35 GHz measurements, (f) 60 GHz measurements.

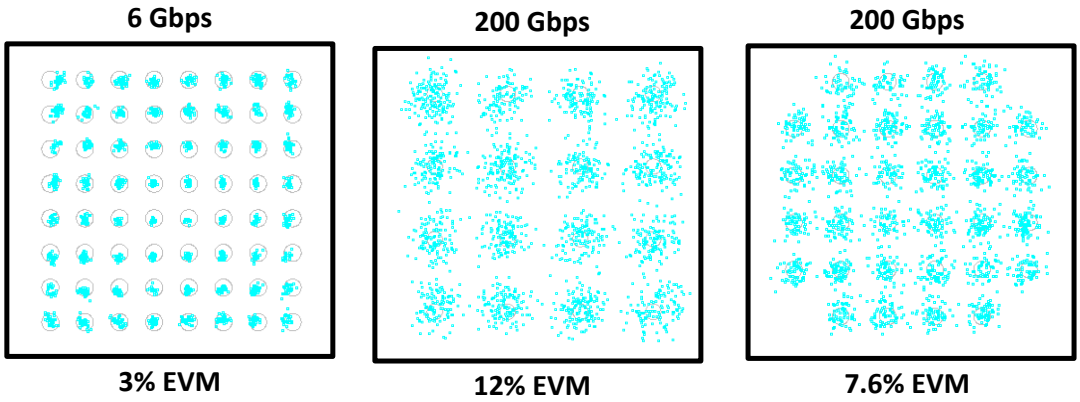
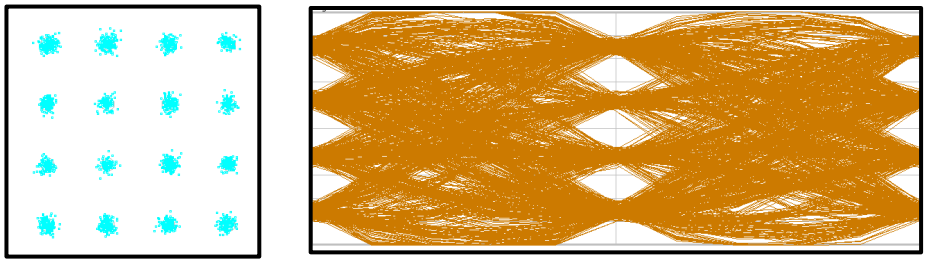
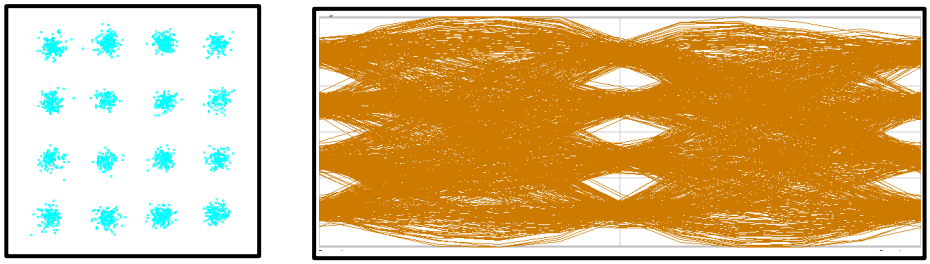


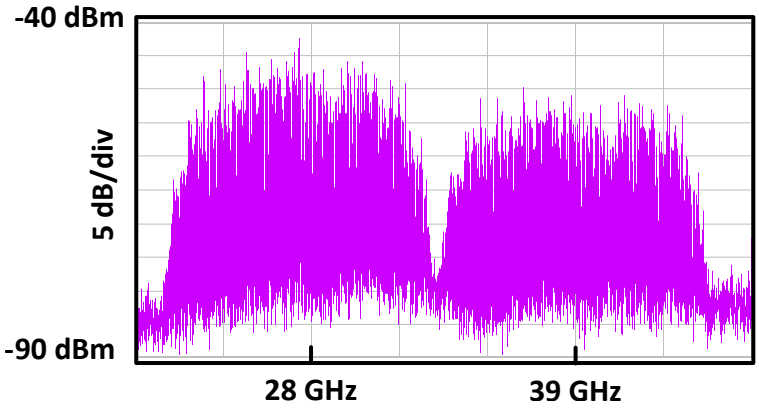
Figure 3.25: Measured constellations at 28 GHz for various modulation formats, demonstrating low-EVM at 64-QAM and peak data rate of 200 Gbps in 16-QAM and 32-QAM.



(a) 32 Gbps, 4.8% EVM at 28 GHz.



(b) 32 Gbps, 7% EVM at 39 GHz.



(c) Measured spectrum showing simultaneous transmission of the two carriers.

Figure 3.26: Demonstration of 5G mm-wave carrier aggregation at 28 GHz and 39 GHz.

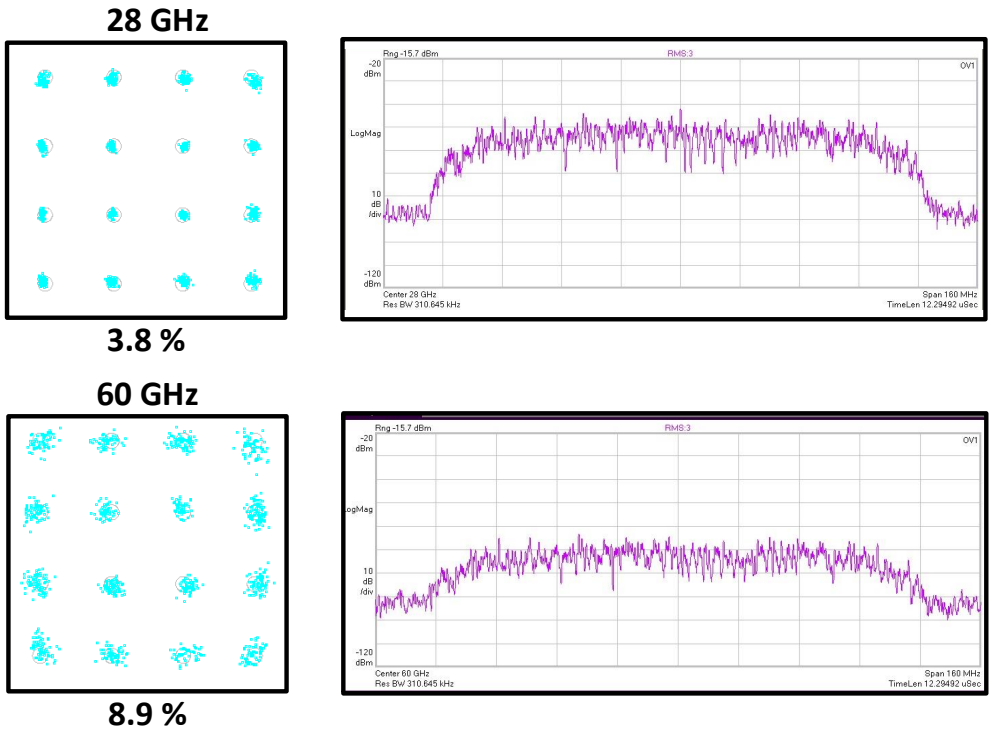


Figure 3.27: Demonstration of 5G mm-wave carrier aggregation at 28 GHz and 60 GHz.

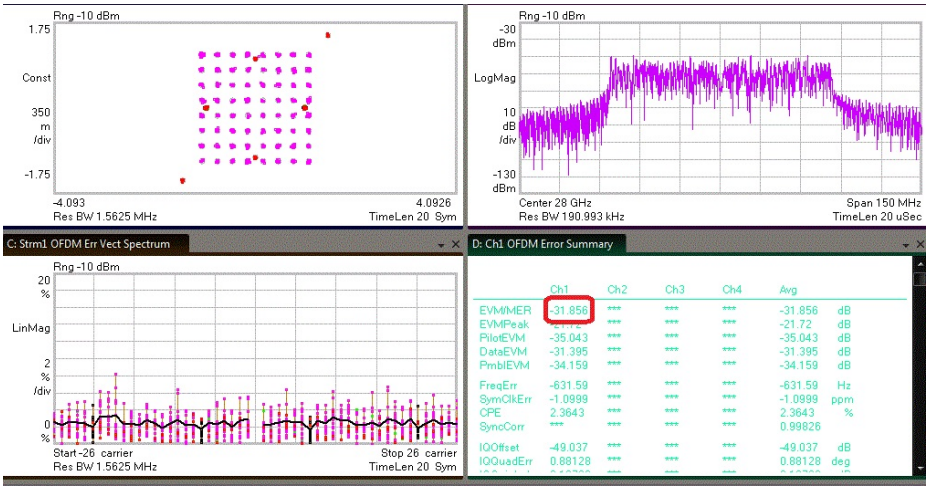


Figure 3.28: Measured spectrum and constellation of 100 MHz 64-QAM OFDM signal at 28 GHz with -31.8 dB EVM.

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