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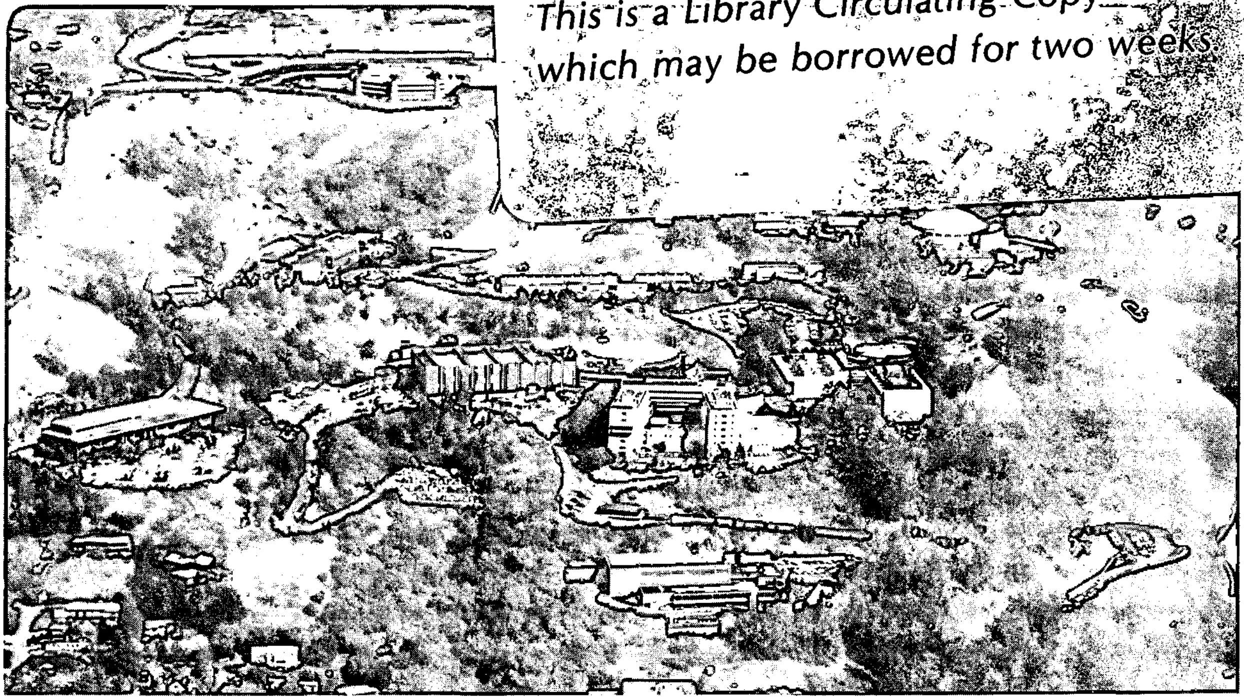

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SILICON RADIATION DETECTORS WITH OXIDE CHARGE STATE COMPENSATION

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Abstract

This paper discusses the use of boron implantation on high resistivity P-type silicon before oxide growth to compensate for the presence of charge states in the oxide and oxide/silicon interface. The presence of these charge states on high resistivity P-type silicon produces an inversion layer which causes high leakage currents on N^+P junctions and high surface conductance. Compensating the surface region by boron implantation is shown to result in oxide passivated N^+P junctions with very low leakage currents and with low surface conductance.

Introduction

The recent popularity of silicon strip detectors for particle physics applications has resulted in considerable interest in the properties and performance of oxide-passivated planar diode structures(1). Proposed large arrays involve detector strips 10 to 50 μm wide, 1 to 2 cm long, separated by a surface covered by silicon dioxide 10 to 50 μm wide. A high inter-strip resistance (surface conductance $< 5 \times 10^{-9}$ S/□) is required to reduce signal interactions between the strips, while low leakage currents (< 10 nA/cm^{-2}) are desirable to minimize the noise and power consumption. Furthermore, the detectors should be stable, largely independent of ambient conditions, and should exhibit good radiation tolerance.

At present most silicon strip detectors are based on the oxide passivated P^+N diode structure shown schematically in Fig. 1a. The P^+ region is formed either by boron ion implantation or by diffusion through a hole etched in the silicon dioxide. The silicon dioxide not only serves as a mask for the implantation or diffusion, but also serves as protective layer for the P^+N junction edge against ambient effects.

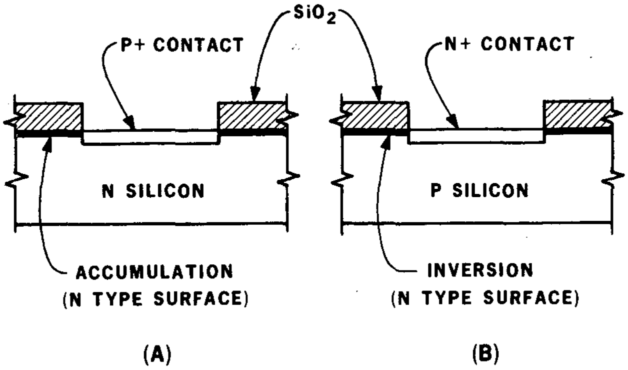

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Fig. 1. A schematic representation of the P^+N and N^+P diode structures. The electrons which are attracted to the Si/SiO$_2$ interface are shown as a heavy line in the figures.

The alternative N^+P structure, shown in Fig. 1b, can be made by implantation or diffusion of phosphorus or arsenic through the oxide mask into the high resistivity bulk P material. Again the silicon dioxide acts both as a mask and a passivating layer.

While the P+N structure has yielded devices with very impressive characteristics(2), the alternative N+P structure has not been employed on strip detectors due to the generally higher leakage currents and lower inter-strip resistance. The N^+P structure does, however, offer the possibility of improved radiation resistance. For thin silicon detectors, the important radiation damage effects are the increase in leakage current and the conversion of the bulk material to P type with increasing fluence(3). The increase in the acceptor-like centers leads, in the P^+N device, to the eventual conversion of the N bulk material to P type and the failure of the detector. For N^+P devices an increase in the acceptor concentration results in a higher voltage being required to fully deplete the device. In addition, the "damage constant" which relates the increase in leakage current due to the fluence, is about a factor of five lower for P-type silicon than for N type. For these reasons it is therefore important to investigate the N^+P structure as an alternative to the present P^+N devices employed on strip detectors.

The silicon dioxide passivation on both of these structures contains positive charge centers, and the presence of these charge centers causes the substantially higher leakage currents and lower inter-strip resistance on the N^+P structures than on similar P^+N designs thereby obscuring a comparison of device radiation tolerance.

In this paper we describe a procedure for compensating these oxide charge centers thereby enabling N^+P diodes to be fabricated with leakage currents and inter-strip resistances similar to the P^+N structures.

N^+P Junctions

The Si/SiO$_2$ System

Commercial interest in the characteristics of the Si/SiO$_2$ interface that occurs in metal-oxide-semiconductor (MOS) structures has resulted in this being perhaps the most thoroughly studied and best understood solid phase system(4). The model(5) that has evolved to describe the charge effects in this system is shown in Fig. 2. While a complete review is well beyond the scope of this paper, salient features can be highlighted. Four kinds of charge centers have been identified: mobile ionic charge, oxide trapped charge, fixed oxide charge, and the interface trapped charge. With careful attention to processing, only the fixed oxide charge density, N_f, and interface trap density, D_{it}, are of importance in detector fabrication. Methods for characterizing these charge centers are well developed and representative values that we have measured for two different oxide growth conditions on [111] orientation silicon are given in Table 1.

Table 1. Oxidation Conditions and Oxide Parameters

Oxide growth conditions	D_{it} ($cm^{-2}\ eV^{-1}$)	N_f (cm^{-2})
Steam: 120 minutes at 1000°C	1 to 4×10^{11}	2 to 3×10^{11}
Oxygen + Cl: 180 minutes at 1060°C	4 to 8×10^{10}	1 to 2×10^{11}

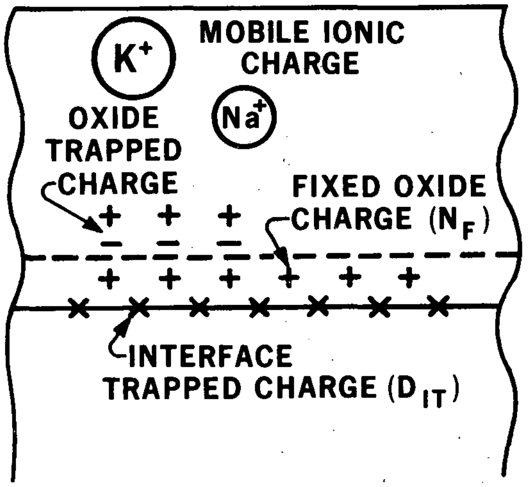

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Fig. 2. A model of the oxide charges present in the Si/SiO_2 system(5).

Surface Inversion

Both of these oxide charge centers, N_f and D_{it}, are normally positive which attracts electrons to the Si/SiO_2 interface. If their density is sufficiently large, these centers can cause the electron concentration at the silicon surface to exceed the bulk impurity concentration and consequently, in the case of high purity P-type silicon, cause the surface to become N type (i.e., to invert). The oxide charge density, N_o, required to cause this inversion is given by(6),

$$N_o = 2\lambda_i \sqrt{n_i N_A \ln(N_A/n_i)}\ \ cm^{-2} \qquad (1)$$

where λ_i is the intrinsic Debye length (λ_i = 28 μm at 290 K), n_i the intrinsic carrier concentration ($n_i = 1 \times 10^{10}\ cm^{-3}$ at 290 K), and N_A, the acceptor impurity concentration in the P-type silicon. This relationship is plotted in Fig. 3.

The resistivity range used to fabricate radiation detectors on P-type silicon is 10 ohm-cm to 20 K ohm-cm which allows fully depleted 10 μm to 500 μm thick devices to be operated with a bias voltage of about 100 volts. However, as was noted earlier, the fixed oxide charge density and the interface trap level density are in the $10^{11}\ cm^{-2}$ range. Consequently it can be seen from Fig. 3 that for oxide passivated detectors fabricated on P-type silicon in the above resistivity range, the surfaces will be N type. This surface inversion causes high leakage currents on N^+P devices as the junction does not terminate at the metallurgical boundary, but extends across the surface thereby allowing the injection of carriers into the bulk. Further, for N^+P strip detectors, this N surface results in a low inter-strip resistance since the surface structure is N^+NN^+.

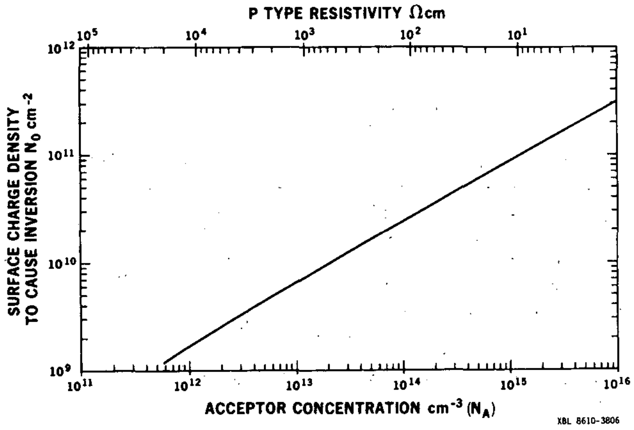

Fig. 3. The oxide charge density, N_o, required to cause the inversion of P-type crystal surface as a function of the acceptor concentration in the crystal.

Junction Breakdown Voltage

The presence of this N surface was noted in early publications on oxide-passivated N^+P junction devices(7) and a light P diffusion was used prior to the oxide growth to compensate the surface(8). Since a typical oxide charge surface density is about $1 \times 10^{11}\ cm^{-2}$, Fig. 3 indicates that a P-type bulk concentration of greater than $1 \times 10^{15}\ cm^{-3}$ is required to prevent inversion of the surface. However, the junction breakdown voltage is also dependent on the bulk impurity concentration. The relationship between the breakdown voltage (abrupt junction) and the bulk resistivity is shown in Fig. 4(9). For device operation of 100 volts, this figure suggests that an upper limit on the bulk impurity concentration is about $5 \times 10^{15}\ cm^{-3}$. Therefore from Figs. 3 and 4 and for 100-volt operation, the concentration of the surface compensating impurity, N_s, should be in the range:

$$1 \times 10^{15} < N_s < 5 \times 10^{15}\ cm^{-3}. \qquad (2)$$

Control of dopant impurities to this precision using a diffusion process is difficult and therefore N^+P devices are rarely made with this technique. However, implantation allows precise impurity control and in the following we describe our results using boron implantation to compensate the oxide charge states.

Process Modeling

The surface concentration of interest is that present after implantation and oxidation. We therefore employed the process modeling program, SUPREM(10), to examine the results of various processing sequences. Figure 5 shows a representative result from this program. Here the impurity concentration is plotted as a function of depth for an implanted dose of 5×10^{11} boron cm^{-2} at 25, 65, and 100 keV with a subsequent oxidation (100 min at 1000°C in steam followed by 60 min at 1060°C in dry O_2 + 3% HCl). As can be seen from the figure, the boron impurity concentration at the Si/SiO$_2$ interface is 3 x 10^{15} cm^{-3} and the concentration profile is flat for approximately 1 μm into the silicon from the interface. Since the extrinsic Debye length at an impurity concentration of 3 x 10^{15} cm^{-3} is 0.065 μm, the high resistivity bulk silicon is effectively screened from the oxide interface.

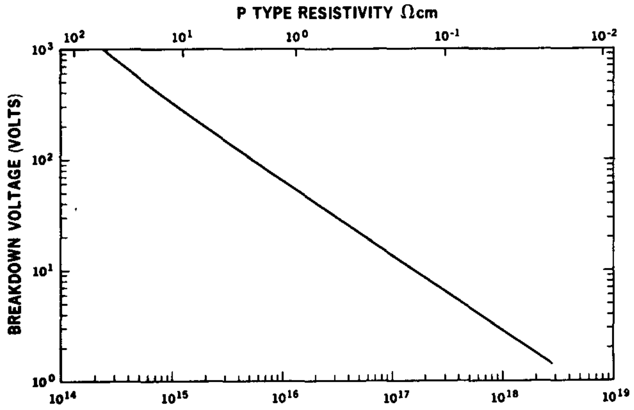

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Fig. 4. The breakdown voltage for an abrupt junction as a function of the acceptor impurity concentration.

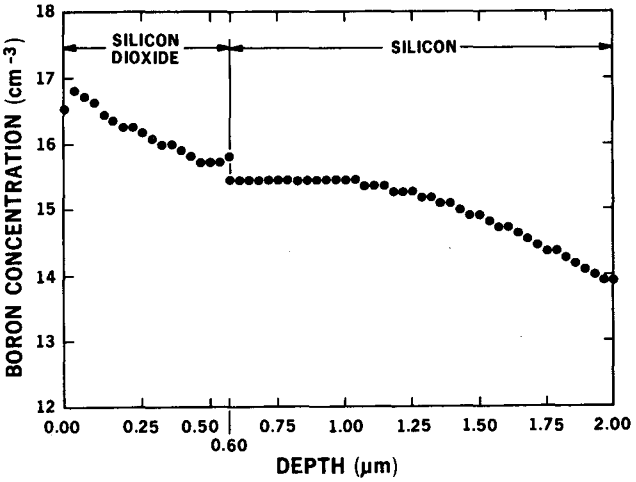

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Fig. 5. The boron implantation profile (calculated with SUPREM[10]) in the oxide and P-type silicon after oxidation.

For an initial comparison of the device performance with and without oxide charge state compensation, we have fabricated diodes using our conventional phosphorous diffusion process to produce the N$^+$P junctions. Of course the presence of the compensating boron implantation changes the phosphorous doping profile as compared with diodes lacking the compensation. The extent of this change is shown in Fig. 6 where the profiles (from SUPREM) are plotted for the phosphorous diffusion with and without the compensating boron. As would be expected, the presence of the boron steepens the phosphorous profile and in effect makes the N+ contact "window thickness" smaller than it would be otherwise.

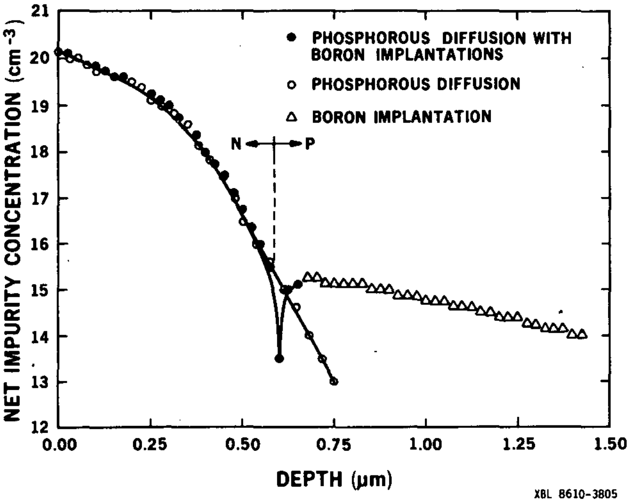

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Fig. 6. The phosphorous diffusion profile (calculated by SUPREM[10]) with and without the compensating boron implantation.

Results

The results to be discussed are on devices which have the structure shown in Fig. 7 where the dopant profile in the bulk silicon for the cross-section at A is given in Fig. 5 and the profile at B is given in Fig. 6. Briefly, the processing sequence employed is as follows:

a) Boron implantation into a chemically-polished wafer,
b) Oxidation,
c) Oxide mask and etch,
d) Phosphorous diffusion,
e) P$^+$ contact on the opposite face.

The final processing step, e), is neither shown in Fig. 7 nor in the profiles. We normally employ a boron implantation dose of 2 x 10^{13} cm^{-2} at 25 keV with an anneal at 800°C for 30 min followed by a gold evaporation to form this P$^+$ contact.

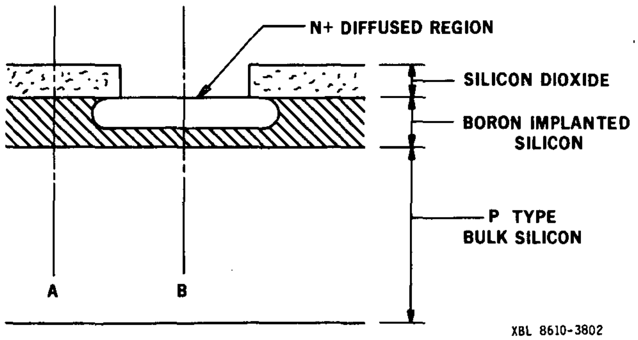

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Fig. 7. A cross-section of an oxide charge-state compensated device.

Current-Voltage Measurements

Representative current voltage characteristic for 5 mm diameter test devices fabricated on 4 k ohm-cm P-type silicon using the preceding processing sequence is shown in Fig. 8. For comparison, the published leakage current curve(11) for a similar sized P^+N diode is also shown in the figure. As can be seen, the leakage currents of the two structures are comparable.

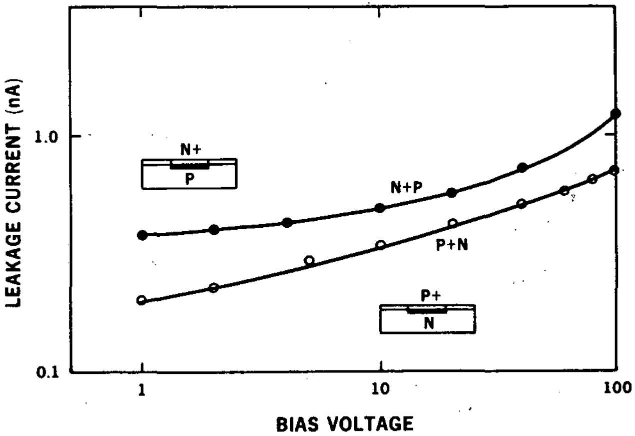

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Fig. 8. A comparison between the leakage currents of a 5 mm diameter N^+P device with oxide charge state compensation and that of published P^+N device(2) of similar size.

Surface Conductance

As noted in the introduction, the effective surface conductance on the N^+P diode structure needs to be low if this technology is to be applied to the high energy physics multi-strip detectors. Measurements on strip detectors, made using the process described here, with N^+ diffused strips separated by a 100 μm wide and 2.5 cm long Si/SiO_2 surface region yielded an effective surface conductance, when biased at the operating voltage, of 1×10^{-11} S/□ which is considerably lower than the 5×10^{-9} S/□ design goal given in the introduction.

Radiation Tolerance

For the reasons noted earlier and because of the screening by the boron implantation of the high resistivity bulk from the oxide interface, we expect these N^+P devices to have good tolerance to radiation damage. Preliminary results of exposing some samples to 1×10^{12} cm^{-2} thermal neutrons are shown in Table 2.

Table 2. Neutron Irradiation Effects

	Before Irradiation	After Irradiation
I 10 V (nA)	3.5	51.2
I 100V (nA)	6.8	125.0
D_{it} (cm^{-2} eV^{-1})	1.5×10^{11}	1.8×10^{11}
N_f (cm-2)	1.2×10^{11}	1.2×10^{11}
τ (μs)	330	28

Assuming that the entire leakage current is due to bulk generation, the effective minority carrier lifetime, τ, listed in Table 2 was obtained from the leakage current, I,(12)

$$I = \frac{qn_i WA}{2\tau}$$

where q is the electronic charge, W the depletion depth and A the device area. From Table 2 the oxide parameters D_{it} and N_f appear to be relatively unaffected by the irradiation. We have therefore made the simplifying assumption that the increase in leakage current is solely due to a decrease in the minority carrier lifetime in the bulk. However, the surface generation velocity was not measured on these devices and a change in this parameter would affect the leakage current and therefore, the estimated carrier lifetime.

The neutron dose did not change the acceptor concentration in these devices as the depletion voltage was the same before and after irradiation.

Discussion

The use of a shallow boron-implanted layer to compensate for the effects of the oxide charge states has been demonstrated to yield N^+P structures with low leakage currents and low surface conductance. Several areas need further examination before this technique can be applied on a large scale to the fabrication of detector arrays: 1) The dependence of the surface compensation on subsequent processing steps requires further study. For example, improvements in device leakage current may be realized by using an arsenic implantation with a stepped oxide(13) to form the N^+ contact. But this may require a different boron profile than was reported here. 2) The radiation tolerance of these devices needs considerably more examination. The radiation damage results presented illustrate that better characterization of the interface state properties(14) is required to separate the radiation effects in the bulk and at the surface of these devices.

Conclusions

It has been demonstrated that a shallow, low dose boron implantation prior to oxidation can be used to compensate the charge states that occur at the Si/SiO_2 interface. With this method, N^+P diodes with characteristics similar to P^+N devices are realizable. This technique should allow a valid comparison to be made between these two structures as to their relative superiority for the fabrication of the large arrays of strip detectors that are proposed for many high energy physics particle tracking schemes.

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References

1. Proceedings of the Third European Symposium on Semiconductor Detectors, Munich, November 1983, Nucl. Inst. and Methods, 226, 1984.

2. J. Kemmer, "Fabrication of Low Noise Silicon Detectors by the Planar Process", Nucl. Inst. and Methods, 169, 1980, pp 499-502.

3. H.W. Kraner, "Radiation Damage in Semiconductor Detectors", IEEE Trans N.S., NS-29, 1982, pp 1088-1100.

4. E.H. Nicollian and J.R. Brews, MOS Physics and Technology, Wiley, New York, 1982.

5. B.E. Deal, "Standardized Terminology for Oxide Charge Associated with Thermally Oxidized Silicon", IEEE Trans E.D., ED-27, 1980, pp 606-607.

6. S.M. Sze, Semiconductor Devices, Physics and Technology, New York, Wiley, 1985, Ch. 5, p 191.

7. T.C. Madden and W.M. Gibson, "Silicon Dioxide Passivation of p-n Junction Detectors", The Review of Scientific Instruments, Vol. 34, No 1, 1963, pp 50-55.

8. W.L. Hansen and F.S. Goulding, "Oxide-Passivated Silicon p-n Junction Particle Detectors", Nucl. Inst. and Methods, 29, 1964, pp 345-347.

9. S.M. Sze and G. Gibbons, "Effect of Junction Curvature on Breakdown Voltage in Semiconductors", Solid State Electronics, 9, 1966, pp 831-845.

10. C.P. Ho, J.D. Plummer, S.E. Hansen, and R.W. Dutton, "VLSI Process Modeling - SUPREM III", IEEE Trans E.D., ED-30, 1983, pp 1438-1453.

11. J. Kemmer, op cit.

12. A.S. Grove, Physics and Technology of Semiconductor Devices, New York, Wiley, 1967, Ch. 6, pp 176-177.

13. J. Kemmer, Patent No. DE 3003391 A1

14. W.D. Eades, J.D. Shott, and R.M. Swanson, "Refinements in the Measurement of Depleted Generation Lifetime", IEEE Trans E.D., ED-30, 1983, pp 1274-1277.

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