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Power Dense DC-DC Converters for Electric Transportation: Design Optimization and
Practical Considerations

By

Sahana Krishnan

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Robert Pilawa-Podgurski, Chair
Chenming Hu Assistant Professor Jessica Boles
Professor Duncan Callaway
Dr. Pradeep Shenoy

Spring 2026

Power Dense DC-DC Converters for Electric Transportation: Design Optimization and
Practical Considerations

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Abstract

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Professor Robert Pilawa-Podgurski, Chair

Advancements in vehicle technology and transportation electrification come with changing voltage architectures to support higher power demands. Hybrid switched-capacitor converters and other novel converter architectures are attractive solutions in this application space due to their ability to achieve high power densities and efficiencies. However, there are challenges associated with the adoption and implementation of these converters into automotive subsystems. This dissertation focuses on the design optimization of novel power converter topologies while addressing practical challenges vital to transportation. The critical challenges addressed in this thesis encompass electromagnetic interference, dynamic operation, isolation, and output voltage regulation. Through several hardware design case studies, these challenges are addressed to further advance electronic systems in vehicular environments.

To my family, with love and gratitude.

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Chapter 1

Introduction

1.1 Introduction

Global efforts to decarbonize transportation have accelerated the transition to vehicle electrification. This has a positive influence on the reduction of carbon dioxide emissions, and we already see many electrified passenger vehicles as well as medium- and heavy-duty (MDHD) vehicles on the roads today. The amount of information and power that needs to be processed in a given electrical subsystem within these vehicles is only increasing, and this large modern current draw makes higher voltage distribution necessary to keep up with power demands. The higher voltage distribution allows for a reduction in current to maintain the same power level, and this reduction in current corresponds to lower conduction losses.

Both low-voltage and high-voltage buses in vehicles have seen an increase in voltage. This architectural change can influence aspects of vehicle design and performance such as charging time, cabling thickness, and therefore losses through this cabling. On the low-voltage side, increasing the bus voltage of the conventional 12 V bus to 48 V allows for both reduced transmission losses and cabling weight in automotive powertrains. Internal combustion engine (ICE), hybrid electric vehicles, and fully electric vehicles (EVs) exhibit this trend. This trend also extends to higher voltage buses where the 800 V architecture is a significant increase from the more common 400 V high-voltage battery seen in EVs today.

High-performance, lightweight power conversion is necessary to keep up with the higher voltages and increasing power demands in vehicles and other transportation. While high performance is an imperative aspect of power converter design in transportation, there are many practical aspects that also need to be considered. This dissertation focuses on the design and optimization of novel power converter topologies while addressing practical challenges crucial to transportation applications. Much of the work in this dissertation is motivated by the need to transition more of these novel topologies into industry. The practical challenges that are addressed are:

- electromagnetic interference (EMI)

- dynamic operation
- isolation
- output voltage regulation

Each of the converters discussed in the following chapters takes one or more of these aspects into consideration, and the design, build, and test of several power converters is described in detail.

1.2 Organization of Thesis

Chapter 2: Transportation Electrification Trends and Capacitor-Based Power Conversion

Advancements in transportation electrification require higher voltage architectures, such as 800 V and 48 V, to sustain increasing power levels. While hybrid switched-capacitor converters offer the high power density and efficiency required of power converters in these applications, their adoption into the transportation sector faces critical implementation barriers. This chapter introduces modern power architecture trends within the automotive industry and reviews challenges in electromagnetic interference, dynamic operation, isolation, and output voltage regulation as they pertain to hybrid switched-capacitor converters.

Chapter 3: An EMI-Compliant and Automotive-Rated 48 V to PoL Dickson-Based Hybrid Switched-Capacitor DC-DC Converter

With the move to a 48 V distribution rail in data center power delivery architectures and automotive powertrains, high performance hybrid switched-capacitor (hybrid SC) converters have become an attractive power delivery solution in both spaces. However, automotive power systems present unique design challenges due to strict electromagnetic interference (EMI) and reliability requirements. This work investigates a regulating Dickson-based hybrid SC topology with low inherent EMI, and discusses the incorporation of control-based EMI mitigation techniques such as resonant and above resonant operation, as well as spread spectrum frequency modulation (SSFM). The impact of such techniques on efficiency in hybrid SC converters is explored, as well as passive filter designs to achieve EMI compliance. The proposed filter and modulation schemes enable this converter to meet the CISPR 25, automotive EMI standard. A 150 W hardware prototype is built and tested to demonstrate the merit of hybrid SC topologies for use in 48 V automotive systems. The converter achieves a peak efficiency of 97.1% for 48 V-to-5 V operation and meets CISPR 25, Class 5 EMI regulation limits.

Chapter 4: Discrete-Time Dynamical Modeling of Hard-Charged and Soft-Charged Hybrid Dickson Converters

Hybrid switched-capacitor converters have been investigated for use in data center and automotive applications due to their ability to achieve high efficiencies and power densities at large conversion ratios. One such converter, the hybrid Dickson converter, is popular for its superior volt-amp switch stress characteristics. However, flying capacitor hard-charging can impact the performance of these converters and influence the open-loop dynamic response. This work derives a small-signal model for both hard-charging and soft-charging operation of the hybrid Dickson converter and compares it to a “transformer buck” model that is used to describe hybrid switched-capacitor circuits without considering flying capacitor dynamics. The model is discussed and validated with both simulation and hardware results.

Chapter 5: Design and Implementation of a GaN-Based, Cascaded Isolated DC-DC Converter for Satellite Applications

CubeSat and SmallSat class spacecrafts are gaining popularity and becoming compelling alternatives to traditional, heavy-weight satellites. Power converters for these satellite applications are required to be lightweight and highly efficient. This work proposes a two-stage power converter comprised of a cascaded boost stage and dual active bridge (DAB) stage for satellite applications. The design achieves high performance by utilizing GaN transistors, which are able to withstand radiation conditions in space, as well as planar magnetics to reduce the power-stage volume and mass. A 150 W hardware prototype boasting efficiencies above 92% is built to demonstrate the merit of this cascaded topology for use in low-voltage space systems.

Chapter 6: A High-Performance Flying Capacitor Multilevel DAB DC-DC Converter for Isolated 800 V Automotive Systems

Legacy power architectures in automotive systems are being replaced by higher voltage rails to reduce conduction losses. High-step-down power conversion is therefore necessary to derive auxiliary voltage rails, such as 48 V from the main supply. Isolation is also critical for power converters within these systems to meet safety requirements. This work presents an isolated dc-dc converter for an 800 V automotive application. The converter topology is derived from the dual active bridge converter and the flying capacitor multilevel converter. The primary side of the proposed converter comprises a 6-level flying capacitor multilevel stage. This is connected to the secondary-side full-bridge rectifier via a transformer. The proposed topology is validated in hardware using a planar magnetic implementation of the galvanically isolated transformer. The converter demonstrates greater than 95% efficiency across the full load range at a high conversion ratio making it a compelling alternative to a conventional dual active bridge converter.

Chapter 7: Conclusions

This chapter summarizes and concludes the work presented in this dissertation. Future work and research directions in power electronics for transportation are highlighted.

Chapter 2

Transportation Electrification Trends and Capacitor-Based Power Conversion

2.1 Electrification Trends in Transportation

The transportation sector is responsible for a large portion of global greenhouse gas emissions and in 2022, transportation accounted for approximately 29% of total United States greenhouse gas emissions [2]. To combat these emissions, internal combustion engine (ICE) vehicles are being replaced by battery electric vehicles (EVs) and global EV sales are on the rise. These sales span passenger cars as well as commercial medium- and heavy-duty (MDHD) vehicles such as trucks and buses. In 2024, greater than 20% of passenger vehicle sales were attributed to EVs and this number is only growing [3]. With the growth of electric transportation and the increased technological demand of subsystems such as driver assistance and infotainment, it is evident that the voltage and electrical power requirements within these vehicles are changing as well.

To achieve both increased power capability and weight savings within EVs, moving to higher voltage architectures becomes imperative [4]. Higher voltages can reduce cabling thickness and conduction losses as the required current is reduced at the higher voltage for a given power level. Fig. 2.1 shows the evolution of the voltage architectures in ICE, hybrid, and fully-electric vehicles. These architectures are evolving to balance cost, weight, and performance in vehicle designs [5]. This thesis mainly focuses on the EV architecture and the challenges it presents for dc-dc power conversion.

There are a few things to note in Fig. 2.1. Even as higher voltages such as 48 V are introduced into the vehicle, 12 V architectures may still remain to support legacy loads and local power conversion. Furthermore in modern EVs, the “HV” denoted in Fig. 2.1 represents the high-voltage battery (400 V or 800 V) which presents a safety hazard to humans. Car manufacturers must be aware of where these higher voltages are located in relation to lower

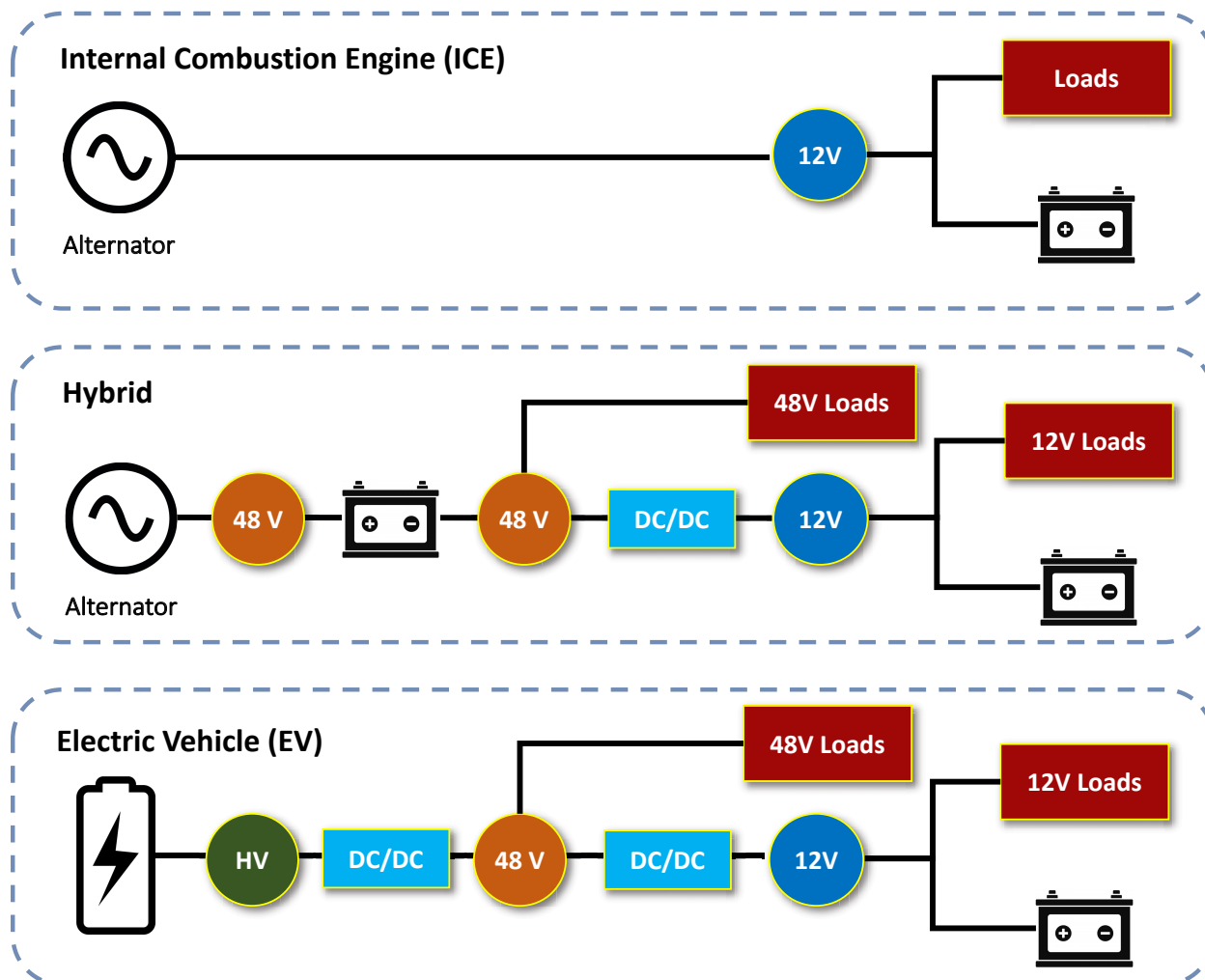


Figure 2.1: Evolution of on-board vehicle voltage architecture for ICE, hybrid, and electric vehicle classes.

voltages and human touch points.

Fig. 2.2 provides a deeper look into an example voltage architecture for an EV along with the necessary power conversion stages for: 1) charging, 2) conversion between high and low voltages, and 3) power delivery to low-voltage loads. The converters that support each of these functionalities in the vehicle have different design requirements and present various challenges in design and implementation. For example, power converters that interface high and low voltages need to be designed with safety in mind while lower voltage converters may serve loads that require strict voltage regulation in the presence of transient events. One way to address these challenges in power electronics for transportation is to innovate on the power converter topologies themselves.

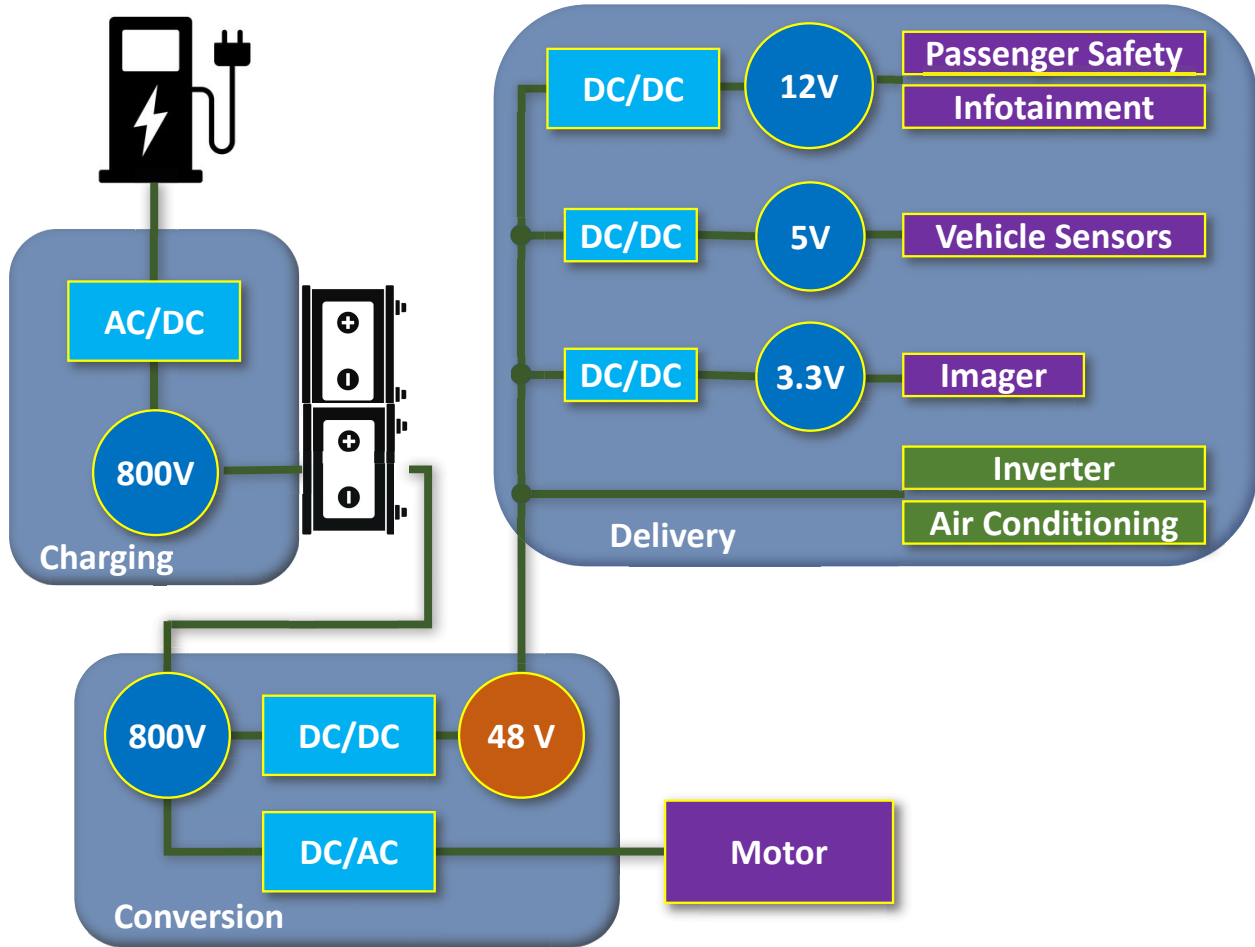
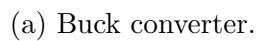


Figure 2.2: Example voltage and power delivery architecture for electric vehicles.

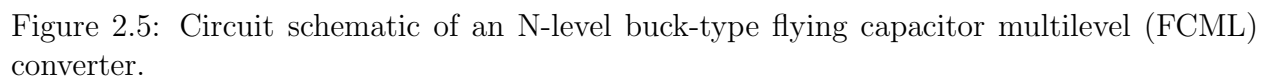
2.2 Hybrid Switched-Capacitor Converters

Hybrid switched-capacitor (SC) converters are power converters that are able to achieve high efficiencies and power densities even at large conversion ratios. Hybrid SC converters rely on capacitors as the primary element of energy storage rather than magnetics, aiming to reduce converter volume with significant gains in converter performance.

The authors in [6] conducted a comprehensive survey of over 500,000 commercially available components comparing the volumetric energy density of capacitors versus inductors. Up to a $1,000\times$ difference in the fundamental energy storage capability between capacitors and inductors is observed in this work, showing that capacitors are more energy dense than inductors [6]. Therefore, capacitor-based power converters are advantageous when optimizing a converter design for weight as the majority of the energy in these converters is now stored in capacitors rather than in large inductors. Furthermore, adding a small inductor to a pure



(b) 2-to-1 hybrid SC converter.



switched-capacitor converter allows for output voltage regulation and soft-charging [7–10] of the flying capacitors. In this way, large impulse currents and corresponding losses associated with hard capacitor charge redistribution are avoided. Even with the addition of a small inductor, converter passive volume still stays competitive as the flying capacitors can now be utilized with a higher capacitor voltage ripple and high efficiency levels are maintained [11, 12].

Figs. 2.3a and 2.3b show a buck converter and a 2-to-1 hybrid SC converter. The inductor at the output of the hybrid SC converter allows for soft-charging of flying capacitor C_1 . Furthermore, Figs. 2.4 and 2.5 show two examples of hybrid SC converters – the hybrid Dickson converter and the flying capacitor multilevel (FCML) converter. Both the hybrid Dickson and the FCML converters will be discussed in more detail within the chapters of this dissertation.

2.3 Suitability for Transportation Applications

Hybrid SC converters have become increasingly popular in applications where both high efficiency and high power density are required, such as data center power delivery. Leveraging the precedent set by the automotive industry, rack-level datacenter voltage architectures [13, 14] are following trends in automotive drivetrain voltage architectures [15, 16] in both the high-voltage and low-voltage domains. For example, both industries are moving towards higher bus voltages such as 800 V and 48 V to mitigate conduction losses. In the data center application space, high efficiency high step-down converters can be used as first-stage intermediate bus converters, to step the 48 V bus in data centers down to the low voltage used at the point-of-load (PoL) by the CPUs and GPUs. Previous work has demonstrated several high performance, large step-down hybrid SC converters used in this application [12, 17–20]. Knowing that these hybrid SC converters have shown promise in data center applications, we would like to apply similar topologies to the transportation space.

Fig. 2.6 shows an example low-voltage architecture on-board an EV. Two options for 48 V to 5 V conversion are shown. The plot on the left shows this conversion using an intermediate 12 V bus and two dc-dc converter stages. The plot on the right shows a single-stage conversion with the 48 V being directly converted to 5 V. Compared to two-stage solutions, the single-stage converter does not suffer from cascading efficiency penalties. However, the larger voltage step-down ratio is a challenge here, and hybrid SC converters excel in this area – we can achieve the high conversion ratio while maintaining high efficiency and power density levels.

2.4 Implementation and Adoption Challenges

There are many challenges that arise when trying to adopt these novel, high-performance topologies into the transportation environment. Vehicles present harsher conditions for power

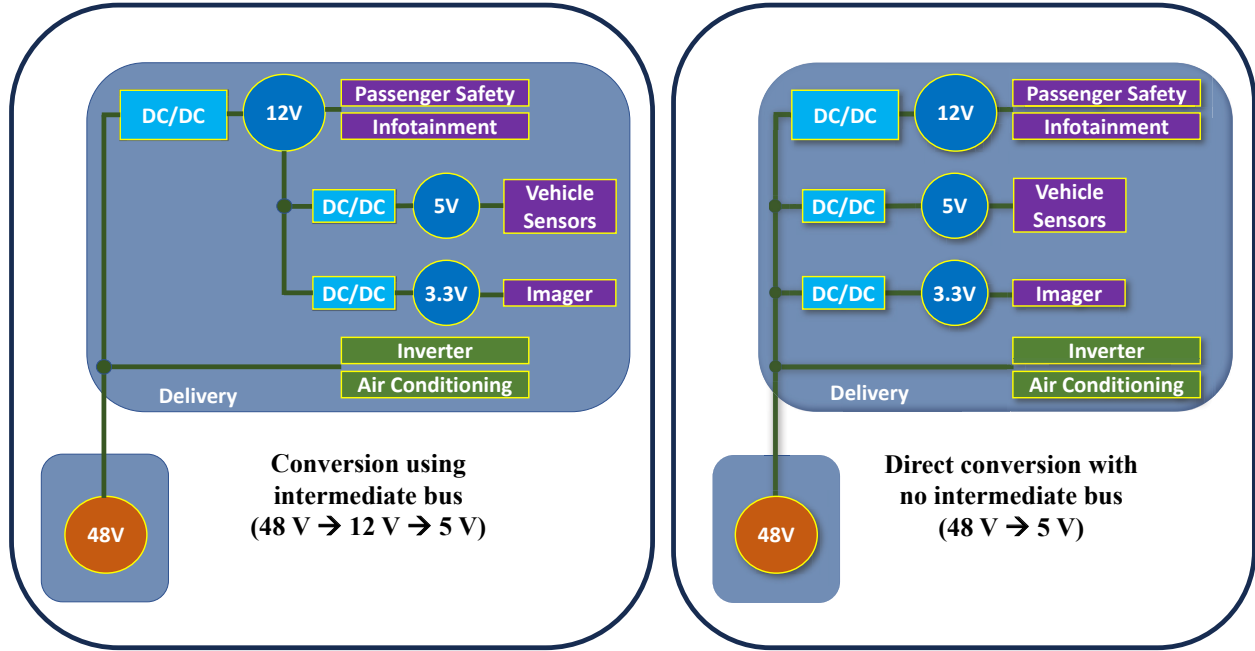


Figure 2.6: Comparison of 48 V power delivery architectures with and without an intermediate bus on-board a vehicle.

converters in the context of temperature, shock, and vibration, and components need to be chosen for both high performance as well as robustness and reliability.

A few more challenges pertaining specifically to hybrid SC converters themselves are listed and explained below. This thesis addresses each of these challenges using novel topologies, control techniques, and optimized converter design. Many of the techniques presented here are generalizable to power converters in other modes of transportation as well.

Electromagnetic Interference (EMI)

In transportation environments, power converters are surrounded by many other converters and in-vehicle electronics. Electromagnetic interference (EMI) refers to the unwanted conducted and radiated noise that arises within these dense, electronic systems [21]. Mitigating EMI within these systems becomes a challenge, and EMI is further exacerbated by fast voltage and current switching events in power converters. Hybrid SC converters, with their many switching devices, should be designed while keeping EMI in mind. In this thesis, the EMI for these converters is explored both at a design optimization level and at a more fundamental modeling level.

Dynamic Operation

Power converters do not always operate in steady-state, and they can suffer from line (input) and load disturbances. The converters need to operate dynamically during transient events and respond to these events as quickly as possible. In hybrid SC converters, it is important to model the full converter dynamics (including the flying capacitors) to understand how the converter dynamic response may differ for this class of converters compared to more conventional power converter topologies.

Isolation

EVs contain both high and low voltages on-board the vehicle. The need for both physical and electrical separation between the two voltage levels presents challenges in power converter size, form factor, and design. A portion of this thesis explores combining galvanic isolation with hybrid SC topologies and exploring the design optimization techniques and tradeoffs of this approach.

Output Voltage Regulation

Within transportation applications, fixed-ratio power converters may not be suitable for loads that require regulated voltages. Hybrid SC converters can be operated both in fixed-ratio and regulated regimes. This thesis discusses output voltage regulation techniques for hybrid SC converters and presents hardware demonstrations of regulated hybrid SC converters.

Chapter 3

An EMI-Compliant and Automotive-Rated 48 V to PoL Dickson-Based Hybrid Switched-Capacitor DC-DC Converter

Portions of this chapter are adapted in whole or in part from [22, 23]. Reference [22] provides more complete theoretical and design details on this work. The chapter in this dissertation provides additional, improved EMI results and analysis not captured in [22] that further corroborate the merits of the EMI mitigation techniques outlined in this chapter. This chapter also provides an extension to fundamental EMI modeling for hybrid SC converters. The major practical considerations explored in this chapter are EMI and output voltage regulation.

3.1 Introduction

Hybrid switched-capacitor (hybrid SC) converters can achieve high efficiencies and power densities due to their more effective utilization of passive components compared to conventional switched-inductor topologies [11, 24]. Particularly, high conversion ratio hybrid SC converters designed for data center power delivery have demonstrated stellar performance according to efficiency and power density metrics [25–27]. However, these converters are not yet commonly used in other high-energy-consumption industries, such as the automotive industry. Though these hybrid SC topologies boast high performance and passive component utilization, they often are constructed with a large number of switching elements, which can be a drawback when considering complexity. However, due to their multi-level structure, hybrid SC converters can have reduced switch blocking-voltages and lower dv/dt events at the switch nodes compared to conventional two-level topologies, resulting in reduced EMI.

This makes them strong candidates for use in automotive applications [28], where the EMI requirements are more stringent. Therefore, further investigation into hybrid SC converter performance within these environmental constraints is necessary.

Moreover, as the automotive market shifts towards more hybridized and fully electric vehicles (EVs), internal combustion engine (ICE) vehicles are also beginning to adopt 48 V batteries in place of the legacy 12 V battery for partial hybridization of the powertrain [29]. This allows ICE vehicles to align themselves with EVs where 48 V is emerging as a low-voltage dc bus for auxiliary electrical loads [30]. The use of a higher bus voltage decreases transmission conduction losses as power demands increase and allows for lighter-weight cabling systems to be employed within the vehicle. The higher power subsystems may be powered from a 48 V bus directly, while the lower-voltage subsystems may be driven using high-density point-of-load (PoL) converters [31–35]. Following similar trends to data-center power delivery [25–27, 36–38], automotive power delivery can eliminate a voltage conversion step by completely removing the intermediary 12 V bus. An example EV power architecture based on a 48 V distribution bus is shown in Fig. 3.1.

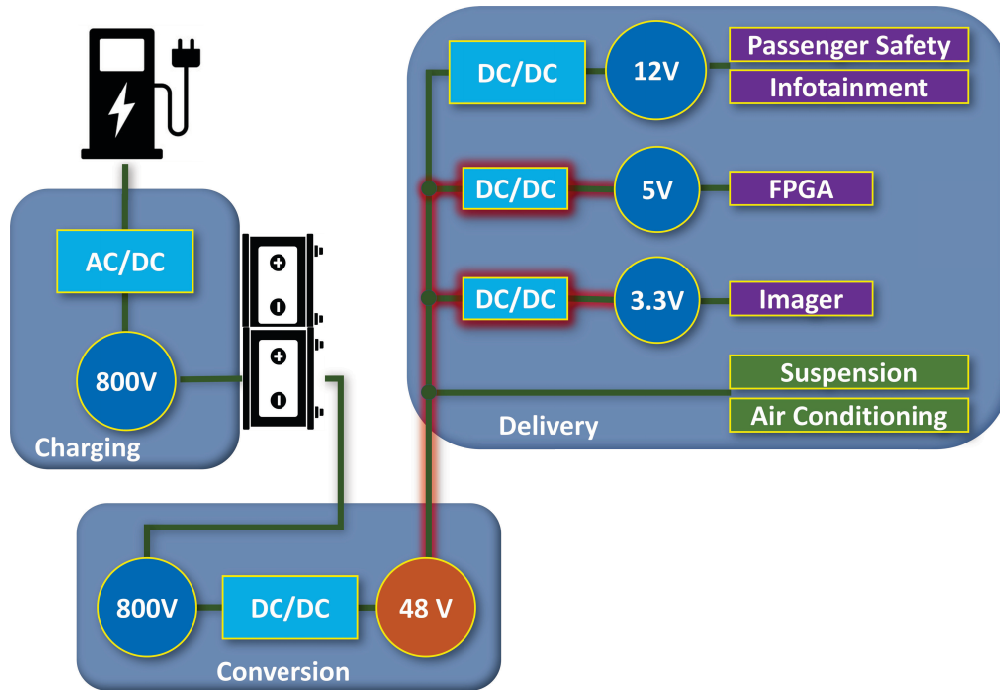


Figure 3.1: Diagram of an electric vehicle power delivery architecture, highlighting potential use-cases of the power converter presented here.

The similarity in power delivery architecture indicates an opportunity to apply the advanced power converter designs used in data center applications to automotive power solutions, with some additional design considerations. First, in the automotive powertrain,

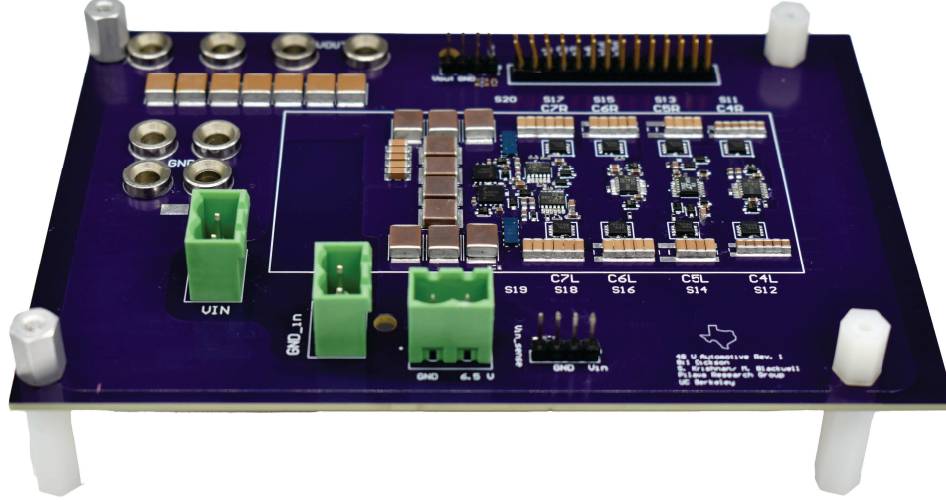


Figure 3.2: Photograph of an EMI-compliant 48 V to 5 V HISID converter.

the 48 V nominal bus voltage can vary above and below the nominal 48 V [39], which the power converter must regulate to the desired output voltage. Second, the power converters themselves must meet industry EMI requirements so that they do not interfere with any other electrical subsystems in the vehicle.

Current industry solutions for 48 V high-step-down power conversion from companies like EPC and MPS boast high efficiencies (upwards of 98%) [40,41]. However, similar automotive solutions qualified for standards such as the CISPR 25, Class 5 electromagnetic interference (EMI) may suffer in terms of efficiency ($\sim 94\%$) [42,43]. This points to a need for innovation. Moreover, industry reference designs from companies such as TI [43,44] and EPC [45] further motivate the need for high efficiency converter designs at the power level discussed in this chapter (100-300 W). Table 3.1 provides a listing of solutions that were found to be similar to this work at the time of publication. Many designs for this application do not publish power density in a consistent and easily comparable way, so power density is not included in the table.

This work investigates the hybrid interleaved-input, single-inductor Dickson (HISID) converter [48] (Fig. 3.2) for use in automotive power distribution systems as a regulating converter with an added custom front-end EMI filter. The hardware implementation demonstrates the ability of hybrid switched-capacitor converters to meet CISPR 25, Class 5 EMI standards [1], the most stringent class for on-vehicle applications. This work is the first demonstration of using a *combination* of several EMI mitigation techniques to develop an

Table 3.1: Survey of 48 V power converters.

Work	Voltage Conversion	Power* [W]	Peak Efficiency* [%]	Topology	Notes
[44]	48-to-5 V	150	94.0	2-phase Buck	Regulated, automotive
[42]	48-to-5 V	100	93.2	Buck	Regulated
[33]	48-to-3.3 V	10	93.0	Hybrid Dickson	IC, regulated
[40]	48-to-6 V	900	98.0	LLC	Fixed-Ratio
[46]	48-to-3.4 V	450	96.3	Hybrid Ladder	Fixed-ratio
[47]	48-to-6 V	420	98.6	CaSP	Fixed-ratio

* at noted conversion ratio.

automotive-rated solution which leverages the benefits of hybrid switched-capacitor topologies.

Combining previously investigated EMI mitigation techniques – Spread-Spectrum Frequency Modulation (SSFM) [48], and passive EMI filters [49] – with novel layout techniques, this work presents a high-performance, low-EMI power converter with an integrated passive front-end filter. The dependencies of each of these topics, particularly as they pertain to hybrid SC designs, are discussed in the following sections. While the techniques discussed are only analyzed and demonstrated on the HISID converter, they are applicable to many hybrid SC converters that have similar challenges such as having many switches and complex commutation loops. Converter efficiency is measured for this prototype at varying input and output voltages to demonstrate the converter’s regulation capability and to showcase operation at common voltage levels found in automotive systems. Furthermore, a detailed loss breakdown is also presented for the nominal operating condition with a discussion of the critical loss mechanisms for such hybrid SC converters, highlighting the printed circuit board (PCB) layout improvements over prior works [48, 49]. Finally, aggregate EMI data measured on the positive and negative terminals of the converter are presented in this work to demonstrate overall EMI compliance.

The remainder of this chapter is organized as follows: Section 3.2 details the converter topology and its theory of operation. Section 3.3 discusses EMI implications associated with this topology and possible mitigation techniques, most notably converter layout, passive filter design and SSFM. Finally, Section 3.4 includes specifications for the experimental prototype and EMI filter as well as measured efficiency and conducted EMI results.

3.2 Hybrid Interleaved-Input, Single-Inductor Dickson Converter

This work utilizes the HISID topology (Fig. 3.3) described in [48] to demonstrate an efficient, compact, and EMI-compliant dc-dc power conversion for a rugged automotive environment. Even without any additional EMI mitigation, this topology is attractive for automotive

applications as it features interleaved inputs, low switch blocking voltage stress, low- dv/dt switching transitions, and output regulation capability.

Topology Description

The proposed converter evaluated in this work [48,50], shown in schematic form in (Fig. 3.3), is a variation on the hybrid Dickson converter [51, 52]. This topology is named the hybrid interleaved-input, single-inductor Dickson (HISID) converter [48,49].

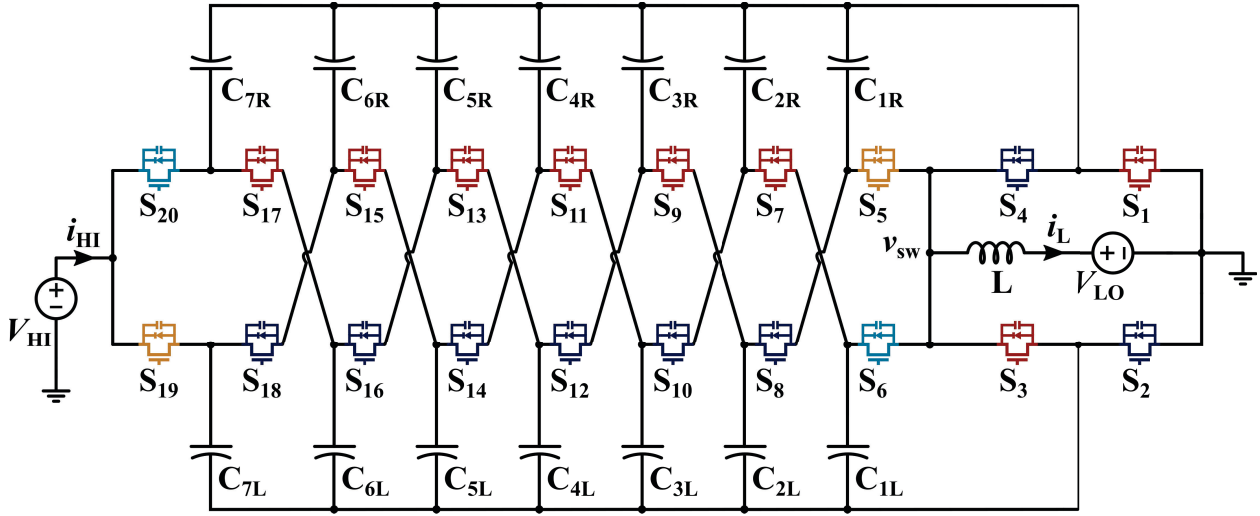


Figure 3.3: Schematic drawing of an 8-to-1 HISID converter with switches color-coded according to their control signals.

Fig. 3.4 describes how the HISID converter is derived from the single-ended hybrid Dickson converter using a 4-to-1 converter example. We begin with the single-ended hybrid Dickson converter and place two of them in parallel. The converters are then interleaved and operated 180° out of phase relative to each other. After doing this, we can see that both the low-side outputs have identical, inductively loaded full-bridges. Since they are both operating in the exact same manner, we can remove one of them (highlighted in red in Fig. 3.4) and merge the remainder of the two structures together. The resulting converter is the HISID converter. More information about the HISID derivation can be found in [22].

The HISID converter takes a similar approach to reducing current and voltage ripple at the input and output ports as the two-phase interleaved stacked-ladder in [53], thereby reducing filtering requirements at those ports. However, in this work, the base topology does not require the bulky capacitor column of [53] because it is inherently interleaved with a single inductor on the output instead of two tank-configured inductors as in the stacked-ladder topology. While the interleaved stacked-ladder in [53] requires $4N$ switches for an $N : 1$ conversion, the proposed topology only requires $2N + 4$ switches. Moreover, the HISID con-

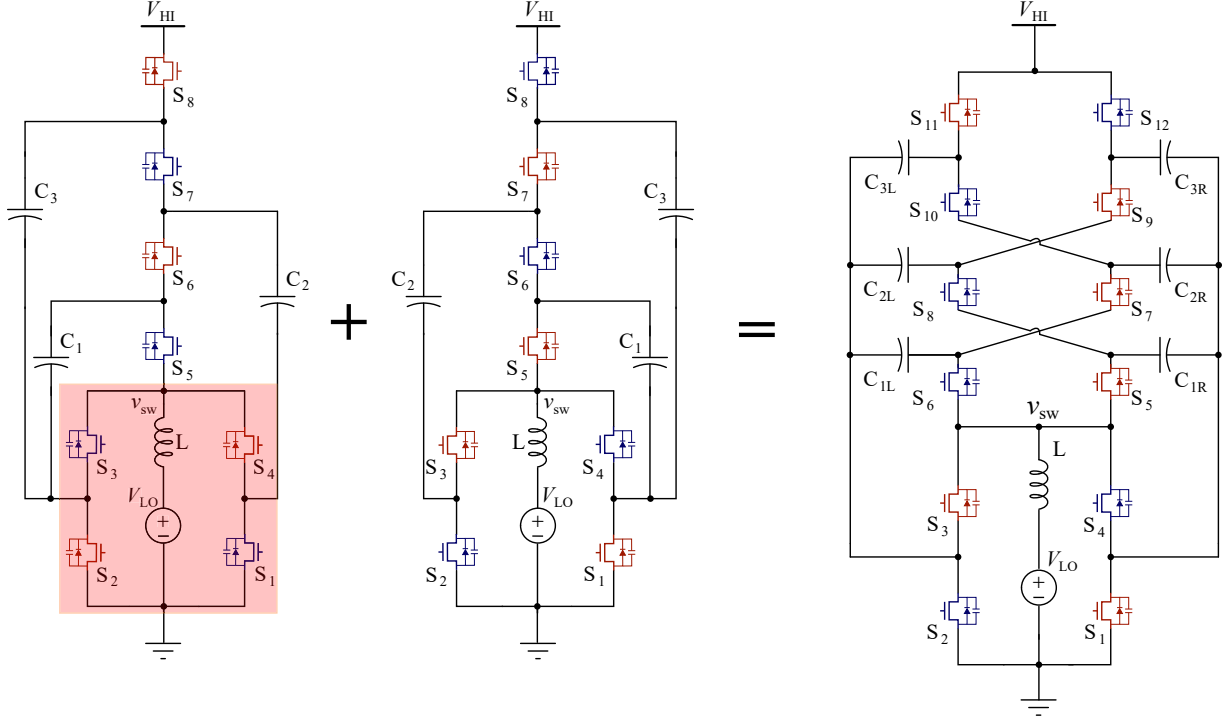


Figure 3.4: Dickson topology evolution from single-ended hybrid Dickson to HISID converter.

verter is capable of above-resonant operation and continuous forward conduction [10]. This allows for output voltage regulation without incurring increased circulating currents [54], albeit while sacrificing some zero-current switching (ZCS)/ zero-voltage switching (ZVS) capability.

The HISID converter topology is also intrinsically advantageous for achieving EMI compliance. In the proposed converter, the interleaved nature of the input allows charge to flow from the high-side source during portions of *both* switching phases (Fig. 3.5), rather than just one phase as is typical with many two-phase converters. Because of this characteristic, the rms value of the input current is reduced compared to the non-interleaved single-inductor Dickson topology [48], thereby reducing the necessary input capacitance. The size of the total input low-pass EMI filter can be reduced due to the HISID input effectively seeing twice the switching frequency of the converter. Simultaneously, the HISID input switches conduct half of the input rms current compared to the input switches in its non-interleaved counterpart. Therefore, the required input filter capacitance and inductance are theoretically smaller and have lower required current ratings. This is helpful for achieving high power density of the total power conversion system and helps simplify any input filter design.

As described in [11, 24, 55], the family of Dickson-style converters demonstrate minimal total switch stress, making them attractive options for high-efficiency and low-cost applications. Furthermore, the inductor at the low-side port of the converter not only allows for

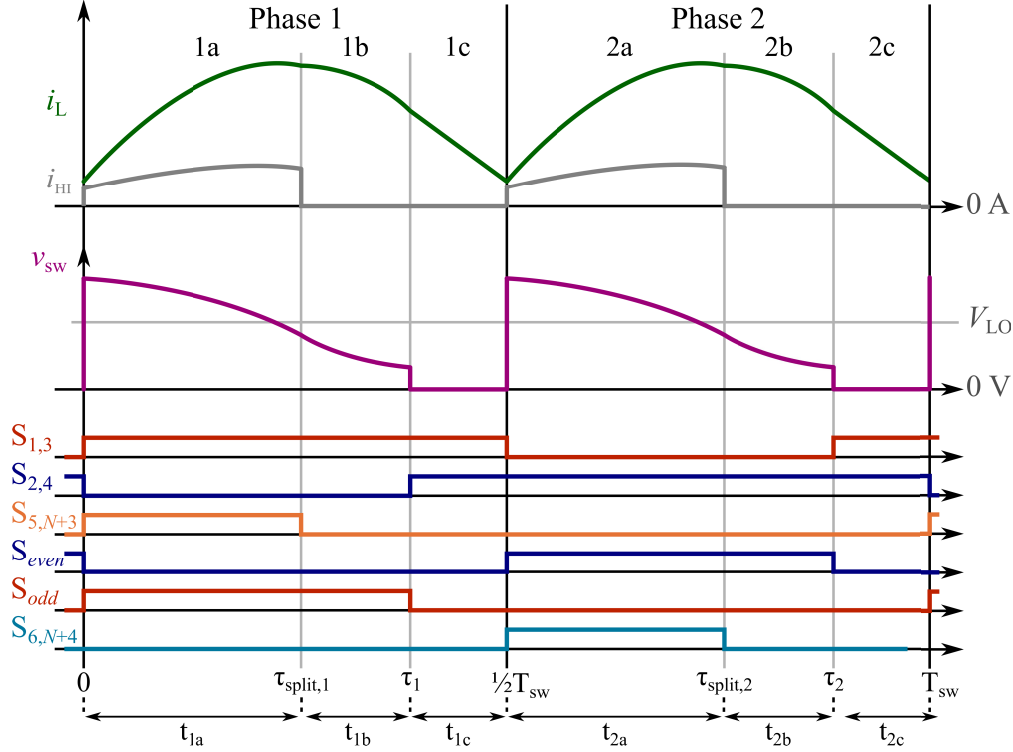


Figure 3.5: Switching scheme and converter waveforms for output voltage regulation of the interleaved-input hybrid Dickson converter operating at a switching frequency faster than resonance.

resonant and above-resonant operation, but serves as an output EMI filter, and facilitates soft-charging of the flying capacitors [7, 56]. While there are many facets of this topology that make it attractive for both EMI and automotive applications, it does require additional control complexity to maintain soft-charging of the flying capacitors. Soft-charging is typically achieved via split-phase operation [56], which introduces two additional sub-phases within the main switching phases.

Circuit Operation

Example gating signals and corresponding converter operation waveforms for an 8:1 ($N = 8$) HISID converter are shown in Fig. 3.5, with equivalent circuits for each phase (and sub-phase) shown in Fig. 3.6. The converter operates with a 50% duty cycle for Phases 1 and 2. This implementation imposes a voltage ripple at the switch node and a current through the inductor which has a frequency twice that of the switching frequency. Assuming two-phase operation, all odd-numbered switches (“bridge” switches S_1, S_3 and “string” switches $S_5 - S_{19}$) are ON during Phase 1 and all even-numbered switches (“bridge” switches S_2, S_4 and “string” switches $S_6 - S_{20}$) are ON during Phase 2. Due to the interleaved symmetry

of the topology, sizing the flying capacitors such that $C_{iL} = C_{iR}$ for $i \in \{1, N - 1\}$, results in an identical effective capacitance presented to the switch-node v_{sw} during both Phase 1 (Fig. 3.6a) and Phase 2 (Fig. 3.6d). Because the single inductor at the output is engaged with an identical capacitor network during both phases, Phase 1 and Phase 2 exhibit equivalent operation, thereby simplifying the analysis of this topology.

Operating in this manner, however, will result in hard-charging of the flying capacitors. In order to maintain soft-charging, the converter must be operated with split-phase operation. Detailed in [56], split-phase operation describes the introduction of sub-phases within the two main switching phases to ensure soft-charging of the flying capacitors through the output inductor. Without these additional switching states, large current spikes occur at phase transitions due to mismatched KVL loop voltages. These hard-charging events have a negative impact on efficiency due to capacitor charge-sharing losses, and on EMI performance from increased voltage and current spikes. Furthermore, without soft-charging operation, capacitor voltage ripple may need to be reduced to improve efficiency and EMI performance, decreasing passive utilization.

For a step-down HISID converter the following split-phase switching scheme is implemented to satisfy all voltage loops at phase transitions, thereby ensuring capacitor soft-charging: Sub-phases 1b (Fig. 3.6b) and 2b (Fig. 3.6e) are inserted between the transition from Phase 1a to 2a and from 2a to 1a, respectively. Since capacitors $\{C_{1R}, C_{7L}\}$ and $\{C_{1L}, C_{7R}\}$ are not series-connected to other capacitors during Phase 1a and Phase 2a, respectively, these capacitors accrue charge more quickly than the other flying capacitors (assuming all capacitors are equally sized). Switches S_5 and S_{19} (Phase 1b) and Switches S_6 and S_{20} (Phase 2b) are turned off to remove these capacitors $\{C_{1R}, C_{7L}\}$ and $\{C_{1L}, C_{7R}\}$ from the circuit once they have reached the necessary voltage for soft-charging at the transition to the following phase, where they are reconnected in a different configuration. Correct timing of the “b-phase” durations and placement within the primary Phases 1 and 2 are necessary to achieve full capacitor soft-charging [20, 56].

Moreover, selection of the desired switching frequency is non-trivial. The resonant frequency is related to the equivalent LC tanks formed at the switch-node during each phase and corresponds to zero current switching (ZCS) operation where the inductor current reaches 0 A at the end of each primary phase. The ratio of switching frequency to resonant frequency ($\Gamma = f_{sw}/f_{res}$) can then be tuned for best performance. Considerations are given to optimize the design for switching and conduction losses, as well as the EMI regulatory frequency range [1] and resultant EMI filter size. Each of these considerations informs the choice of switching frequency and resonant frequency, and thereby the inductor and capacitor values.

Trade-offs for different operating regimes of this Dickson-variant converter topology are explored in detail in [48], specifically with regard to how the choice of switching frequency impacts efficiency and EMI performance. An advantage of above-resonant operation is the ability to operate in continuous conduction mode (CCM) and regulate the output voltage to a value lower than V_{HI}/N , typically a requirement for PoL converters. Additionally, operation of hybrid SC converters above resonance provides tolerance to component mismatch, which enables the use of high energy density, Class II ceramic flying capacitors [36, 57, 58].

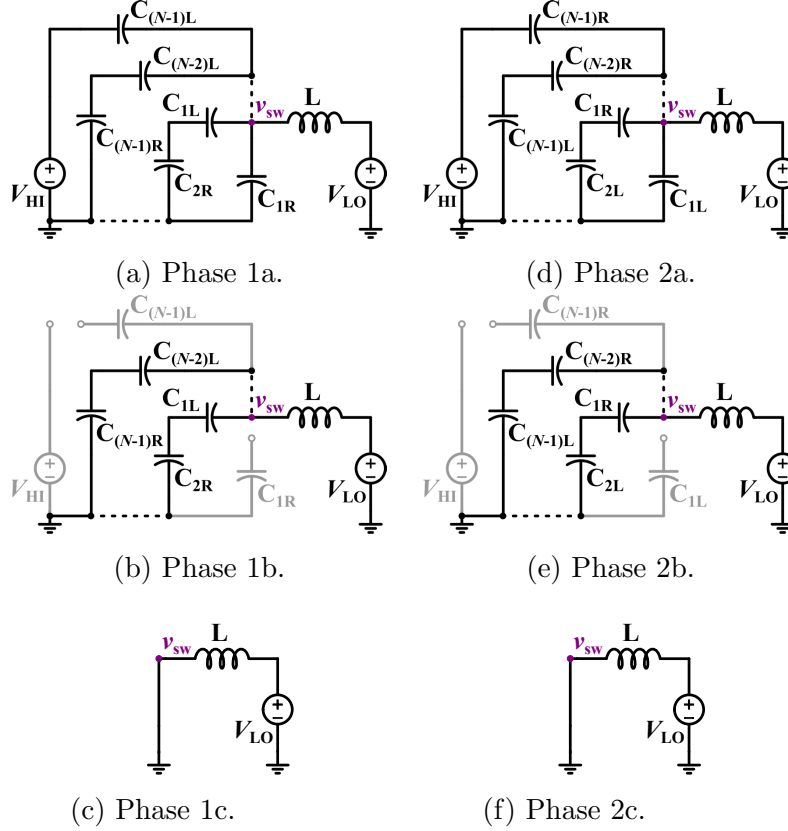


Figure 3.6: Equivalent circuits for each sub-phase of a regulating $N = 8 : 1$ Dickson converter, with split-phase switching and regulating sequence as ordered a-f: Phase 1a $\rightarrow$ Phase 1b $\rightarrow$ Phase 1c $\rightarrow$ Phase 2a $\rightarrow$ Phase 2b $\rightarrow$ Phase 2c.

Interleaved converters such as the HISID converter can have reduced input rms currents. However, due to the requirement for split-phase switching, input switches S_{19} and S_{20} turn off towards the end of primary Phases 1 and 2, respectively, and the input source is disconnected. Even though the input current is not fully continuous throughout each period, there is still significant improvement over a single-ended topology where the input current would be zero for 50% of the switching period.

Output Voltage Regulation

The topology demonstrated in this work achieves a fixed-conversion ratio when operated with 50% duty cycle. However, due to the output configuration of the inductor, L , and bridge switches, $S_1 - S_4$, this Dickson-variant converter can also be viewed as a fixed ratio switched-capacitor network merged with a buck converter at the output. Switches $S_1 - S_4$ can be controlled to regulate the output voltage to any value lower than the fixed-conversion-

ratio output. This work focuses on validating the converter for operation with a regulated 5 V output or a regulated 3.3 V output. These voltage levels were chosen as the 5 V and 3.3 V bus are important low voltage rails in an automotive subsystem, powering downstream loads such as processors, sensors, and in-vehicle networks (see Fig. 3.1).

To regulate the output voltage, a regulation sub-phase (Phase 1c and 2c in Fig. 3.5) is inserted within each main switching phase, wherein the output inductor is connected between the output and ground [58, 59]. Phase 1 consists of Phase 1a (Fig. 3.6a), its corresponding split-phase, Phase 1b (Fig. 3.6b), and its regulating sub-phase, Phase 1c (Fig. 3.6c). Similarly, Phase 2 consists of Phase 2a (Fig. 3.6d), Phase 2b (Fig. 3.6e), and Phase 2c (Fig. 3.6f). During the regulating intervals, switches $S_5 - S_{20}$ are off and the current through inductor L freewheels via the four bridge switches, $S_1 - S_4$. The duration of each regulation sub-phase is set according to the desired output voltage and the relationship between the switching frequency and resonant frequency. The switching frequency and resonant frequency are often selected to optimize efficiency and power density. However, in automotive applications, these frequencies can also play a large role in determining EMI performance and compliance with regulatory standards.

3.3 EMI Mitigation Techniques

Automotive power converters are generally placed in close proximity to other in-vehicle electronics, many of which are susceptible to EMI. Thus, the high di/dt and dv/dt associated with the power converter switching transitions must be mitigated [60, 61]. These switching transitions are made steeper by the implementation of high-speed, wide-bandgap power transistors such as GaN devices. In automotive systems, the allowable EMI noise levels are standardized in CISPR 25, under Class 5 limit requirements [1]. The EMI spectrum is measured over the frequency range of 150 kHz to 108 MHz and there are peak, quasi-peak, and average noise limits set within this range. A summary of the specifications for this

Table 3.2: Conducted Noise Limits for CISPR 25, Class 5 EMI Standards [1]

Band	Frequency (MHz)	Limit (dB μ V)	
		Peak	Average
LW	0.15-0.3	70	50
MW	0.53-1.8	54	34
SW	5.9-6.2	53	33
FM	76-108	38	18
TV	41-88	34	24
CB	26-28	44	24
VHF I	30-54	44	24
VHF II	68-87	38	18

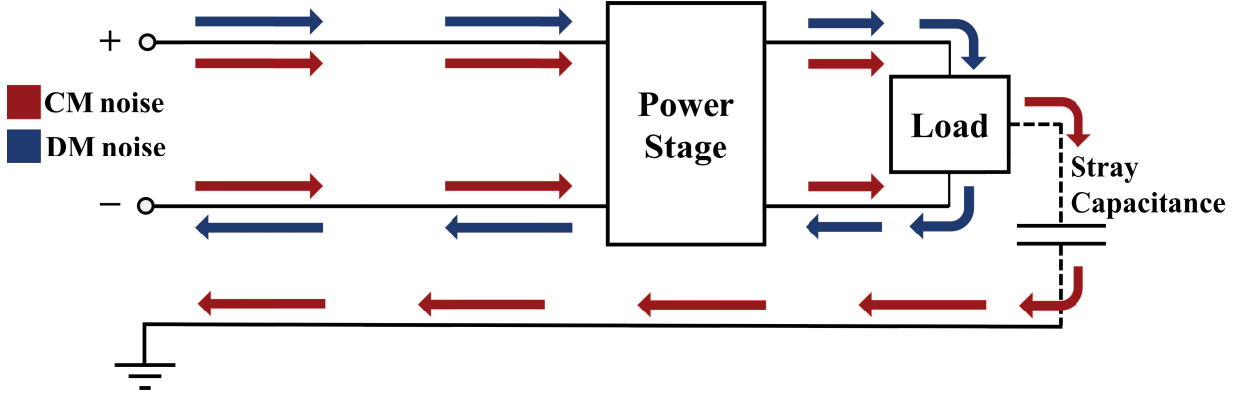


Figure 3.7: Common Mode and Differential Mode noise paths through the system.

standard is presented in Table 3.2. Full compliance testing requires peak, quasi-peak, and average detectors, but, both the quasi-peak and average measured results cannot exceed the peak levels [62]. In this work, peak EMI data is reported to quantify “worst case” noise levels for the converter, and average data is reported to demonstrate the positive impact of the SSFM technique on noise levels.

While both conducted and radiated emissions are regulated, this work focuses on reducing the conducted emissions of the converter. We measure the EMI at the 48 V input bus because this bus voltage should be stiff and free of excess injected noise. The conducted emissions are measured in a pre-compliance setup, which provides a good indication of overall EMI performance. Radiated emissions measurements are more intricate, involving the use of a large, fully-shielded anechoic chamber, and are also highly dependent on cable routing and mounting orientation [63]. For an initial demonstration of emissions performance of this hybrid SC converter, only conducted emissions are analyzed.

Noise from conducted emissions can be broken down into two different types: common mode (CM) and differential mode (DM), shown in Fig. 3.7. CM noise increases with increasing parasitic capacitance in the power stage and larger and/or faster switched-voltage transitions [64–66]. On the other hand, DM noise is increased by increasing load current which exacerbates the impact of parasitics in larger current loops throughout the power stage [66].

While the HISID converter has many inherent merits for both CM and DM noise mitigation as described in Section 3.2, it contains complex circuit connections and, therefore, more loops (both current loops and commutation loops) of varying size than standard power converter topologies. Additionally, topologies which require split-phase switching have larger rms input currents than non-split phase converters, due to the input voltage being disconnected from the circuit within at least one sub-phase. This leads to slightly greater DM noise. Despite this increase in rms currents, clever circuit configuration (e.g. the implementation of an interleaved-input in this work) serves to reduce this source of DM noise as compared

to a single-ended topology.

There are several ways to reduce EMI in switching power converters. EMI mitigation often starts with power converter layout practices such as strategic component placement, loop area minimization, and effective grounding and shielding techniques [67–71]. EMI filters are also commonly added to the input side of a power stage and are tuned to mitigate noise peaks within the EMI measurement range. While EMI can be reduced with changes to the converter hardware, switching frequency control techniques such as spread spectrum frequency modulation (SSFM) can also be used [72]. Different SSFM schemes and their specific impacts on converter EMI in this hybrid SC topology are explored in more detail in [48]. In this work, each of these techniques is utilized to balance converter efficiency, size, and EMI compliance.

Layout Considerations – Commutation and Conduction Loop Design

Optimizing both commutation and conduction loops within power converter layout is beneficial for converter EMI and efficiency performance metrics. Figs. 3.8 and 3.9 are simplified diagrams that show a few different loops within this HISID converter layout. They serve as examples for the discussion of layout impacts on both losses and noise levels.

Prior work has shown that EMI performance can be improved by minimizing commutation loop parasitic inductance [73, 74]. Typically, power converter topologies which comprise half-bridge modules (e.g., buck [73, 75], flying capacitor multi-level (FCML) [76], and series-capacitor buck [59] converters) have relatively simple commutation loops that are straightforward to minimize in layout. However, for many hybrid SC topologies, which have not only more switches but also more complex circuit connections, optimization of commutation loops becomes more difficult.

In a hybrid SC converter, *each* switch of Phase 1 forms a commutation loop with *each* switch of Phase 2. Topologies such as the Dickson converter have many commutation loops overall, and many loops per switch. For example, the 8-to-1 HISID converter has $(\frac{N_s}{2})^2 = 10 \times 10 = 100$ commutation loops for $N_s = 20$ number of switches. It is most effective to layout the switch network to create a single small commutation loop per switch, rather than attempting to minimize multiple loops per switch. Generally, there is a trade-off between power-stage size, PCB loss, and commutation loop size in layout design. For the HISID converter, minimizing commutation loops reduces PCB loss as well as switching noise and switching loss.

The comparison between two different PCB layouts of the HISID converter is depicted in Fig. 3.8 for two specific commutation loops. ANSYS SiWave was used to analyze commutation loops and power path resistances, which are discussed in more detail in [22]. Because the focus of this work is a high performance, low EMI power converter, reducing both noise and losses is imperative. Commutation loop areas are shrunk to decrease ringing (noise generation). At the same time, power paths are shortened to decrease resistive losses. These

two goals may potentially be conflicting, however, in the proposed layout, both of these can be achieved.

The layout configuration for the HISID converter in this work is depicted in the bottom row of Fig. 3.8. In this configuration, the converter is folded vertically which is more advantageous than the lateral fold (top row of Fig. 3.8) implemented in [49] due to the significantly smaller commutation loops. This can be seen from the comparison between Figs. 3.8a and 3.8c and Figs. 3.8b and 3.8d showing the reduced loop areas and consequent reduced commutation loop inductance.

Furthermore, for this cross-connected HISID converter, configuring the commutation loops in this way also reduces the PCB trace resistance associated with many conduction loops. As an example, Fig. 3.9 shows the PCB trace resistance of the power path through C_{3R} during Phase 2 (consisting of $V_{HI} \rightarrow S_{12} \rightarrow C_{3R} \rightarrow S_4 \rightarrow L \rightarrow V_{LO} \rightarrow \text{ground} \rightarrow V_{HI}$) for two different layout configurations¹. The trace resistance of this loop is significantly reduced with this ‘vertical-fold’ layout (Fig. 3.9b) due to the placement of switch S_{12} (top-side) above switch S_4 (bottom-side) rather than the power path through these switches traversing the full-length of the power-stage (Fig. 3.9a). The PCB trace resistance for this conduction path is reduced by 72% compared to the layout in Fig. 3.9a. A lower DC resistance is beneficial for decreasing conduction losses and allowing for higher power throughput without needing more complex thermal solutions.

¹As a note, the ground return path is shown only on Layer 6 to simplify the illustration of each loop. However, in practice, parallel ground planes should also be placed on inner layers for improved shielding and reduced trace resistance.

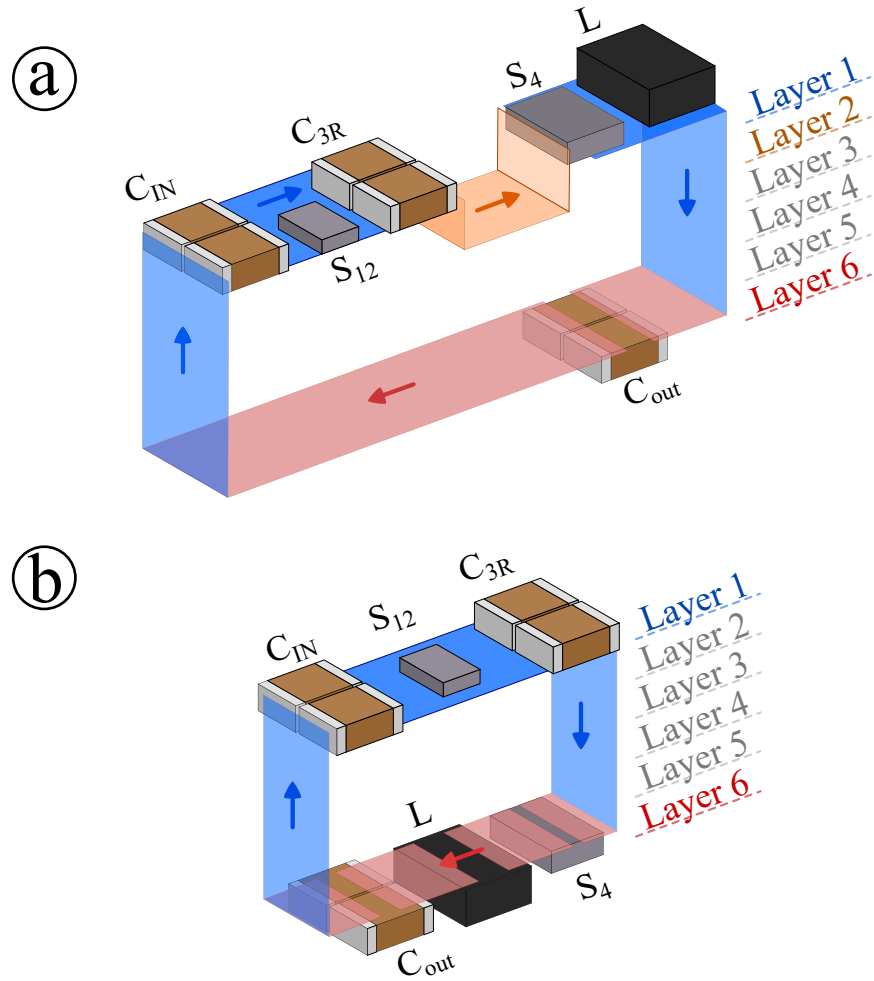
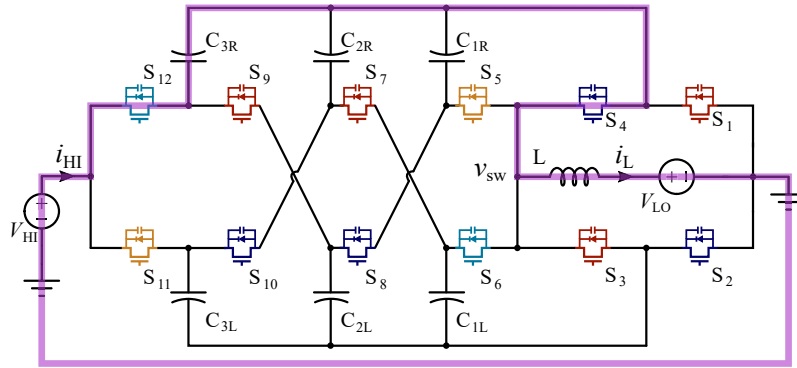


Figure 3.9: Conduction loop comparison of (a) lateral and (b) vertical layouts.

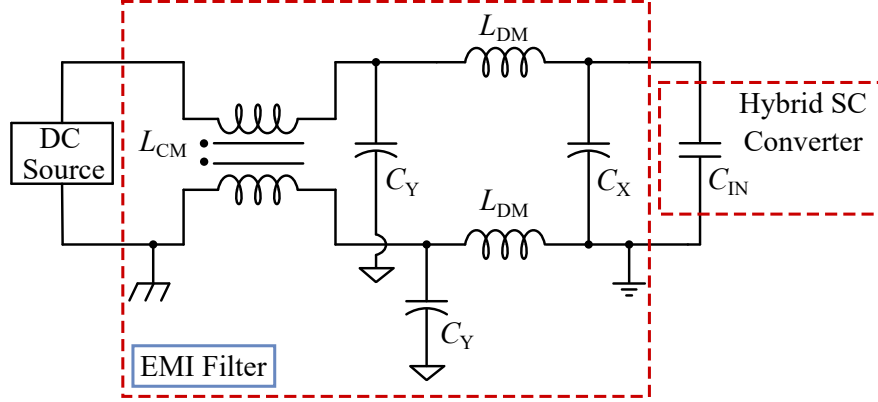


Figure 3.10: Schematic of the front-end EMI filter.

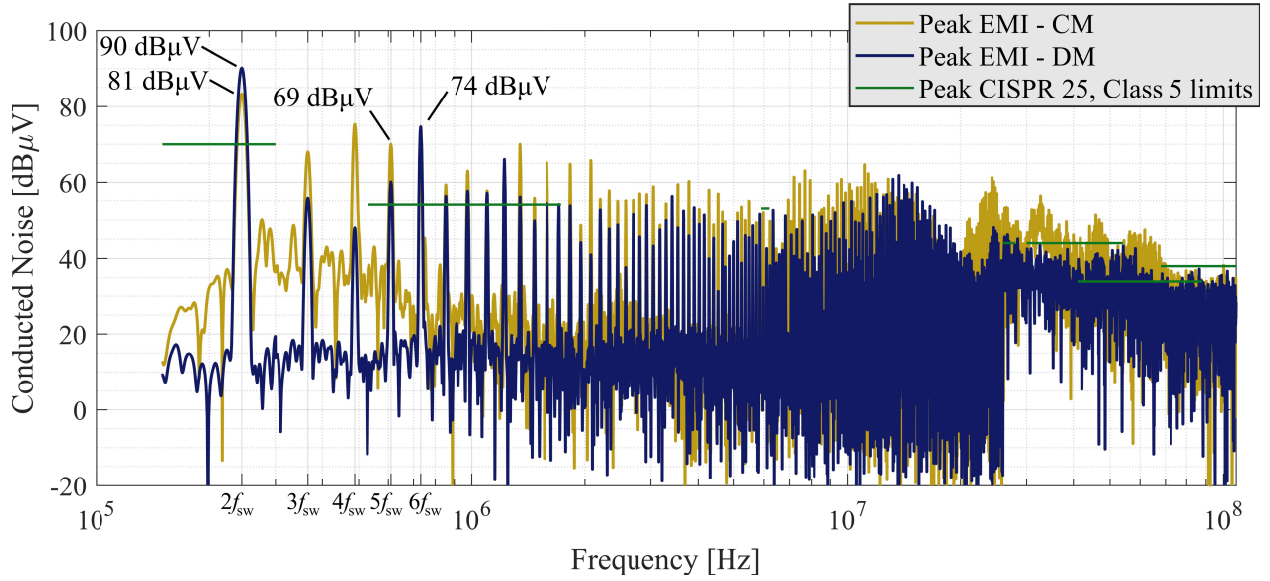


Figure 3.11: Peak CM and DM conducted emissions with no EMI mitigation techniques, measured on positive terminal of converter.

While good layout is important in ensuring good EMI performance, passive filters are also commonly used for mitigating converter EMI. This work examines the power stage design process for reducing emissions from the converter on the 48 V bus. Therefore, only the EMI at the input side of the converter is characterized. The input-side EMI filter circuit designed for this hardware prototype is depicted in Fig. 3.10. The filter components are sized based on preliminary conducted EMI measurements of the converter that determine at which specific frequencies the noise peaks occur. For this two-phase Dickson converter, peaks correspond

to the frequency of the switched input current frequency, which is twice that of the switching frequency, due to the interleaved input. The highest noise peaks within the CISPR frequency range — which the filter targets — occur at the second switching harmonics for both CM and DM noise. The initial CM and DM measurements shown in Fig. 3.11 inform the EMI filter design discussed here. The EMI filter stages² are designed such that the CM filter has a corner frequency of 80 kHz and 19 dB attenuation at 244 kHz and the DM filter has a corner frequency at 55 kHz and 26 dB attenuation at 244 kHz.

Because EMI filters add to overall passive component volume and loss, spread-spectrum, or “dithering”, frequency techniques can be used to reduce conducted EMI that is generated by fixed-frequency switching schemes [77]. If used in conjunction with a passive filter, frequency dithering can decrease the required attenuation for the filter, potentially reducing the size and losses of the filter. Spread-spectrum frequency modulation (SSFM) [72, 78–80] is a control technique that modulates, or dithers, the converter’s periodic switching frequency, consequently spreading out the original energy of each harmonic about a specified frequency band. In [48], four popular periodic modulation schemes – right-triangular, triangular, trapezoidal, sinusoidal – were analyzed with respect to how they affect the HISID converter’s conducted EMI. Based on this analysis, a triangular SSFM scheme is implemented here with the results presented in Section 3.4.

Moreover, the switching frequency and SSFM scheme for this prototype are carefully chosen keeping efficiency and EMI tradeoffs in mind. The EMI benefits from SSFM may not outweigh the negative impacts on efficiency when operating near resonance, but may be significant for above-resonant operation of the converter [48]. As the switching frequency becomes greater than the resonant frequency, the effective output resistance, R_{eff} , approaches its limit, R_{esr} , which is the effective series resistance of the power components, and represents the lowest possible output resistance [58] (as dictated by ohmic losses in realistic components). Consequently, operating with a center frequency sufficiently above resonance (at least 70% higher) and with a relatively small dithering band, the losses for the converter remain relatively constant across the SSFM frequency range.

3.4 Experimental Prototype and Results

An 8-to-1 discrete hardware prototype was constructed to verify operation of the proposed HISID converter (Fig. 3.12) as well as to explore the effectiveness of the different EMI mitigation techniques. The experimental prototype, measuring 84 mm × 41 mm × 8 mm, utilizes mixed switch technologies (both Si and GaN) to optimize for on-state resistance ($R_{\text{DS(on)}}$), drain-to-source voltage (V_{DS}), and gate charge (Q_{G}). Both Cascaded Bootstrap and Gate-Driven Charge Pump methods [81] are used for bootstrapping in the gate drive power circuit. As discussed in [81], these methods improve upon original bootstrapping techniques. They are used in tandem in this prototype to efficiently power the large number of switches in this topology and to optimize for power density. Furthermore, all components (Table 3.5)

²A detailed design process for this EMI filter can be found in [22].

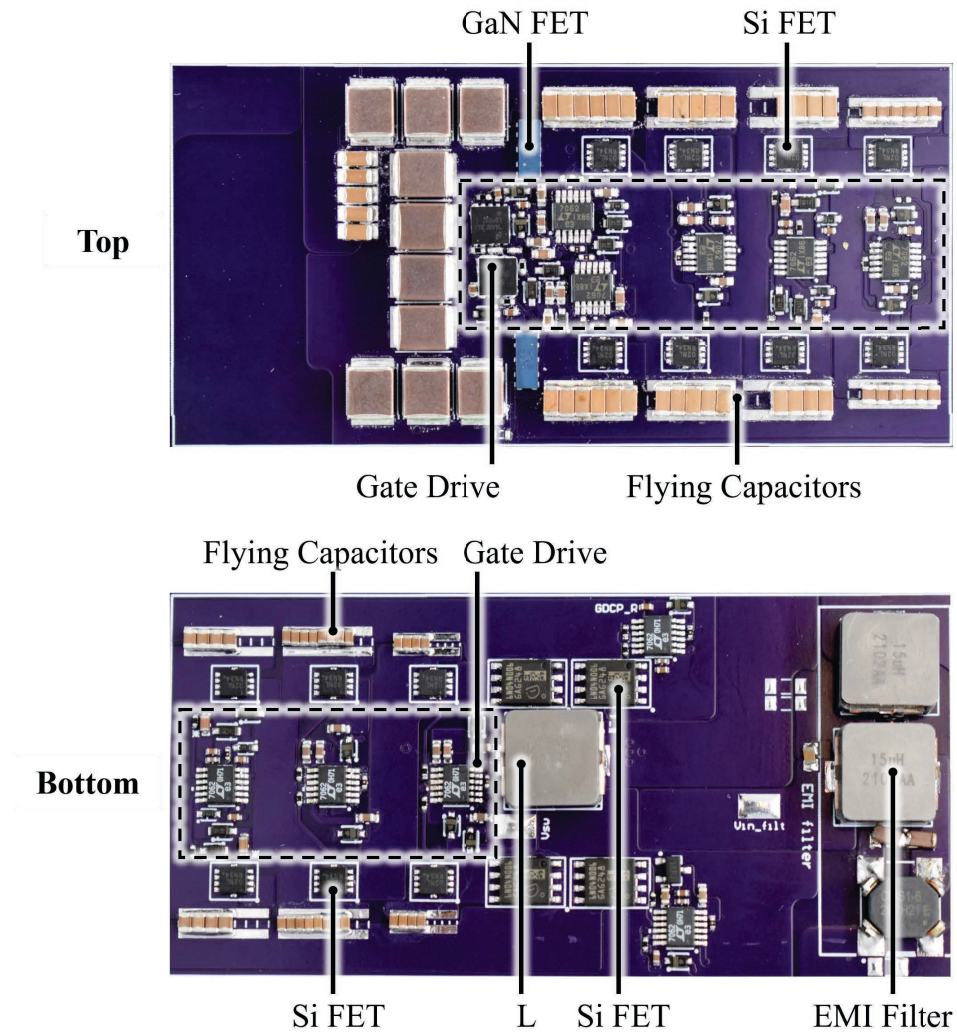


Figure 3.12: Annotated photographs of prototype board with key components labeled.

on the board are automotive-qualified so as to adhere to the Automotive Electronics Council (AEC) standards. Inductor and capacitor values were chosen to give a resonant switching frequency of 43 kHz, with the second and third harmonic falling below the lowest relevant EMI frequency band to alleviate passive filter requirements when operating above resonance.

Table 3.3: Converter Operating Parameters

Parameter	Value	Units
V_{IN}	48	V
V_{OUT}	5	V
$P_{OUT,max}$	150	W
f_{sw}	122	kHz
f_{res}	43	kHz
L	0.56	μ H
C_{in}^*	60	μ F
C_{fly}^*	6	μ F

* Voltage-de-rated values.

Table 3.4: Complete gate driver component listing.

Component	Value
GaN Gate Drive	
Gate Driver	Texas Instruments LM5113QDPRRQ1
Gate Drive Voltage	5 V
Gate Resistance	47 Ω
PWM RC Filter: Resistance	3.3 k Ω
PWM RC Filter: Capacitance	2.2 pF
Si Gate Drive	
Gate Driver	Analog Devices Inc. LTC7062IMSE
Gate Drive Voltage	6.5 V
Gate Resistance	1 Ω

Table 3.3 defines the operating parameters for this prototype. The selection for the maximum power level of 150 W is chosen to align with the application to 5 V subsystems within the automotive powertrain. Table 3.4 provides additional details for the gate drive circuitry, including the gate resistance and filter values used. Due to the faster switching transitions enabled by GaN transistors, a larger gate resistance is used for the GaN devices compared to the gate resistance used for the Si FETs. This helps prevent high dv/dt transitions that could negatively impact EMI performance.

Converter Operation

Both inductor current, i_L , and switch-node voltage, v_{sw} , waveforms are shown in Fig. 3.13 for above-resonant fixed-ratio and regulating operation of the hardware prototype at the

Table 3.5: Component Listing of the Hardware Prototype

Component	Mfr. & Part Number	Parameters
Dickson Power Stage		
Start-up Switches $S_{19} - S_{20}$	EPC EPC2206	GaN, 80 V, 2.5 mΩ
String Switches $S_5 - S_{18}$	ON Semiconductor NVTFS002-N04CL	Si, 40 V, 3.5 mΩ
Bridge Switches $S_1 - S_4$	Infineon IAUC100-N04S6L014	Si, 40 V, 1.4 mΩ
Flying Capacitors C_{1x}, C_{2x}	Murata GRT188R61H225ME13D	X5R, 50 V, 2.2 μ F (x4, x8)
C_{3x}, C_{4x}	TDK CGA4J3X5R1H475K125AB	X5R, 50 V, 4.7 μ F (x4, x6)
C_{5x}, C_{6x}, C_{7x}	TDK CGA5L3X5R1H685K160AB	X5R, 50 V, 6.8 μ F (x4, x5, x7)
Inductor L	Vishay Dale IHLP4040DZERR56M01	0.56 μ H, 49 A I_{sat}
Gate Drive		
GaN Driver	Texas Instruments LM5113QDPPRRQ1	90 V, high and low-side
LDO	Microchip MCP1792T-5002H	5.0 V, 100 mA
Si Gate Driver (and Charge Pump)	Analog Devices Inc. LTC7062IMSE	Dual high-side driver
Bootstrap Diodes	Nexperia PMEG6002EJ,115	Schottky, 60 V, 200 mA
Charge Pump Diodes	Diodes Inc. PD3S230L-7	Schottky, 30 V, 2 A
Charge Pump Capacitors	Murata GRT188R61H225ME13D	X5R, 50 V, 2.2 μ F
EMI Filter		
CM Choke, L_{CM}	Eaton CMS1-6-R	32.8 μ H, 3.1 A I_{sat}
CM “Y” Capacitance, C_Y	TDK CGA4J3X7S2A105K125AB	X7S, 100 V, 1 μ F
DM Inductors, L_{DM}	Vishay Dale IHLP4040DZER150M8A	15 μ H, 7.7 A I_{sat}
DM “X” Capacitance, C_X	TDK CGA4F3X7S2A224K085AE	X7S, 100 V, 0.22 μ F
Controller Board		
FPGA	Terasic Inc. P0466	DE10-Lite, Max10 FPGA

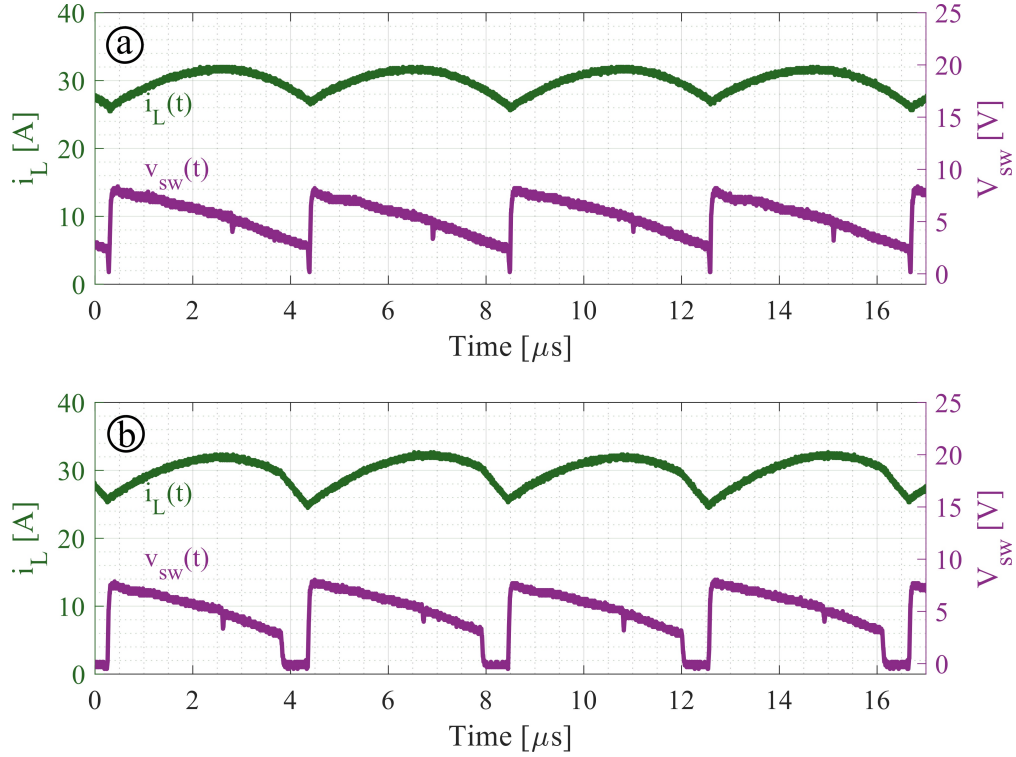


Figure 3.13: (a) Above resonant, and (b) regulating inductor current, i_L , and switch-node voltage, v_{sw} , measured waveforms for the 8-to-1 discrete hardware prototype at 30 A load current.

conditions listed in Table 3.3. As discussed above in Section 3.2, operating the hybrid SC converter above resonance enables reduced rms currents compared to resonant operation. This is beneficial when the converter is pushed to higher load currents, where conduction loss dominates [48]. However, output voltage regulation implemented as discussed in Section 3.2 exhibits higher rms currents compared to operation at a fixed-conversion ratio, incurring greater conduction losses in the switches and magnetics. Furthermore, switches $S_1 - S_4$ conduct for longer durations (depicted in Fig. 3.5), again resulting in increased losses. Higher di/dt transitions in the regulating case also contribute to higher core loss in the inductor [59].

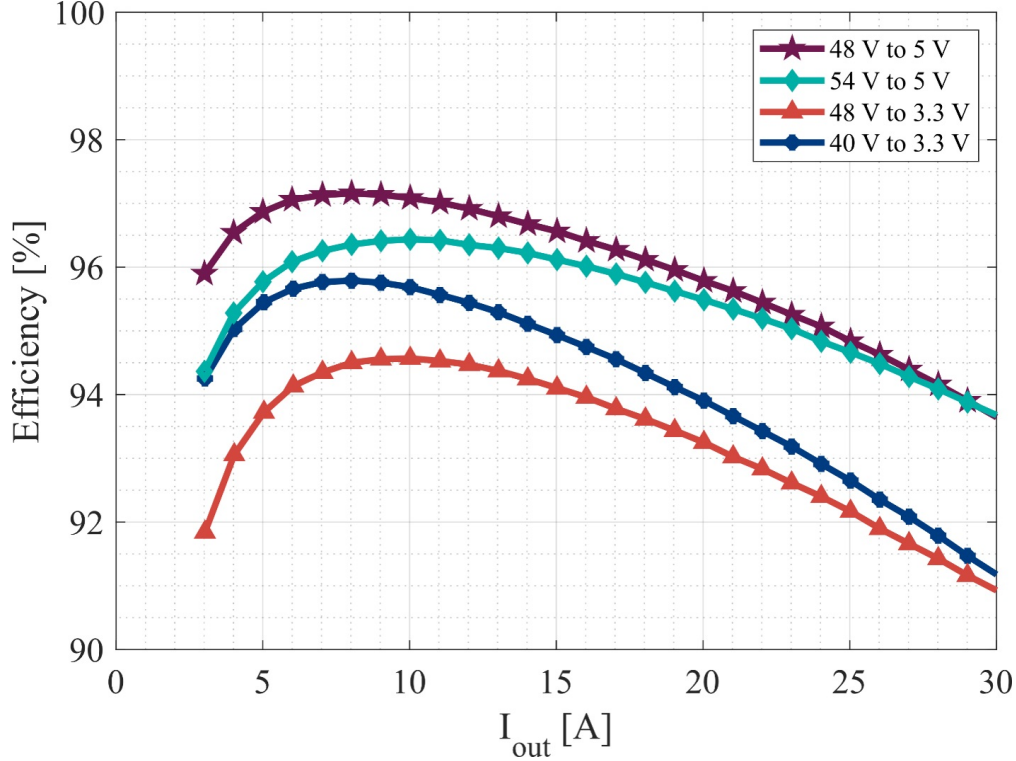


Figure 3.14: Measured efficiency of 8-to-1 hardware prototype at 40-54 V input and both regulated 5 V and 3.3 V outputs, switching at 122 kHz ($2.8\times$ higher than resonance).

Converter Efficiency and Loss Breakdown

Fig. 3.14 shows efficiency versus load curves measured for a regulated 5 V output with varied input voltage when the converter is operated at a nominal switching frequency of ~ 122 kHz ($\Gamma = 2.8$) with no SSFM employed. The work in [48] demonstrated that employing SSFM at frequencies much higher than resonance does not affect the efficiency significantly, regardless of the spread-spectrum modulation scheme.

The peak efficiency of the full solution including the EMI filter (but not gate-drive power) at a 48 V nominal input voltage is 97.1%. To demonstrate the converter's ability to regulate to other voltage rails present in an automotive system, efficiency measurements are also reported for the conversion from 48 V to 3.3 V. Finally, the 48 V rail in a vehicle may vary about the nominal 48 V value if the 48 V source is a battery [39]. Therefore, converter efficiency data is also reported with input voltages of 40 V and 54 V. Each of these cases has peak efficiencies greater than 94% and a full load efficiency of above 90%.

An approximate loss breakdown for full-load operation at 48 V-to-5 V conversion is shown in Fig. 3.15. Examining the source of loss within the circuit can inform not only component selection and choice of switching frequency, but also the PCB layout as discussed above. For the 48 V-to-5 V regulating converter HISID prototype, the inductor and switch conduction

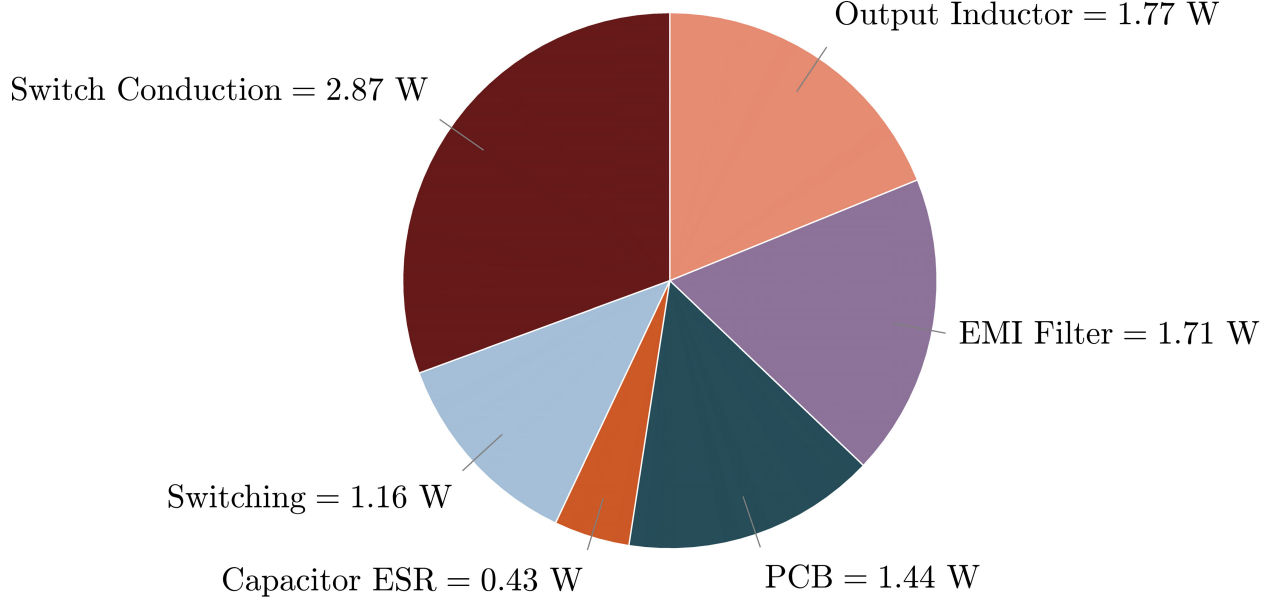


Figure 3.15: Power loss breakdown for full-load (150 W) regulating (48 V to 5 V) operation of the HISID hardware prototype.

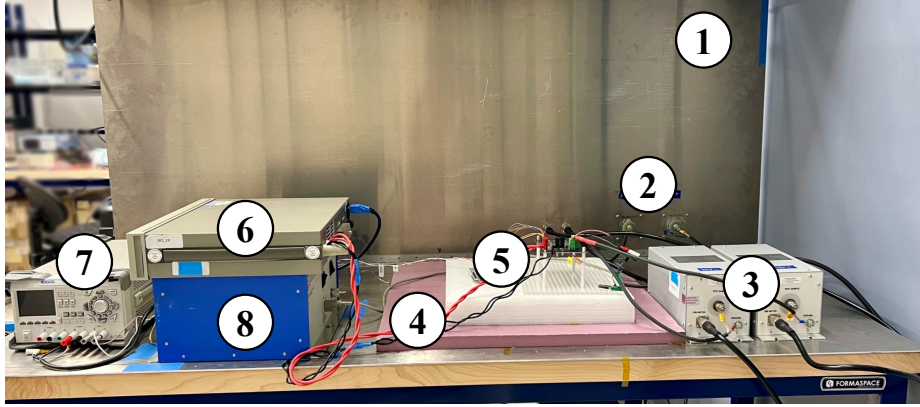
losses dominate the losses at full-load. Furthermore, the PCB losses only contribute to 14% of the total loss, a 2.5 times reduction over the prototype presented in [49], due to improved layout techniques. The EMI filter contributes to about 16% of the overall loss, further justifying the need to use multiple EMI mitigation techniques, such as SSFM, to optimize filter design.

Implementation of EMI Mitigation Techniques

For the prototype shown in Fig. 3.12, the input-side EMI filter accounts for 7.5% of the overall converter volume. Preliminary (i.e., with no EMI mitigation employed) aggregate EMI noise levels for the regulating converter operating at $2.8\times$ the resonant switching frequency are shown in Fig. 3.17a.

Aggregate EMI must be measured on both the positive and return terminals for CISPR 25 compliance because, as is shown in this section, the noise levels on each terminal may not be the same. These noise measurements were taken in a laboratory pre-compliance, semi-shielded environment using the Tektronix RSA306b Real-time RF Spectrum Analyzer. The laboratory EMI setup is shown in Fig. 3.16, with key equipment labeled. The spectrum analyzer, input supply, and feed-through capacitances are located behind the vertical ground plane to reduce any potential noise contributions.

The EMI filter stages on the hardware prototype are designed as follows: the CM filter has a corner frequency of 80 kHz and the DM filter has a cutoff frequency at 55 kHz. A



- ① Reference ground plane
- ② Feed-through capacitance (10 μ F)
- ③ HV Line Impedance Stabilization Networks (21702-5-TS-50-N)
- ④ Dielectric foam
- ⑤ 8-to-1 Dickson prototype
- ⑥ Electronic load
- ⑦ Gate drive power supply
- ⑧ LV Line Impedance Stabilization Network (21106-50-BP-25-BNC)

Figure 3.16: Laboratory setup for conducted EMI measurements with key equipment labeled.

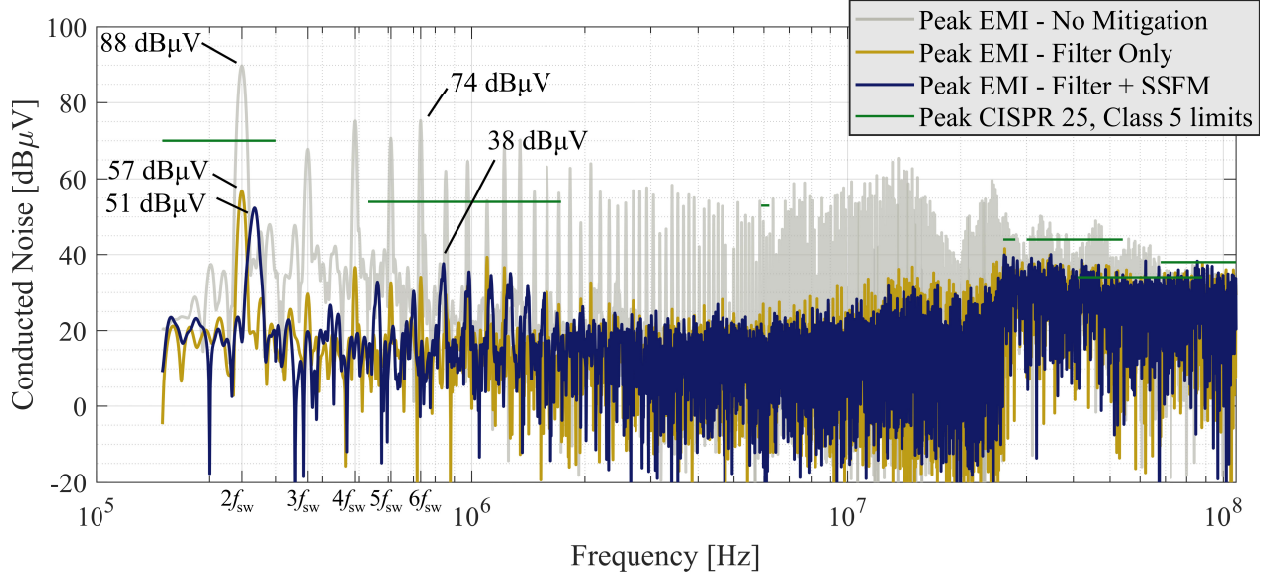
triangular SSFM scheme with a dithering step size of ± 420 Hz with a maximum deviation of ± 2.5 kHz from the center frequency at a modulation frequency of 780 Hz is employed. Fig. 3.17 shows the peak conducted emissions measured on both the positive and negative terminals of the converter and shows how the emissions are affected by using each EMI mitigation technique, incrementally. The impact of SSFM on reducing the EMI filter size is discussed in [49], Here, by utilizing *both* SSFM and a passive filter, the noise peaks are reduced significantly. Looking at the peak conducted emissions in Fig. 3.17, the highest noise peak at $2f_{sw}$ is reduced by more than 15 dB while still maintaining a relatively small passive filter (about 7.5% of total converter volume).

Moreover, with SSFM, the fundamental switching frequency is also changing with the modulation scheme, so the noise peaks occur at different harmonics along the EMI measurement range at the time of the measurement. In this case, an average EMI measurement is useful to showcase the true impact of SSFM (Fig. 3.18b). Average detection takes the

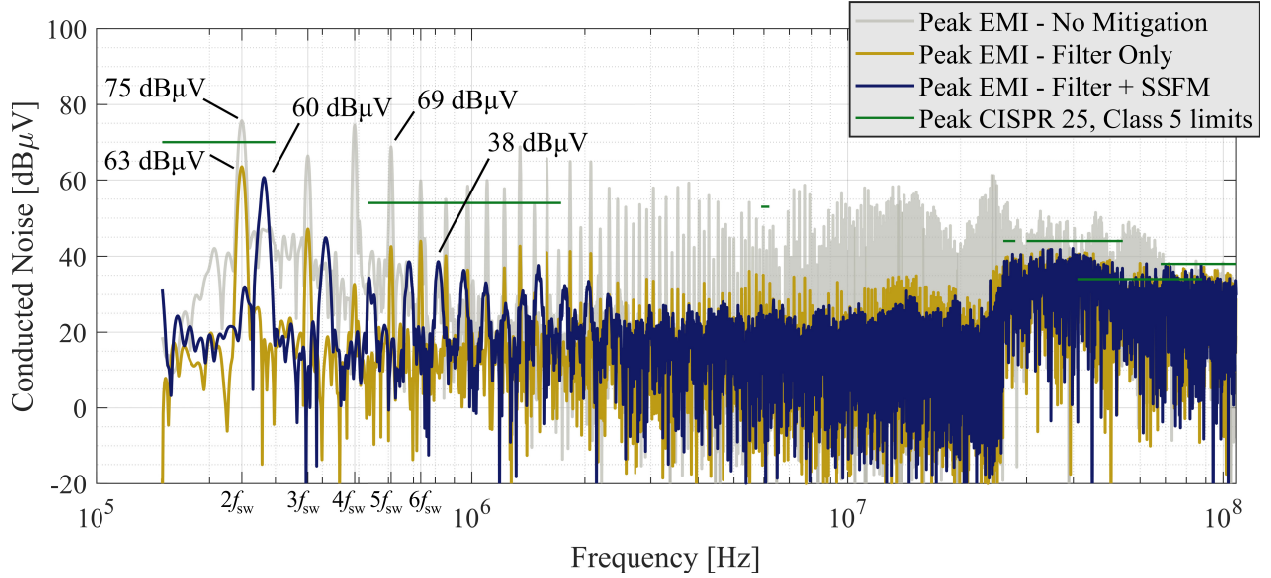
average amplitude of each noise signal across its period.

Fig. 3.18 shows the average conducted emissions measured on both the positive and negative terminals of the converter. It is seen that only implementing a front-end EMI filter is not sufficient for the converter to adhere to CISPR 25, Class 5 specifications for average emissions. Only when SSFM is implemented along with the filter, the noise peaks are lower and more spread out. This enables optimization of the EMI filter size, while maintaining adherence to the EMI standard. As a note, the high frequency noise between 26 MHz and 108 MHz does not come from the power stage itself. This noise is a measured phenomenon of the pre-compliant setup which contains both an electronic power supply and load, and which is not fully enclosed.

The 48 V converter presented in this work with passive EMI filter and SSFM passes CISPR 25, Class 5 limits. In a power converter solution, each of the aforementioned techniques – EMI filtering and SSFM – can be employed in lieu of or in conjunction with one another depending on the noise levels that must be mitigated. In applications where passive component volume is a primary concern, SSFM can be used as the primary EMI mitigation technique as showcased in [48].

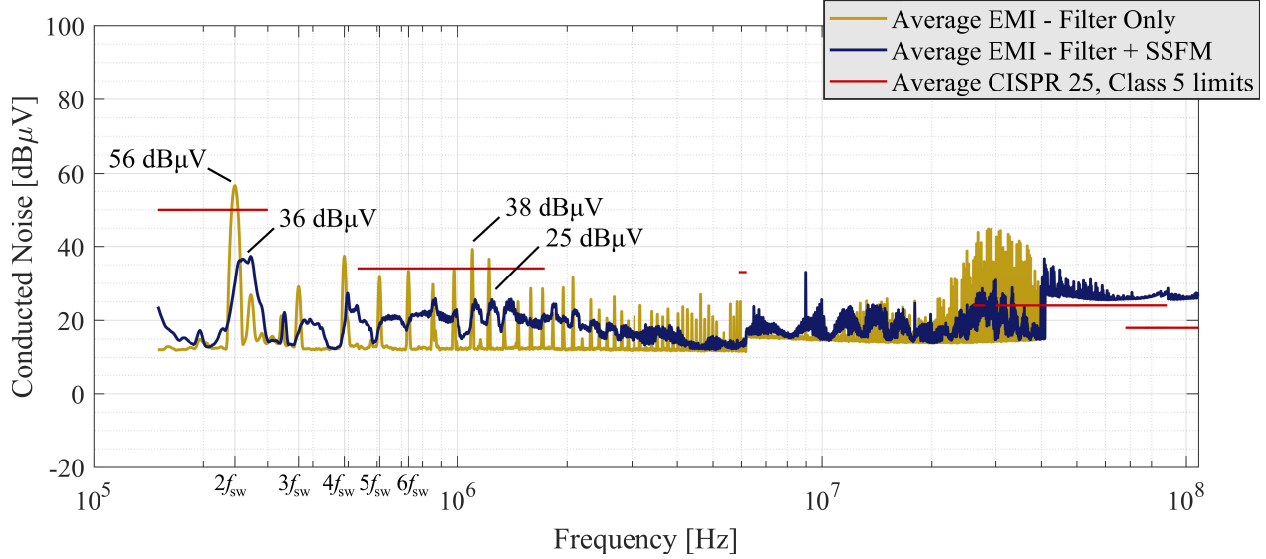


(a) Peak conducted emissions measured on positive terminal of converter.

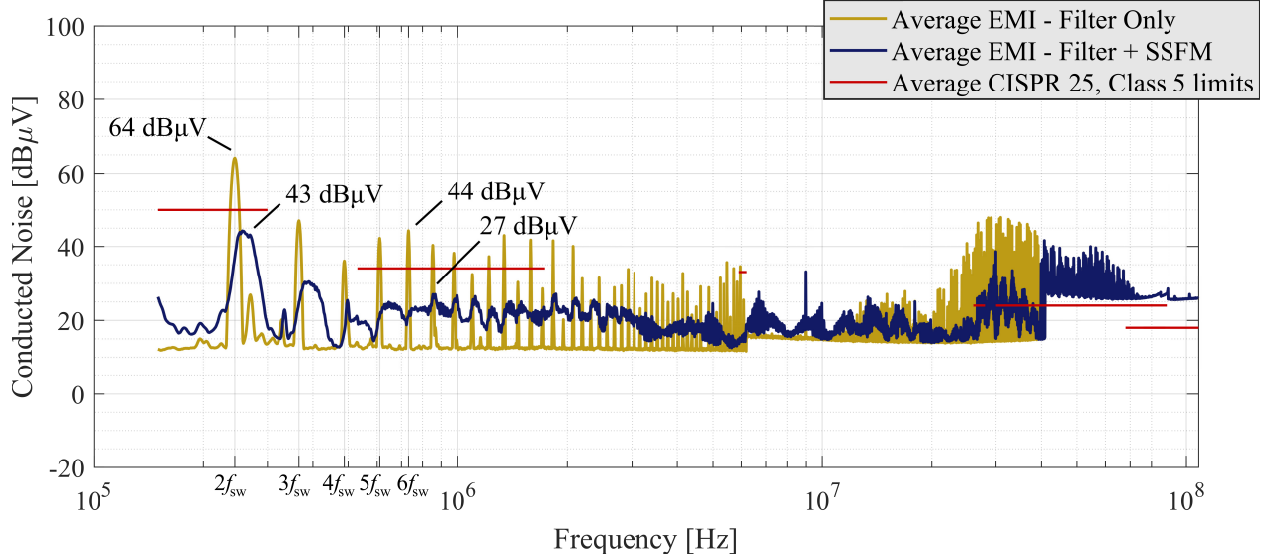


(b) Peak conducted emissions measured on negative terminal of converter.

Figure 3.17: Peak conducted emissions plots for above-resonant (~ 122 kHz) regulating operation with and without EMI mitigation operating at 48 V input and 5 V, 150 W output.



(a) Average conducted emissions measured on positive terminal of converter.



(b) Average conducted emissions measured on negative terminal of converter.

Figure 3.18: Average conducted emissions plots for above-resonant (~ 122 kHz) regulating operation with EMI mitigation (EMI filter, SSFM) operating at 48 V input and 5 V, 150 W output.

3.5 Conclusions and Future Work

The development of a 48 V distribution bus in both EVs and ICE vehicles opens opportunities for adapting advancements in high-efficiency, high-power-density data center power conversion techniques to automotive applications. However, in-vehicle power electronics also

require both robust component selection and qualification for industry EMI standards. This work discusses the construction of a 150 W automotive EMI pre-qualified regulating hybrid Dickson switched-capacitor converter for 48 V-to-5 V conversion. EMI mitigation techniques such as improved converter layout, a passive front-end EMI filter, and spread spectrum frequency modulation (SSFM) are discussed in detail and implemented on the hardware prototype. This work showcases the viability of combining conventional EMI mitigation strategies with a multi-switch, split-phase, hybrid, switched-capacitor converter. Finally, conducted EMI results showcasing the benefits of the input filter and SSFM implementation are reported demonstrating the interleaved-input hybrid Dickson converter passing CISPR 25, Class 5 EMI specifications at a peak efficiency of 97.1%.

This work has highlighted the possibility of using control methods such as SSFM on hybrid SC converters with their many switches and possibly more complex switching schemes. In addition, it demonstrates the potential to use hybrid SC topologies in more regulated industries such as automotive. In future work, it may be interesting to delve further into the sources of conducted EMI and consider why the converter EMI is dominated by either CM or DM EMI. Device selection and packaging (for example, Si vs. GaN) and layout within the design could provide useful insight here. Further quantifying the reduction in input EMI filter size compared to single-ended topologies would also be an interesting avenue of research. Finally, comparing the EMI signatures of the hybrid Dickson converter with that of a buck converter at the same operating conditions would provide insights into how each of these converters performs across a given EMI frequency range.

This chapter thus far has shown the capability of switched-capacitor-based topologies to meet industry EMI standards, despite their many switching elements. More fundamentally, the conducted EMI of these converters can be modeled at the switch level in order to predict the conducted EMI spectra of a given converter. The chapter section that follows presents an analytical model for predicting common-mode EMI in flying capacitor multilevel (FCML) converters that can be extended to other hybrid SC topologies, such as the hybrid Dickson converter. This work was conducted in collaboration with Francesca Giardine.

3.6 An Analytical Model for Common-Mode EMI in Flying Capacitor Multilevel Converters

This section is based on the results of a collaborative project with Francesca Giardine. For more detailed theory, hardware results and insights, please see “An Analytical Model for Common-Mode EMI in Flying Capacitor Multilevel Converters” published in the 2025 IEEE 26th Workshop on Control and Modeling for Power Electronics (COMPEL) [82].

The FCML converter is becoming increasingly popular for its high power density and high performance capabilities in many applications. However as presented before, capacitor-based topologies can have a large number of switching elements. Furthermore, the use of wide-bandgap technology such as GaN in FCML converters allows the devices to be operated at faster switching frequencies, and the generation of conducted EMI in these converters is of particular interest. The specific mechanisms by which FCML converters generate conducted common-mode (CM) EMI has been underexplored, and this work derives CM EMI scaling behavior for the FCML converter from first principles. The insights and lessons learned from this work can be extended to other hybrid SC topologies so that circuit designers have a fundamental understanding of the sources of hybrid SC converter EMI and how they scale.

Fig. 3.19 depicts an example 6-level FCML converter with parasitic capacitances drawn to chassis ground. Denoted $C_{p,ia}$ and $C_{p,ib}$ in Fig. 3.19 where $i \in [1, (N - 1)]$, these parasitic capacitances are generated by a grounded heatsink mounted on the field effect transistors (FETs).

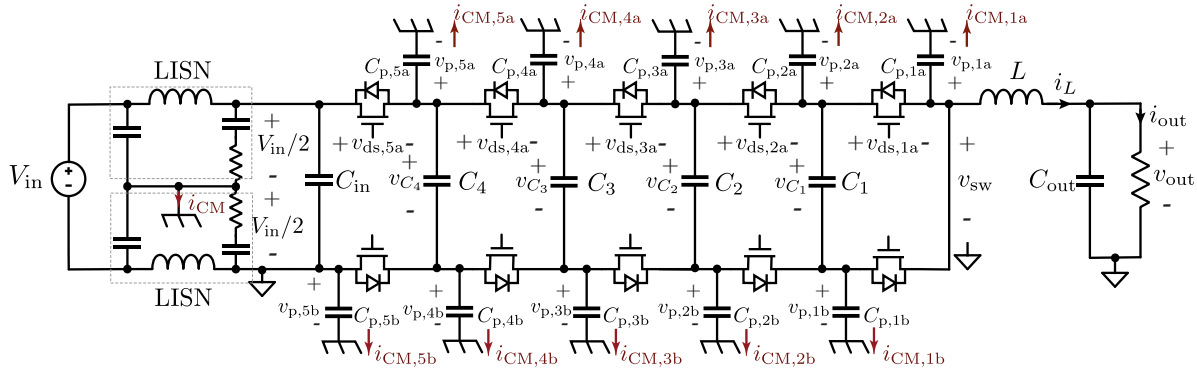


Figure 3.19: A 6-level FCML converter showing the generation of parasitic capacitances through a heat sink grounded to chassis. Figure made by Francesca Giardine.

Using this model of the FCML converter with parasitic capacitance included and considering how common-mode currents are generated in multilevel operation, we are able to construct an analytical harmonic decomposition of the Fourier coefficients of the continuous-time CM current for each harmonic ($a_{\text{CM},k}$) as a sum of all the common-mode current peaks. In the term $a_{\text{CM},k}$, $k \geq 1$ and is defined as the harmonic number. Eqn. 3.1 shows the final-form equation for determining the harmonic magnitudes and Table 3.6 lists the crucial parameters that allow us to derive this relationship. This Fourier transform represents the common-mode current in the frequency domain as a sequence of periodic rectangular pulses.

$$a_{\text{CM},k} = \sum_{i=1}^{(N-1)} -\frac{2 \cdot M_{f,i}}{k\pi} \sin(k\pi \frac{t_f}{T_{\text{sw}}}) e^{-j \frac{i-1}{N-1} 2\pi k} + \frac{2 \cdot M_{r,i}}{k\pi} \sin(k\pi \frac{t_r}{T_{\text{sw}}}) e^{-j(D + \frac{i-1}{N-1} + \frac{t_r}{2T_{\text{sw}}} - \frac{t_f}{2T_{\text{sw}}}) 2\pi k} \quad (3.1)$$

Table 3.6: Parameters for Calculating Harmonic Magnitudes ($a_{\text{CM},k}$) in an FCML Converter

Parameter	Symbol	Description
FCML level count	N	$N \geq 2$
Switch duty cycle	D	$0.1 \leq D \leq 0.9$
Switching period	T_{sw}	$T_{\text{sw}} = \frac{1}{f_{\text{sw}}}$
Rise and fall times	t_r and t_f	Design parameters
Harmonic number	k	$k \geq 1$
Sum of CM currents	i_{CM}	$i_{\text{CM}} = -\sum_{i=1}^{N-1} (i_{\text{CM},ia} + i_{\text{CM},ib})$
CM current peak magnitude (rise time)	$M_{r,i}$	$M_{r,i} = \frac{V_{\text{in}}}{t_r(N-1)} \cdot C_p(2i-1)$
CM current peak magnitude (fall time)	$M_{f,i}$	$M_{f,i} = \frac{V_{\text{in}}}{t_f(N-1)} \cdot C_p(2i-1)$

The model is validated in hardware using a 6-level FCML converter prototype that easily interfaces with a grounded heatsink. The prototype was also designed with considerations to minimize CM noise arising from the gate drive circuitry and careful layout was implemented

Figure 1 consists of a schematic diagram and two photographs. The schematic diagram on the left shows the electrical connections between various components. A coordinate system (x, y, z) is shown at the top left. The components and their connections are as follows:

- 1** Ground Planes: Two ground planes are shown, one for the HV DC Supply and one for the Spectrum Analyzer.
- 2** Through-capacitance to HV Supply: A capacitor connects the HV DC Supply ground plane to the Spectrum Analyzer ground plane.
- 3** LISNs: Two Line Impedance Stabilization Networks (LISNs) are connected between the HV DC Supply and the Spectrum Analyzer.
- 4** LISNs to Spectrum Analyzer + EMI Splitter: Two LISNs are connected between the Spectrum Analyzer and the EMI Splitter.
- 5** 6-Level FCML: The 6-level Full-Bridge Cascaded Multilevel (FCML) converter is shown with its internal components.
- 6** Electronic Load: An electronic load is connected to the output of the FCML.
- 7** LV Supply: A low-voltage supply is connected to the FCML.

The top photograph shows the physical setup of the FCML, with numbered callouts (1-7) corresponding to the schematic components. The bottom photograph shows the front and back views of the FCML PCB, with component labels S_{5b} , S_{4b} , S_{3b} , S_{2b} , S_{1b} , C_4 , C_3 , C_2 , C_1 , and L .

The FCML EMI in this section is measured on the input side of the converter. Figs. 3.21 and 3.22 show frequency-domain data for converter operation at two different duty cycles ($D = 0.1$ and $D = 0.8$) for both a 2 A load and a no-load condition. Strong matching between the modeled and measured peaks is observed and the model captures the global shape of the frequency content quite well in both plots.

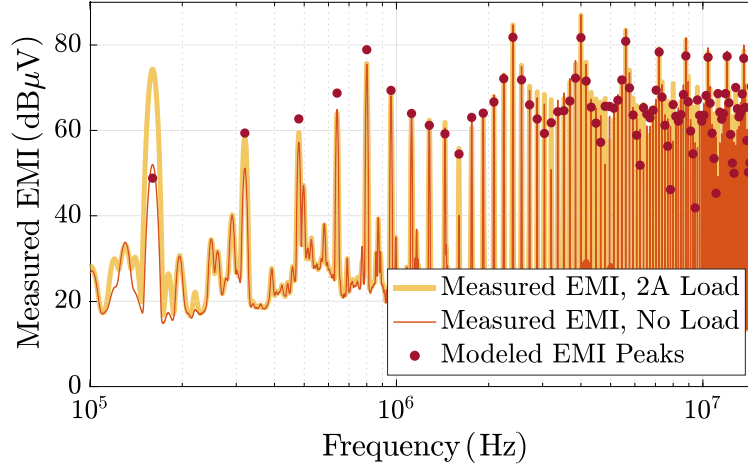


Figure 3.21: Frequency domain data for $D = 0.1$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks. Figure made by Francesca Giardine.

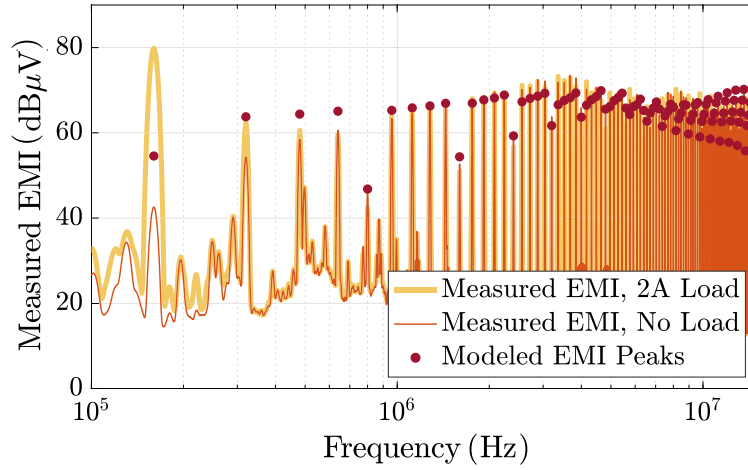


Figure 3.22: Frequency-domain data for $D = 0.8$ showing spectrum for a 2 A load and for the unloaded circuit, compared to modeled peaks. Figure made by Francesca Giardine.

The modeling approach in this section is able to capture the CM EMI behavior of the FCML power stage quite accurately. It verifies that modeling a parasitic capacitance per switch is the level of detail that is required to predict CM EMI behavior in the FCML power stage. This modeling technique can then be extended to other hybrid SC converters to derive their EMI scaling behavior in a similar way.

3.7 Chapter Summary

EMI remains a prevalent challenge in electrical systems and needs to be strategically characterized and mitigated. This chapter first discussed both the topological considerations and design optimization of a hybrid SC converter for 48 V automotive applications. The prototype is qualified for CISPR 25, Class 5 emissions in a pre-compliant EMI setup, showcasing the ability of hybrid SC converters to fit into vehicle power architectures. While this work is a step forward in qualifying novel hybrid SC topologies for use in transportation, there is more research to be done in characterizing the fundamental sources of EMI in these converters.

In an effort to understand how CM EMI arises in hybrid SC converters, an analytical model is developed for characterizing the CM EMI from first principles in an FCML converter. Key assumptions and details on the model were presented in this chapter and the model is validated on a pre-compliant EMI test bench with excellent matching between theory and hardware. Finally, the modeling techniques showcased here can be extended to other hybrid SC topologies to characterize their CM EMI so that power converter designers can ultimately be more informed about what level of EMI mitigation is required.

Chapter 4

Discrete-Time Dynamical Modeling of Hard-Charged and Soft-Charged Hybrid Dickson Converters

The major practical consideration explored in this chapter is dynamic operation.

The previous chapter demonstrated the combination of conventional EMI mitigation strategies with a hybrid Dickson SC converter to produce an EMI-pre-compliant prototype for use in automotive systems. However, this previous work was for the converter operating in steady-state. Practical transportation applications contain many dynamic loads and the power converters must respond to and recover from these transients successfully. This chapter focuses on modeling those dynamics for hybrid SC converters as well as their implications for hybrid SC controller design. The single-ended hybrid Dickson converter studied in this chapter is a building block of the HISID converter described in Chapter 3.

4.1 Introduction

Understanding the dynamic operation of hybrid SC converters is crucial to their implementation in transportation environments. Compared to pure SC converters, which have hard-charged flying capacitors, hybrid SC converters can be either fully or partially soft-charged. The hybrid Dickson converter is one hybrid SC converter topology that can achieve very efficient switch utilization and low normalized switch stress compared to other hybrid SC converters [24, 55]. The hybrid Dickson converter can be operated in all three of the regimes listed above: hard-charged, partially soft-charged, or fully soft-charged. However, in order to achieve complete soft-charging on the flying capacitors in steady-state operation, the converter requires the use of split-phase switching [83]. The split-phase control technique introduces two sub-phases in addition to the two main operating phases.

The schematic for the 4-to-1 hybrid Dickson converter used in this work is shown in Fig. 4.1 with key components labeled. Fig. 4.2 shows the gating signals for both split-

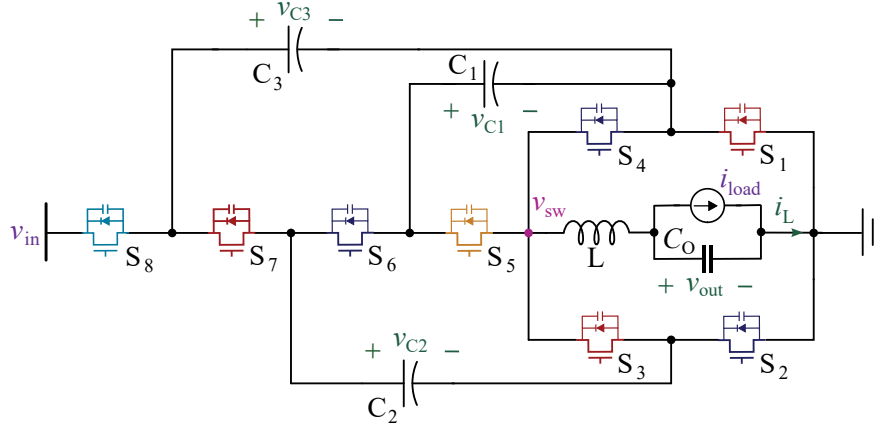


Figure 4.1: Schematic of the 4-to-1 hybrid Dickson converter with major components labeled and state variables shown in green and inputs shown in purple.

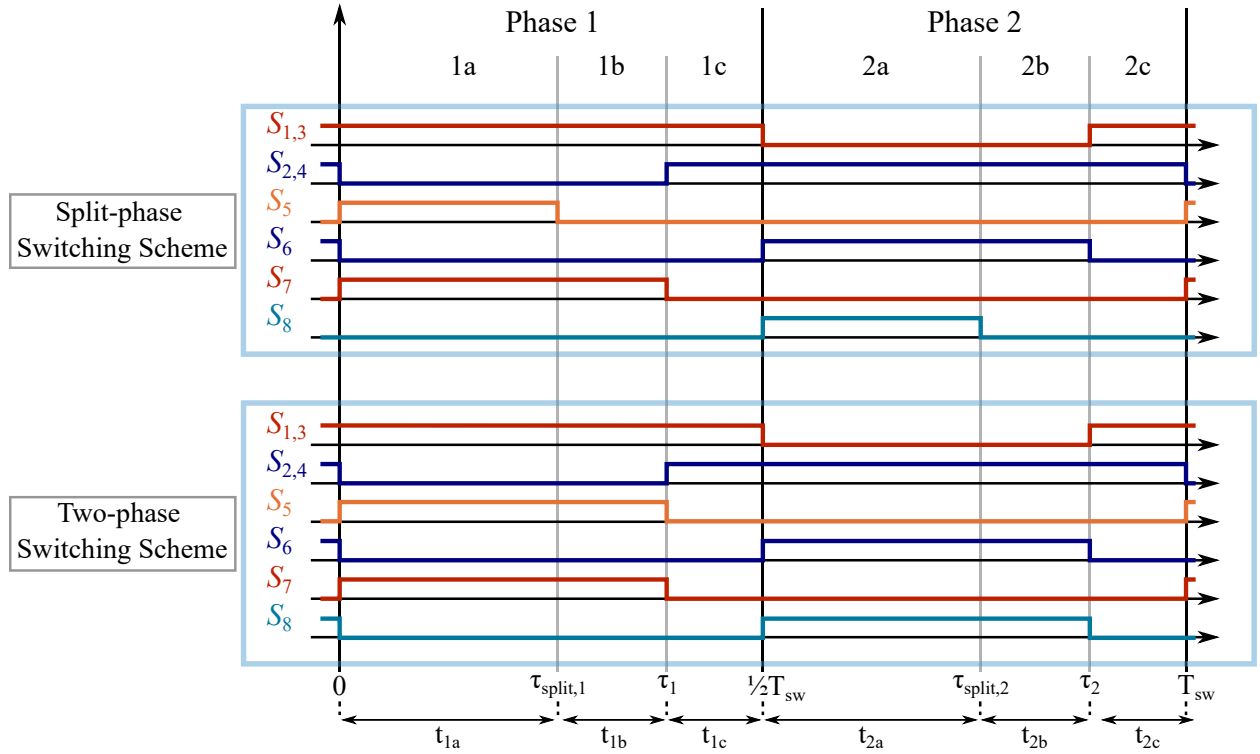


Figure 4.2: Gating signals for regulating split-phase and two-phase operation of the 4-to-1 hybrid Dickson converter.

phase and two-phase, regulating operation of the 4-to-1 hybrid Dickson converter. The main phases (1a and 2a), the split-phases (1b and 2b), and the regulating phases (1c and 2c) are illustrated. Regulating phases 1c and 2c are inserted within the switching scheme to regulate the converter output voltage to below its fixed-ratio voltage. The control of switches S_5 and S_8 (Fig. 4.1) is the fundamental change between split-phase (“soft-charged”) and two-phase (“hard-charged”) operation.

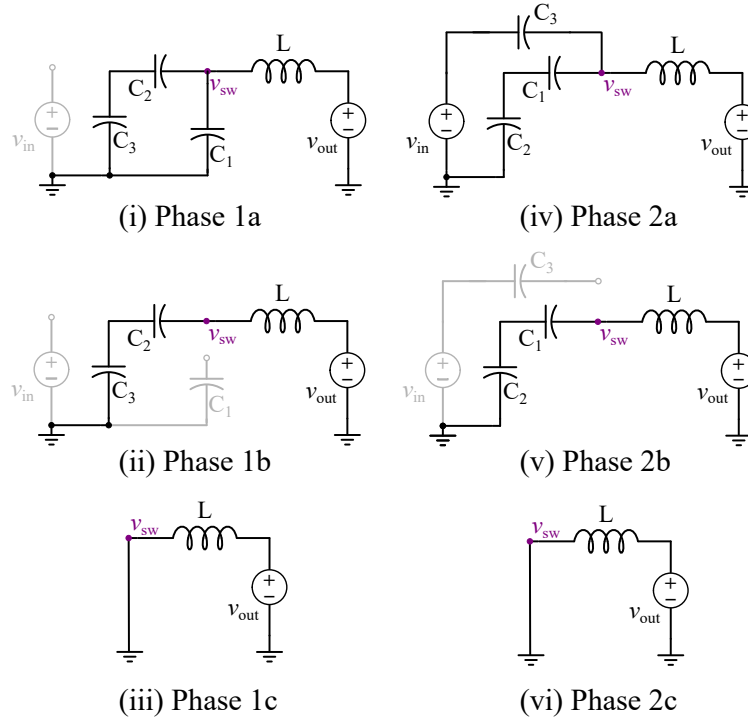


Figure 4.3: Equivalent circuits for each sub-phase of the converter.

Fig. 4.3 depicts the equivalent circuits of each of the phases necessary for full soft-charging, split-phase operation of the hybrid Dickson converter. Because the Dickson converter has the ability to operate in all three regimes – fully, partially, or not at all soft-charged – it is used as a case study in this work.

While the hybrid Dickson converter achieves high efficiency and power density metrics, modeling the flying capacitor dynamics and the effects of capacitor hard-charging in two-phase operation is non-trivial. Previous literature has introduced control and modeling strategies for pure SC and hybrid SC converters. However, these works only focused on two-phase operation [34] or provided minimal insight into the plant model of the converter itself [84]. Other works only examine the large signal response and output slew rate of the converter [12] or analyze the steady-state behavior without investigating the dynamic behavior [85]. It is a worthwhile effort to fully model these converter dynamics as the depth of

this modeling and the accuracy of the resulting plant model can impact closed loop controller design for SC converters.

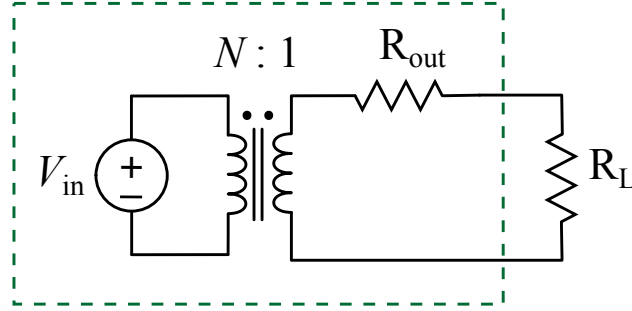
In this work, we develop a full small-signal model for the Dickson converter and compare the model results to a “transformer buck” model which assumes negligible flying capacitor voltage ripple. The “full model” presented in this work provides a more accurate description of flying capacitor dynamics to inform real-world controller design and provides insight into when the “transformer buck” model assumptions are no longer appropriate. The findings from the comparison between the two models are then used to develop insight into closed-loop controller design for both hard-charged and soft-charged SC converters. As a case study, we derive a small-signal model for both two-phase and split-phase operation of the hybrid Dickson converter and compare these models to the “transformer buck” model that is conventionally used to describe such circuits [12]. The two-phase operation results in a more damped circuit compared to the split-phase operation, and as such, necessitates a different compensator design compared to split-phase operation to achieve the same performance.

4.2 Large-Signal Modeling Framework

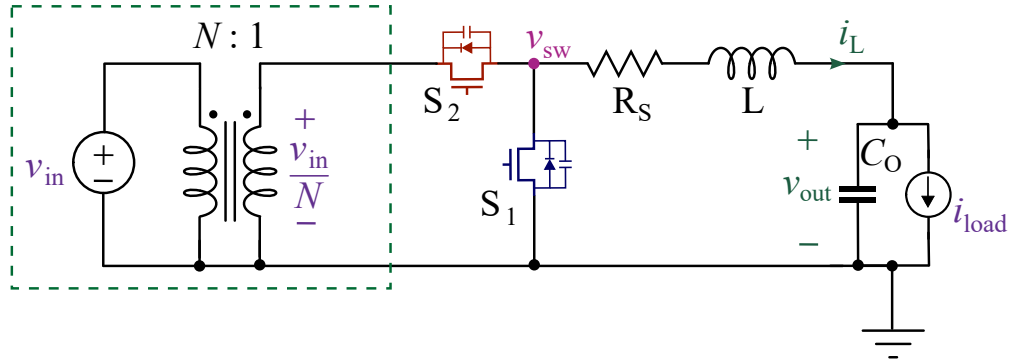
The simplest way to model hybrid SC converters is to approximate the SC network as an ideal transformer and to view the system as a buck converter with a reduced input voltage as shown in Fig. 4.4b. By assuming the flying capacitors have negligible voltage ripple, the SC network can be modeled using the generic pure SC converter model operating in the fast switching limit. This was first presented in [57], and Fig. 4.4a depicts this model of an SC converter with R_{out} representing the output impedance.

Cascading the SC network model with an inductor results in the “transformer buck” model. The effective lumped resistance (R_S) in the model is comprised of the on-resistance of the switches (R_{on}), the ESR of the flying capacitors (R_{esr}) and the resistance of the inductor (R_L). The lumped resistance R_S is representative of the converter operating in the fast switching limit (FSL), so we are not accounting for any frequency-dependent resistances or charge-sharing losses. The full voltage conversion ratio of the hybrid SC converter can then be allocated differently between the SC stage and the buck stage [12]. This “transformer buck” model reduces the order of the system and allows different levels of hybrid SC converters to be condensed into the same model. While this model greatly reduces the complexity of the system, information about the flying capacitor dynamics is lost. Although the voltage ripple of flying capacitors is commonly neglected to implement complex control strategies [86], many hybrid SC converters are operated with large capacitor voltage ripple to reduce the size of the flying capacitors and increase overall power density. Therefore, a model that incorporates the dynamics of the flying capacitors is required to fully capture the dynamical behavior of the hybrid SC converter.

The procedure for deriving both a large-signal and small-signal model including the flying capacitor dynamics is outlined here, and the hybrid Dickson converter is used as an example. The first step of constructing this model is to derive the state matrices for the hybrid Dickson



(a) Model of a fixed-ratio switched-capacitor (SC) converter.



(b) “Transformer buck” hybrid switched capacitor (SC) converter model.

Figure 4.4: Models of fixed-ratio SC converter and “transformer buck” hybrid SC converter. The dashed box shows where the pure SC converter model fits within the “transformer buck” model.

converter (Fig. 4.1), and R_{on} , R_{esr} , and R_L are included in the circuit state analysis. The fundamental state-space equation (Eqn. 4.1) represents the first-order differential equations describing the system.

$$\dot{x} = A \cdot x + B \cdot u \quad (4.1)$$

The state variables and inputs are assigned as shown in Eqns. 4.2 and 4.3 , and the state matrices are written out for each of the main and split-phases of the circuit.

$$x = \begin{bmatrix} v_{C1} & v_{C2} & v_{C3} & i_L & v_{out} \end{bmatrix}^T \quad (4.2)$$

$$u = \begin{bmatrix} v_{in} & i_{load} \end{bmatrix}^T \quad (4.3)$$

The final form A and B state matrices for each of the main, split-, and regulating phases are given in Appendix B.

All of the following analysis is conducted for the hybrid Dickson converter operating at or above resonance. If the hard-charging time constant¹ of the flying capacitors is much less than the resonant time period of the flying capacitors and inductor, then the hard-charging will result in impulse changes in the flying capacitor voltages. These large changes in flying capacitor voltage are not well represented by the average voltage during a circuit state. Furthermore, while a 4-to-1 hybrid Dickson converter has an even switched-capacitor conversion ratio, it is an odd-order system. Therefore, if we consider a lossless system, a steady-state indeterminacy arises [87]. Even with resistances included, equal disturbances in the voltages of flying capacitors C_1 and C_3 will result in a valid steady-state solution. Thus, standard averaging techniques cannot accurately describe the system. We are able to show this using the fundamental state-space equation. Illustratively, using the fundamental state-space equation (Eqn. 4.1) and setting $\dot{x} = 0$ to solve for the steady-state solution necessitates an invertible A matrix. In this case, we are unable to solve for the steady-state solution as the A matrix is non-invertible.

Figs. 4.5 and 4.6 show the magnitude and the phase of the converter output impedance ($Z_{\text{out}}(z) = -\frac{v_{\text{out}}}{i_{\text{out}}}(z)$), respectively. The “Full Model” label in these figures is a discrete-time model, and this will be described in more detail throughout the rest of this chapter. The results of the averaged model compared to the results from other modeling techniques are shown. The averaged model results deviate from the “Full Model”, further validating the claim that averaging does not capture the system dynamics accurately.

¹The hard-charging time constant of the flying capacitors is defined here as a dominant RC time constant related to the parasitic resistances in the hard-charging path (R) and the connected hard-charged flying capacitors (C).

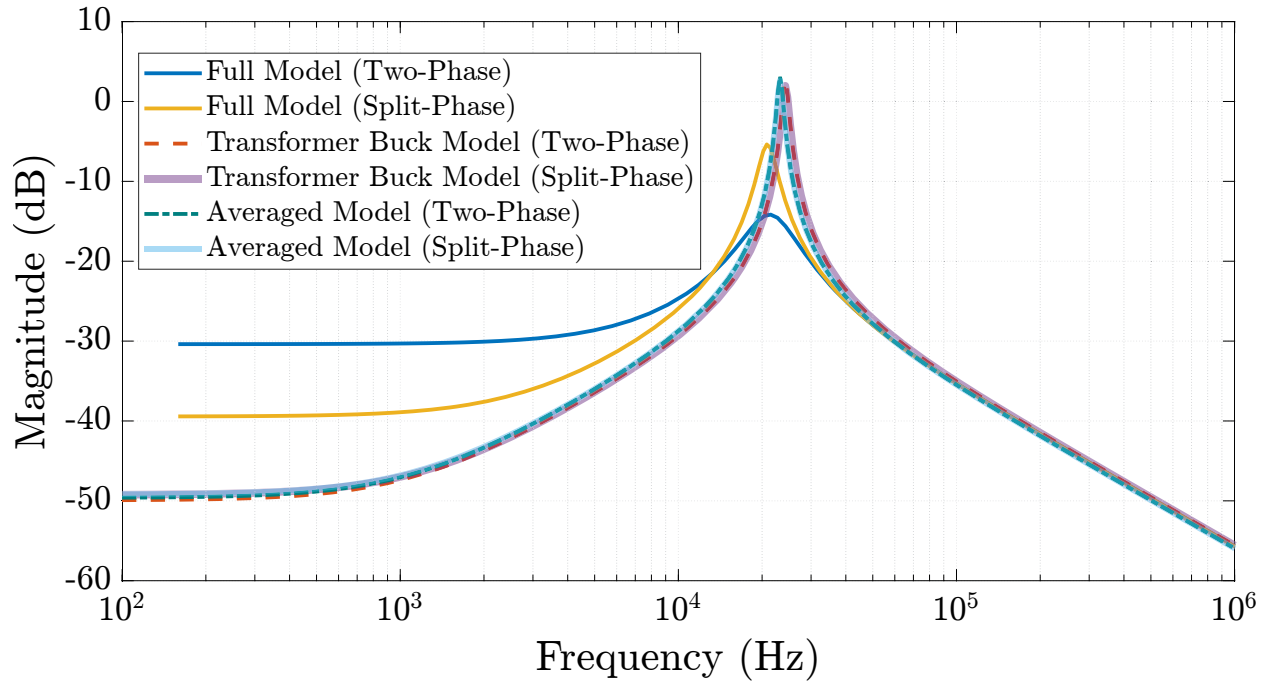


Figure 4.5: Model output impedance comparison - magnitude.

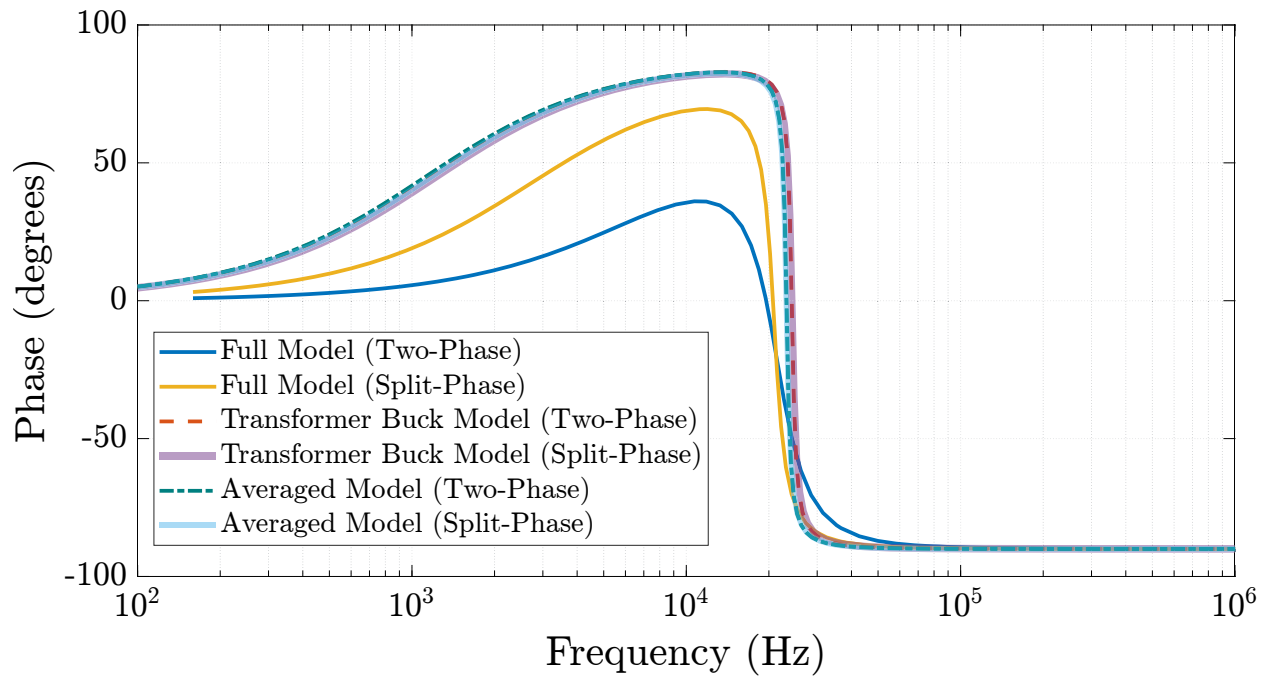


Figure 4.6: Model output impedance comparison - phase.

Because averaging techniques do not sufficiently capture system dynamics, discrete-time modeling [88] is used to investigate how a sample of our state vector evolves over a switching period. To illustrate this, Fig. 4.7 shows an example state variable waveform with key points along the periodic waveform and key time intervals labeled. To find the value of the state vector at the end of each phase (state vector value at $\tau_{\text{split},1}$, τ_1 , $1/2T_{\text{sw}}$, etc.), we use Eqn. 4.4 to calculate its dependence on the previous state variables (φ in Eqn. 4.4) and the dependence on the inputs (γ in Eqn. 4.4). The φ and γ terms are derived for each switching phase within the switching period. As an example, Eqns 4.5 and 4.6 show how these values are calculated for Phase 1a.

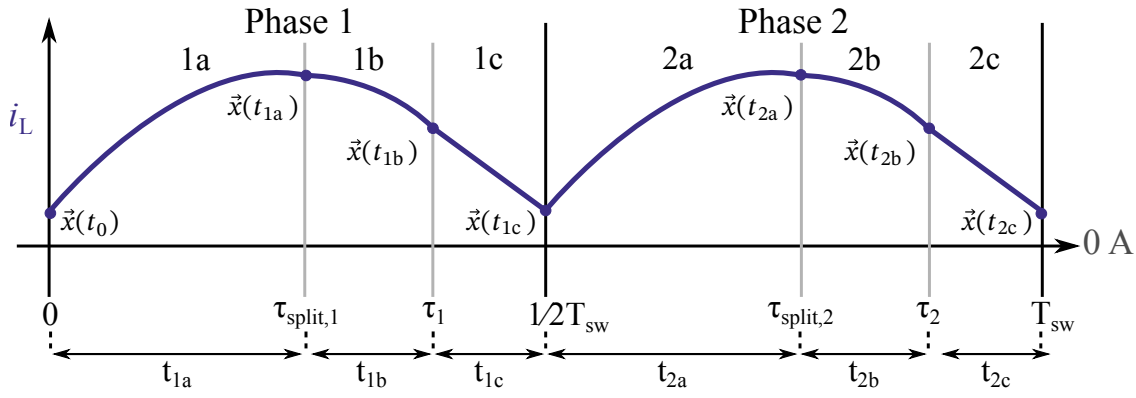


Figure 4.7: Example inductor current state variable waveform and its evolution in the regulated hybrid Dickson converter.

$$\vec{x}[n+1] = \varphi \vec{x}[n] + \gamma \vec{u}[n] \quad (4.4)$$

$$\varphi_{1a} = e^{A_{1a}t_{1a}} \quad (4.5)$$

$$\gamma_{1a} = e^{A_{1a}t_{1a}} \int_0^{t_{1a}} e^{A_{1a}\tau} B_{1a} d\tau \quad (4.6)$$

Finally, Eqns. 4.7, 4.8, and 4.9 accumulate each circuit state across each switching phase to solve for the state vector behavior across the entire period. The accumulation of φ 's and γ 's over all of the phases allows us to find the discrete-time A and B matrices, A_d and B_d , respectively.

$$\vec{x}[t_0 + T_{\text{sw}}] = A_d \vec{x}[t_0] + B_d \vec{u}[t_0] \quad (4.7)$$

$$A_d = \varphi_{2c}\varphi_{2b}\varphi_{2a}\varphi_{1c}\varphi_{1b}\varphi_{1a} \quad (4.8)$$

$$B_d = (\varphi_{2c}\varphi_{2b}\varphi_{2a}\varphi_{1c}\varphi_{1b}\gamma_{1a}) + (\varphi_{2c}\varphi_{2b}\varphi_{2a}\varphi_{1c}\gamma_{1b}) \\ + (\varphi_{2c}\varphi_{2b}\varphi_{2a}\gamma_{1c}) + (\varphi_{2c}\varphi_{2b}\gamma_{2a}) + (\varphi_{2c}\gamma_{2b}) + \gamma_{2c} \quad (4.9)$$

4.3 Small-Signal Modeling Framework

To find the transfer function mapping the control action (duty cycle) to the output voltage, a small-signal model was developed for the Dickson converter. The duty cycle is defined as $D = \frac{t_{1a}+t_{1b}}{T_{sw}} = \frac{t_{2a}+t_{2b}}{T_{sw}}$. The general form small-signal discrete-time model can be written as

$$\hat{x}[n+1] = \varphi\hat{x}[n] + \gamma\hat{d}[n] \quad (4.10)$$

$$\hat{y}[n+1] = C\hat{x}[n] \quad (4.11)$$

where Eqn. 4.10 describes how the effects of perturbations in the duty cycle ($\hat{d}$) are propagated during converter switch states and Eqn. 4.11 shows the output state space equation [89]. The C matrix in Eqn. 4.11 relates the state vector to the output and is written as

$$C = [0 \quad 0 \quad 0 \quad 0 \quad 1]. \quad (4.12)$$

Fig. 4.8 shows the same example inductor current state variable waveform as before but provides a more detailed view of the small-signal dynamics. As a note, Fig. 4.8 only shows the waveforms for half of a given switching period ($T_{sw}/2$) as the second half of the switching period behaves in the same manner. In Fig. 4.8, we consider the effect of perturbations $0.851\hat{d}$ and $0.149\hat{d}$ on the duty cycle. The ratios 0.851 and 0.149 are chosen based on the steady-state split-phase timings, and the duty ratios are scaled such that the overall switching period still remains the same. The first perturbation that occurs in the state is marked by $\hat{x}_{d1}$ in the figure. The second perturbation is marked by $\hat{x}_{d2}$. Each of these perturbations can be mathematically described as

$$\gamma\hat{d}[n] = \hat{x}_{d1} = 0.851(A_{1a}X_{p1a} + B_{1a}U)\hat{d}T_{sw} \quad (4.13)$$

and

$$\hat{x}_{d2} = [0.149(A_{1b} - A_3)X_{p1b} + 0.149(B_{1b} - B_3)U]\hat{d}T_{sw}. \quad (4.14)$$

where X_{p1a} and X_{p1b} are the steady-state values of the state variable at the end of each of the original switching states. Eqn 4.13 considers the impact of t_{1a} being $0.851\hat{d}T_{sw}$ longer. Eqn 4.14 considers the impact of t_{1b} being $0.149\hat{d}T_{sw}$ longer and t_{1c} being $\hat{d}T_{sw}$ shorter. The steady-state values are solved for using the previously developed large-signal model using

$$X_p = (I - A_d)^{-1} \cdot B_d U. \quad (4.15)$$

The small-signal control action (duty cycle) to output voltage ($G_{vd}(z) = \frac{v_{out}}{d}(z)$) transfer function (z-domain) is then given by

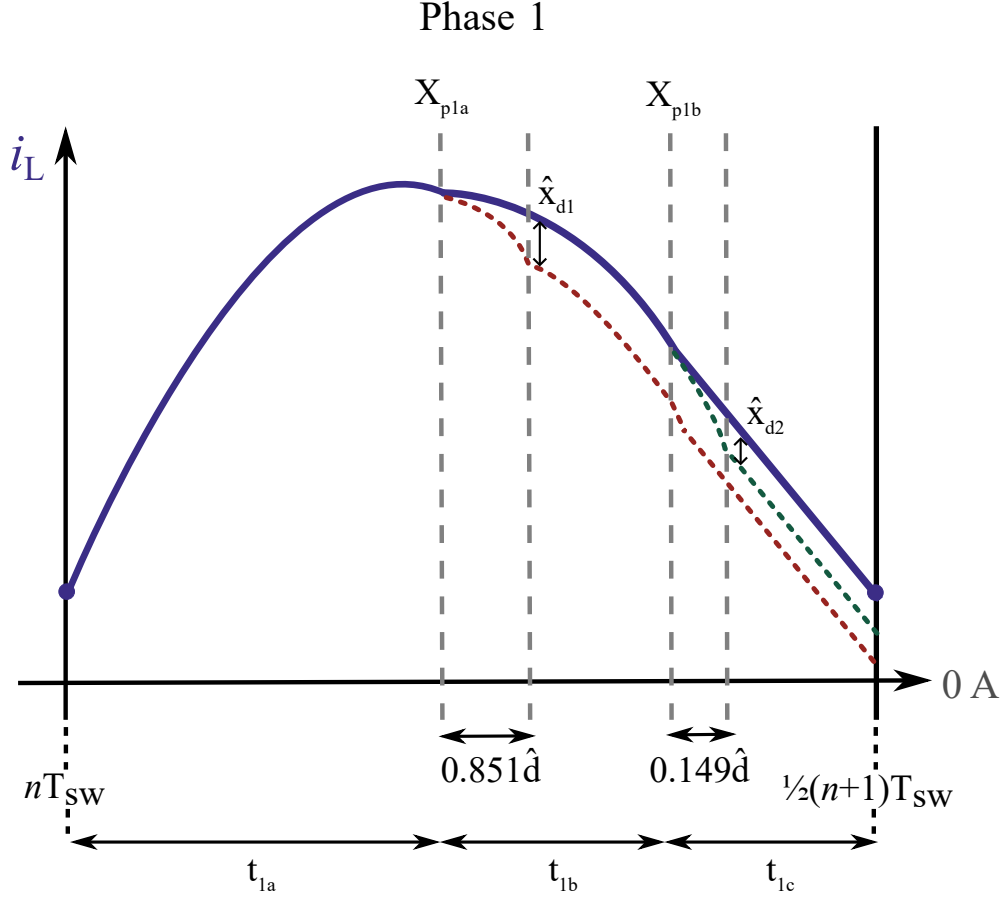


Figure 4.8: Example inductor current state variable waveform showing the propagation of perturbations in the duty cycle. Dimensions are exaggerated to show perturbation effects more clearly.

$$G_{vd}(z) = \frac{\hat{v}_{out}}{\hat{d}} = \frac{C(I - z^{-1}\varphi)^{-1}\gamma}{z} \quad (4.16)$$

where I is the identity matrix.

4.4 Modeling and Experimental Results

The large-signal and small-signal discrete-time models are validated in both simulation and hardware. The results of this validation provide insights into the open-loop dynamic response and closed-loop controller design for hybrid SC converters. Deriving this complete discrete-time model also allows us to see under what conditions the full circuit model approaches the “transformer buck” model. For the hybrid Dickson converter case study, these results are used to gain insights into the dynamics of the output voltage of the converter under both

two-phase and split-phase operation.

The eigenloci of the Dickson converter are shown in Fig. 4.9 where the flying capacitance, C_{fly} , is swept from $2.64 \mu\text{F}$ to $26.4 \mu\text{F}$ in simulation. This analysis assumes that all the flying capacitors are equally sized. It is noted that all of the eigenvalues are located within the unit circle in the complex plane ($|\lambda_i| < 1, \forall i$) rendering the system asymptotically stable. While all five eigenvalues are depicted in the left plot, the output voltage does not participate in all of the modes corresponding to all the eigenvalues. The dominant eigenvalues are highlighted in the right plot of Fig. 4.9, and these eigenvalues are useful in characterizing and providing insights into the dynamic behavior of the system.

As C_{fly} increases, the two-phase Dickson converter and the split-phase Dickson converter eigenvalues converge. Additionally, these eigenvalues approach the eigenvalues predicted by the “transformer buck” model evaluated with split-phase timings. This is consistent with the assumption that the “transformer buck” model has infinitely large C_{fly} and is operating in FSL. Qualitatively, the increasing C_{fly} leads to reduced flying capacitor voltage ripple and, therefore, reduced hard-charging in the two-phase Dickson converter. With this increasing C_{fly} , the two-phase operation and split-phase operation eventually converge and become more similar to the “transformer buck” model, which is most representative of a converter operating very far above resonance.

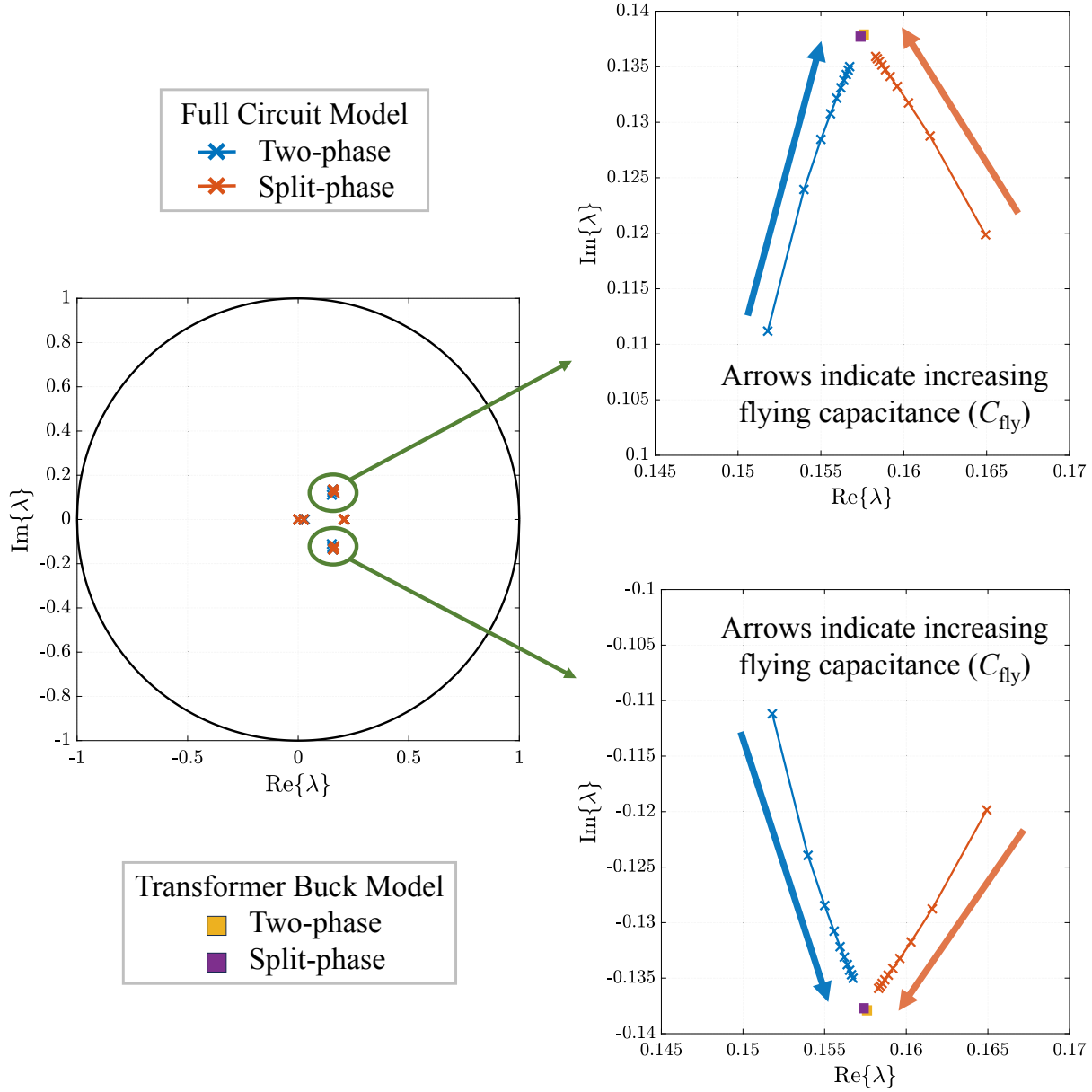


Figure 4.9: Eigenloci of the Dickson converter with C_{fly} swept. The arrows indicate the direction the eigenvalues move as C_{fly} increases. The output voltage participates in the dynamic modes corresponding to the eigenvalues highlighted in the zoomed-in plot.

The transfer functions for the output impedance ($Z_{\text{out}} = -\frac{v_{\text{out}}}{i_{\text{out}}}(z)$) and control action (duty cycle) to output voltage ($G_{vd}(z) = \frac{v_{\text{out}}}{d}(z)$) were found from the discrete time model and are plotted in Fig. 4.10 and Fig. 4.11 respectively. Eqn. 4.17 shows how the dc gain is calculated for the output impedance Bode plot, where x is the dc gain. A similar approach

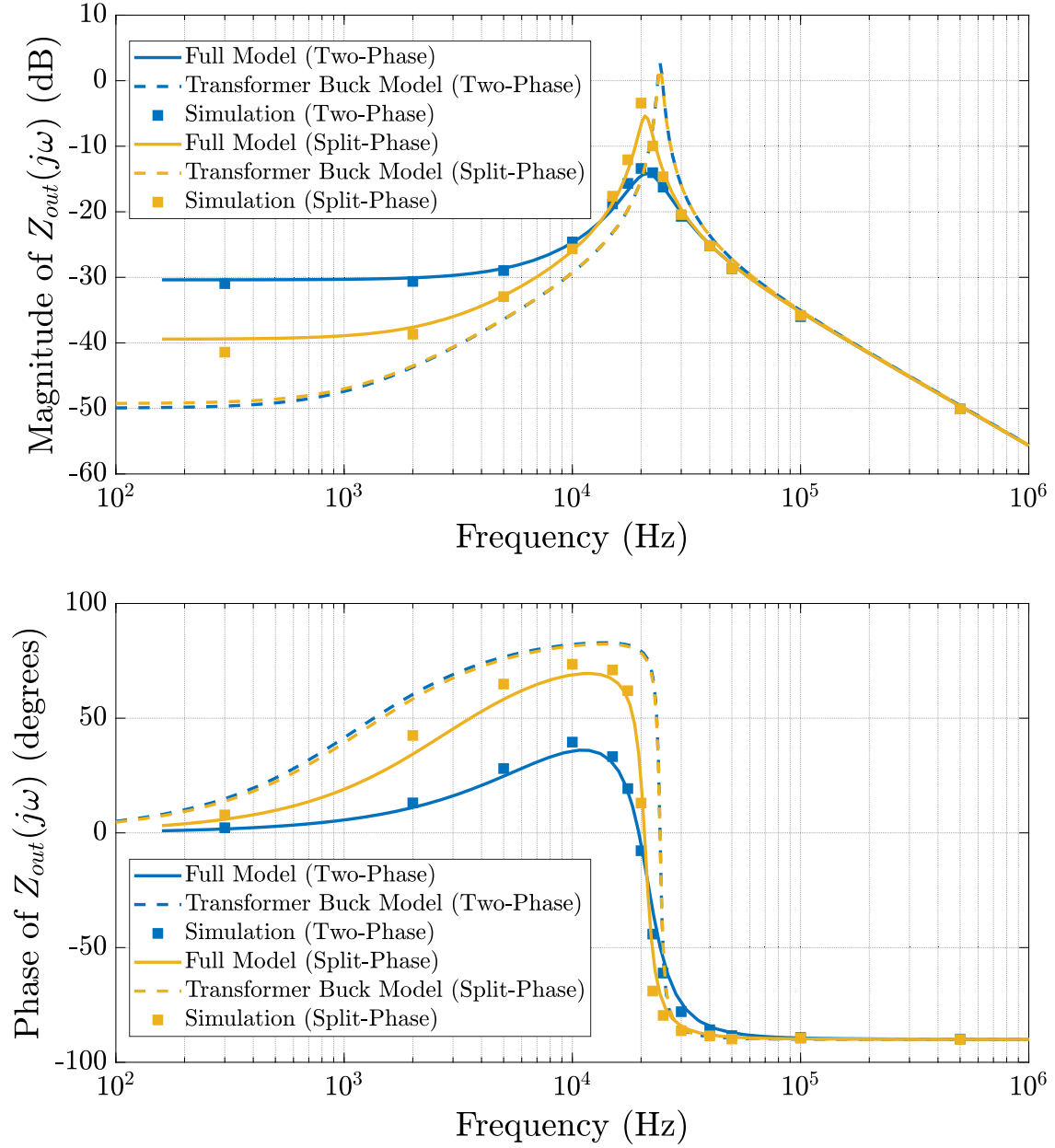


Figure 4.10: Bode plot of the transfer function representing the output impedance ($Z_{out} = -\frac{v_{out}}{i_{out}}$).

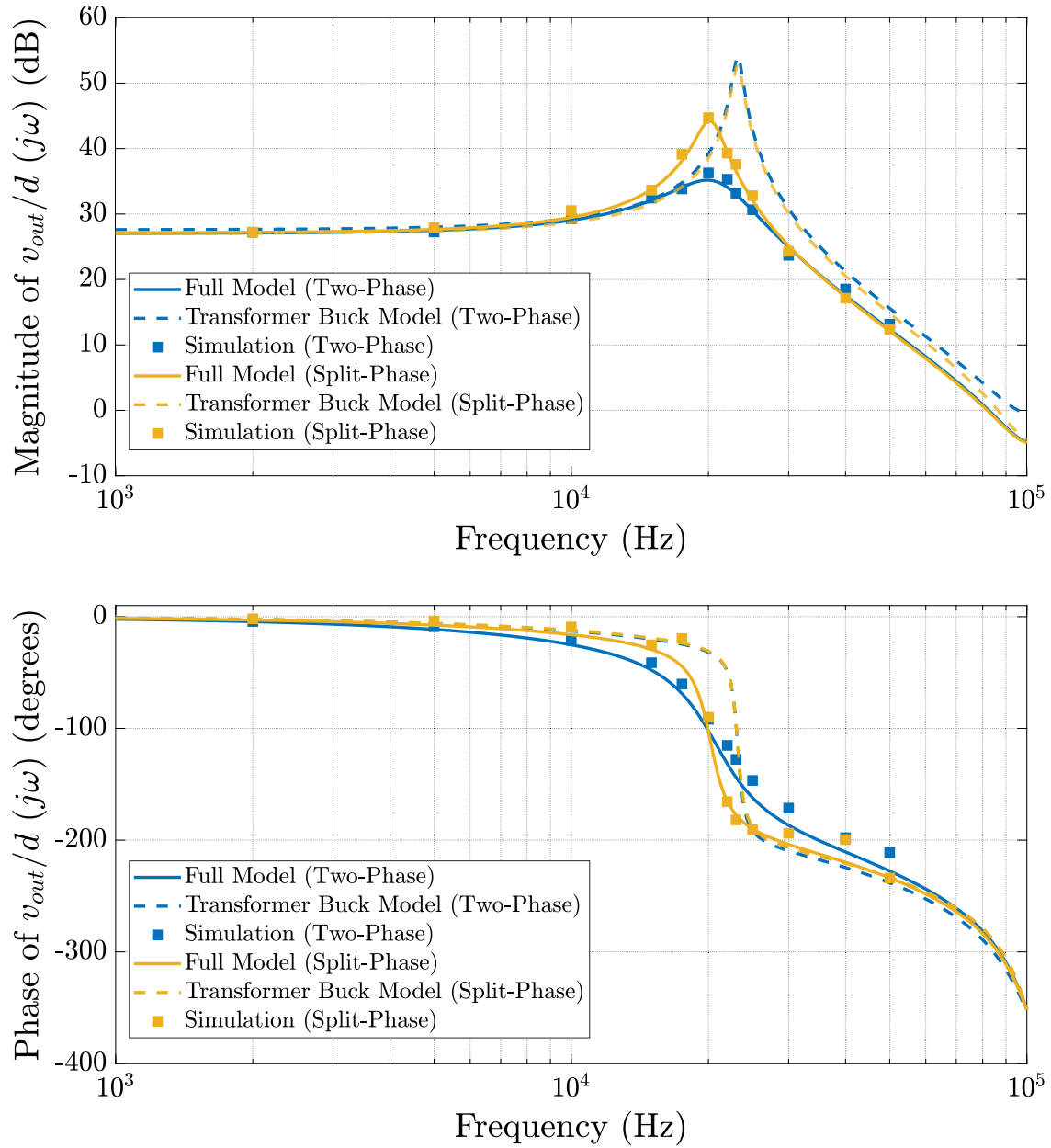


Figure 4.11: Bode plot of the transfer function representing the control input to output voltage.

can be used to calculate the control action to output voltage dc gain.

$$\Delta v_{\text{out}} = 10^{x/20} \cdot \Delta i_{\text{out}} \quad (4.17)$$

In both cases, by omitting the influence of the flying capacitor dynamics, the “transformer buck” model overestimates the resonant frequency of the response compared to the full circuit models by about 3 kHz or 16%. Additionally, compared to the other models, the model of the Dickson converter in two-phase operation has a much lower quality factor, indicating more damping. The increased damping seen in the model can be attributed to the hard-charging loss mechanism present in the converter in two-phase operation, resulting in much higher overall loss compared to the split-phase case. The difference in damping between the two models indicates that different compensators must be designed in the case of two-phase vs. split-phase operation to achieve the same closed-loop performance.

The discrete-time model evaluated in this work is validated in hardware using a 4-to-1 hybrid Dickson prototype. The hardware prototype is pictured in Fig. 4.12, and its design parameters are listed in Table 4.1. The converter is operated at a 48 V to 10 V voltage conversion ratio with an output power of 50 W. Table 4.2 lists the major components used in the power stage design.

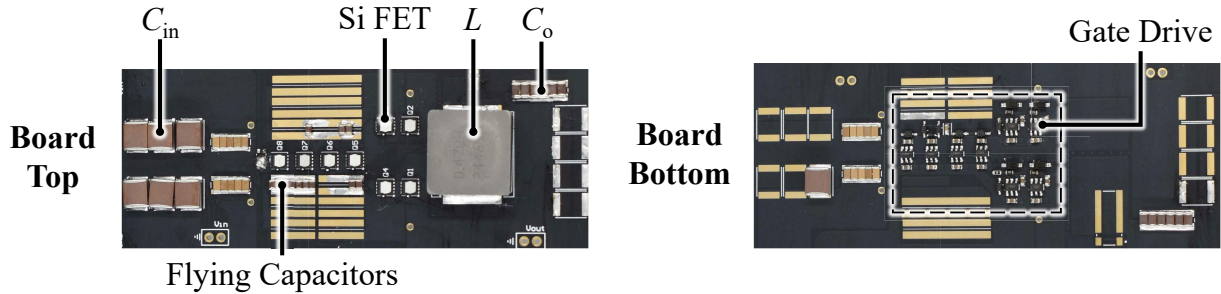


Figure 4.12: Photograph of top and bottom of hardware prototype. The hardware prototype was designed by Nagesh Patle.

A duty cycle step from 0.40 to 0.42 was applied to the converter output and the open-loop output voltage response is compared for the Dickson converter operating with the two-phase and split-phase switching schemes. The resulting transient output voltage waveforms are shown in Fig. 4.13 and 4.14, with a quantitative comparison tabulated in Table 4.3 where f_d is the oscillation frequency and τ_d is the damping time constant.

Notably, the frequency of the oscillations of the split-phase operation matches with the resonant frequency found by the full, discrete-time model with a value of approximately 21 kHz. In two-phase operation, we note a larger discrepancy between experiment (21.025 kHz)

Table 4.1: Converter Operating Parameters

Parameter	Value	Units
V_{in}	48	V
V_{out}	10	V
I_{out}	5	A
f_{sw}	203	kHz
f_{res}	135	kHz
L	0.47	μ H
C_{fly}^*	2.64	μ F
C_o^*	100	μ F

* Voltage-de-rated values.

Table 4.2: Component Listing of the Hardware Prototype

Component	Mfr. & Part Number	Parameters
Dickson Power Stage		
Switches $S_1 - S_8$	Infineon IQE013N04LM6CGSC	Si, 40 V, 1.35 m Ω
Flying Capacitors C_1, C_2, C_3	Murata GRM31C5C1H224GE02L	C0G, 50 V, 12 x 0.22 μ F
Inductor L	Vishay Dale IHLP6767GZERR47M11	0.47 μ H, 57 A I_{sat}
Output Capacitors C_o	Murata GRM31CC81E226KE11L	X6S, 25 V, 22 μ F
Gate Drive		
Si Gate Driver	Analog Devices Inc. LTC4440ES6	Single high-side driver
Controller Board		
FPGA	Terasic Inc. P0466	DE10-Lite, Max10 FPGA

and the predicted (20.933 kHz) oscillation frequencies. This is due to less derating of the output capacitor considering that the steady-state voltage in the two-phase case is lower due to higher losses. Moreover, the output voltage experiences more oscillations in split-phase operation than in two-phase operation, which is consistent with the model predicting less damping for the split-phase case. The damping time constant in hardware is smaller than what was predicted by the full model. The model does not account for device switching loss such as overlap loss, and C_{oss} loss, which likely contributes to much of this time constant discrepancy.

4.5 Conclusion and Future Work

This work explores the effects of hard-charging and soft-charging on the dynamics of hybrid switched-capacitor converters. A 4-to-1 Dickson converter is used as a case study where two-

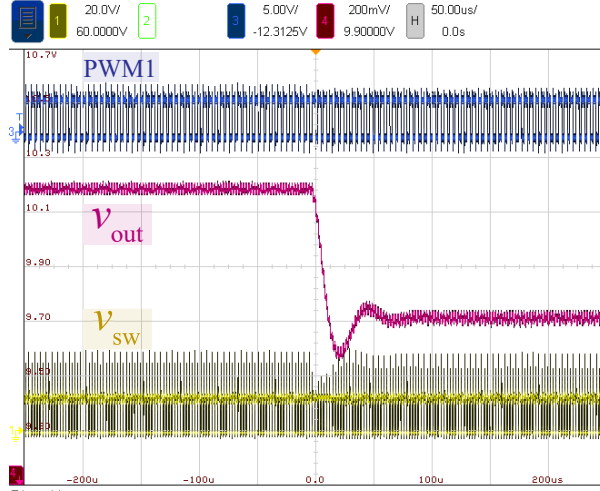


Figure 4.13: Experimental output voltage response to a step in duty cycle with two-phase operation.

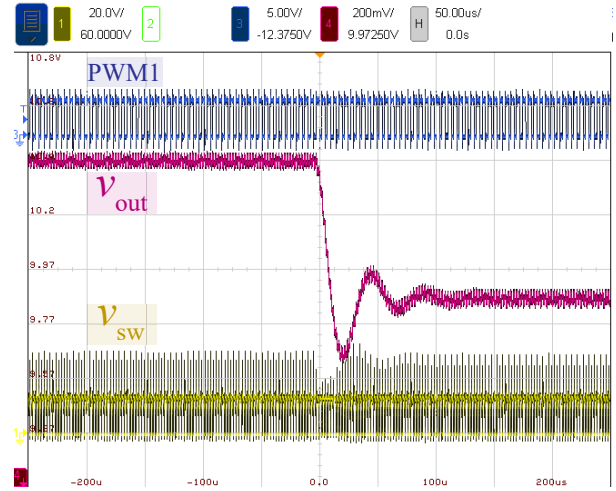


Figure 4.14: Experimental output voltage response to a step in duty cycle with split-phase operation.

Table 4.3: Summary of Transient Response Parameters With Two-Phase and Split-phase Switching Schemes

	f_d	τ_d
No Split-phase		
Experiment	20.429 kHz	0.019 ms
Full Model Prediction	20.849 kHz	0.2216 ms
Transformer Buck Model Prediction	24.245 kHz	1.6287 ms
With Split-phase		
Experiment	21.025 kHz	0.0277 ms
Full Model Prediction	20.933 kHz	0.651 ms
Transformer Buck Model Prediction	24.243 kHz	1.5056 ms

phase operation results in hard-charging of the flying capacitors and split-phase operation enables the soft-charging of the flying capacitors. In either mode of operation, a “transformer buck” model is insufficient for capturing the effects of the flying capacitors on the output voltage dynamics. Additionally, the hard-charging in two-phase operation results in more damping and requires a different compensator design compared to split-phase operation.

The modeling approach presented in this chapter creates many new avenues of future research. The insights gained from this model can be used to influence closed-loop compensator design and controller bandwidth. The effects of hard- and soft-charging operation on

compensator design should be further investigated, as the tradeoffs between compensator designs for these two systems is valuable to hybrid SC converter designers. For hybrid SC converters used in applications where load changes are predictable, a controller could be designed around leveraging hard-charging dynamics during a transient event. Furthermore, this modeling technique can be extended and generalized to other hybrid SC converters, including the HISID variant of this Dickson converter.

Chapter 5

Design and Implementation of a GaN-Based, Cascaded Isolated DC-DC Converter for Satellite Applications

Portions of this chapter are adapted in whole or in part from [90]. The major practical consideration explored in this chapter is isolation.

5.1 Isolation in Power Converters

Isolation refers to a technique for electrically separating two domains in a system such that electrons cannot flow directly from the converter input to the converter output. It is a critical practical consideration for systems with disparate voltage levels and in systems where noise is a major concern. In power converters within transportation applications, isolation is typically required for two major reasons: signal integrity and human safety.

The converter designed in this chapter is presented in the context of satellites in space. This application requires isolation to prevent noise from propagating from higher voltage/power loads and to achieve improved signal integrity.

In the automotive domain, both EV and hybrid EV architectures differ from ICE architectures due to the multiple batteries and voltage levels that these vehicles need to support. While the higher voltages (400 V, 800 V, etc.) must be isolated from the low-voltage domain, isolation can also be useful within low-voltage power conversion itself.

Findings from the work in this chapter can be extended to hybrid EVs and fully-electric vehicles where increased noise immunity is imperative for low-voltage architectures on-board the vehicle. For example, an isolated dc-dc converter may be required between the 48 V and 12 V voltage rails to prevent common-mode noise on the 48 V ground from coupling onto

the 12 V side [91]. Faults occurring on the 48 V side can also be isolated from the 12 V lower-voltage side in this way.

Fig. 5.1 shows a simplified block diagram of an isolated system. The isolation barrier shown in the diagram can take many forms, including magnetic, capacitive, and optical isolation. This dissertation focuses on designing and using magnetics (transformers) for this isolation barrier.

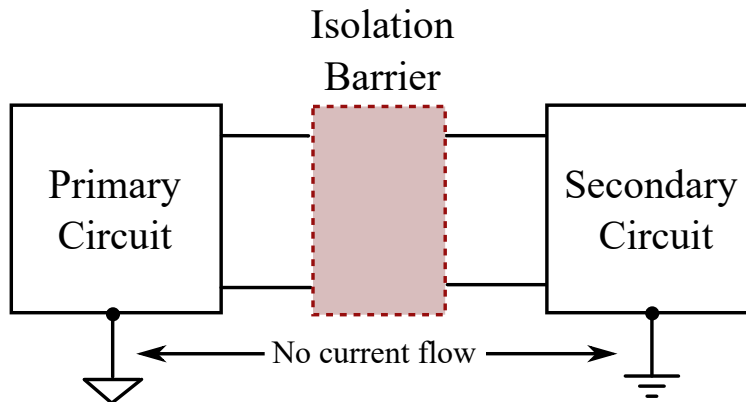


Figure 5.1: Basic concept of isolation between the primary and secondary sides of a circuit shown using a transformer.

5.2 Introduction

As space exploration progresses, there is a need for increased propulsion capability in satellite systems. CubeSat and SmallSat class spacecrafts are gaining popularity and becoming compelling alternatives to traditional, heavy-weight satellites. In these applications, often a wide range of input and output voltages must be supported to handle large voltage swings in dynamic loads such as metal plasma thrusters (MPTs), a type of electric propulsion system [92]. MPTs utilize a resonant high-voltage circuit, fed by a low voltage (less than 45V) dc source, to create an arc which ionizes a small portion of a solid metal puck in a pulsed manner [92]. The low-voltage dc source is partially discharged in each pulse, requiring an isolated dc-dc converter with a wide operating range to ramp up the dc source voltage after each pulse. Moreover, it is desirable to provide the dc-dc power conversion through galvanically isolated converters, to prevent noise from propagating from high voltage/power loads to sensitive on-board equipment.

To generate this wide range of voltages, and to keep up with advancements in satellite technology, a light, power-dense, and efficient power converter is required. Therefore, innovations in the area of high performance, high power density power converters are imperative to the continued improvement of such systems. However, the extreme environments of

aerospace power systems present unique design challenges in isolation, form factor, thermal management, and reliability.

In aerospace applications where high-step-up or high-step-down voltage conversion is needed, hybrid switched-capacitor topologies are compelling alternatives to conventional power converter designs [93, 94]. In satellite applications with narrower voltage operating ranges, the flyback and forward converters [95] are common power converter solutions. While the flyback is a simple, galvanically-isolated solution with the necessary buck-boost capability, it is limited by higher peak currents and voltages present in the switches and transformer. This can lead to penalties in efficiency and power density compared to other isolated topologies [96].

Cascaded power converter architectures have been investigated in previous work [97] to overcome some of these limitations. Additionally, improvements can be made to other aspects of the power stage – such as the magnetics design and implementation – in order to increase the overall power density of the system. Illustratively, a similar cascaded buck converter and LLC structure is investigated in [98] for railway applications and is able to achieve high efficiencies using a planar magnetic structure and GaN HEMTs. Zero-voltage switching (ZVS) full-bridge topologies are gaining traction in industry for low-power, radiation-tolerant space applications [99]. However, in each of these prior works, the converter has only fulfilled the need to step down the input voltage. For many satellite applications with wide input and output voltage ranges, the power converter must both step down and step up the input voltage, or both “buck” and “boost” the input voltage. This work further explores how to use many of the advances made in both academic and industrial power topologies to increase converter efficiencies while still ensuring that radiation tolerance and isolation requirements are met in this application for space.

This work investigates a two-stage, isolated, GaN-based, dc-dc power converter. The boost converter takes a variable input voltage and is used as a regulating, non-isolated first stage to create a stiff intermediate bus voltage input to the dual active bridge (DAB) converter stage. The DAB converter provides galvanic isolation and additional voltage conversion via a planar transformer. The DAB converter is characterized by high efficiencies, making it an attractive option for applications where thermal management and loss minimization is crucial. The topology is also able to handle a broad range of input voltages, which makes it an appropriate second stage in this case. The proposed design utilizes components selected for radiation tolerance and with appropriate voltage derating. Furthermore, the custom planar transformer serves to increase volumetric power density and thermal performance of the total system.

This chapter presents the design, implementation, and operation of a cascaded, two-stage power converter for satellite applications. The remainder of this chapter is organized as follows: Section 5.3 of the work details the selection of the two stages for the cascaded topology, as well as the converter theory of operation and design. Section 5.4 discusses the converter implementation with special attention given to planar transformer design and component selection. This section also includes specifications for the experimental prototype as well as waveforms and efficiency results for the prototype. Finally, Section 5.5 concludes

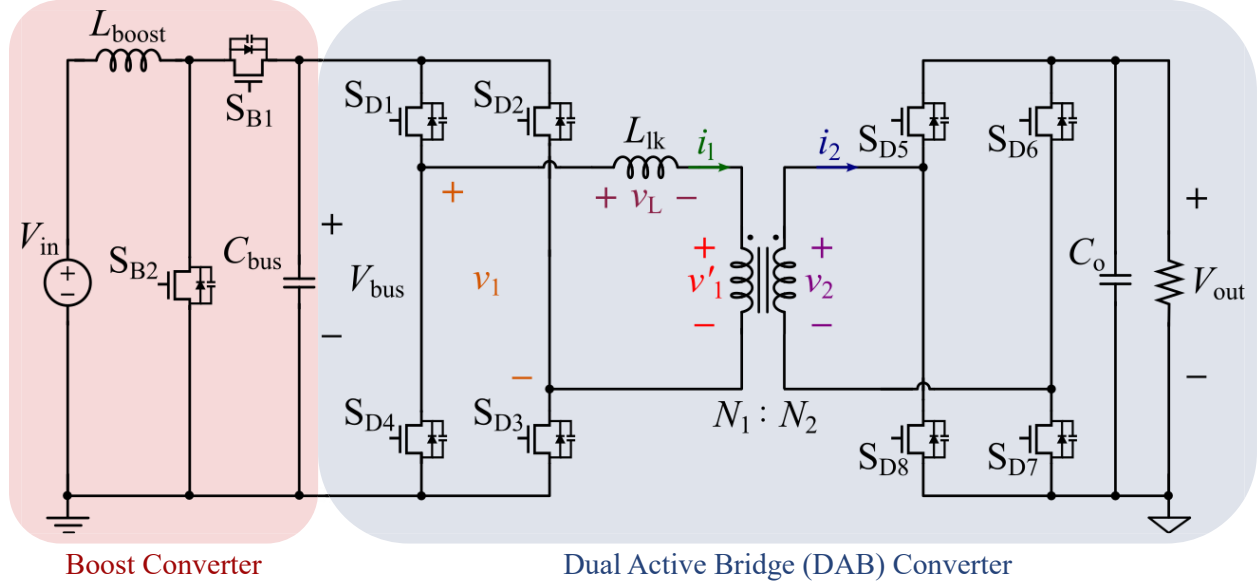


Figure 5.2: Schematic of the cascaded boost and dual active bridge topology architecture.

the chapter.

5.3 Cascaded Converter Topology Selection and Design

A two-stage converter design provides a modular and flexible solution for the power converter in this application in lieu of the conventional flyback converter. The schematic for the two-stage buck-boost architecture is shown in Fig. 5.2. The boost stage takes the variable input voltage and converts it to a fixed intermediate bus voltage. The output of the boost converter serves as the stiff input to the DAB converter, which then operates as a fixed-ratio galvanically isolated stage with a tunable power level. The two-stage approach is beneficial as each of the converter stages can be optimized and controlled separately such that the boost stage regulates the converter voltage, and the DAB stage regulates power flow.

Boost Front-End Stage Design

The first stage of the cascaded power converter consists of a synchronous boost converter. The boost converter supports a wide input voltage range of 18 - 36 V. Using GaN HEMTs, this stage boosts the input voltage up to an intermediate bus voltage (V_{bus}) with a range of 40 - 60 V. This is determined by a duty cycle $D = 1 - \frac{V_{in}}{V_{out}}$. The boost converter operates at a fixed frequency of 700 kHz to maintain a peak-to-peak inductor current ripple of 30 -

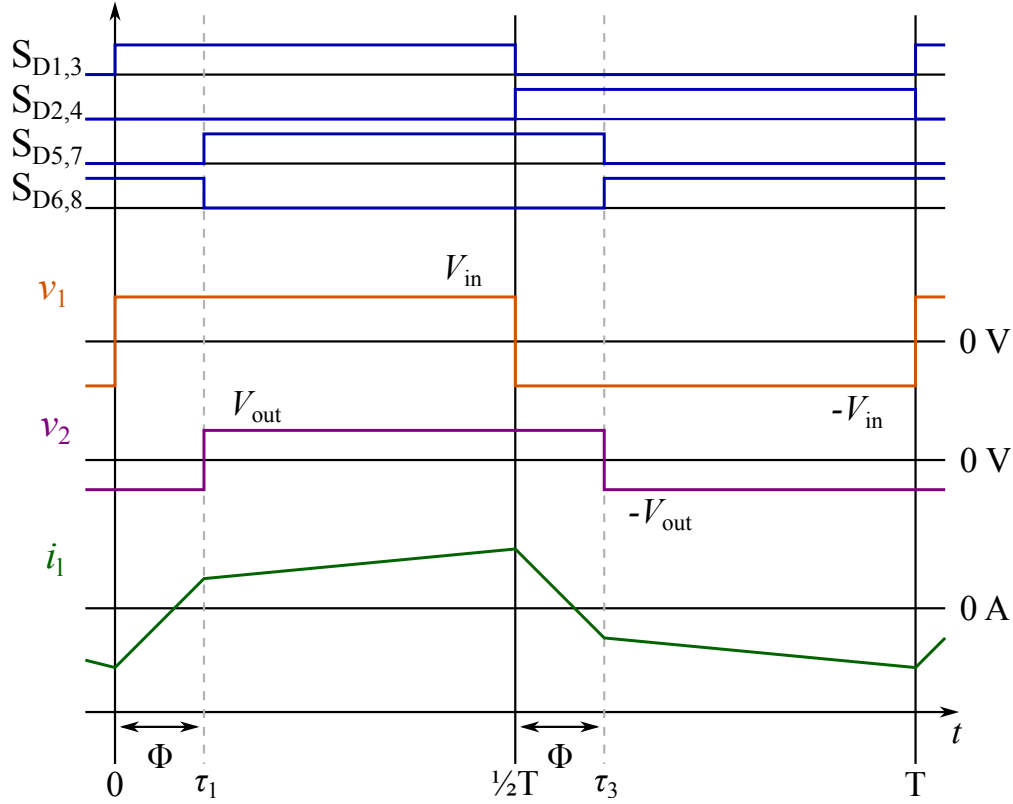


Figure 5.3: Example converter waveforms and switching signals for the DAB converter under single phase-shift (SPS) modulation.

50 % across full-load operating conditions. The bus capacitance, C_{bus} , is sized to ensure a stiff intermediate bus voltage, V_{bus} .

DAB Stage Design

The conventional DAB structure comprises two full-bridge circuits connected via a transformer and energy transfer inductance [100]. When operating under the single phase-shift (SPS) modulation scheme, the output power of the DAB converter is changed by controlling the phase shift between the two bridges. This phase shift, ϕ , dictates how much power flows and which direction it flows in. Associated waveforms for the DAB converter operating under SPS modulation are shown in Fig. 5.3. Voltages v_1 and v_2 are 50 % duty cycle square waves with a frequency of $f_{\text{sw,DAB}}$. The slope of the leakage inductor current, i_l , is set by the magnitude of the voltage across the leakage inductance, L_{lk} , during each time interval of the DAB switching sequence. The magnitude of this voltage is labeled v_L in Fig. 5.2.

If the two bridges are phase-shifted relative to each other across an $N_1 : N_2$ transformer that has leakage inductance, L_{lk} (referred to the primary side), with phase shift, ϕ , the

output power is given by

$$P_{\text{out}} = \frac{V_{\text{in,DAB}} V_{\text{out}}}{2\pi^2 L_{\text{lk}} f_{\text{sw,DAB}}} \cdot \frac{N_1}{N_2} \cdot \phi(\pi - \phi) \quad (5.1)$$

In this work, the DAB stage takes the output of the boost converter stage as its input to provide an output voltage between 30 - 45 V, depending on the desired operating condition. Therefore, the input voltage to the DAB is $V_{\text{in,DAB}} = V_{\text{bus}}$. The leakage inductance, L_{lk} , is sized to be 4 μH for the given operating conditions, such that a maximum output power of 150 W can be achieved.

DAB Planar Transformer Design

Table 5.1: Planar Transformer Parameters

Parameter	Value
Primary Turns	4
Primary Winding Resistance	13 m Ω
Secondary Turns	3
Secondary Winding Resistance	4.9 m Ω
Simulated Leakage Inductance	0.2 μH

The transformer used in the DAB converter provides isolation and voltage conversion, and the intrinsic leakage inductance is a critical mechanism for power flow. In this work, the transformer is realized as a planar magnetic structure to leverage the thermal and manufacturing/implementation benefits that planar magnetics offer over wire-wound structures [101]. Furthermore, by operating the transformer at a high (~ 300 kHz) frequency, the physical volume and mass can be reduced compared to a lower frequency transformer, as described in [102]. The windings of the planar transformer are implemented as copper traces within a printed circuit board (PCB), giving the transformer a reduced size and profile. Furthermore, the designer is able to very precisely dimension and place windings within the PCB structure, which allows for a more repeatable transformer design with regards to magnetizing and leakage inductances. This enables a transformer with good thermal behavior, well-controlled electrical characteristics, and a high magnetic power density [101].

For the DAB converter to operate with an input voltage of 40 - 60 V and an output voltage of 30 - 45 V, the transformer is designed to have a turns ratio, N , that satisfies the constraint $NV_2 = V_1$ to ensure the maximum ZVS range [103]. In this work, this corresponds to $N = \frac{4}{3}$.

Several transformer designs were analyzed in ANSYS PExprt and MATLAB using the loss calculation methodology detailed in [104] to find the best tradeoff between loss, switching

frequency, and practical size of the transformer. The general flow of this methodology [104] is shown in Fig. 5.4 and is adapted for the DAB converter in this work. The inputs to the sweep are: 1) feasible switching frequencies, 2) the different magnetic cores, and 3) the transformer design specifications such as primary- and secondary-side voltages, currents, and number of turns. Each magnetic core geometry is represented in the sweep using empirical data from core manufacturer datasheets. The script iterates through each core and switching frequency to synthesize different transformer designs. Limits on flux density ($B_{pk} > B_{max}$) and current density ($J_{wire} > J_{max}$) are used to constrain the feasible set of designs. Losses are calculated for all feasible designs.

The transformer losses are calculated as a combination of core (P_v) and winding (P_{wind}) loss. Core loss is estimated using the Steinmetz equation. Its general form is shown in Eqn. 5.2 below where P_v is the power loss density, f is the frequency of the sinusoidal excitation, and B_{ac} is the peak magnetic flux density. In this case, f is the switching frequency of the converter. The constants k , α , and β are material-specific and take different values depending on the frequency and flux density for which they are fitted.

$$P_v = k \cdot f^\alpha \cdot B_{ac}^\beta \quad (5.2)$$

Winding loss is calculated for both the primary and secondary windings using the standard equation for conduction loss. The equation for calculating total winding loss is shown in Eqn. 5.3. $R_{wind,pri}$ and $R_{wind,sec}$ are the total primary and secondary winding resistances, respectively. Each of these winding resistances is calculated in terms of the resistance of a single turn which is then scaled to make up the total primary and secondary winding resistances.

$$P_{wind} = I_{rms,pri}^2 \cdot R_{wind,pri} + I_{rms,sec}^2 \cdot R_{wind,sec} \quad (5.3)$$

From the results of this sweep, the TDK EPCOS EILP 22 core was chosen with N87 material for reduced core loss at higher frequencies. The magnetic flux density (B) is plotted in Fig. 5.5 for this core operating at $V_{in} = 40$ V. The saturation flux density of the N87 material is 390 mT at 100°C [105].

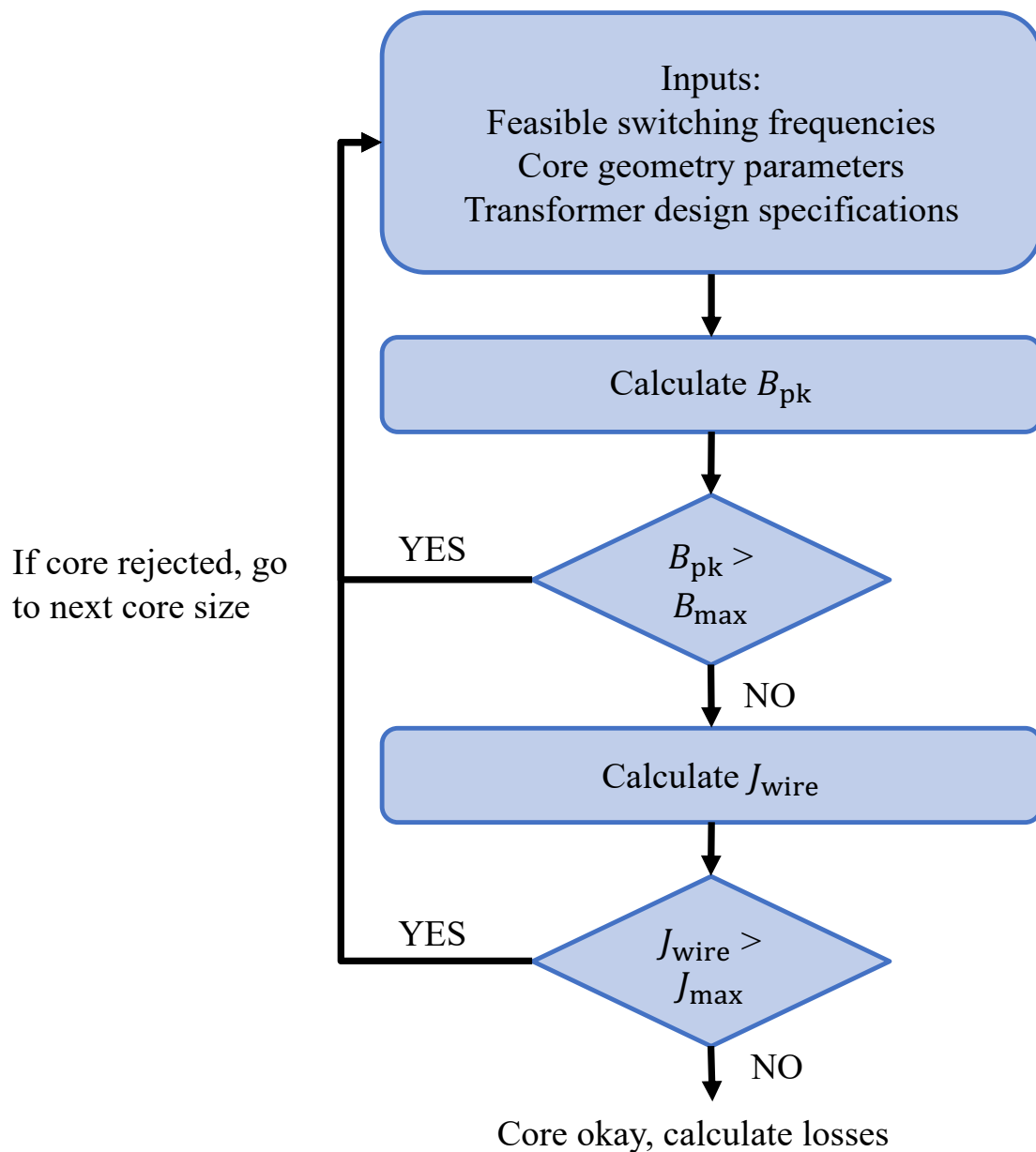


Figure 5.4: Flowchart showing the procedure for selecting a transformer core and analyzing transformer design losses.

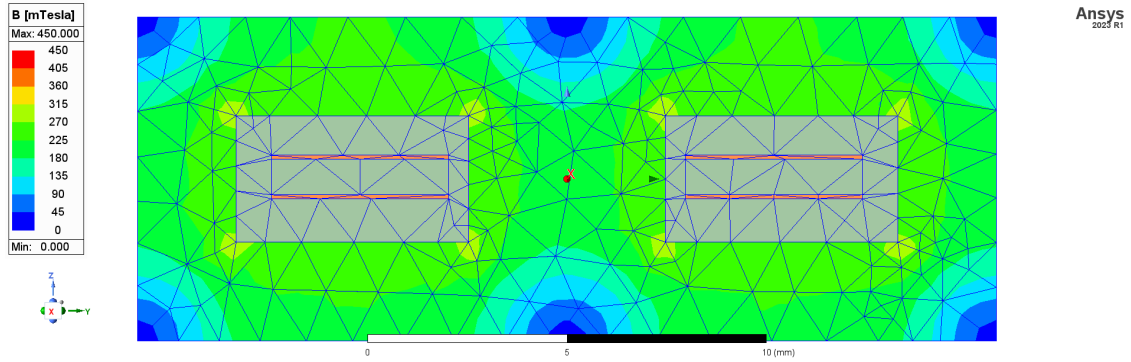


Figure 5.5: ANSYS simulation results showing the B field of an EILP 22 core with N87 material operating at $V_{in} = 40$ V.

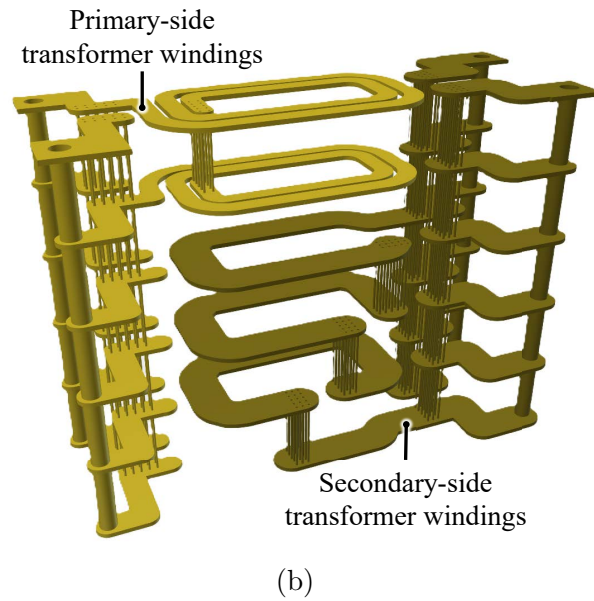
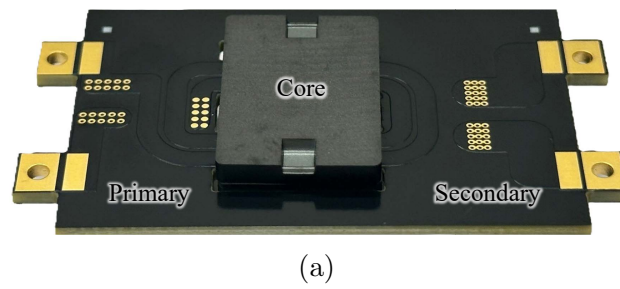


Figure 5.6: (a) Annotated photograph of the planar transformer daughterboard. Dimensions: 50.3 mm x 22.3 mm (b) PCB stackup of copper planar transformer windings.

The transformer is constructed on a PCB daughterboard for ease of prototyping, as shown in Fig. 5.6a. A 6-layer PCB stackup is used for the transformer windings as depicted in Fig. 5.6b. Layers 1 and 2 each contain 2 primary windings, connected in series. Layers 3 - 6 contain 3 series-connected secondary windings. As this is a low-current design, connecting the windings in series across layers allows for design simplicity as the transformer windings are able to fit within the 6 PCB layers that are allocated for the power stage. Both the primary and secondary windings are wound around the center leg, rather than being wound around the two outer legs of the core, to increase the power density of the transformer. This winding configuration reduces the amount of leakage fields, which subsequently lowers the leakage inductance. This necessitates the use of external inductors to increase the leakage inductance and more precisely control the power flow from input to output. An external inductor of $1.8 \mu\text{H}$ is symmetrically added at both the positive and negative terminals of the primary winding to supplement the intrinsic $0.2 \mu\text{H}$ leakage inductance and achieve the required total of $4 \mu\text{H}$.

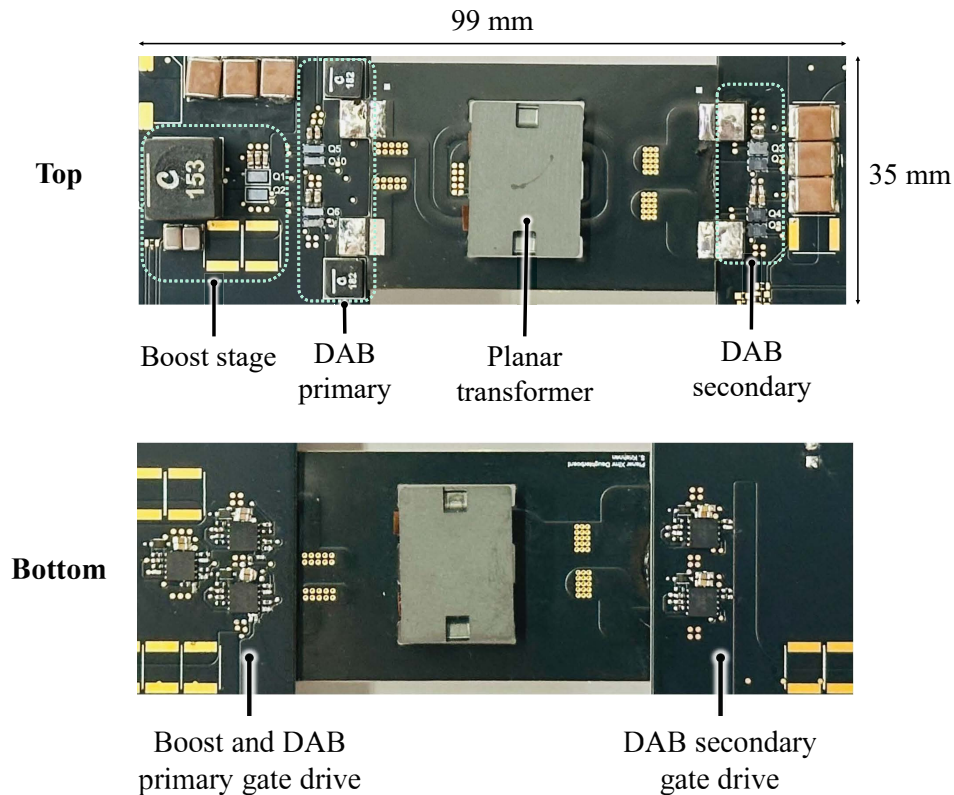


Figure 5.7: Photograph of hardware prototype.

5.4 Hardware Prototype and Experimental Results

A hardware prototype was constructed to verify converter operation and to assess its performance for future system-level implementation. The prototype is shown in Fig. 5.7, and the power stage of the experimental prototype measures $99.2 \text{ mm} \times 34.6 \text{ mm} \times 10 \text{ mm}$ with the boost inductor being the tallest component on the board, further highlighting the benefit of the low-profile planar transformer.

The hardware prototype utilizes GaN switches that are sized with a safety factor of 2 in order to account for the combined impact of voltage derating and radiation conditions imposed by the environmental conditions in space [106]. For devices with similar on-resistances ($R_{ds,on}$), GaN HEMTs have lower output capacitances (C_{oss}) compared to Silicon (Si) MOSFETs, making them an attractive option for high-efficiency, soft-switched power converters [107]. Furthermore, GaN switches, which have low gate-charge requirements and better parasitic profiles, enable faster switching frequencies than their Si MOSFET counterparts [108]. This is beneficial in reducing the overall size and weight of the power stage.

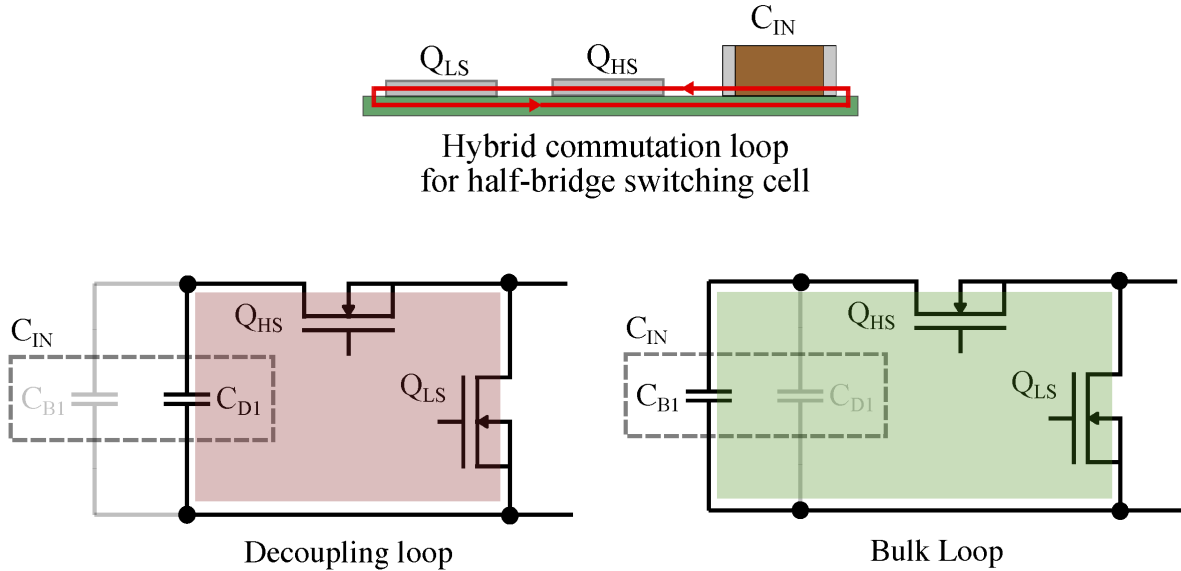


Figure 5.8: Hybrid commutation loop for half-bridge switching cell with decoupling and bulk loops shown.

To enable the fast switching speeds that the GaN HEMTs are capable of, careful PCB layout implementing a hybrid commutation loop and capacitive decoupling was used to manage parasitic inductances as shown in Fig. 5.8 [109]. In the gate drive circuitry for each stage, the automotive-qualified LM5113-Q1 half-bridge GaN driver from Texas Instruments is

used. The component listing for the GaN switches, gate-driving components, and magnetics is provided in Table 5.2. The operating parameters for this prototype are defined in Table 5.3.

Table 5.3: Converter Operating Parameters

Parameter	Value
V_{in}	18 - 36 V
V_{out}	30 - 45 V
$P_{out,max}$	150 W
$f_{sw,boost}$	700 kHz
$f_{sw,DAB}$	250 kHz
N	4:3 turns

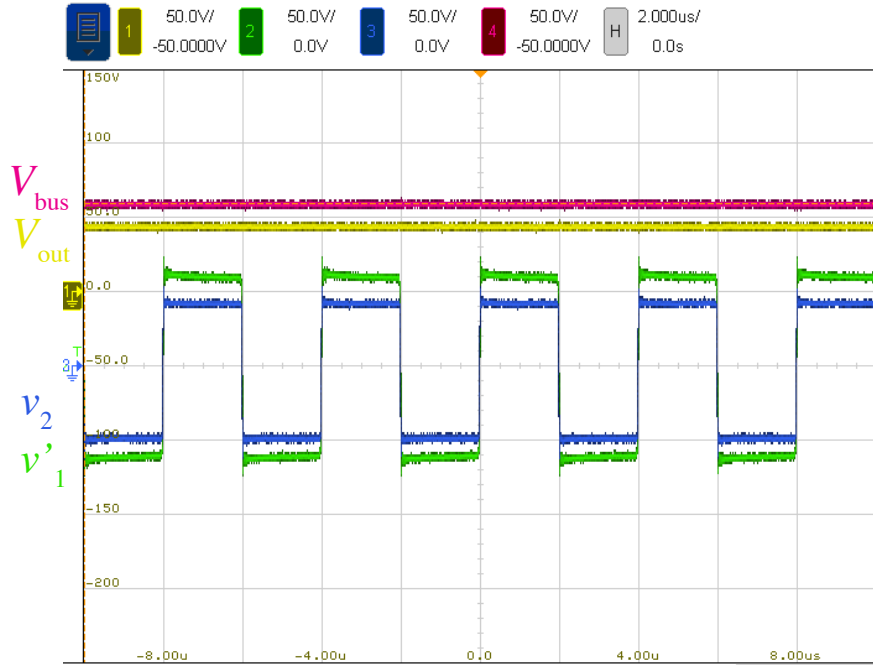


Figure 5.9: Measured waveforms of the intermediate bus voltage (V_{bus}), primary-side voltage measured after the leakage inductance (v_1'), secondary-side voltage (v_2), and output voltage (V_{out}) of the DAB stage for the conversion of $V_{in} = 24$ V to an intermediate bus voltage of $V_{bus} = 60$ V down to $V_{out} = 45$ V.

Table 5.2: Component Listing of the Hardware Prototype

Component	Mfr. & Part Number	Parameters
Boost Converter Stage		
Switches S_1, S_2	EPC EPC2059	GaN, 170 V, 9 m Ω
Inductor L	Coilcraft XAL1010-153MED	15 μ H, 15.5 A I_{sat}
Bus Capacitance C_{bus}	TDK CGA9P3X7S2A156M250KB	45 μ F, 100 V
Dual Active Bridge Converter Stage		
Primary Side Switches $S_3 - S_6$	EPC EPC2207	GaN, 200 V, 22 m Ω
Secondary Side Switches $S_7 - S_{10}$	EPC EPC2619	GaN, 100 V, 4.2 m Ω
Leakage Inductor L_{lk}	Coilcraft XGL5030-182	1.8 μ H, 10.6 A I_{sat}
Gate Drive and Digital Isolator		
GaN Driver	Texas Instruments LM5113QDPPRRQ1	90 V, high and low-side
Bootstrap Diodes	Nexperia BAT46WJ,115	Schottky, 100 V, 250 mA
Digital Isolator	Analog Devices Inc. MAX14850ASE+	6-channel, uni- & bi-directional
Planar Transformer		
E Core	EPCOS/TDK B66285G0000X187	ELP22/6/16, N87 Material
I Core	EPCOS/TDK B66285K0000X187	I22/2.5/16, N87 Material
Controller Board		
Microcontroller	Texas Instruments TMDSCNCD28379D	C2000

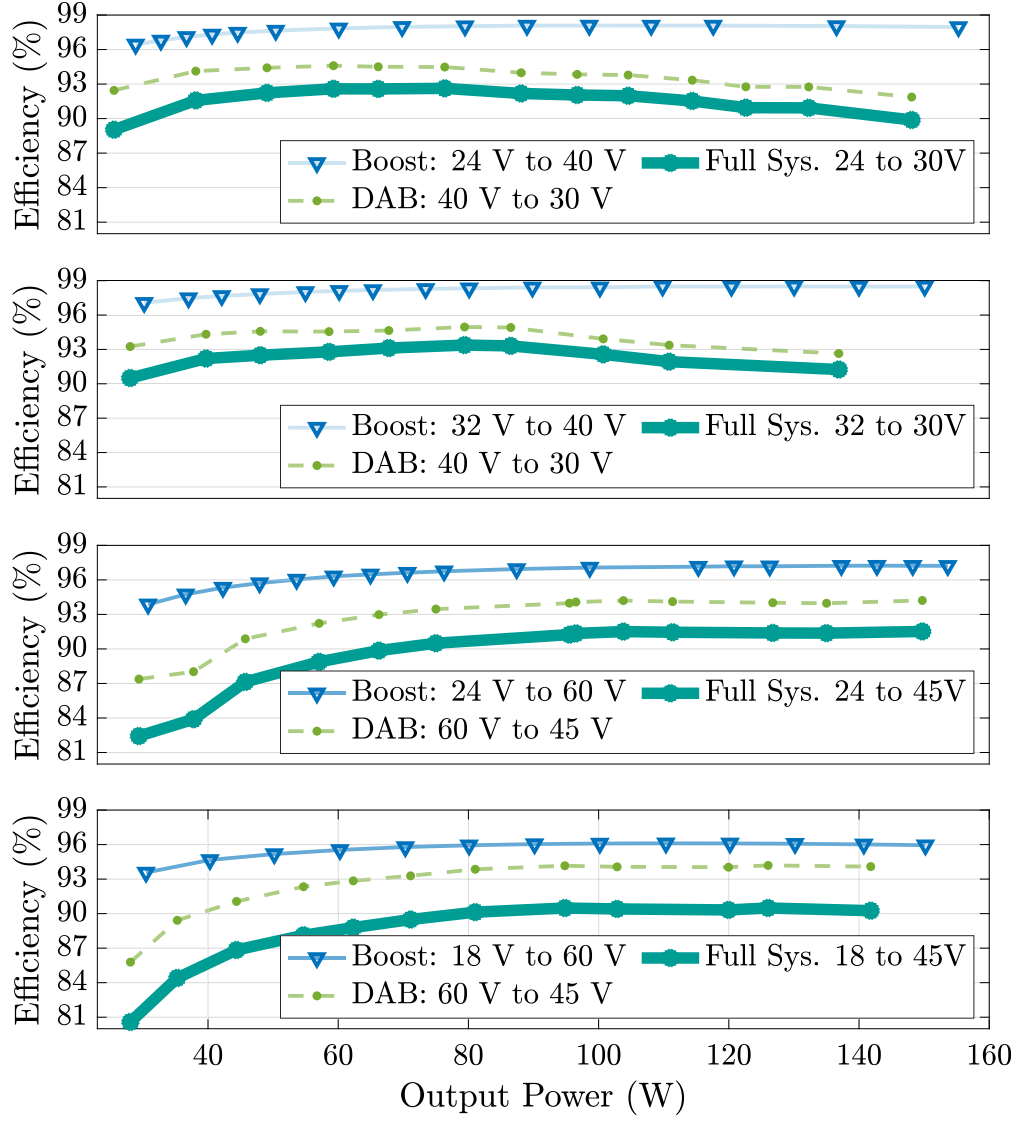


Figure 5.10: Measured efficiency results for the converter operating from 24 V to 30 V, 32 V to 30 V, 24 V to 45 V, and 18 V to 45 V.

Fig. 5.9 shows measured converter waveforms for the output of the boost converter as well as both the primary and secondary bridges of the DAB converter while it converts an input voltage of 24 V to a dc output of 45 V. Fig. 5.10 shows the full converter efficiencies, measured on a high-precision PA2201A IntegraVision Power Analyzer with fan cooling only. For the nominal condition, an input voltage of $V_{in} = 24$ V is used to supply the boost stage, and measurements are taken for both $V_{out} = 30$ V and $V_{out} = 45$ V at the output of the DAB stage to best capture the range of feasible efficiencies at this nominal input voltage. For the 24 V to 30 V operating condition, the full converter achieves a peak efficiency of

92.6% and a full-load efficiency of 89.9%. For the 24 V to 45 V operating condition, the full converter achieves a peak efficiency of 91.5% and a full-load efficiency of 91.5%. For both conversion ratios, the boost converter is more efficient than the DAB converter, achieving peak efficiencies of 98.1% and 97.2%. At full load, the volumetric power density of the converter is 4.1 kW/L.

Fig. 5.10 also shows measured efficiencies for input voltages that are both higher and lower than the nominal (i.e. $V_{in} = 18$ V and $V_{in} = 32$ V). These plots show the “buck-boost” capability of this converter and the boost front-end stage’s ability to operate successfully at extreme conversion ratios while maintaining high efficiencies. It is seen that across operating points, this converter can outperform the conventional flyback converter with minimal physical design and timing complexity.

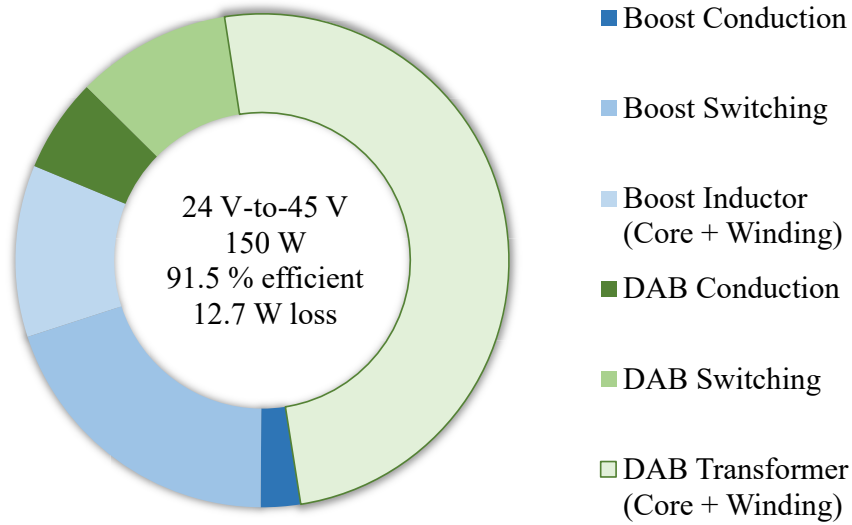


Figure 5.11: Power loss breakdown for full-load (150 W), 24 V to 45 V operation of the cascaded converter hardware prototype.

An estimated loss breakdown for the hardware prototype operating at a full-load of 150 W for the nominal 24 V to 45 V conversion is shown in Fig. 5.11. At this output power condition, the cascaded converter is 91.5% efficient with 12.7 W of loss. The loss at this full-load condition is comprised of 4.3 W of loss from the boost converter stage, and 8.4 W of loss from the DAB converter stage. Switching loss is the dominant loss mechanism in the boost converter stage as the GaN HEMTs are operated at higher switching frequencies. This can be seen from the efficiency curves in Fig. 5.10 as the switching losses continue to dominate even at higher loads. In the DAB converter stage, the transformer core loss dominates. The transformer contributes approximately 6.4 W of core and winding loss toward the total DAB converter stage loss (8.4 W). This prototype showcases that high efficiencies are feasible even at high switching frequencies.

5.5 Conclusion and Future Work

The advent of small, lightweight satellite technology creates opportunities for advancements in high-efficiency, high-power-density power converters for space applications. However, designing power electronics for space requires the use of robust radiation-tolerant components that can make it challenging to achieve competitive power densities and efficiencies, especially in scenarios where galvanic isolation is required. This work discusses the design and construction of an isolated, cascaded two-stage power converter for low-voltage space systems that is able to achieve efficiencies over 89 % at a full load of 150 W, making it an attractive alternative to the conventional flyback converter.

The design of novel power converter topologies for space applications is a burgeoning area in power electronics research. However, radiation effects in space can make it challenging to adopt these higher-performance topologies. Furthermore, the flyback remains an attractive option for power conversion in space because of its relatively simple architecture and low component count which can reduce cost. Other topologies, including the boost-DAB architecture presented in this chapter, have higher component counts and some increased control complexity. Further investigation into how the more complex power converter architectures can be qualified for space is required. For example, future research could address challenges related to mechanical stress, reliability, and form factor for these more complex topologies to make them more compelling for use in aerospace applications.

Chapter 6

A High-Performance Flying Capacitor Multilevel DAB DC-DC Converter for Isolated 800 V Automotive Systems

Portions of this chapter are adapted in whole or in part from [110]. The major practical considerations explored in this chapter are isolation and output voltage regulation.

In the previous chapter, we addressed isolation in the context of signal integrity for power converters. This chapter of the dissertation looks at using isolation for human safety within a dc-dc power converter in transportation applications. Moving to higher voltages on-board a vehicle forces isolation to become a more critical design consideration [111]. This isolation is crucial to ensuring the safety of both vehicle users and technicians. For example, the 48 V systems on-board a vehicle can be serviced without additional protection as long as there is isolation from the high-voltage side.

6.1 Introduction

As electric vehicle (EV) adoption becomes more widespread, there is an increased need for higher performance power electronics to serve these complex and dynamic electrical systems. Legacy architectures are also changing as 800 V and 48 V voltage rails replace the more common 400 V and 12 V buses in hybridized and fully electric vehicles. Moving to higher voltages at each of these buses reduces system-level conduction losses in cabling while enabling higher power capability [112]. One increasingly prevalent challenge for EVs is stepping down the high voltage bus (400/800 V) to the appropriate intermediate voltage, e.g. 48 V. Fig. 6.1 shows a potential use case of the dc-dc power converter discussed in this chapter, on-board an electric vehicle.

The power converters performing this work must be efficient, lightweight, and compact, while providing isolation to meet safety standards. Recently, similar high-voltage dc bus

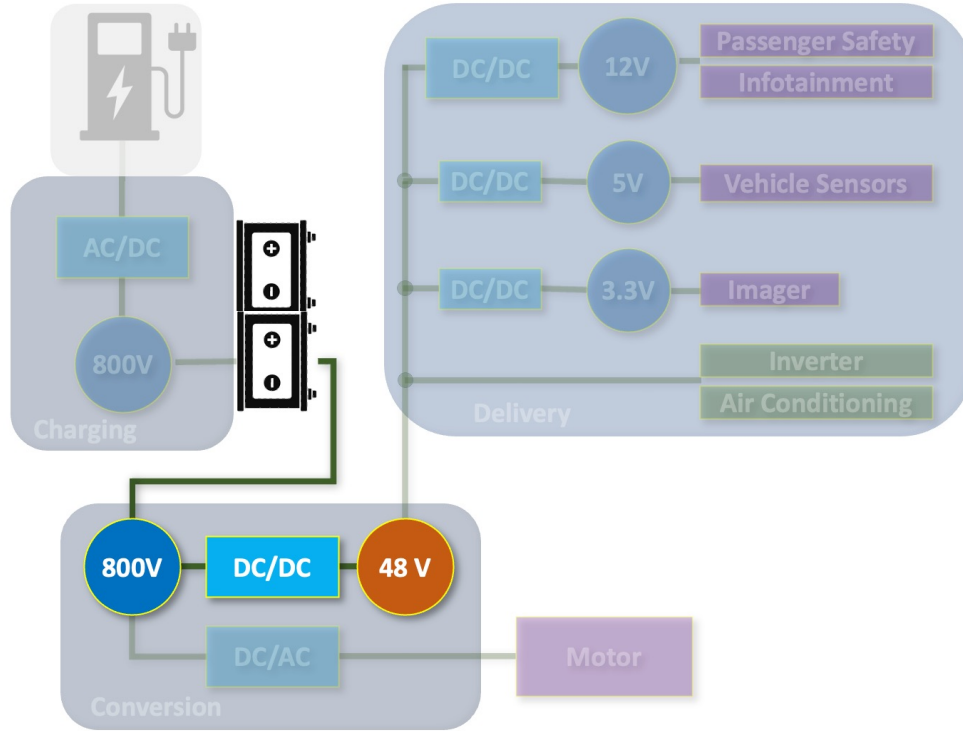


Figure 6.1: Diagram of an electric vehicle power delivery architecture, highlighting a potential use case of the 800 V power converter presented in this chapter.

systems have also been proposed for data center applications, where 800 V dc architectures are emerging at the rack-level [113].

The 800 V isolated converter design space is a promising new area of exploration with many recent designs innovating on topological performance and power density [114–117]. A survey of 800 V isolated, dc-dc power converters was conducted, and a comparison of this work to the surveyed academic works is provided in Table 6.2.

This work presents a single-stage converter topology derived from a dual active bridge (DAB) converter [100]. A conventional DAB converter comprises an H-bridge inverter that generates a square wave as an input to a transformer, and a rectifier that converts the output of the transformer to a dc voltage. The DAB converter is an attractive topology in automotive applications, characterized by soft-switching and regulation capabilities as well as bi-directionality. However, for the DAB topology, the switches in the primary-side inverter stage must be rated to block the full input voltage. For high dc voltages such as the emerging 800 V bus, this results in the use of large, low figure-of-merit (FOM) devices [121]. In the proposed topology, a flying capacitor multilevel (FCML) inverter stage is utilized [122]. The FCML topology has been shown to achieve high efficiencies and power densities through the use of high FOM switching devices, and by using energy-dense capacitors to perform much

Figure 6.2: Survey of 800 V isolated power converters.

Work	Max Conversion Ratio	Power* [W]	Peak Efficiency [%]	Topology
This Work	800-to-53.3 V	700	96.4 (@ 800Vin)	FC-DAB
[118]	800-to-100 V	1000	Not reported	Stacked-bridge DAB
[116]	840-to-12 V	2000	96.6 (@ 630Vin)	DAB + interleaved PWM converter
[16]	800-to-48 V	1200	96.3 (@ 800Vin)	PSFB-based converter
[119]	800-to-14 V	3600	95 (@ 560Vin)	Two-stage 3-level buck + 2x LLC converters
[120]	800-to-14 V	1200	93 (@ 460Vin)	Interleaved input series half-bridge converter with integrated transformer

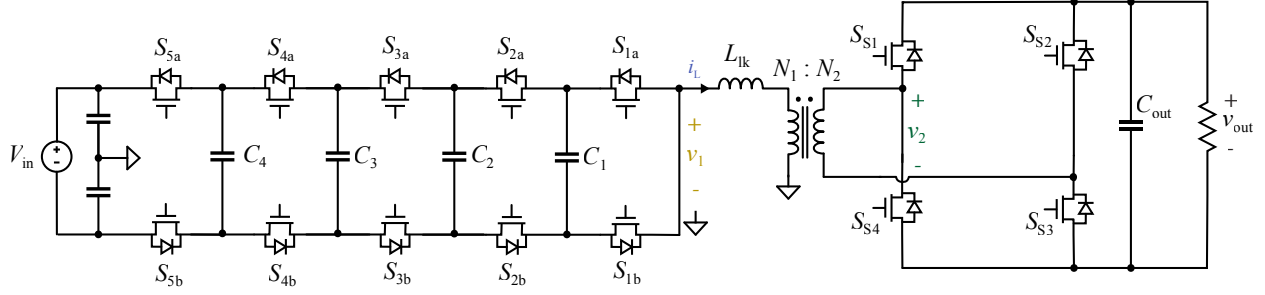
*Output power at maximum conversion ratio.

of the required energy storage and transfer [6].

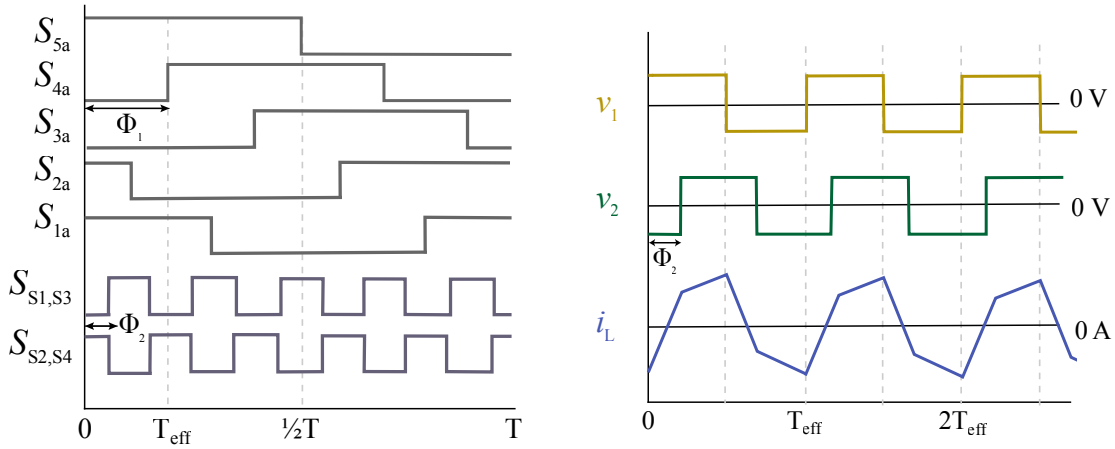
We position the work presented here in the field of galvanically isolated, high-step-down, 800 V converters. In this work, the implementation of a flying capacitor multilevel dual active bridge (FC-DAB) converter for an 800 V input aims to innovate on the design of the power stage while maintaining the high performance required of automotive converters. The FC-DAB topology is a natural extension of the conventional DAB converter with minimal increase in control complexity, leveraging intrinsic strengths of both the FCML and DAB converters at a high step-down ratio.

This work differs from previous variations on the DAB converter that have been proposed. For example, stacked active bridge converters [123, 124] utilize a larger number of lower-voltage switching devices on either the inverter or the rectifier side to achieve high-efficiency, high-voltage conversion, but may require more complex magnetics structures and design. Lower level count switched-capacitor-based DABs have also been proposed [125–127], but these works have mostly focused on flying capacitor voltage balancing as well as control/modulation schemes. The benefits of multilevel switched-capacitor topologies can increase with a higher number of levels. Therefore, it is worthwhile to investigate the resulting challenges and tradeoffs when using switched-capacitor stages in isolated topologies within automotive applications.

The design and implementation of the FC-DAB converter is presented in the following sections. Section 6.2 presents the converter topology, operation and design. Section 6.3 provides details on the hardware prototype as well as operating waveforms and efficiency results for the prototype, demonstrating its high step-down capability. Furthermore, this chapter builds on the FC-DAB converter design presented in a prior conference paper [110] and provides additional analysis, hardware results, and insight into closed-loop control techniques.



(a) Schematic of the FC-DAB topology utilizing a 6-level FCML stage on the primary side.



(b) Ideal switching signals and converter waveforms for the FC-DAB converter under a control scheme based on single-phase shift (SPS) modulation.

Figure 6.3: FC-DAB topology and operating waveforms.

6.2 Topology and Design Considerations

The circuit schematic for the FC-DAB converter presented here is shown in Fig. 6.3a. In this topology, the FCML stage generates a square wave at v_1 , which is translated across a transformer and converted to a dc output voltage by a full-bridge rectifier. The FC-DAB converter utilizes a single split-bus FCML stage in lieu of a full bridge on the primary side. The split-bus configuration enables the FCML stage to generate an ac output voltage [128].

The FCML and Considerations for Use in an Isolated Topology

Fig. 6.4 shows a 6-level split-bus FCML converter with the nominal blocking voltages of the flying capacitors labeled. A general N -level FCML converter contains $(N - 1)$ switch pairs and $(N - 2)$ flying capacitors. Each of the switches in the FCML must nominally block

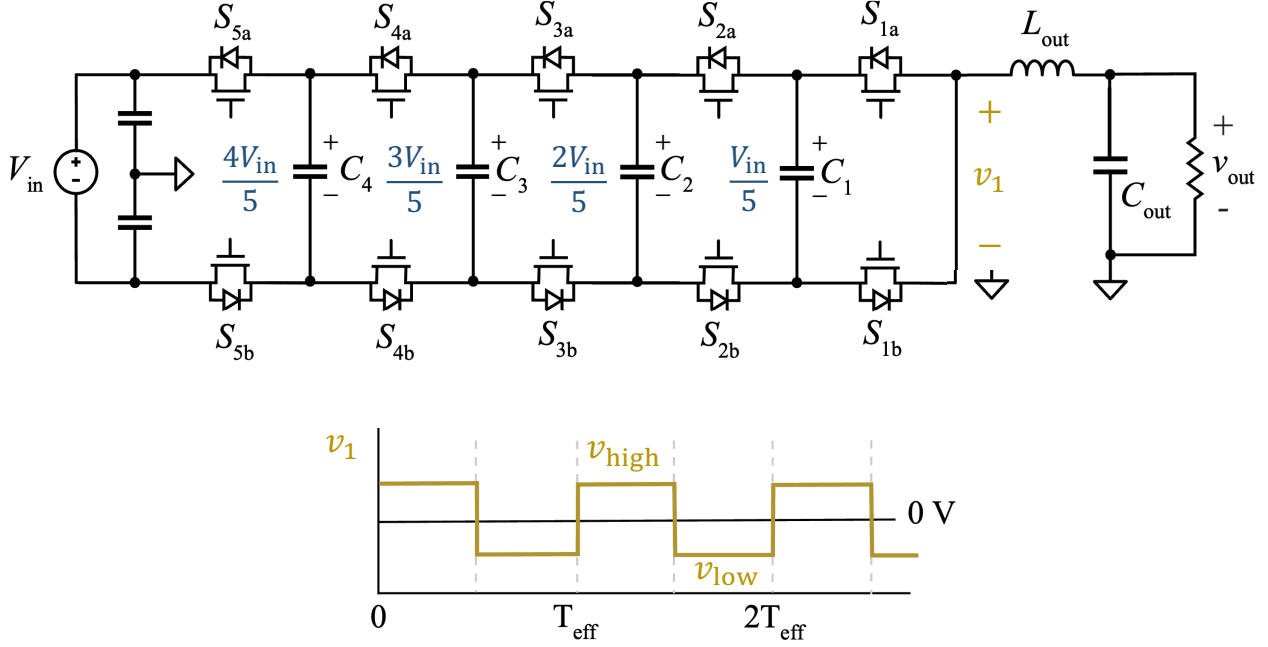


Figure 6.4: Schematic of an $N = 6$ level FCML converter with a split-bus input.

$$V_{q,\text{blk,nom}} = \frac{V_{\text{in}}}{(N-1)}, \quad (6.1)$$

enabling the use of lower-voltage-rated, higher FOM switches [121]. The flying capacitors sustain dc voltage offsets that are fractions of the input voltage ranging from $\frac{V_{\text{in}}}{(N-1)}$ to $\frac{(N-2)V_{\text{in}}}{(N-1)}$.

The FCML converter can be operated using a circularly symmetric phase-shifted pulse-width modulation (PS-PWM) control scheme [122,129]. In this scheme, the pairs of switches are phase shifted relative to each other by $\frac{360^\circ}{(N-1)}$. This phase shift corresponds to ϕ_1 in Fig. 6.3b. This same figure shows example PS-PWM switching signals for switches $S_{1a} - S_{5a}$ of the 6-level FCML. $S_{1b} - S_{5b}$ are switched complementary to their “a” counterparts. With this modulation scheme, the switch node sees an effective switching frequency,

$$f_{\text{eff}} = (N-1)f_{\text{sw}}, \quad (6.2)$$

and effective switching period,

$$T_{\text{eff}} = \frac{1}{N-1}T_{\text{sw}}. \quad (6.3)$$

Each switch in the FCML stage is controlled with duty cycle D . The effective duty cycle D_{eff} at the switch node is then given by

$$D_{\text{eff}} = D(N - 1) - \text{floor}(D(N - 1)). \quad (6.4)$$

We use the PS-PWM scheme to control the FCML stage in the FC-DAB converter to generate a $D_{\text{eff}} = 0.5$ square wave at its switch node (voltage v_1 in Fig. 6.4). Using Eqn 6.4, we find that a duty cycle $D = 0.5$ achieves this.

Furthermore, the split-bus FCML switch node, v_1 , alternates between

$$v_{\text{high}} = \frac{V_{\text{in}}}{2} - \frac{k}{N - 1} V_{\text{in}} \quad (6.5)$$

and

$$v_{\text{low}} = \frac{V_{\text{in}}}{2} - \frac{k + 1}{N - 1} V_{\text{in}} \quad (6.6)$$

where $k = \text{floor}(D(N - 1))$, $k = [0, 1, 2 \dots N - 2]$. The amplitude of v_1 in Fig. 6.3b is given by $V_{\text{in}}/(2(N - 1))$. From Eqns. 6.5 and 6.6, odd-level count FCML designs are not feasible in order to generate a square wave at v_1 .

In a conventional FCML converter, using the PS-PWM modulation scheme leads to the miniaturization of the filter inductance by a factor of $(N - 1)^2$ through reduced volt-seconds across the inductor. For the FC-DAB converter, the benefits of the associated frequency multiplication are largely extended to the divided switch-node voltage amplitude, enabling a reduction in transformer turns ratio.

A 6-level FCML stage is selected for the primary side of the FC-DAB in this work to enable the use of 200 V GaN devices, which have a much higher FOM than higher voltage switches [130]. The secondary side of the FC-DAB is an H-bridge rectifier that operates at $f_{\text{rect}} = f_{\text{eff}} = (N - 1)f_{\text{sw}}$. The rectifier-side voltage v_2 is phase shifted from v_1 by ϕ_2 to control power flow to the output of the converter, as shown in Fig. 6.3b. As in a conventional DAB converter, the leakage inductance in the transformer defines the power-handling capability of the FC-DAB converter. Power flow between the primary-side FCML stage and the secondary-side rectifier is controlled by the phase shift ϕ_2 between the control signals for S_{5a} and S_{S1} , as shown in Fig. 6.3b. This figure shows ideal waveforms assuming that flying capacitors $C_1 - C_4$ are large with no ripple.

Using a control scheme that is modeled after single-phase shift (SPS) modulation [131] for conventional DAB converters, the output power for the FC-DAB converter can be expressed as

$$P_{\text{out}} = \frac{v_1 v_2}{2\pi^2 L_{\text{lk}} f_{\text{eff}}} \cdot \frac{N_1}{N_2} \cdot \phi_2 (\pi - \phi_2) \quad (6.7)$$

where the effective switching frequency $f_{\text{eff}} = (N - 1)f_{\text{sw}}$, and the transformer has an $N_1 : N_2$ turns ratio, with leakage inductance L_{lk} (referred to the primary side). By substituting $v_1 = V_{\text{in}}/(2(N - 1))$ and $v_2 = V_{\text{out}}$ into Eqn. 6.7, we arrive at

$$P_{\text{out}} = \frac{\frac{V_{\text{in}}}{2(N-1)} V_{\text{out}}}{2\pi^2 L_{\text{lk}} f_{\text{eff}}} \cdot \frac{N_1}{N_2} \cdot \phi_2(\pi - \phi_2). \quad (6.8)$$

Eqn. 6.8 modifies the standard SPS output power relationship [131] by reducing V_{in} by a factor of $2(N-1)$ and increasing the switching frequency f_{sw} by a factor of $(N-1)$. While this work controls the FC-DAB converter using SPS modulation, other modulation techniques applicable to the DAB converter – such as dual-phase shift (DPS) modulation [132] – may be extended to the FC-DAB converter as well.

FCML Stage Level Count Selection

For this high step-down ratio converter, the level count (N) of the FCML stage constrains the maximum achievable power flow through the FC-DAB converter for given operating conditions V_{in} , V_{out} , f_{sw} , and design parameters L_{lk} and $N_1 : N_2$. This is because, from Eqn. 6.8, the achievable output power is now set by $V_{\text{in}}/(2(N-1))$, the amplitude of the FCML switch node, rather than V_{in} as in the conventional DAB converter. Therefore, an optimal level count needs to be selected for the primary-side FCML design based on parameters such as switching frequency, flying capacitor voltage ripple, and the best available switches. Switch parameters such as voltage rating, on-resistance ($R_{\text{ds,on}}$), and switch output capacitance (C_{oss}) are considered here.

Using a variation on the methodology presented in [133, 134], a detailed loss analysis is performed for the FCML stage with consideration given to the effects of transformer loss on system-level design efficiency and volume. The framework includes flying capacitor voltage ripple and volume, as well as reasonable considerations for semiconductor device loss limits. This analysis specifically considers the impact of the following parameters on the converter design:

- **Input voltage (V_{in}):** This is the supply voltage at the input of the converter on the primary side.
- **FCML stage level count (N):** This variable quantifies the number of levels on the primary side of the FC-DAB converter. Only even-level count ($N = 2, 4, 6, \dots$) FCML stage designs are considered in this sweep, as these level counts enable the generation of a 50% duty cycle voltage waveform centered around zero at the primary-side switching node in a split-bus FCML stage. Eqns 6.5 and 6.6 show that this is not possible using odd-level count FCML stages. Even-level count FCML stages also exhibit improved natural flying capacitor balancing compared to their odd-level counterparts [135].
- **Flying capacitor voltage ripple (α):** Each flying capacitor in the FCML converter has a nominal dc voltage offset with a ripple component. The ripple component has a peak-to-peak magnitude $2\Delta v_c$. Therefore, the nominal flying capacitor voltage can be written as

$$v_{c,k} = V_{c,k} \pm \Delta v_c \quad (6.9)$$

where $k = [0, 1, 2 \dots N - 2]$.

The peak flying capacitor voltage ripple (Δv_c) is then defined as a percentage (α) of the nominal switch blocking voltage (Eqn. 6.10).

$$\Delta v_c = \alpha \cdot \frac{V_{in}}{(N - 1)} \quad (6.10)$$

Thus, each FCML switch then needs to be rated to block $V_{q,blk}$ (Eqn. 6.11).

$$V_{q,blk} = \frac{V_{in}}{(N - 1)} + 2 \cdot \Delta v_c \quad (6.11)$$

For the FCML stage in the FC-DAB converter, the flying capacitor voltage ripple is restricted to maintain as close to a nominal square wave as possible on the switch node. The tradeoff here is that each flying capacitor value will be larger, but the switches in the FCML stage do not have to be overrated by a substantial factor to accommodate large flying capacitor ripple.

- **Switching frequency (f_{sw}):** Each device on the primary side of the FC-DAB converter will operate at this switching frequency.
- **Type of flying capacitance:** The designer either chooses “Identical” or “Optimal” capacitance. “Identical” capacitance indicates that the same commercial component is used for each flying capacitor. “Optimal” capacitance corresponds to using a minimum-sized combination of commercial components for each flying capacitor’s unique blocking voltage. “Identical” capacitance simplifies layout and assembly while “Optimal” capacitance optimizes for converter volume.
- **Transformer loss (γ):** The transformer loss is represented as a combination of core and winding loss and is included in the optimization sweep as a fraction of the total power converter loss [136]. As the allowable transformer loss increases, the reduced transformer volume enables higher power density.

Table 6.1 summarizes and lists the parameters and values used in this particular sweep for the FC-DAB design.

The 2-level ($N = 2$) primary-side design is also included in this sweep to compare against the FCML stage designs. The assumptions made in this sweep to compare 2-level vs. FCML designs are as follows. The FCML converter designs use GaN HEMTs while the 2-level design uses SiC FETs that support the full input voltage. The GaN HEMTs used in the FCML stage design sweeps span Infineon 650 V GaN devices (originally developed by GaN Systems) and EPC devices with drain-to-source voltages (V_{ds}) between 100 V and 200 V. The

Table 6.1: FC-DAB Design Optimization Parameters

Parameter	Value	Description
V_{in}	800 V	Input voltage
N	[2, 4, 6, 8, 10]	Number of levels on primary side
α	0.1	Peak ripple percentage of nominal blocking voltage
f_{sw}	[20, 40, 60, 80, 100] kHz	Operating frequency of each switch
Flying capacitor type	[1, 2]	1: Identical capacitors, 2: Optimal capacitors
γ	$[0.25, 0.5, 0.75, 1] \times 10^{-2}$	Ratio of transformer loss to the total output power

SiC FET used in the 2-level analysis is a state-of-the-art On Semi Power N-Channel JFET with $R_{ds,on} = 72 \text{ m}\Omega$ and $C_{oss} = 35 \text{ pF}$ at $V_{in} = 800 \text{ V}$. Both SiC and GaN are state-of-the-art wide-bandgap device technologies in their respective voltage classes. Fig. 6.5 shows a comparison of example device packages available at discrete V_{ds} levels. When making this comparison, FETs used in both the 2-level and FCML primary-side designs are switched at the same f_{sw} .



Figure 6.5: Example device packages across manufacturers for discrete voltage levels.

A full parametric sweep was conducted using the parameters in Table 6.1, and the results are shown in Figs. 6.6 and 6.7. Each possible design is plotted as a point in Figs. 6.6 and 6.7 along with predicted peak efficiency and maximum power density. These two figures highlight variation in the level count (N) and switching frequency (f_{sw}) with different shapes/ colors to provide insight into how converter efficiency and power density are affected by these two parameters.

As demonstrated in Fig. 6.6, FCML designs are shown to be more optimal than the 2-level designs on the primary side of the FC-DAB converter. Within the FCML design space, maximum power density is predicted for 6-level designs. Below this, the available switches

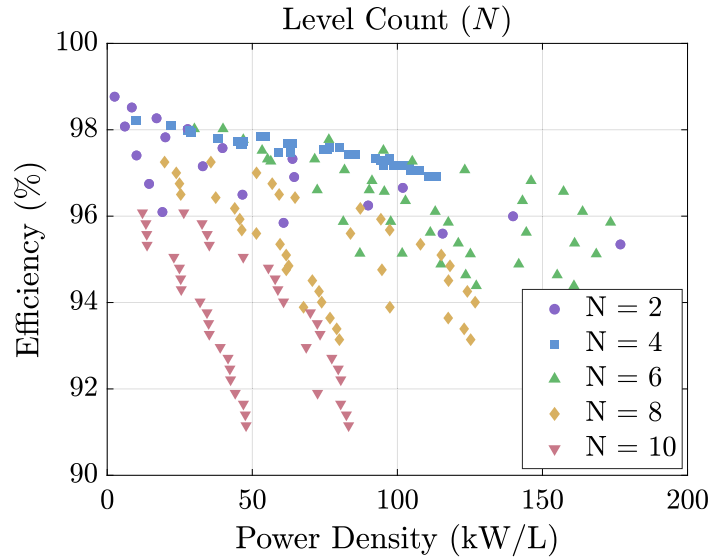


Figure 6.6: Peak efficiency vs. power density for varying level counts (N) on the primary side of the FC-DAB converter.

limit performance, while higher level counts limit output power as shown in Eqn. 6.8.

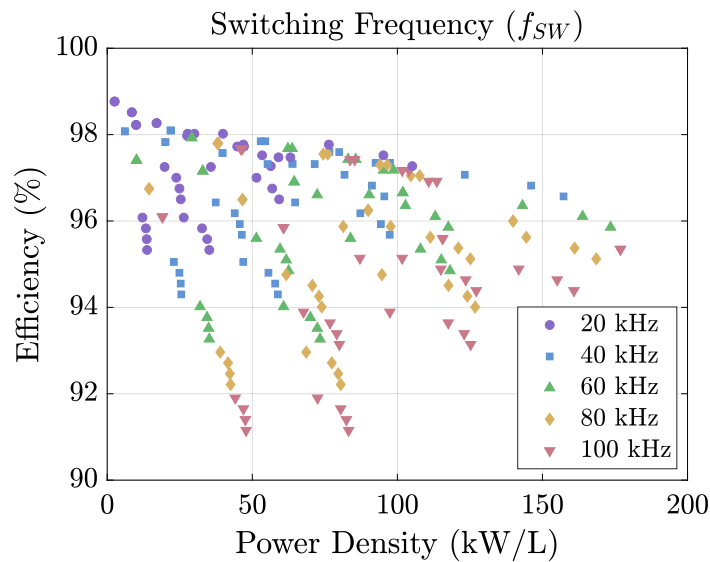


Figure 6.7: Peak efficiency vs. power density for varying switching frequency (f_{sw}) on the primary side of the FC-DAB converter.

Planar Transformer Design

A planar transformer is used to provide galvanic isolation, and to enable power transfer across the intrinsic leakage inductance of the converter. The planar structure lends itself to a reduced profile, while the planar PCB structure provides inherent thermal relief [101].

In the FC-DAB topology, the ability of the FCML stage to perform an initial voltage step-down means that the primary-side windings of the transformer see a voltage of just $\pm V_{\text{in}}/(2(N-1))$. Thus, compared to a conventional DAB converter, the transformer in the FC-DAB converter has reduced voltage (but increased current) on the primary side, and the same low-voltage, high-current on the secondary side. The more symmetric (i.e. lower transformer step-down ratio) planar transformer design enabled by the FC-DAB converter can be advantageous in controlling transformer parasitics and in enabling a converter with a smaller form factor. Designing a more symmetric transformer helps to avoid many of the challenges that come with higher frequency, high-step-down PCB-based planar transformers. These challenges include greatly increased leakage inductance, and higher ac resistance on the high-voltage side due to an increased number of turns [137]. Furthermore, applying a lower voltage to the primary side of the transformer also allows for a reduction in the primary-side volt-seconds. This is in comparison to a conventional DAB with a full-bridge structure on the primary side. Reducing the volt-seconds enables a reduction in the peak flux density, B_{pk} .

The equation for B_{pk} is as follows, where λ represents the applied volt-seconds on the ideal transformer and A_c represents the core area. The turns ratio is defined as $N_{\text{turns}} : 1$, where N_{turns} is equal to $\frac{N_1}{N_2} = \frac{v_1}{v_2}$.

$$B_{\text{pk}} = \frac{\lambda}{N_{\text{turns}} A_c} \quad (6.12)$$

λ can be re-written in terms of the primary-side voltage, v_1 , and the effective switching period, T_{eff} , as

$$\lambda = \int v_1 dt = \frac{v_1 T_{\text{eff}}}{2}. \quad (6.13)$$

Table 6.2: Magnetic Parameter Comparison between DAB and FC-DAB

Topology	v_1	$ i_1 $	T_{eff}	B_{pk}
Conventional DAB	V_{in}	$i_2 \frac{v_2}{V_{\text{in}}}$	$\frac{1}{f_{\text{sw}}}$	$\frac{1}{2} \frac{v_2}{A_c f_{\text{sw}}}$
FC-DAB	$\frac{V_{\text{in}}}{2(N-1)}$	$i_2 \frac{2(N-1)v_2}{V_{\text{in}}}$	$\frac{1}{(N-1)f_{\text{sw}}}$	$\frac{1}{2(N-1)} \frac{v_2}{A_c f_{\text{sw}}}$

For this analysis, we keep A_c fixed between the conventional DAB and FC-DAB, and Table 6.2 shows how B_{pk} changes between the conventional DAB and the FC-DAB converters.

Then, the ratio of the peak flux density between the FC-DAB and conventional DAB can be written as shown in Eqn. 6.14.

$$\frac{B_{pk,FC-DAB}}{B_{pk,DAB}} = \frac{1}{N-1} \quad (6.14)$$

This reduction in peak flux density is directly proportional to the FCML stage level count and has positive implications for reducing core loss in the FC-DAB converter at the expense of increased conduction loss. For an ideal transformer

$$v_1 i_1 + v_2 i_2 = 0 \quad (6.15)$$

where i_1 and i_2 represent the currents entering the transformer dots. In the FC-DAB converter, the reduction in v_1 incurs a corresponding increase in i_1 on the primary side of the transformer, as shown in Table 6.2.

Several transformer designs and structures were analyzed in Ansys Q3D to find the best tradeoff between loss, intrinsic leakage inductance, and practical size of the transformer. The Ferroxcube E58/11/38 core was chosen with 3C95 material due to its low loss properties at the operating frequency [138]. Two planar E cores are joined to construct a single EE core and the two transformer windings are each placed on a separate PCB, as shown in Fig. 6.8. Thus, the designer can both tune the gap between the two E cores and tune the gap between the two windings to better control the transformer parameters in this prototype. The turns ratio of the transformer is $N_1 : N_2 = 3 : 2$, which completes the remainder of the necessary fixed-ratio voltage conversion after the FCML stage.

The transformer is constructed as shown in Fig. 6.8. A 6-layer, 2 oz PCB stackup was used for each of the transformer windings, and the copper thickness allows for high current conduction through the windings. Furthermore, Fig. 6.9 shows a more detailed view of both the primary and secondary winding configurations across the PCB layers.

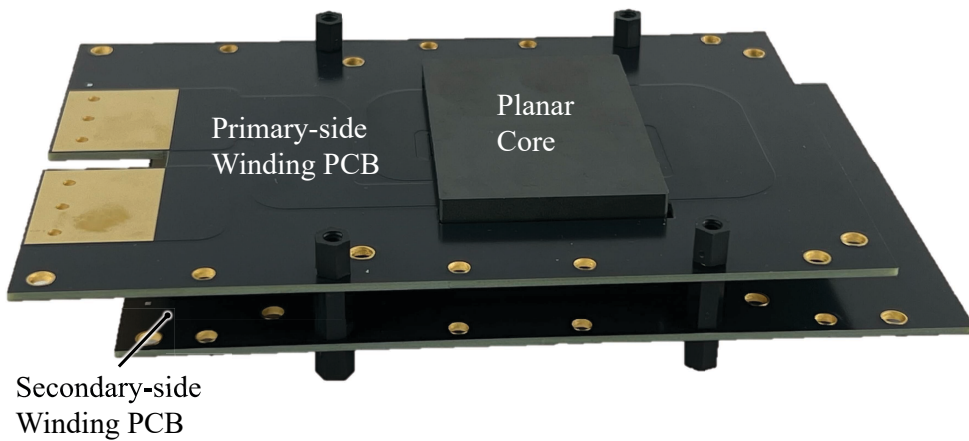


Figure 6.8: Annotated photograph of the planar transformer daughterboard with primary- and secondary-side PCB configurations shown.

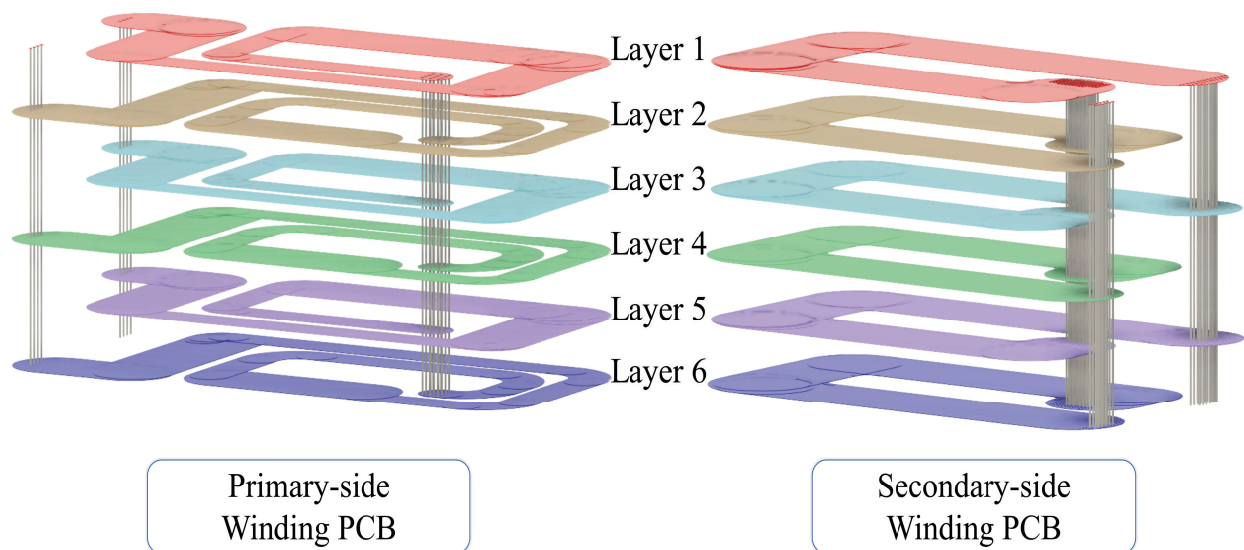


Figure 6.9: Detailed, exploded views showing both the primary and secondary winding configurations.

6.3 Hardware Prototype and Experimental Results

Table 6.3: Converter Design Parameters

Parameter	Value
V_{in}	800 V
V_{out}	53.3 V
$f_{\text{sw, FCML}}$	40 kHz
$f_{\text{sw, rectifier}}$	200 kHz
N	3:2 turns
C_{fly}	6 μF
Total L_{lk}	2.8 μH

A hardware prototype was built and tested to verify the operation of the FC-DAB converter. The operating conditions are shown in Table 6.3. Each major part of the converter – the primary-side FCML stage, transformer, and secondary-side rectifier – was designed on a separate printed circuit board to increase the modularity of the overall system. This modularity allows for a lower profile design and an increase in total system power density. The system is shown in Fig. 6.10, where the secondary-side rectifier board is stacked below the primary-side FCML board, and is coupled to it via the transformer. Fig. 6.11 shows a more detailed view of the top and bottom sides of the prototype with major components labeled. EPC GaN switches are used for both the primary- and secondary-side switches, as indicated in Table 6.4. The FCML stage employs a lateral commutation loop with a shielding plane on the PCB layer directly below the FETs [139, 140]. Local decoupling capacitors are used to reduce commutation loop inductance, and the bulk flying capacitance is placed on the back side of the board [141, 142]. High-voltage clearances on the internal layers of the hardware prototype are based on the IPC 2221B standard, and external clearances would be met through the addition of a conformal coating. Appendix B contains more detailed information about the FCML stage schematic and PCB layout.

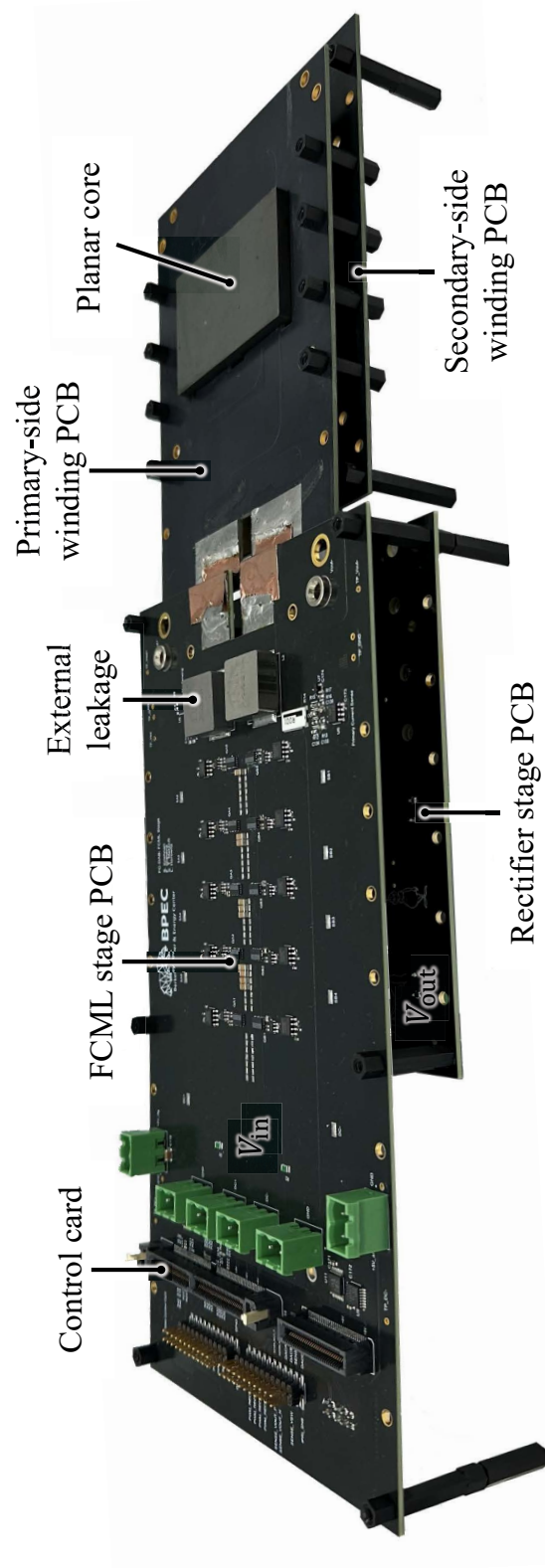
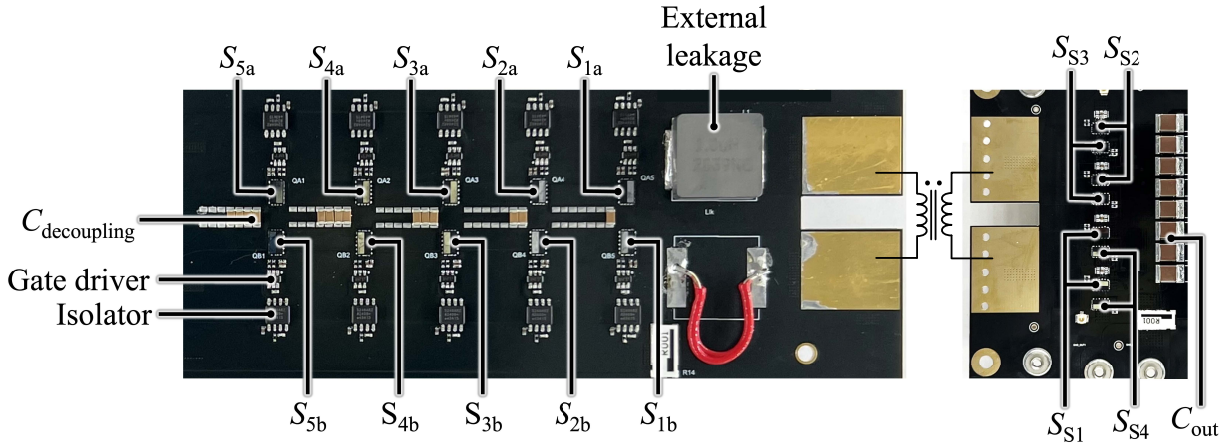
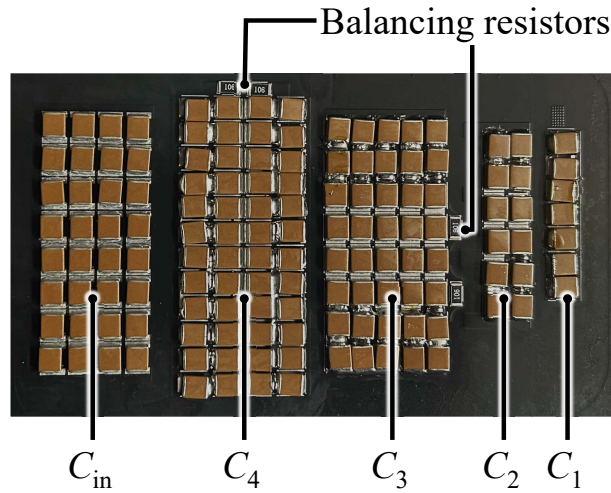


Figure 6.10: Photograph of the full system hardware prototype with major components labeled.



(a) Top of hardware prototype, showing both the FCML stage and rectifier stage PCBs.



(b) Bottom of FCML stage PCB, showing flying capacitance volume required to achieve 6 μF of C_{fly} .

Figure 6.11: Detailed photographs of the FC-DAB hardware design with major components labeled.

Since the conversion ratio is quite high in this work, the output rectifier must handle high currents at a frequency of f_{rect} , warranting thoughtful PCB layout. To reduce conduction losses at high load currents, two parallelized GaN HEMTs are employed. A detailed schematic showing the parallelized FET structure for the full-bridge rectifier is depicted in Fig. 6.12. For example, S_{S1} is comprised of two parallel GaN HEMTs, S_{S1a} and S_{S1b} , and each of the rectifier switches is configured in this way. To mitigate ringing and overshoot, a tight decoupling strategy is used. Instead of placing parallel FETs adjacent to each other,

they are each placed in a separate half-bridge configuration with local decoupling capacitors for each half-bridge. This is shown in detail in Fig. 6.12 along with the tight commutation loop that is employed for each switch pair in a single half-bridge within the layout. Symmetric layout enables even current sharing between parallel devices, while the tight commutation loop minimizes ringing.

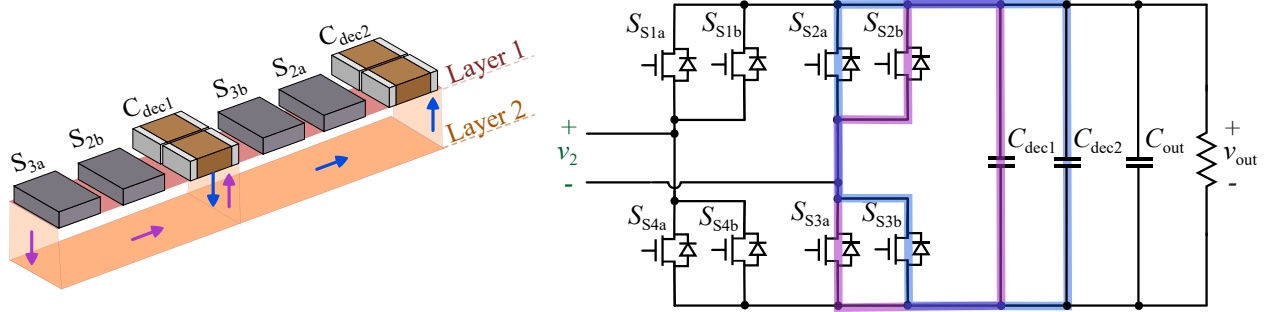


Figure 6.12: Half-bridge commutation loop and schematic for parallelized GaN HEMTs within the secondary-side rectifier.

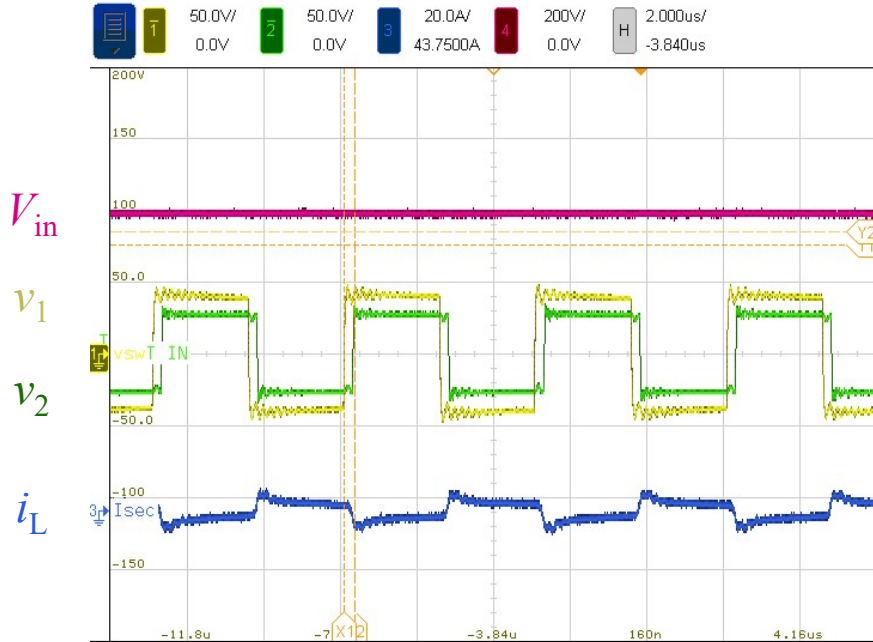


Figure 6.13: Measured waveforms of the input voltage (V_{in}), primary-side voltage (v_1), secondary-side voltage (v_2), and leakage inductor current referred to the secondary side (i_L) of the FC-DAB converter for the conversion of $V_{in} = 400$ V to $V_{out} = 26.6$ V.

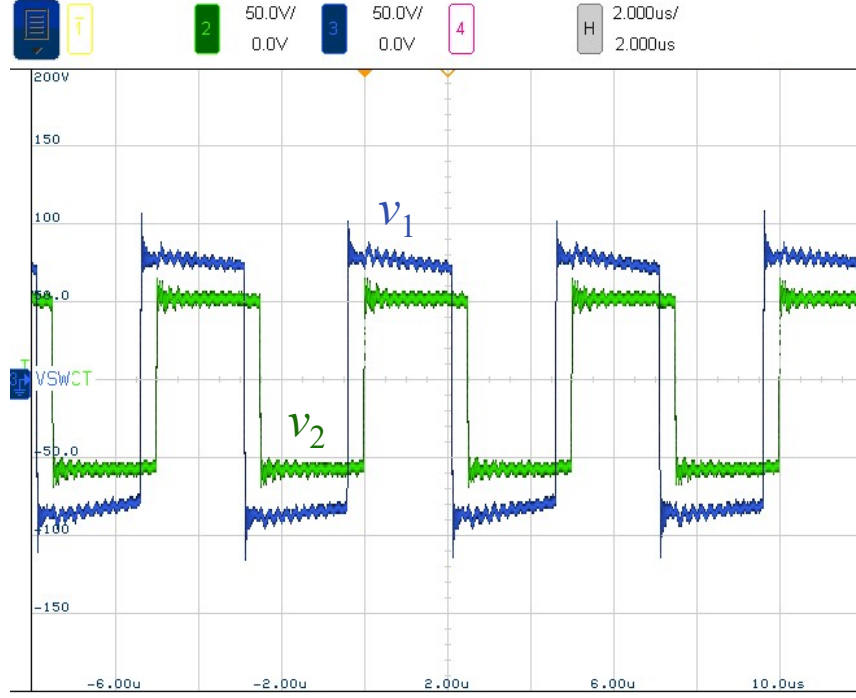


Figure 6.14: Measured waveforms of the primary-side voltage (v_1) and secondary-side voltage (v_2) of the FC-DAB converter for the conversion of $V_{in} = 800$ V to $V_{out} = 53.3$ V at $P_{out} = 704$ W.

Fig. 6.13 shows measured hardware prototype waveforms for a fixed-ratio conversion from a 400 V input voltage to a 26.6 V output, or a 15:1 step-down. The waveforms showcase that converter operation is consistent with theoretical expectations. Data taken at $V_{in} = 800$ V is depicted in Fig. 6.14 and showcases the primary-side and secondary-side ac voltages seen at the two terminals of the transformer. The inductor current i_L is not shown here as the required insertion of the current probe exacerbated unwanted parasitic elements in the design. Voltage v_1 starts to exhibit flying capacitor voltage ripple as the current through the converter is increased.

The switch-node waveforms (v_1) demonstrate excellent flying capacitor voltage balancing as indicated by the even heights of the pulse trains, while maintaining modest high-frequency oscillation from parasitic capacitances [143]. To further validate flying capacitor voltage balancing, Fig. 6.15 shows experimental voltage waveforms for the four flying capacitors on the primary side of the FCDAB converter. An inset shows the flying capacitor voltage ripple as measured by high-bandwidth differential voltage probes. Good natural balancing is observed, and may be attributed here to symmetric layout, and the choice of an even level count FCML converter stage [135].

Table 6.4: Key Components of the FC-DAB Hardware Prototype - Power Stage

Component	Mfr. & Part Number	Parameters
Primary Side: FCML		
Switches S_{1a} - S_{5b}	EPC EPC2304	GaN, 200 V, 5 m Ω
Flying Capacitance C_1 - C_4	TDK C5750X6S2W225K250KA	2.2 μ F, 450 V
Decoupling Capacitance	Kemet C1206C103KFRACU	10000 pF, 1500 V
Level Shifter	Texas Instruments SN74LV4T125PWR	buffer, non-inverting
Isolator	Analog Devices Inc. ADUM5240ARZ	2-channel, unidirectional
Gate Driver	Texas Instruments LM5114	low-side driver
Secondary Side: Rectifier		
Switches S_{S1} - S_{S4}	EPC EPC2302	GaN, 100 V, 1.8 m Ω
Digital Isolator	NVE IL 711-3E	2-channel, unidirectional
Gate Driver	Texas Instruments LM5114	low-side driver
Bootstrap Diode	Diodes Incorporated MBR0580S1-7	Schottky, 80 V, 500 mA
Planar Transformer		
E Core	Ferroxcube E58/11/38-3C95	3C95 material
Control		
Microcontroller	Texas Instruments TMDSCNCD28379D	C2000

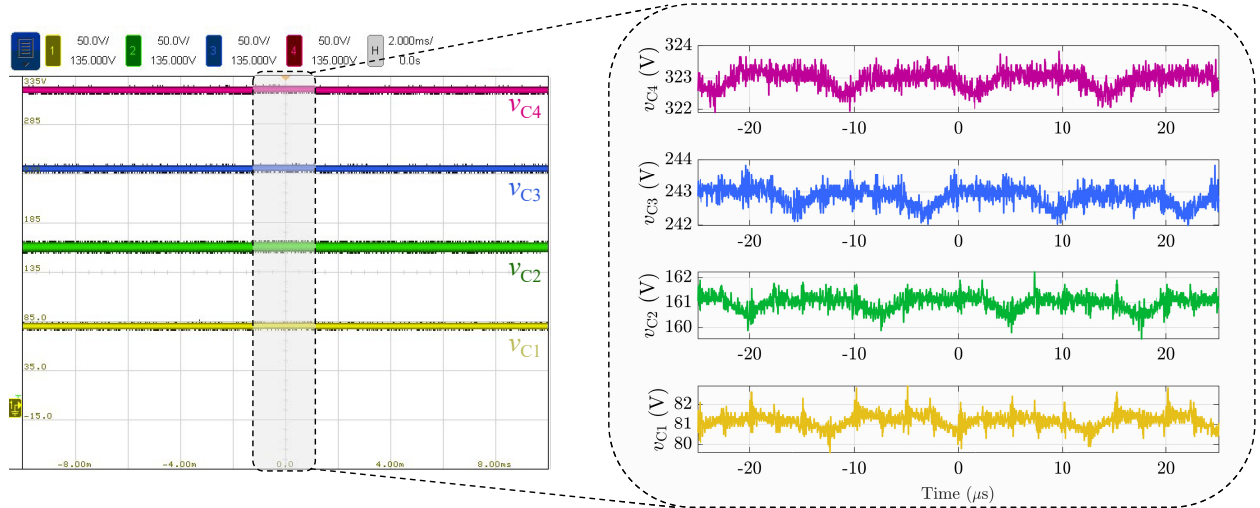


Figure 6.15: Measured flying capacitor voltages at fractions of the input voltage, $V_{in} = 400$ V, on the primary side of the FCDAB converter. In this measurement, $P_{out} = 110$ W at $\phi_2 = 15^\circ$. This demonstrates that the capacitors naturally balance to their nominal steady-state values.

Fig. 6.16 shows an efficiency sweep for the FC-DAB converter operating with an 800 V

input, measured with fan cooling only, on a high-precision PA2201A IntegraVision Power Analyzer. In these measurements, the phase shift between the primary and secondary sides (ϕ_2) is swept from 9° to 26° to achieve a range of output powers. This phase shift range is restricted to limit the converter rms currents as well as the voltage ripple on the flying capacitance for a given leakage inductance. The converter achieves a peak efficiency of 96.48% at an output power of 547 W and a full load efficiency of 95.77% at an output power of 704 W. Notably, the light load efficiency is improved in comparison to a conventional DAB converter as the FCML stage has reduced switching losses in this light load regime. Some of this improvement in light load efficiency is attributed to reduced C_{oss} loss. As each switch only blocks a fraction of the input voltage, the C_{oss} of each switch in the FCML stage needs to only discharge a fraction of the input voltage, rather than the entire input voltage. For low-side and high-side switches of the FCML stage to achieve ZVS, both positive and negative inductor current is required [144, 145]. Utilizing the FCML stage on the primary-side of the FC-DAB configuration naturally satisfies this condition as the leakage inductor current is bidirectional.

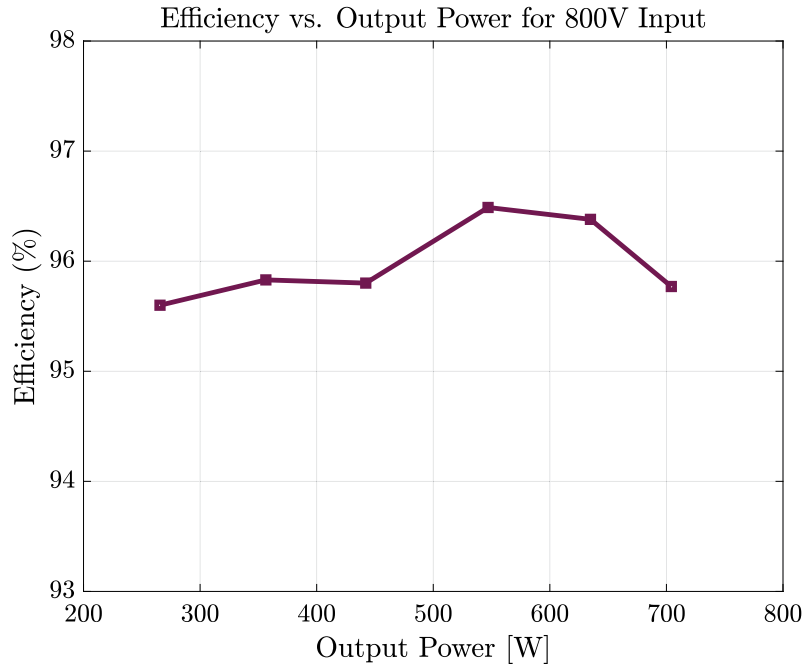


Figure 6.16: Measured efficiency results for the converter operating from $V_{in} = 800$ V to $V_{out} = 53.3$ V.

6.4 Closed Loop Voltage Regulation for the FC-DAB Converter

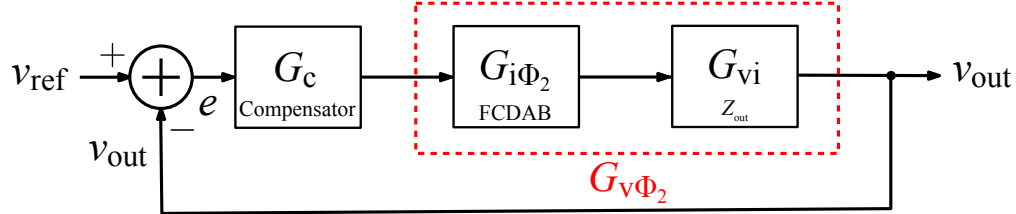


Figure 6.17: Control block diagram for output voltage regulation of the FCDAB converter.

High-voltage line ripple rejection is imperative to the proper functioning of downstream electrical systems in vehicles [146]. The variations at the electrical frequency of the motor/traction system on the order of 100s of Hz are too small to be filtered out effectively without very large capacitances, so this ripple can arise on the bus itself. Subsequently, the high-voltage bus varies periodically, creating a disturbance that the converter has to reject. If not managed properly, ripple noise can present as a safety hazard and be detrimental to automotive systems [146]. Many power converters within a vehicle need to maintain a regulated output voltage rail in response to these line disturbances.

While the focus of this work is on the power converter stage itself, a closed-loop controller is designed around the FC-DAB system to demonstrate that existing modeling and control methods for the DAB may be readily extended to the FC-DAB converter. Motivated by line ripple rejection, the closed-loop controller is implemented to regulate the output voltage in the presence of line disturbances. The general controller block diagram for the system is shown in Fig. 6.17, and the various gains within this controller are derived below.

We begin by deriving a reduced-order model for the FC-DAB operating with SPS modulation. The control techniques for SPS used in standard DAB applications may be applied to the FC-DAB converter as well. The reduced-order model [147] simplifies DAB modeling by neglecting the dynamics of the leakage inductor current and is readily applied to the FC-DAB converter, by considering that the flying capacitor stage modifies the amplitude and frequency at the output of the inverter stage.

To start, the power flow equation can be written as

$$p_{\text{out}}(\phi_2) = \frac{N_1 V_1 V_2}{2\pi L_{\text{lk}} f_{\text{eff}}} \cdot \left(\phi_2 - \frac{\phi_2^2}{\pi} \right) \quad (6.16)$$

where $0 < \phi_2 < \frac{\pi}{2}$, $V_1 = \frac{V_{\text{in}}}{2(N-1)}$, and $V_2 = V_{\text{out}}$.

Taking the derivative of P_{out} with respect to ϕ_2 yields

Table 6.5: Key Components of the FC-DAB Hardware Prototype - Sensing

Component	Mfr. & Part Number	Parameters
Primary Side		
Input Voltage Sense	Analog Devices LTC6268IS8#TRPBF	Ultra-low bias amplifier
Secondary Side		
Output Voltage Sense	Texas Instruments AMC1211AQDWVRQ1	Precision, isolated amplifier

$$\frac{dp_{\text{out}}(\phi_2)}{d\phi_2} = \frac{\frac{N_1}{N_2}V_1V_2}{2\pi L_{\text{lk}}f_{\text{eff}}} \cdot \left(1 - \frac{2\phi_2}{\pi}\right). \quad (6.17)$$

Here, p_{out} can be written in terms of its dc and small-signal ripple components as shown in Eqn. 6.18 where $\Phi_{2,0}$ refers to the steady-state equilibrium point around which the derivative is evaluated

$$p_{\text{out}}(\phi_2) = P_{\text{out}}(\phi_2) + \left. \frac{dp_{\text{out}}(\phi_2)}{d\phi_2} \right|_{\Phi_{2,0}} \tilde{\phi}_2. \quad (6.18)$$

Substituting Eqn. 6.17 into Eqn. 6.18, we get

$$p_{\text{out}}(\phi_2) = P_{\text{out}}(\phi_2) + \frac{\frac{N_1}{N_2}V_1V_2}{2\pi L_{\text{lk}}f_{\text{eff}}} \cdot \left(1 - \frac{2\Phi_{2,0}}{\pi}\right) \cdot \tilde{\phi}_2. \quad (6.19)$$

The output current, i_{out} , can be written as

$$i_{\text{out}}(\phi_2) = \frac{P_{\text{out}}(\phi_2)}{V_2} + \frac{\frac{N_1}{N_2}V_1}{2\pi L_{\text{lk}}f_{\text{eff}}} \cdot \left(1 - \frac{2\Phi_{2,0}}{\pi}\right) \cdot \tilde{\phi}_2. \quad (6.20)$$

Therefore, the transfer function from $\tilde{\phi}_2$ to $\tilde{i}_{\text{out}}$, $G_{i\phi_2}$, can be determined as

$$G_{i\phi_2} = \frac{\frac{N_1}{N_2}V_1}{2\pi L_{\text{lk}}f_{\text{eff}}} \cdot \left(1 - \frac{2\Phi_{2,0}}{\pi}\right). \quad (6.21)$$

The FC-DAB converter has an output filter comprised of R_{load} and C_{out} (Fig. 6.3) allowing us to write the output impedance as a transfer function, $Z_{\text{out}} = \frac{R_{\text{load}}}{1+sR_{\text{load}}C_{\text{out}}}$.

Finally, the transfer function from $\tilde{\phi}_2$ to $\tilde{v}_2$, $G_{v\phi_2}$, is given as

$$G_{v\phi_2} = G_{i\phi_2} \cdot Z_{\text{out}} = \frac{\frac{N_1}{N_2}V_1}{2\pi L_{\text{lk}}f_{\text{eff}}} \cdot \left(1 - \frac{2\Phi_{2,0}}{\pi}\right) \cdot \frac{R_{\text{load}}}{1+sR_{\text{load}}C_{\text{out}}} \quad (6.22)$$

The FC-DAB hardware prototype is equipped with both primary-side and secondary-side voltage sensing to enable output voltage regulation on the low-voltage side. Table 6.5 lists the key sensing components used in the hardware prototype.

A PI feedback controller that adjusts the phase shift between the primary and secondary sides of the FC-DAB converter is implemented on a C2000 DSP with a 2 kHz bandwidth and a 40 kHz sampling frequency. To validate the closed-loop control scheme in hardware, a 100 Hz ac disturbance with an amplitude of 10 V is injected onto a 100 V_{dc} line at the input of the FC-DAB converter. The output voltage of the FC-DAB is successfully regulated to 6 V at this condition. This is illustrated in Fig. 6.18. Prior to enabling the control, v_{out} tracks the sinusoidal V_{in} instead of maintaining a constant dc value. The non-linear relationship between v_{out} and ϕ_2 leads to larger output voltage deviations under line disturbances. After the control is enabled, the output voltage is regulated to the target 6 V and is able to successfully reject the line disturbance.

For control necessitating a higher bandwidth, active balancing for the flying capacitors may be required. In this case, a parallel balancing control scheme may be designed, which is able to regulate both the flying capacitors as well as the output power [148].

The hardware findings are summarized here. The FC-DAB converter prototype showcases full high-voltage capability at the rated 800 V input voltage and achieves a peak efficiency of 96.48%. Successful closed-loop output voltage regulation is demonstrated in the presence of a line disturbance.

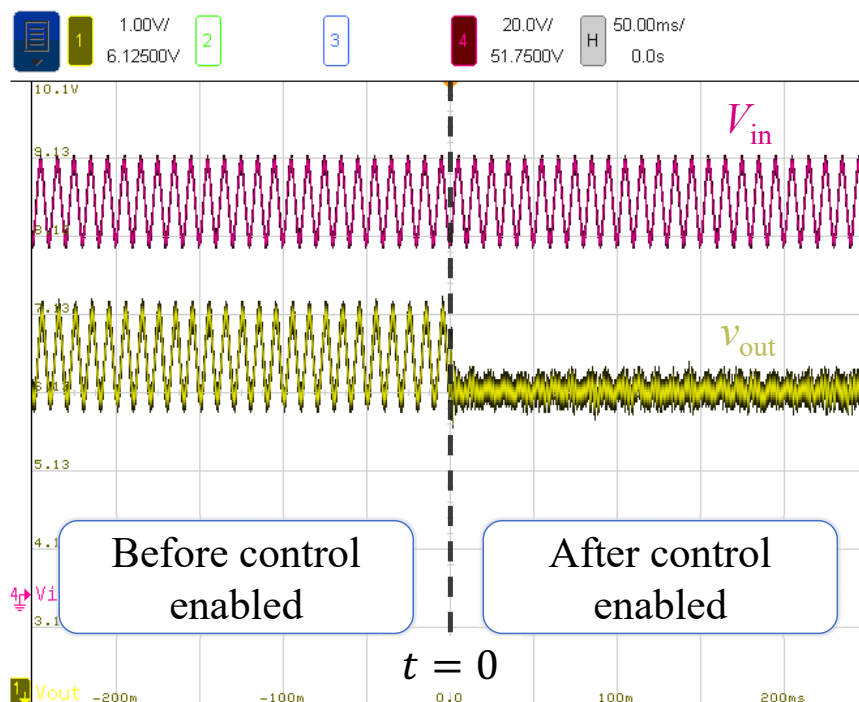


Figure 6.18: Demonstration of closed-loop operation of the FC-DAB converter in response to a line disturbance. The controller is enabled at $t = 0$.

6.5 Conclusion and Future Work

The arrival of higher voltage architectures in automotive applications creates opportunities for innovation in high-performance power converter topologies. This work presents the FC-DAB converter, an isolated power topology that utilizes an FCML converter stage on the primary side in lieu of the traditional full-bridge inverter found in a conventional two-level DAB. This chapter discusses the converter topology and operation, as well as important design considerations that influence the final experimental prototype. Finally, experimental results are presented for the FCDAB converter, which achieves a peak efficiency of 96.48% at a 15:1 step-down conversion ratio. It is also able to regulate its output voltage in the presence of line disturbances, showcasing the viability of using such a converter in 800 V systems.

As the 800 V bus grows more popular and the power industry is looking towards adopting even higher voltage architectures, research in the area of novel converter topologies is only beginning. Future work on the FC-DAB topology includes further quantifying the optimal relationship between how much voltage conversion the FCML stage handles compared to the transformer stage. Additional modulation techniques beyond SPS modulation may also be possible with the FCML stage on the primary side, and this warrants further investigation to increase converter efficiency. Finally, it would be worthwhile to develop a hardware prototype with improved packaging to further assess the power density limits of the converter.

Chapter 7

Conclusions

7.1 Concluding Remarks

Transportation electrification is increasingly prevalent in the modern world and the amount of power that needs to be processed in a single vehicle is only increasing. To keep up with these increased power demands and the changing voltage architectures that come with them, novel power converter topologies are needed for improved power density and performance. Hybrid switched-capacitor converters are one class of converter that shows promise for high performance in this design space, but there are practical challenges that arise when trying to transition these converters into industrial transportation environments. This dissertation presented the design and test of novel dc-dc converters for modern transportation voltage architectures. Each of these designs explores one or more of four major challenges: EMI, dynamic operation, isolation, and output voltage regulation.

EMI pre-compliance and output voltage regulation are addressed within the context of 48 V automotive systems with a Dickson-based hybrid SC topology. A single-ended, regulating hybrid Dickson topology also serves as a case study for modeling the dynamic operation of hybrid SC converters. Isolation for signal integrity is addressed with an isolated two-stage converter for satellite applications. Finally, insights from this design are applied to the 800 V voltage architecture with a high-step-down, isolated, FC-DAB topology which addresses both isolation and output voltage regulation.

7.2 Future Work

During the Ph.D. degree, I have been fortunate enough to tackle many practical challenges in power electronics. This section briefly outlines some of this work and provides some general direction for future research.

Hybrid SC EMI Modeling and Measurement

EMI remains a challenge and roadblock for adopting many novel topologies into the industry. There is much opportunity for extending current modeling approaches more generally to other hybrid SC topologies. The analysis of the EMI behavior becomes interesting in hybrid SC topologies where the switching phases are not symmetric and special control techniques (such as split-phase switching) are required to maintain soft-charging of the flying capacitors. Moreover, hybrid SC converters that are less “cellular” in nature and that utilize switches with uneven blocking voltages merit further investigation. Investigation of fundamental EMI behavior, and practical converter implementation challenges that impact EMI such as layout create many opportunities for future research. Work in this space can extend to more streamlined qualification of hybrid SC converters for application-based EMI standards.

Simplified Hybrid SC Control

Hybrid SC converters can be fully or partially soft-charged through the addition of one or more inductors. Eliminating capacitor charge-sharing losses in these converters is crucial to their high efficiencies. This research direction is motivated by the complexity of switching schemes (such as split-phase control for the hybrid Dickson converter), and reducing this control complexity to make these topologies easier to adopt.

In [149], the authors outline an approach to analyze the soft-charging operation of hybrid SC converters based on circuit inspection and intuition rather than heavy numerical computation. This analysis can be extended to optimizing the number of inductors required to achieve soft charging, and where they should be placed within different hybrid SC topologies. Such research can inform tradeoffs in component sizing, component mismatch, efficiency, and solution size for designers.

Hybrid SC Compensator Design

Many applications have stringent transient requirements and hybrid SC converters must respond to disturbances while meeting specifications related to settling time, voltage overshoot/ undershoot. The modeling of hybrid SC converters involves capturing the dynamics of flying capacitors which can change how optimized feedback control loops should be designed. These flying capacitor dynamics warrant further study to determine their impact on compensator design. Furthermore, it is useful to analyze when it makes sense to treat the switched-capacitor network as a “black box” to reduce control and modeling complexity.

Isolation and Hybrid SC Converters

Merged topologies utilizing both switched-capacitor (SC) stages and various forms of isolation (capacitive and magnetic) have been showcased with success. These converters show promise by utilizing better FOM devices and show that SC topologies interface well with

isolation techniques. Future research directions include establishing general procedures for deriving isolated topologies from non-isolated SC converters [150]. A detailed framework could provide insight into how design constraints and modulation techniques may change with the required isolation.

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Appendix A

State-Space Matrices for Discrete-Time Dynamical Dickson Modeling

This appendix contains the full-form state-space matrices for each of the hybrid Dickson converter switching phases as well as the state-space matrices for the “transformer buck” model. These matrices are utilized in the discrete-time model comparisons presented in Chapter 3.

The A and B matrices are constructed for each phase of the hybrid Dickson converter operation – main phases, “split” phases, and regulating phases. These matrices are similarly constructed for the “transformer buck” model. The fundamental state-space equation used in both models is reproduced here (Eqn. A.1).

$$\dot{x} = A \cdot x + B \cdot u \quad (\text{A.1})$$

To reiterate information presented in Chapter 4, the effective lumped resistance (R_S) in the model is comprised of the on-resistance of the switches (R_{on}), the ESR of the flying capacitors (R_{esr}) and the resistance of the inductor (R_L). While this term R_S is not explicitly used in the state matrices, its value changes in each circuit state as a facet of the other terms. The terms within the matrices for both the full model and the “transformer buck” model are defined as follows:

- C_1 - C_3 : Flying capacitors in the 4-to-1 hybrid Dickson circuit. Each flying capacitor has an identical value and is derated for the voltage it blocks.
- R_{on} : Switch on-resistance which is identical for each switch in the hybrid Dickson circuit.
- R_{esr} : Flying capacitor equivalent series resistance (ESR) which is identical for each flying capacitor in the hybrid Dickson circuit.

- L : Output inductor value.
- R_L : Resistance of the output inductor.
- C_o : Output capacitance derated for the desired output voltage.

A.1 State-Space Matrices for Full Model

For the full model, the state variable and input equations are shown in Eqns. A.2 and A.3.

$$x = \begin{bmatrix} v_{C1} & v_{C2} & v_{C3} & i_L & v_{out} \end{bmatrix}^T \quad (\text{A.2})$$

$$u = \begin{bmatrix} v_{in} & i_{load} \end{bmatrix}^T \quad (\text{A.3})$$

Each of the matrices is written out in the subsections below. Eqns. A.4 and A.5 and Eqns. A.6 and A.7 show the matrices for the main operating phases in the circuit. Eqns. A.8 and A.9 and Eqns. A.10 and A.11 show the matrices for the “split” operating phases in the circuit. Finally, Eqns. A.12 and A.13 show the matrices for the two regulating phases in the circuit.

Full Model: Main Phase 1a (A_{1a} and B_{1a})

In the following matrices, let $\Gamma = \frac{1}{3(R_{on}+R_{esr})}$. The state-space matrices for the main phase 1a are then given by:

$$A_{1a} = \begin{bmatrix} -\frac{\Gamma}{C_1} & -\frac{\Gamma}{C_1} & \frac{\Gamma}{C_1} & \frac{-2}{3C_1} & 0 \\ -\frac{\Gamma}{C_2} & -\frac{\Gamma}{C_2} & \frac{\Gamma}{C_2} & \frac{1}{3C_2} & 0 \\ \frac{\Gamma}{C_3} & \frac{\Gamma}{C_3} & -\frac{\Gamma}{C_3} & \frac{-1}{3C_3} & 0 \\ \frac{2}{3L} & \frac{-1}{3L} & \frac{1}{3L} & -\frac{5R_{on}+3R_L+2R_{esr}}{3L} & \frac{1}{L} \end{bmatrix} \quad (A.4)$$

$$B_{1a} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{C_o} \end{bmatrix} \quad (A.5)$$

Full Model: Main Phase 2a (A_{2a} and B_{2a})

Once again, let $\Gamma = \frac{1}{3(R_{\text{on}} + R_{\text{esr}})}$. The state-space matrices for the main phase 2a are then given by:

$$A_{2a} = \begin{bmatrix} -\frac{\Gamma}{C_1} & \frac{\Gamma}{C_1} & \frac{\Gamma}{C_1} & \frac{1}{3C_1} & 0 \\ \frac{\Gamma}{C_2} & -\frac{\Gamma}{C_2} & -\frac{\Gamma}{C_2} & -\frac{1}{3C_2} & 0 \\ \frac{\Gamma}{C_3} & -\frac{\Gamma}{C_3} & -\frac{\Gamma}{C_3} & \frac{2}{3C_3} & 0 \\ -\frac{1}{3L} & \frac{1}{3L} & -\frac{2}{3L} & -\frac{5R_{\text{on}} + 3R_L + 2R_{\text{esr}}}{3L} & -\frac{1}{L} \end{bmatrix} \quad (\text{A.6})$$

$$B_{2a} = \begin{bmatrix} -\frac{\Gamma}{C_1} & 0 \\ \frac{\Gamma}{C_2} & 0 \\ \frac{\Gamma}{C_3} & 0 \\ \frac{2}{3L} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (\text{A.7})$$

Full Model: Split Phase 1b (A_{1b} and B_{1b})

The state-space matrices for the split phase 1b are given by:

$$A_{1b} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{C_2} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_3} & 0 \\ 0 & \frac{-1}{L} & \frac{1}{L} & -\frac{3R_{on}+R_L+2R_{esr}}{L} & \frac{-1}{L} \\ 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix} \quad (A.8)$$

$$B_{1b} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{C_o} \end{bmatrix} \quad (A.9)$$

Full Model: Split Phase 2b (A_{2b} and B_{2b})

The state-space matrices for the split phase 2b are given by:

$$A_{2b} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L} & \frac{1}{L} & 0 & -\frac{3R_{on}+R_L+2R_{esr}}{L} & -\frac{1}{L} \\ 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix} \quad (A.10)$$

$$B_{2b} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{C_o} \end{bmatrix} \quad (A.11)$$

Full Model: Regulating Phases 1c and 2c (A_{1c} , A_{2c} and B_{1c} , B_{2c})

The state-space matrices for the regulating phases 1c and 2c are given by:

$$A_{1c}, A_{2c} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R_{on}+R_L}{L} & -\frac{1}{L} \\ 0 & 0 & 0 & \frac{1}{C_o} & 0 \end{bmatrix} \quad (A.12)$$

$$B_{1c}, B_{2c} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.13)$$

A.2 State-Space Matrices for “Transformer Buck” Model

The following subsections contain the state matrices for the “transformer buck” model. The state variable and input equations (Eqns A.14 and A.15) for this model are written below.

$$x = \begin{bmatrix} i_L & v_{out} \end{bmatrix}^T \quad (A.14)$$

$$u = \begin{bmatrix} v_{in} & i_{load} \end{bmatrix}^T \quad (A.15)$$

“Transformer Buck” Model: Main Phase 1a (A_{1ax} and B_{1ax})

The state-space matrices for the main phase 1a are given by:

$$A_{1ax} = \begin{bmatrix} \frac{-\frac{5}{3}R_{on}-R_L-\frac{2}{3}R_{esr}}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}, \quad B_{1ax} = \begin{bmatrix} \frac{1}{4L} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.16)$$

“Transformer Buck” Model: Main Phase 2a (A_{2ax} and B_{2ax})

The state-space matrices for the main phase 2a are given by:

$$A_{2ax} = \begin{bmatrix} \frac{-\frac{5}{3}R_{on}-R_L-\frac{2}{3}R_{esr}}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}, \quad B_{2ax} = \begin{bmatrix} \frac{1}{4L} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.17)$$

“Transformer Buck” Model: Split Phase 1b (A_{1bx} and B_{1bx})

The state-space matrices for the split phase 1b are given by:

$$A_{1bx} = \begin{bmatrix} -\frac{3R_{on}+R_L+2R_{esr}}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}, \quad B_{1bx} = \begin{bmatrix} \frac{1}{4L} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.18)$$

“Transformer Buck” Model: Split Phase 2b (A_{2bx} and B_{2bx})

The state-space matrices for the split phase 2b are given by:

$$A_{2bx} = \begin{bmatrix} -\frac{3R_{on}+R_L+2R_{esr}}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}, \quad B_{2bx} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.19)$$

“Transformer Buck” Model: Regulating Phases 1c and 2c (A_{1cx} , A_{2cx} and B_{1cx} , B_{2cx})

The state-space matrices for the regulating phases 1c and 2c are given by:

$$A_{1cx}, A_{2cx} = \begin{bmatrix} -\frac{R_{on}+R_L}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}, \quad B_{1cx}, B_{2cx} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix} \quad (A.20)$$

Appendix B

FC-DAB: FCML Stage Hardware Prototype Circuit Schematic and PCB Layout

The schematics and PCB layout for the FCML stage PCB, which serves as the primary-side of the FC-DAB converter, are included in this appendix. The Altium software rendering of the top and bottom sides of the PCB are shown below.

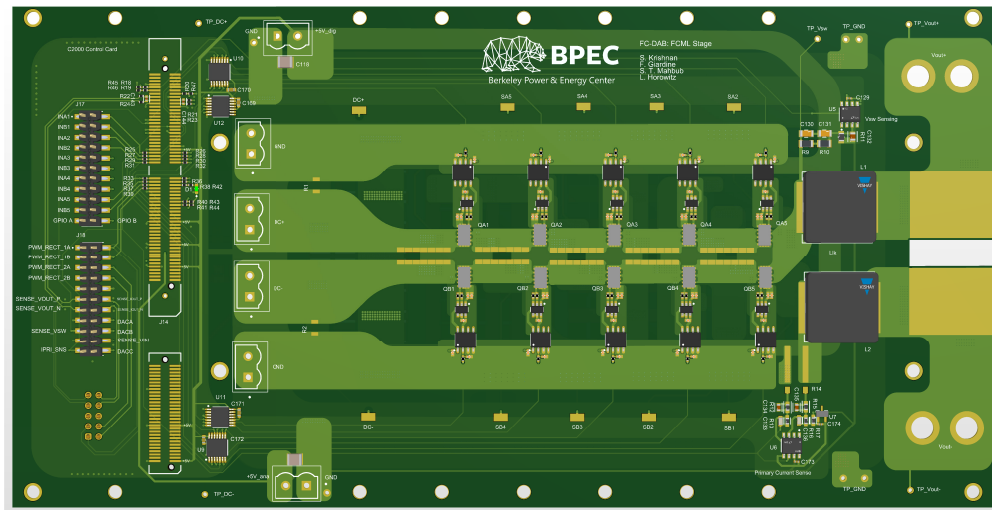


Figure B.1: Altium rendering of top of FCML stage PCB.

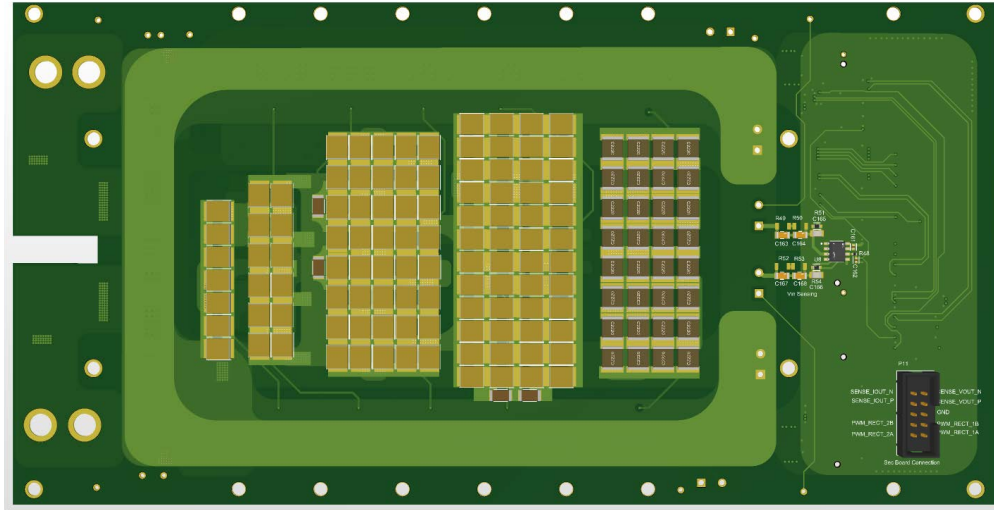


Figure B.2: Altium rendering of bottom of FCML stage PCB.

B.1 Schematics

The schematic sheets for the FCML stage design are shown below.

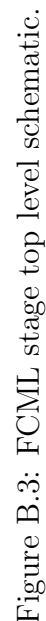
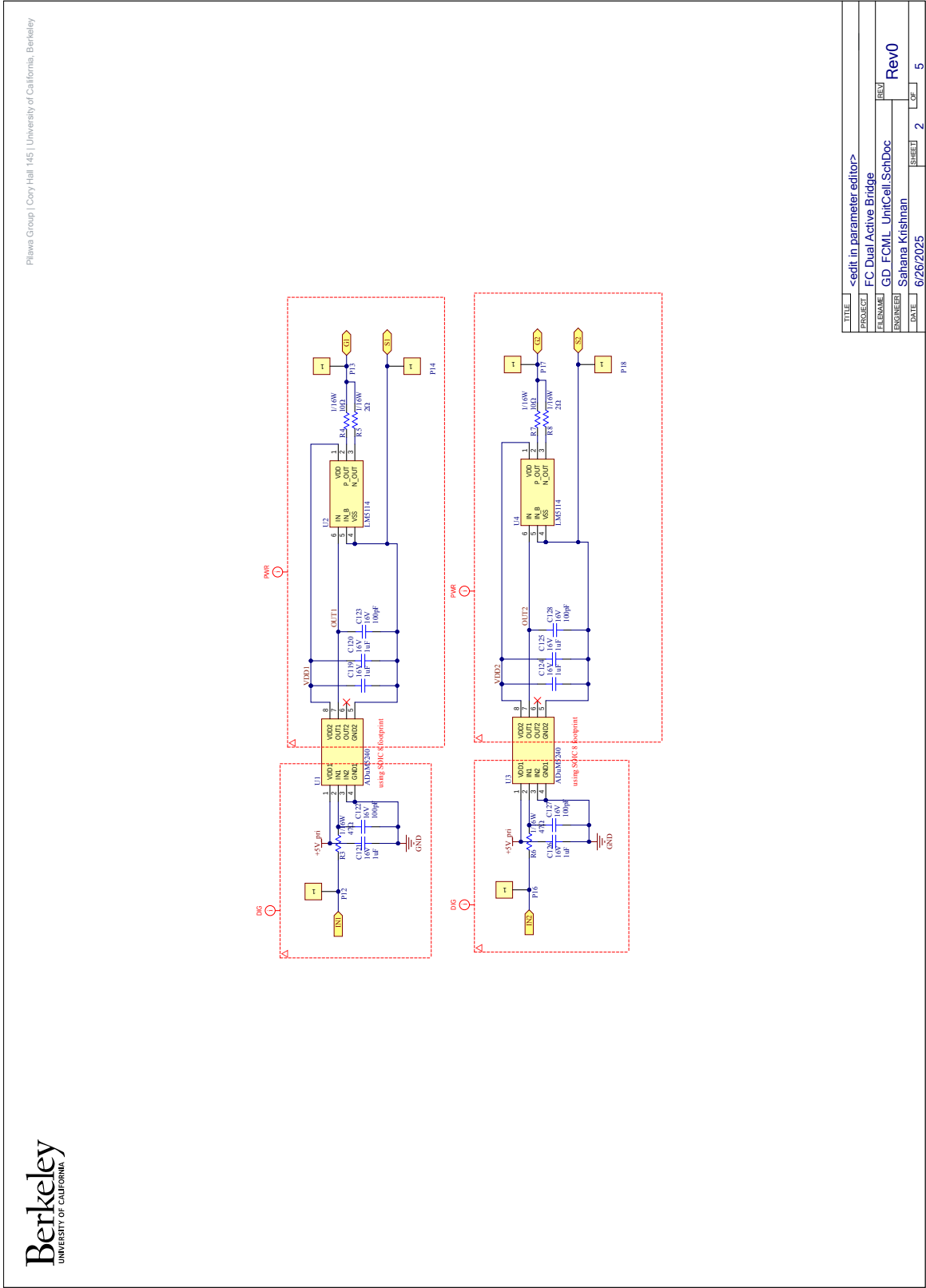


Figure B.3: FCML stage top level schematic.

APPENDIX B. FC-DAB: FCML STAGE HARDWARE PROTOTYPE CIRCUIT SCHEMATIC AND PCB LAYOUT

Figure B.4: FCML stage gate driving schematic.



APPENDIX B. FC-DAB: FCML STAGE HARDWARE PROTOTYPE CIRCUIT SCHEMATIC AND PCB LAYOUT

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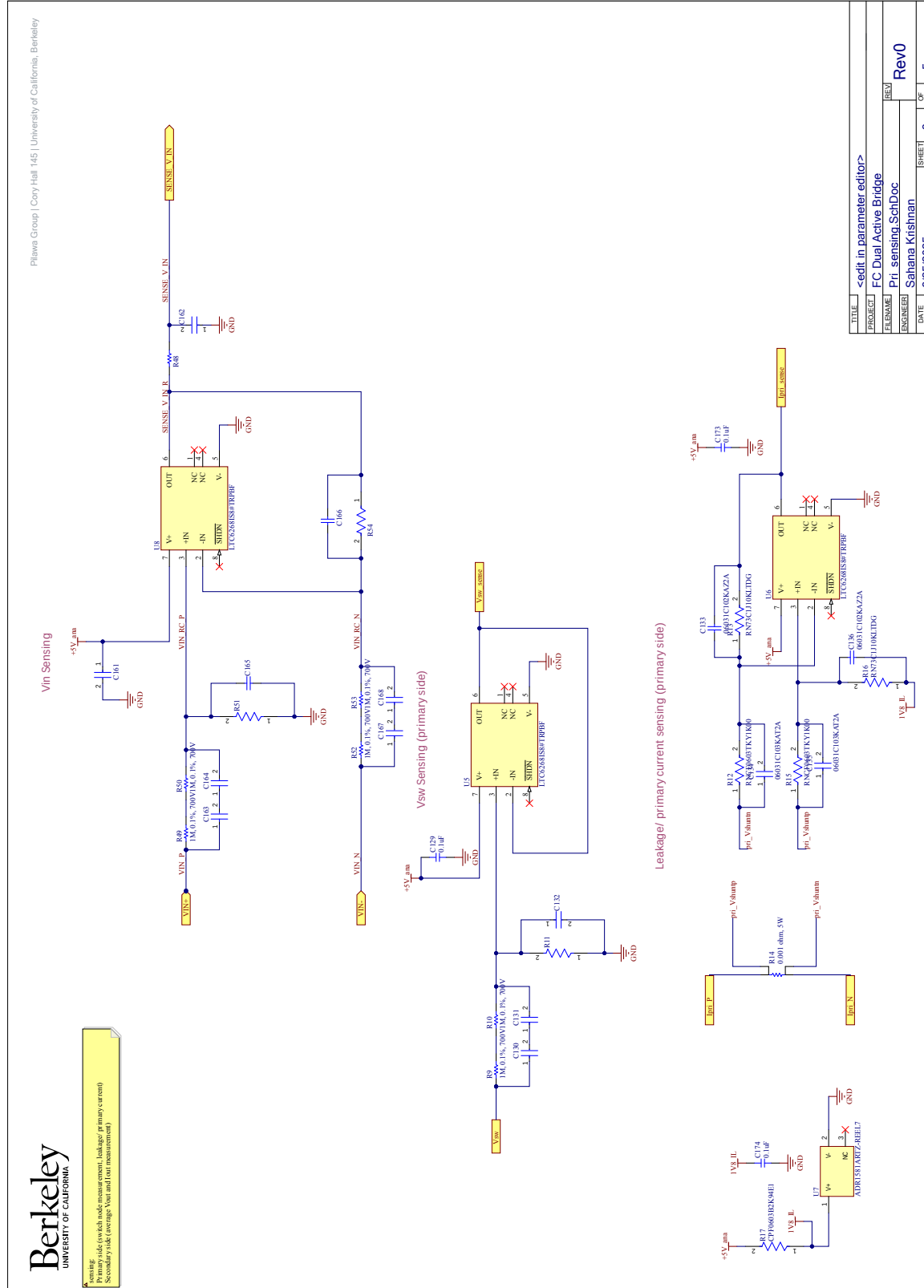


Figure B.5: FCML stage primary-side sensing schematic.

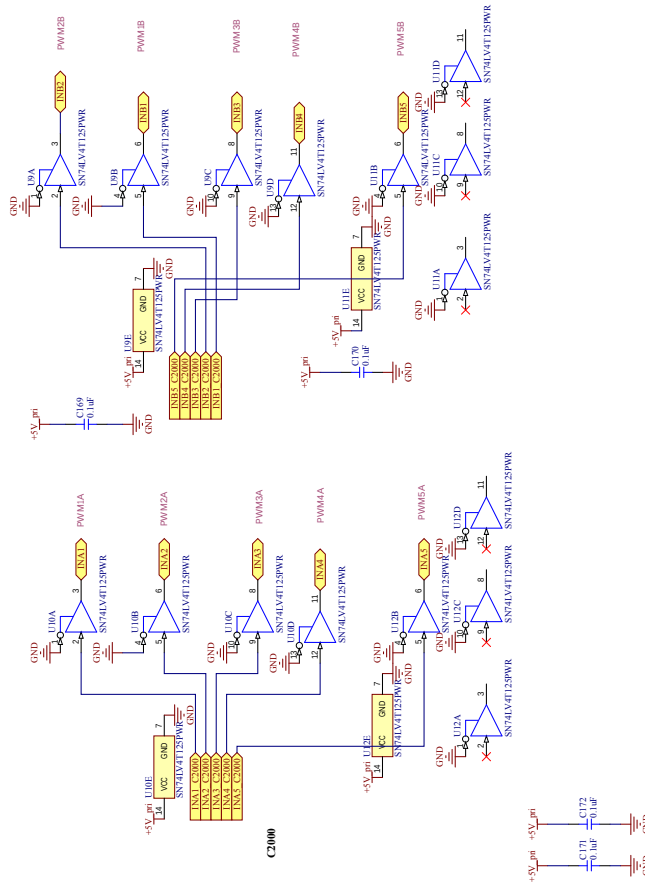
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Figure B.6: FCML stage C2000 control card schematic.

APPENDIX B. FC-DAB: FCML STAGE HARDWARE PROTOTYPE CIRCUIT SCHEMATIC AND PCB LAYOUT

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TITLE	*
PROJECT	FC Dual Active Bridge
FILENAME	LevelShifters SchDoc
ENGINEER	Sahana Krishnan
DATE	6/24/2025
SHEET	5
OF	5
REV	Rev0

Figure B.7: FCML stage level shifter schematic.

B.2 PCB Layers

The PCB layers for the FCML stage design are shown below.

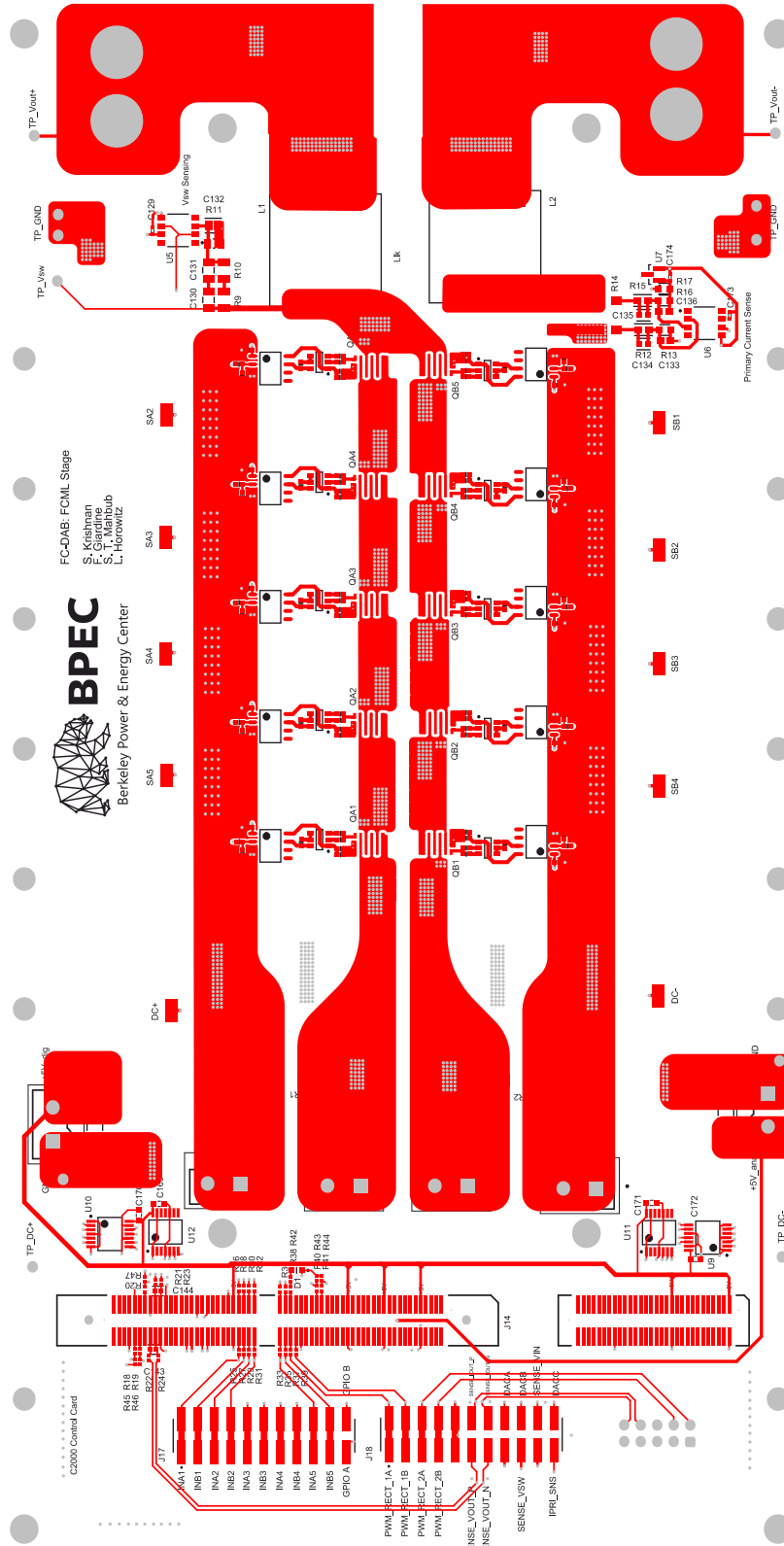


Figure B.8: Top layer of PCB.

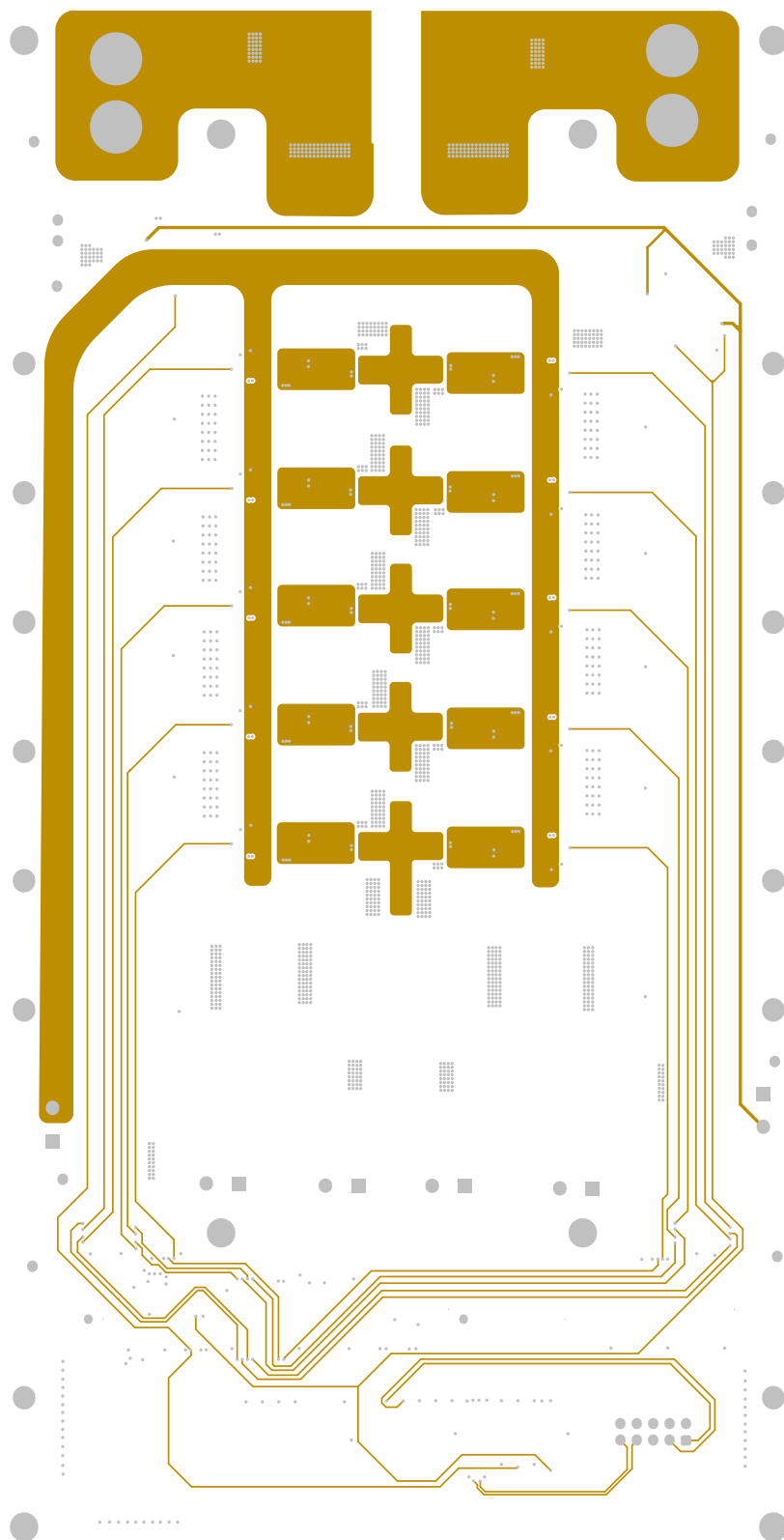


Figure B.9: First inner layer of PCB.

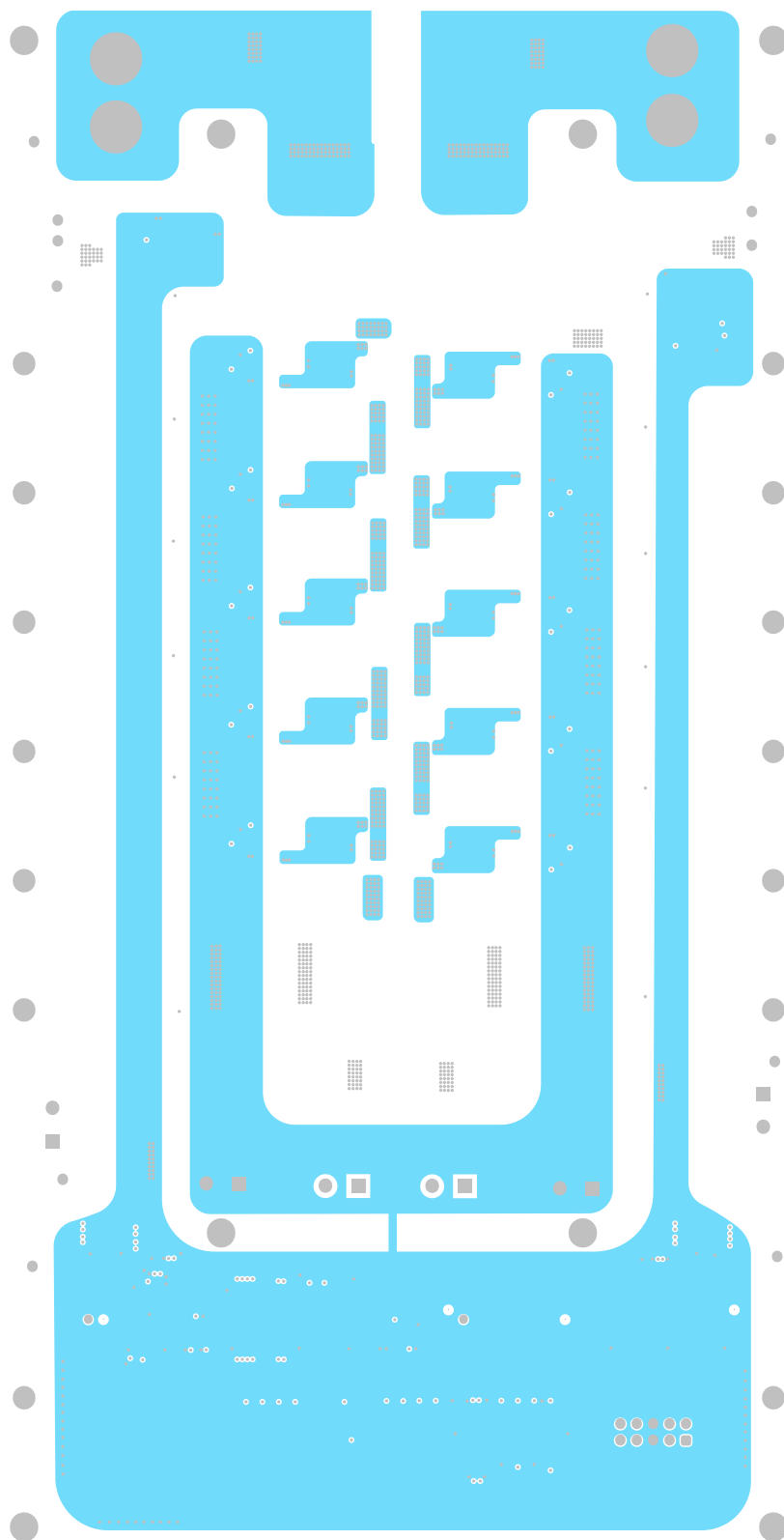


Figure B.10: Second inner layer of PCB.

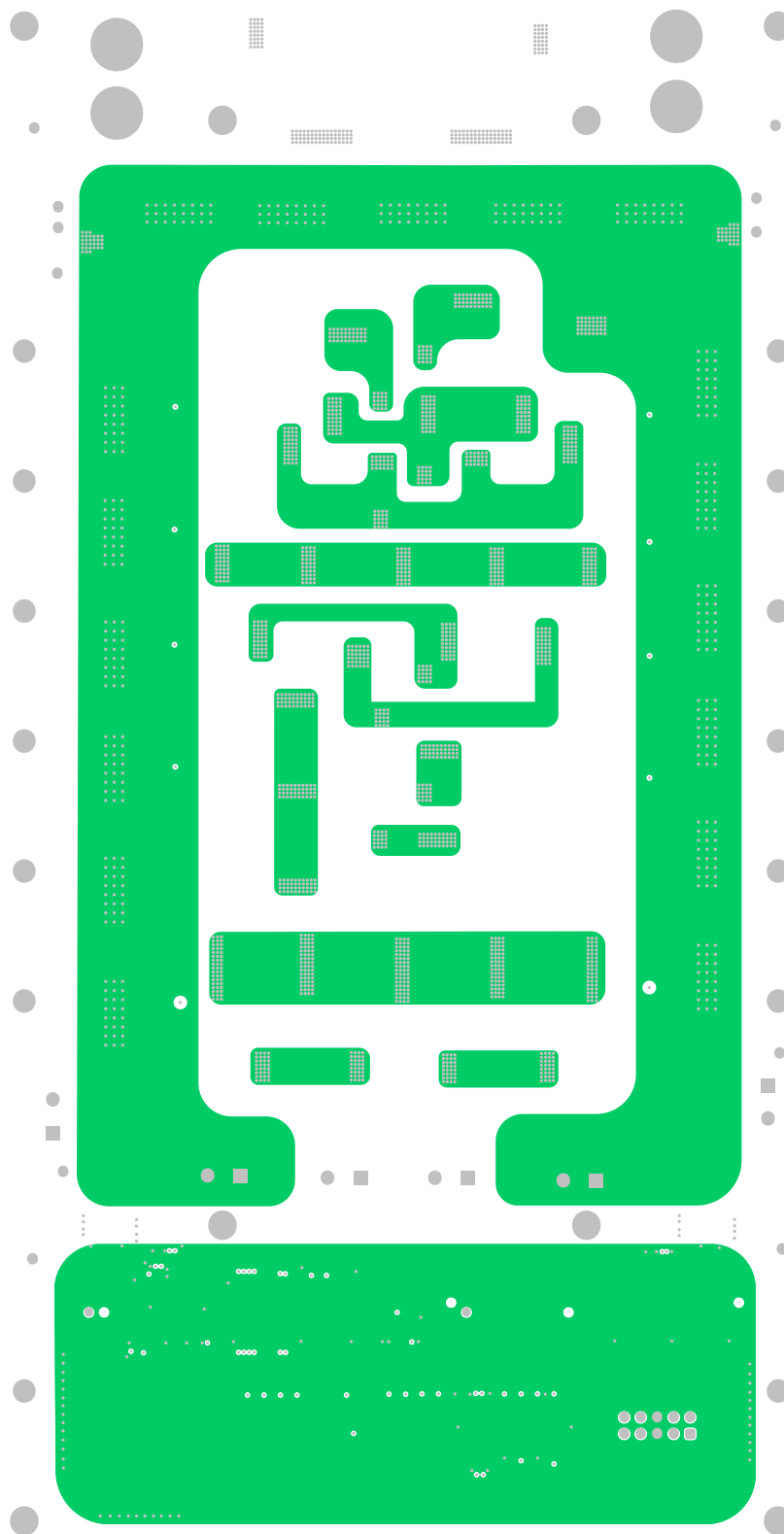


Figure B.11: Third inner layer of PCB.

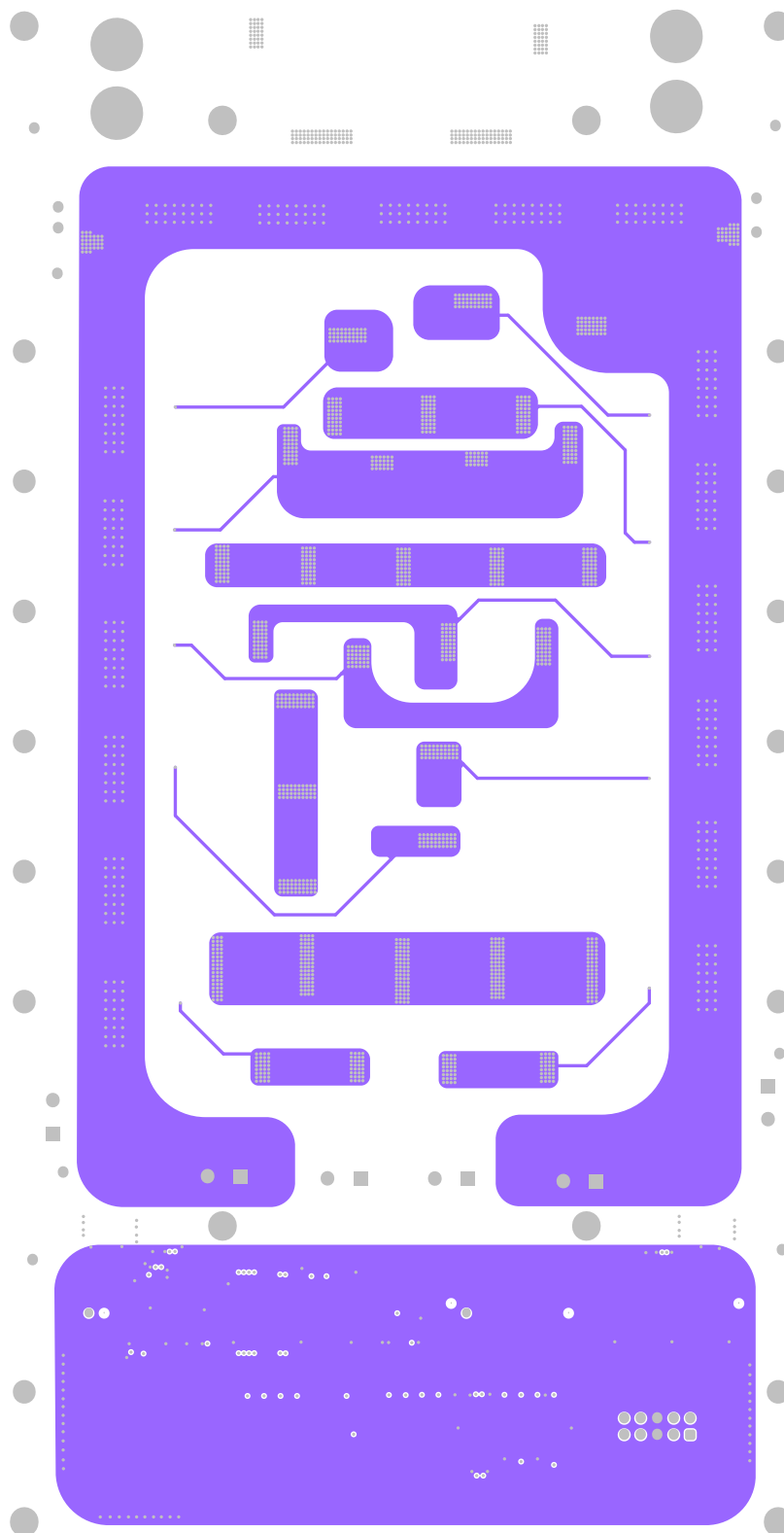


Figure B.12: Fourth inner layer of PCB.

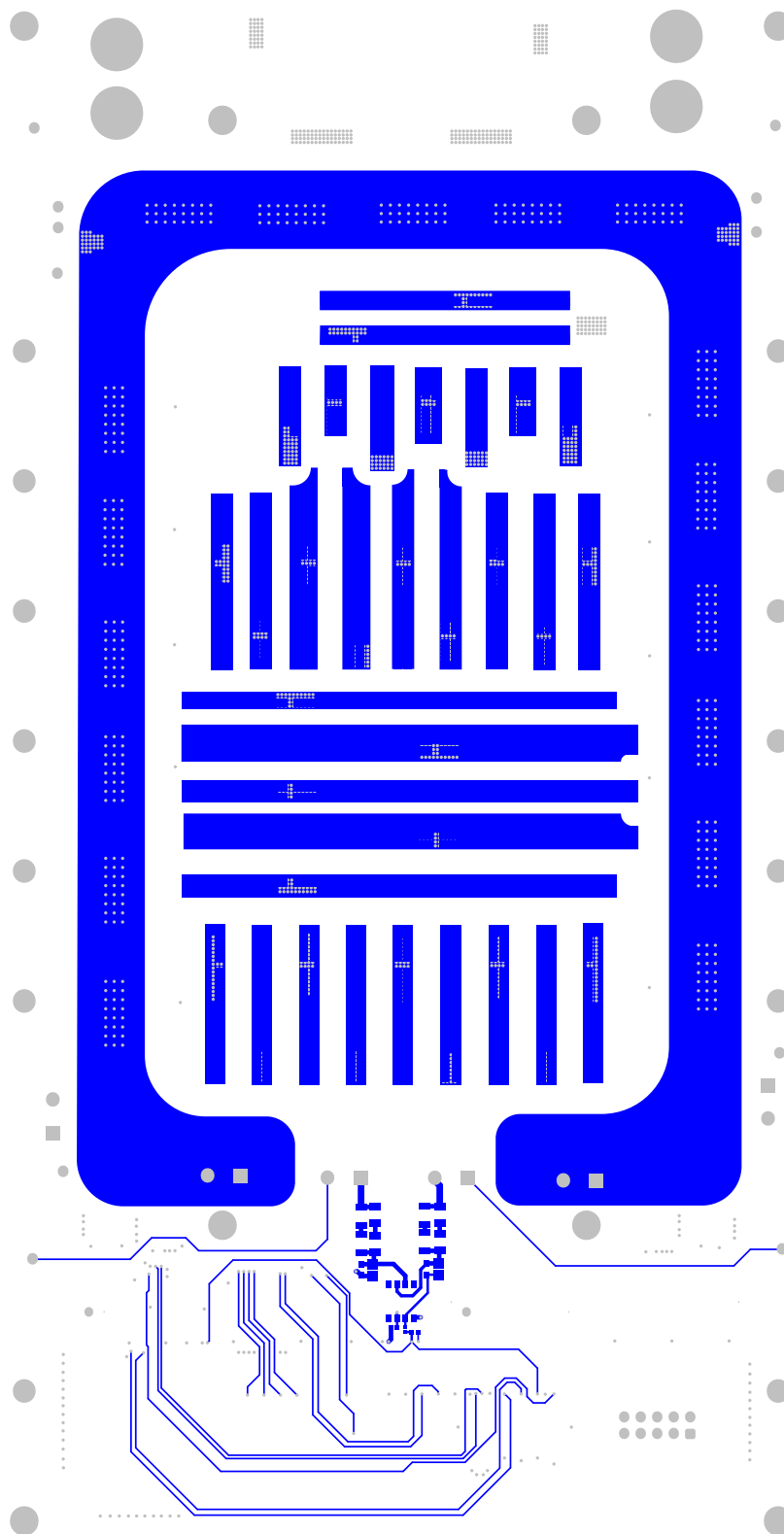


Figure B.13: Bottom layer of PCB.