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Schottky-Diode-Based Wake-Up Receiver and Power Management Systems for IoT Applications

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Schottky-Diode-Based Wake-Up Receiver and Power Management Systems for IoT Applications

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical and Computer Engineering

by

Mahmoud M Rashad Ibrahim Elhebeary

2020

ABSTRACT OF THE DISSERTATION

Schottky-Diode-Based Wake-Up Receiver
and Power Management Systems for
IoT Applications

by

Mahmoud M Rashad Ibrahim Elhebeary
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2020
Professor Chih-Kong Ken Yang, Chair

Internet of Things (IoT) has recently become a crucial technology in our daily lives that has applications ranging from managing airports' passenger flow to taking care of the elder. It aims at connecting all appliances and products to create a vast network of applications. An IoT system is composed of leaf nodes that collect data from different applications which then transmit the data to a gateway or hub and eventually for storage and processing in the cloud. Battery life is a key bottleneck for leaf nodes that are either mobile or distributed without a fixed power connection. In order to communicate with a very low power budget, wake-up receivers (WuRx) that are part of a power management unit are needed in order to extend a device's service period.

While several approaches to wake-up a leaf node is possible such as using a watchdog timer that periodically and systematically wakes up the device, this work, we target leaf nodes with high throughputs and accessed in an asynchronous manner by a centralized hub. Such a WuRx imposes specific challenges including low wake-up latency, high data rate, good sensitivity, and ultra-low power budget targeting a battery life >10 years. Existing designs do not satisfy all challenges for the WuRx system or the battery power management efficiencies at such low power. Hence, we propose a new WuRx technique with the sub-microwatt power management unit that significantly bridges the gap between the required

and achievable performance. New integrated circuit techniques are implemented in CMOS chip such as building Schottky diode on CMOS, a novel data-locking oscillator technique, and a digital correlation unit to identify signatures from the hub.

Existing solutions for low voltage regulation suffer from low power efficiency especially with load currents that transitions from nano-watts to milli-watts. In this dissertation, we first propose a two-stage hybrid power management unit (PMU) that employs a highly-efficient novel ON-OFF LDO as the second stage and uses a switched-capacitor dc-dc divider as the first stage. This design is then enhanced to operate across a wide range of loads from sub-microwatt to 100's of microwatts by using selectable sizing of its switches to improve efficiency to >95% across the target range of load current. The output voltage that is divided from the first stage is then regulated using the proposed ON-OFF LDO with a dropout voltage of <30mV. The hybrid architecture regulates battery voltage to 0.4V and achieves a power efficiency of >85% for the wake-up receiver as the load.

Lastly, when the main transceiver receives the wake-up signal, it requires a short time for settling so that it communicates the necessary information to the gateway quickly. The main transceivers consume in order of 10s of milli-Watts which is regulated through an LDO. Existing solutions could not provide short settling with small overshoot for a fast start-up. We propose a novel LDO that uses a new Coarsely-Quantized Class-D control that enables wide loop bandwidth using a multi-level and pulse-width modulated (MLPWM) gate control of the output device. The flipped voltage follower (FVF) output stage is adopted with a feed-forward derivative path to limit overshoot/undershoot. The proposed LDO settles within 280ns when the load is stepped in 7ns from 0 to 300mA with no observed overshoot or undershoot.

The dissertation of Mahmoud M Rashad Ibrahim Elhebeary is approved.

Gregory Pottie

Danijela Cabric

Sudhakar Pamarti

Chih-Kong Ken Yang, Committee Chair

University of California, Los Angeles

2020

To my family

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PUBLICATIONS

M. Elhebeary and C. K. Yang, "A Class-D FVF LDO with Multi-Level PWM Gate Control, 280-ns Settling Time, and No Overshoot/Undershoot," in IEEE Transactions on Circuits and Systems I: Regular Papers, (In press).

M. Elhebeary and C. K. Yang, "A 92%-Efficiency Battery Powered Hybrid DC-DC Converter for IoT Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, (In press).

M. Elhebeary, L. Chen, S. Pamarti, and C. KenYang, "An 8.5pJ/bit Ultra-Low Power Wake-Up Receiver Using Schottky Diodes for IoT Applications," ESSCIRC 2019 - IEEE 45th European Solid-State Circuits Conference (ESSCIRC), Cracow, Poland, 2019, pp. 205-208.

M. Elhebeary and C. K. Yang, "An 85%-Efficiency Hybrid DC-DC Converter for Sub-Microwatt IoT Applications," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 2019, pp. 9-12.

CHAPTER 1

Introduction

Internet of Things (IoT) aims at connecting appliances and products embedded within our environment that would then gather a broad scope of information to be used to enhance our ability to respond to the environment or for our environment to respond to us. In addition to any individual's normal daily life, the applications include numerous specific fields such as agricultural, medical, manufacturing, automotive, etc. Fig. 1.1 shows the basic hierarchy of how leaf nodes are connected in a system. Leaf nodes collect data and transmit the data to a gateway through a handshaking protocol, where it only transmits the data to a gateway that may have limited availability. The gateway may be mobile such as a quadcopter that only passes once in a while over the group of sensors in a remote location or a fixed transmission unit that sends the broadcast signal to collect data from nearby leaf nodes. The data collected then is uploaded to an IoT cloud where it's analyzed and processed to forecast and analyze different phenomena.

IoT leaf nodes are extremely sensitive to energy dissipation as it directly corresponds to their deployment lifetime. Not only do they need a low-power means to monitor the environment for an activation signal, but they also need to draw little total energy from an energy source such as a battery or supercapacitor while reacting to activation. This dissertation demonstrates both with a wake-up receiver that draws less than 4.2μA of current from a 0.4V source and a power management unit that achieves 85% efficiency at such low currents while achieving a fast transition to higher current load and maintaining efficiency.

1.1 Motivation

In this work, we focus on the design of leaf nodes with a limited source of energy, i.e. battery-powered and limited energy harvesting. The leaf node structure is shown in Fig. 1.2 composed of the following: a wake-up receiver to sense the channel and wake-up the high power radio when the predefined signature is being asserted, a high-sensitivity transceiver which is always sleeping and only wakes up when the wake-up receiver sends a signal. A power management unit that regulates the battery voltage to multiple voltage levels for the ultra-low-power wake-up receiver and high-power blocks on the chip. The leaf node is battery powered and should have a lifetime of >10 years. Thus minimizing average power consumption from the battery is the main concern for the system specifications.

Due to the limited power budget, a wireless data transceiver of the leaf node cannot be always on. Instead, a very low-power wake-up receiver that is always on and monitoring a specific frequency spectrum awakens the primary data transceiver should a signature be detected. For targeted real-time applications, low latency is critical specification as the gateway will be available only for a short time, this leads to high data rates required for the primary data transceiver and fast power management unit chip for fast wake-up <1ms. A highly effi-

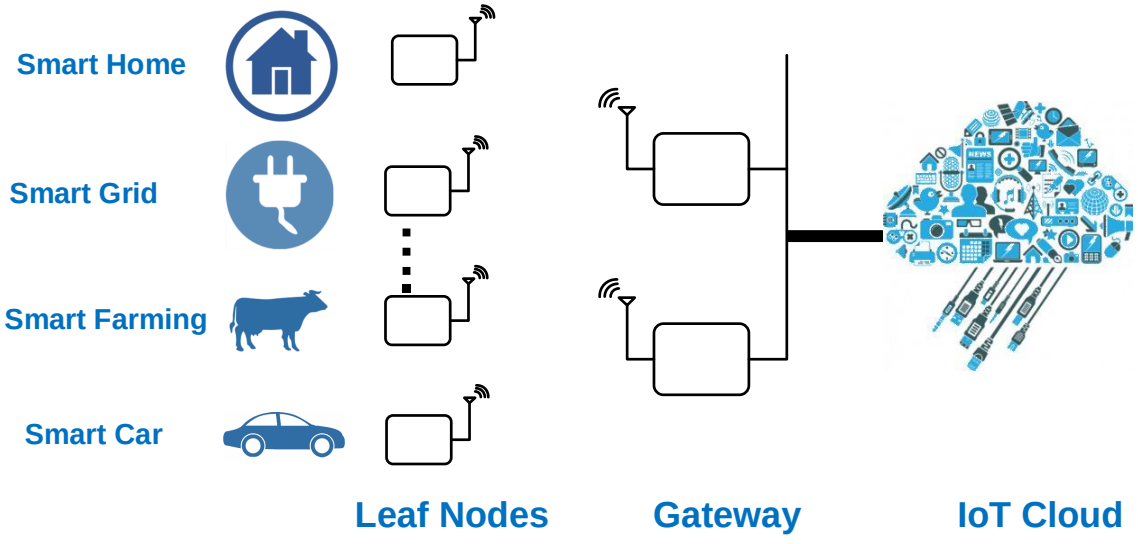

Figure 1.1: IoT nodes top-level structure

cient wake-up receiver is achieved by combining two techniques: a Schottky diode front end that is optimally biased for low energy/bit, and a two-phase wake-up technique which further lowers the quiescent operating power when no data is sensed on the channel by turning off the second phase. Therefore, the energy efficiency of the WuRx is optimized on both the circuit level and the architectural level. On the circuit level, we propose a low-power CMOS Schottky diode as a power detector consuming only 18% of total power, while providing sufficient bandwidth, compared to >35% in prior publications. On the architectural level, the proposed two-phase architecture reduces the average power consumption further by 12% by activating the second phase only in case of detection of the data stream in the channel. For the given latency specification along with the battery capacity of 800mAh, this would limit the wake-up receiver power budget to $<2\mu$W. Thus allowing the battery-operated leaf node to operate for >10 years. This work consumes low power of 1.69μW at 200kbps resulting in sub 9pJ/bit with normalized sensitivity of -103dB which compares favorably with prior

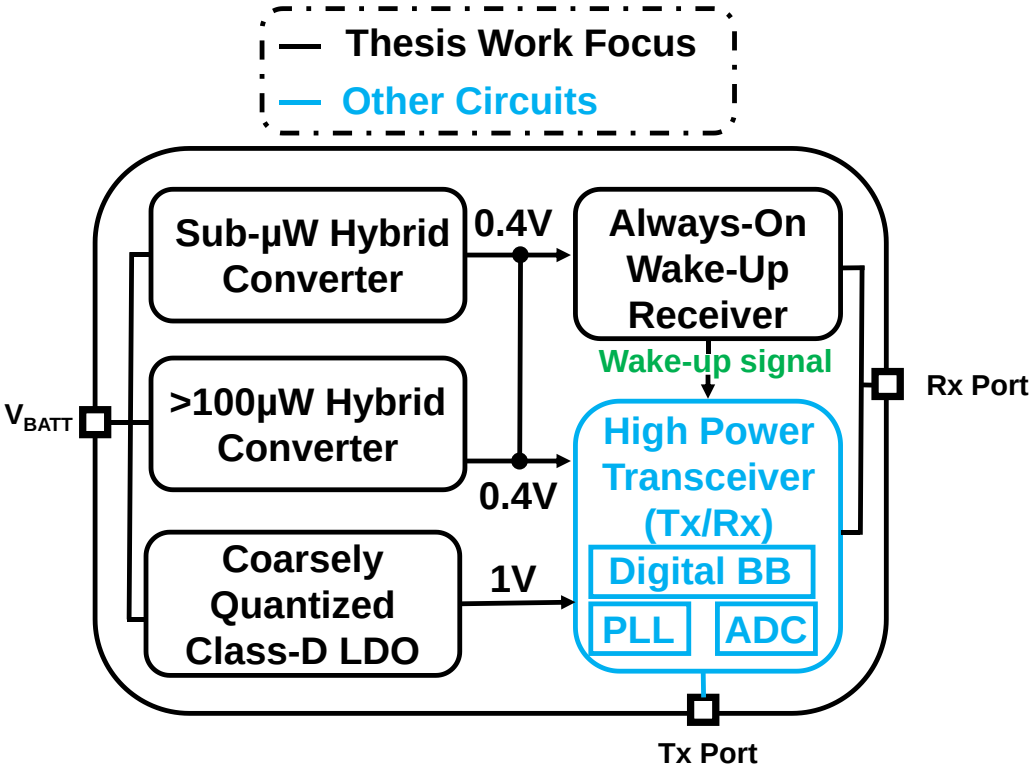

Figure 1.2: Leaf nodes architecture and Thesis work focus

publications as shown in Fig. 1.3. To operate with such strict power consumption, the low supply voltage is adopted for sub-threshold operation.

An efficient power management unit is a critical component of the leaf nodes. First, the wake-up receiver circuit requires a high power-efficiency regulator. The regulation overhead for such low loads is often poor and degrades the overall life-time of the leaf node. The power management unit (PMU) furthermore needs to achieve high power efficiency at low output ripple levels. Since subsequent stages are turned on after wakeup, the PMU must handle a wide range of load current and continuous output voltage levels, not just discrete predefined levels. Multiple power management solutions are explored including low dropout regulators and switched capacitor dividers. LDO achieves continuous output level and low ripple levels, however, it has low power efficiency. For switched capacitor divider, it can achieve high power efficiency, however, it can not provide continuous output voltage levels. We combine the merits of both approaches and implemented a hybrid converter for low voltage supply generation. The hybrid converter achieves high power efficiency exceeding 80% at low power loads and across wide load range while regulating output voltage at

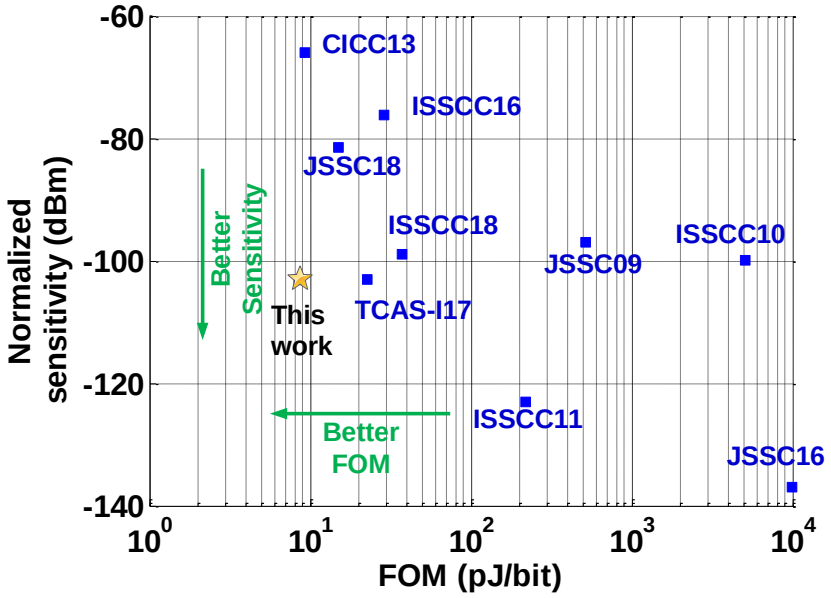

Figure 1.3: Wake-up receiver normalized sensitivity versus FOM for prior publications

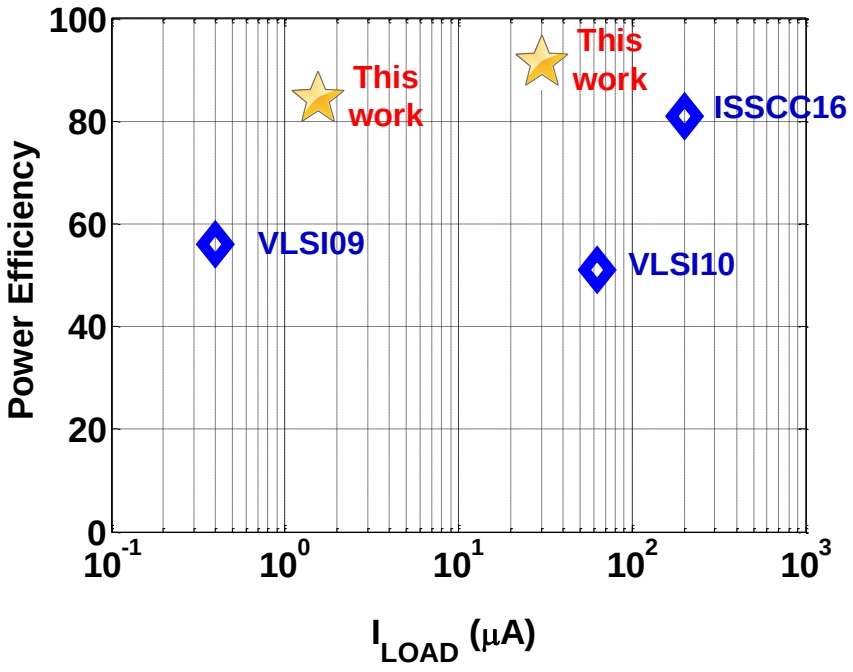

Figure 1.4: Power efficiency versus load current of prior work

0.4V. The first stage is a switched-C divider with a fixed 3:1 divide ratio and achieves an efficiency of 97%. Similar to prior literature, a larger input voltage range can be supported by selecting different division ratios. This work introduces an LDO second stage that uses an all-digital ON-OFF controller that uses small quiescent current to maintain an overall efficiency of >85%. The LDO provides a regulated output voltage with a dropout voltage of 30mV and leverages the output capacitance to suppress the ripple to less than 10mV. To maximize efficiency, we jointly optimize both stages so that they share the same clock signal. Also, a system-level switching between different configuration is proposed to increase the range of load currents that the at which efficiency is optimized to supply the required power for additional blocks that are turned on. Figure 1.4 shows the power efficiency of the hybrid power management unit compared to prior work. One final challenge in the power management of leaf nodes is the high power radio regulation. When different load ranges switch to the high power mode, it requires fast settling, low overshoot supply regulation since it wakes up for a short period.

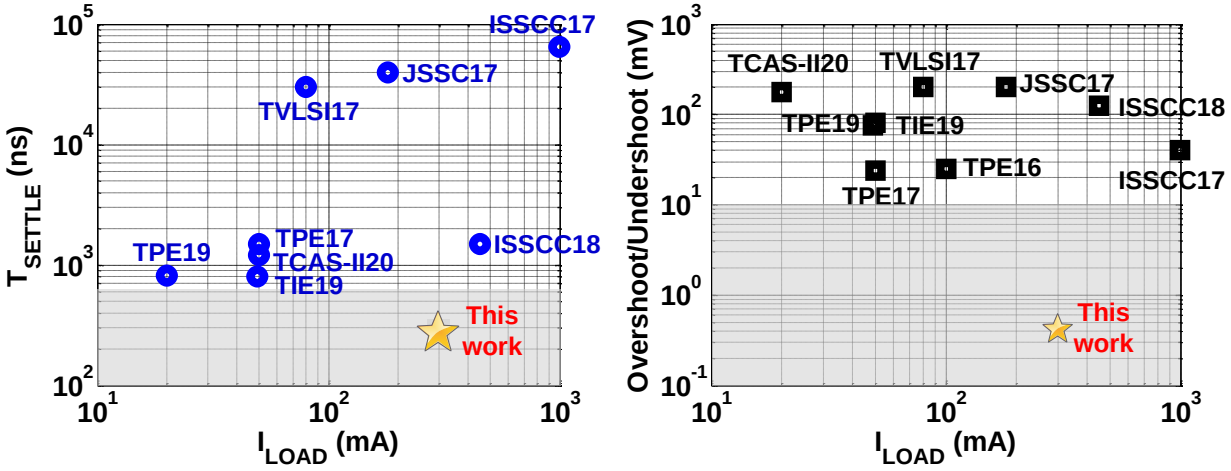

Figure 1.5: Settling time and overshoot/undershoot versus load current of prior work

For the fast transient response regulation unit, we present a novel Coarsely-Quantized Class-D LDO that provides a regulated output voltage at 1V for the main-radio. The main motivation behind this work is to achieve fast transient response in case of fast load change along with short settling time. To achieve these system specifications, we introduced a novel gate control scheme for the output stage. In this control scheme, we decoupled the control path from the power path, hence allowing fast loop control over sudden changes at the load. Also to sense these sudden load changes and to stabilize the output ripples within a small time, we introduced a feed-forward path that acts as a derivative path for the control signal. These techniques helped in achieving fast settling time(i.e. 10x lower compared to same load changes in the prior art) and no overshoot or undershoot(i.e. only static load regulation due to load increase) as compared to prior work as shown in Fig. 1.5. The proposed LDO achieves settling of 280ns for load change of 300mA with an edge time of 7ns. The LDO shows no-overshoot or undershoots at fast transient load changes that resemble digital core switching, hence it can be of benefit to operating digital core circuits.

1.2 Thesis Organization

The dissertation is composed of seven chapters. In Chapter 2, we begin with background information on the thesis two main contributions. First, we cover the different ways of implementing wake-up receivers and also covers different approaches for always-on wake-up receivers and power, sensitivity trade-offs. Second, we highlight the different approaches to implementing power management for leaf nodes. Also, we provide the system specifications requirements for ultra-low-power generation along with different load range-switching resulting in the need of fast transient regulator.

The main contributions of this dissertation can be split into two parts. The first part discusses the wake-up receiver of power limited leaf node, whereas the second part discusses the power management solutions for the leaf node. In Chapter 3, we present the implementation of an ultra-low-power wake-up receiver for high throughput applications with asynchronous communications. We propose a CMOS Schottky diode used as an energy detector for better detection with low power cost. For reducing the overall power consumed of the wake-up, we divided the system into 2 phase which saves 12% on average. Also, we propose a data-locked oscillator as the second phase of the wake-up system to avoid the usage of bulky crystal oscillators. We also show circuit implementation and system analysis of the system.

The second part is discussed in Chapters 4 and 5, where we discuss power management unit implementation which comprises of the hybrid DC-DC converter and Coarsely-Quantized class-D LDO. In Chapter 4, we discuss the power management solution to operate the WuRx at the low supply of 0.4V while achieving power efficiency exceeding 80% for low load below 2μW. We show the system implementation of a wide load (0.8μW-100μW) of the hybrid DC-DC converter. The wide load coverage is achieved through system-level switching to improve power efficiency across the whole range. In Chapter 5, we present a novel class-D flipped voltage follower (FVF) low-dropout (LDO) regulator. The system is enabled after the wake-up system asserts the wake-up signal to the main transceiver. This binds the system startup and settling time to provide a high load in a short time. The system implementation and system analysis are presented in the chapter along with stability analysis.

The proposed LDO is modeled as and provided a linearized stability model to show different system parameters. The implementation responds to load changes from 0-300mA in 7ns with no observed overshoot/undershoot and can operate down to 10mV dropout voltage.

Multiple test-chips were built as part of this dissertation to validate the various design approaches. Chapter 6 shows the experimental measurement results for each of these experiments as follows. First, we present the wake-up receiver chip fabricated in CMOS 65nm. Second, we present PMU chips fabricated in CMOS 28nm (2 chips for different load ranges). Third, we present the Class-D LDO chip fabricated in 28nm. Chapter 7 concludes the work, lists the contributions, and offers some ideas for future work.

CHAPTER 2

Background

This chapter provides a brief overview of the different issues of limited power leaf node design. We focus on the background of the thesis main contributions in the wake-up receiver and the power management for the leaf node. First, we review the different implementations of the wake-up receiver which are the duty-cycled or the always-on. Then we will discuss in detail the always-on wake-up receiver architecture which is compatible with our targeted application. We show different trade-offs of sensitivity, latency, and energy per bit cost for each of the different approaches. Then we discuss the trade-offs of the envelope detector based wake-up receiver and the power management challenges at low voltage and power levels. Also, we discuss the challenges of operating the wake-up receiver at low voltage, and quiescent current would require high power efficiency regulation which is challenging at these levels.

Second, we review different approaches for voltage regulation and the trade-offs at low power levels. The Wake-up receiver system consumes low power is a challenging problem to achieve high power efficiency. After the wake-up signal is asserted, the high power radio wake-up with low latency which requires stable supply. We discuss the different topologies of LDOs to supply the high power radio and the trade-offs between analog, digital, and the proposed class-D LDO. This discussion is important to understand the challenges in limited power leaf node implementation.

2.1 Wake-up Receiver

2.1.1 Low-power radios

Low power radio becomes a critical component in leaf nodes since it forms a large portion of the power used. Since the power consumption of the receiver chain used in the unlicensed band is relatively high. Different approaches have been implemented to reduce the average power consumption in these sensor nodes which are divided mainly into two approaches. The first approach is suitable for sensor nodes that are characterized by long idle periods and burst mode reception and transmission of data. Figure 2.1(a) shows a duty-cycled receiver approach which is a common way in 4G transceivers [1], [2]. In the sleep mode, lower power consumption for the sensor node is required since it is almost >90% of the time. The following equation shows the average power consumed for the wake-up receiver.

$$P_{avg} = \frac{P_{slp}t_{slp} + P_{on}t_{on}}{t_{slp} + t_{on}} \tag{2.1}$$

So the on time will decide the average power consumed by the wake-up receiver. Also, the system is required to wake-up at low power cost and allow higher power circuit components to operate through the transmission and reception phase. This approach requires a precise clock and fast startup oscillator to minimize its on-time detection phase. This approach trades-off power with the periodicity which can lead to slow response and long latency.

The second approach is to use a low-power wake-up receiver system that is always on and constantly listen to the channel. In this approach, the high power receiver is on sleep mode unless a wake-up signal is received from the always-on wake-up module. The wake-up system consumes low power and sacrifices high sensitivity compared with a high power receiver. The wake-up system detects certain data sequence and enables the high power receiver to allow higher data rate transmission and higher sensitivity. Figure 2.1(b) shows the data sequence which starts with the transmitter sends a preamble sequence, so the wake-up receiver receives this preamble and enables the operation of the high power receiver. Then the high power receiver sends an acknowledgment reply to establish a communication channel with the transmitter. Finally, the transmitter sends data to the receiver and the

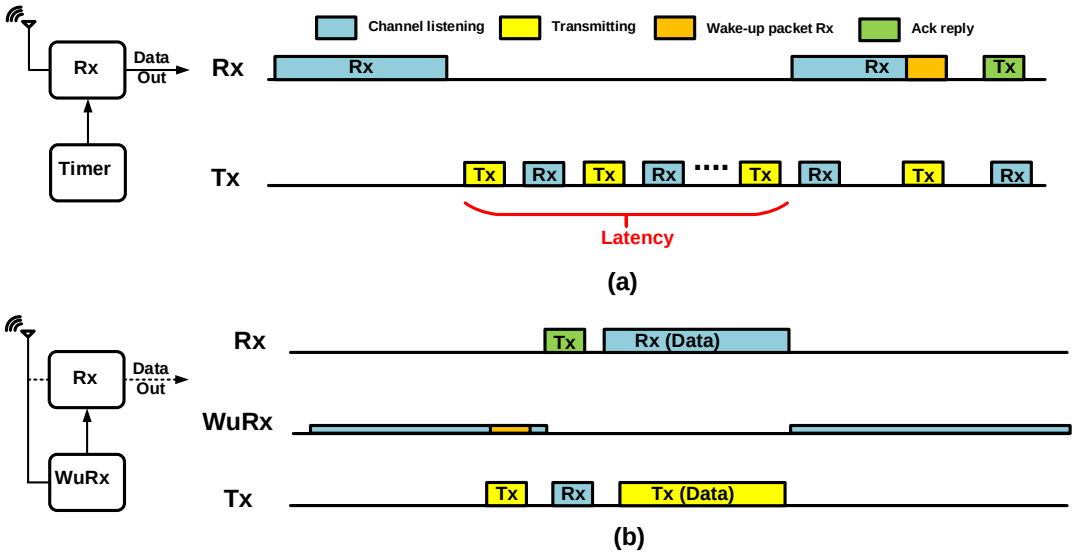

Figure 2.1: (a)Periodically wake-up receiver (b)Always-on wake-up receiver.

receiver goes back to sleep again. The challenge is maintaining minimal energy per bit of the always-on receiver with the required data rate for different applications. In this thesis, we will emphasize the implementation of the second approach with more details about different architectures and design details.

Different parameters are used to define the figure of merit for wake-up receivers. In the next section, we will show the main parameters used for different approaches and their impact on the overall power consumption and the overall latency of the system.

2.1.1.1 Battery life

Battery life elongation is the motivation for this work. For billions of sensor nodes required to sense physical phenomenons and provide reliable data for the life-time of more than 10 years. For a given data-rate requirement, the power consumption of the receiver is optimized to elongate the battery life. This is done by having duty cycling of the receiver system with small on-time to lower the average power consumption. Other approaches use an always-on wake-up receiver to put the main receiver always on sleep and have an ultra-low-power wake-up receiver to always listens to the channel. Another way of elongating the battery life

is to integrate it with energy harvesting as auxiliary power source [25]-[26].

2.1.1.2 Wake-up latency

The wakeup latency is an important factor for the wake-up receiver design. Since the gateway can be only available for a few minutes per data collection as well the power limitation over the gateway which requires a short time to accommodate the data transmission. Different applications have different wake-up latency requirements ranges 250μs to 10ms [24]. To achieve the lower end of the wake-up latency, the system is required to run at a data rate of >50kbps [9]-[17]. Thus imposing high quiescent current used in baseband amplification circuits compared to low data rate <1kbps. From which we can see that energy per bit is considered the main parameter to compare different wake-up receivers with different data rates.

2.1.1.3 Probability of false alarm

The probability of false alarm is defined as the false wake-up for the main receiver given that the correct signature is not detected. This can happen due to the noise in one of the following two scenarios. First, the noise is high enough to invert "0" to "1" and it coincides with the predefined pattern. Second, another pattern sent and the noise changed it to the correct pattern. This will result in unwanted wake-up of the main transceiver which consumes in the order f few milli-watts, hence, resulting in battery life degradation. Typically, the probability of false alarm is required to be sufficiently low i.e. $< 10^{-}4$ so that the power consumption of the overall leaf node kept within the power consumption of the always-on wake-up receiver.

2.1.1.4 Probability of detection

The probability of detection is defined as the detection rate when the correct signatures are sent over the channel. The missed detection rate is the complement of the probability of detection and it is set at $10^{-}3$, which puts the probability of detection at 99.9%. The gateway can further relax the specification over the probability of detection by having mul-

tiple transmissions (i.e. example 5 times) which put the requirement over the probability of detection for the system to be 66.5%. This would further relax the design of an energy detector minimum signal to noise ratio.

2.1.1.5 Energy per bit

The basic figure-of-merit for the wake-up receiver is the energy per bit cost, which is calculated by dividing the average power over the data rate. Wake-up latency plays an important rule in the choice of the data-rate thus affecting average power consumption. However, for base-band circuits the bandwidth is directly proportional to the current consumption (i.e Bandwidth BW=g_m/C_L, where $g_m \propto I_{SS}$), where I_{SS} is the bias current. Thus more power is required as data rate increases. Which is also applicable for digital circuits in the system and base-band clock generation. Since the power is P=$Cf_{clk}V_{DD}^2$, which shows higher power levels at higher data rates. Different wake-up receiver architectures target improving the energy per bit cost along with maximizing the system sensitivity.

2.1.1.6 Sensitivity

Sensitivity is defined as the minimum detectable signal which the radio can sense. It sets the distance range of detection as well as the transmitted power to accommodate the medium losses. For a receiver, the sensitivity is the goal of improvement for a given data rate. For receivers, the sensitivity improvement comes at the expense of power consumption by using high power low noise amplifiers (LNA) to amplify the signal at pass-band. Other approaches use a mixer as a front-end to lower the power consumed on the expenses of the receiver sensitivity. Also, the bandwidth in RF and the filtering lowers the total integrated noise and improves the overall sensitivity. For a receiver, the sensitivity can be expressed as:

$$P_{sen} = NF_{Rx} + 10logBW - 174 + SNR_{min} \tag{2.2}$$

2.1.2 Always-on wake-up receiver

Always-on wake-up receivers can be categorized into 3 main architectures as shown in Fig. 2.2. The first architecture is a superheterodyne mixer which is first introduced in [3]. This architecture is a mixer based architecture that achieves a 52μW power. It operates from a 0.5V supply and achieves high sensitivity of -72dBm. The power consumption in this approach is a function of the frequency of operation since the oscillator consumes the largest power portion. This approach achieves good interference rejection which is required in many applications. However, the high power consumed in the local oscillator and mixer power sometimes limits its usage for long-life battery-based applications. Different implementations followed that one and achieved higher sensitivity and different bands of operation as in [4]-[7]or even used different modulation schemes as FSK as in [8].

The second architecture is a conventional tuned RF. This architecture uses LNA in the front-end to achieve high sensitivity. This architecture amplifies the low power input signal and then passes it over the envelop detector to decode the data sent. The signal after the envelop detector is in baseband and can be amplified using a low power baseband amplifier. This approach is used [9]-[10]. In [10], the power dissipated in LNA forms 66% of the total power dissipated in the circuit of 23μW. This power consumption for LNA at 900MHz frequency would be much higher if the 4G band was targeted or Wi-Fi bandwidth. This architecture achieves -78.5dBm due to the use of LNA at the front-end. In [8], the LNA also forms 55% of the total power. Even without the LNA and having the detector circuit in the front-end, this architecture would still consume relatively high power >20μW resulting in high Joule per-bit cost.

The third architecture used the square-law detector as the front-end. The square-law detector can be in the form of NMOS in the sub-threshold region with bias current as in [12]. Using NMOS in sub-threshold as in [11], achieved sensitivity up to -69dBm with a data rate of 300bps but in the expenses of bandwidth and start-up latency exceeding 100ms. The power consumption is 4.2nW in the expenses of the data rate which consequently reflects on the energy per bit cost at 15pJ/bit. Other architectures used voltage rectifiers using diode-

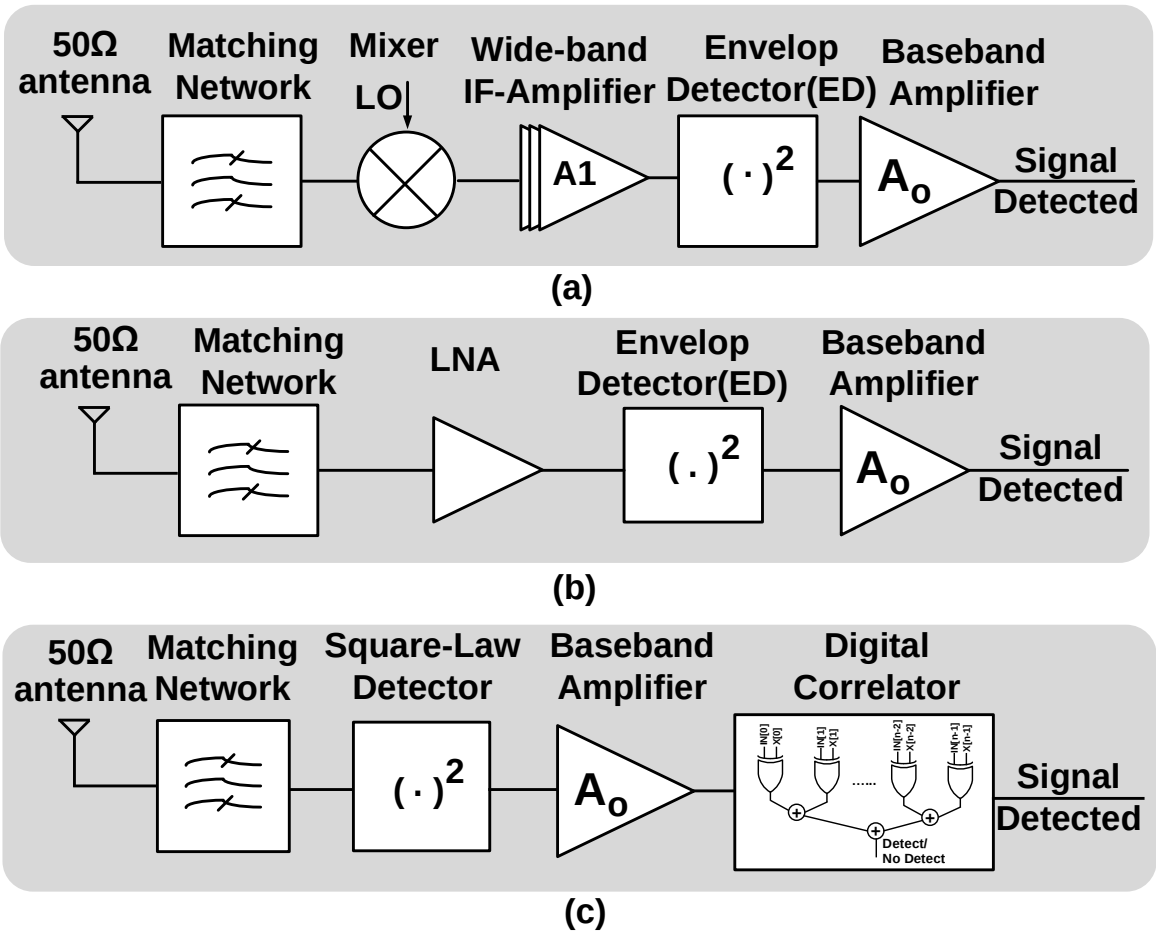

Figure 2.2: (a) Conventional IF/Uncertain-IF Superhetrodyen WuRx (b) Conventional tuned RF WuRx (c) square-law detector based WuRx.

connected transistors as in [13], [14]. These architectures trade-off the bandwidth (data rate) and power consumption. Other approaches uses off-chip components for the wake-up operation as in [15], [16]. In these approaches, the wake-up receiver can work at a maximum frequency of 1GHz with high power consumption and low data rate transmission of 1kbps.

The proposed always-on wake-up receiver is presented in Chapter 3. Also, we discuss the evaluation of the architecture through the different figures of merits (FOM). Published techniques have used sensitivity, power, data-rate, latency, and carrier frequency as ways of comparison. Wake-up receivers are used mainly in two kinds of applications, (1) high latency with high sensitivity requirement [12] (2)low-latency with moderate sensitivity required[17].

An example of low-latency and moderate sensitivity is the health care devices that use wireless body area network (WBAN) are located at short distances from the body requires data rate ranges of 100's of kbps and low sensitivity of -40 dBm. The power constraints for such devices are high since battery replacement is extremely difficult, so it must operate under 2μW to achieve reasonable battery life.

2.2 Power Management Unit for IoT Application

Power management of leaf nodes consumes large power overhead. In this thesis, we will focus on two main design challenges for supply regulation. First the voltage regulation of the low power-low voltage loads as in wake-up receivers. Second, the fast settling regulators for the main receiver when it starts-up. There are different design parameters for power management systems. We will focus mainly on power efficiency, load transient, voltage overshoot and undershoot, and settling time.

2.2.1 Wide range hybrid DC-DC converter

Battery-powered systems have used several options to down-convert and regulate supply voltages at low power levels. Buck converters are a common architecture in step-down voltage converters for high power regulations that target 100s of milliwatts. Due to the large overhead associated with its control [32] along with the inductor size, buck converters are not good candidates for low power applications. Low dropout (LDO) regulators [33], [34] provide high supply rejection and regulated output voltage. However, this approach results in poor power efficiency. For example, a regulated voltage at 0.4V from a battery output at 1.3V would have a maximum efficiency of η=30% under the assumption of no quiescent current as per Eq. 2.3

$$PE = \frac{V_{OUT}}{V_{IN}} * \frac{I_{OUT}}{I_{IN}} \tag{2.3}$$

Where V_{OUT} is the output voltage, I_{OUT} is the load current, V_{IN} is the input voltage,

and I_{IN} is the current drawn from the input voltage.

Another approach is to use a switched-capacitor dc-dc converter which has power efficiency up to 97% [35]. However, switched capacitor designs typically only divide the input voltage and does not provide any supply rejection or regulation. A hybrid architecture [36] has been shown where the first stage divides the battery voltage by five using a switched-capacitor dc-dc converter. The design then uses an LDO in the second stage for output voltage regulation. This system provides an efficiency of up to 56% at low loads. However, the work suffers from a high voltage ripple of up to 50mV at the output and can only operate across a narrow range of load. Other two-stage approaches include using multiple switched-capacitor dividers with feedback to sense the output voltage and control the divider's ON-time to deliver achieve regulation. The approach has been shown to achieve maximum

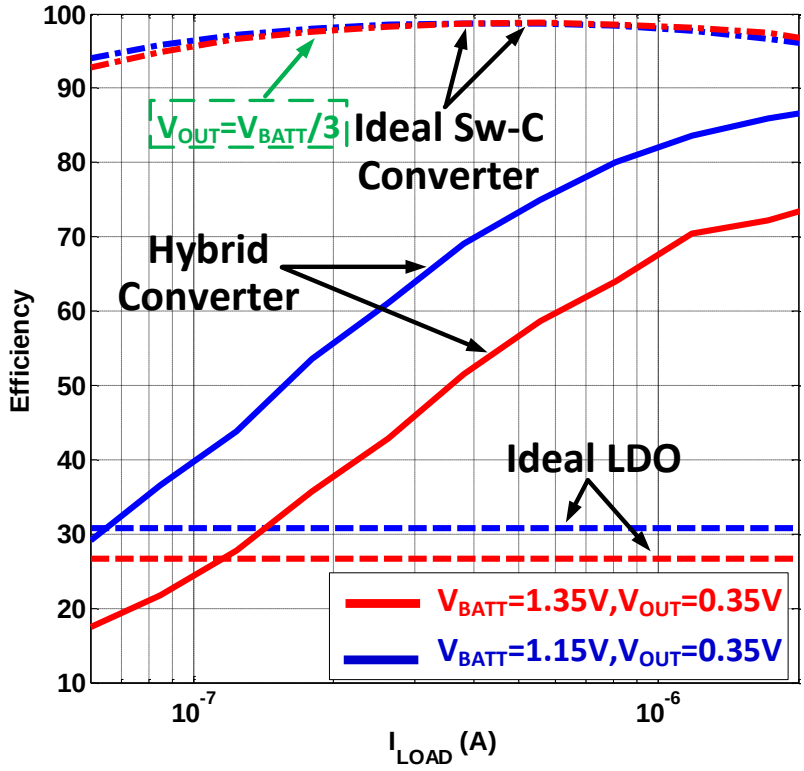

Figure 2.3: Efficiency for ideal switched-C, ideal LDO and proposed hybrid converter at different supply voltages.

efficiency of 70.4% [37]. Hybrid step-up converters are also used for energy-harvesting applications as in [38],[39], [40], and [41] in which the first stage is a boost converter or switched capacitor charge pump to boost the low input voltage, and the second stage is an LDO for output voltage regulation.

For the low voltage-low power regulation challenge, we propose a two-stage hybrid power management unit that can cover a wide load range through multiple phases of activation. Fig. 2.3 shows the efficiency comparison between the 2 approaches discussed in the literature and the proposed approach at low load which resembles the wake-up receiver circuit. The wake-up receiver is continuously ON and monitors the environment at power consumption. When a triggering event is detected, a higher power component is activated such as a radio to establish a communications channel. Ahead of this activation, the PMU activates another portion of the converter to provide efficiently the necessary power. The system then has additional tiers of activation which will require high power which can be fulfilled using class-D LDO proposed in Chapter 5. A battery's discharge characteristics [42] for such a system shows that over 90% of battery charge being utilized within the range of 1.4-1.15V [43]. The output voltage during the first two phases of operation of IoT application targets the range of 0.35-0.4V to power the always-ON wake-up circuit with up to a few μA of load current and power the low power radio with up to a few hundreds of μA of load current. Chapter 4 describes the proposed two-stage architecture in detail.

2.2.2 Coarsely Quantized Class-D LDO

After the startup signal is asserted by the wake-up receiver, the main transceiver is required to startup and perform the handshaking technique. The system activates then the LDO required for powering up the main transceiver unit. This restricts the startup time and the settling time for the regulated supply. The settling time of the regulated supply is defined by the time in which the output voltage is within a small range from the predefined reference. The sudden load increase change causes supply voltage to undershoot and long settling time. However, achieving low overshoot at fast load changes is challenging, as it requires wide loop

bandwidth often at the expenses of high quiescent current of 10mA as in [56].

For digital circuits of the main radio, another important specification for the supply voltage is ripple and overshoot/undershoot. The voltage overshoot/undershoot can not exceed 10% of the regulated voltage, otherwise, this will cause setup time and hold time violation for the system. An illustration is shown in Fig. 2.1 to show the overshoot/undershoot of the regulated voltage as well as the settling time of the output voltage to have a stable supply.

Several approaches have commonly been used in implementing LDO regulators. The most common is by an analog control loop as shown in Fig. 2.5(a). Such an analog LDO is chosen for high supply rejection and can achieve moderate overshoot and undershoot in transient load changes as in [57]-[61]. However, achieving wide loop bandwidth for fast settling affects the stability of the control loop across a wide range of loads and requires complex compensation of multiple loops. Improving the loop gain and achieving wider loop bandwidth improves transient response for the LDO as conceptually demonstrated in [62]

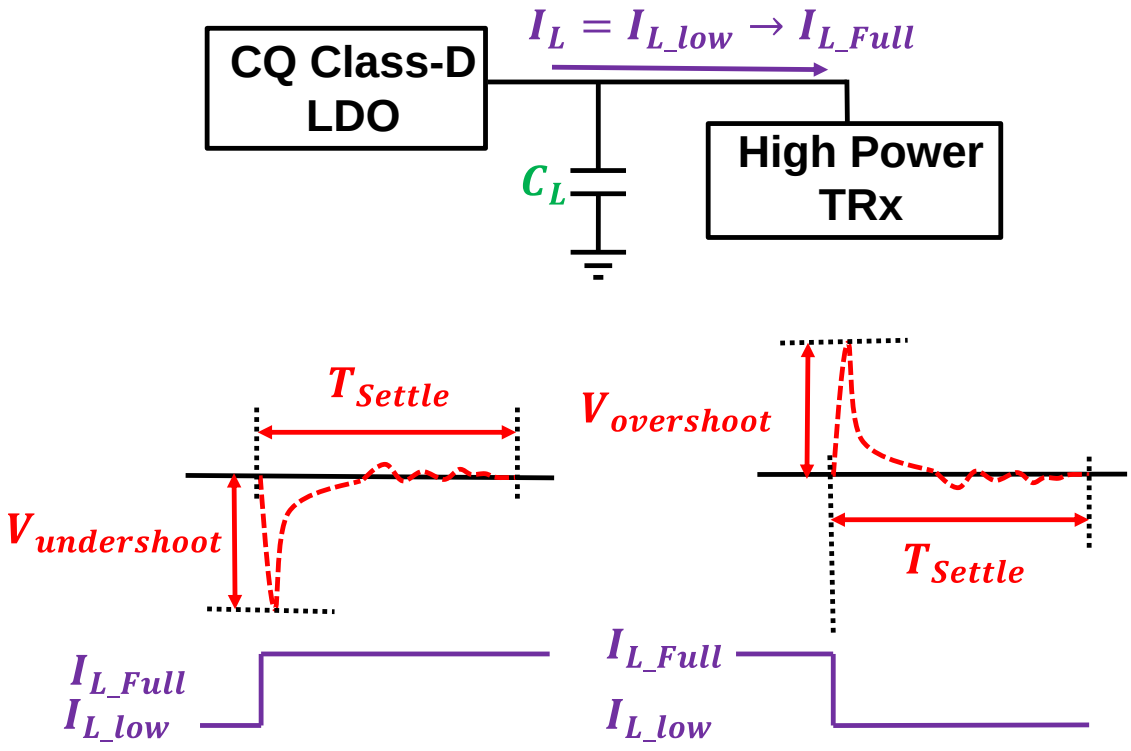

Figure 2.4: Transient response for load change for leaf node radio.

but is at the cost of the quiescent power of the controller and voltage headroom.

Digital LDOs [63]-[66], has more recently been shown to effectively regulate low output voltages and occupy a smaller layout area. However, it requires a minimum load current for proper operation and commonly exhibits large overshoots and long settling times with sharp load changes as shown in Fig. 2.5 (b). Variants of the digital LDO addresses some of these drawbacks by incorporating hybrid techniques of analog-assisted digital LDOs [67], [68] in which analog loops are added to digital LDOs to enhance transient response. However large overshoots/undershoots can still occur.

A conventional class-D control LDO has been proposed [69] in which the control loop comprises an analog amplifier which compares the reference voltage to the output voltage and accordingly controls a charge pump at the gate of the output stage with the corresponding pumping pulse width. In [69], the control loop's bandwidth is limited by the equivalent time constant at the gate of the output stage. Similar to an analog LDO, due to the bandwidth limitations, the work reports small ripple but has large overshoots (>40mV) and long settling times (>6μs).

For the fast start-up and setting challenge, we proposed a Coarsely-Quantized Class-D LDO as shown in Fig. 2.5 (c). We introduced a new method to control the gate voltage of the output stage using a multi-level pulse width modulated (MLPWM) signal and reduce the output stage's gate capacitance with the use of a flipped-voltage follower (FVF) output stage. This approach extends the loop bandwidth by pushing the dominant open-loop pole to the output node at the cost of voltage ripple at the output. We trade-off the number of quantization steps at the gate voltage with the desired ripple. A feed-forward transition detection path (FFTDP) is also introduced at the FVF output stage to substantially reduce the quiescent current. This design achieves no noticeable undershoot at 300mA/7ns load change and 280ns to settle at the required voltage. Chapter 5 discusses the proposed architecture for the novel LDO.

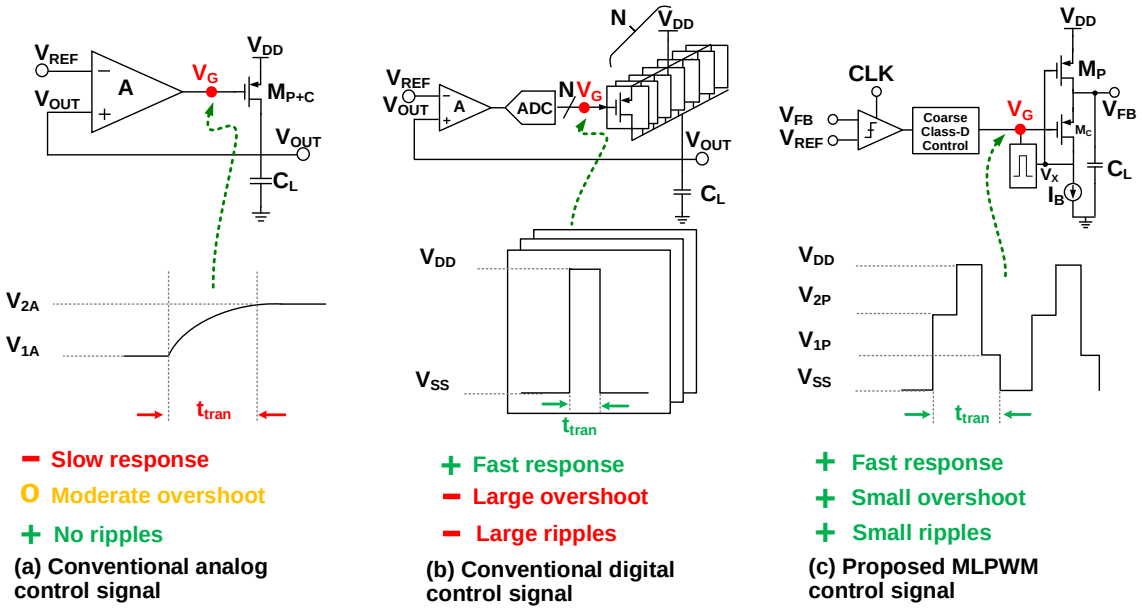

Figure 2.5: Conventional (a) analog and (b) digital control versus, (c) proposed MLPWM control

2.3 Summary

In this chapter, we showed the background of different approaches to building a low-power radio. We discussed different architectures of the always-on wake-up receiver and the trade-offs for different applications. We discussed the main parameters for wake-up receiver performance which will be further discussed in Chapter 3. Also, we gave a background for the power management challenges in leaf nodes. We discussed the hybrid converter challenges in achieving high power efficiency and the alternatives for low power regulation. Also, we highlighted the challenges in achieving fast startup regulation and the different architectures used in literature.

In the next chapter, we will discuss the system and circuit implementation of the proposed Schottky diode-based wake-up receiver system. We will show the analysis of using digital correlator and how it improves the probability of false alarm which improves the overall power consumption of the leaf node. Also, we will show the proposed architecture and circuit-level implementation of the wake-up receiver and the different design challenges.

CHAPTER 3

Wake-Up Receiver for IoT Applications

In this chapter, we propose a two-phase wake-up receiver that can be used in different bands and provides lower operating average power by 12% at low channel activity. We target high throughput applications with asynchronous communications where the wake-up system is primarily used to avoid the use of watchdog timers that performs synchronization and need low-latency in the startup of the main receiver. For energy detector, we propose a Schottky diode that is fabricated using CMOS technology, i.e. not part of the technology design-kit, to minimize parasitic capacitance allowing operation at high frequency ranges [23]. The second phase based on the novel data-locked startable oscillator allows correct data correlation at no need for an external clock or expensive external crystal oscillator. Digital correlator compares the received data to the preset signature to avoid interferer false wake-up for the main receiver. Digital correlator compares the received data to the preset signature to avoid interferer false wake-up for the power-hungry main receiver, which can dominate the system-level energy consumption. By optimizing the correlator length and the energy detector thresholds, we show that the two-phase wake-up receiver can reduce the system-level energy consumption by up to 60x compared to the single-stage energy detector equivalent. Wide bandwidth front-end design is adopted in the design to satisfy wake-up latency of 200μs corresponding to 40-bits signature comparison at 200kbps data rate. This work consumes low power of 1.69μW resulting in energy per bit of 8.45 pJ/bit.

The chapter is organized as follows, in Section 3.1 we discuss the wake-up receiver model and the noise analysis for envelope detector based receivers. We also show a performance comparison between the matched filter and correlator based wake-up receivers. In Section 3.2 we show the proposed 2-phase architecture and the CMOS Schottky diode used as energy

detector. The circuits implementation is shown in Section 3.3, showing the implementation challenges. The measurement results are presented in Section 6.1 with the chip micrograph built using 65nm CMOS technology.

3.1 Wake-up Receiver Model

From the point of view of a wake-up receiver, the ground truth can be described as one of two; either the $\underline{s}$ was transmitted or no. In the absence of $\underline{s}$, there are two possible scenario; a signal $\underline{s}'$ was transmitted or no signal at all was transmitted. This can be described using the following hypotheses

- H_0: The sequence $\underline{s}$ was not transmitted.
  - H_{0A}: No signal was transmitted
  - H_{0B}: A sequence $\underline{s}' \neq \underline{s}$ was transmitted.
- H_1: The sequence $\underline{s}$ was transmitted .

where $H_0 = H_{0A} \cup H_{0B}$. The probability of detection is defined as the probability of declaring H_0 when the truth is H_1 $P_{FA} = Pr(declare H_0|H_1)$, and the probability of detection is defined as $P_D = Pr(declare H_1|H_1)$ The prior distributions of the different events are given by $P(H_0)$, and $P(H_1)$, where $P(H_0) = P(H_{0A}) + P(H_{0B})$. Given our definitions of the possible event, the transmitted signal x is signal given by

$$\boldsymbol{x} = \begin{cases} \mathbf{0} & H_{0A} \\ \boldsymbol{s}' & H_{0B} \\ \boldsymbol{s} & H_1 \end{cases} \tag{3.1}$$

Since we are using OOK modulation, s is a binary sequence of length L having d ones. As for s', it is any sequence of the same length not equal to $\underline{s}$. To trigger the WuRx, we constraint the first element of both $\underline{s}$ and $\underline{s}'$ to have the first bit equal to one. The received signal is modeled as z whose k-th element $z[k]$ is given by

$$\underline{z} = \underline{x} + \underline{n} \tag{3.2}$$

where $\underline{n}$ is the additive white Gaussian noise (AWGN) vector with zero mean and covariance matrix variance $\sigma^2\underline{I}$, where $\underline{I}$ is the identity matrix. Since in our analysis we assume that the received signal was normalized to have magnitude one, the signal to noise ratio (SNR) is equal to $1/\sigma^2$.

3.1.1 Comparison of WuRx Architectures

After describing the signal model and the possible events, we consider how different wake-up receiver architectures decide whether to fire the receiver. We consider three architectures, the energy detector, the correlator, and the matched filter and compare their performance.

Energy Detector (ED) The energy detector decides as follows

$$\text{ED declares} \begin{cases} H_0 & z[1] \leq \lambda \\ H_1 & z[1] \geq \lambda \end{cases} \tag{3.3}$$

where λ is a threshold and $z[1]$ is the first element of the vector $\underline{z}$. Due to the simplicity of the energy detector, it is unable to differentiate between H_{0A} and H_{0B}.

Correlator (Corr) Instead of waking up the receiver for every signal that crosses the energy threshold, the correlator compares to the sequence $\underline{s}$. The system consists of two stages. In the first, the always-on energy detector compares the input energy with a threshold of λ. When the first element of the received vector $z[1]$ crosses the threshold, the correlator is activated. The binary vector $\bar{\boldsymbol{z}}$ is obtained using the ED threshold λ. Once, $\bar{\boldsymbol{z}}$ is obtained it is compared to the sequence $\boldsymbol{s}$. The system declares H_1 if the received sequence $\bar{\boldsymbol{z}}$ differs by at most l bits from the reference sequence $\underline{s}$. This can be expressed as follows

$$\bar{z}[k] = \begin{cases} 0 & z[k] \leq \lambda \\ 1 & z[k] > \lambda \end{cases} \tag{3.4}$$

$$\text{WuRx declares} \begin{cases} H_{0A} & \bar{z}[1] = 0 \\ H_{0B} & \bar{z}[1] = 1,\ \sum_{i=2}^{L} \bar{z}[i] \oplus s[i] > l \\ H_1 & \bar{z}[1] = 1,\ \sum_{i=2}^{L} \bar{z}[i] \oplus s[i] \leq l \end{cases} \tag{3.5}$$

where $\oplus$ is the binary xor operator. Since the correlator uses the entire sequence for comparison, it is expected to have a probability of false alarm lower than the ED. However, at low SNR, if we consider the exact match only ($l = 0$), any mistakes in the bits would lead to a misdetection.

Matched Filter (MF) The matched filter compares the analog values of $\boldsymbol{z}$ with the signature $\underline{s}$. The MF operation can be written as $\eta = \boldsymbol{z}^T \boldsymbol{s}$

$$\text{MF declares} \begin{cases} H_0 & \eta \leq \lambda \\ H_1 & \eta > \lambda \end{cases} \tag{3.6}$$

Since, $\boldsymbol{s}$ is a binary sequence, η can be rewritten as the sum of the elements of $\boldsymbol{z}$ at the location where $s[i]$ is equal one

$$\eta = \sum_{\{i:s[i]=1\}} z[i] \tag{3.7}$$

Since η is the sum of multiple values of $\boldsymbol{z}$, it is expected to be more robust to false alarm compared to ED, which only considers the first value of $\boldsymbol{z}$. However, the MF does not take into consideration the values of $\boldsymbol{z}$ where $\boldsymbol{s}$ is equal to zero. Hence, many different values of $\boldsymbol{z}$ will map to the same value of η even at high SNR leading to more false alarms than the correlator.

We compare the performance of the three architectures. Since, there is a trade-off between the probability of false alarm and the probability of detection, we use the receiver operation characteristics curves (ROC) to show this tradeoff [79]. Both the correlator, and a Matched filter used as sequence have $L = 8$ and $d = 4$. The ROC curve was obtained for ED and MF by scanning the values of λ in the range $[-2, 2]$ and $[-L, L]$ respectively. For the correlator, l was sweeped from 0 to L and for each value of l, the threshold was sweeped between $[-2, 2]$. The prior probabilities were chosen as $P(H_{0A}) = 0.9$, and $P(H_{0A}) = 256P(H_{0B})$. This equivalent to 10% utilization with 256 equiprobable 8 bit sequences.

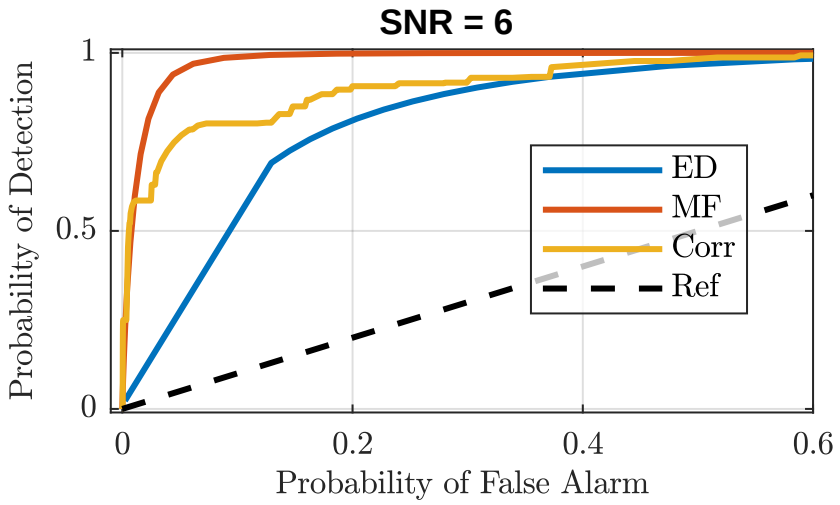

Figure 3.1: ROC curves of ED, MF, and Corr at SNR=6dB.

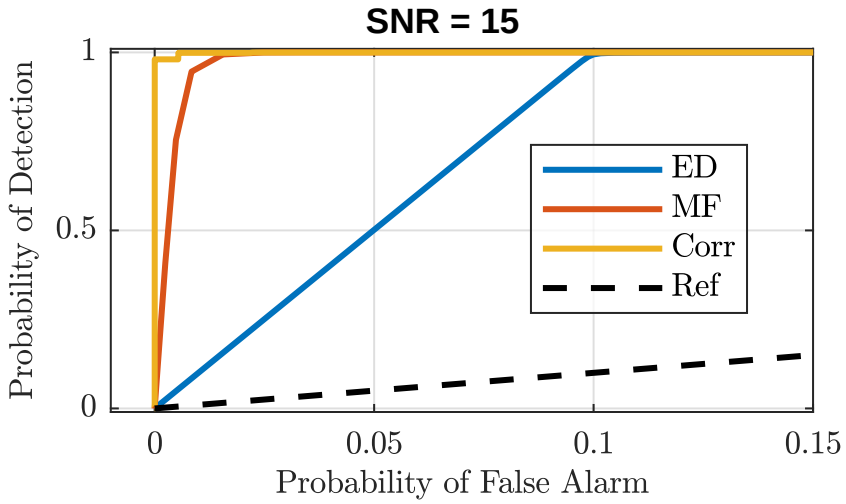

Figure 3.2: ROC curves of ED, MF, and Corr at SNR=15dB.

The ROC curves at SNR of 6 dB and 15 dB are shown in Fig. 3.1. We can see at 15dB, Correlator outperforms both the MF and ED. Since Corr checks the entire sequence, it can achieve lower PFA compared to ED. MF is unable to distinguish sequences matching $\boldsymbol{s}$ at its ones while differing at its zeros, and hence, has a lower P_{FA}, even at this high SNR. As the SNR drops, MF starts to outperform the correlator. Since the correlator will suffer from a misdetection if the first bit of the sequence was not correctly detected. Unlike the matched filter which uses all the energy of the sequence to perform the detection.

From these results, we see that the correlator parameters l and λ can be optimized to outperform the energy detector. Due to its low power requirement compared to the matched filter, we decided to build a correlator. In our design, we pick L to trade off the wakeup latency with the performance as measured by P_{FA} and P_D.

3.1.2 Noise Analysis

In this subsection, we analyze the noise contribution of envelop detector based wake-up receiver based on [22]. The system model is shown in Fig. 3.3. The model consists of the following: the noise due to the antenna ($\sigma_{n,rf}$) and with passive gain with (A_v) at center frequency of (f_{rf}). The square law detector with input impedance of (R_{ED}) and (C_{ED}) and gain of (k_{ed}). The input RF signal (v_{in}(t)) is amplified by the passive gain provided by the matching network. The input signal can be presented as:

$$v_{in}(t) = A_t cos(2\pi f_{rf} t + \phi_{rf}) \tag{3.8}$$

The signal power at the antenna can be written as $v^2_{in,rms} = P_{in} R_S$. The input noise from the antenna passed through a band-pass filter of the matching network which results in input referred noise of $\sigma^2_{n,rf} = KTR_s BW_{RF}$ where K is Boltzmann's constant, T is absolute temperature, R_s is antenna 50 ohm resistance, and BW_{RF} is the RF bandwidth.

This signal is amplified by the passive gain provided by the impedance transformation. The output voltage at the matching network is given by

$$v_{ed,in}(t) = A_v v_{in}(t) \tag{3.9}$$

The output noise at the envelop detector output is calculated as function of the input noise as follows

$$\sigma^2_{n,ed,in} = \sigma^2_{n,rf} A^2_v NF \tag{3.10}$$

where the noise contribution of the matching network is given by (NF) which is the losses of this network.

The input signal and the input referred noise are added together and inserted at the

square law detector

$$v_{ed,out}(t) = k_{ed}(v_{ed,in}(t) + v_{n,ed,in}(t))^2 \tag{3.11}$$

where $v_{n,ed,in}$ is the voltage noise at the input of the square-law device with variance of $\sigma^2_{n,ed,in}$. By calculating the rms output voltage signal

$$v_{ed,out,rms} = k^2_{ed} v^4_{ed,in,rms} = A^4_v k^2_{ed} P^2_{in} R^2_s \tag{3.12}$$

Then by calculating the noise at the output of the square law-detector from equation 3.11, we see that we have 2 main components. The first one is the noise due to the multiplication of the signal and the noise which is negligible. The second term due to the matching network and envelop detector noise and is presented as

$$\sigma^2_{n,ed,out} = 4kTR_{ED}BW_{BB} \tag{3.13}$$

Where R_{ED} is the input resistance at f_{rf} and it's tied to the antenna source resistance at the matched condition as follows

$$R_{ED} = A^2_v R_s \tag{3.14}$$

So the signal to noise ratio (SNR_{out}) at the output of the envelop detector can be expressed as

$$SNR_{out} = \frac{A^4_v k^2_{ed} P^2_{in} R^2_s}{4kTR_{ED}BW_{BB}} \tag{3.15}$$

The sensitivity equation can be expressed according to the SNR_{out} equation as follows

$$P^2_{sens} = \frac{4kTR_{ED}BW_{BB}SNR_{min}}{A^4_v k^2_{ed} P^2_{in} R^2_s} \tag{3.16}$$

where SNR_{min} is the minimum SNR at which the signal can be detected at the input of the WuRx. To simplify the equation, we can substitute using eq. 3.14, then the expression can be expressed as

$$P^2_{sens} = \frac{4kTBW_{BB}}{A^2_v k^2_{ed} R_s} \tag{3.17}$$

From the resulted equation, we find out that the system sensitivity is directly proportional to the base-band bandwidth of the system (data rate). Also it's inversely proportional to the envelop detector gain and the passive gain which both needs to be maximized in order

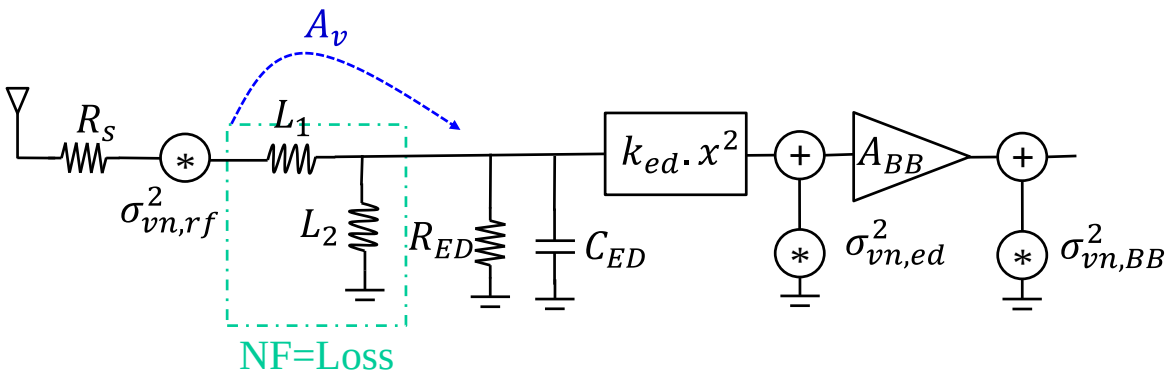

Figure 3.3: System model for noise analysis.

to achieve the maximum sensitivity for a given data rate. As we will show in Section 3.2, the Schottky diode maximizes the conversion gain as well as the passive gain through matching network for the data rate of 200kbps.

3.1.3 Correlator Design Analysis

To determine the effect of our choice of the correlator length L on the performance of the wake-up receiver, we generate a ROC curve for the candidate values of L at different SNRs. The area under the ROC curve (AUC) was used as a comparison metric. An ideal detector would have an AUC value equal to one. The ROC curves were generated using the same parameters as in Section 3.1.1. The results are shown in Fig. 3.4, from which we see that by increasing L, we can find the values of l and λ that improve the performance of the detector. However, increasing L increases wake-up latency. Hence, we decided to use $L = 8$.

After choosing $L = 8$, we aim to determine the values of the parameters l and λ, which optimize the system performance. The effect of changing the threshold for different l at SNR=15dB is shown in Fig. 3.5. As we increase l, the probability of detection increases but, the P_{FA} increases at least by up to 100 folds. To avoid erroneous wake-ups of the receiver, we decided to choose $l = 0$.

After choosing $l = 0$, we plot the effect of the choice of the threshold on the system

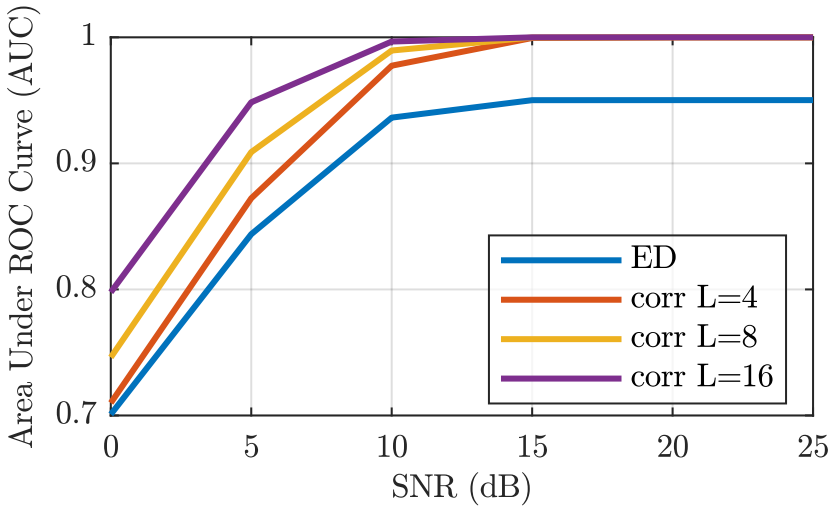

Figure 3.4: The effect of the correlator length (L) on the WuRx performance measured using AUC at different SNRs.

performance at different SNRs in Fig. 3.6. From this figure, we see that setting setting the threshold to 0.5 gives the best detection performance for any SNR. This is intuitive since the noise distribution is Gaussian and the sequences are binary.

3.1.4 Energy Analysis

The expected energy consumption E of any WakeUp receiver architecture is related to the probability of false alarm and detection using

$$E = E_{\text{WuRx}} + (P_D P(H_1) + P_{FA} P(H_0)) E_{\text{Rx}} \tag{3.18}$$

where E_{WuRx} is the energy of the wakeup receiver and E_{Rx} is the energy of the receiver. Since, $E_{\text{Rx}} >> E_{\text{WuRx}}$, we want a wakeup receiver with the lowest P_{FA} for a given P_D. Our proposed receiver optimizes E from an analytical perspective by reducing both E_{WuRx} and reducing P_{FA}. E_{WuRx} is reduced since the correlator turns on only when the energy detector is activated as shown.

$$E_{\text{WuRx}} = E^{ED} + (P(H_0) P_{FA}^{ED} + P(H_1) P_D^{ED}) E_{Cor} \tag{3.19}$$

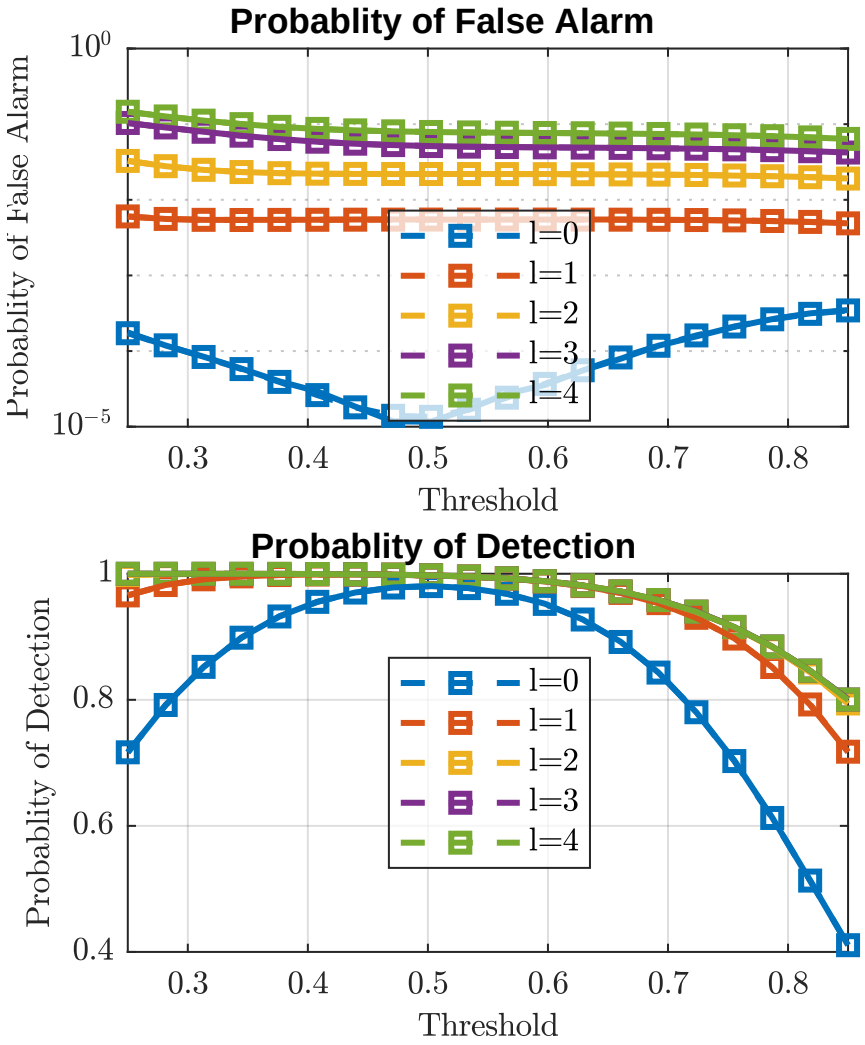

Figure 3.5: Probability of false alarm and detection as a function of the threshold of an 8 bit correlator for different number of bits allowed to be wrong while still declaring a match l.

P_FA is reduced by combining two stages of filtering before waking up the power hungry receiver

$$P_{FA} = P(H_0) P_{FA}^{ED} P_{FA}^{Cor} \tag{3.20}$$

For a fair comparison between a single-stage and two-stage system, we set a minimum value of P_D. We assume that the system requires a probability of detection γ to be realized with at most q retransmission. Hence, the probability of at least one transmission out of q being detected should be greater than γ. $P(\text{det. at least one of } q) = 1 - (1 - P_d)^q \geq \gamma$ This

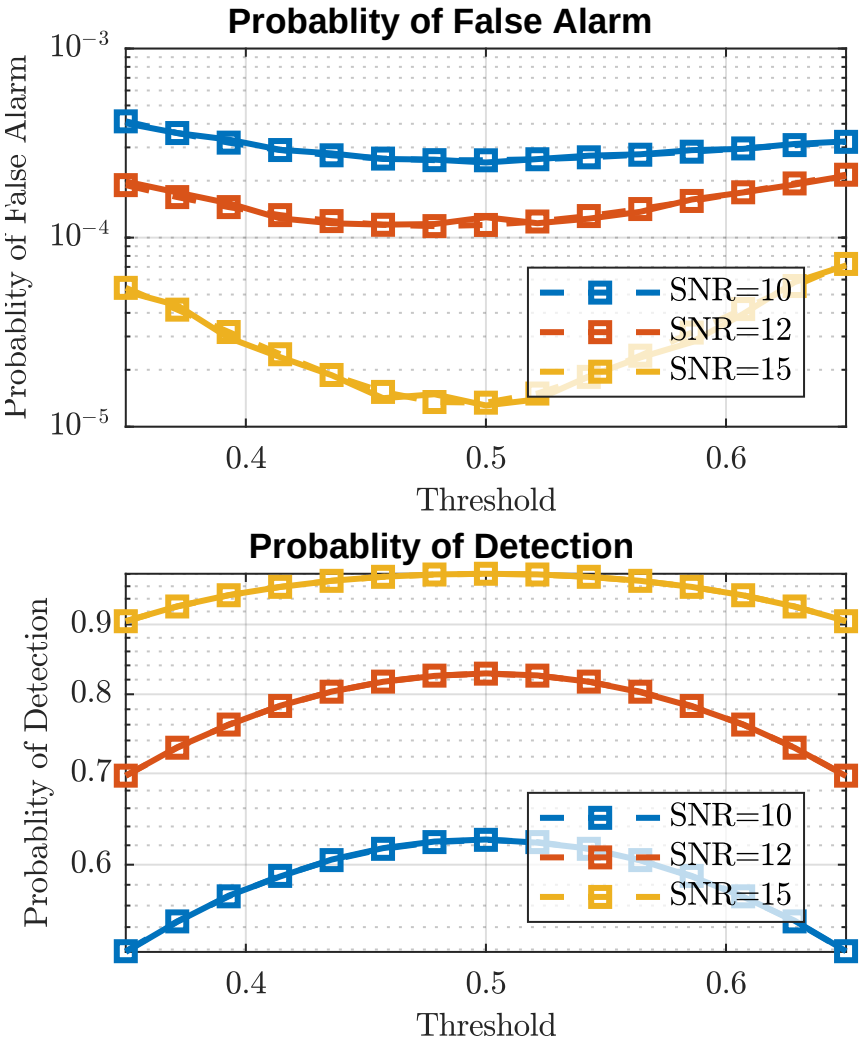

Figure 3.6: Probability of false alarm and detection as a function of the threshold of an 8 bit correlator for different SNRs.

is equivalent to having $P_d \geq 1 - (1-\gamma)^{1/q}$.

For both ED and MF, we considered the lowest expected energy consumption by optimizing the value of the parameters of each architecture at each SNR for $\gamma = 0.99$ and $q = 5$. The results are shown in Fig. 3.7. Although the ED circuit by itself has a lower energy consumption than the correlator, it mistakenly awakes the main receiver often. This increases the energy consumption of the system by up to 60 times. A correlator, on the other hand at SNR of 10 and above has P_{FA} approaching zero. Thus, it almost attaining the lower bound of power consumption, which occurs when receiver $P_{FA} = 0$. At these SNR

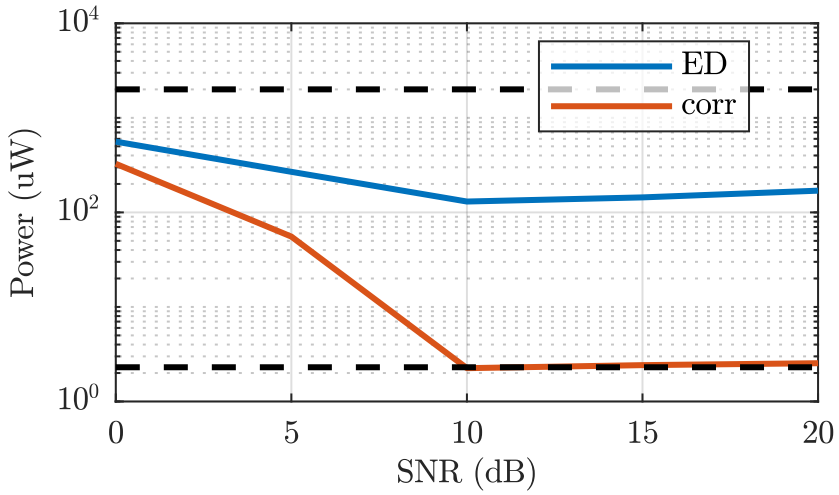

Figure 3.7: The expected energy consumption of ED and Corr when parameters are optimized as a function of SNR.

(10 and above), the optimal parameters of the correlator are $\lambda = 0.5$ and $l = 0$, which we have chosen previously. At SNRs lower than 10, l has to be increased to meet the required P_D leading to higher P_{FA} and thus higher energy consumption.

3.2 System Architecture

The system architecture is shown in Fig. 3.8. The proposed system is an ultra-low-power (ULP) wake-up receiver with two phases whereby the first phase that detects the existence of a signal triggers the activation of a signature detection phase. Since the average power consumed of the system is the average sum of the two phases as shown in the following equation.

$$P_{avg} = P_{ED} + \frac{P_{corr} t_{corr}}{t_{tot}} \tag{3.21}$$

Where P_{ED} is optimized to the minimum so that the signature comparison phase and oscillator launching is done in the second phase of the wake-up. Thus average power consumption will fall by breaking the wake-up sequence into two phases. More analysis in Section 3.1.4 shows the improvement of average power consumption reduction and the probability of false alarm which lowers the power of the system . Minimizing power consumption is done by only

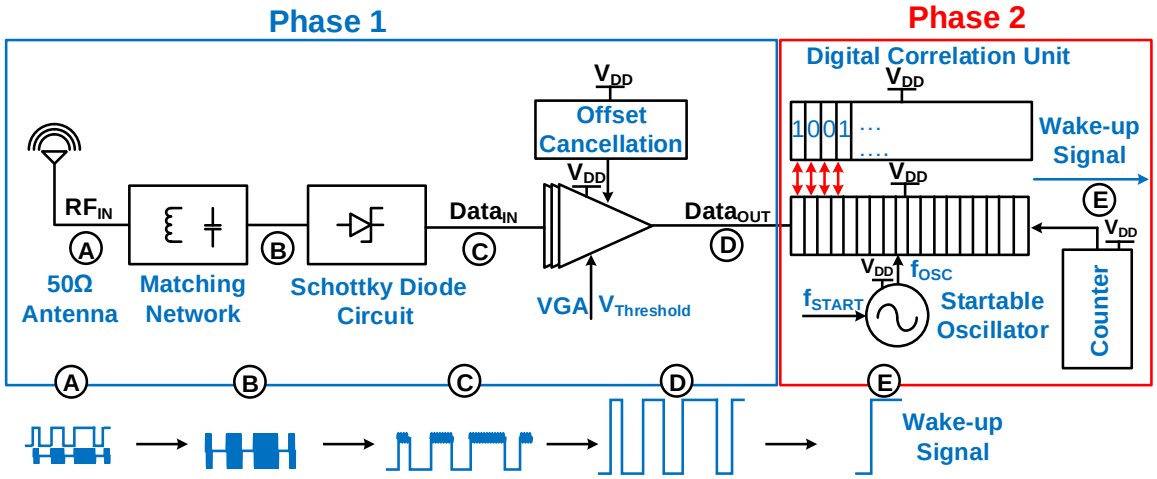

Figure 3.8: Proposed wake-up receiver architecture

firing the second phase in case of detection of the data stream in the channel, comparing the data to a preset signature within 16 clock cycles. If the signature does not match, the second phase will be disabled again till the new data stream is detected thus reducing t_{corr}.

The proposed architecture can be explained as follows. The first phase is composed of a matching network, Schottky diode, and a variable gain amplifier. The first stage is always-ON and relies on the passive gain of the matching network and power detection to make a decision based on the received power within the control channel on whether to enable the subsequent phase. This passive gain is essential at the low input power level to enhance the detection probability. The diode detector is a key innovation that avoids GHz oscillators and mixers hence enables low-power operation consuming 18% of the power at high data rates. Following the diode's square-law detection, a variable gain amplifier that operates in sub-threshold with the maximum gm/I_D and provides enough signal swing to fire the second phase.

The second phase is composed of a low power data-locked startable oscillator, digital correlation unit, and counter. The data-locked oscillator is the key point for two-phase architecture. It starts up in one clock cycle and performs data sampling running at the same frequency as the data rate. The digital correlator compares the received signal to

a predefined signature and generates the wake-up signal accordingly. The correlator is a key element since square-law detectors are sensitive to strong interferes especially in an unlicensed frequency band. By introducing a signature within the control carrier frequency and associated interference cancellation, thus improve overall sensitivity. Since the average operating power of the system is the sum of the product of the power of each stage with the cumulative probability of a false positive to each stage, such a design is optimized by adjusting the threshold and signature code length to minimize false positives under a given power constraint while being robust to noise and interference. Further analysis for the PFA, threshold, and signal to noise ratio is presented in Section 3.1.

3.2.1 Schottky diode doubler as energy detector

Square-law detectors are the key-point in low power wake-up receivers. The criteria for choosing a detector are achieving required base-band bandwidth with acceptable conversion gain while having a low-power percentage of the overall system to minimize energy per-bit cost. In this architecture, we chose the Schottky diode as a power detector and fabricated on CMOS to provide an integrated wake-up system solution. The Schottky diode acts as the square-law detector for the incident power resulting in $V_{out_1 stage}$=Γ_o*V_{rf}^2, where (Γ_o) is the conversion gain for the power detector which is dependent on the incident power. Schottky diode doubler stage allows better biasing and a small power penalty compared to a single diode. Multiple Schottky diode doubler stages (N) as shown in Fig.3.9(a) will result in boost in the output voltage shown as $V_{out_N stage}$=N*$V_{OUT_1 stage}$. However, using multiple stages results in the following limitations. First, it causes more capacitance at the input limiting the operation bandwidth (BW$\propto 1/N^2$) [14]. This is owing to the model of each stage as an RC circuit resulting in an increase of delay by (N^2) which forces the use of lower data-rate results in longer wake-up latency. Second, having N-stages lower the input impedance by a factor of (N) resulting in lower passive gain through matching network, hence only $\sqrt{N}$ of voltage gain by taking into consideration the matching network passive gain as shown in Fig. 3.9(b). Third, it increases the biasing power required to achieve the same in-band noise since the thermal noise in the diode is $\propto$1/(biasing diode current), which will result in a

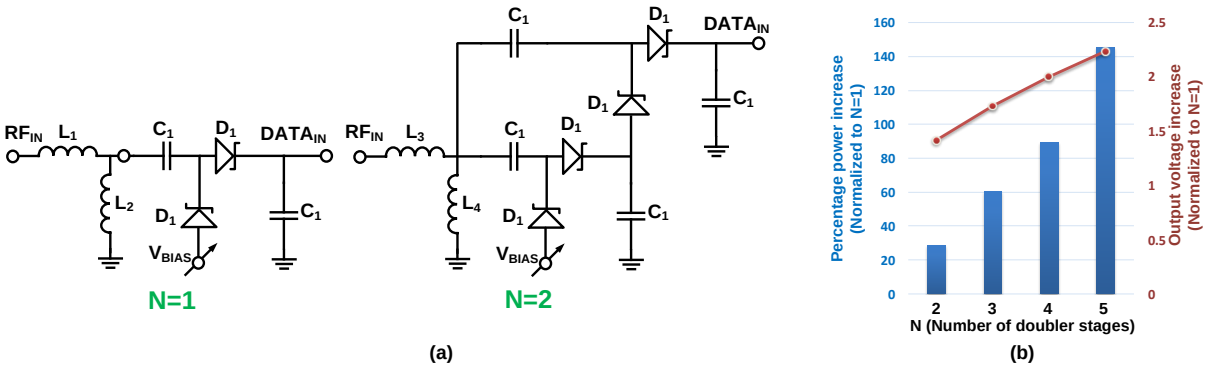

Figure 3.9: (a)voltage doubler configuration for N=1 and N=2, (b) percentage increase in power and voltage gain of having multiple double stages normalized to N=1

higher more complicated biasing and in higher power compared to single doubler structure as shown in Fig. 3.9(b).

For the targeted latency, we chose doubler configuration (N=1) which achieves the required data rate with the ease of biasing with small power. Also smaller input impedance compared to the single-stage which allowed us to match the input impedance with the use of non-expensive inductors with reasonable Q≈25. CMOS integrated Schottky diode input impedance was first measured using a vector network analyzer (VNA) at the operating biasing condition then a matching network is built as discussed in Chapter 6.3. Schottky diode stage and VGA are the main noise contributors to the system. The noise for the square-law detector stage can be modeled using the following equation

$$NF_{SD} = 1 + \frac{N_{o,SD}}{N_s G_P^2} \tag{3.22}$$

Where N_s=4kTR_s, G_P is the conversion gain of the passive network multiplied with the gain through the voltage doubler configuration gain. G_P depends on the incident power to the power detector which corresponds to lower gain at lower input power leading to higher noise figure. The noise figure of the Schottky diode doubler impacts the sensitivity of the overall system. Noise analysis for envelop detector based wake-up receiver is presented in Section 3.1.2. To achieve better sensitivity, smaller bandwidth is required which corresponds to lower data rate resulting in high wake-up latency. The integrated noise power in the Schottky diode

is a function of the biasing current since the main noise source is R_j is inversely proportional to the biasing current, where R_j is the equivalent resistance of the diode. A biasing current of 1.6μA is used for achieving input impedance that can be easily matched, as further illustrated in Chapter 6.3 while achieving the required baseband bandwidth for a data rate of 200 kbps.

3.2.2 Injection-locking startable oscillator

To achieve correct data correlation, a stable, precise oscillator is required. In this work, we propose a two-phase wake-up to lower average power consumption which requires a second phase based on the startable oscillator. The oscillator should start-up within one clock cycle and maintains stable frequency across a wide range of temperature variation. Different approaches were investigated for stable clock generation which includes a delay-locked loop (DLL). DLL has simple and efficient architecture, however, it requires multiple clock cycles to lock to the correct edge which will in return impact the latency of wake-up. Another approach is the use of oversampling by 2-3x, however, this will increase power dissipation for the second phase significantly, since P=C$f_{sw}V_{DD}^2$.

We propose a data-locked startable oscillator that uses the data transition amplified by the first phase as a start signal. The data transitions are further used to create a pulse that aligns the "CLKB" signal with the data transition allowing the correct slicing of data in the middle of the period. The clock variation is corrected each data transition assuring an average running frequency matching the data-rate. The top-level operation for the proposed oscillator is shown in Fig. 3.10. The proposed oscillator starts-up in one cycle which serves the targeted low-latency start-up applications. The startup latency for the targeted system is 200μs.

3.3 Wake-Up Receiver Circuit Design

3.3.1 CMOS integrated Schottky diode

CMOS integrated Schottky diode square-law detector is the key for performance enhancement at the high carrier frequency. The Schottky diode acts as a power detector and uses low biasing current to accommodate the required bandwidth. The voltage double structure passes the required biasing voltage to the next amplifier chain stage. The diode model is shown in Fig. 3.11(a) and it shows DC operating point for single diode and how it impacts

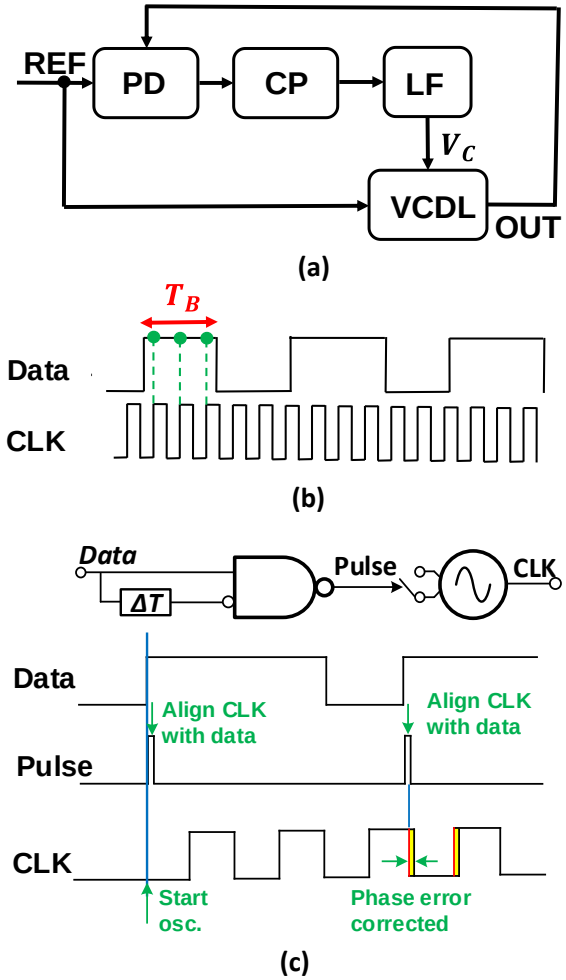

Figure 3.10: (a)DLL conceptual design, (b) oversampling oscillator, and (c)conceptual diagram for data-locked startable oscillator operation

the level of the noise and input impedance. To achieve the required bandwidth while having acceptable noise levels, a small biasing current is chosen for the diodes to have the maximum input impedance. The power transformation equation can be understandable by considering the model for the diode detector circuit as follows: R_J is the dynamic equivalent resistance of the diode, R_X is a parasitic series resistance, C_J is a parasitic capacitance, P_J is the power delivered to R_J, γ_0 is the DC voltage-sensitivity, and C_L represents the load. The equivalent noise source is also shown in the figure. Since R_X and C_J limit the power delivered to R_J, the effective voltage sensitivity of the diode detector can be shown to be:

$$\gamma_{eff} = \frac{\gamma_0}{1 + \omega_{rf}^2 C_J^2 R_X R_J} \tag{3.23}$$

$$\gamma_{eff} = \frac{1}{2(I_D + I_S)} \times \frac{1}{1 + \omega_{rf}^2 C_J^2 R_X R_J} V/W \tag{3.24}$$

where it is assumed that C_L is short at RF. Clearly, zero bias ($I_D = 0$) and a very small reverse saturation current (I_S) increases the DC voltage-sensitivity i.e. for low ω_{rf}. This also results in a very large diode resistance which results in higher input impedance that can be translated into higher passive gain. However, it also means higher noise in the diode output voltage. In this work, we choose doubler configuration to achieve higher conversion gain as well as biasing current of 1.6μA to have a 50mV drop across each diode and set the biasing of the variable gain amplifier stage. The biasing condition sets the input impedance of R_{IN}=2.15kΩ in parallel with C_{IN}=3.7pF observed at the voltage double input into passive gain by the matching network. The input impedance is matched to 50 ohms resulting in a passive gain of 16 dB. However, due to the finite quality factor (Q$\approx$25) of inductors, the simulated gain is 13 dB. The matching and filtering for this stage at the center frequency of 750MHz. The bandwidth of filtering is chosen to be enough for the data rate and also has good rejection for close-by interferes. The matching network provides filtering for the signal and lower integrated noise in the band. Also, the quality factor choice is to allow a wide bandwidth for the required data rate of 200kHz with reasonable data settling time.

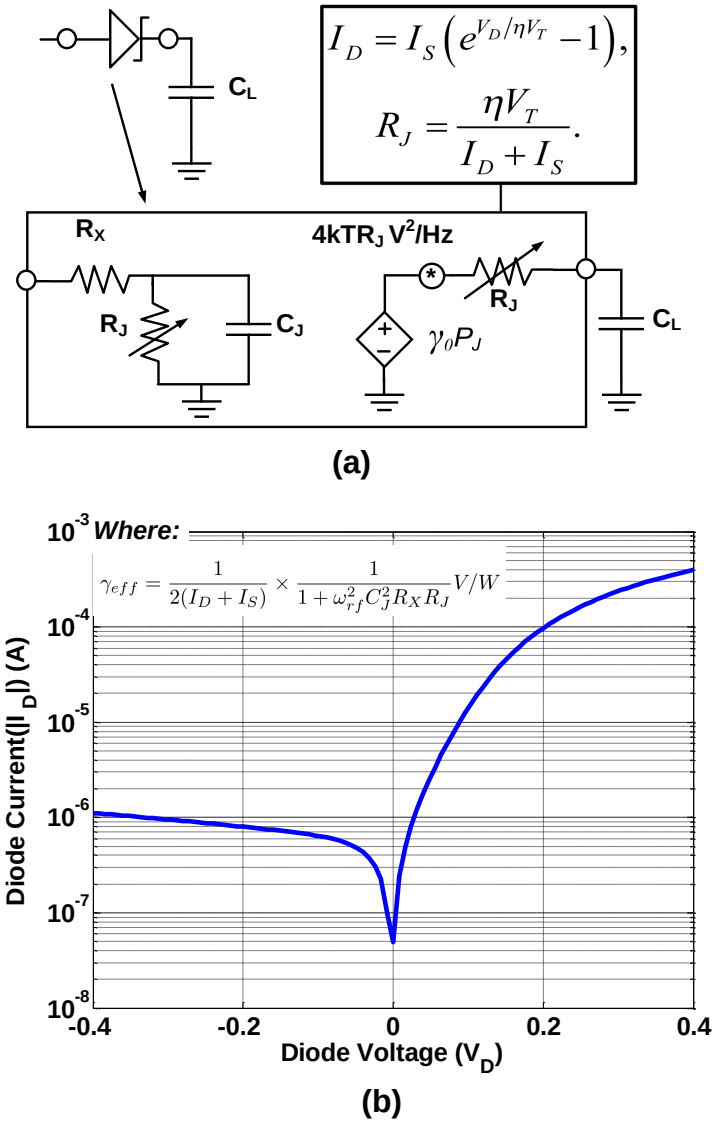

Figure 3.11: (a) Schottky diode small-signal model and equations, (b) Schottky diode measured I-V characteristics

3.3.2 Variable gain amplifier with variable threshold voltage

The down-converted signal at 200kbps requires amplification to full scale before being correlated to the signature stored. A chain of amplifiers is used to amplify the signal out of the power detector circuit shown in Fig.3.12. The programmable gain is used to lower the overall power consumption of the chain if the higher input power is incident. The chain consists of five amplifiers are controlled to be disabled to save power in case of lower sensitivity needed.

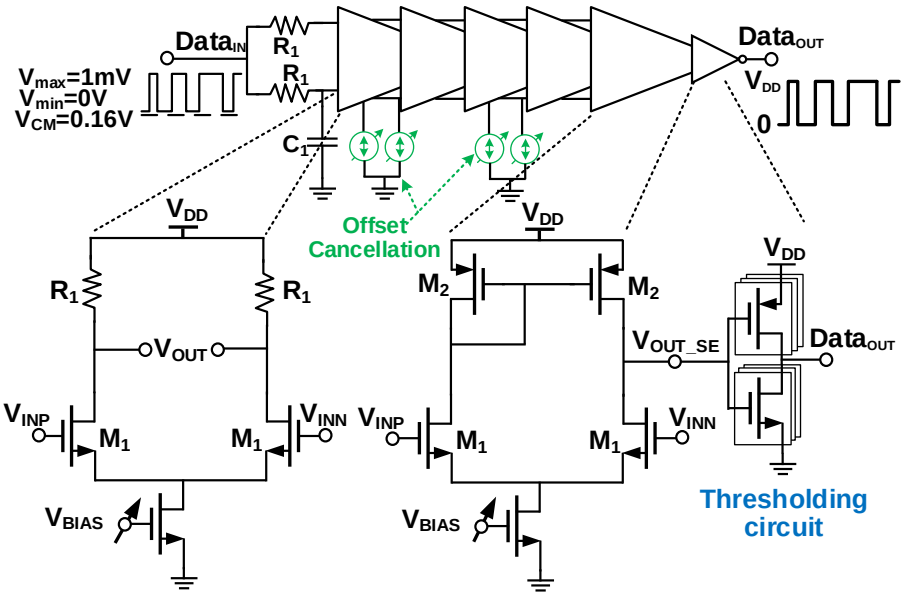

Figure 3.12: (a) Amplifier chain circuit implementation, (b) different threshold voltage configuration,(c) amplifier gain configuration for different input power levels

The control of the chain of the gain of the amplifier is done by bypassing amplifiers and disable them. The different gain configuration for the amplifier chain that covers a wide range of gain from 66dB to 0dB, as shown in Fig 3.13(a). These limits are chosen to cover the range of signal of 1mV which is equivalent to input power of -50dBm at the output of the diode structure. The minimum gain is chosen to pass the input of 0.4V directly to the output with no amplification or attenuation if needed.

The biasing of the chain of the amplifiers is a challenging design problem. To assure the proper biasing conditions, more current biasing program-ability is added at each stage with roughly 400nA of tail biasing for each stage. The sizing of the amplifiers is done with the maximum gm/I_D to ensure the maximum gain with the minimum biasing currents. A differential amplifier structure is used rather than single-ended due to its numerous advantages as it has better common-mode (CM) rejection as well as the output common-mode of each stage can be defined for the next stages of the amplifier chain. Also, the supply rejection is one of the main advantages for a differential structure over single-ended and that is necessary at a

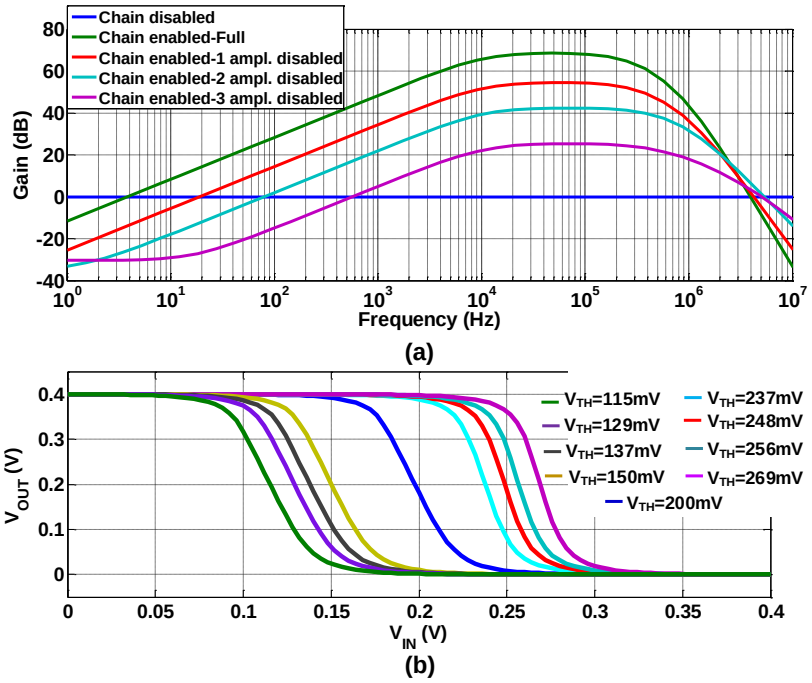

Figure 3.13: (a)Thresholding at different configurations, (b)amplifier gain configuration for different input power levels

low regulated power supply of 0.4V [80]. An offset cancellation technique is implemented to reduce the offsetting impact of different stages and to assure the biasing setting of different stages in the chain. The offset cancellation is set once at the calibration phase.

A variable size inverter is added at the last stage to add ≈15dB of gain to the amplification chain. The transistor size controls the threshold levels for setting "0" and "1" logic, hence adds another degree of freedom in deciding the data sent according to the noise level. Changing the width of the NMOS or PMOS transistor will change the threshold voltage for the detection of the received signal as shown in Fig. 3.13(b), which allows a wide range of threshold voltage change from 115mV up to 270mV. Threshold control lowers the probability of false alarm of the main receiver as well as control the probability of starting the second phase of the proposed system.

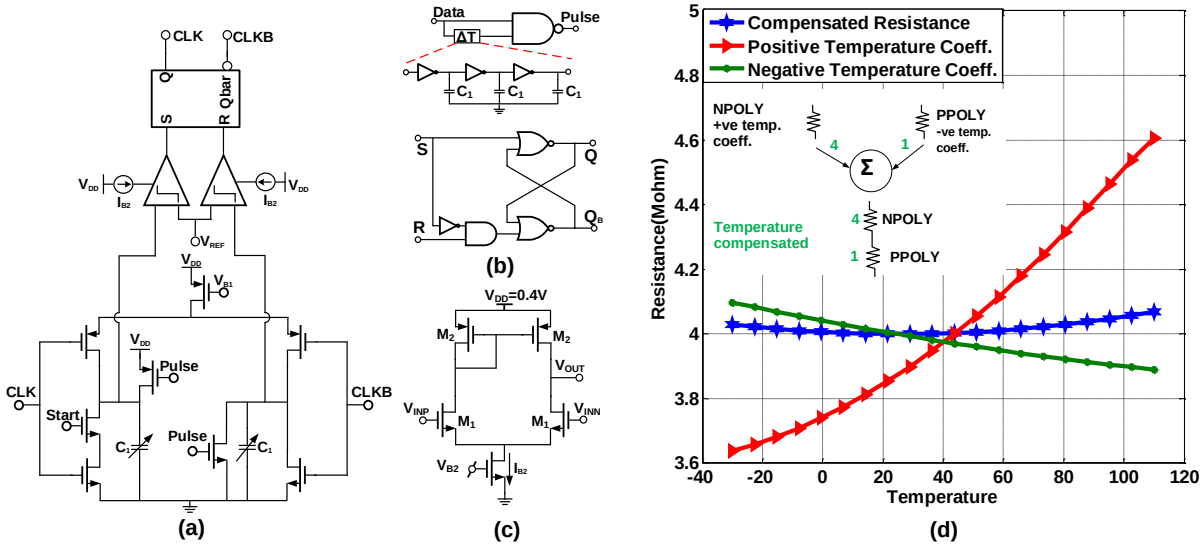

Figure 3.14: (a)Relaxation oscillator architecture with data locking technique (b) pulse generator for data locking technique and SR latch with set dominant to avoid delayed startup (c) comparator design for the oscillator (d)zero-order temperature compensation using Npoly and Ppoly

3.3.3 Data-locked startable oscillator

Two-phase wake-up architecture is based on the proposed data-locked startable oscillator. Fig. 3.14(a) shows the data-locking architecture of the relaxation oscillator. The data received from the first stage creates a pulse to align the start oscillator signal with the data edge. Then the data correction for the clock edge takes place and corrects up to 5% of clock frequency, as shown in Fig. 3.14(b), drifting across different temperatures. In this design, we limited the frequency variation across temperature to be <5% using temperature compensation techniques at the lowest power cost. Since the frequency of oscillation, the equation is given by

$$f_{clk} = \frac{I_{B1}}{C_1 \times V_{REF}} \tag{3.25}$$

The temperature dependence terms of the oscillator as the reference voltage V_{REF} is compensated using zero-order compensation as shown in Fig. 3.14(d). The compensation is done by having a positive temperature coefficient resistor (Npoly)added in series to negative

temperature coefficient resistor (Ppoly) with the ratio of 4:1 when generating the biasing current and the reference voltage. By having a ratio of these two resistors we can generate a constant resistance within <0.1% variation across a temperature range of [-30 to 110]. Thus it limits the frequency variations from ±15% to ±5%. Thus allowing the data locking technique to correct for the variation resulting in average frequency variation of <0.1%.

Another important feature in the proposed oscillator is a fast start-up. The set dominant SR latch is shown in Fig. 3.14(b) avoids having the "CLK" and "CLKB" signal both at the stuck state, hence avoid the need for any start-up circuits that consume high power and takes multiple cycles to settle. It starts up with the correct oscillation frequency at the first cycle since it only waits for the "start" signal to oscillate with the previously set bias current. That start signal is asserted when the incident data changes from '0' to '1'. This represents the start of the packet that carries the signature to wake-up the main receiver. For data correlation, the system requires the frequency to be stable and operate at low power. The proposed techniques show to be sufficient to correctly sample the incident packet of 40 bits and achieve BER of less than 10^{-3}. The proposed oscillator consumes a power of less than 200nW at 200kHz oscillation frequency.

3.3.4 Digital correlation unit

In the operating unlicensed frequency band, interferers are present, increasing the possibility of a false wake-up for the main receiver if only the energy detection stage is used. The digital correlation unit correlates the preset signature with the received data minimizing the probability of false wake-up that has a large power penalty. Signature comparison is based on 2-step detection, the first step is after the start signal is detected from the VGA output. First a 4-bit counter at which is activated when data input changes from '0' to '1' along with an 8-bit shift register which compares the data received to externally defined preamble sequence within 16 clock cycles. If the preamble is not found, the counter disables the oscillator in the second phase to save power until another change from '0' to '1' is detected. If the preamble signature is detected, that will enable the second step in detection. The preamble sequence

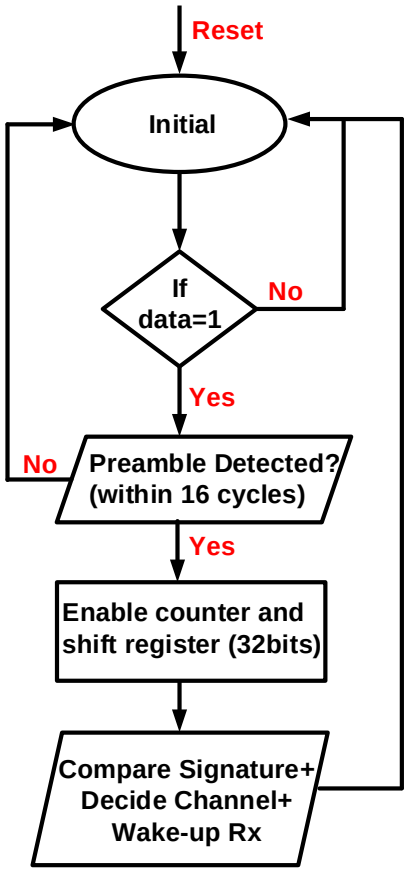

Figure 3.15: Digital correlation unit flow-chart operation

will trigger the 'wake-up' signal. In the second step of detection, a 5-bit counter and a 32-bit shift register are implemented to store the data after the preamble. The 32-bit data provides information for the channel selected and the transmitter signature. After storage of the channel information and the transmitter signature, the 5-bit counter will disable the second phase of the system by disabling the startable oscillator. The second phase will stay off until the data input changes from '0' to '1'. The flow chart is shown in Fig. 3.15 shows the sequence of detection of data in the second phase in the proposed architecture. Another mode of operation for the digital correlation unit is to check the stream of data bits to check for BER of 10^{-3}.

3.4 Summary

In this chapter, we presented a two-phase wake-up system operating at 750MHz and achieving low latency of 200μs. By optimizing the parameters of the proposed two wake-up receiver, the lower rate of false wake-ups of the main receiver can lead to up to 60x system-level energy reduction compared to the single-stage energy detection receiver. The proposed Schottky diode doubler biased at low power and achieves required bandwidth enabling achieving sub 10pJ/bit target. The newly proposed data-locking relaxation oscillator consumes 1nW/kHz, achieves <0.1% frequency variation across temperature, and avoids the use of expensive external crystal oscillator. The system can receive data with 200 kbps with -50dBm of sensitivity and achieves FOM=8.45pJ/bit [28]. The system is implemented in 65nm CMOS technology and occupies an active area of 800μm×350μm. The wake-up system operates using a 0.4V supply which requires voltage regulation from the battery voltage.

In the next chapter, we introduce the system and circuit techniques for a hybrid power converter that is used for the supply regulation of the proposed wake-up receiver. Also, we further extend the operating load range of the hybrid converter to cover wide load ranges with small ripples and high power efficiency. The range switching on the system level mainly to improve overall efficiency and allow switching to fast transient LDO which we propose in Chapter 5.

CHAPTER 4

Power Management for IoT Applications

Recent emerging technologies and systems on chip (SoC) operating at sub-1V have increased demand for power management units with high efficiency at low power loads. Internet of things (IoT) applications along with other applications such as biomedical implants and wake-up receivers operate at power levels ranging from a few microwatts to hundreds of microwatts [4]-[28]. As discussed in Section 2.2, for near-threshold operation and ultra-low power, these applications operate at low supply voltages which often range from 0.3-0.8V. While energy harvesting techniques have been shown [29]-[31], most systems provide a battery as the primary or auxiliary power source for their stable voltage supply. These battery voltages can range from 1.2V to 5V which then uses dc-dc converters to provide the supply voltages of these circuits. To maintain long battery life, the high power-conversion efficiency is critical for these converters since they can add substantial overhead for the overall power consumption of the chip. As discussed in Chapter 3, the wake-up receiver system requires a 0.4V supply with high power efficiency at 1.69μW load. This challenge is the second contribution of the thesis of power regulation at high power efficiency. In the next chapter, we discuss the challenge of power management for the main radio when it wakes up.

In this chapter, we show the system implementation of the hybrid DC-DC converter used for the wake-up receiver. Section 4.1 introduces the hybrid converter architecture which is based on 2 stages. The first stage is a switched capacitor divider and the second stage is the proposed ON-OFF LDO. Section 4.2 shows the circuit implementation for the two stages and the system analysis. The measurement results are presented in Section 6.2 with the chip micrograph built using 28nm CMOS technology.

4.1 Hybrid-Converter System Architecture

In this work, we propose a hybrid dc-dc converter architecture to achieve improved efficiency for low load applications. The output voltage of the first two 2 shows the top-level architecture of the proposed design. In the first stage, we use a switched-capacitor divider to provide the initial step-down [35] of divide-by-3 without feedback regulation of the output to maximize the power efficiency. As shown in [44], higher division factors are readily achievable if a higher battery voltage is present. The output of the first stage is a direct division and hence tracks any transient behavior of the supply voltage at the output voltage. A VDD step from 1.5V to 1.3V is shown in Fig 4.1. The second stage regulates the output voltage to the target voltage of 0.4V using the proposed LDO. This proposed "ON-OFF" LDO uses an all-digital control to minimize quiescent power. Both stages are designed to be adaptable by enabling and disabling parallel elements to support a wide range of loads. To maintain efficiency, the LDO is designed for a very low dropout of <30mV while providing good feedback regulation and noise response. The following two sub-sections describe each of the two stages and describe how the combined converter is designed to reduce its quiescent current and improve the overall efficiency

4.1.1 Switched-Capacitor DC-DC Converter

Switched-capacitor dc-dc converters have five common topologies: ladder, Dickson, Fibonacci, doubler, and series-parallel [45]. Unlike switched-capacitor regulators where the power density is the most important performance factor of a design [51], this design targets maximum efficiency at relatively low load currents. We chose a series-parallel topology, as shown in Fig. 4.2, because it provides an efficient step-down conversion. The configuration of its switches and capacitors determines the division ratio. A typical switched-capacitor converter operates in one of two regions: a fast switching limit (FSL) and a slow switching limit (SSL) [43]-[45]. A design operating in SSL has an output impedance dependent on the switching frequency and design in FSL has an output impedance dependent on the switch impedance. Operating in SSL is well-suited for low-power applications due to a low switching

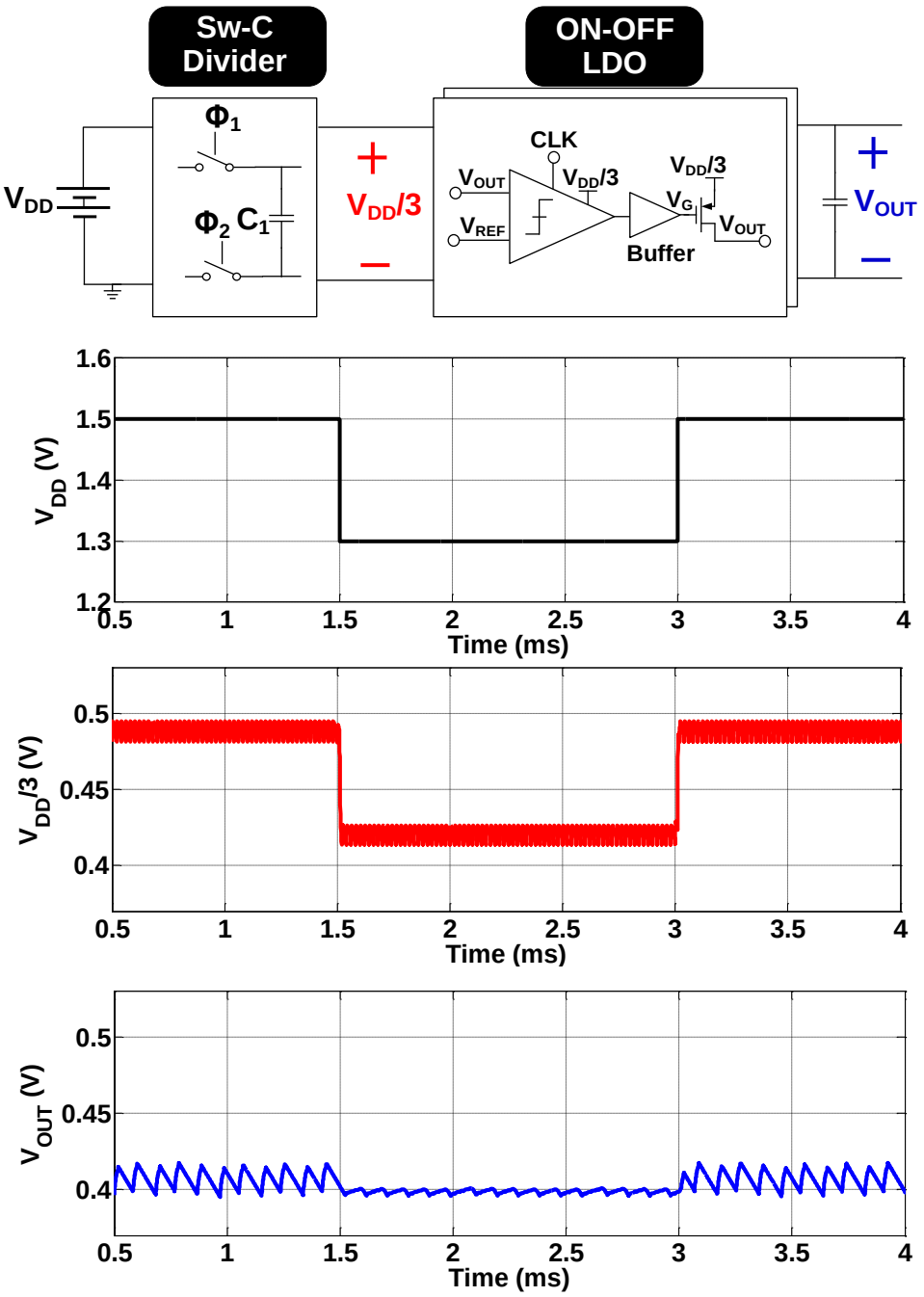

Figure 4.1: Proposed hybrid converter top-level and supply changing impact on the first stage of switched capacitor divider and the output voltage regulated at 0.4V.

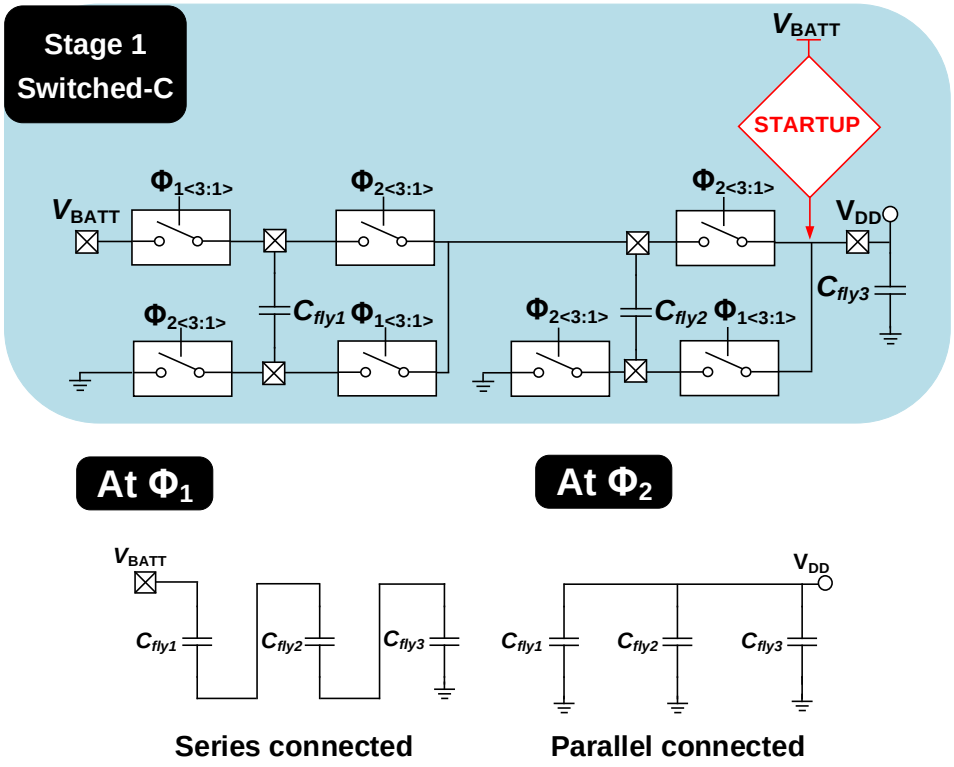

Figure 4.2: Switched-capacitor divider architecture and series-parallel operation at 2 clock phases.

frequency whereas operating in FSL provides low drive impedance for high power density.

This design targets a maximum load current of 300μA. The goal is to maintain high efficiency even at very low load currents of below 1μA. Due to the ripple suppression of the subsequent LDO, we target a ripple of 30mV from this stage. The design is a balance of these criteria. The output impedance which determines the amount of load current is a function of the region of operation. In FSL, the impedance depends entirely on the ON resistance (R_{ON}). In SSL, the impedance can be expressed as follows [43]:

$$R_{SSL} = \frac{V_{OUT}}{I_{OUT}} = \frac{k(n-1)^2}{C_{tot-fly} f_{sw}} \tag{4.1}$$

In the equation, n is the conversion ratio, k is an analysis constant from simulation, and $C_{tot-fly}$is the total flying capacitor used in the switched capacitor divider. The overall

impedance can be expressed as

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{4.2}$$

For a series-parallel configuration, three primary factors contribute to the loss (P_{Loss}) and hence degrade efficiency: switch conduction losses (P_{Rsw}), switching losses (P_{Cgs}), and quiescent losses (P_Q).

$$P_{Loss} = P_{Rsw} + P_{Cgs} + P_Q \tag{4.3}$$

$$P_{Rsw} = R_{ON} I_{Load}^2 \tag{4.4}$$

$$P_{Cgs} = f_{SW} C_{GS} V_{GS}^2 \tag{4.5}$$

Switch conduction losses, (P_{Rsw}), describe the losses due to the load current (I_{LOAD}) flowing through the ON resistance of the switch (R_{ON}). The second loss term, (P_{CGS}), is the switching loss which corresponds to the charging and discharging of the voltage (V_{GS}) of the capacitance of the gate of each switch (C_{GS}) as they are turned ON and OFF. The frequency of switching (f_{SW}) contributes directly to the loss. Any additional power due to factors such as clock generation is accounted for in (P_Q). Finally, the ripple is determined by the maximum load current, the switching frequency and the capacitance of the flying capacitor (C_{fly}).

$$\Delta V = \frac{I_{LOAD}}{C_{fly}} . \frac{T}{2} = \frac{I_{LOAD}}{2 C_{fly} f_{SW}} \tag{4.6}$$

Eq. 4.6 are used to properly choose the switching frequency, switch sizing, and flying capacitor value. To minimize switching losses and improve efficiency, a low range of switching frequency of <50 kHz is used. Consequently, we chose a (C_{fly}) of 100nF to maintain a low ripple. The switches are sized so that the output impedance suffices for the maximum target load current. Fig. 4.3 plots the output impedance of the design across switching frequency showing the SSL and the FSL.

This design operates in the SSL. It targets operating low load current at low (f_{SW}) to maintain efficiency. To further improve efficiency, the switch size is reduced to reduce switching losses. The smaller switch size raises the impedance floor in the FSL region. Hence, the size is reduced until the operating point of the design at the (f_{SW}) is near the

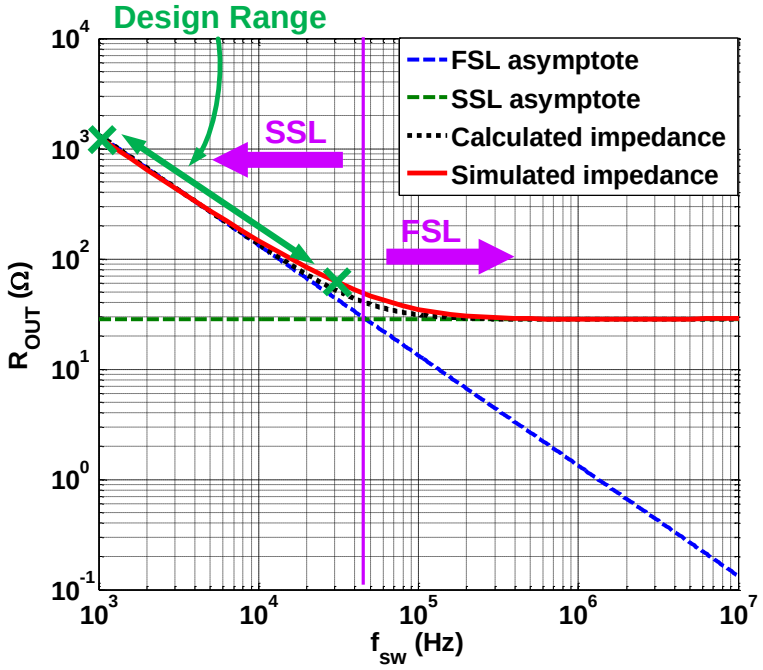

Figure 4.3: Output impedance for Series-Parallel configuration versus frequency.

corner of the FSL region of operation. Fig.4.4 shows efficiency for three different switch sizing with each operating at their corresponding (f_{SW}). When using a fixed switch size, while the peak efficiency can reach 95% at (I_{LOAD})>50μA, at a low load current of a few μA, the efficiency can drop to 20%. By allowing multiple programmable settings, the overall power efficiency of better than 95% can be maintained from 0.4μ-300μA. The output ripple of the divider is roughly constant across these different settings since (f_{SW}) coarsely scales with (I_{LOAD}) and is unaffected by the scaled switch size.

4.1.2 ON-OFF LDO

The second stage of the hybrid converter is a nonlinear LDO in which the control signals are switched digitally ON and OFF. Fig. 4.5 shows the proposed design. A clocked digital comparator serves as the error amplifier that compares the feedback voltage to the reference voltage. The comparator is followed by a buffer that drives the gate of the power transistor, MP. The power transistor, in turn, charges an external capacitor which is also the supply

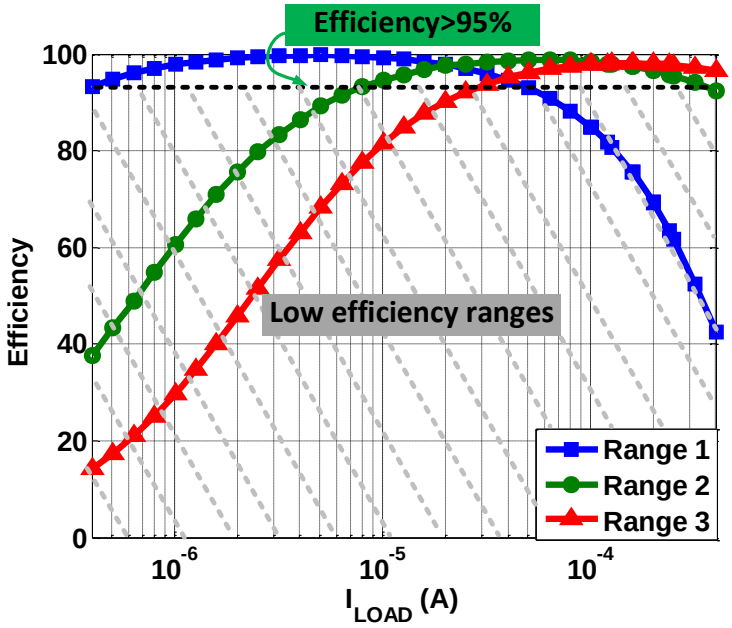

Figure 4.4: Efficiency of switched capacitor divider across load currents.

decoupling capacitance for the subsequent circuits. We choose 1μF for this capacitance as a reasonable value for good decoupling and transient response. The same clock that is used in the switched-capacitor divider is used for the error amplifier. Hence, the sampling rate of the error sampler adapts to different ranges of load current. Also, the size of the power device is different for different ranges of load current. The lowest load range operates up to 6μA with the desired dropout voltage of <30mV. The sizing for the higher load range operates up to a maximum current of 300 μA with the same dropout voltage.

This LDO has a single dominant time constant at the output with the 1μF capacitor. Due to the nonlinear switching, an inherent limit cycle is present at the output and accounts for the ripple. This ripple is similar to the nonlinearity from a hysteretic-control LDO [52] which exhibits an inherent limit cycle from an analog hysteresis error amplifier. Fig. 4.6 shows the ripple voltage as a function of the switching frequency and at different load currents. The simulation includes ESR and ESL in the simulated load. The ripple stays relatively constant across load current since the switching frequency is increased along with the load. The magnitude of voltage ripple can be determined by the charging of the 1μF capacitance

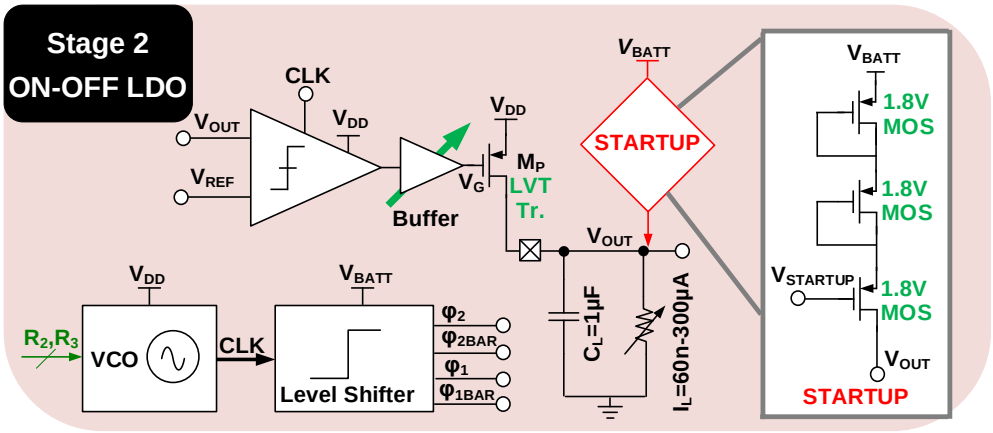

Figure 4.5: Proposed ON-OFF LDO implementation with startup circuit implementation.

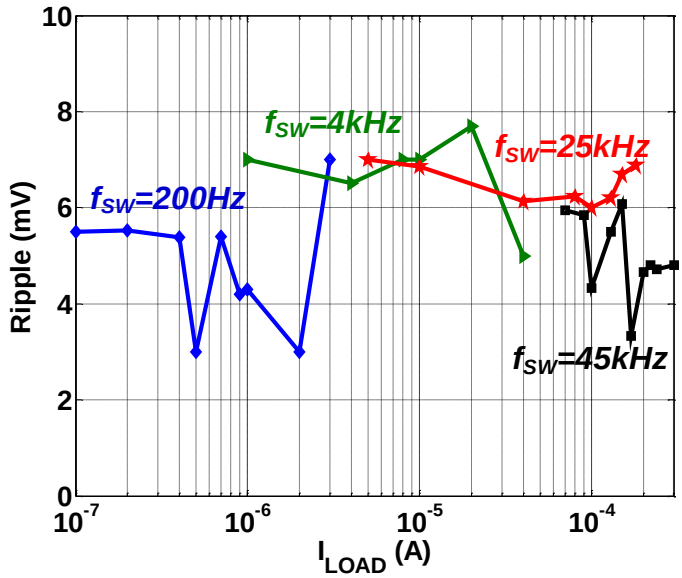

Figure 4.6: Output ripple across different load currents at different ranges of operation.

through M_P for the clock cycle of the ON pulse. This can be expressed as

$$\Delta V_{ripple_{LDO}} = \frac{I_p t_{cycle}}{C_L} \tag{4.7}$$

where I_p is the current through M_P, t_{cycle} is the comparator cycle time and C_L is the load capacitance. The load current discharges the load capacitance. The period of the ripple, Eq.

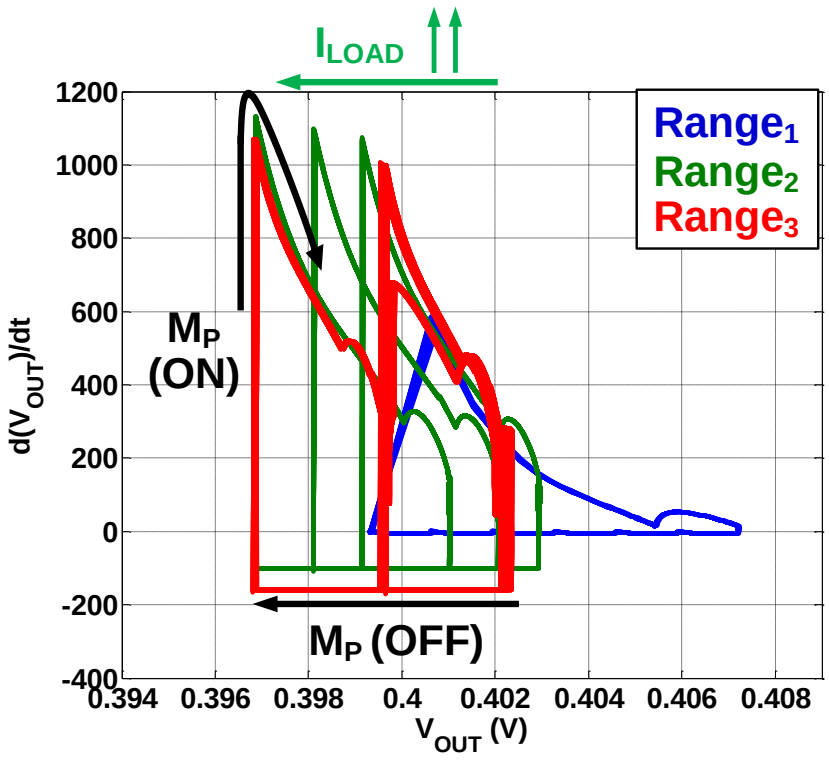

Figure 4.7: Limit cycle for the ON-OFF LDO at different ranges as load changes from 10μA-60μA-180μA

4.8, is determined by the number of cycles for the voltage to lower by the ripple

$$n = \frac{C_L \Delta V_{ripple}}{t_{cycle} I_L} \tag{4.8}$$

where I_L is the load current at the output and n is the number of clock cycles to discharge to voltage. The ripple frequency corresponds to the load. The limit cycle can be seen by plotting the state trajectory for the state variable, Vout. Fig. 4.7 shows the state trajectory for different ranges as the load current changes. The values in the figure are extracted from the current and voltage of the load capacitor. As discussed in [43], this first-order control loop is unconditionally stable across our target load range and initial voltage.

The quiescent current of the proposed LDO is due to dynamic power dissipation from the error amplifier and buffer which is similar to digital LDOs [53], [54] in which the quiescent power is primarily from the comparator and SAR logic. By using a low switching frequency,

the power dissipation driving the power transistor is small allowing us to use large device sizes and hence reduce the dropout voltage. Furthermore, since the frequency is reduced at low loads, the quiescent current roughly scales with the load current. The small dropout and low quiescent current lead to the improved power efficiency of this ON-OFF LDO.

4.1.3 Ranges Switching

The switching between the different load ranges occurs with two possible mechanisms. With many systems, a load change can be anticipated since a load element may be awakened or put into sleep mode. The configuration of the dc-dc converter can be changed before the load change. Alternatively, a load change may also be detected by sensing a change in the load current. In which case, the configuration is changed after the load changes. Both methods are investigated and the results are shown in Fig. 4.8 as the dc-dc converter's configuration is switched across four ranges of load current.

In Fig. 4.8(a), the configuration is changed before the change in the load current as it is increased with more load elements being enabled. Switching to a configuration that handles higher load current incurs very little performance penalty except for a loss in efficiency. Hence, the switching results in the output regulation being maintained with no impact on the ripple. The change from Range-0 to Range-1 shows a larger transient due to an implementation detail that is discussed in

Fig. 4.8(b) shows the behavior when the load current is being decreased. As one would expect, changing the dc-dc converter to a configuration tuned for a lower current would result in the output being unregulated or insufficiently regulated. A large perturbation can be seen until the load current is switched to match the dc-dc converter's configuration.

In Fig. 4.8(c), the configuration is changed after a change in the load current is detected. The figure shows an improved response in comparison to Fig. 4.8(b) when the load current is reduced. Hence a combination of the two approaches is desirable for smooth switching.

To sense load changes internally on the chip, the design takes advantage of the digital nature of the ON-OFF LDO. The duty cycle of the gate control signal of the driver transistor,

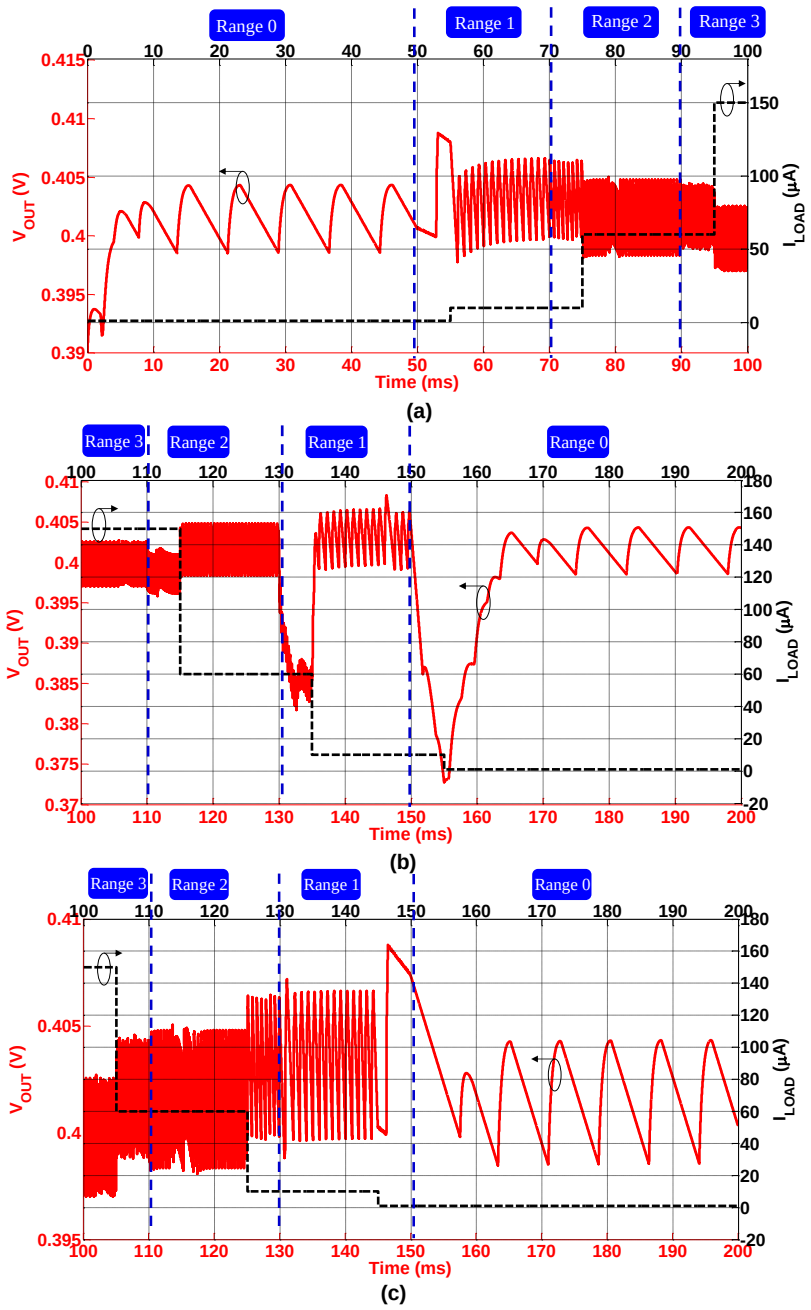

Figure 4.8: (a) Ranges switching prior to load change across all ranges while load increases, (b) range switching prior to load change across all ranges while load decreases, and (c) ranges switching post load change across all ranges while load decreases.

VG, corresponds to the load current. The duty cycle corresponds to the average of the up and down signals from the error amplifier and is implemented logically. Fig. 4.9 shows the duty cycle for each configuration of the dc-dc converter as the load current is increased. This simulation corresponds to the implementation in Section 3.2. The figure shows that even with very coarse configurations, there is sufficient overlap between the different ranges of load current to be able to use the duty cycle to control the switching between configurations. Different duty cycle thresholds are needed between the ranges as the load current decreases. For instance, from Range-3 to Range-2, the threshold can be as high as 35%, and from Range-1 to Range-0, the threshold can need to be 5%. These thresholds depend on the number of configurations. For instance, additional configurations between Range-0 and Range-1 would allow for a higher threshold. As described earlier, a change in the load current from low to high is handled by changing the configuration prior to the change in load current. If instead the configuration is changed after detecting a change in the load current, the output would not be in proper regulation until the configuration is switched. The high side of the duty cycle detection window for detecting low-to-high changes is not needed in normal operation and is kept active only as a backup to handle unanticipated high load currents. It is noteworthy that this approach to dynamically switch the converter configuration incurs a negligible power penalty due to the all-digital implementation that operates at low frequencies.

4.2 Hybrid-Converter Implementation

This section describes the implementation details of the proposed hybrid converter. Two distinct dc-dc converter blocks are built. Block-1 addresses the lowest load of the current range (Range-0). The second block, Block-2, addresses the three higher current ranges (Range-1 to Range-3). The separation is made because of the critical importance of the quiescent current and hence the control circuitry is carefully sized to minimize power dissipation for Range-0 while the control circuitry is separately designed and shared across the higher load ranges. The slightly larger ripple is evident in Fig. 4.8(a) as the system switches from Range-0 to Range-1 is due to the make-before-break switching between the two blocks. Both blocks

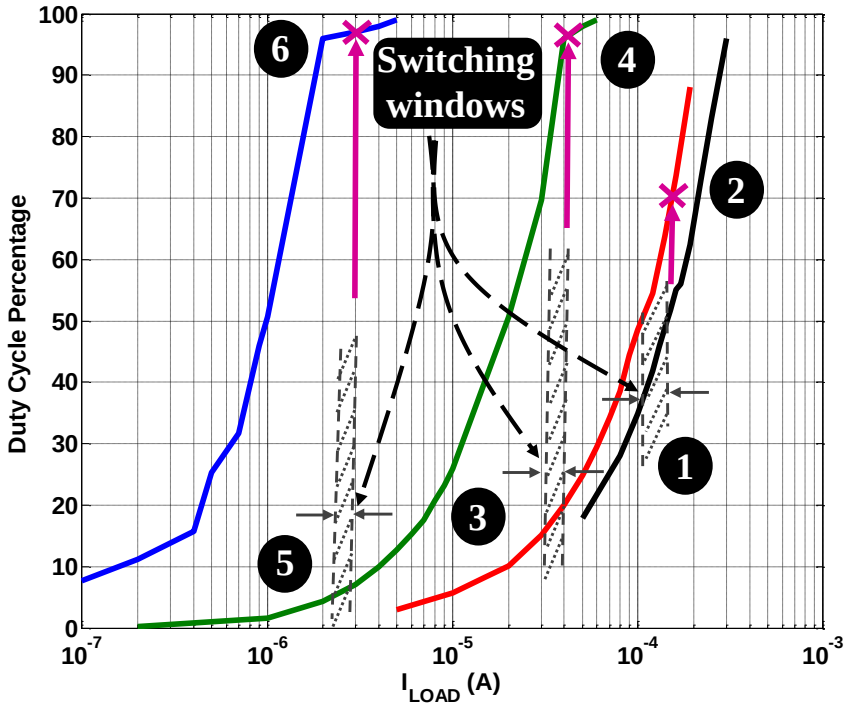

Figure 4.9: Duty cycle of voltage controlling LDO power PMOS (V_G) across different ranges and switching points between different ranges.

share the same two-stage hybrid architecture as described in Section II. The same clock source is used for both stages of the converter. This clock reuse would result in the lower quiescent current. Fig. 4.10 shows the design of the clock generator. The clocks are the outputs of an embedded relaxation oscillator. The frequency is controlled by changing the biasing current which is directly proportional to the output frequency per the Eq. 4.9.

$$f_{SW} = \frac{I_B}{C_1 V_m} \tag{4.9}$$

In Eq. 4.9, C_1 is the integration capacitor with a chosen value of 1pF, and and V_m is the inverter threshold voltage. To reduce power, inverters are used instead of amplifiers to set the threshold for resetting the capacitors. The oscillator uses the divided voltage. The oscillator signal is then level shifted to the battery voltage to drive the switched-capacitor switches.

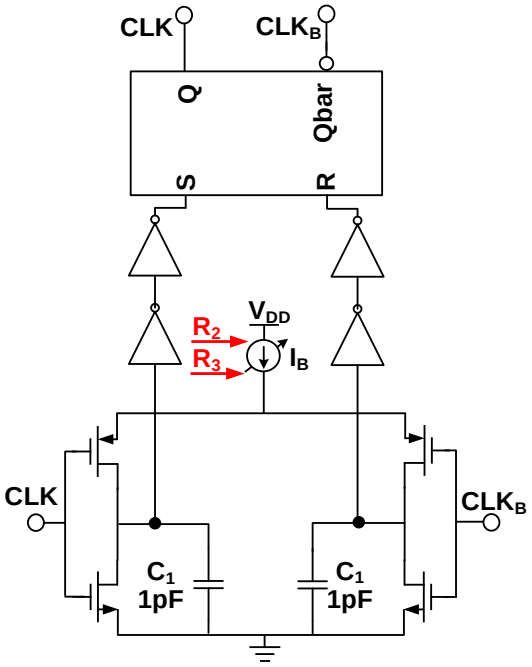

Figure 4.10: Relaxation oscillator with variable frequency control.

The higher driving voltage results in lower switch resistance. With the use of temperature compensation in the bias current, the frequency of oscillation can deviate by <15% across a temperature range of 0°C to 80°C. Simulated results show the efficiency variation with this deviation across the ranges of operation to be <3%. The oscillator of Block-1 is designed for 200Hz. For Block-2 to satisfy three ranges of operation, three bias currents are set by two control registers, R2 and R3, to produce 3.3 kHz when neither registers are set and 23 kHz and 42 kHz when R2 or R3 is set respectively. The power consumption of the oscillator and clock buffers across the different frequencies is 30nA for Block-1 and 70nA-160nA for Block-2.

The first stage of the converter divides down the battery voltage by three to an output a few 10's of millivolts above the target supply voltage of the load. Block-2 implements the programmable switch sizing based on the load range. Fig. 4.11(a) shows the implementation of each switch and the circuit that selects the switching signal from the clock source. Each switch is an array of multiple fingers (each finger with a size of 2μm/150nm). The switches

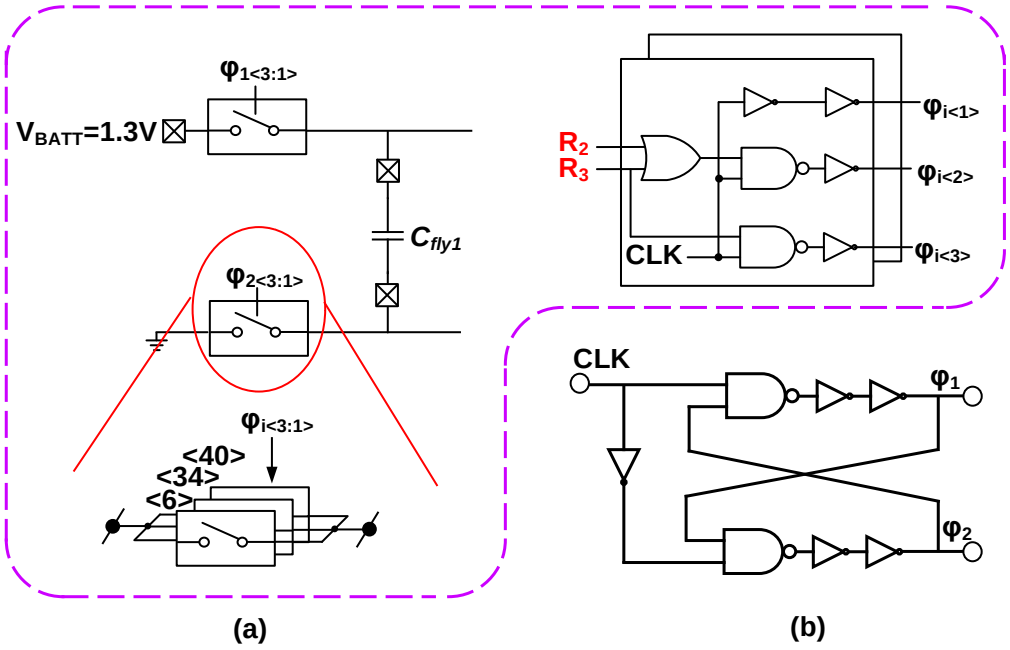

Figure 4.11: (a) Variable switch size for optimizing the overall efficiency, (b) non-overlapping clock generator.

use 1.8-V transistors to withstand the high voltage down conversion without the risk of breakdown. The same two registers, R2 and R3, which control the clock frequency also control the selection of switches to enable Range-2 and Range-3 respectively. These control signals increase the number of minimum-sized transistor fingers from 6 to 40 in the case of activating Range-2 and to 80 when activating Range-3. A cross-coupled NAND structure, as shown in Fig. 4.11(b), is used to produce non-overlapping clocks for the two clock phases, ϕ_1 and ϕ_2. This avoids short circuit current through the switched-capacitor divider.

Several design features enable low quiescent power for the second stage of the hybrid converter. The control circuitry is built using a low-V_T transistor to support low-voltage operation down to 0.35V. The clocked comparator is a double-tail latched comparator and consumes no static power, as shown in Fig. 4.12. Since the input capacitance of the comparator is not critical, the comparator does not have explicit offset compensation and is sized to have a voltage offset of <6mV.

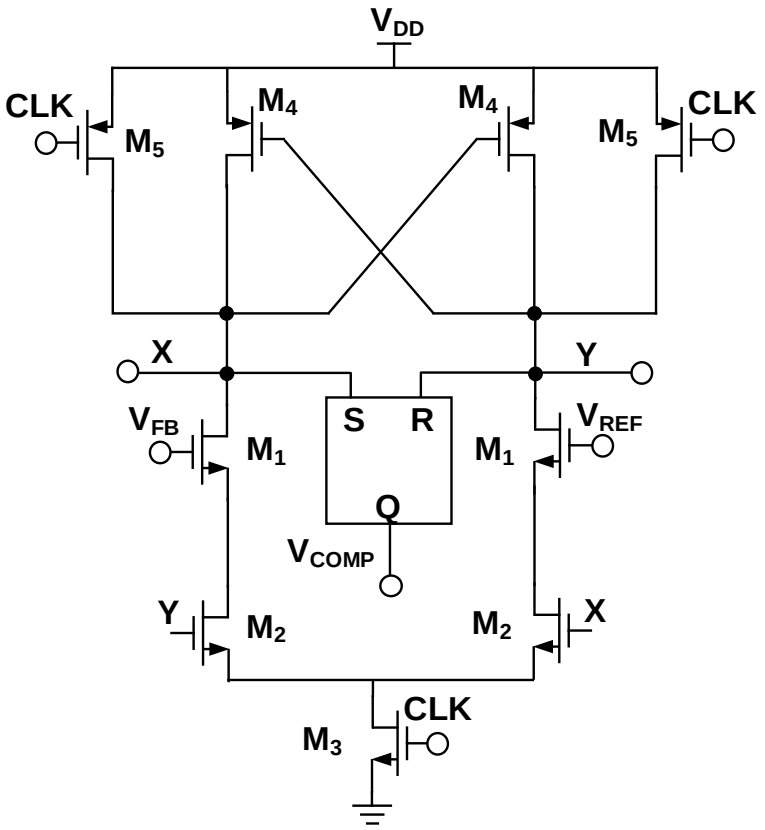

Figure 4.12: Double tail latched comparator circuit implementation.

The overall offset of the hybrid converter is simulated using Monte-Carlo simulation for device mismatch without temperature or supply variations, and the result is shown in Fig. 4.13. A buffer is used at the comparator's output for several reasons. The buffer decouples the capacitance at the gate of the PMOS driver from the comparator output. By reducing the capacitance at the comparator's output, the crowbar current is reduced. The buffer also serves to control the slope of the signal driving the gate of the PMOS output stage. The size of the PMOS driver is 6μm for Range-0 and 160μm for Range 1-3. The PMOS driver sizing targets dropout voltage of <30mV at maximum load condition. Nearly all of the building blocks are digitally switched and hence the control circuitry consumes no static current and leads to good efficiency.

A startup circuit, as shown in Fig. 4.5, is used upon initialization of the system and

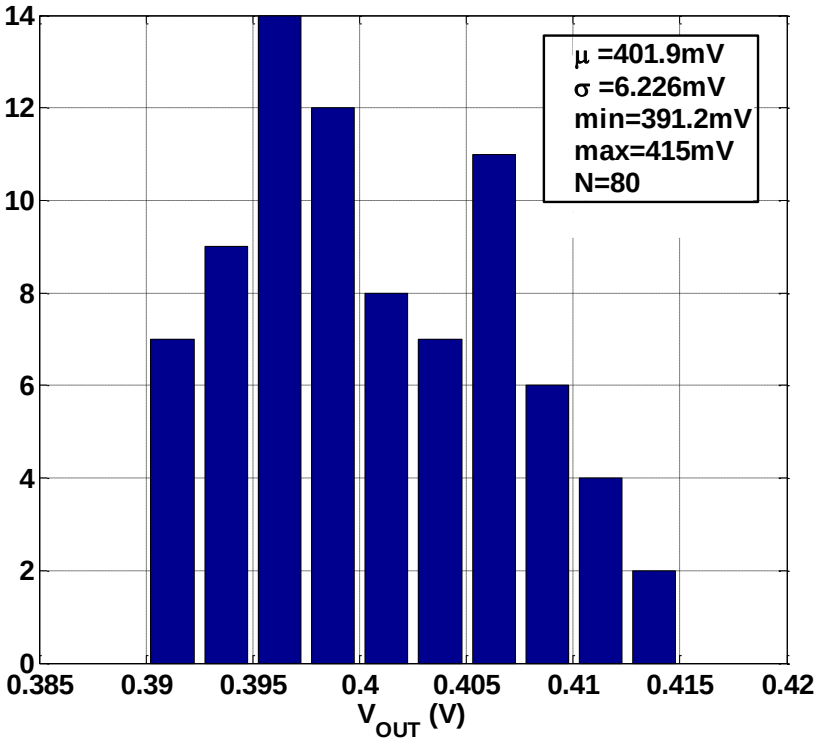

Figure 4.13: Output voltage offset of the overall converter across 80 runs.

is disabled once the system is in operation. Minimally-sized, diode-connected devices step down the battery voltage to produce a startup voltage. During startup, the output capacitor of the switched capacitor stage and the output capacitor for the LDO are charged to the startup voltage. The charged output enables the oscillator that starts the voltage division and feedback regulation.

4.3 Summary

In this chapter, we proposed a hybrid power management unit for IoT leaf node. The design incorporates multiple variable and select-able components to dynamically optimize efficiency across different ranges of load current. The basic dc-dc converter is composed of two stages; the first stage is a switched-capacitor dc-dc converter and the second stage is an ON-OFF LDO. The system achieves high power efficiency exceeding 80% across wide

load ranges 0.4μW to 100μW at an output voltage of 0.4V. The architecture demonstrates the possibility of achieving a high efficiency even at very low load currents and maintains the efficiency across a wide range of load currents. The system achieves a fast transient response that is limited by the decoupling capacitance at the output and excellent tracking for reference voltage changes with nearly no overshoot or undershoot. The proposed design is implemented in 28-nm CMOS and has an active area of $0.012mm^2$ across all blocks. With the exception of the capacitors, the entire design is fully integrated and allows for a system-on-chip integration of the PMU with the load application. The architecture can be customized to different battery voltages, output voltages, and current load. It is attractive for un-tethered systems that continuously monitor their environment at very low power levels, i.e. wake-up receivers, and react with varying degrees of higher power when triggered.

In the next chapter, we introduce a Coarsely-Quantized Class-D LDO which covers the high power ranges for the radio. The range switching occurs as the main radio receives the wake-up signal to fast startup the LDO. The proposed LDO achieves no overshoot or undershoot at sudden load increase occurring at startup and shutting down.

CHAPTER 5

Coarsely-Quantized Class-D LDO

The fast startup requirement for the main radio of the leaf node imposes challenges to the PMU design. PMUs rely considerably on low-dropout (LDO) regulators to provide an output voltage at different levels with the maximum possible efficiency. For fast transient changes, the LDO requires fast control loop along with good control over the output voltage. As discussed in Chapter 4, the adaptive range change as the load increases optimizes switch sizes to operate at the maximum power efficiency. We extended the switching mechanism to the main radio regulation using the proposed LDO. In this chapter, we show the system analysis and the circuit implementation of a novel Coarsely-Quantized Class-D LDO. The implementation is based on a non-linear comparator which drives class-D control at which it controls the output stage. The output stage is an FVF where the control transistor is driven using (MLPWM) signal to allow fast loop dynamics and smaller quiescent current.

In this chapter, we discuss the LDO design considerations for a fast startup. We start with the design consideration in Section 5.1 where we discuss the coarse step of control for the FVF stage, the proposed feed-forward path, and the stability of the system. In Section 5.2 we show the system implementation and the circuit design challenges for different blocks. The measurement results are presented in Section 6.3 with the chip micrograph built using 28nm CMOS technology.

5.1 System Design Considerations

The architecture of the proposed design is shown in Fig. 2.5 (c). A clocked comparator serves as the error amplifier operating at a sampling rate (f_{sw}) of approximately 100MHz.

The clock is from an internally generated timing source. Instead of integrating the error output with small voltage increments at V_G, large coarse control steps are maintained at V_G leading to a PWM signal. The final output voltage at the output of the FVF buffer reflects the average of the PWM signal with some voltage ripple due to the inherent limit cycle. The coarse step size is a trade-off between ripple and loop bandwidth. This section first discusses the choice of the coarse control steps along with the use of the FVF output stage to extend the loop bandwidth and reduce output ripple. The FFTDP is then discussed as an addition to the FVF output stage to reduce the quiescent current and maintain small voltage ripples at high load conditions. A discussion on the stability of the loop is provided last.

5.1.1 Coarsely-Quantized Class-D Control with FVF Output Stage

Fig. 5.1 compares the output stage of a conventional class-D LDO with the proposed architecture. A class-D LDO introduces two open-loop poles: the first is at the output and the second is at the gate of the power transistor. Any additional poles due to the error amplifier or any feedback delay from the controller further degrade the phase margin of the feedback loop. In a conventional class-D design, due to the large device size of the power transistor, the dominant open-loop pole is at the gate of the power transistor. Compensation [69] is needed to provide sufficient pole splitting to ensure closed-loop stability. The resulting loop bandwidth is often below 100 kHz. Pushing the speed of the transient response at high load current transitions to improve overshoot/undershoot often leads to a reduced phase margin and stability issues. Fig. 5.2 illustrates a simulation in which the output exhibits >110mV overshoot when the load current changes from 0-250mA in 7ns.

The proposed class-D control moves the dominant open-loop pole to the output of the LDO. The response time (effectively the pole frequency) at the gate control node of the output buffer, V_G, is pushed to be substantially faster than the output node. Continuous-time feedback analysis can be used to approximate the behavior of the LDO and develop an intuition on the operation. The dominant open-loop pole at the output can be expressed as:

$$P_1 = \frac{1}{C_L(R_{OUT}||R_L)} \tag{5.1}$$

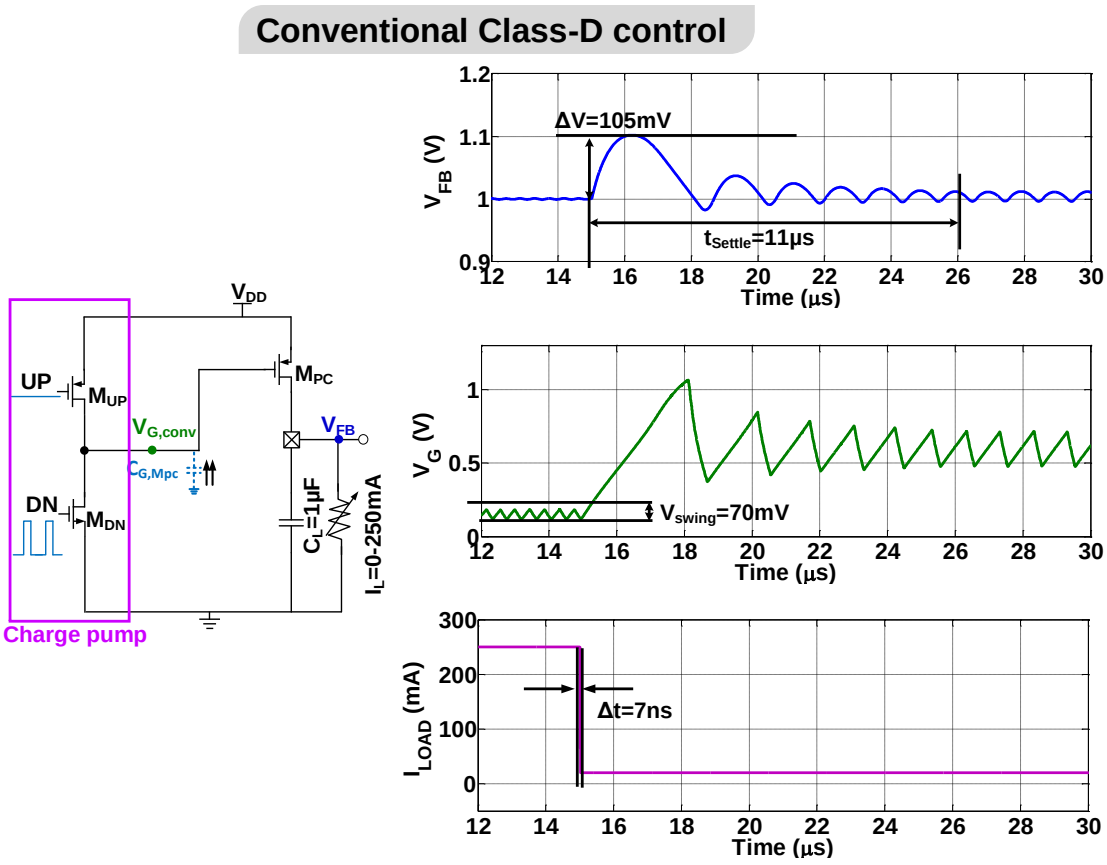

Figure 5.1: Conventional class-D control charge pump and output stage and simulation waveforms

The response of the internal node can be approximated by

$$P_1 = \frac{1}{C_{GMc}R_{eq}} = \frac{f_{sw}Q_{step}}{V_{swing}C_{GMc}} \tag{5.2}$$

Where f_{sw} is the sampling rate of the error amplifier, C_{GMc} is the gate capacitance of the output buffer, V_{swing} is the voltage swing available for change at the gate, V_G, and Q_{step} is the amount of charge per step. Fast response time is achieved with (1) operating at the high switching frequency, f_{sw}, of the control path and (2) injecting a large charge, Q_{step}, onto the node V_G per cycle while using a small gate capacitance for a given output impedance. For a given output capacitance, the resulting closed-loop bandwidth as compared to a conventional class-D is considerably higher, as discussed in the following section, leading to improved transient response and overshoot. The stability analysis section discusses a

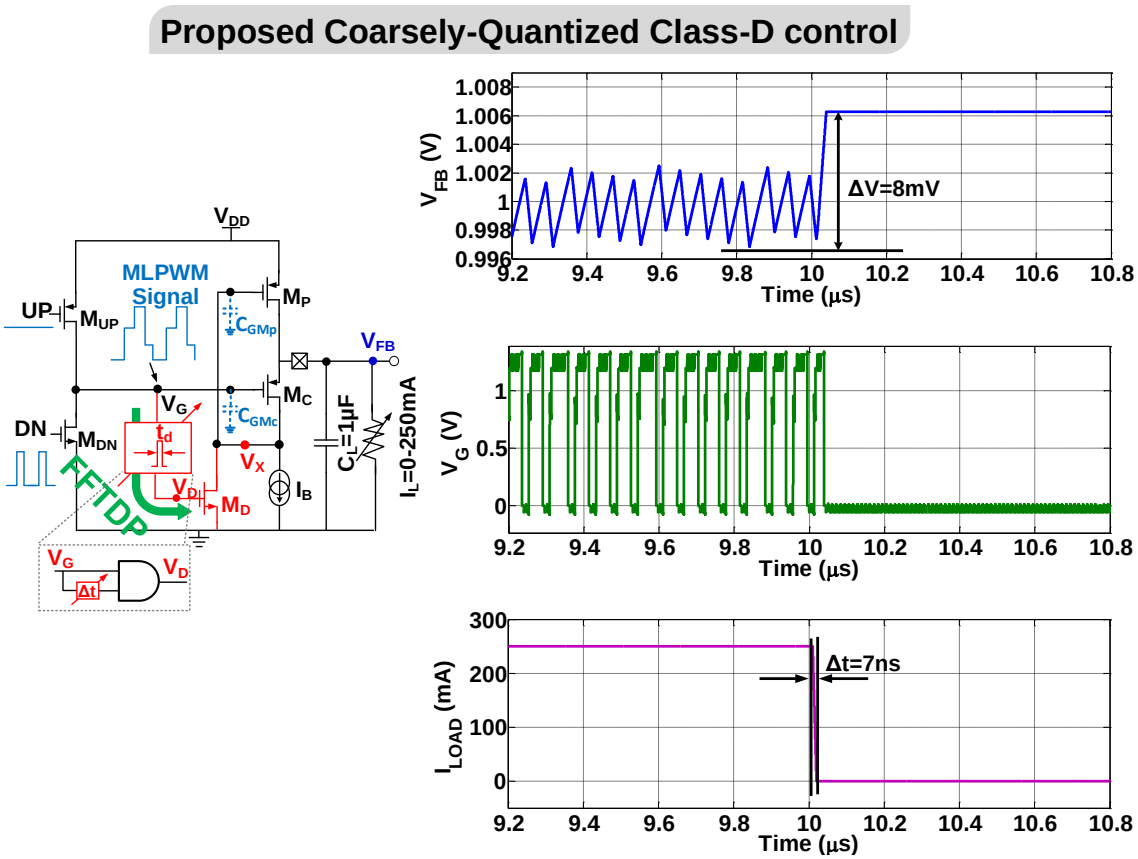

Figure 5.2: Proposed Coarsely-Quantized Class-D control with FVF output stage and simulation waveform

linearized discrete-time stability analysis of the proposed LDO.

The drawback is that the change in charge at the gate of M_C every cycle translates to dither at the output appearing as output ripple. This tradeoff is shown in Fig. 5.3. Larger V_{step} results in lower overshoot but with larger ripples at the high loads. Smaller voltage steps approach the behavior of analog control and result in larger overshoots and smaller ripples. Our design point balances fast response with reasonable ripples by adopting a few multi-level voltage steps by choosing coarse steps of roughly $0.5V_{DD}$ to modulate the gate control voltage, V_G. The sampling rate of the proposed class-D controller is designed to operate at approximately 100MHz. With large steps, the coarse-quantization for the control signal is essentially 4 control levels of the gate control which are 0, V_{1P}, V_{2P}, and V_{DD} as shown in the timing of Fig. 2.5(c) and Fig. 5.2. Due to the size of the coarse steps, the

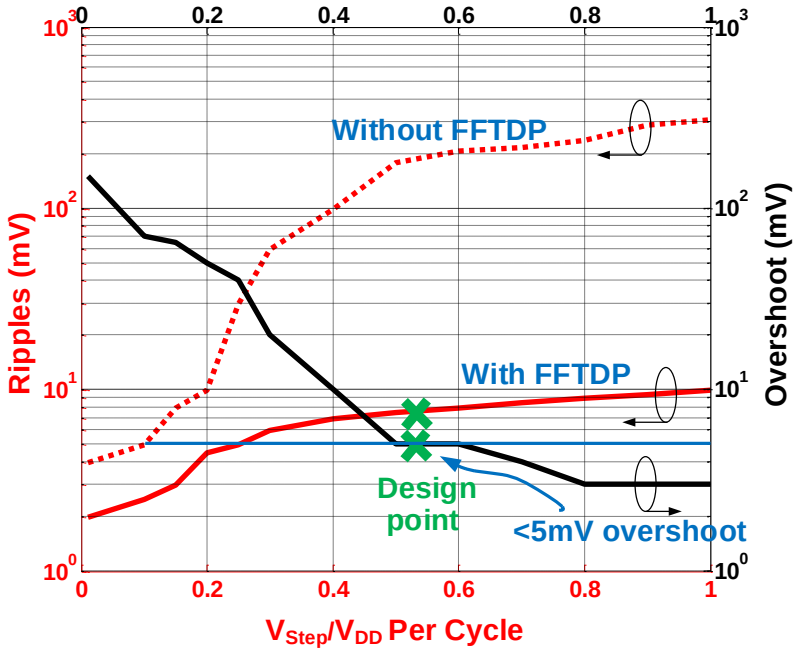

Figure 5.3: Impact of V_{Step} on transient behavior with and without FFTDP.

resulting waveform of V_G is a 4-level PWM signal that sets the value of the output voltage.

The design uses an FVF buffer stage to reduce the input capacitance of the buffer enhancing the loop dynamics. The flipped voltage follower output stage with the charge pump is shown in Fig. 5.2 to compare with a conventional class-D design. The FVF output stage has an output impedance lowered by the gain of the shunt feedback loop [70].

$$P_1 \approx \frac{1}{g_{mMc} g_{mMp} r_{oMc}} \tag{5.3}$$

This gain boosting of the FVF results in a smaller gate capacitance, C_{GMc}, for a target R_{OUT}, as compared to the gate capacitance C_{GMc} of conventional class-D design. In addition to improving the internal node's response, the charge pump would dissipate less power when changing the voltage on the gate control node and hence improve efficiency.

5.1.2 Feed Forward Control for Power Transistor

The driving capability and bandwidth of an FVF buffer depend on its bias current (I_B). This bias current provides the internal drive to pull down the large gate capacitance of the PMOS transistor (C_{GMp}). Having a constant high bias current at the tail of the FVF output stage leads to poor current efficiency, an important metric for LDOs.

This design improves efficiency by reducing I_B and at the same time introducing a secondary control path to directly control and turn on the PMOS transistor, M_P, to compensate for the decrease in bandwidth. We refer to this path as a feed-forward transition detection path (FFTDP). As shown in Fig. 5.2, a rising transition of the output is detected when the PWM voltage at the gate of M_C crosses a threshold near $V_{DD}/2$. The crossing triggers a short pulse, V_D, which turns on M_D, an NMOS transistor in a feed-forward path to pull "LOW" the gate of M_P. Hence, the gate of M_P is pulled "LOW" quickly instead of relying on I_B and, as a result, speeds up the rising transient response of the LDO.

Fig. 5.4 shows I_B impact on transient behavior at maximum load conditions. Since the driving device, M_P, is sized to supply the large load current, its gate capacitance can be large and is only discharged by I_B. So, reducing I_B slows the turn-on of M_P under a load transient. The time constant from the discharge time would result in a slower loop response. Reducing I_B also lowers the bandwidth of the FVF. The combined result is an increase in output ripple. The proposed FFTDP, as shown in the figure, has the significant enhancement of the quiescent power (100x) for the same ripple level. By introducing FFTDP without increasing I_B, similar ripple performance and overshoot (<6mV and <1mV respectively) as maintaining a high I_B are achieved. It is noteworthy that the design only detects the rising transition at the output. For the falling transition, M_P is turned off quickly by the class-D controller when it turns on M_C and shorts the gate of M_P to the output voltage.

The pulse width of the FFTDP signal, V_D, and the size of the M_D device determine the amount the gate voltage of M_P is discharged and the speed of the discharge. Transients at high load currents require M_P to be turned fully on as quickly as possible. Reducing the pulse width results in larger ripple and slower transients. At low load currents, turning

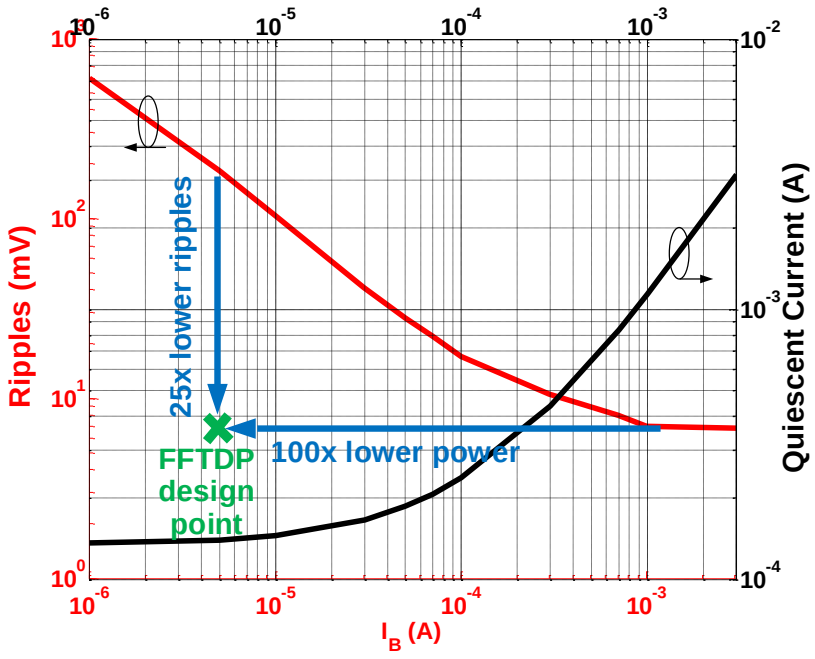

Figure 5.4: I_B impact on transient behavior without FFTDP and improvement due to FFTDP.

M_P on for a long duration results in charging the load capacitance excessively and hence increasing ripple. Since the control loop is being clocked at f_{sw}, the pulse width would need to be longer than $1/f_{sw}$ for the ripple to be larger than the inherent ripple of this LDO. Hence, in this design, we choose a pulse width sufficient to discharge the gate of M_P and $< 1/f_{sw}$.

To illustrate the operation, Fig. 5.5 shows a line transient simulation from 1V to 0.8V and then raised back to 1V in <10ns at 170mA load for different load capacitors. As expected, the speed of the transient and the amount of ripple is directly proportional to the capacitance. In the design described in the next section, a 1μF external capacitance is chosen which is sufficient for supply decoupling for most LDO applications.

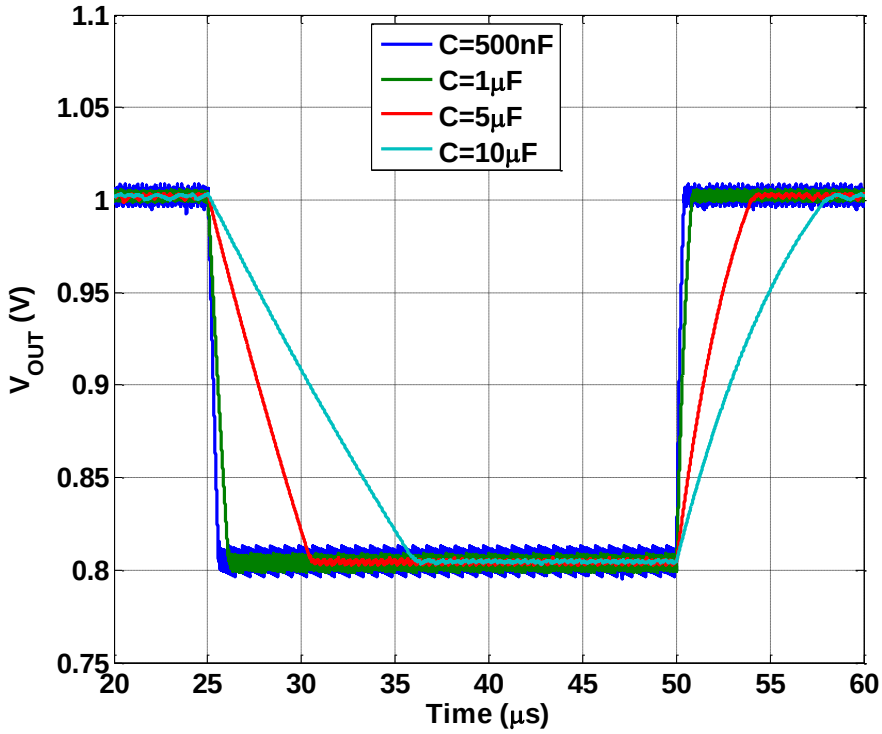

Figure 5.5: Simulated line transient response at different load capacitance.

5.1.3 Stability Analysis

With the use of a sampling comparator as the error amplifier and large control steps, the proposed design is essentially a bang-bang controller. To maintain stability, the response of the control loop is dominated by the pole at the output node. All other nodes and elements such as the output buffer, the class-D controller, and buffer driving the MLPWM signal, and the error comparator have much faster response times leading to a first-order loop that is unconditionally stable. Furthermore, the total delay through the control loop is maintained to less than two cycles to limit the impact on the phase margin.

Fig. 5.6 shows a state-space simulation including the output voltage, V_{OUT}, and the derivative, dV_{OUT}/dt. The state-space is simulated in a manner similar to [74], [75] by taking the current that flows through the load capacitor (i_c=C_L (dV_{OUT})/dt), normalizing it by C_L for the derivative and then plotting the output voltage versus its derivative at full

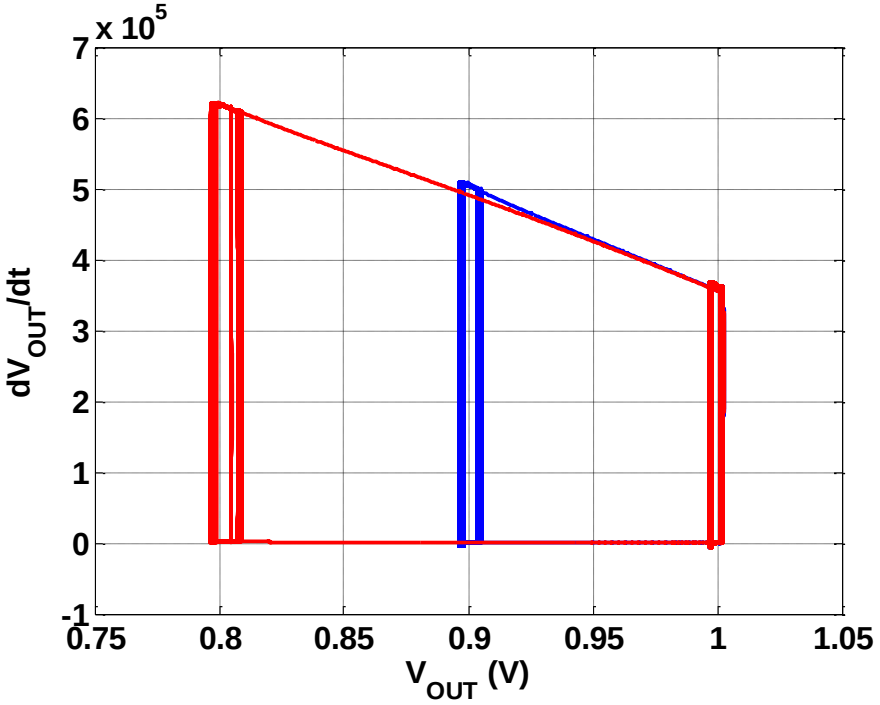

Figure 5.6: Limit cycle simulation results at different reference voltage changes

load conditions. The reference voltage is changed from 0.9V-1V and 0.8V-1V at full load. As expected from a first-order bang-bang controller, a hysteretic response in the form of a limit cycle can be seen at the steady-state operating points that correspond to the output ripple. The output transient converges nicely to the limit cycle with ripples below 10mV.

A more rigorous analysis of the loop can be approximated used a small-signal linear discrete-time model similar to ones employed in bang-bang phase-locked loops (BBPLL) [76], [77]. The system block diagram of Fig. 5.9 can be reduced to Fig. 5.7. The error amplifier followed by the current DAC and pulse generator can be reduced to G_c, $G_{Class-D}$, and a delay. The gain, G_c, linearizes the nonlinear decision of the clocked comparator similar to that of a bang-bang phase detector [78]. The total gain includes any adjustments as the comparator decision is translated into current then into a pulse width, ΔT_1. The delay, $z^{-0.5}$, is due to the current integration and pulse generation. The pulse width, ΔT_1, determines the ON-time for the charge pump to charge the node, V_G. The gate voltage, V_G, is the

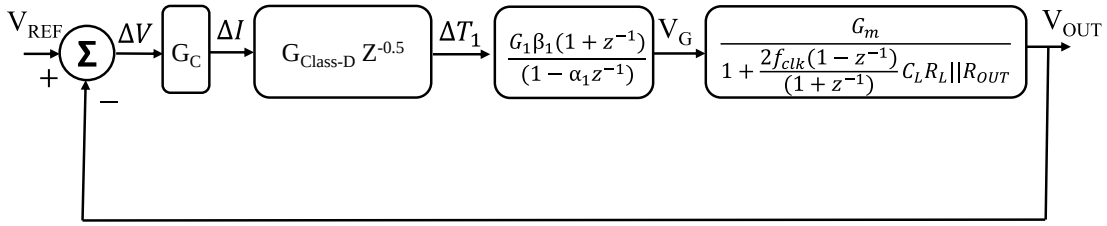

Figure 5.7: Class-D FVF system modeling.

input of the FVF. The s-domain V-I transfer function of the FVF is transformed into the z-domain using the bilinear transformation. The overall open-loop transfer function (A) can be written as:

$$A = \frac{G_c G_{Class-D} G_1 \beta_1 G_m (1 + z^{-1}) z^{-0.5}}{(1 - \alpha_1 z^{-1})(1 + \frac{2f_{clk}(1-z^{-1})}{(1+z^{-1})} C_L R_L || R_{OUT})} \tag{5.4}$$

In the expression,

$$\beta_1 = \frac{1}{2C_G V_{swing}/Q_{step} + 1} \tag{5.5}$$

, and

$$\alpha_1 = \frac{2C_G V_{swing}/Q_{step} - 1}{2C_G V_{swing}/Q_{step} + 1} \tag{5.6}$$

introduces the second pole in the system which is dependent on the step size used and the gate capacitor associated with M_C. The larger the gate capacitance C_G and the smaller the step size would push the second pole towards the dominant pole causing phase margin degradation.G_1 is the gain of the integrator. The dominant pole at the FVF output is depended on the load capacitance and resistance at the output. The gain of G_c $G_{Class-D}$ is $\approx$40,$G_1\beta_1$ is $\approx$0.8, and G_m is $\approx$ 400mΩ^{-1}.

In Fig. 5.8, we use this parametrized model and plot the open-loop gain and phase margin. The same plots for the s-domain approximation of Section 4.1.1 is overlaid on the figure to show correlation. With a load current of 250mA, the gain is 25dB and the phase margin is 86° which is considerably higher than the 40° phase margin of a conventional class-D [69]. The result matches the estimate from the transient behavior measured for the system in Fig. 5.5.

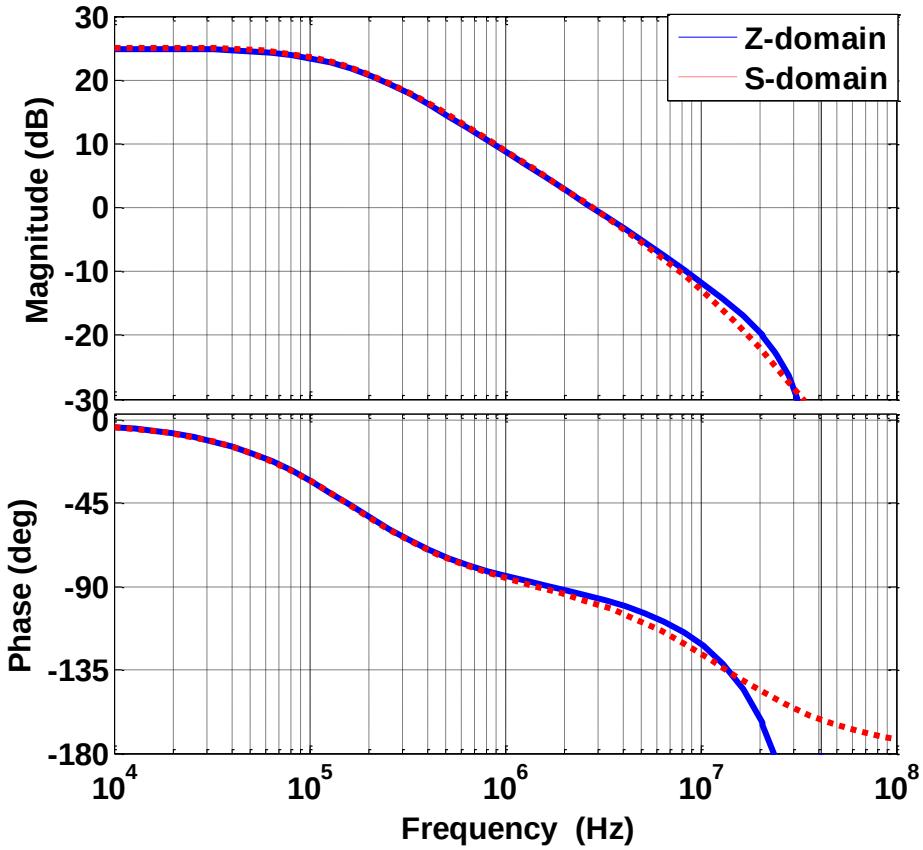

Figure 5.8: System open-loop gain and phase margin in Z-domain and S-domain pole approximation.

5.2 Coarsely-Quantized Class-D Implementation

The detailed implementation of the proposed LDO is shown in Fig. 5.9. The error amplifier is a Strong-Arm Latch [73] followed by an SR latch to hold the comparison result for the duration of the clock cycle. The comparator is sized to ensure a 3σ offset of <1% of the regulated voltage based on Monte-Carlo simulations.

The design of the class-D controller is shown in Fig. 5.9 and the timing diagram in Fig. 5.11. The 1-bit current DAC drives a current to either P1 or N1 depending on the polarity of the error. The two nodes, N1 and P1, are initially set at V_{DD} and GND respectively. The

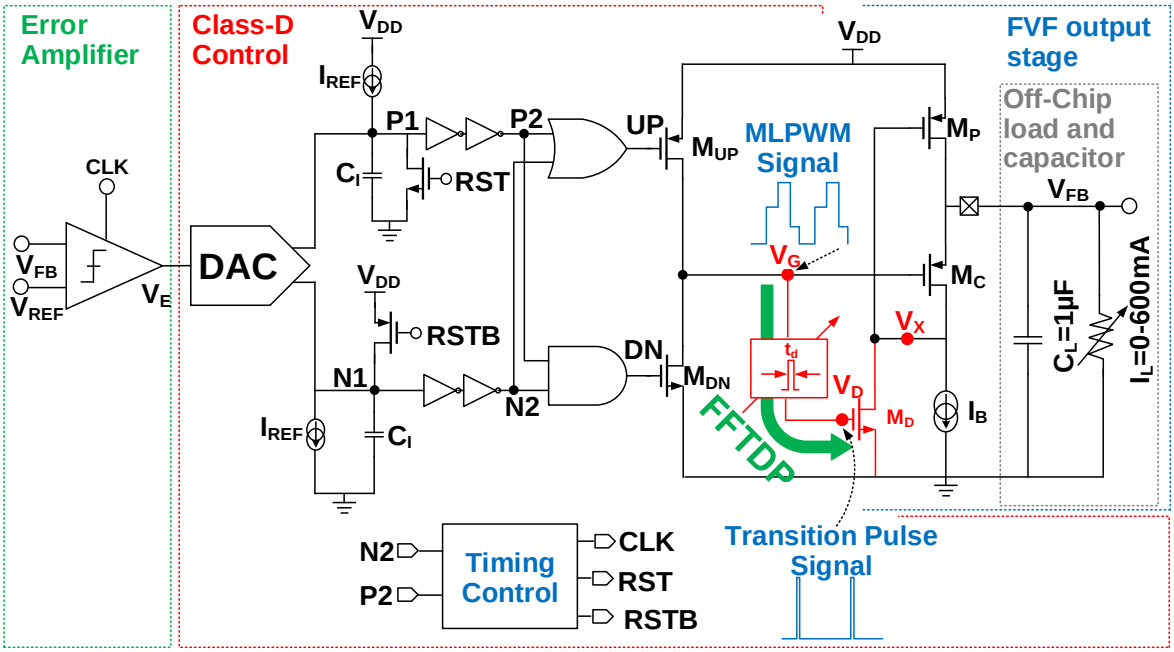

Figure 5.9: System architecture for the proposed Coarsely-Quantized Class-D FVF LDO.

DAC current adds to I_{REF}, which is integrated by the capacitor (C_I) on P1 and N1. The integrated waveform, in turn, determines the duration of the UP/DN pulses. For example, in the case of increasing the charge on V_G, the DAC current is directed to discharge N1. N1 discharges past an inverter threshold faster than P1 which is charged only by the reference current. The buffered nodes, N2 and P2, transition when N1 and P1 crosses a logical threshold. The pulse-width difference between N2 and P2 are reflected in the resulting UP pulse that drives a push-pull buffer that delivers an upward step to V_G. The slope of charging and discharging for both branches determines the pulse width of the generated signal as the current is either being added or subtracted from the current DAC according to the following equation, t=$(C_1 V_{DD}/2)/(I_{REF} \pm \Delta I)$. Where (t) is the rise time for the voltage at the node (N1) or (P1) until it reaches the threshold of switching. The voltage step for each error sample depends on the pulse width and the size of the M_{UP} and M_{DN} transistors. This pulse width is also designed to be controllable by adjusting the DAC current relative to the integrator reference current (I_{REF}).

The timing-control circuit is shown in Fig. 5.10. The clock generation circuit is similar to

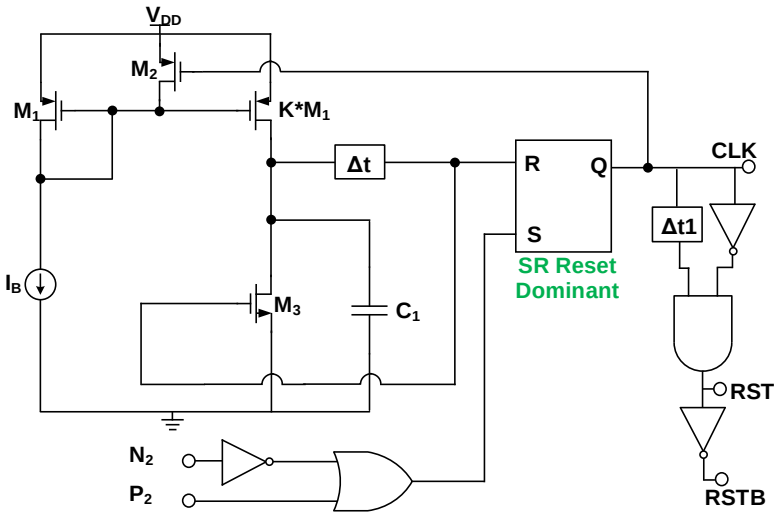

Figure 5.10: Timing control circuit implementation.

a relaxation oscillator. The "HIGH" half cycle of the sampling clock is based on the charging time of capacitor C_1. When C_1 is charged above a logical threshold, the rising edge triggers an SR latch to reset the output clock "LOW". The same rising edge from C_1 after a delay,Δt , self-resets the capacitor, C_1. The falling edge of CLK is the sampling clock for the error comparator. It is used as the input to a pulse generator that produces the RST signal. The pulse width of the RST signal is determined by a delay, Δt_1. The "LOW" half-cycle of the sampling clock is determined by the class-D control circuit. The RST signal is the signal that resets the integration nodes N1 and P1. When both nodes complete their current integration with N2 (LOW) and P2 (HIGH), the reset for the SR latch is triggered causing the rising edge of CLK. The cycle then repeats. By including the delay of the class-D control inside the clock generation, the timing relationship of each sample and the resulting voltage step is maintained. The frequency of CLK, f_{sw}, can be adjusted by changing I_B.

The operating frequency of the system is chosen so that that the output ripple with FFTDP is below 10mV. A frequency sweep for the class-D is shown in Fig. 5.12 showing large overshooting at low-frequency operation with low quiescent current consumption. As the frequency of operation increases the output ripples and overshot reduces gradually. In this design, we target output ripples $<$10mV at maximum load which achieves a 150μA

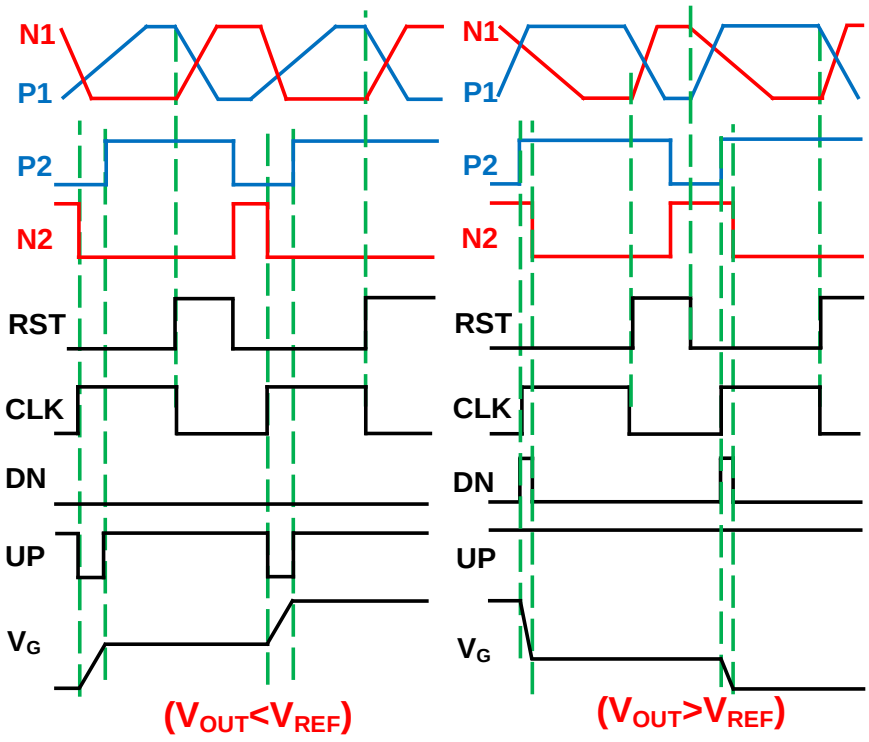

Figure 5.11: Timing diagram for Coarsely-Quantized Class-D control operation.

quiescent current which results in a current efficiency of >99.9%.

The FFTDP is generated by taking the gate control voltage V_G of the control transistor M_C into a rising edge pulse generator. The pulse generator is designed with multiple pulse width options that are programmed at the initial start of the LDO according to the chosen operating frequency. The generated pulse is designed with a pulse width of T_D>5×$R_{ON,MD}$×$C_{G,MP}$ to fully pull down the gate voltage of the power transistor M_P. Where T_D is the pulse width of the pulse, R_{ON}, M_D is the on-resistance of the M_D transistor and$C_{G,MP}$ is the gate capacitance associated with the large power transistor.

Fig. 5.13 shows the sensitivity to varying the pulse width of the FFTDP across a wide range of loads from 1mA-200mA. The pulse width is varied within one clock cycle of 83MHz from 100ps to 2ns. The simulation shows the effectiveness of FFTDP at pulse width >400ps in limiting voltage ripple to <6mV. This pulse width is sufficient to fully pull down the gate of M_P which stays LOW for the entire cycle allowing current to flow to the load until the

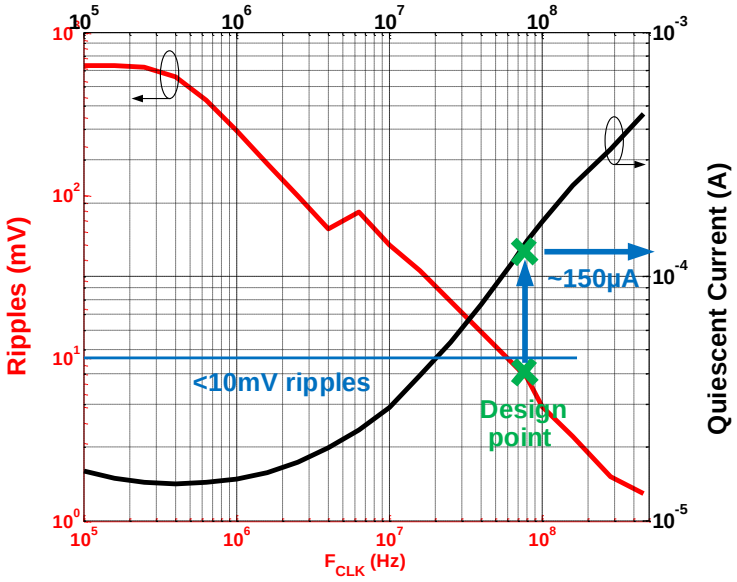

Figure 5.12: Clock frequency impact on the transient behavior of ripples and quiescent current.

next clock cycle. There is no excessive charging of the output at low loads (i.e. 1mA) since the error amplifier senses when the voltage exceeds the regulated voltage and turns off the power transistor, M_P, by turning on M_C in the next clock cycle.

The proposed LDO is designed using thick-oxide 1.8-V NMOS and PMOS transistors in 28-nm CMOS technology. The transistor thresholds are approximately 0.5V. The FVF output stage sizes are selected to be 6800μm/0.15μm for the M_P and 100μm/0.15μm for the M_C to supply a maximum load current of 600mA at a maximum dropout of 500mV. To minimize quiescent current, the FVF is designed with a DC bias current of only 5 μA.

At load currents below 0.6mA, the design can accommodate a range of inputs between 1.2 to 1.8V and can provide an output with dropout below 10mV. Simulations show a power supply rejection ratio (PSRR) of 15dB. Our design specification includes an output capacitor of 1μF with low ESR and. The overall size of the output stage is 6x smaller compared to designs that use PMOS as the output stage as in [71] with the same maximum load.

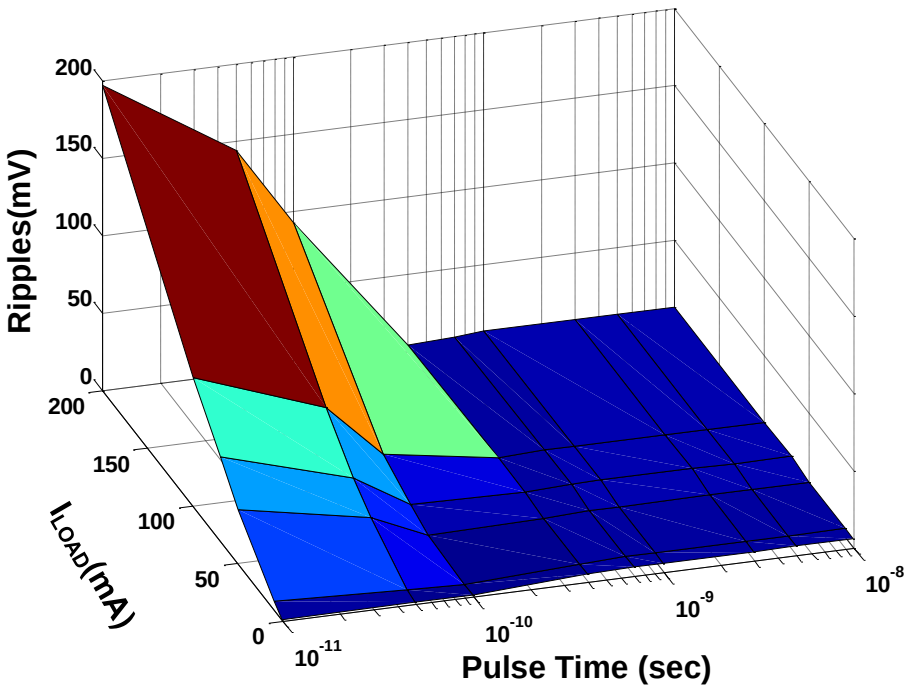

Figure 5.13: Pulse width variation across different loads and the output ripples results at f_{sw} of 83MHz.

5.3 Summary

In this chapter, we presented a novel class-D control with the FVF output stage. We introduced an MLPWM gate control signal and combined it with a novel FFTDP which results in having good load regulation and fast transient response. No overshoot or undershoot is observed beyond the inherent hysteretic ripple of the bang-bang controller. The settling time for this load change is 280ns which is ≈10x faster than settling of prior work at the same load level. The fast settling time helps the system startup as the main radio chip is enabled at a short period of time. The LDO achieves static load regulation of 70μV/mA. The LDO has PSRR of <-25dB at 10MHz. The LDO achieves FOM_V of 1mV and 99.93% efficiency. The controller occupies a small area of $0.004mm_2$ and built using 1.8-V transistors in 28-nm CMOS technology and the same technique can be used for low voltage devices to regulate

output voltage sub 1V.

This chapter concludes the second part of the dissertation addressing the power management challenges for the battery-powered leaf node. We covered the challenge of voltage regulation at the low-load condition and the voltage regulation at the fast startup of the main radio. In the next chapter, we show the measurement and experimental results from various test chips for the systems analyzed so far in this dissertation.

CHAPTER 6

Experimental Results

This chapter demonstrates the details of the experimental results of the for chips. The first chip is an ultra-low-power wake-up receiver prototype that is based on CMOS implemented schottky diode as discussed in Chapter 3. The second and the third chip are the hybrid DC-DC converter for the wake-up receiver and the higher power ranges which achieves peak power efficiency of 92% as discussed in Chapter 4. The fourth chip is the Coarsely-Quantized Class-D LDO which achieves fast transient response and is discussed in Chapter 5. The chips are fabricated in CMOS 65nm and 28nm and tested in chip-on-board assemblies. The next sections shows the measurement results for the fabricated chips.

6.1 Measurement Results of Wake-up receiver

In this section, we present the measurement results for the wake-up receiver chip fabicated using 65-nm CMOS technology. The chip occupies an active area of 800μm$\times350\mu$m as shown in Fig. 6.1. The implemented chip consists of the baseband part of the chip which performs amplification, digital correlation, and generating the wake-up signal. The CMOS Schottky diode is part of a separate fabrication and connected by bonding to the chip and the input matching network as shown in Fig. 6.1.

Fig. 6.2 shows the output data matching the previously set preamble sequence. The shift register data setting the preamble sequence of "10011010" along with other control bits are loaded using NI PXIe-1082, then the pulse modulation is set for the frequency generator to use external modulator which uses the data sent through the NI data-acquisition system. The clock starts when the data changes from 0 to V_{DD} and searches for the preamble se-

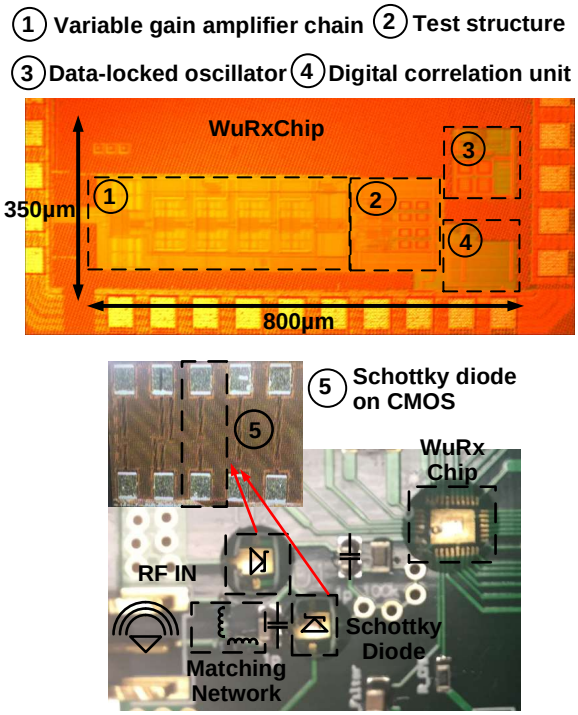

Figure 6.1: WuRx chip and Schottky diode chip Micrographs and PCB for the overall system.

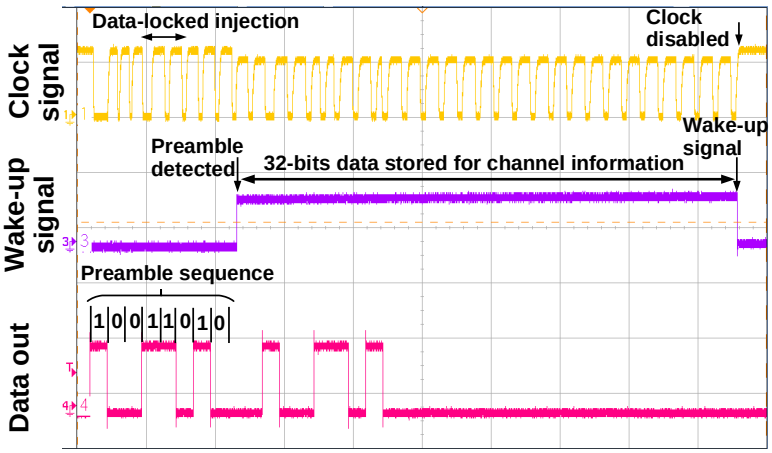

Figure 6.2: Measured wake-up system preamble detection and wake-up signal at P_{IN}=-50dBm and data rate of 200kbps.

quence within 16 clock cycles. The measurement result also shows the data-locked technique correcting the clock phase using data transitions. The wake-up signal is generated after

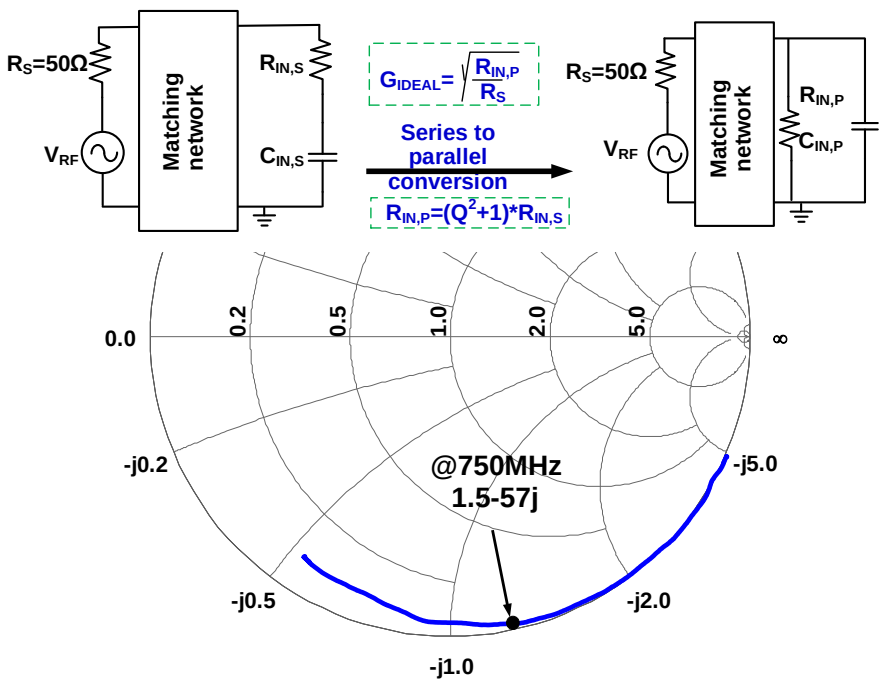

Figure 6.3: Measured input impedance for Schottky diode doubler structure at the operating biasing conditions

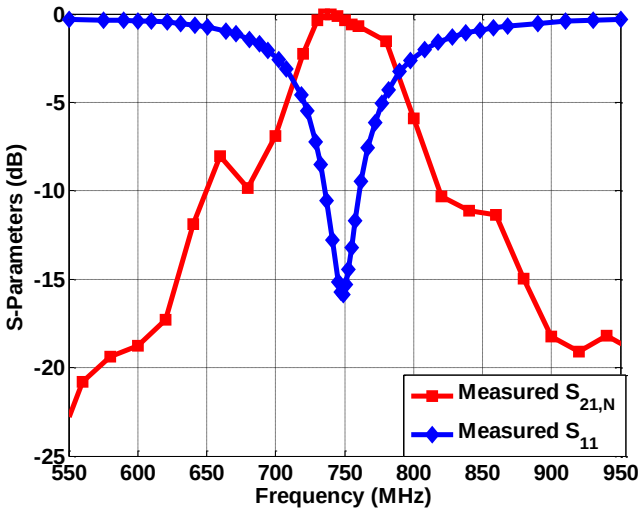

Figure 6.4: S_{11} and $S_{21,N}$ measurement

storing 32-bits of channel information and wakes-up the main receiver then disabling the data-locked oscillator to save power.

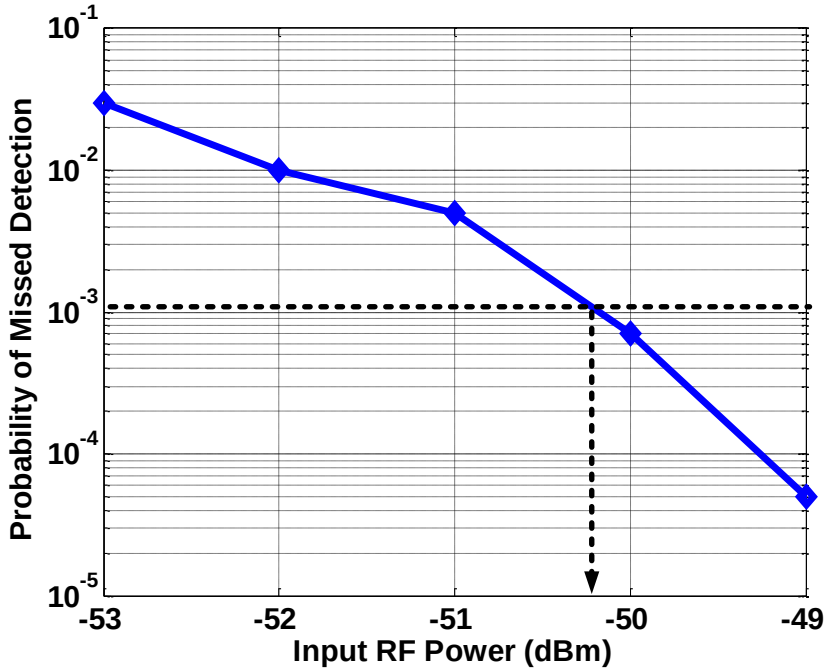

Figure 6.5: Measured missed detection versus input power of the wake-up receiver

The fabricated Schottky diode input impedance is first characterized using Vector Network Analyzer (VNA) HP8720D sweeping from 100MHz-1.8GHz as shown in Fig. 6.3. For the desired frequency of operation, an input impedance of (1.5-57j) is realized that requires effective matching components of L_1=5.3nH and L_2=40nH to compensate for parasitic capacitance associated with PCB pads. The matching network is built on PCB and then to assure 50-ohm matching we measured S-parameters.

Fig. 6.4 shows the measured input matching S_{11} for the detector with the matching network, using (VNA) sweeping from 500MHz-1GHz. The measured normalized S_{21} shows a band-pass behavior for the matching network around the carrier frequency and the bandwidth of matching sufficient for the 200kbps data rate and reduces the integrated in-band noise. The simulated passive gain from used inductors used in the matching network shows roughly 13dB of gain at the carrier frequency.

To verify the system analysis in Chapter 3, measurement results are carried for the probability of detection and the probability of false alarm. The probability of detection

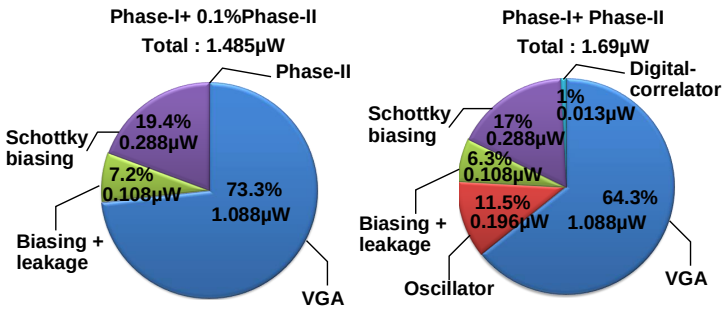

Figure 6.6: Power breakdown of proposed wake-up receiver

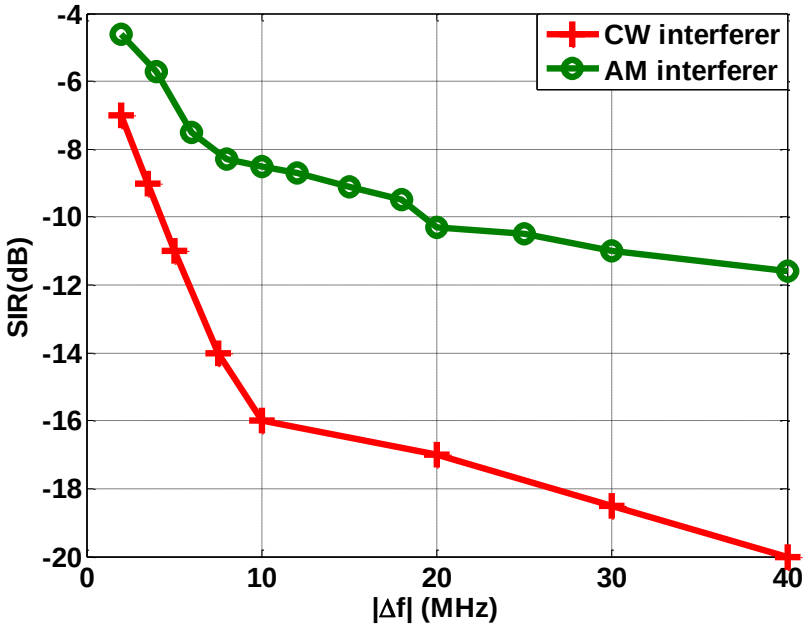

Figure 6.7: Measured signal-to-interferer ratio (SIR) at different offset frequencies from carrier with CW and AM interferer

measurement, shown in Fig. **??**, shows the PD at an input power of -50dBm and -56dBm while varying the threshold voltage as a ratio of the supply. The measurement results match the analysis in Section 3.1.3 as the lower the threshold voltage the higher noise flipping "0" to "1" causing missed detection and vice versa. The measurement shows the optimum threshold voltage at the mid-way of the supply.

We measured the probability of false alarm as it impacts the average power consumed

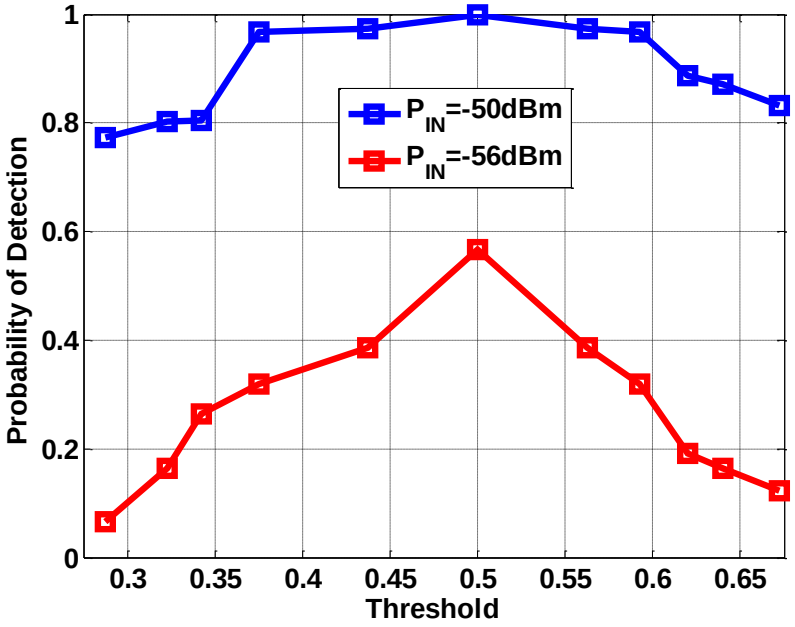

Figure 6.8: Measured Probability of detection at P_{IN}=-50dBm and P_{IN}=-56dBm

in the wake-up receiver. For the measurement setup, we first measured the probability of detection at minimum detectable power and 6dB lower than that. Then we changed the correct sequence with a wrong random pseudo-sequence as the input of the WuRx. In the input sequence, we excluded the correct sequence that's stored on the shift register and inserted the wrong sequence. The probability of detection before inserting the wrong sequence was 0.99 and 0.58 at the optimum threshold voltage. Then, for each threshold voltage, we transmit the wrong sequence with 10^6 packets and counted the signal detected signal. The probability of false alarm is the number of sequences detected divided by the number of packets sent to the WuRx. The measurement results are shown in Fig. **??**shows close results to that reported in the analysis section as in Fig. 3.6. The measured probability of false alarm is $< 10^{-4}$ which assures a small power penalty on the average power of the leaf node.

Fig. 6.6 shows the power breakdown of the proposed architecture when running at 200kbps at P_{IN}=-50dBm. The power consumption of 1.485μA at 0.1% activity rate of Phase-II which is translated into 7.45pJ/bit.The main power portion in the first phase in

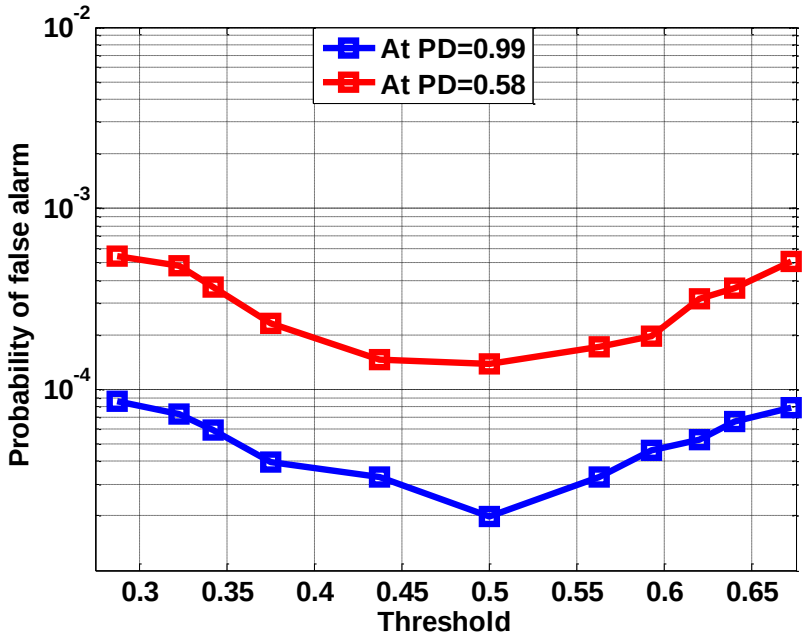

Figure 6.9: Measured Probability of false alarm at PD=0.99 and PD=0.58

the amplifier chain which operates with a 0.4V supply, since the Schottky diode and the matching network consumes no power. The two-phase approach saves 12% of the power by having the second phase disabled till a signature is detected on the communication channel which results in overall better Joule per bit factor. For the second phase, the main power portion consumed of 200nW in the oscillator, while the digital correlator consumes 13.4nW only.

Fig. 6.7 shows the signal to interference ratio (SIR) of -16dB at a 10-MHz offset frequency. The interferer is a continuous wave at different offset frequencies added to the main OOK signal using a combiner. The input power used in the measurement is 6 dB lower than the reported sensitivity. Also, we measure the SIR for an AM modulated interferer with 5% modulation depth. The modulated signal shows more impact on the system compared to the continuous wave. This result shows that the continuous wave act as an offset for the OOK correct sequence at which the proposed system has better resilience. Whereas the AM modulated signal can impact the OOK correct sequence as it changes the energy of "0" and "1" bits sent.

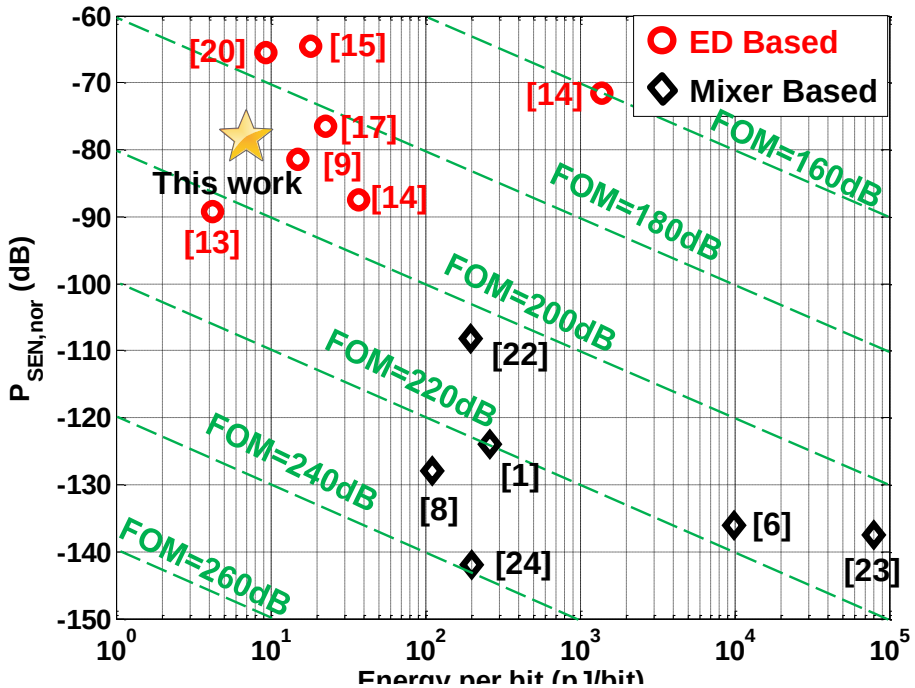

Figure 6.10: Normalized sensitivity versus energy per bit and proposed FOM for WuRx system comparison for prior publications

Fig. 6.8 shows the probability of false alarm at minimum detectable signal (P_{in})and at 6dB lower. The measured results are in good agreement with the analysis for the PFA in Section 3.1.4. The measurement results show PFA below $10^{-}5$ as the analysis requirement showed to lower the overall power consumption.

Table 6.1 compares the performance metrics of the proposed wake-up receiver using the Schottky diode. The energy per bit of the proposed system of 8.45pJ/bit compares favorably with the prior art. The proposed system also has the merit of low latency in wake-up by having a high data rate of 200kbps and 40 bits of correlated data which translates to 200μS. The wake-up receiver working at 750MHz carrier frequency and achieve -50dBm of sensitivity.

Envelop detector based wake-up receivers have different design parameters. In general, the main parameters are the sensitivity of the system, the data rate, the power, and the carrier frequency. Normalized sensitivity proposed in [?] compensated the noise reduction advantage due to using a lower data rate. For the square-law detector, the normalized

sensitivity is given by:

$$P_{SEN,nor}(dB) = P_{SEN} - 5log(BW_{BB}) \tag{6.1}$$

The proposed FOM in [**?**] gives more advantage to lower data rate as it always achieves low power. This can be fixed by taking into consideration the power scaling with the data rate of the WuRx. The power consumption is directly proportional to the data rate after down-conversion. This can be seen through the energy detector biasing current mainly depend on the base-band bandwidth requirement. Also, the amplification stage which is mainly the (gm) of the transistor. Also the correlator and the oscillator power (P=C$f_{osc}V_{DD}^2$ which is directly proportional to the base-band data rate (f_{osc}).

Therefore we propose a figure of merit (FOM_1) that takes into consideration the energy per bit (E/bit) of the wake-up receiver to normalize the power to different data rates. The proposed FOM_1 accommodate the normalized sensitivity and the energy per bit normalized to 1 J/bit and can be expressed as follows:

$$FOM_1 = -P_{SEN,nor} - 10log(\frac{E/bit}{1J/bit}) \tag{6.2}$$

The proposed FOM_1 weights the three main parameters of the wake-up receiver design fairly. The proposed wake-up receiver system achieves FOM_1=187.23dB which compares favorably to prior work as shown in Fig.6.10.

Table 6.1: Comparison of the proposed WuRx with state-of-the-art designs

	TCAS-I20 [26]	JSSC16 [4]	JSSC19 [25]	JSSC18 [11]	CICC12 [21]	TCAS-I17 [17]	**This work**
Technology(nm)	90	65	130	180	130	180	**65**
Supply voltage(V)	1.2	0.5	0.6/1	0.4	1.2/0.5	0.8	**0.4**
Carrier frequency (GHz)	0.771	2.4	0.43	0.113	0.403	2.4	**0.75**
Passive gain (Av) (dB)	12	N/A	27	25	5	N/A	**13**
Data rate(kbps)	2	10	0.2	0.3	12.5	200	**200**
Wake-up latency(μs)	N/A	N/A	82.5	106	2.48	0.2	**0.2**
Sensitivity(dBm)	-46	-97	-76	-69	-45	-50	**-50**
Normalized Sensitivity(dB)*	64.49	-136	87.5	81.4	-65.5	76.5	**76.5**
Power (μW)	0.036	99	0.0074	0.004	0.116	4.5	**1.69**
Energy per bit (pJ/bit)	18	9900	37	15	9.3	22.5	**8.45**

6.2 Measurement Results of PMU Chip

In this section, we present the measurement results of the power management chips fabricated using 28-nm CMOS technology. Fig. 6.11 (a) shows the die photograph of the two blocks. Block-1 and Block-2 occupy an active area of $0.0043mm^2$ and $0.0089mm^2$ respectively. Fig. 6.11 (b) shows the measurement setup in which a Rigol DG1022 is used for line and load measurements and the output voltage is analyzed using an oscilloscope.

Testing is done across all four ranges of operation. Fig. 6.12 shows the output voltage during a transient from no-load current to a current value that ranges from 2μA-180μA in a step of <1μs. Such a condition is more extreme than normal operation since this measurement disables the range switching. The results show no overshoot or undershoot at the output and the output ripples confined to <10mV which is mainly due to the regulation provided through the second stage (ON-OFF LDO). The result shows the expected decrease in the frequency of the output ripple at light load and vice versa. The range switching keeps the output ripple voltage bounded to <10mV for different load conditions.

The system prototype is tested with different reference voltages at the maximum load. Fig. 6.13 (a) and (b) show the line transient response for Block-1 at a load current of 2μA and Block-2 at a load current of 130μA respectively. When the reference voltage steps-low, the

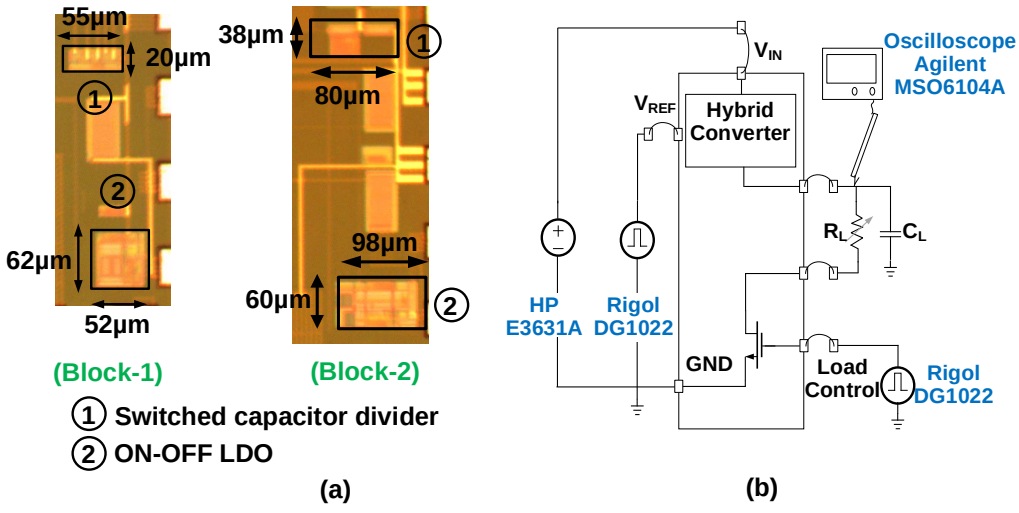

Figure 6.11: (a) Chip Micrograph for Block-1 and Block-2, and (b) test setup

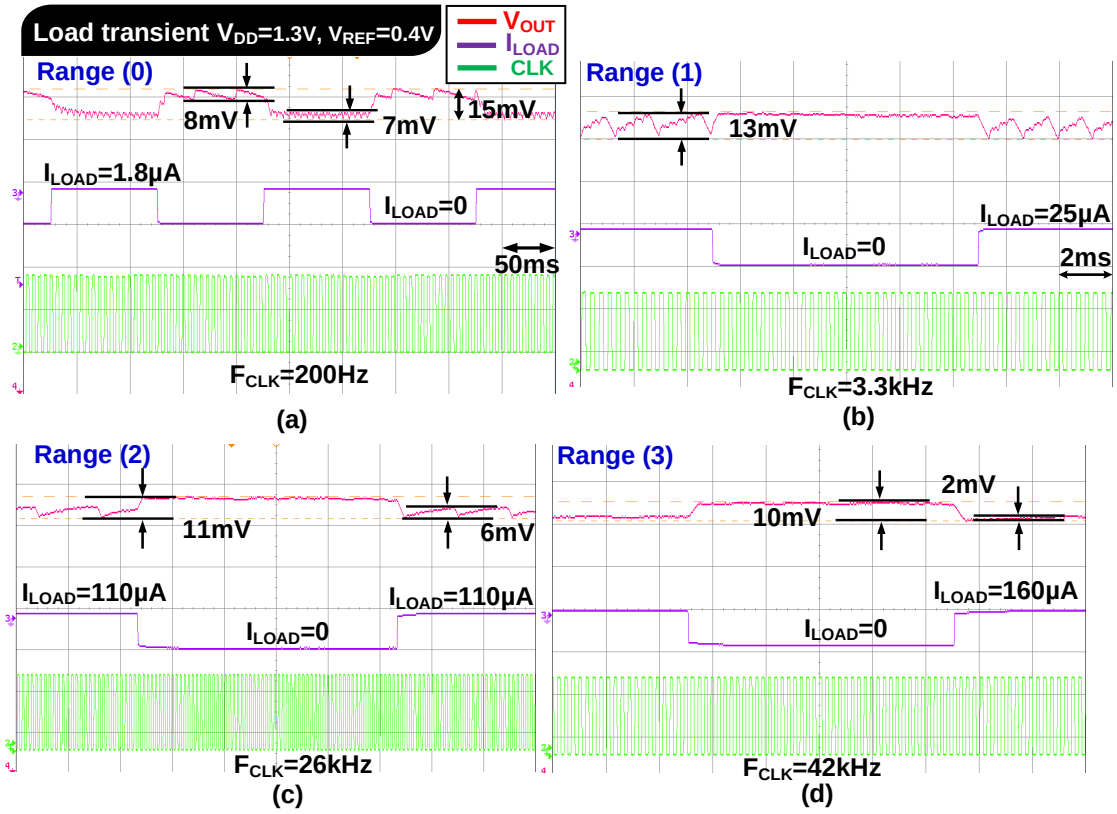

Figure 6.12: Measured load transient from no-load condition to (a) 1.8μA for the sub-microwatt block (Range-0), (b) 25μA for higher ranges block (Range-1), (c) 110μA for higher ranges block (Range-2), and (d) 160μA for higher ranges block (Range-3).

output tracks and settles at the time constant determined at the output node and exhibits with no noticeable overshoot or undershoot as expected in a first-order feedback loop. The voltage ripple is maintained at <8mV in accordance with simulation.

Fig. 6.14 shows the efficiency at each of the four regions of operation. The peak efficiency is as high as 91.8% at the optima load current of 30μA. Each configuration is tested at the designed frequency of operation with the switch size optimized at each of the 4 regions. The overall measured efficiency is >80% at load current ranges from 1μA to 240μA across the four ranges. The quiescent current of the system, at no-load condition, spans the range of 60nA to 800nA for Range-0 to Range-3. The overlap window during configuration changes can introduce an efficiency penalty. Compared to the Pareto optimum, the point of switching

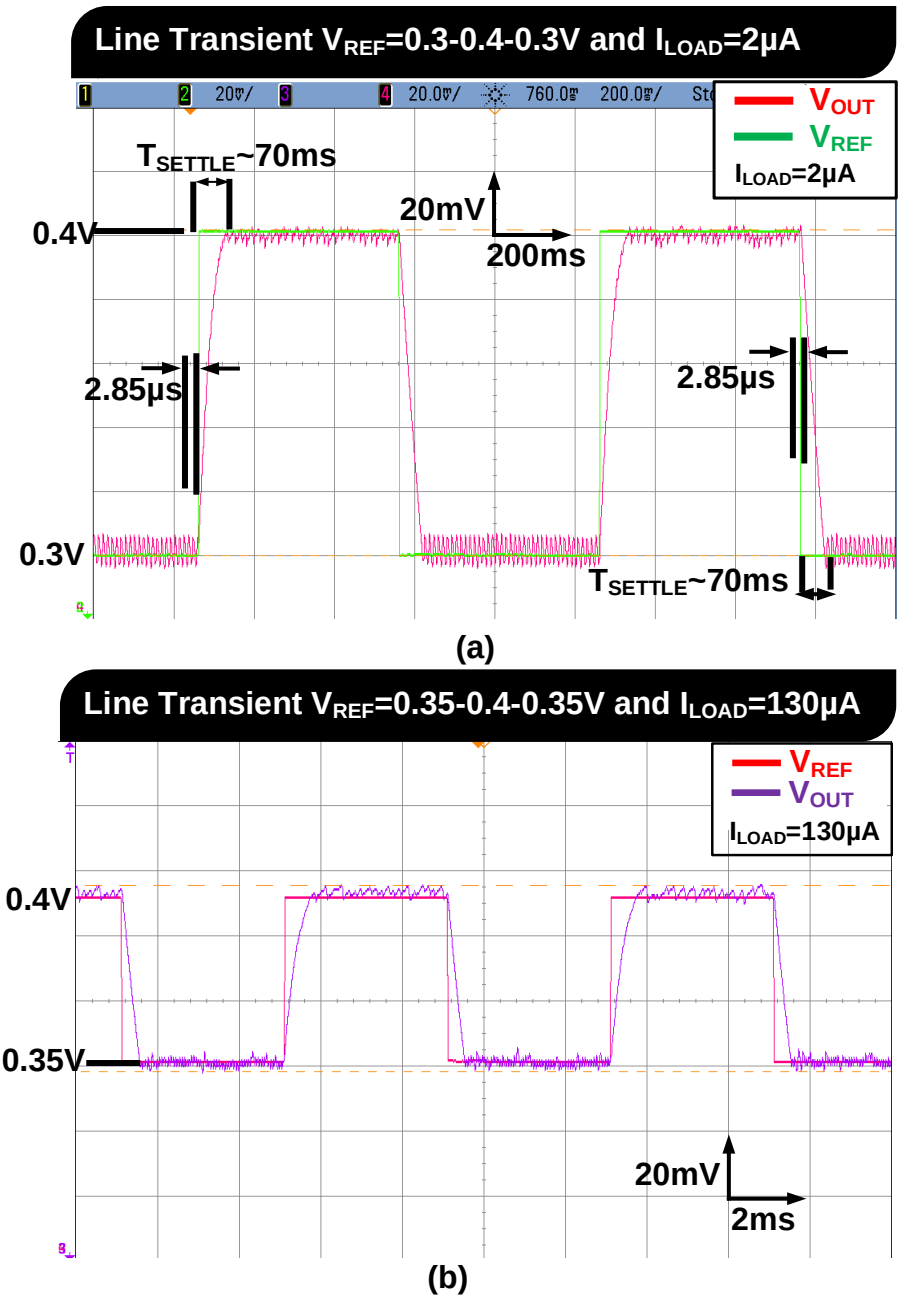

Figure 6.13: (a)Measured line transient for sub-microwatt block-1 when reference voltage change from 0.3V-0.4V, and (b) measured line transient for block-2 at a load current of 130μA and reference voltage change from 0.35-0.4V.

is at a slightly lower load current. Using the windows described in Section 3.2 would result in a modest penalty of only 5%. The reduced efficiency is a small penalty in comparison to the benefits of the extended range.

Table 6.2 compares the proposed power management unit to prior publications showing. The use of large flying capacitors enhances the efficiency of the first stage but the overall efficiency enhancement is due to the combined use of the two-stage hybrid and ON-OFF LDO. This architecture can be designed for different output voltages and with different battery voltages and customized for optimum performance.

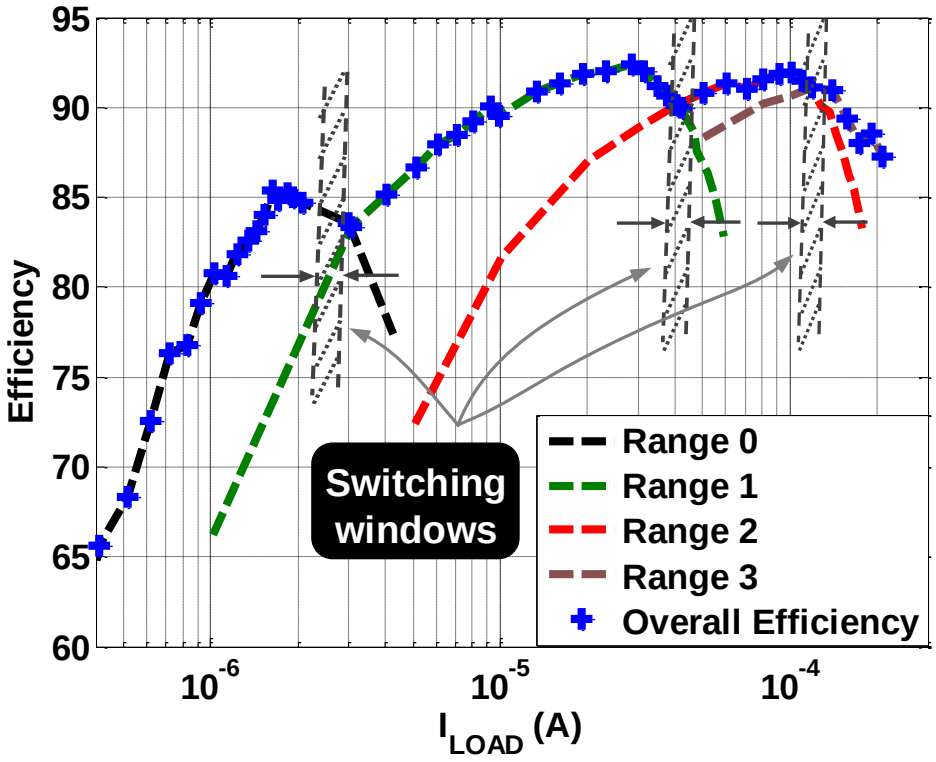

Figure 6.14: Measured overall efficiency across 4 operating ranges.

Table 6.2: Comparison with prior publications

	[36]	[50]	[49]	This work
Process (nm)	130	180	180	28
Input range (V)	2.5-3.6	1.25-2.5	0.9-4	1.15-1.45
Output (V)	0.44	0.3-1.1	0.6,1.2,3.3	0.35-0.45
Load range	2nW-250nW	10μW-100μW	20nW-500μW	20nW-100μW
Clock frequency	2kHz	1.5MHz	50Hz-10MHz	200Hz-50kHz
Output ripples	<50mV	200mV	N/A	<10mV
Total Flying capacitor	800pF	200pF	3nF	300nF
Peak efficiency	56% @I_L=400nA	51% @I_L=62μA	81% @I_L=200μA	92% @I_L=30μA 85% @I_L=1.5μA

6.3 Measurement Results of Class-D LDO

In this section, we present the measurement results of the proposed class-D LOD. The chip micrograph, shown in Fig. 6.15(a), shows the controller, error amplifier, and the FVF output stage occupies a small area of 54μm×77μm and 10μm×280μm, respectively. Fig. 6.15(b) shows the measurement setup for the proposed LDO where the signal generator is used to control the load current changes and the edge time. In the line-transient measurements, a signal generator is used to change the reference voltage at a fast edge time. The output node is probed by a 1GHz sampling oscilloscope. The measured quiescent current of the proposed LDO is 225μA, almost constant at different load conditions, which includes the biasing current, the comparator, the controller, and all timing generation blocks. This quiescent current results in 99.93% current efficiency at 300mA load.

Fig. 6.16 shows the load-transient measurements. The LDO is designed with an external 1-μF capacitor and a load resistor that is switched by on-chip switches. These switches inject sharp current steps with transition times down to 7ns. The R_L switches from open circuit to 3.33Ω which corresponds to 300mA of load current. The measurement shows details of

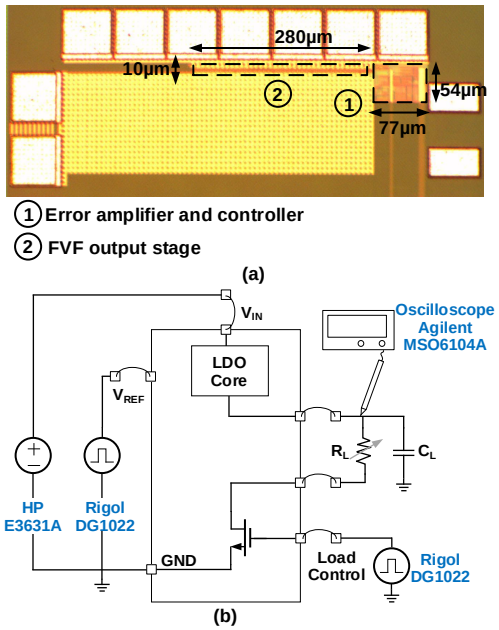

Figure 6.15: (a) Chip micrograph, (b) measurement setup of the proposed Class-D LDO.

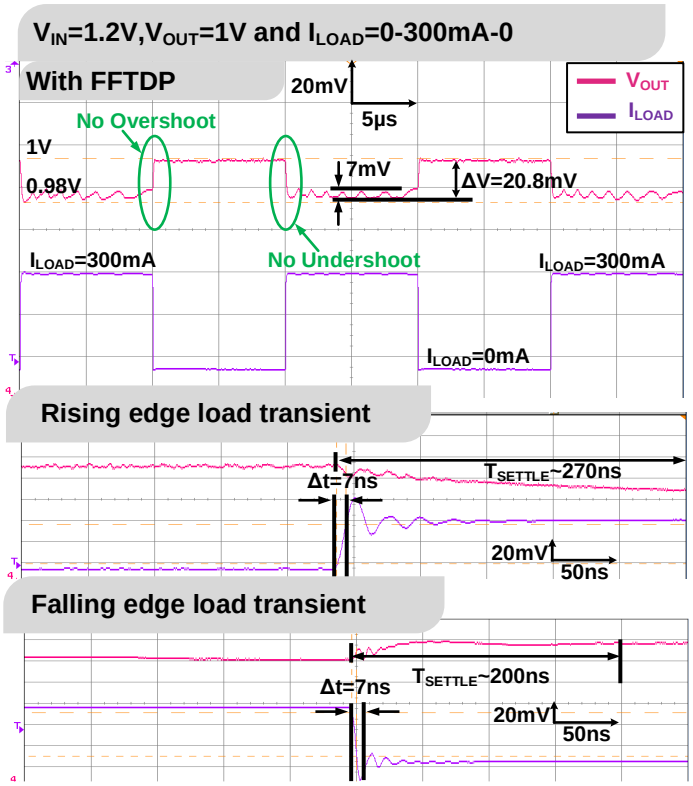

Figure 6.16: Measured load transient at load change from 0-300mA in 7ns at V_{DD}=1.2V and V_{OUT}=1V with FFTDP and zoomed-in rising and falling edges.

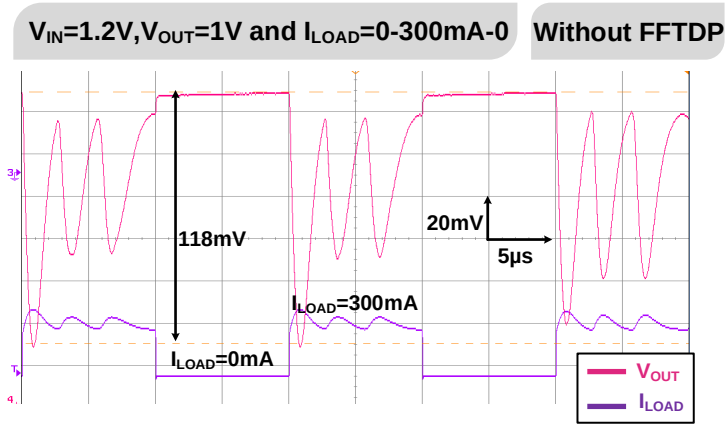

Figure 6.17: Measured load transient at load change from 0-300mA in 7ns at V_{DD}=1.2V and V_{OUT}=1V without FFTDP

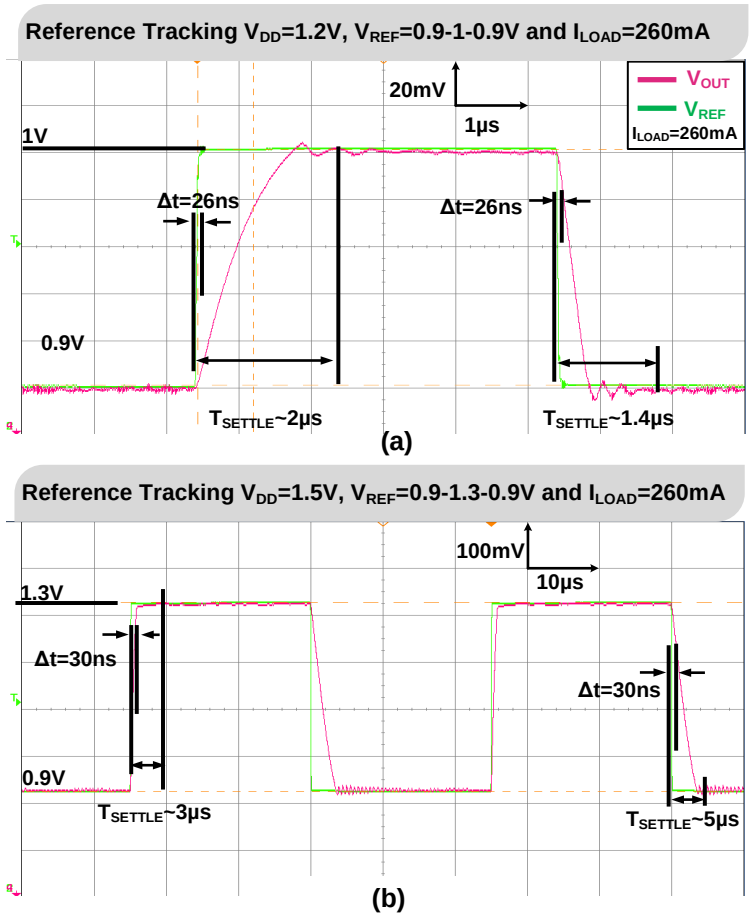

Figure 6.18: (a) Measured line transient at supply voltage of 1.2V and edge time of 26ns, (b) measured line transient at supply voltage of 1.5V and wider reference voltage change 0.9V-1.3V

pulsed load current with a transient slew rate of 300mA/7ns. No overshoot or undershoot is observed. The measurement is shown in Fig. 6.17 show the output voltage when FFTDP is disabled. Incorporating the FFTDP eliminates the overshoot that results from an FVF with low bias current and at the same time improves the ripple from 120mV to less than 7mV.

Fig. 6.18(a) shows line-transient measurements with the reference voltage pulsing from 1V to 0.9V. Similarly, no overshoot or undershoot is observed at a high load of 260mA (equivalent load resistance, R_L=3.85 Ω). The settling time for line transient shows a maximum of 2μs and 1.4μs when transitioning from 0.9-1V and 1-0.9V respectively. As shown in Fig. 6.18(b), large reference voltage steps are measured where the supply is set at 1.5V and the

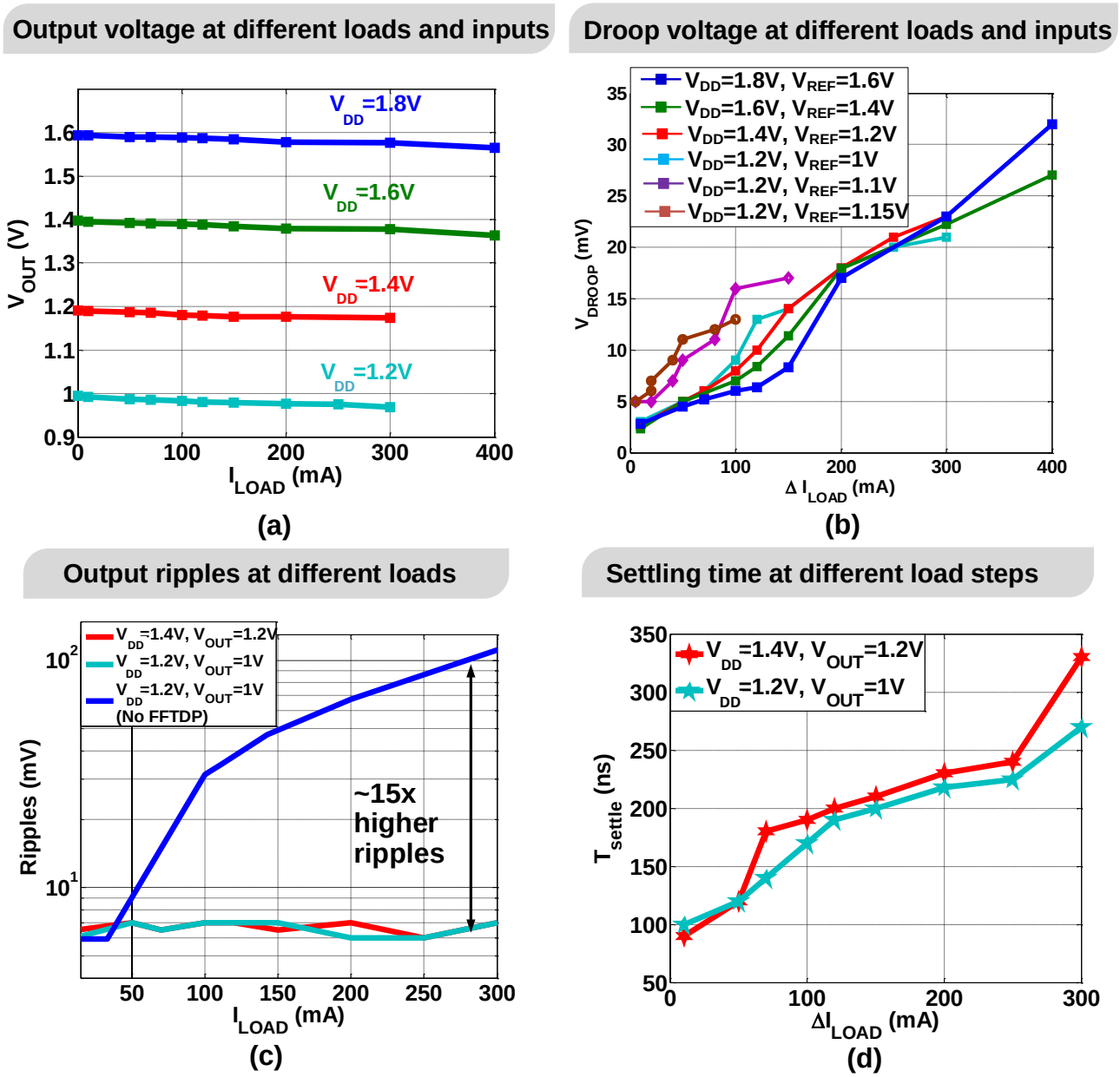

Figure 6.19: (a) Various measured performance of proposed LDO at 200mV of dropout voltage: (a) load regulation, (b) Vdroop, (c) ripple, and (d) settling time.

reference voltage changes from 1.3V-0.9V-1.3V at a load of 260mA with similar performance.

Fig. 6.19 shows a number of performance metrics of the LDO at varying operating voltages and load transients with 200mV of dropout voltage. The load regulation impedance

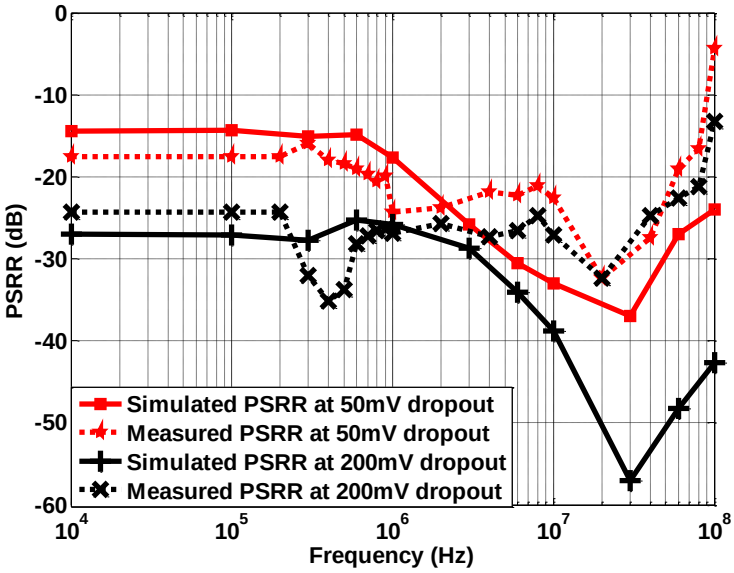

Figure 6.20: Measured and simulated PSRR at 50-mV and 200-mV dropout voltage at 30-mA and 60-mA load respectively.

is maintained at 70μV/mA across the entire range of input and output voltage. The droop voltage at various ΔI_{Load} is primarily due to the static load regulation and ripple. The ripple is relatively constant with various load current and output voltage. The ripple without the FFTDP path also measures and shows 15x lower ripples at 300mA load. The results also show that the settling time is roughly proportional to the size of the load current step. The stability of the LDO is tested across different load resistors with effective current steps of 50mA from 0-400mA and no noticeable overshoot/undershoot is observed. The output voltage response reflects that the dominant pole is at the output node and has a sufficient phase margin.

Fig. 6.20 shows the simulated and measured (PSRR) at two different dropout voltages. The proposed LDO achieves PSRR<-25dB across the frequency range of 10 kHz to 20MHz at a dropout voltage of 200mV with a load current of 60mA. For a small dropout configuration of 50mV, the LDO achieves PSRR<-17dB across the same frequency range.

Table 6.3 compares the results with other prior publications showing substantial improvements in voltage droop at transient load changes. The measured voltage droop is primarily

due to the static load regulation. The proposed LDO achieves lower settling time and FOM_V than comparable designs while maintaining high current efficiency.Where

$$FOM_P = \frac{C_{OUT}\Delta V_{OUT} I_Q}{\Delta I_{max}^2} \tag{6.3}$$

$$FOM_V = \frac{K I_Q \Delta V_{OUT}}{\Delta I_{max}} \tag{6.4}$$

where (K) is edge time relative to 100ps

Table 6.3: Performance summary and comparison with prior art

	TPE17[72]	JSSC17[63]	ISSCC18[68]	ISSCC18[69]	TPE16[71]	This work
Type	ALDO	DLDO	AADLDO	Class-D	ALDO	CQ Class-D
Process (nm)	180	28	65	28	180	28
V_{DD}(V)	1.4-1.8	1.1	0.6-1.2	1.2-1.8	1.2-1.8	1.2-1.8
V_{OUT}(V)	1.2	0.9	0.55-1.05	1.05	1	1-1.6
I_{OUTmax} (mA)	50	200	500	1000	100	400
f_s (MHz)	N/A	N/A	100	120	N/A	83
C_{OUT} (nF)	1000	23.5	0.9	1000	1000	1000
Edge time Δt(ns)	10	4000	20	500	10	7
ΔI_{max} (mA)	50	180	450	999.2	100	300
Overshoot (mV)	0	200	45	40*	0	0
Undershoot (mV)	24	120	125	20*	25	0
ΔV_{OUT} (mV)@ ΔI_{max}	5	N/A	25*	16*	17	20.8
I_Q (μA)	1.6-200	110	500	152	135.1	224
Current efficiency	99.6%	99.94%	99.9%	99.99%	99.86%	99.93%
Load regulation(μV/mA)	100	35	N/A	N/A	75	69
T_{SETTLE} (ns)	1200	≈40000*	1500*	65000*	N/A	280
FOM_P (ps)	18.5	7.75	0.28	6.08	337.5	51.7
FOM_V(mV)	9.6	2933.33	27.7	30.424	3.38	1

6.4 Summary

In this chapter, we discussed the measurement results for the two main contributions of the thesis. First, we demonstrated the performance for the Schottky diode wake-up receiver which achieves 8.45pJ/bit and latency of 200μs of wake-up. The Schottky diode and circuits are fabricated in CMOS 65nm technology. The design shows a robust performance of PFA$<10^{-}5$ which is validated by measurements highlights the importance of the second digital correlator stage in an always-on wake-up system. Second, we demonstrated the performance of the hybrid DC-DC converter with peak power efficiency 92% with adaptive ranges switching with load changes. The hybrid converter chips are fabricated in CMOS 28nm technology. The ranges change extend to wake up of the main radio and the Coarsely-Quantized Class-D LDO. The proposed LDO performance summarized in Table 6.3 shows substantial improvement in settling time after load change and no overshoot or undershoot. The LDO is fabricated in 28 CMOS technology which is widely used in RF applications. In the next chapter, we conclude the contributions of this thesis and propose future directions for the work.

CHAPTER 7

Conclusion and Future Work

IoT leaf nodes are extremely sensitive to energy dissipation as it directly corresponds to their deployment lifetime. Not only do they need means to monitor the environment for an activation signal that uses little current, but they also need to draw little total energy while reacting to activation from an energy source such as a battery or supercapacitor. In this dissertation, we demonstrate both with a wake-up receiver that draws less than 4.2μA of current from a 0.4V source and a power management unit that achieves 85% efficiency at such low currents while achieving a fast transition to higher current load and maintaining the efficiency. We further demonstrate the main radio power management with a novel Class-D LDO which achieves no overshoot or undershoot at fast load changes.

In the first part of the dissertation, we proposed three techniques to improve the energy per bit and the sensitivity of the always-on wake-up receiver. The first technique introduced on the device level uses a CMOS integrated Schottky diode that senses the energy across a bandwidth set by the bandpass filter after the antenna. The Schottky diode is implemented using standard CMOS but is not a part of the technology design-kit. As part of the research, the diode is fabricated and its performance characterized. The characteristics of the CMOS Schottky diode provide high conversion gain at low biasing conditions compared to the normal diode and CMOS diode-connected transistor which improves the overall sensitivity of the system. The second technique introduced on the system level by dividing the wake-up receiver into two-phases, which resembles having a sub-wake-up within the main wake-up receiver. This technique lowers the average power consumption by 12% which elongates the battery life. The third technique introduced on the circuit level by proposing a data-locked startable oscillator as a sampler for digital correlator. The proposed data-locked

oscillator running at the same frequency as the data rate, thus lowering the average power consumption. Also, it starts-up in one clock cycle allowing the system level sub-wake-up for the second phase and oscillates with stable frequency across a wide temperature range. The proposed techniques resulted in energy per bit of 8.45 pJ/bit and sensitivity of -50 dBm with low startup latency of 200μs [28].

In the second part of the dissertation, we address the challenge of power management for the leaf node. This challenge is addressed in two parts. The first is to provide high power efficiency current to the sub-micro-watt wake-up receiver. The second provides a fast transient supply for the high power transceiver of the leaf node. We also proposed a system-level switching between different blocks to achieve maximum power efficiency. For the first challenge, we proposed a hybrid DC-DC converter that provides a high power across wide load ranges. The hybrid converter composed of two stages, where the first stage divides the battery voltage by three and the second stage is the proposed ON-OFF LDO which regulates the output voltage with a dropout voltage of 30mV. The proposed solution provides a regulated output voltage at 0.4V with a power efficiency of 85% for 2μA load [28]. The implementation is further improved to accommodate wide load ranges with efficiency improvement techniques as adaptive switch sizing for the switched capacitor divider according to the load range. This improvement resulted in a wide load range from 0.4μ-400μA with a peak efficiency of 92% [80]. Different switching load windows are incorporated to cover this wide load range which makes it a suitable solution for the low output voltage of 0.4V with high power efficiency.

For the second challenge, we proposed a novel Coarsely-Quantized Class-D LDO [81]. After the wake up of the primary data transceiver, the high load current is drawn from the regulator. Sudden load changes cause large overshoot and undershoot at the output voltage which can cause problems for the powered circuits. Also, the settling time for the supply is another important factor for the regulator design. We achieved a fast settling time of 280ns for 300mA load change through the following three key contributions. First, we use MLPWM signal to control the output voltage which allowed faster internal loop speed. Second, we use FVF as an output stage which provided low output impedance compared to a normal

PMOS output stage along with a smaller capacitor value on the control path. Third, we introduce an FFTDP which detects any sudden load changes and act as an adaptive bias for the output stage. Through these techniques and the circuits described in Chapter 5, we improve the response time and achieved no overshoot or undershoot for fast load change.

Since this work demonstrated the effectiveness of a Schottky diode that is available on any standard CMOS technology as an energy detector, such a diode can be useful in other systems. The integrated diode can be matched for different input filters for better integration. The system used for the thesis can be applied to any center frequency. The wake-up receiver can also be implemented using multiple voltage doublers at low data rates <1kbps targeting better sensitivity and lower quiescent current than current implementations.

In addition, the current results we have obtained from the Schottky diode show promising performance for the use of these diodes in RF energy harvesting. The voltage doubler structure at no biasing will provide high voltage gain with maximum conversion gain from the matching network. Also, the I-V characteristics proved to be a good candidate as it has near-zero voltage for turning on with negligible reverse current. The power management system can then be extended for energy harvesting using the same architecture of the switched-capacitor charge pump along with the battery. The Schottky diode can provide a path for RF energy harvesting in parallel with different sources as a thermoelectric generator (TEG) and piezoelectric. This can potentially result in a fully integrated solution that improves life for the leaf node beyond the capacity of the battery. Lastly, for a fast transient response during wakeup of the primary data transceiver, the use of an integrated capacitor can be investigated along with the use of an auxiliary analog loop as a dual loop for improved loop dynamics.

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