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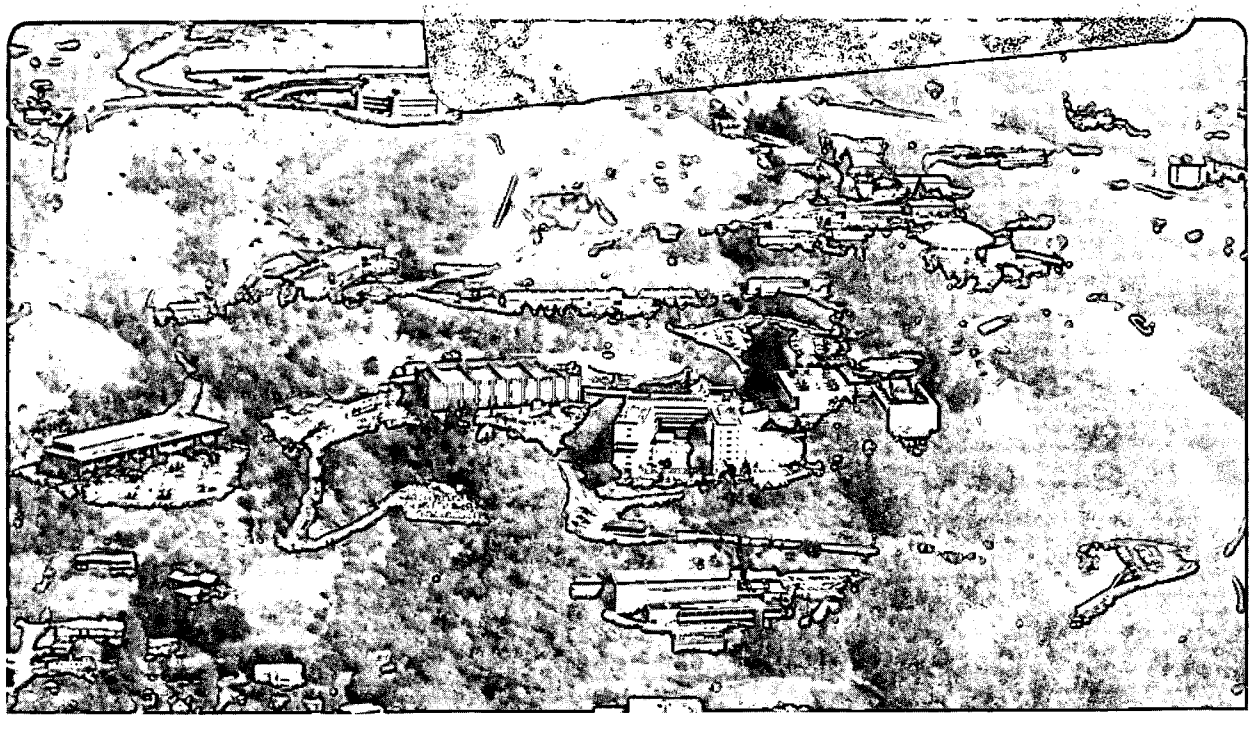

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HIGH-RATE CAMAC ACQUISITION SYSTEM

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High-Rate Camac Acquisition System[1]

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Abstract

The High Energy Resolution Ball (HERB) consists of 21 bismuth-germanate shielded germanium detectors, clustered in three rings. In the center of the cluster is a 40 element bismuth-germanate ball which functions as a sum spectrometer and a multiplicity filter. The purpose of the system is to measure the energy, multiplicity, and correlations of gamma rays emitted from a target located in the center of the ball.

This paper describes the data acquisition hardware and software which was developed to support this apparatus. The high data rates generated are handled by two levels of FIFO buffering in CAMAC hardware. Also of interest is the method of calibrating the individual analog input channels. The software obtains calibration information from the incoming experimental data and sets up a special CAMAC module which dynamically adjusts the gain and offset of each input channel.

1 Introduction

The data acquisition system for the germanium array depends on external coincidence hardware to generate a trigger when an event is to be digitized. This trigger causes four (or more) analog multiplexers (8 channels each) to sample their input channels and begin a conversion cycle in an associated ADC. The multiplexer/ADC units operate asynchronously and in parallel, with a threshold detector on each channel to determine which of the 8 channels will be digitized. Associated with each multiplexer is a CAMAC module which contains a FIFO memory large enough to hold the digitized values from all 8 channels. As each channel is digitized, which takes from 5 to 15 μs depending on the pulse height, the 13-bit value and a 3-bit channel number is stored in the FIFO memory. When all multiplexers have finished, the FIFO memories and any other modules which contain data associated with the event are read into a 2 K word FIFO memory in the CAMAC crate controller. For a typical event, which has only one or two channels above threshold in each multiplexer, the total cycle time is about 25 μs. The crate controller contains two independent FIFO memories, so the acquisition cycle never has to wait while the host computer reads the data.

In some experiments, data from two-parameter coincidence events are routed directly to a large (4 megaword) histogramming memory, and only triple or higher coincidence events are routed to the host computer for storage on tape. This mode of operation greatly reduces the number of data tapes used.

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The instrumentation was designed to satisfy several criteria, mainly: high data rates with minimum dead time, CAMAC compatibility, flexibility, and expandability. High data rates must be handled because each of the 21 germanium detectors can produce up to 10K analog pulses per second. CAMAC compatibility was chosen to provide computer independence, to use readily available standard components, and to easily fit into an existing system. Flexibility and expandability are needed because of the number of detectors and different types of input data to be handled, such as time to digital converters (TDC), scalers, analog to digital converters (ADC), event identifiers, and multiplicity data.

The primary function of the data acquisition software package (CDAS) is to transfer the stream of event data from the CAMAC hardware to a magnetic tape. Direct Memory Access (DMA) channels are used for both the CAMAC input and the tape output, leaving over 90 percent of the processor time available for on-line histogramming and displays.

2 Hardware

2.1 Design Considerations and Compromises

Because of the high data rates produced by the detectors, a fast ADC was required. While an ADC for each of the 21 detectors would have been ideal, the cost was prohibitive, and a major compromise was necessary: the use of an analog multiplexer (MUX) which allows each ADC to service eight input channels. We chose the Silena model 7420/S, a 13 bit, 400 MHz Wilkinson ADC. An important feature of this ADC is that it has dynamic inputs for zero offset and gain correction, permitting separate calibration of each input channel.

The hardware for this system was designed to meet the requirements of a variety of different input devices, and to maintain correlation between the various parameters which are produced by each event. A signal standard had to be established, and a chassis with many input connectors was required. The design and fabrication costs for this sort of data gathering chassis can be substantial. The CAMAC crate and bus standard was chosen because it fulfills all of the above criteria.

2.2 Configuration (fig 1)

The configuration chosen for this system consists of two NIM crates, and two CAMAC crates. The ADC modules, Multiplexer modules, and the Master Gate controller are contained in the NIM crates, everything else is in the CAMAC crates.

The ADC to CAMAC interface modules and the event crate Controller/Formatter are contained in the "fast" (event) crate. This is a standard CAMAC crate which is cycled

at twice the normal speed by the Controller/Formatter. All CAMAC modules which handle event data are in this crate.

The "slow" CAMAC crate contains a standard A2 controller, a single 16-bit input module which reads the event data stream from the Controller/Formatter in the event crate, the ADC gain/offset correction modules, and any other modules which do not handle event data. This is a standard CAMAC crate, operating at the normal rate of one microsecond per cycle. The unit which connects the A2 controller to the host computer is a Differential Branch Driver (DBD) designed at the Los Alamos Laboratory for the Modcomp computer[1]. The maximum data rate of the DBD is 3 μs per 16-bit word.

2.3 Master Gate Controller 71X253B (fig 2)

In order to maintain event correlation, that is, to keep all of the parameters of a particular event together, a traffic director is needed. When an event is sensed by the external coincidence detector, an event trigger is sent to the Master Gate Controller. This unit makes checks to guarantee that the previous event has been completed, then issues a master gate to each MUX/ADC unit to permit digitization. When all of the multiplexers become idle, it initiates a crate scan pulse to the Controller/Formatter unit in the event crate. Event triggers which arrive while the controller is busy are ignored.

When two-parameter events are to be routed to the histogramming memory, the external coincidence detector also generates the "2D EVENT" trigger. This causes the crate scan pulse to be sent to the 2D controller instead of the Controller/Formatter.

2.4 Analog Multiplexer 21X740, 21X741 (fig 3)

This unit was designed at LBL to work with the Silena ADC. It consists of two modules, an analog stretcher and a digital control unit, each of which is two NIM slots in width. The analog module has eight analog inputs, eight independent veto inputs, and one master veto input to reject the whole event. The veto inputs are enabled only during the master gate time. Each analog channel has independent upper and lower level discriminators; parameters with values outside the discriminator levels are skipped. The 16-bit digital output from the multiplexer consists of a header word which identifies the multiplexer, an optional pattern word designating which channels have been digitized, and one to eight parameter values. Each parameter value consists of a three-bit channel designator (tag) and a 13-bit digitized value.

2.5 ADC to CAMAC Interface 71X234 (fig 4)

This module provides a data path between the multiplexer and the CAMAC dataway, using a 16-word FIFO memory to collect the multiplexer output. The FIFO allows the

MUX to transmit each value as soon as possible after it has been digitized (there is often more than one parameter to be digitized by each MUX), thus minimizing dead time. It obeys the CAMAC standards (F2, C, Z, Q, X, and L) and accepts the 0.5 μs cycle length of the fast crate. The module asserts its LAM (Look At Me) whenever it contains any data, and it is read by repeated access of subaddress zero.

2.6 Event Crate Controller/Formatter 71X235 (fig 5)

This two-slot module is the heart of the event correlated data collector. It contains two FIFO memories (2048 words by 16 bits) and the control logic for filling one of these memories while data is being read from the other. The output of this module connects to a 16 bit CAMAC input module which resides in the "slow" crate.

When the Controller/Formatter receives a crate scan pulse from the Master Gate Controller, it examines the LAM lines of each slot sequentially. Each slot with LAM asserted will initiate a 0.5 μs F2 read cycle. Slots that are empty or are not asserting their LAM will be bypassed. Slots with more than one word to be read must maintain their LAM signal until emptied. Initially, the incoming data is stored in the "A" FIFO. When this FIFO is full, data is vectored to FIFO "B". Simultaneously, FIFO "A" sends a demand flag to the A2 controller in the "slow" CAMAC crate. This in turn causes the branch driver to initiate DMA reads to the CAMAC input module using the Q-stop mode.

The effect of this unit is to allow bursts of event data to be read from the multiplexers at a 2 MHz rate, while the branch driver is transmitting data to the host computer at a 250 KHz rate.

2.7 Silena ADC Gain and Offset Control 71X251 (fig 6)

This module has an 8-word by 16-bit holding register at addresses A0 to A7. The most significant 8 bits contain the gain corrector value for each associated parameter, and the least significant 8 bits contain the offset corrector value. This non-clocked device uses the 3-bit parameter number from the multiplexer to determine which word in the holding register is presented to two 8-bit digital to analog converters (DAC). The outputs of the DACs (zero to 10 V) are cabled to the gain and offset correction inputs of the Silena ADC.

Since the MUX is a zero-skipped device, the three-bit parameter numbers seen by this module are in random order. The internal timing of the MUX delays the analog signal presented to the ADC by 1.5 μs. to allow for the settling time of DAC outputs from this module.

2.8 Event Separator 71X252

This module produces the 16-bit event separator word needed by the data analysis software. It has a LAM input which is triggered by the "set event separator" output of the Master Gate controller. The value of the event separator word (normally hex FFFF) is set by 16 front panel switches.

2.9 2D Address Controller 71X258

This module, when triggered, scans the LAM lines of slots 16-19 sequentially, in the same manner as the Controller/Formatter. Two 16-bit words are read, and selected bits from each of these values are used to form a 24-bit address which is transmitted to the histogramming memory.

2.10 Histogramming Memory

This unit is a Dataram model DR229S memory with slots for up to 16 megawords of 16-bit error correcting solid state memory. An adder unit accepts a 24-bit address from the 2D address controller and adds one to the designated memory word. A DMA controller unit allows the host computer to transfer data to and from the memory without interfering with the operation of the adder unit.

3 SOFTWARE (fig 7)

The CAMAC Data Acquisition System (CDAS)[2] software package handles CAMAC setup, tape assignment, writing data on tape, histogramming of incoming events, calibration, and on-line displays. The package consists of five tasks, which communicate with each other through shared memory areas. These programs are all written in Fortran. Input of data from the branch driver is done through a DMA channel, using a modified version of the I/O handler written for the DBD at Los Alamos[3].

3.1 CDAT- Data Acquisition Task

This task controls the overall operation of the system, sets up the CAMAC acquisition, activates the other tasks, watches for abnormal situations, and handles most user commands.

3.2 CDRT- Data Recording Task

This task records the incoming data stream on tape. It is controlled by communication flags which are managed by CDAT and the interrupt level DMA I/O handler. CDRT is activated whenever a data buffer is ready to be written to tape. If data is being acquired faster than it can be written to tape, the I/O handler suspends input, and CDRT restarts input when buffer space becomes available. Data buffer size is variable, from 100 to 5000 words. In all experiments to date, we have used three data buffers of 5000 words each.

3.3 CSORT- On-Line Sorting Task

This task is used to build histograms in memory from the incoming data. CSORT is very similar to the off-line sorting task, EVA. The user must create a program, in the EVAL[4] language, which defines the spectra to be generated and the sorting algorithm to be used. Because EVAL is a relatively high-level language, these programs are easy to understand, and the changes from one experiment to the next are not difficult. Buffers are passed to CSORT after they have been written to tape by the recording task and sorting is done at a lower priority than data recording. When the acquisition rate is faster than the sorting routine can handle, buffers are relinquished back to the acquisition task before they have been completely sorted.

3.4 CCAL- Calibration Task

The purpose of this task is to monitor and adjust the calibration of the analog digitization system. Each channel of each multiplexer is separately calibrated by loading the proper values into the holding registers of the gain and offset control modules.

The steps of the calibration procedure are:

1. Set all the registers of the gain and offset control modules to mid scale.
2. Collect data from a source which emits gamma rays of known energy and build a histogram (using CSORT) for each channel to be calibrated.
3. CCAL then reads a previously prepared file, called the calibration control file, which specifies the energy of two peaks in the spectrum and the desired energy per channel and offset. The program first finds the two peaks, then makes a calculation which determines the gain and offset error in each channel, and a table showing the magnitude of the errors in each channel is printed. This table also shows the value which would be required in the gain and offset registers to correct the errors.
4. Using this table, the gain of the amplifier in each analog channel is manually adjusted to reduce the error, and we return to step 2.

5. When the errors have been reduced to values which are within the range of the gain and offset control module (approximately 2 percent of full scale), the program is instructed to load the corrector values into the control module. Again we return to step 2 to check for the remaining errors. One or two iterations are usually sufficient to reduce all errors to less than 1 channel in 4000.

6. When the input of real experimental data begins, we look at the spectrum produced by each detector and identify two peaks of known energy. A new calibration control file is prepared which contains this information. Using these peaks, we monitor the stability of each detector and correct calibration errors during the course of the experiment by periodically restarting this sequence at step 2. The normal drift in detector gain and offset is within the range of the control module, so further manual adjustments (step 4) are not required.

3.5 CLOOK- On-line Display Task.

This task generates an on-line display of the spectra created by the CSORT task. The user may look at any spectrum or group of spectra and may expand the display to show any range of channels desired. A pair of movable vertical cursors are maintained, and a continuous readout of the area and centroid between the cursors is presented.

CLOOK runs at the lowest priority of any in the CDAS package, thus using only the CPU time which is not needed by the acquisition or sorting tasks. All control is done from the Tektronix 4014 keyboard.

4 Conclusions

This system has performed well for several experiments. The on-line calibration serves as a check on the operation of each detector during data collection and has nearly eliminated the need to do calibration during off-line analysis. Typical data rates are from 10 K to 35 K words per second written on tape.

Maximum performance tests have been made using a 2.5 V analog pulse into one channel of each multiplexer. Measured dead time was 15 μs, which is equivalent to a burst rate of 66 K events/second. The total sustained throughput rate was 250 K words per second onto 6250 bpi tape, corresponding to 35.7 K three-parameter events per second.

5 Acknowledgment

We wish to thank M. A. Deleplanque, R. M. Diamond, and F. S. Stephens for their help in the specifying and testing this system, R. L. Rozzano who designed the controller

for the histogramming memory, and F. Gin and J. D. Meng who designed the analog multiplexor.

Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U. S. Department of Energy to the exclusion of others that may be suitable.

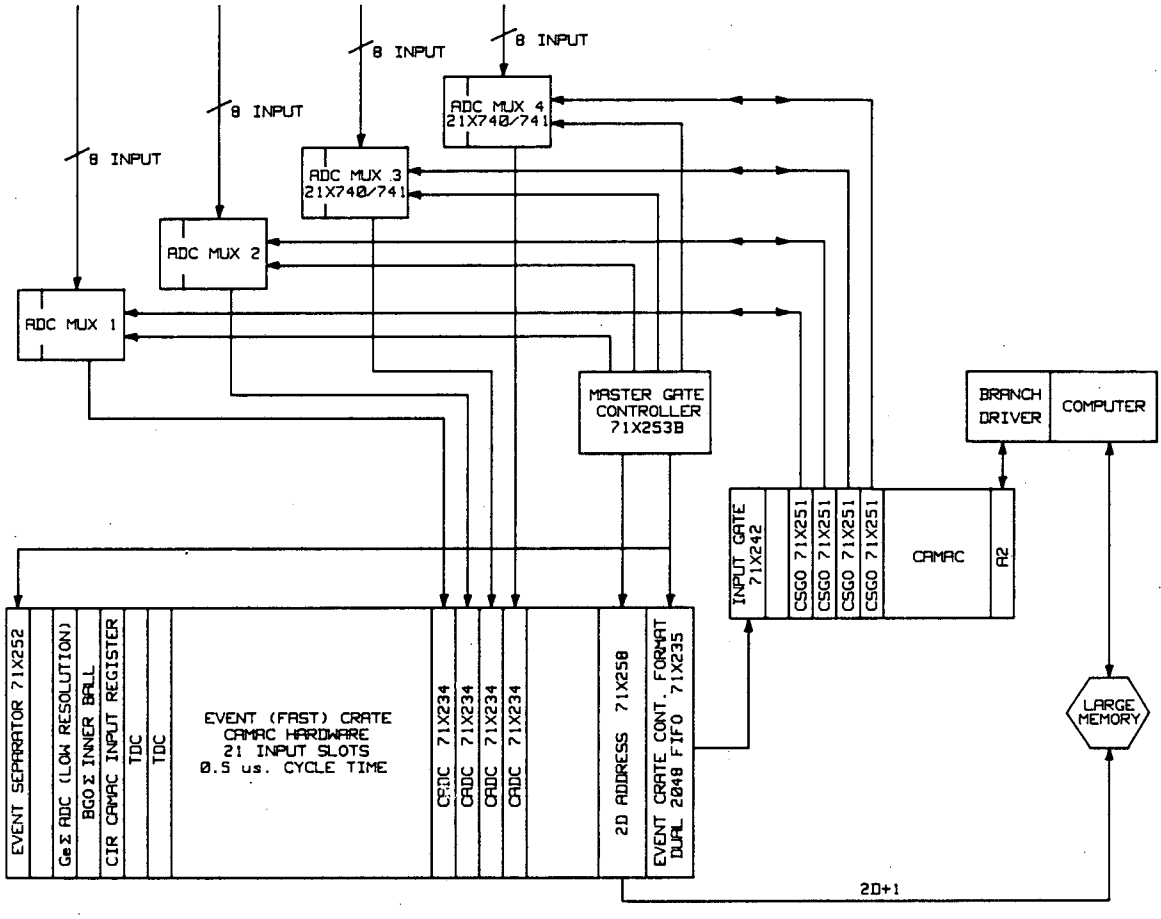
References

[1] D. E. McMillan et al., IEEE Trans. Nucl. Sci. NS-26 (1979) 4450.

[2] R. A. Belshe, Camac Data Acquisition System, Lawrence Berkeley Laboratory (1986).

[3] R. V. Poore and J. W. Sunier, Modcomp Data Acquisition Documentation, Los Alamos Scientific Laboratory (1977).

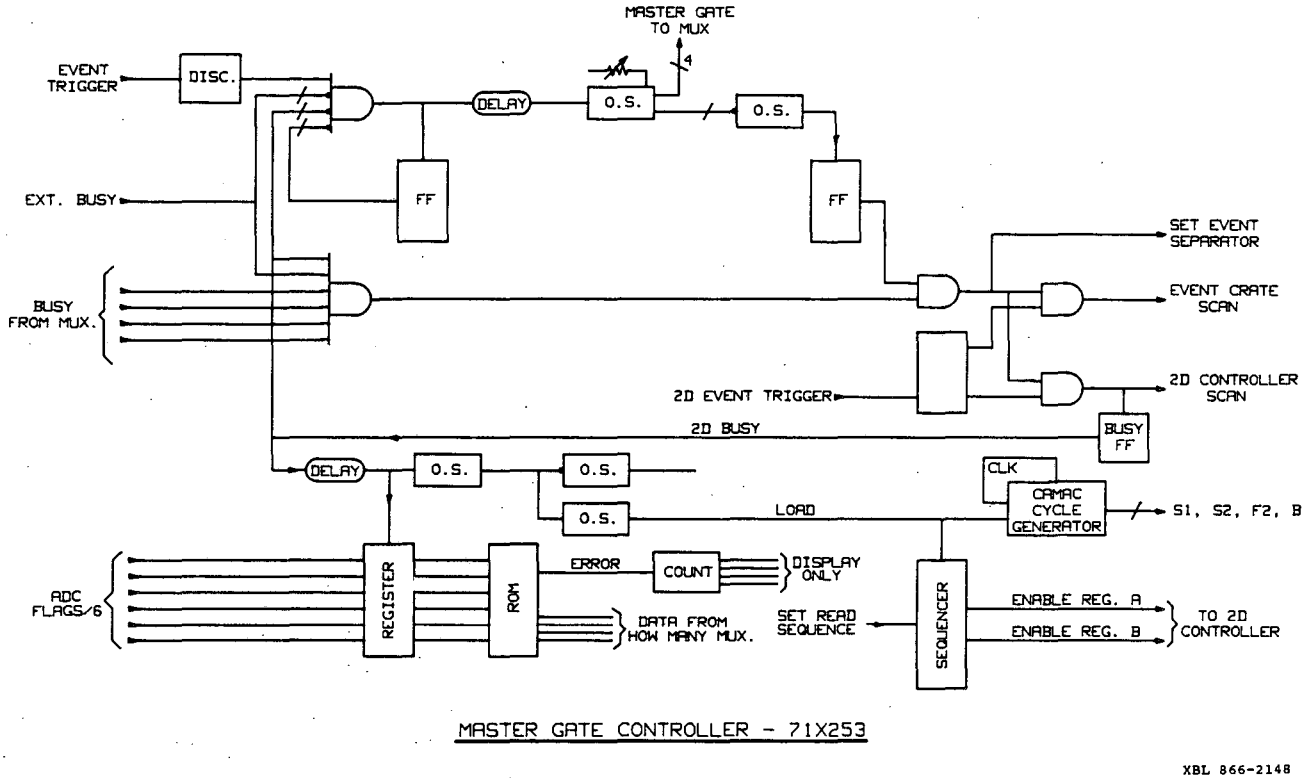
[4] R. A. Belshe, EVA Reference Manual, Lawrence Berkeley Laboratory (1985).



SYSTEM BLOCK DIAGRAM

XBL 866-2149

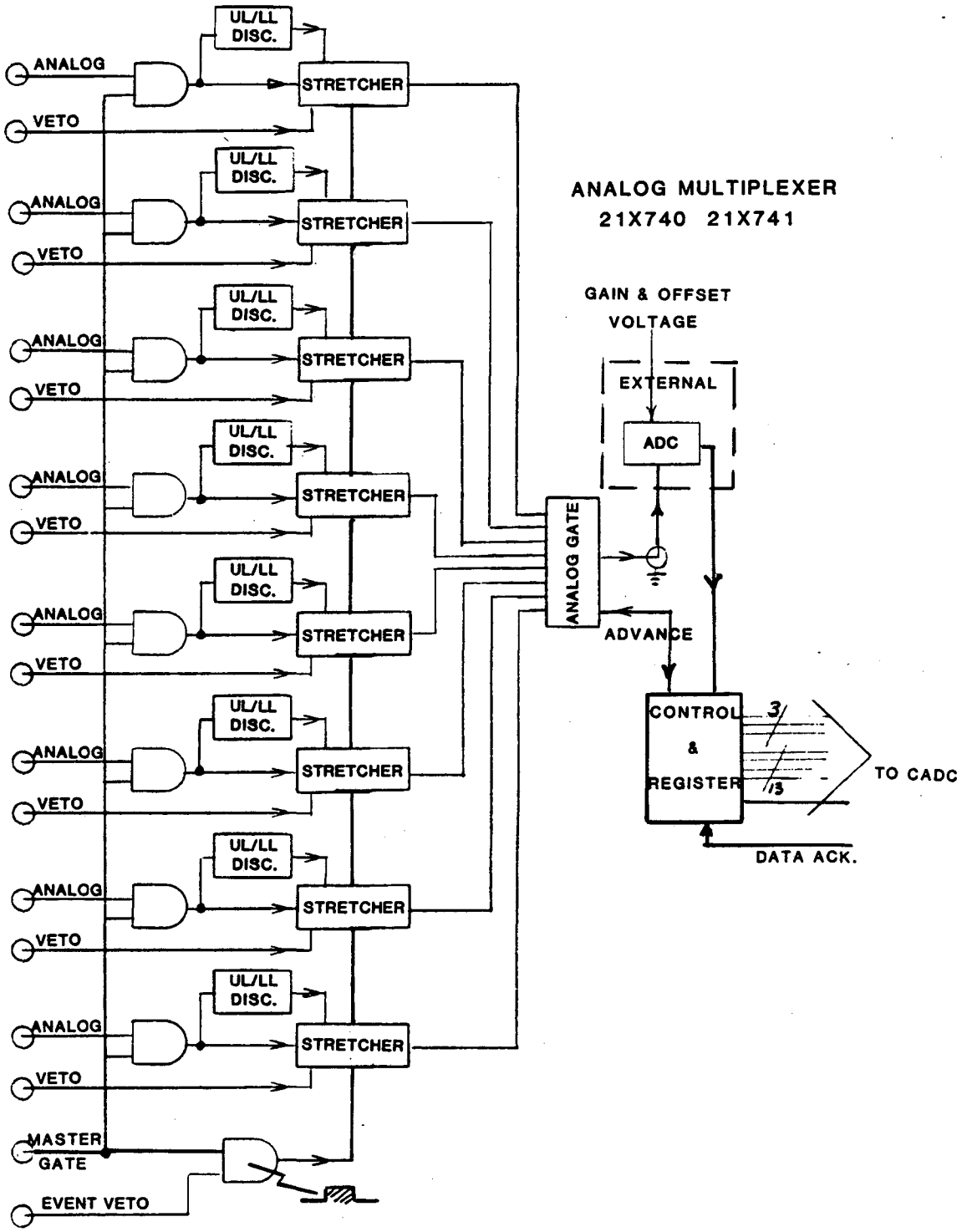
Fig. 1 System Block Diagram



MASTER GATE CONTROLLER - 71X253

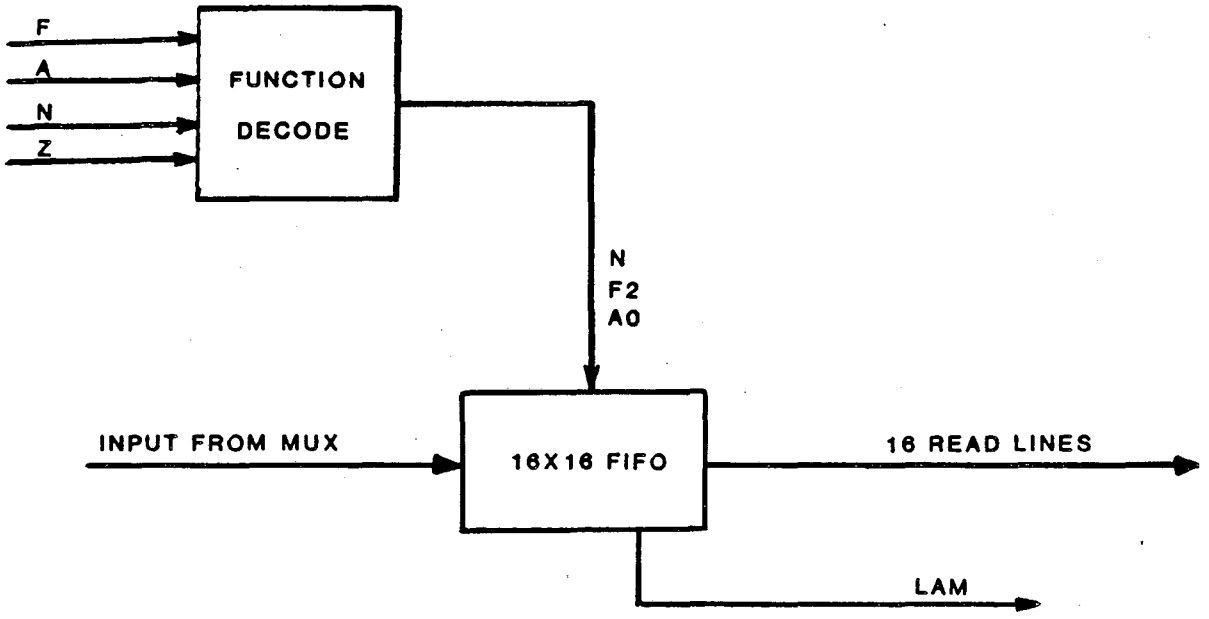
XBL 866-2148

Fig. 2 Master Gate Controller Module



XBL 864-1674

Fig. 3 Analog Multiplexer Module



CADC 71X234

XBL 865-1866

Fig. 4 ADC to CAMAC Interface Module

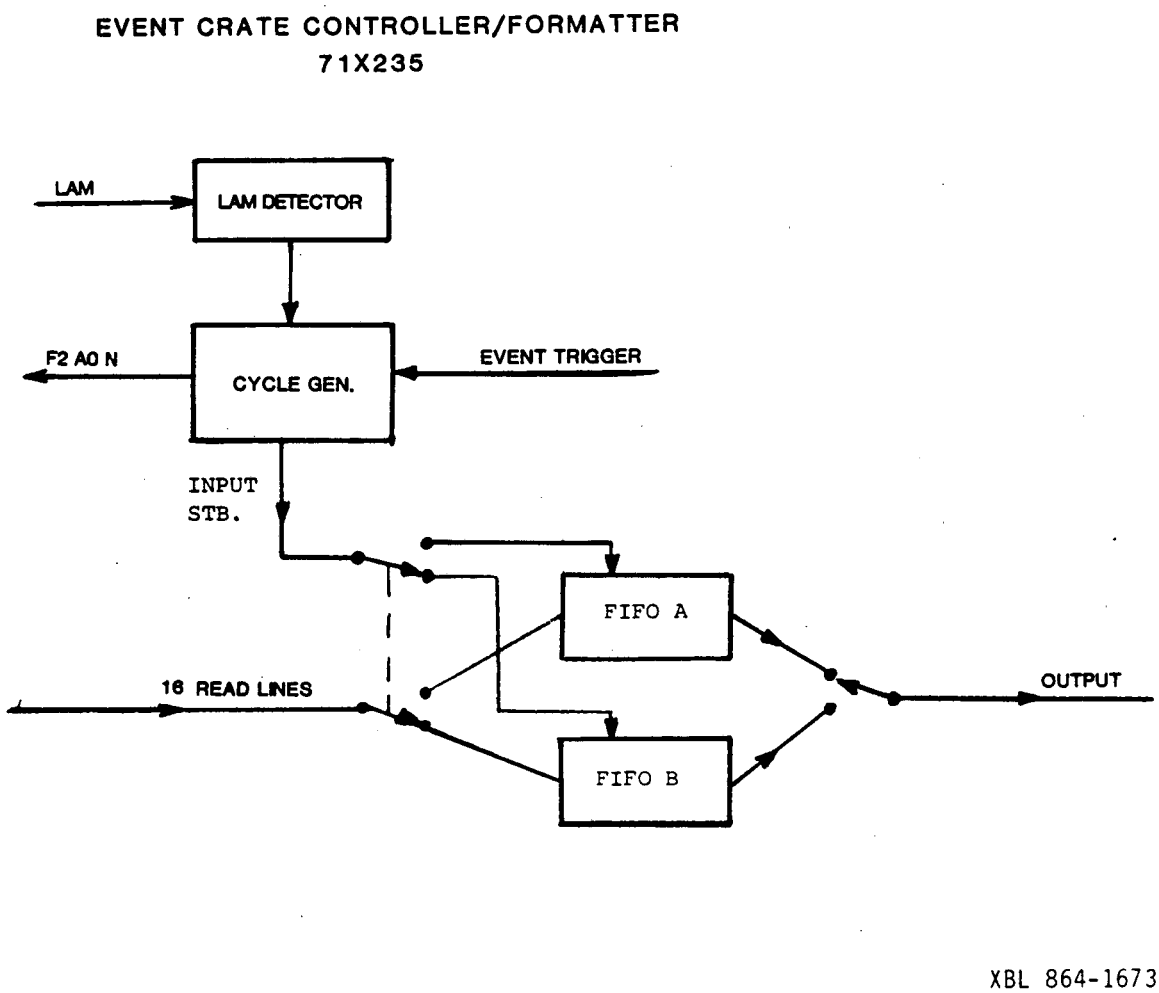


Fig. 5 Event Crate Controller/Formatter Module

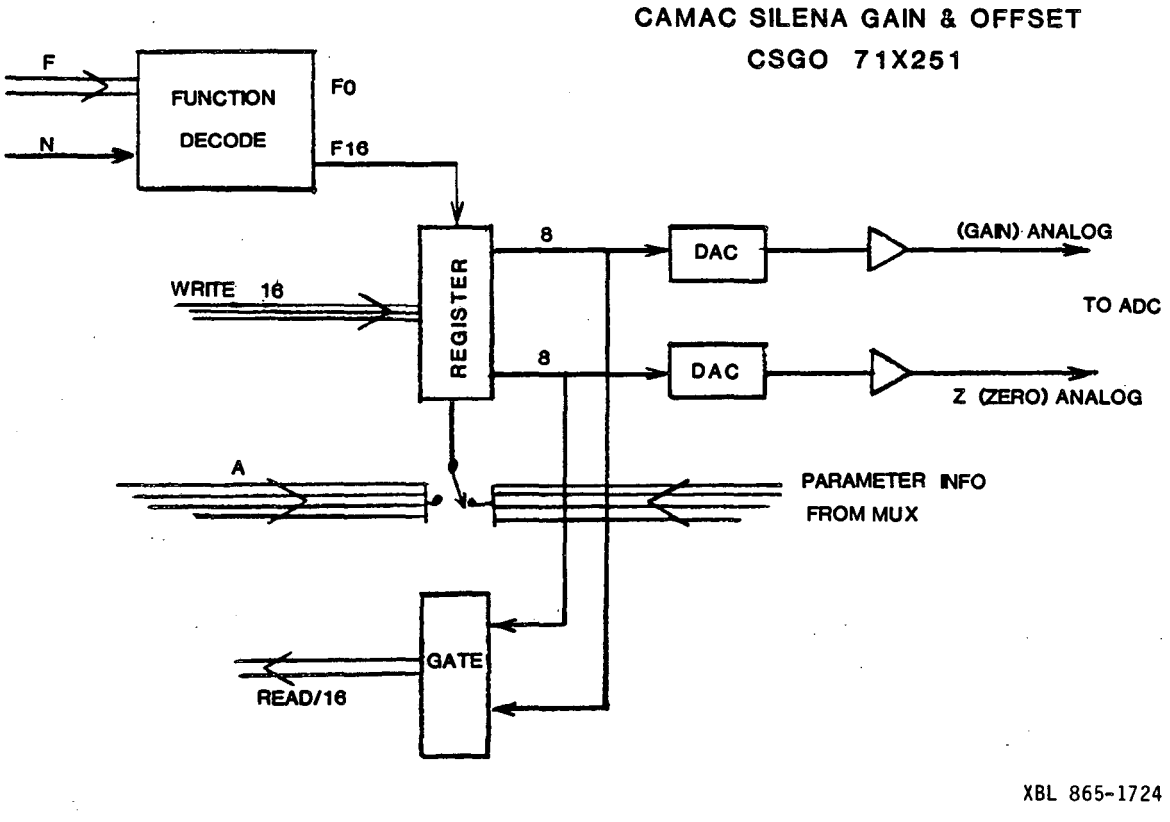


Fig. 6 Silena ADC Gain and Offset Control Module

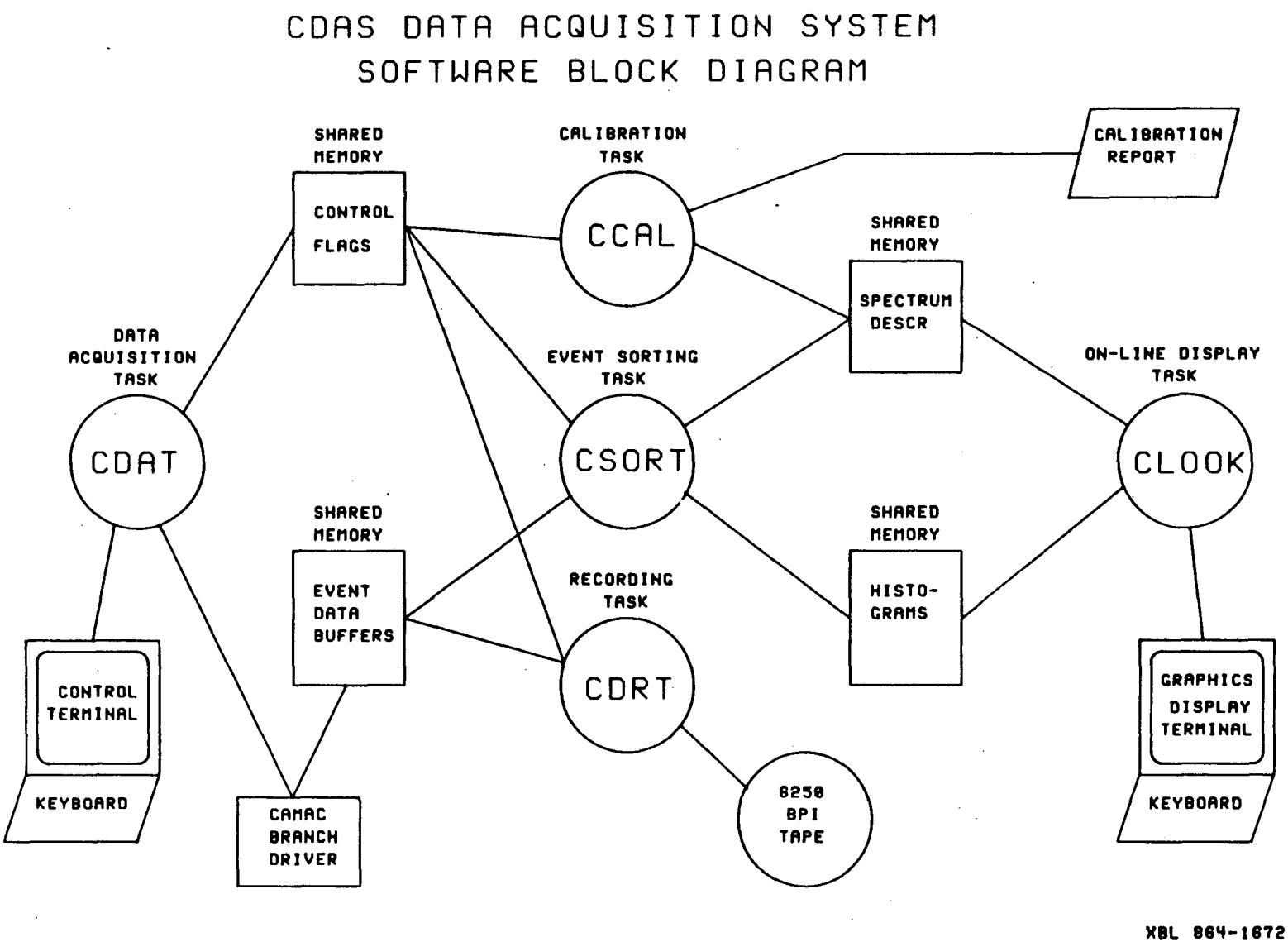


Fig. 7 Software Block Diagram

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